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FOREIGN TECHNOLOGY DIVISION

ON CONSTRUCTION OF SERIAL-PARALLEL DIGITAL-DIFFERENTIAL ANALYZER

by

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ABSTRACT: The digital differential analyzer proposed in the article contains only one integral, which assumes in succession during each integration step the role of all the necessary integrators; however, the information in the digital integrator is processed not sequentially, but in parallel code. Its advantages are claimed to be higher operating speed than possessed by the sequential-sequential differential analyzer, approaching the speed of the parallel-sequential operation (where there are many integrators as are required for the solution of the problem), but requiring much less equipment. The author discusses the possible block diagram of such an analyzer, the parallel-type digital integrator employed, the various individual circuit elements, and the scheme whereby the increments of the integrand are generated. Orig. art. has: 6 figures and 6 formulas. English Translation: 18 pages.

U. S. BOARD ON GEOGRAPHIC NAMES TRANSLITERATION SYSTEM

Block	Italic	Transliteration	Block	Italic	Transliteration
А а	*А а*	A, a	Р р	*Р р*	R, r
Б б	*Б б*	B, b	С с	*С с*	S, s
В в	*В в*	V, v	Т т	*Т т*	T, t
Г г	*Г г*	G, g	У у	*У у*	U, u
Д д	*Д д*	D, d	Ф ф	*Ф ф*	F, f
Е е	*Е е*	Ye, ye; E, e*	Х х	*Х х*	Kh, kh
Ж ж	*Ж ж*	Zh, zh	Ц ц	*Ц ц*	Ts, ts
З з	*З з*	Z, z	Ч ч	*Ч ч*	Ch, ch
И и	*И и*	I, i	Ш ш	*Ш ш*	Sh, sh
Й й	*Й й*	Y, y	Щ щ	*Щ щ*	Shch, shch
К к	*К к*	K, k	Ъ ъ	*Ъ ъ*	"
Л л	*Л л*	L, l	Ы ы	*Ы ы*	Y, y
М м	*М м*	M, m	Ь ь	*Ь ь*	'
Н н	*Н н*	N, n	Э э	*Э э*	E, e
О о	*О о*	O, o	Ю ю	*Ю ю*	Yu, yu
П п	*П п*	P, p	Я я	*Я я*	Ya, ya

* ye initially, after vowels, and after ъ, ь; e elsewhere. When written as ё in Russian, transliterate as yё or ё. The use of diacritical marks is preferred, but such marks may be omitted when expediency dictates.

ON CONSTRUCTION OF SERIAL-PARALLEL DIGITAL-DIFFERENTIAL ANALYZER

A. V. Kalyayev and R. V. Korobkov

Digital differential analyzers [DDA] (ЦДА) according to principle of construction of logic structure and according to method of data processing in digital integrators, can be divided into four classes: serial-serial, serial-parallel, parallel-serial, and parallel-parallel.

At present in practice are used only two classes of digital-differential analyzers: serial-serial, in which there is one real integrator, executing consecutively the role of all integrators participating in solution of problems (where information in integrators is processed in (serial code), and parallel-serial type, containing as many real parallel-working integrators as are required for solution of assigned range of problems (where information in every integrator is processed, as in the preceding case, in serial code).

Of significant interest besides these two classes of digital-differential analyzers is class of series-parallel digital-differential analyzers, in which there is one integrator, executing consecutively in every step of integration the role of all necessary integrators, while information in digital integrator of similar DDA's is processed not in serial but parallel code.

Serial-parallel digital-differential analyzer is favorably distinguished by the fact that it considerably exceeds in speed of operation the most simple digital-differential analyzer of serial-serial type, vying in this respect the parallel-serial DDA. At the same time, for construction of serial-parallel DDA there is required considerably less equipment than for the construction parallel-serial DDA. These merits of serial-parallel digital-differential analyzers are very significant during use of DDA as control computers.

In this work are considered questions of construction of separate units of digital-differential analyzers of serial-parallel type.

1. Block Diagram of Serial-Parallel DDA

Let us consider basic functions which should be executed by digital-differential analyzer utilized as control machine. First of all, the DDA should be capable of obtaining initial information in the form of initial data, program of solution of problem , and certain criterion in accordance with which program can be corrected in process of work. Further, in the DDA should be provided possibility of obtaining current information about state of object of control and about influences of environment on it.

The DDA should provide possibility, on the basis of available current information and criterion of reprogramming, for correcting program for the purpose of obtaining optimum result of control.

On the basis of corrected program and initial data the DDA should solve necessary problem and produce instructions in the form of numbers. Numerical instructions developed have to be, in necessary cases, converted to continuous form and fed to executive control devices. In the process of work of DDA should have possibility of storing intermediate results and program, and should also be able

to carry out electronic commutation between separate units. Finally, in DDA the possibility should be proceded for operator interference within its work for execution of such operations as preparation of DDA for work, starting, stopping, etc.

The enumerated operations ensues logic structure of the serial-parallel DDA presented in Fig. 1.

Main unit of DDA is parallel digital integrator or arithmetic unit [AU] (АУ), which in every step of integration consecutively processes information of all integrators participating in solution of problem. In the process of work the digital integrator obtains information in the form of programs of commutation Π_x and Π_y, scale packet of pulses M, values of integrand y and remainder of integral S_0, and also in the form of increasements of integrals ΔS of other integrators. As a result of treatments of this information, new values of integrands y and remainders S_0 are issued, which go to memory unit [ZU] (ЗУ). Besides this, in digital integrator are produced values of increments of of integrals ΔS, which are placed in corresponding cells of overflow storage register [RP] (РП). Memory unit ZU serves for storage of program Π_x, Π_y, and M plus intermediate values of y and S_0 appearing process of solution of problem. Parallel codes of program

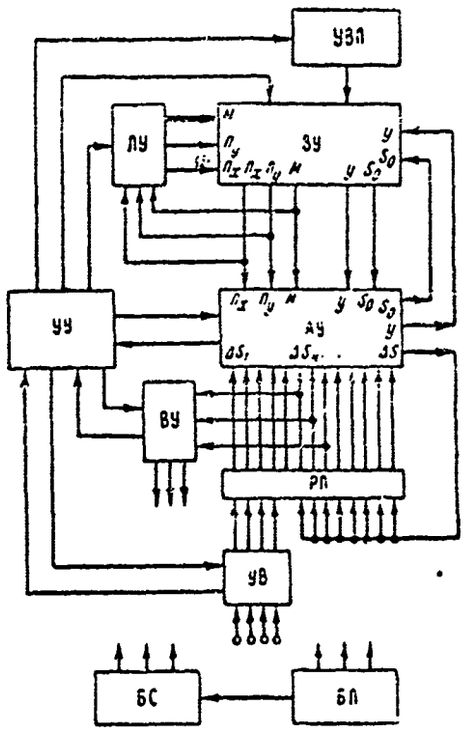

Fig. 1. Block diagram of DDA.

Π_x, Π_y, and M are issued from ZU simultaneously to input of digital integrator [AU] (АУ) and to logic unit [LU] (ЛУ). In logic unit codes of programs can be corrected, after which the corrected program Π_x, Π_y, and M is again transmitted to memory unit for storage and further use. However, in a number of cases work of DDA is possible without correction of program. Here, program is copied and passes through logic unit without changes. Values of Y and S_0 are fed from ZU to input of integrator in parallel code. Some of these values can enter logic unit for evaluation of the course of processing information in accordance with criterion embodied in logic unit.

Overflow storage register RP serves for storage of increments of integrals ΔS calculated in arithmetic unit AU. Increments of integrals ΔS issued after data processing by integrator are placed in corresponding cells of RP. Information from all cells of overflow register is fed, in turn, in parallel code to integrator. Increments of integrals ΔS and program Π_x and Π_y, fed simultaneously to input of integrator, permit forming in it increment of independent variable x and integrand y.

Logic unit LU serves, as was already noted, for correction of program Π_x and Π_y in accordance with criterion embodied in it. Depending upon criterion, structure of logic unit can be different. In the simplest case the logic unit can switch solution of problem can be changed after achievement of some indices of quality of process. Moreover, in the process of solving a problem structure of commutation of integrators used will be changed. In logic unit there can be organized search for the most optimum variants of solution of problem satisiying assigned criteria of quality. For input to memory unit of initial program (Π_x, Π_y, and M) and initial data (y and S_0) serves

program input and initial data unit [UVP] (УВП), with the help of which all initial data are introduced into ZU of DDA automatically. The most rational way to carry out input of data is from wide punched tape.

In the process of solution of problem the DDA should obtain information from controlled object. As a rule, this information is given in the form of continuous quantities (in particular, in the form of voltages). For the purpose of conversion of continuous information proceeding from object to form suitable for use in digital integrator of DDA, in block diagram of DDA (Fig. 1) is an input unit [UV] (УВ). In the input unit continuous quantities are quantized by levels and converted to increments, which are fed to specially allotted cells of overflow storage register. Subsequently these increments are used in integrator as ordinary increments of integrals.

Some of the values worked out as a result of work of DDA have to be fed to actuators, which control object. For this serves special output unit [VU] (ВУ), in which are special counters that store control quantities in digital form. Conversion of these quantities to continuous form is carried out by usual methods. From output of VU unit converted quantities are issued in the form of voltages.

Synchronization of work of separate units of digital-differential analyzer and coordination of them among themselves are carried out with the help of synchronizing pulses and control potentials produced by unit [BS] (БС).

For control under different operating conditions of separate units of DDA and of entire digital-differential analyzer on the whole

serves control unit [UU] (УУ). With the help of control unit is produced input to DDA of initial information, starting and stopping of DDA are carried out, and prophylactic tests of DDA are produced. Control unit is supplied with signalling, facilitating monitoring of work of DDA.

Power supply [BP] (БП) provides for all units of DDA necessary voltages and currents. This unit runs alternating line current.

Basic distinctive pecularity of all units of serial-parallel DDA is that all information in them is transmitted and processed in parallel code, being expanded spatially. In accordance with this, all units of considered DDA are designed on the parallel principle. During the designing of the majority of units of DDA's of this class the shown circumstance causes no special problems. However, during the designing of digital integrator of parallel type serious difficulties appear, which, in essence, prevent propagation of similar computers. In connection with this, we shall dwell in greater detail on the question of designing block diagram of parallel digital integrator and shall show that the difficulties noted are fully surmountable.

2. Digital Integrator of Parallel Type

Block diagram of digital integrator of parallel type is depicted in Fig. 2. Process of digital integration in this circuit takes place in accordance with system of equations:

$$\left.\begin{aligned} &o_{k-1}y\,\frac{[1-(-1)^k]}{2} = R^{-n}\sum\frac{\Delta_{k-1}y}{\Delta y}\cdot\frac{[1-(-1)^k]}{2}\,y_{k+1}\,\frac{[1-(-1)^k]}{2} = \\ &\qquad = (y_{k-1}+\delta_{k-1}y)\cdot\frac{[1-(-1)^k]}{2}, \\ &\left(\frac{\Delta_k S}{\Delta x}+\frac{S_{0k}}{\Delta x}\right)\frac{[1+(-1)^k]}{2} = \left(y_k\,\frac{\Delta_k x}{\Delta x}+\frac{S_{0(k-2)}}{\Delta x}\right)\frac{[1+(-1)^k]}{2}, \\ &\Delta_{k+1}x\,\frac{[1-(-1)^k]}{2} = (x_{k+2}-x_k)\,\frac{[1-(-1)^k]}{2}. \end{aligned}\right\} \qquad (1)$$

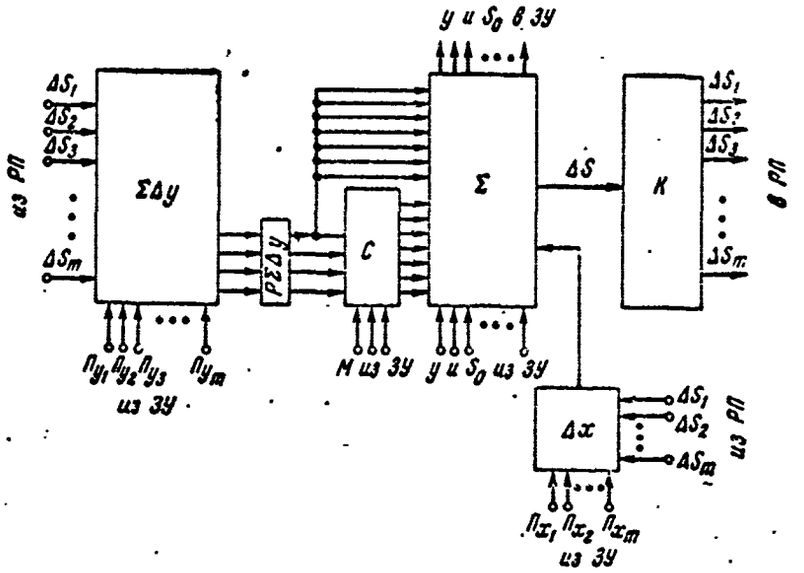

Fig. 2. Block diagram of digital integrator.
KEY: и — and; из — from; в — to.

This system of equations, executing the operation of digital integration, ensures accuracy of integration of the same order as formula of trapezoids. As a result of fulfillment of operations provided by system of equations (1), one step of integration is carried out for one integrator. In accordance with system of equations (1), mathematical operations are executed in every step in two stages, during two elementary intervals of integration. In first odd elementary interval of integration are calculated increments of independent variable $\Delta_{k+1}x$ and integrand $\delta_{k-1}y$ and also the integrand itself y_{k+1}. In second even elementary interval of integration are calculated increment of integral $\Delta_k S$ and remainder of integral S_{0k}. In accordance with considered process of calculations for one step of integration block diagram of digital integrator should contain the following units (Fig. 2). For formation of increment of independent variable $\Delta_{k+1}x$ serves circuit of formation of Δx,

input of which is fed increments of all integrals and program Π_x, and at output is formed value of sought increment. Increment of integrand

$$\delta_{k-1}y = \sum \Delta_{k-1}y \qquad (2)$$

is formed in circuit of $\Sigma\Delta y$, input of which is fed program Π_y and increments of all integrals from overflow storage register [R] (P) For intermediate storage of increment of integrand serves register $\Sigma\Delta y$. Formation of new value of integrand y_{k+1} is produced in adder Σ. For this it first is fed preceding value of integrand y_{k-1} from memory unit ZU, and then, with the help of shifter C, controlled by pulses M from ZU, to corresponding digits of y_{k-1} is added increment $\delta_{k-1}y$. Newly formed value of y_{k+1} is transmitted for storage to ZU and also is kept in adder Σ for further operations. When this is finished odd elementary interval of integration, requiring, as closer examination shows four cycles.

In second even elementary interval of integration to adder Σ is fed increment of independent variable $\Delta_k x$, which can take one of three values: +1.0 or -1. If $\Delta_k x = 1$, the value of y_k stored in adder remains without change. When $\Delta_k x = 0$, adder Σ is set to zero, and when $\Delta_k x = -1$, in adder there forms additional code of y_k. Then from ZU to adder Σ goes preceding value of remainder of integral $S_{0(k-2)}$, which is added to contents of adder. As a result there is formed new value of remainder S_{0k} and increment of integral $\Delta_k S$. Increment of integral $\Delta_k S$ is sent by commutator K for storage to corresponding cell of overflow register RP, and remainder S_{0k} is sent for storage to ZU, after which adder Σ is dumped and step of integration is completed. For realization of first interval, four cycles.

Thus, in all, for fulfillment of one step of integration for one integrator eight cycles are required. For a clock frequency of 2 MHz this will constitute 4 microseconds.

The most complicated element of the considered block diagram of parallel digital integrator is circuit of formation of increment of integrand $\Sigma\Delta y$. On it we shall dwell in greater detail.

3. Circuit of Formation of Increment of Integrand

Increment of integrand in digital integrator is formed as the sum of increments of integrals ΔS of other integrators, outputs of which are connected to input of given integrator. Circuit of commutation of integrators among themselves in serial-parallel DDA is set with the help of program Π_y, consisting of zeroes and ones. A one in j-th cell of program $\Pi_{yj} = 1$ signifies that corresponding increment ΔS_j from overflow register RP should enter into $\Sigma\Delta y$. If, however, $\Pi_{yj} = 0$, increment ΔS_j during formation of $\Sigma\Delta y$ is not considered. In brief, increment of integrand $\delta_{k-1}y$ is formed as follows:

$$\delta_{k-1}y = \sum \Delta_{k-1}y = R^{-n} \sum_{j=1}^{j=m} \frac{\Delta_{k-1}S_j}{\Delta x_j} \Pi_{yj}, \qquad (3)$$

where m – quantity of integrators, n – quantity of y digits in given integrator, R – base of system of calculation.

Thus for calculation of increment of integrand it is necessary to form product of quantity Π_{yj}, entering in program Π_y, and of quantities $\Delta_{k-1}S_j/\Delta x_j$, stored in overflow register, and to add obtained products algebraically. Let us note that Π_{yj} and $\Delta_{k-1}S_j/\Delta x_j$ can take only the following values:

$$\Pi_{yj} = \begin{cases} 1, \\ 0, \end{cases} \quad \frac{\Delta_{k-1}S_j}{\Delta x_j} = \begin{cases} +1 \\ 0, \\ -1, \end{cases} \qquad (4)$$

and their product respectively

$$\Pi_{yj} \cdot \frac{\Delta_{k-1}S_j}{\Delta x_j} = \begin{cases} +1 \\ 0 \\ 1. \end{cases} \qquad (5)$$

In circuit of formation of $\Sigma\Delta y$ it is more convenient to first add positive products (5), then negative, and then in register $R\Sigma\Delta y$ to produce summation of obtained partial values of increments $\Sigma\Delta y = \Sigma + \Delta y + \Sigma - \Delta y$. In accordance with the above, block diagram of circuit of formation of $\Sigma\Delta y$ takes form presented in Fig. 3. Into it enters circuit of formation of positive part of increment of integrand $\Sigma + \Delta y$, circuit of negative part of increment $\Sigma - \Delta y$, and register-adder $\Sigma\Delta y$. Register-adder $R\Sigma\Delta y$ is a most usual parallel adder and we shall not dwell on it. Circuits $\Sigma + \Delta y$ and $\Sigma - \Delta y$ are absolutely identical and therefore it is sufficient to consider construction of one of them. Let us consider circuit $\Sigma + \Delta y$. Unit of formation of $\Sigma + \Delta y$ should accomplish the following. To inputs of unit $\Sigma + \Delta y$ are fed values of ΔS from all m outputs of that part of register RP in which are stored positive values of ΔS and also program Π_y from memory unit. In one or two operating cycles of machine unit $\Sigma + \Delta y$ must sum numerical material stored in cells of register RP designated by program Π_y and issue obtained sum in binary code. With the contemporary level of development of computer technology probably the only possible means of solving given problem is amplitude method of summation, since attempts to solve this problem by logical methods lead to extraordinarily unwieldy circuits.

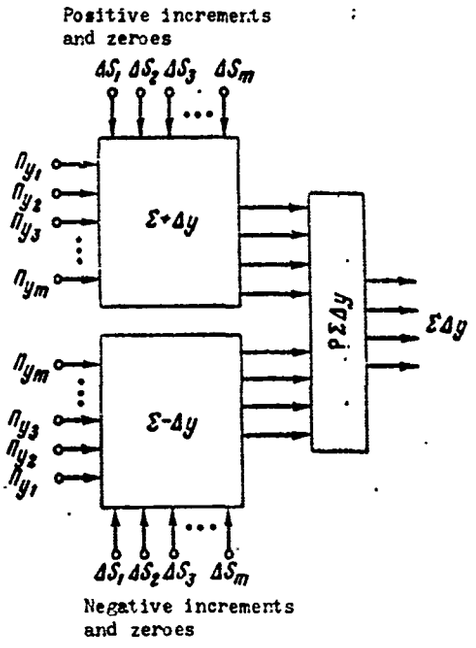

Fig. 3. Circuit of formation of increments.

In Fig. 4 is presented one of possible variants of unit $\Sigma + \Delta y$.

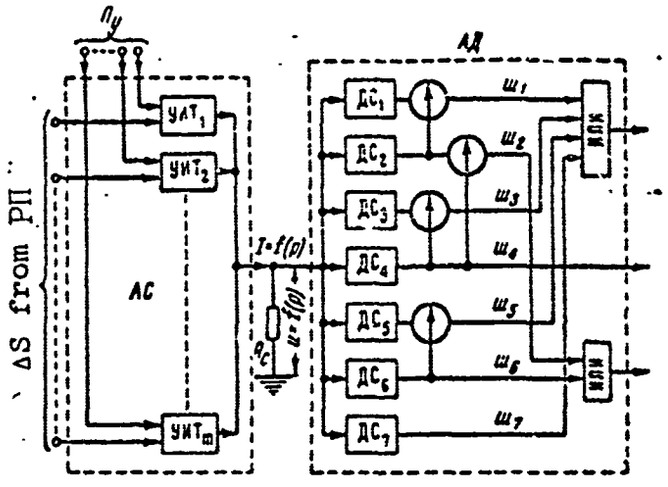

Fig. 4. Variant of circuit of summation unit [ИЛИ = OR]

Give variant, although designed around amplitude method, in realiability is in no way inferior to usual logic circuits. From Fig. 4 one may see that the unit of formation of Σ + Δy consists of two parts: amplitude adder [AS] (АС) and amplitude decoder [AD] (АД) Unit AS produces summation of numerical information stored in cells of register RP designated by program Π_y and issues result in the form of a pulse whose amplitude is proportional to magnitude of sum:

$$u = kp, \qquad (6)$$

where p is number of ones in selected cells of register RP Pulse with amplitude u = kp goes to second part of unit of formation of Σ + Δy – amplitude decoder AD. Amplitude decoder deciphers pulse amplitude and issues obtained sum in binary code.

Conversion of number p pulse with amplitude u = u(p) is produced per principle of summation of currents. Unit AS consists of m controlled sources of current [UIT] (УИТ). Every controlled source of current has two control input: one for program Π_y and a

second for corresponding output of register RP. Current at output of controlled source of current flows only if both of its inputs are fed "one" signal. Upon entry into unit AS of program Π_y and increments ΔS only those sources of current will be opened at whose inputs are signals $\Pi_y = 1$ and $\Delta S = 1$, i.e., number of opened sources of current will be equal to number of ones appearing outputs of register RP designated by program Π. Currents of opened controlled sources of current are summed across resistance R_c. Number of controlled sources of current is equal to number of integrators and can attain 100 and more. With such a large number of sources of current, presence of interference at output of controlled source of current with combinations of input signals of form ($\Pi_y = 1$, $\Delta S = 0$); $\Pi_y = 0$, $\Delta S = 1$) and ($\Pi_y = 0$, $\Delta S = 0$) is not permissible since, being summed across resistance R_c, even very small interferences of 3-5% can be the cause of failures. Current issued by controlled source of current must be strictly constant, not depending on elements of circuit, parameters of which can change. It is easy to show what internal resistance of controlled source of current must satisfy inequality $R_{B\Pi} >> p_{max} \cdot R_c$. Voltage across resistance R_c, formed by current of one controlled source of current Δu, must be sufficient for starting unit AD. So that unit AD works reliably during variation of parameters of transistors or after replacement of transistors, it is necessary that inequality $\Delta u \geq 1$ V be satisfied. It is easy to calculate that emf forming source of current here should be of the order of 200 V. Certainly, requirements imposed on controlled sources of current are high, but creation of them is possible. In Fig. 5 is presented variant of such controlled source of current.

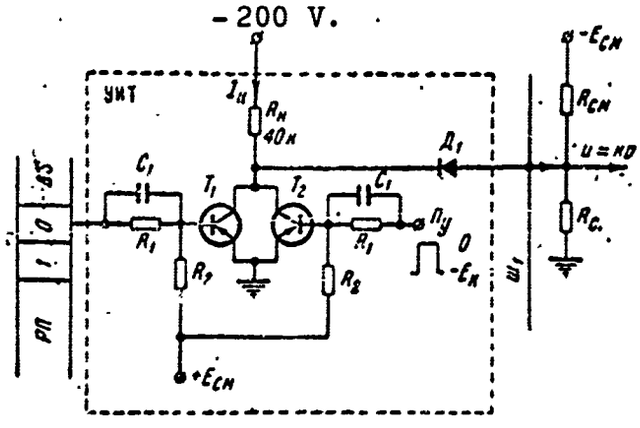

Fig. 5. Variant of circuit of source of current.

Principle of work of given controlled source of current is quite simple. Through resistance R_k always flows current I_k. Depending upon state of transistors T_1 and T_2, it can flow through diode $Д_1$ to resistance R_c (both transistors cut off) or to mass [sic] (when one or both transistors are above cuttoff). Magnitude of this current, with sufficiently large resistance R_k, does not depend on parameters of transistors and diode $Д_1$ but is determined by value of resistance R_k, which can be selected with necessary degree of accuracy. So that current I_k flows to resistance R_c, it is necessary that both transistors T_1 and T_2 be cut off (i.e., that $П_y = 1$ and $\Delta S = 1$). If at least one of the transistors is above cut off, current I_k does not go to resistance R_c. Resistance R_c is fed constant bias $E_{см}$. Necessity for this is caused by the following. Collector voltage of operating transistor u_{k0} does not drop to zero but is 0.3 to 0.5 V. Let us assume that all [UIT's] (УИТ) connected to bus $Ш_1$ are closed and do not issue current I_k to R_c. However, voltage on collectors of transistors T_1 and T_2 will not be equal to zero here. Depending upon parameters of transistors and on number of operating transistors, for different

UIT's this voltage will be different. Let us assume that for some UIT this voltage is maximum. In the absence of bias $-E_{CM}$ this voltage, through diode $Д_1$, goes to resistance R_c and boosts diodes of all remaining UIT's. Through resistance R_c will flow zero current I_{k0}, formed by UIT with maximum u_{k0}. (Current I_{k0} can be formed also by several UIT's with equal u_{k0}.) With income to inputs of one UIT's of signals $П_y = 1$ and $\Delta S = 1$, current I_k of this UIT flows through resistance R_c and voltage across the latter is equal to $I_k R_c$. Since $I R_c > u_{k0\ max}$, flow of current I_{k0} ceases and real increment of voltage across resistance R_c is not $I_k R_c$ $(I_k - I_{k0}) R_c$, i.e., is less. Decrease of pulse amplitude is especially dangerous when $p = 1$. Introduction of bias voltage $-E_{CM}$ removes this danger. Besides this, bias $-E_{CM}$ removes danger of appearance of interference when $p = 0$, $\Delta S = 1$, and $П_y = 0$ for a large number of UIT's. For correct operation of given circuit of UIT coincidence of form and amplitude of input pulses is not mandatory. Circuit also works correctly with pulses of different duration and amplitude.

Thus, selected circuit of unit AS is free from deficiencies inherent to the majority of amplitude circuits. Input pulses need not coincide in form. It is sufficient that pulse ΔS overlap pulse $П_y$, which is ensured without any additional measures. It is necessary to ensure only strictly simultaneous issuance of $П_y$ pulses, which is simple. Amplitude of input pulses can vary within wide limits, remaining, of course, above lower permissible limit. Current issued by controlled source of current is determined by resistance of R_k and does not depend on parameters of transistors and diodes. Resistance of R_k can be selected for sufficient stability and with

necessary degree of accuracy. But dependence of current I_k on supply voltage is kept. However, possibility of appearance of failures from variations of supply voltage can be easily eliminated through proper designing of unit AD (see below). Experimental tests of developed circuit of unit AS showed that unit AS, being extremely simple, is distinguished by high reliability. During assembly of mockup of unit AS were applied transistors П403 and П403А, with range of β from 20 to 120, and diodes Д11 and Д9. In spite of this, work of all sources of current was sufficiently identical. Consequently, during assembly of unit AS there is no necessity for matching of transistors and diodes. Resistance R_k were sorted for precision of ±0.5kΩ. Unit AS causes practically no delay of input pulses (delay time is considerably less than 0.1 microsecond). Form of input pulse is not distorted by unit AS. Voltage drop at outputs of register RP and ZU is fully sufficient for starting unit AS. Through proper selection of input circuits of transistors T_1 and T_2 lower threshold of operation of unit AS can be set for amplitude of input pulses of 2-2.5 V. Amplitude of output pulse is described practically exactly by equation u = kp. Interference at output of unit AS is absent completely during connection to bus ш25 of UIT under the most dangerous conditions, $\Delta S = 1$ and $П_y = 0$. There is no reason to consider that interference appears with a large number of UIT's (for instance, 100 and more). Unit AS works well with frequency of control pulses of up to 2 MHz. At higher frequencies unit AS was not tested. But it is possible to affirm what upper frequency ceiling of unit AS considerably exceeds 2 MHz. Unit AS has no low-frequency limit. Thus, the problem of creation of a simple and reliable device for

conversion of number p to pulse with amplitude u(p) = kp should be considered solved.

Let us consider amplitude decoder AD. Unit AD (Fig. 4) must decipher pulse amplitude u(p) = kp and to issue number p in binary code. Unit AD consists of 7 selectors [DS_1] ($ДС_1$), DS_2, ..., DS_7. Every i-th selector passes an input pulse u(p) only when $p \geq i$, i.e., $DS_i = 1$, with $p \geq i$. At outputs of selectors DS_1, DS_2, DS_3, DS_5 are inhibitor circuits. Therefore on bus $Ш_1$ there will be a pulse only when p = 1, i.e.,

$$Ш_1 = 1 \text{ when } p = 1 \text{ and } Ш_1 = 0 \text{ when } p \neq 1$$

Analogously

$$Ш_2 = 1 \text{ when } p = 2 \text{ and } p = 3$$

$$Ш_2 = 0 \text{ when } p < 2 \text{ and } p > 3$$

$$Ш_3 = 1 \text{ when } p = 3,\ Ш_3 = 0 \text{ when } p \neq 3$$

$$Ш_4 = 1 \text{ when } p \geq 4,\ Ш_4 = 0 \text{ when } p < 4$$

$$Ш_5 = 1 \text{ when } p = 5,\ Ш_5 = 0 \text{ when } p \neq 5$$

$$Ш_6 = 1 \text{ when } p \geq 6,\ Ш_6 = 0 \text{ when } p < 6$$

$$Ш_7 = 1 \text{ when } p = 7,\ Ш_7 = 0 \text{ when } p < 7$$

Busses $Ш_1$, $Ш_3$, $Ш_5$, and $Ш_7$, untied by a buffer circuit, give least significant digit of number p-c. Buses $Ш_2$ and $Ш_6$ give second digit, $П_1$, and bus $Ш_4$ gives third, П. Such logic of work of unit AD permits deciphering number p with least consumption of inhibitor circuits and buffer circuits. For contemporary transistors maximum permissible base-emitter inverse voltage is minute (usually not more than +1 V); therefore it is not possible to construct a sufficiently reliable transistor circuit of selector for unit AD. A sufficiently reliable

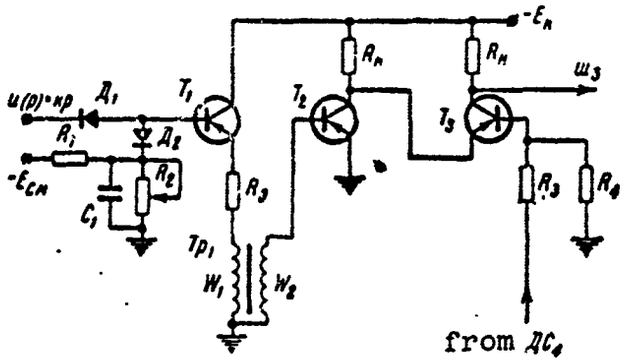

Fig. 6. Circuit of selector

selector can be built around diodes. In Fig. 6 is given circuit of selector DS_3 with inhibitor circuit. The diode selector itself consists of diodes $Д_1$ and $Д_2$ and bias circuit R_1, R_2, C_1. Diode selector is coupled to a two-stage amplifier, containing transistors T_1 and T_2. Coupling between stages is transformer. Application of capacitive coupling is hampered by accumulative effect of d-c charge by capacitor. Inhibitor circuit is built around transistor T_3. Operation of given circuit is quite simple and does not require special explanation. But, let us note its one peculiarity. Earlier it was indicated that pulse amplitude u(p) is proportional to supply voltage. In diode selector is compared amplitude u(p) with reference voltage. So that comparison be unerring it is possible to stabilize power supplies and reference voltage. This is not complicated and does not require large consumption of equipment. However, it is also possible to remove danger of failures without resorting to stabilization of power supplies and reference voltage. Comparison of $u_{оп}$ and u(p) will be unerring not only with strictly constant $u_{оп}$ and u(p) but also if they both change, but change per one law.

For instance, for selector DS_2 $u(1) \leq u_{оп} < u(2)$. If with

variations of voltage of supply circuits $u_{оп}$ and u(p) change proportionally, this inequality always will be satisfied and comparison will always be unerring. In our case it is very simple to obtain identical dependence of $u_{оп}$ and u(p) on voltage of supply circuit. It is sufficient to feed controlled sources of current and bias circuit of selector from one and the same source. But all this, of course, does not signify that supply voltage can vary within any limits. Supply voltage is limited from below by the condition that Δu must be sufficient for starting unit AD. Maximum supply voltage is limited by possibility of breakdown of transistors of unit AS. However, permissible variations of supply voltage can be reduced to ±30%. Experimental investigations of above mentioned circuit of unit AD showed that given circuit, being very simple, is sufficiently reliable. When condition $\Delta u \geq 1$ V is met, unit AD does not require matching of transistors. For mockup of unit AD were used transistors П403 and П403А, without any matching. Delay of pulse by unit AD is 0.4 microseconds. Interferences at outputs of unit AD are insignificant. Mockup of unit AD well works with frequencies of entry of pulses u(p) of up to 2MHz. Tests of unit AD were not conducted at higher frequencies. Summerizing the above-mentioned, we note that offered design of unit $\Sigma + \Delta y$ permits one to solve very simply the problem of formation of increment of independent variable. Unit $\Sigma + \Delta y$ is quite reliable in operation. It imposes no raised requirements on other units (ZU and RP) or supply sources. The mockup of unit $\Sigma + \Delta y$ worked stably during variations of supply voltage within limits of ±20%. Tuning of unit $\Sigma + \Delta y$ is quite simple and is reduced to selection of resistance R_2 of selector. Offered circuit of unit $\Sigma\Delta y$ can be used to frequencies of 2 MHz, and possibly higher.