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A Digitally Controlled Satellite Frequency Synthesizer

J. B. Connolly

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MASSACHUSETTS INSTITUTE OF TECHNOLOGY

LINCOLN LABORATORY

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J. B. CONNOLLY

Group 63

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ABSTRACT

This report considers two well-known methods of frequency synthesis, the VCO approach and the modular or iterative mix-filter-divide approach from the point of view of use in the Lincoln Experimental Satellite (LES) series. System parameters are chosen and a specific implementation is described.

Accepted for the Air Force
Franklin C. Hudson
Chief, Lincoln Laboratory Office

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A DIGITALLY CONTROLLED SATELLITE FREQUENCY SYNTHESIZER

I. INTRODUCTION

In a communications system design in which anti-jam (AJ) protection is desired two well known techniques are generally considered first. These are frequency hopping (FH) and direct sequence, pseudonoise (PN). If the system is such that timing synchronization is difficult then the FH approach may be better suited. A reasonable degree of AJ protection can be provided with the number of possible FH tones in the thousands.

Each frequency must of course be separately generated. The requirement of the generation of thousands of distinct frequencies rules out most classical methods such as multiple oscillators or various types of tuned circuit variations. The problem is best handled by one or more methods of frequency synthesis. This report is devoted to a consideration of the design of a frequency synthesizer suitable for satellite applications, in particular the Lincoln Experimental Satellite (LES) series.

II. INITIAL SATELLITE FREQUENCY SYNTHESIZER REQUIREMENTS

The initial satellite frequency synthesizer design requirements are shown in Figure 1. The first six requirements were determined by the system in which the synthesizer is one of the principal components. Requirements 7, 8 and 9 are a result of the Lincoln Experimental Satellite (LES) series specifications and allocations. The remaining requirements result from orbit conditions and launch plans.

III. SYNTHESIS TECHNIQUE

There are two very powerful frequency synthesis techniques which deserve consideration for this application. They are, for the want of better names, the VCO approach and the modular approach.

A typical block diagram of the VCO approach is shown in Figure 2. The division factor, K, is fixed and the output of the divide by K forms a constant frequency input to the phase detector. The final output frequency, f_o, is

generated by the VCO. It is to be divided by N in a variable pre-set counter. The output from the divide by N is compared with the constant frequency input in the phase detector and a control voltage is developed and sent to the voltage controlled oscillator. The value for N must be equal to or greater than the number of possible output frequencies. This becomes somewhat complex and requires a considerable amount of logic due to the preset requirements. Low power operation dictates that the input frequency to the divide by N counter be reasonably low. Depending on the output frequency, f_o, a combination of down conversion and fixed integer high speed divide may be required. Thus a down conversion local oscillator is required which is conveniently obtained by multiplying f_R by M. Also shown is a fixed high speed divide by L. The system then seeks the following equality.

$$\frac{f_R}{K} = \frac{f_o - Mf_R}{LN}$$

or

$$f_o = (M + \frac{LN}{K}) f_R \qquad (1)$$

Since M, L, K and f_R are fixed, frequency change is accomplished by varying N. This is done by periodically setting the divide by N counter. For a fixed frequency output, f_j, the counter is preset to j and counts to all zeros. The all zero count is detected and the counter set again to j. This presetting must be done between input pulses. If a frequency change from f_j to f_i is desired, then the counter is set to i from whatever state it happens to be in and the counter ripples through to the all zero state where it is set again to i.

The modular approach is shown in block diagram form in Figure 3. The synthesizer consists of a frequency generator and n identical modules, each composed of one stage and one switching network.

From a single frequency standard the frequency generator produces f_o, f_g, and Δf. The frequency f_o feeds only stage 1. Also produced are 2^m frequencies designated $f_g + i_k \Delta f$ where

$$k = 1, 2, 3, \ldots, n$$

and

$$i_k = 0, 1, 2, \ldots, 2^m - 1 \qquad (2)$$

These 2^m equally-spaced frequencies all feed each switching network.

Each switching network receives an independent set of m bits from an external source which uniquely specifies one of the 2^m frequencies. The function of the k-th switching network is to pass only the specified frequency $f_g + i_k \Delta f$ to stage k.

Stage 1 operates on $f_g + i_1 \Delta f$ and f_o so as to produce one of 2^m equally-spaced frequencies. Similarly stage k operates on $f_g + i_k \Delta f$ and the frequency produced by stage k-1 ($k \geq 2$) to produce one of 2^{km} equally-spaced frequencies. Thus the integers m and n are related to the total number of frequencies, N, by the formula

$$mn = \log_2 N \qquad (m, n \geq 1) \qquad (3)$$

Given N, Fig. 3 and the above relationship define a family of frequency synthesizers with each member uniquely specified by an (m, n) pair. Complete families of (m, n) pairs can be easily calculated.

A simple method of realizing each stage of the synthesizer is shown in Figure 4. Following a standard mixing operation the frequency is scaled down by a factor 2^m, which is equal to the number of possible equally-spaced frequencies produced by switching network k. This scaling ensures that the 2^{km} possible frequencies produced by stage k are also equally-spaced. Since all stages are identical, the input and output frequencies of each stage must be approximately equal (i.e., $f_k \approx f_o$) regardless of the values assumed by the indices i_k. Assuming that Δf is sufficiently small, this requirement is satisfied if

$$f_g = (2^m \mp 1) f_o \qquad (4)$$

The choice of sign depends on whether or not the upper or the lower sideband, respectively, is passed by the bandpass filter.

As mentioned, Δf must be sufficiently small to satisfy the requirement that $f_k \approx f_o$. The restriction on Δf depends on f_o, the (m, n) pair, and the condition dictated by general design considerations for implementing bandpass filters, namely, that the passband should be much less than the center frequency of the filter. For stage n, this condition is equivalent to requiring that the range of f_n be much less than the center value of f_n.

Now for a brief comparison of these two approaches, one generally observes that the two techniques complement one another rather than compete. This may be appreciated by considering the following listing of many important characteristics.

(1) Percentage Bandwidth: The modular approach is limited to about 10-20% due to the requirements on filter implementation. The VCO approach may easily cover the range 10-35%, limited only by the range of the VCO.

(2) Switching Speed: The modular approach may easily be designed to switch in several microseconds. The VCO approach, being limited by the phase detector bandwidth is generally limited to several milliseconds.

(3) Spectral Purity: The modular approach can yield 70 db or better spurious suppression; this degree of purity, however, requires great pains in fabrication design and exacting filters. On the other hand, the VCO approach much more naturally delivers spectral purity in excess of 70 db with the exception of plus and minus multiples of the phase detector frequency centered on the output. These might be only 50 db down.

(4) Frequency Spacing: The spacing may be decreased to the point where the reference oscillator instability begins to mask the nominal output frequency from its nearest neighbors in the modular approach. However, in the VCO approach, the minimum frequency spacing is a function of the phase detector sampling frequency and the resulting VCO short term stability.

(5) Size and Weight: In an application where both approaches could be reasonably used, that is all other things being equal, the VCO approach could be between 1/2 and 3/4 the size and weight of the modular approach due to the relative number of filters required.

(6) Power Consumption: Again, all other things being equal, the power consumptions would be approximately equal. This is so even with the disparity in circuits because the extra circuitry in the modular approach consists mostly of passive filters.

(7) Parts Count: In similar applications, with all other things equal, the VCO approach might require only 80% of the number of parts which the modular approach might require.

(8) Flexibility: The number of frequencies and frequency spacing are relatively easy to change with the modular approach. Similar changes in the VCO approach would require a fresh design.

(9) Environment Sensitivity: This includes radiation effects, r.f.i., voltage margins and regulation. The two approaches probably could be rated 5 to 1 in favor of the modular approach.

(10) Operations: The modular approach is far simpler to trouble shoot and debug due to its serial nature.

In summary then it may be said that a typical modular synthesizer is distinguished by very fast switching times and densely spaced frequencies. The VCO synthesizer can operate at relatively high percentage bandwidths and has good spectral purity. On the other hand, the modular synthesizer operates at a lower percentage bandwidth, is more complex, and inherently generates spurious signals; while the VCO synthesizer has much slower switching times. The modular approach is much more amenable to changes than the VCO approach; because of its modular character it is probably simpler to design than the VCO type. After considering these fundamental differences and the specific requirements of the LES program, the modular type synthesizer was chosen to realize the requirements shown in Figure 1.

IV. DESIGN CONSIDERATIONS FOR THE MODULAR SYNTHESIZER

The type chosen for this LES application is based on a modular approach. This approach, also referred to as the iterative mix-filter-and-divide type, is used in various types of commercial equipment and has achieved great success in the Lincoln Experimental Terminal (LET) program. The synthesizer characteristics in the satellite application are different than in the other uses. The environment of a space vehicle also creates unusual requirements.

Figure 1 shows the required synthesizer characteristics. The first set results from system considerations. In essence the remaining ones imply that the switching speed be modest, the spurious suppression be quite high, the volume small and the d. c. power consumption be quite low. Previous designs using the same approach have in general emphasized high speed switching more or less to the exclusion of these other characteristics. For this application we must have a synthesizer which simultaneously possesses all of these characteristics and which also is operable over a broad temperature range even in the presence of damaging radiation. It must be mechanically designed to withstand the stresses of a Titan 3-C launch and must also be built using reliable components.

Consider the parameters of the synthesizer as shown in Figure 3, let the number of frequencies, N, be equal to $4096 = 2^{12}$, then from (3) a family of (m, n) may be calculated as shown below.

$$mn = \log_2 2^{12} = 12 \tag{5}$$

m	n
12	1
6	2
4	3
3	4
2	6
1	12

where the frequency generator generates $2^m = 1$ frequencies and there are n modules. Weighing the complexities of each case, it was decided to use a series of six, divide-by-four modules with five frequencies from the frequency generator to produce one of N = 4096 possible frequencies spaced at 100 Hz intervals within a total available bandwidth of about 410 kHz. Figure 5 shows the conceptual block diagram of this arrangement, m = 2, n = 6.

Figure 6 shows the block diagram of an iterated module. The comb of frequencies is sent to the module along with a number of digital inputs. The r.f. gate does the selection of the particular comb frequency determined by the digital inputs. A power amplifier is used to raise the level of the signal selected in the r.f. gate such that it can act as the local oscillator for the balanced mixer. The other mixer input is the output from the previous stage. The mixer drives a bandpass filter, an amplifier, a divider and a lowpass filter. The output from the lowpass filter is the input to the following stage. The bandpass filter may select either the upper or the lower sideband in the mixer output.

Observe that if there is any feedthrough in the r.f. gate this feedthrough will immediately give rise to an inband spurious signal. No amount of filtering will eliminate this spurious signal. For most of the circuits which would be considered as being useful for an r.f. gate, feedthrough will arise primarily due to capacitance appearing between input and output. This capacitance can of course be minimized, but the situation can also be helped by choosing the input frequencies as low as possible. The ability to do this is enhanced if it is required that the bandpass filter select the upper sideband. This allows the frequencies passing through the r.f. gate to be as low as possible.

In addition it is observed that in order to minimize size and weight it is convenient to make maximum use of commercially available integrated circuits, certainly for the divide by four and hopefully for some of the amplifiers. A survey of what is available on the market indicates that operating frequencies must be less than about 8-10 MHz. This is required because at frequencies higher than about 10 MHz the digital circuit power consumption begins to become unreasonable and also amplifier gains begin to fall off drastically.

A lower bound for the operating frequencies is determined primarily by the switching speed specification. For an iterated frequency synthesizer the switching speed is primarily the sum of the delay times associated with each module. This is essentially determined by the delays of the filters included in each module. The specification in this application can easily be met if the

filter bandwidths all are in excess of about 100 kHz. Now for reasonable filter rolloff characteristics consistent with the spurious specification it is required that the operating frequencies be between 1 and 8 MHz and preferably as low as possible. Specific frequencies may be chosen with two things in mind. First the system bandwidth and spacing requirements and second that the frequencies must give rise to a simple frequency generator design. The nominal input and output frequency, f_o, of the iterated modules was chosen to be 1.024 MHz.

Figure 7 shows the rest of the frequencies which are compatible with this particular choice of f_o for a divide by four upper sideband system. Using (4) for an upper sideband system we have that

$$f_g = (2^2 - 1) f_o \tag{6}$$

or

$$f_g = 3f_o \tag{7}$$

Thus f_g equals 3.072 MHz. The comb frequency spacing, Δf, was chosen such that

$$\Delta f << f_o \tag{8}$$

or

$$\Delta f = \frac{1}{10} f_o \tag{9}$$

Thus Δf equals 102.4 kHz.

Module one has four output frequencies available from it. However, each one of those output frequencies gives rise to four more output frequencies from module two. Similarly each additional module multiplies the number of available output frequencies by four until from the sixth module these are 4,096 distinct output frequencies.

A straight forward frequency generator design is a definite requirement and obviously the simplicity of this design depends on the choice of frequencies. The particular choices made here result in a comb generator design

shown in Figure 8. A crystal oscillator at 3.072 MHz is used as the lowest comb frequency. A divide by three yields 1.024 MHz, the input to the first module. A further division of ten yields 102.4 kHz which is mixed with the crystal oscillator frequency. The output of the mixer is then sent to three narrowband crystal filters spaced 102.4 kHz apart.

V. OUTPUT FORMAT

The system application for this synthesizer requires the frequencies to be in a range substantially different from the present band. Since a frequency upconverter is utilized for this it makes little sense to have a divider in the sixth module. In its place is an amplifier providing a 50 ohm, 0 dbm output signal in the band 4,096,000 Hz to 4,505,500 Hz. It may easily be verified that the expression for the output frequency from the sixth state is

$$f_{out} = 4f_o + \Delta f \left[i_6 + \frac{i_5}{4} + \frac{i_4}{16} + \frac{i_3}{64} + \frac{i_2}{256} + \frac{i_1}{1024} \right] = 4f_o + \Delta FSN \qquad (10)$$

where $i_k = 0, 1, 2, 3$; $4f_o = 4,096,000$; and $\Delta f = 102,400$ Hz.

The values of i_k are determined by taking 6 adjacent 2 bit pairs of the 12-bit binary command. As the 12-bit number is increased, a corresponding increase is produced in the output frequency. When the least significant bit alone changes from 0 to 1, the output frequency increases by 100 Hz. When the most significant bit alone changes from 0 to 1, the output frequency increases by 102.4 kHz. Other bit changes produce frequency increments in proportion to a strict binary progression as shown in the following equation and in Figure 9.

$$f_{out} = 4f_o + \Delta f \left[i_6 + \frac{i_5}{4} + \frac{i_4}{16} + \frac{i_3}{64} + \frac{i_2}{256} + \frac{i_1}{1024} \right]$$

4,096,000 Hz

102,400 Hz

Adjusts in steps of 102.4kHz 25.6kHz 6.4kHz 1.6kHz 400 Hz 100 Hz

The bandwidth and frequency separation in each module is shown in Figure 10.

VI. CIRCUIT IMPLEMENTATION

The objectives of an implementation of a frequency synthesizer suitable for satellite applications and possessing the characteristics previously described are to demonstrate that: (a) the design considerations are valid and (b) that from an equipment point of view such a synthesizer can, in fact, be built.

The circuit implementation for this frequency synthesizer can be best characterized as conservative. High reliability components were chosen throughout and circuit design was done with the thought that the unit was expected to operate many thousands of hours in space. No simplifications, reduction in either components or power consumption were knowingly made which conceivably could make the long-term reliable operation of the synthesizer marginal.

First, consider the circuit implementation of the block diagram of Figure 6. The r.f. gate is shown in Figure 11. The gate consists of four single pole single throw switches and an integrated circuit post-amplifier. The switch design is a diode implemented attenuator. The switch is closed if the diodes on the top of the TEE are turned on, this requires a negative control voltage. The switch is open if the top diodes are turned off and this requires a positive control voltage. The importance of a spurious signal in the output resulting from capacitive feedthrough in the r.f. gate has been emphasized earlier. Thus, the diodes have to be chosen to have extremely low capacitances, FD 700 diodes are used. In order to minimize the d.c. power consumption the bias resistors and the control voltages were chosen such that the forward bias current is only about 1 ma. This biases the diodes just slightly above the diode characteristic knee on the low resistance portion of the curve. Reverse bias voltage levels are only several volts. Such a biasing scheme requires a total of about 20 mw of power from the four control voltages and yields on off ratios for each switch in excess of about 70 db.

The integrated circuit postamplifier, the Philco PA713, uses about 18 mw and is required since the r.f. levels at the inputs to the diode circuits are low so that the diodes will operate in the small signal mode.

The packaging of the r.f. gate circuit is quite important also, not only from the point of view of achieving small size and weight but also because of the cross talk and feedthrough problem and the spurious which might result in the output. As is seen in Figure 12, the basic construction is an H-frame rail with two switches on either side of the H-frame bar. The two switches on the same side of the H-frame bar are separated by the space occupied by the integrated circuit. On the reverse side the space is occupied by decoupling elements. For the switches which are back to back the bar in the H has been made a solid ground.

The r.f. gate requires control voltages which are both positive and negative. These are determined by a low data rate digital sub-system implemented using low power digital circuitry. The low power digital circuitry does not have sufficient drive capability so an interface circuit is required. It is a complementary transistor circuit using Darlington connections in order to supply logical gain. The packaging system shown in Figure 13 is a four component deep, cordwood module. It is approximately the same length as the r.f. gate and includes the four level shift drivers required for one r.f. gate.

The r.f. gate drives the power amplifier which drives the mixer. This amplifier must match the mixer impedance, have relatively good gain and be reasonably free from distortion which could cause harmful intermodulation products. The circuit used consists of an emitter follower, used as an impedance transformer, and a common emitter amplifier inductively coupled into the mixer. The circuit consumes approximately 60 mw of power and has power gain of about 30 db. The construction is similar to that of the level shift driver, namely, a four component deep cordwood module.

The balanced mixer is a four-diode and two-transformer ring modulator. The transformers are carefully wound double-plated ferrites and the diodes are matched closely. The entire mixer is packaged in a small box. Each mixer is carefully measured to check the intermodulation products. Seventh order intermodulation products were calculated to see the contribution to in-band spurious. The L.O. power at the comb frequency is approximately

+4 dbm as supplied from the power amplifier. The signal at about 1 MHz, supplied from the low pass filter of the previous stage, is applied to the diodes at a level of about -15 dbm. These drive levels are sufficient to keep both in-band and near-in-band spurious signals down to an acceptable level. The output, taken from the second transformer at about 4 MHz, is down from the input by about 8-9 db.

The bandpass filter characteristic is shown in Figure 14. The in-band ripple, shown flat, is actually closer to 1 db, the important sections of the characteristic are the skirt roll-off attenuation and stop-band attenuation. These were selected as a result of the spurious analysis and the mixer characteristics indicated above. The filters are standard L-C type designs and are packaged in boxes.

The saturating amplifier consists of an impedance matching emitter follower and a cascade of two linear integrated circuit amplifiers. The second amplifier is essentially saturated and acts as a squaring device. The linear amplifiers are the same as those in the r.f. gate, Philco PA 713, and use about 18 mw each. The divide by four circuitry is digital; Signetics SJ 424 flip-flops are used. There are two flip-flops per integrated circuit package, thus only one package is required. The flip-flops feed an emitter follower which impedance matches to the low-pass filters. The entire circuit, saturating amplifier and divide by four including both emitter followers consumes about 70 mw of power and is packaged in a four component deep cordwood module.

The low-pass filter with the characteristic shown in Figure 15 is also a standard design and is packaged in a box. The roll-off characteristic was chosen in conjunction with the spurious signal problem previously discussed and so that the second harmonic (which is naturally low in the flip-flop square wave output) and the third harmonic are sufficiently low in the input to the next mixer.

The six modules were arranged on printed circuit boards, two modules per board. An experimental test set-up of the six modules is shown in

Figure 16. The boards are identical and on each board, the various boxes were strategically placed so as to more-or-less electrically wall off various sections of each module and to separate the two modules. The test wiring harness carries the control signals (commands) and the 1 MHz input and output. Power is distributed via the brass pins on both edges. In this experimental test set-up the distance between boards is twice the normal distance to allow for small right angle coaxial connectors to function as the distribution buss for the frequency comb. In a final model this connector would be replaced by shielded brass pins having the same external appearance as the power distribution pins.

Now consider the circuits in the frequency generator shown in Figure 8. The reference crystal oscillator is of the temperature compensated variety, with temperature stability of about 1.5 parts per million over the range $-30^{o}C$ to $+40^{o}C$. Two outputs are provided separated by a buffer amplifier and a filter. The oscillator frequency was chosen at $f_1 = 3,072,000$ Hz and it uses about 70 mw at +12 volts.

The nominal input frequency to the first module, f_o, is obtained by digitally dividing by three using a simple shift register counter implemented with Signetics SJ family circuits. An emitter follower and low pass filter operate on the signal and a pad sets the proper level for the first mixer. The emitter follower, filter and pad are packaged in a cordwood module set in a box.

The other three frequencies in the comb of four are obtained by crystal filtering the output of an unbalanced mixer whose inputs are $f_g = f_1 = 3,072,000$ Hz and $\Delta f = 102,400$ Hz. The 3,072,000 Hz signal comes directly from the crystal oscillator through an isolation pad. The 102,400 Hz signal is obtained by dividing 1,024,000 Hz by 10 = (5)(2). The divide by five is a simple shift register counter configuration and the divide by two is a single flip-flop. This divide by ten is implemented using the Fairchild 9040 low power DTL family of integrated circuits. It interfaces directly with the TTL used in the divide by three. The 9040 series was selected because of its low power consumption, however, it cannot reliably be used in the divide

by three because of the 3 MHz clock rate.* The complete (÷ 30) divider is packaged in a cordwood module and consumes about 60 mw of dc power.

The 102.4 kHz driver is a transistor switch with a tuned coupling circuit in the collector. The unbalanced mixer is the single diode, three-transformer type. The transformers are tuned. Both mixer input levels and the transformer tuning were accomplished experimentally such that the three signals of interest f_2, f_3, f_4 in the output were maximized and equalized in amplitude.

The amplifier, A_1, is a common collector amplifier with a large amount of emitter degenerative feedback. The three A_2 amplifiers boost the voltage still further and impedance match with the following crystal filters. All these amplifiers were built using cordwood construction techniques.

A typical crystal filter characteristic is shown in Figure 17. They were chosen to attenuate adjacent frequencies by at least 70 db so that they would be at least as effective as the r.f. gate.

Output drive capability is provided by emitter followers and small filters to eliminate the second harmonic of f_2, f_3, and f_4. These units were packaged in cordwood modules and individually sealed in boxes. The entire frequency generator consumes about 210 mw of dc power.

The complete frequency generator is assembled on one printed circuit board of approximately the same size as the module boards. It also serves as a distribution board for dc power and the five frequencies.

When completely assembled in a four-board stack the volume occupied will be about 135 cubic inches and the weight, excluding the wiring harness and cover, will be about 3.4 pounds.

All circuits have been temperature tested and radiation tested. The lumped constant filters and crystal filters have been through shock and vibration tests. A system consisting of six flight-type packaged modules and a printed circuit version of the frequency generator has been operational since about mid-1967. The system has been temperature tested. A summary of pertinent electrical characteristics is shown in Table 1.

*Typical binary clock rate as specified by Fairchild is 2.5 MHz.

TABLE 1

1.	Number of output frequencies	4096
2.	Output level	$\approx$ 0 dbm; 50Ω
3.	Frequency separation	100 Hz
4.	Bandwidth (W)	409, 500 Hz
5.	Band location	4, 096, 000 $\leq$ W $\leq$ 4, 505, 500 Hz
6.	D. C. voltages required	+12, +6, +4, -4 volts
7.	D. C. power consumption (25^{o}C)	$\approx$ 1300 mwatts
8.	Switching speed - not carefully measured but much less than	1 msecond
9.	Frequency stability	Identical to reference oscillator used
10.	Spectral purity*	
	Harmonically related	$\approx$ 30 db down
	Non-harmonically related	
	a. In the band W	One discrete spurious signal was encountered on two of seven measured frequencies at about 73 db down. None on any others.
	b. Outside the band W	Typically, two to six discrete spurious signals were encountered below W and one above W. Worst case ratio was 68 db down in all seven measurements.
	c. Signal to average noise level in band W	Typically greater than 75 db down.
	d. Signal to average noise level outside the band W	Typically greater than 75 db down.

*These preliminary results are based on a measurement of seven of the 4096 frequencies. The measurement consisted of sweeping from 900 kHz to 10 MHz plus harmonics using the Rohde and Schwartz Tuned Microvoltmeter Type USVH with a 500 Hz bandwidth and a dynamic range of about 75 db. Each measurement was checked with the Hewlett Packard Spectrum Analyzer, using a 1 kHz bandwidth and 100 kHz/cm dispersion. At least 200 other frequencies were checked with the spectrum analyzer and no spurious signals within the band W were seen.

VII. CONCLUSIONS

This report considers two frequency synthesis methods from the point of view of satellite operation in an AJ communications system. The satellite model is the Lincoln Experimental Satellite (LES) series. On the basis of performance in a particular application one method, the modular approach, is chosen and the synthesizer parameters are carefully considered. So that the validity of these conclusions may be demonstrated a prototype or feasibility model is described.

The results are encouraging, such validation has been accomplished and the effectiveness of the synthesis methods is much better appreciated. In addition, the circuit design and packaging design problems are more fully understood insofar as their relationship to system performance is concerned.

As regards parameter trade-offs, it is to be recognized that changes in size, weight, and power are strongly dependent on the synthesizer parameters of spurious suppression and switching speed for a given number of output frequencies. Variations in these parameters will allow corresponding variations in the circuit and packaging designs.

VIII. ACKNOWLEDGMENT

Details of the Lincoln Experimental Terminal (LET) frequency synthesizer were generously supplied by B. Hutchinson. Throughout the project the author received the benefit of many technical discussions with B. E. White and R. S. Berg. Their help is gratefully acknowledged. Layout and assembly were skillfully done by J. Doucet.

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3-63-8521

(1) NUMBER OF AVAILABLE OUTPUT FREQUENCIES $\geq 2^{12}$
(2) OUTPUT FREQUENCY SELECTED BY BINARY COMMAND
(3) FREQUENCY SPACING $\leq$ 100 Hz
(4) MUST BE FLEXIBLE $\Longrightarrow$ EASY TO CHANGE FREQUENCY NUMBER AND SPACING
(5) SWITCHING SPEED $\ll$ 1 mSEC
(6) SPURIOUS SUPPRESSION $\geq$ 60 dB
(7) DC POWER CONSUMPTION $<$ 2W
(8) WEIGHT $<$ 5 LB
(9) VOLUME $<$ 100 IN^3
(10) MUST OPERATE OVER TEMPERATURE $-30°C \leq T \leq +40°C$
(11) MUST OPERATE IN RADIATION ENVIRONMENT UP TO $10^{15} EL/CM^2$ FOR 1.5 MeV ELECTRONS
(12) MUST WITHSTAND THE SHOCK AND VIBRATION OF A TITAN 3-C LAUNCH

Fig. 1. Satellite frequency synthesizer requirements.

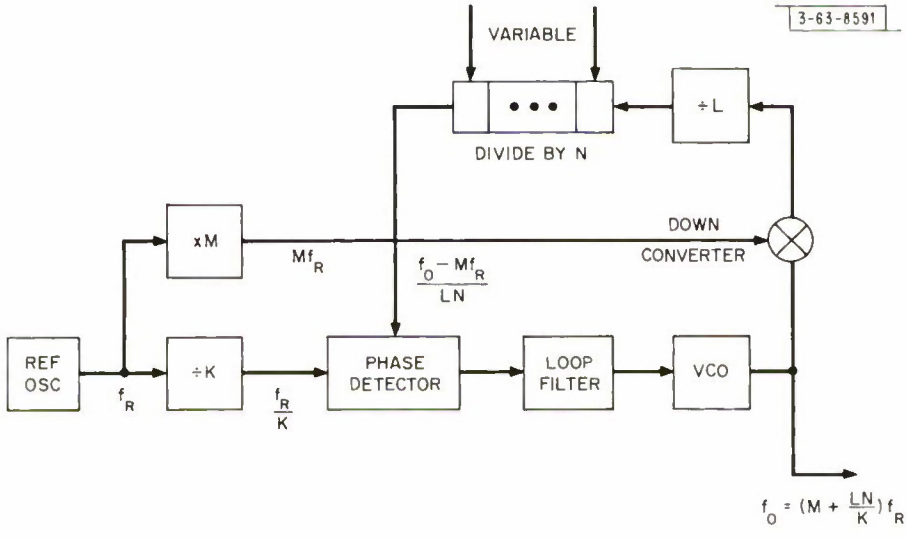

Fig. 2. VCO synthesizer block diagram.

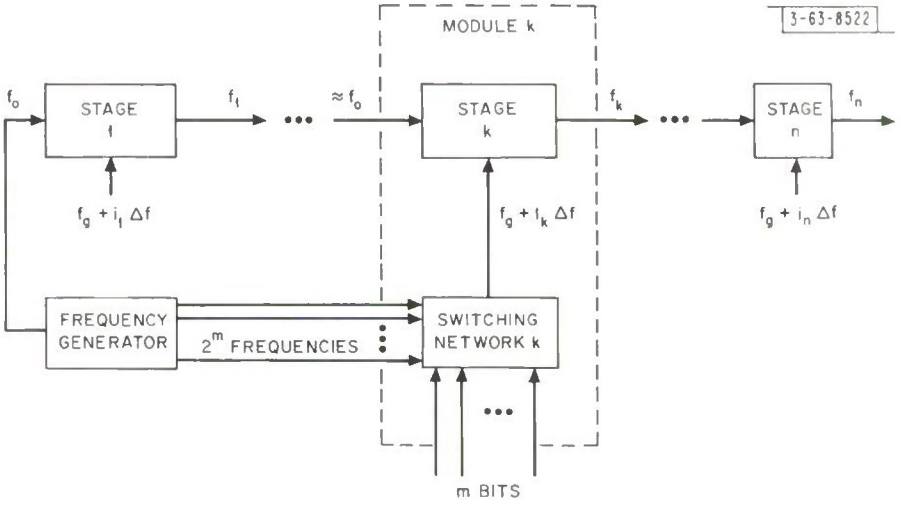

Fig. 3. Modular synthesizer block diagram.

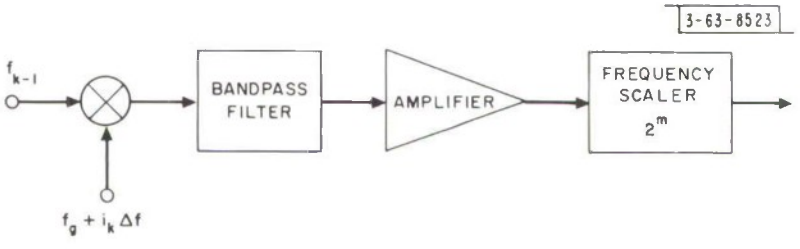

Fig. 4. Module conceptual block diagram.

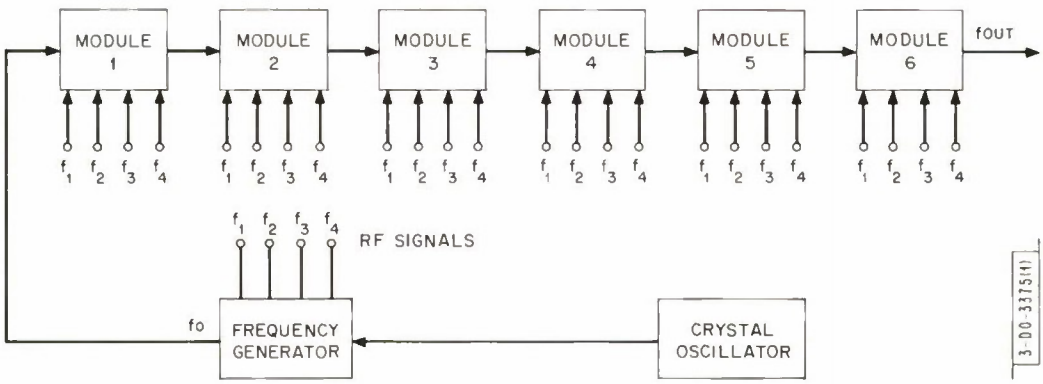

Fig. 5. Conceptual block diagram of modular frequency synthesizer.

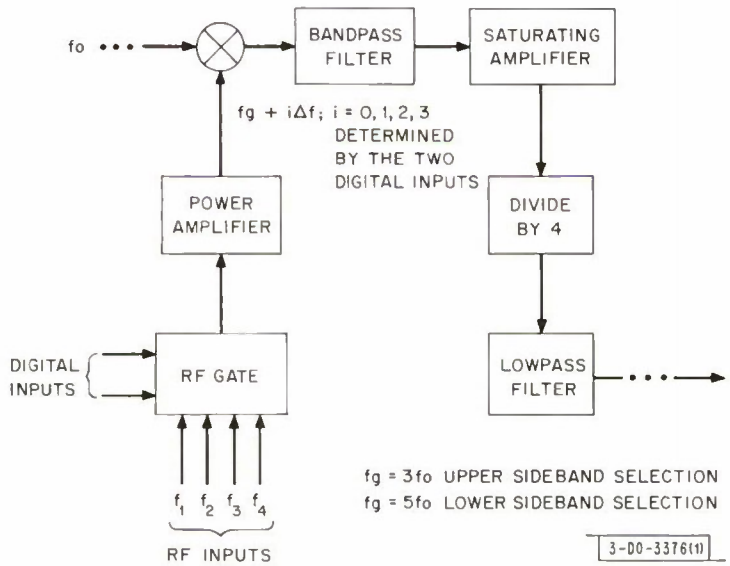

Fig. 6. Interior module of frequency synthesizer.

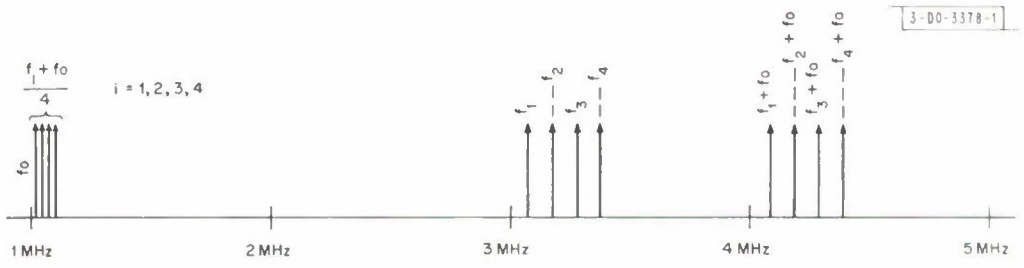

Fig. 7. Modular synthesizer frequency choices and the bands of operation.

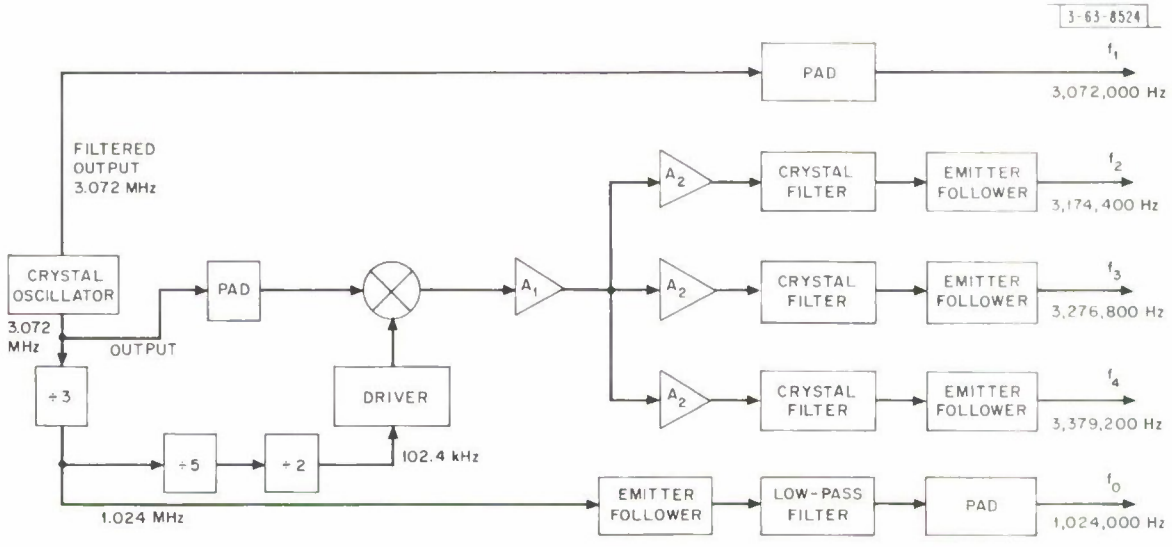

Fig. 8. Frequency generator block diagram.

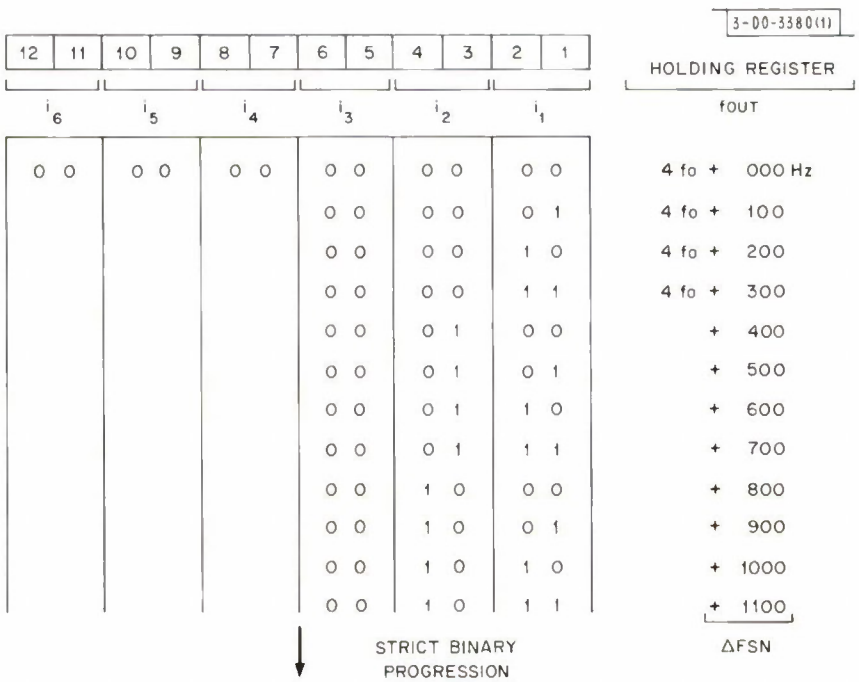

Fig. 9. Output frequency format.

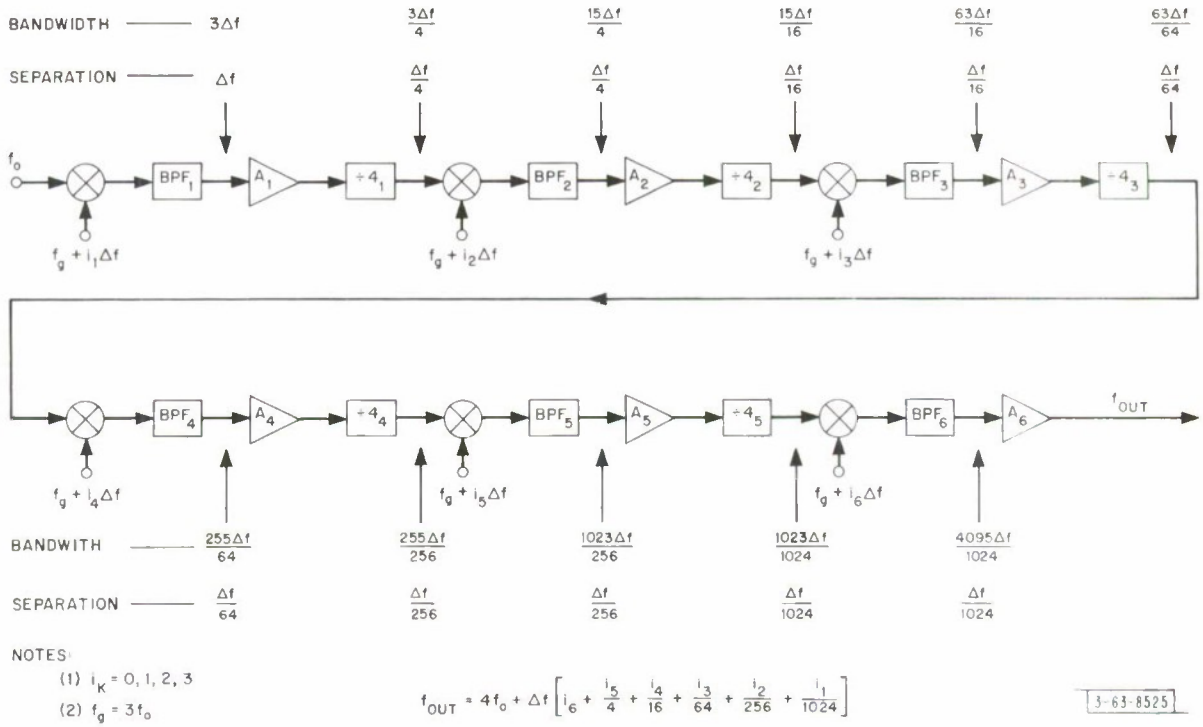

Fig. 10. Bandwidth and separation in the modules.

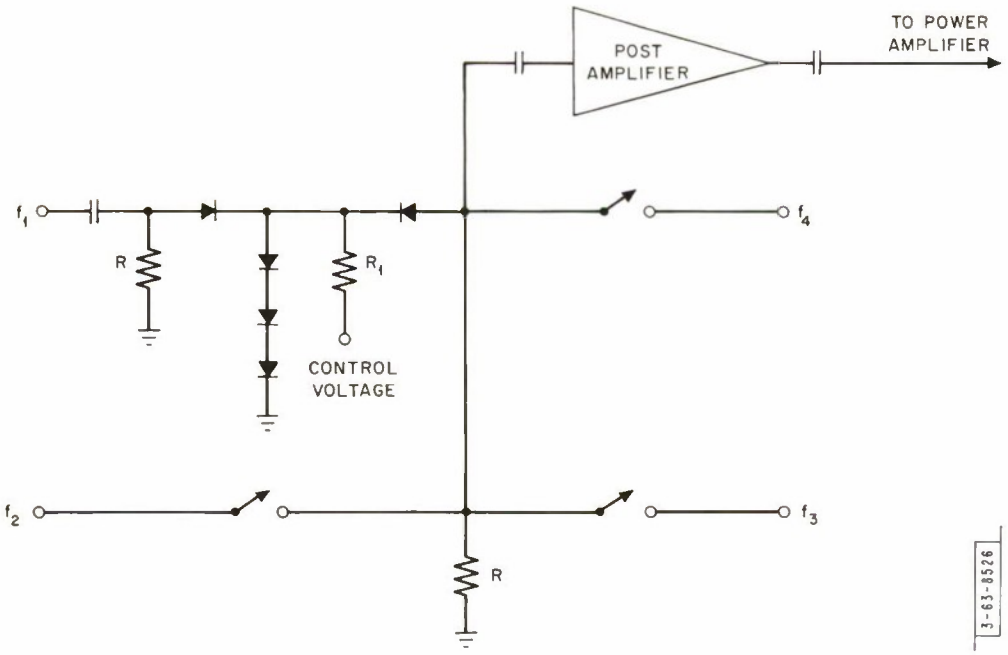

Fig. 11. RF gate diagram.

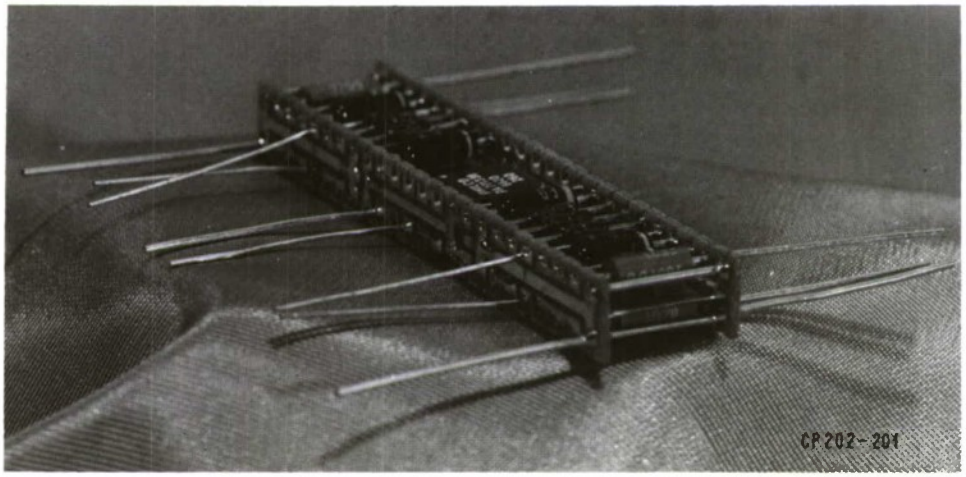

Fig. 12. RF gate circuit module.

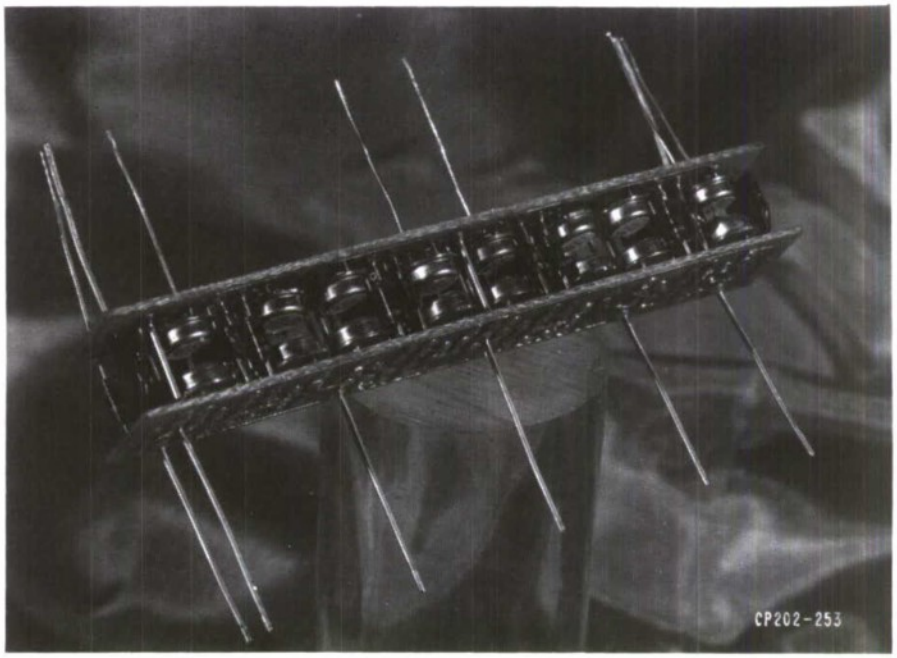

Fig. 13. Level shift driver circuit module.

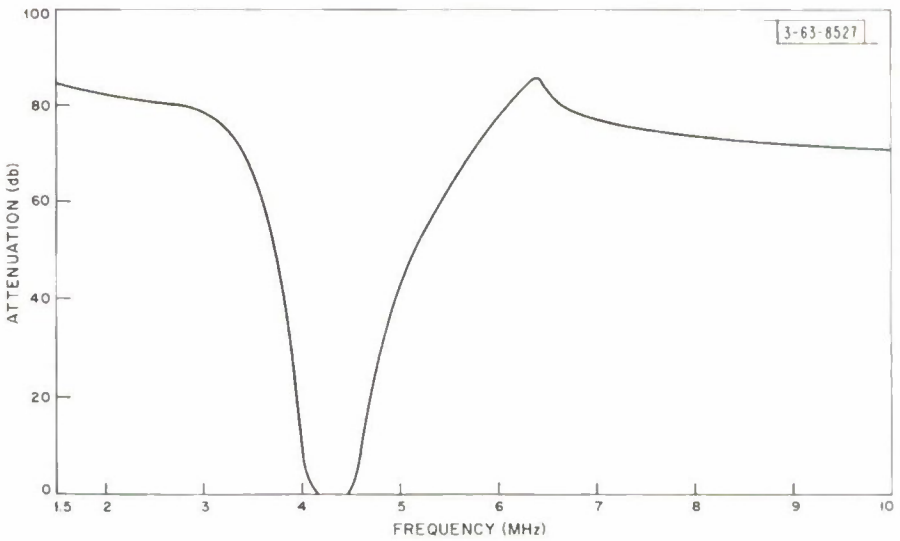

Fig. 14. Band-pass filter characteristic.

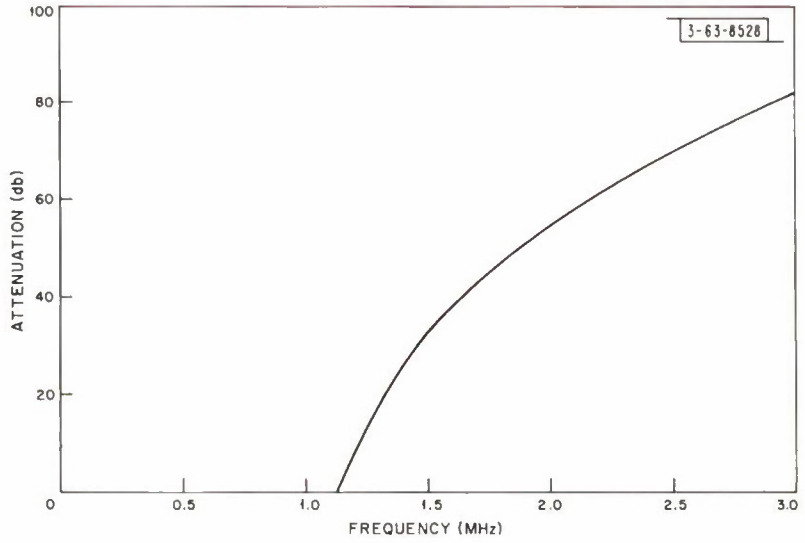

Fig. 15. Low-pass filter characteristic.

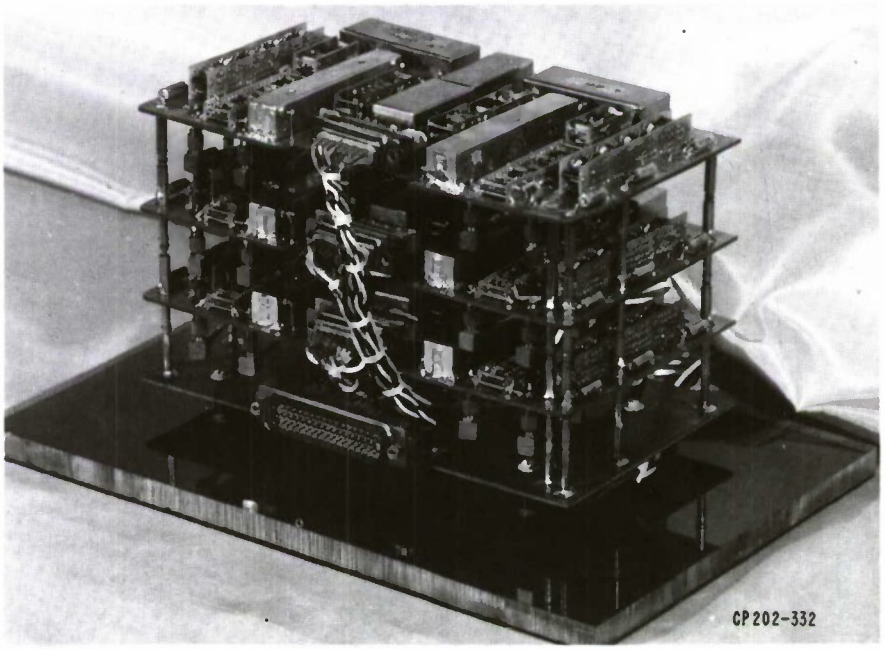

Fig. 16. Six module test stack.

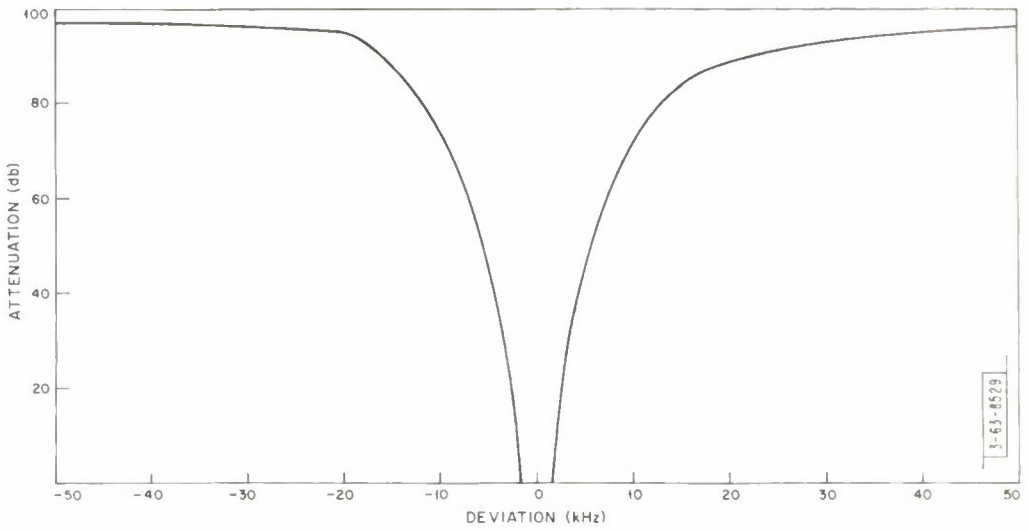

Fig. 17. Crystal band-pass filter characteristic.

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13. ABSTRACT

This report considers two well-known methods of frequency synthesis, the VCO approach and the modular or iterative mix-filter-divide approach from the point of view of use in the Lincoln Experimental Satellite (LES) series. System parameters are chosen and a specific implementation is described.

14. KEY WORDS

voltage regulators
frequency control
frequency modulation
satellite engineering
LES