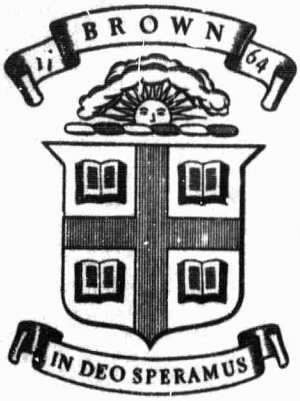

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AN ELECTRONIC SYSTEM FOR MEASURING THE ELECTRICAL CHARACTERISTICS OF NONLINEAR DEVICES

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ABSTRACT

An electronic system for obtaining the electrical characteristics of non-linear devices is described. Three modes of operation provide the I-V curve of the sample and either the differential conductance or resistance as a function of sample bias. A simple feedback system is shown to be particularly advantageous for determining the conductance of low impedance devices. A theoretical analysis provides an algorithm for separating the resistive and reactive components of the sample admittance and gives criteria for conditions of optimum stability and minimum noise. Finally the measured characteristics of a number of devices are shown to illustrate the capability of the instrument.

INTRODUCTION

The discovery of electron tunneling in pn junctions by Esaki in 1957, in superconducting M-I-M structures by Ivar Giaever[1] in 1960 and the observation of phonon structure in tunnel diodes by Hall[2] et al has generated a new and highly active area of endeavour in the study of solids and solid state devices. The experimental aspects of the study of electron tunneling can be divided into three distinct areas: sample fabrication, low temperature cryogenic systems capable of cooling the samples below 1°K, and electronic equipment to obtain the current-voltage characteristics and their first and second derivatives. In this report we shall briefly review the various approaches to differentiation systems that have appeared to date and describe an all electronic, phase locked feedback system capable of providing plots of the current voltage characteristics, and either the incremental conductance $\frac{di}{dv}$ or the incremental resistance $\frac{dv}{di}$ as a function of bias voltage.

The basis upon which all electronic differentiation systems operate is the measurement of the small signal response of the nonlinear element under test while quasistatically sweeping the d.c. bias condition of the element, a technique which has been used for many years for the characterization of electronic devices. The problems encountered in applying this technique to the measurement of the nonlinearity in tunnel junctions are basically dictated by the nature of this nonlinearity or structure itself. Firstly the structure of the current voltage characteristics is highly complex and very "narrow" in the sense that it varies rapidly over d.c. bias ranges of only several millivolts, and hence the measurement often requires a very small sensing signal of the order of microvolts in order to minimize distortion of the incremental parameter to be measured. Secondly, the mag-

nitude of the structure of interest, such as for example the phonon structure in superconducting tunnel junctions and the variety of zero-bias anomalies[3] is often extremely small, representing rapid changes in conductance or resistance of only one or two percent. Therefore, a phase sensitive or lock in detection system is required. Thirdly, the magnitude of the sample impedance of tunnel junctions may range from a fraction of an ohm in superconductor type tunnel junctions to several megohms in some metal-oxide-metal and metal-oxide-semiconductor systems and may consist of both voltage dependent conductive and reactive components. Means should be provided for accommodating such a range of sample impedance, and for separating the conductive and reactive parts. Although no one system is available to cover the entire range of sample impedance, individual systems are now available to provide the required derivatives over the entire range.

Measurement of $\frac{dV}{dI}$ vs V in its simplest form requires external circuitry which will provide a d.c. bias and a high impedance a.c. current source which produces a constant amplitude a.c. sample current ΔI. This in turn produces a variable amplitude a.c. voltage across the test sample $V = \left.\frac{dV}{dI}\right|_{V_{DC}} \Delta I$ which is detected by the lock-in detection system. As long as ΔI remains constant, ΔV and the output from the lock in amplifier will be proportional to $\left.\frac{dV}{dI}\right|_{V=V_{DC}}$. Such a system was described and analyzed by Patterson and Shewchun[4] who show also that synchronous detection with the lock in at the first harmonic of the a.c. current source will provide the quantity $\frac{1}{\left(\frac{dV}{dI}\right)^3_{V_{DC}}} \cdot \left(\frac{d^2I}{dV^2}\right)_{V_{DC}}$ which approaches the second derivative $\frac{d^2I}{dV^2}$ only if $\frac{dv}{dI}$ is slowly varying with d.c. bias. Such a system then can provide $\frac{dV}{dI}$ as a function of bias for sample impedance low enough so that the

constant amplitude requirement on the a.c. sampling current is satisfied over the entire bias range to be investigated (generally less than 10 MΩ). It now becomes obvious that one may easily modify this basic approach to measure $(\frac{dI}{dV})_{V_{DC}}$ for very high impedance samples by providing a low impedance a.c. voltage source ΔV and monitoring the resulting a.c. sample current $\Delta I = \frac{dI}{dV}\Big|_{V_{DC}} \Delta V$. Proper phase selection[5] of the lock in detector also allows relatively simple separation of the conductive and reactive components of the sample impedance with this approach. These systems are both technically and analytically the simplest systems available. It's primary disadvantages are that it cannot provide $(\frac{dI}{dV})$ for low impedance samples and that in the $(\frac{dV}{dI})$ mode of operation, the a.c. sample voltage varies directly with the sample resistance. This can be a serious limitation in the resolution of the equipment, particularly in superconducting tunnel junctions and some zero bias anomalies (giant magnetic anomalies) where the junction resistance increases very rapidly near zero bias. The correspondingly scaled a.c. signal voltage developed across the sample can then obscure considerable detail in the structure of the derivative. As the $\frac{dI}{dV}$ measurement is performed with constant a.c. signal voltage across the sample, it does not present this problem.

$\frac{dI}{dV}$ measurements on low impedance samples have been performed[6], but the external circuitry required to maintain ΔV constant is necessarily more complex and requires some sort of feedback arrangement tc insure the constancy of ΔV . Systems reported to date have all relied on a mechanical servo-motor feedback loop which drives a potentiometer to regulate the magnitude of the a.c. voltage on the sample and to maintain it constant. The

highly nonlinear transfer function has made the analysis of stability criteria very difficult so that the detailed operating characteristics of such systems is not yet completely understood. The attendant problems of mechanical vibrations, added noise due to stray magnetic pickup and potentiometer noise, the added complexity and resulting high price of such systems has led us to develop the electronic differentiation system described below. It is capable of providing continuous plots of I-V, $\frac{dV}{dI}$, and $\frac{dI}{dV}$ curves in impedance ranges not available with the simple systems, with an expanded dynamic range and sensitivity.

In Section 2 we discuss the operation of the system in terms of a block diagram and present the detailed circuit diagrams. Section 3 presents a detailed analysis of the system operation including derivation of the balance conditions, stability criteria, transient response and noise figure. Section 4 gives specific operating recommendations and performance specifications and examples of some typical measurements.

II. PRINCIPLES OF OPERATION

The basic components of the feedback differentiator are the PAR-HR8 lock in amplifier, an operational amplifier (Burr-Brown 1506 or equivalent) and a transistor chopper circuit, along with an attenuator as shown in fig. 1. We consider first its operation in the $\frac{dI}{dV}$ mode, using the block diagram of fig. 1.

Assume first that the set up-operate switch is in the set up position. The feedback loop is now open, and a constant voltage (-1V) is applied to the input of the chopper. The transistor chopper is driven through the chopper amplifier from the "ref. out" terminal or the "cali-

brate" terminal of the HR8 lock in, which is operating in its "internal" mode. The chopped d.c. at the output of the chopper is attenuated and produces a small a.c. sensing voltage on the sample R_D. This sample sensing voltage is then detected by the lock in amplifier which provides a d.c. output voltage V_L proportional to the a.c. sample voltage. The operational amplifier then compares the lock in output voltage V_L with a fixed reference voltage R and provides a d.c. output voltage $e_o = A(R - V_L)$ where A is the gain of the operational amplifier. As the dynamic range of the output of the operational amplifier is limited to $\pm$ 10 volts it will normally be in a saturated state when the system is in the set up position. It is because of the limited dynamic range of the operational amplifier that the set up position is required and its purpose is to allow the operator to select that combination of attenuator setting, R_S, and lock in input sensitivity which will yield a lock in output voltage V_L, approximately equal to the reference voltage R and thus insure that the operational amplifier will operate in a useful portion of its dynamic range.

Let us assume this has been done, and the set up - operate switch is moved to the "operate" position. This now closes the feedback loop, and the d.c. voltage applied to the chopper input is the output voltage of the operational amplifier which then takes on a value such that $V_L \sim R$. This voltage will be maintained regardless of subsequent changes of parameters within the feedback loop. The specific and primary consequence is that the feedback loop will maintain the sensing voltage across the sample R_D constant and independent of the value of R_D. This is the condition required to measure dynamic conductance. The output voltage of the operational amplifier e_o can now be expressed in terms of the a.c. sample current ΔI

or the incremental conductance $(\frac{dI}{dV})$ as follows directly from fig. 1:

$$e_o = \frac{1}{K}(R_S\Delta I + \Delta V) = \frac{R_S\Delta V}{K}[(\frac{dI}{dV}) + \frac{1}{R_S}]$$

where $(\frac{1}{K})$ is the attenuation of the chopper output. The d.c. voltage is thus directly proportional to the dynamic conductance and after being filtered can be directly plotted on an x-y recorder. In normal operation the d.c. bias sweep circuit provides quasistatic biasing conditions on the nonlinear sample to be measured, and the sample conductance is continuously plotted as a function of the sample bias.

Measurement of $(\frac{dV}{dI})$ can be performed in similar fashion if the a.c. sample current is maintained constant. This is accomplished by connecting the input leads of the lock in amplifier (via the function switching block) across the series resistance R_S. In this operating mode the feedback loop operates to maintain the a.c. sample current constant regardless of the magnitude of R_D. Again it follows directly that the d.c. output voltage of the operational amplifier may be expressed as:

$$e_o = \frac{\Delta I}{K}[R_S + (\frac{dV}{dI})] = \frac{\Delta V}{R_S K}[R_S + (\frac{dV}{dI})]$$

Therefore in the $\frac{dV}{dI}$ mode the d.c. output voltage e_o is directly proportional to the dynamic resistance of the sample, and may be plotted as a function of the applied bias.

It should be noted that the series resistance R_S appears both as a scale factor and as an offset term in the $(\frac{dV}{dI})$ mode and in the $(\frac{dI}{dV})$ mode. As the desirable operating conditions are those which maximize the scale factor and minimize the offset term, this requires that $R_S << (\frac{dV}{dI})$

in the $\frac{dV}{dI}$ mode, and $R_S >> (\frac{dI}{dV})$ in the $(\frac{dI}{dV})$ mode. These conditions are the inverse of the conditions required in the conventional differentiator and are one of the characteristics of major importance in the feedback differentiator, because they are naturally satisfied in the measurement of conductivity of arbitrarily low resistance samples, and in the measurement of resistivity of arbitrarily high resistance samples.

The detailed schematic circuit diagram of the system is shown in fig. 2, and will be briefly discussed below in order to clarify the various modes of operation. The four position mode switch selects the mode of operation of the system. In position 1, the current-voltage characteristics are obtained at the X-Y recorder terminals. The sample voltage is measured directly across the sample, while the sample current is obtained on the Y axis by measuring the voltage developed across the series resistor R_S. The lock-in amplifier input is not connected in this mode. The "phase set" position (#2) was provided in order to obtain a reference phase for the lock-in detector, and is required if the sample impedance contains a non-negligible reactive component. The phase reference is the a.c. signal voltage applied across the series combination of R_S and R_D, and in this mode the lock in input terminals are connected across this series combination and the phase control of the lock in is adjusted for maximum d.c. output. The purpose of this set up position will be more clearly defined in the detailed analysis presented in the next section.

In the $(\frac{dI}{dV})$ mode the mode switch connects the lock in input terminals directly across the sample, and also connects a filtered fraction of the d.c. output voltage of the operational amplifier $(\alpha \frac{dI}{dV})$ to the Y channel of the X-Y recorder terminals, through the terminals "0", and "P"

of fig. 2. The filtering is accomplished by the four position R-C filter shown in fig. 2. The actual voltage applied to the output terminals 0 - P is the output of the operational amplifier minus an adjustable offset voltage determined by the ten turn offset potentiometer.

In the $(\frac{dV}{dI})$ mode, the input terminals of the lock-in amplifier are connected across the series resistance R_S while the X and Y channel connections remain unchanged.

The function switch basically provides for a variety of useful input connections for two terminal and four terminal samples, a zero position and a calibrate position. In the "calibrate" position the input terminals are routed to the "R_{cal}," terminals, and the function switch allows direct switching from the sample to a standard resistance for direct calibration of the sample resistance. The "zero" position is an open circuit for the $(\frac{dI}{dV})$ mode and a short circuit for the $(\frac{dV}{dI})$ mode of operation, with the sample disconnected. With these switching arrangements all the necessary connection manipulations can be easily accomplished for measurement of I-V , $\frac{dI}{dV}$ - V , $\frac{dV}{dI}$ - V and their calibration without disturbing the physical connections of the sample and system.

The 3N131 (Crystalonics) chopper transistor is driven through the chopper amplifier from the lock-in "Ref. Out" terminal, or from the "calibrate" terminal. When the lock-in operates in the internal mode, both these terminals provide a signal at the frequency of the lock-in. It should be pointed out here also that the gain of the operational amplifier may be varied from 20 to 40 with the output potentiometer at the rear of the lock-in amplifier, which is not shown in fig. 2. Normal operation is with this potentiometer approximately at mid point with a gain of about 30.

Finally, the reference voltage R referred to earlier is controlled by the 10 k potentiometer shown below the operational amplifier in fig. 2. Values of all capacitors are in microfarads and resistances in ohms unless otherwise specified.

The swept d.c. bias voltage is applied to the sample through the series resistance R_B which is outside the feedback loop and provides an impedance control of the d.c. supply. The schematic circuit diagram for the power supply of the differentiator is shown in fig. 3a. It is Zener diode regulated and supplies the operational amplifier, the chopper amplifier and the required reference and offset voltages.

The d.c. sweep supply is built around an operational amplifier integrator which drives a Harrison Lab. #6823 controllable power-supply-amplifier. The circuit diagram for the integrator, using a Nexus SA-11 operational amplifier is shown in fig. 3b. The power for the integrator is derived from the $\pm$ 20 volt supply of the H-P power supply and all connections to the H-P supply are so made via the terminal strip accessible at the rear of the supply and are identified accordingly in fig. 3b. The integrator is driven by a positive or negative step voltage and gives a positive or negative ramp output with a sweep time of 1, 2, and 5 minutes zero to full scale (20 volts), with vernier control over intermediate ranges. The primary advantage of such a sweep supply, other than convenience, is the elimination of motor driven potentiometers and their inherent noise.

III. ANALYSIS OF THE CIRCUIT OPERATION

Analysis of the operation of the differentiator should answer two distinct questions, the first concerning balance conditions, the second stability conditions. To find the balance conditions as they are modified by a capacitance shunting the diode, it is easiest to work with the simplified block diagrams of fig. 4a and fig. 4b representing the circuit in its $\frac{dI}{dV}$ and $\frac{dV}{dI}$ modes respectively. In these block diagrams, the effect of the lock-in amplifier and of the attenuator between the chopper and the series resistance have been incorporated into the block labeled "phase selector." The property of this block is that its output voltage, e_1, is H times the magnitude that component of the a.c. signal across its input which is a at phase angle ϕ with respect to the output of the chopper. The chopper is understood to give an a.c. output voltage of peak value equal to its input voltage.

Consider the $\frac{dI}{dV}$ mode of fig. 4a. In the usual complex impedance notation the attenuation of the diode and series resistance combination is

$$\frac{R_D}{R_S + R_D + jR_DR_SX} \tag{1}$$

where $X = \omega C = 2\pi f_o C$, f_o is the chopper frequency.

We examine the special cases* of $\phi = 0$ and $\phi = \frac{\pi}{2}$ (it being understood that the direction of ϕ is such that the system is stable at $\phi = \frac{\pi}{2}$). Then we have e_1 equal to He_o times either the real or the imaginary part of (1):

$$e_1 = \frac{He_oR_D(R_S+R_D)}{(R_S+R_D)^2 + (XR_SR_D)^2} \qquad (\phi = 0)$$

$$e_1 = \frac{He_oXR_SR_D^2}{(R_S+R_D)^2 + (R_SR_DX)^2} \qquad (\phi = \tfrac{\pi}{2}) \tag{2}$$

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*For the general case of arbitrary ϕ see the appendix

Since $e_o = A(R - e_1)$, we have

$$e_o = AR \frac{1 + X^2\gamma^2R_S^2}{1 + X^2\gamma^2R_S^2 + HA\gamma} \qquad \phi = 0$$

$$e_o = AR \frac{1 + X^2\gamma^2R_S^2}{1 + X^2\gamma^2R_S^2 + HA\gamma^2R_SX} \qquad \phi = \frac{\pi}{2} \tag{3}$$

where $\gamma = \frac{R_D}{R_S+R_D}$.

Let e_o at $\phi = 0$ be e^o and e_o at $\phi = \frac{\pi}{2}$ be e^π . Then solving (3) gives

$$HA\gamma = \frac{AR-e^o}{e^o}(1 + \eta^2)$$

$$HA\eta\gamma = \frac{AR-e^\pi}{e^\pi}(1 + \eta^2) \tag{4}$$

$$\eta = \frac{AR-e^\pi}{e^\pi} \frac{e^o}{AR-e^o}$$

where $\eta = \gamma R_S X$ is a quantity easily calculated from the measured values of e^o and e^π . Solving (4) for γ gives

$$\gamma = \frac{AR-e^o}{HAe^o}(1 + \eta^2)$$

$$g = \frac{1}{R_D} = \frac{1}{R_S}\left| \frac{HAe^o}{(AR-e^o)(1+\eta^2)} - 1 \right| \tag{5}$$

$$X = \omega C = \frac{\eta HAe^o}{R_S(AR-e^o)(1+\eta^2)}$$

The equations (5) are the balance conditions; but they are still in rather intractable form. Let us first consider the case with no capacitance, i.e. when $\eta = 0$. Also let us assume that $AR >> e^o$, then to terms in second order in e^o

$$g \simeq \frac{1}{V_o R_S}\left[e^o - V_o\right] - \frac{1}{V_o R_S}\left(\frac{e^{o2}}{AR}\right) \qquad (6)$$

where $V_o = \frac{R}{H}$ is the value of e^o when the instrument is being zeroed. In the absence of capacitance the conductance of the diode is linearly proportional to e^o. The system is constructed with A between 20 and 40 depending on the setting of the "output level" control of the lock-in and with R preset to 4 volts. Thus a 5% deviation from linearity will occur between 4 and 8 volts out.

Suppose now that we have some capacitance in the circuit, and suppose further that $AR >> e^o$ and e^π. Then (4) and (5) simplify to

$$\eta = \frac{e^o}{e^\pi}$$

$$g = \frac{1}{R_D} = \frac{1}{V_o R_S}\left[\frac{e^o}{1+\eta^2} - V_o\right] \qquad (7)$$

$$X = \omega C = \frac{1}{V_o R_S}\left[\frac{\eta e^o}{1+\eta^2}\right]$$

where $V_o = \frac{R}{H}$ is still e^o with the instrument zeroed. The equations (7) provide a practical algorithm for separating the resistive and reactive parts of the admittance. They also show that (6) is valid so long as $\left(\frac{e^o}{e^\pi}\right)^2 << 1$.

In practice setting the phase to zero is accomplished by connecting the lock-in input across the output of the attenuator and peaking its response, using the "phase-set"position of the mode switch described earlier. The 90° phase shift is accomplished by simply rotating the bezel of the phase control of the lock-in by one position.

In the $\frac{dV}{dI}$ or resistance mode, analysis of fig. 3b yields as the equivalent of (4)

$$\gamma + X^2\gamma^2R_D^2 = \frac{(AR-e^o)(1+\gamma^2X^2R_D^2)}{HAe^o}$$

$$\gamma^2XR_D^2/R_S = \frac{(AR-e^\pi)(1+\gamma^2X^2R_D^2)}{HAe^\pi} \qquad (8)$$

where γ has been redefined as $\frac{R_S}{R_S+R_D}$. If $X = 0$ and $AR >> e^o$ we have

$$R_D = \frac{R_S}{V_o}(e^o-V_o) - \frac{R_S}{V_o}\frac{e^{o2}}{AR} \qquad (9)$$

Unfortunately there does not seem to be any easy way to solve (8) for X and R_D separately nor to find as simple a criterion for the validity of (9) as was possible for (6).

Figure 5 shows a model of the system which is suitable for analyzing its stability. In this model we have replaced the chopper and the lock-in mixer by simple multipliers which are driven by the same reference voltage, namely $\sin(\omega_o t)$. (Implicit in this is the condition $\phi = 0$.) The transfer function $H(\omega)$ includes the attenuation and phase shift caused by the diode and by the tuned signal amplifier of the lock-in. All filtering of the signal after the mixer stage of the lock-in, including that in the output stage of the lock-in, is included in the transfer function $F(\omega)$.

There are three related questions to be answered by our stability analysis, the most important of which is what loop gain and filter configuration will assume a stable output. It is also desirable to know how fast the system responds to changes in the diode resistance and how large the signal to noise ratio of the system is. All these characteristics are directly related to the loop gain of the system which is calculated by assuming that the feedback loop is broken at point Z (fig. 5) and finding the

ratio of e_o to a voltage fed into the system at Z.

Clearly to find this quantity we need a transfer function to characterize the group of elements enclosed by the dotted line. Let $e_1(\omega)$ be the Fourier transform* of e_1. Then

$$e_2(\omega) = e_1(\omega) * [\frac{1}{2j}(\delta(\omega+\omega_o) - \delta(\omega-\omega_o))]$$

$$e_2(\omega) = \frac{1}{2j}[e_1(\omega-\omega_o) - e_1(\omega+\omega_o)]$$

$$e_3(\omega) = [H(\omega)e_2(\omega)] * [\frac{1}{2j}(\delta(\omega+\omega_o) - \delta(\omega-\omega_o))] = \frac{1}{4} e_1(\omega)(H(\omega-\omega_o) + H(\omega+\omega_o))$$

$$- \frac{1}{4} H(\omega-\omega_o)e_1(\omega-2\omega_o) + H(\omega+\omega_o)e_1(\omega+2\omega_o)) \qquad (10)$$

If $F(\pm 2\omega_o)$ is sufficiently small that $e_o(\omega)$ is non-zero only for $\omega \approx 0$, then the terms of (10) in $e_1(\omega \pm 2\omega_o)$ are non-zero only for $\omega \approx 2\omega_o$. But this region is of no interest as it will be attenuated by F. Therefore

$$e_4 \approx \frac{1}{4}(H(\omega-\omega_o) + H(\omega+\omega_o))\, F(\omega)e_1(\omega)$$

---

* We shall use the Fourier transform pair

$$f(t) = \int_{-\infty}^{\infty} d\omega\, F(\omega)\, e^{j\omega t}$$

$$F(\omega) = \frac{1}{2\pi} \int_{-\infty}^{\infty} dt\, f(t)\, e^{-j\omega t}$$

With this definition of the transform, we have the Fourier transform of a product $f(t)\, g(t)$ given by

$$F * G = \int_{-\infty}^{\infty} F(\omega')\, G(\omega-\omega')d\omega'$$

Suppose $g(t)$ is real, then $G^*(\omega) = G(-\omega)$ and

$$F * G = \int_{-\infty}^{\infty} F(\omega')\, G^*(\omega'-\omega)d\omega'$$

The Fourier transform of $\sin(\omega_o t)$ is $\frac{1}{2j}[\delta(\omega+\omega_o) - \delta(\omega-\omega_o)]$.

The loop gain is then

$$\beta = -\frac{A}{4}\left(H(\omega-\omega_o) + H(\omega+\omega_o)\right) F(\omega)$$

Let α be the DC loop gain: since the form of $F(\omega)$ is always a product of factors of the form $\frac{1}{1+j\omega t}$ we may write

$$\beta = -\alpha\left[\frac{H(\omega-\omega_o) + H(\omega+\omega_o)}{2\mathrm{Re}H(\omega_o)}\right] F(\omega) \qquad (11)$$

It is well known that if the Nyquist plot of $-\beta$ encloses the point (-1) then the system is unstable. Moreover, the nearer it comes to the point -1, even if this point is not actually enclosed, the less stable the system is to small disturbances of its equilibrium. We seek to exhibit β explicitly, so that at least a qualitative understanding of the way its Nyquist plot depends on the parameters of the system may be reached.

In the absence of any capacitance across the diode, $H(\omega)/\mathrm{Re}H(\omega_o)$ is determined solely by the characteristics of the tuned amplifier of the lock-in. This is a Butterworth band pass amplifier (n=1) for which

$$\frac{H(\omega)}{\mathrm{Re}H(\omega_o)} = \frac{j\omega t}{Q(1-\omega^2\tau^2) + j\omega t}$$

where $\tau = \frac{1}{\omega_o}$ and Q is adjustable from 5 to 25 by a control on the front panel of the lock-in. Then

$$\tilde{H}(\omega) = \left[\frac{H(\omega-\omega_o)+H(\omega+\omega_o)}{2\mathrm{Re}H(\omega_o)}\right] = \frac{1}{2}\left[\frac{j(\omega\tau+1)}{Q(2+\omega\tau)\omega\tau+j(\omega\tau+1)} + \frac{j(\omega\tau-1)}{Q(2-\omega\tau)\omega\tau+j(\omega\tau-1)}\right] \qquad (12)$$

$$\beta = -\alpha\tilde{H}(\omega)\, F(\omega)$$

Fig. 6 gives a graphical interpretation of equation (12), and from this graph we may construct the Nyquist plot of β. Suppose that

$F(\omega)$ is a single stage of RC filtering, i.e. $F(\omega) = \frac{1}{1+j\omega\tau_f}$ where τ_f is the time constant of the filter. This corresponds to using only the fixed section at the input of the operational amplifier. The Nyquist plot of $\alpha F(\omega)$ is a circle entirely on the right half plane. The effect of $\tilde{H}$ is to convert this to what is shown in fig. 7a. Notice that this curve can never enclose the point $z = -1$ and, therefore, that the system is always stable. Moreover, so long as the curve lies to the right of the line $X = -\frac{1}{2}$, any noise injected into the system will be reduced in traversing the loop. This condition, which is desirable for reducing noise and overshoot, may be guaranteed by the approximate condition that

$$f_o\tau_f \geq \frac{A\alpha}{3\pi Q} \tag{13}$$

The DC loop gain α can be estimated from $\alpha \simeq \frac{AR}{e_o}$ and is bounded above by AR/V_o.

The derivation of (10) required that $|e_o(\pm 2\omega_o)|$ be small. A criterion for this is that

$$\frac{\alpha}{2(2\pi f_o\tau_f)} \leq 1 . \tag{14}$$

Thus there is a limit to the tradeoff between operating frequency and Q at $Q=5$. Since any feedback system is very sensitive to phase shift in the loop, and since increasing Q adds phase shift to $\tilde{H}$ at low frequencies, it is probably disadvantageous to use a Q greater than 10.

The effect of adding 6 DB/octave or 12 DB/octave filtering from the lock-in to $F(\omega)$ is shown in fig. 7b. Since both these curves can enclose the point -1, stability is a more serious problem, and, therefore, the use of these filters is limited. Only under very noisy conditions

might one wish to use the 6 DB/octave section. In general, its effects are less deleterious the higher the operating frequency and the smaller the loop gain.

The principle source of noise in the system is the preamplifier stage of the lock-in. Its effect can be included by adding a white noise generator of value N to the input of a noiseless lock-in as shown in fig. 8. Since the white noise spectrum is unaltered by chopping, we have, setting $R = 0$,

$$e_N = \frac{N\beta}{\delta(1-\beta)}\left(1 + \frac{R_S}{R_D}\right) \simeq \frac{N\beta}{\delta(1-\beta)}\left(\frac{e^o}{V_o}\right) \tag{15}$$

where δ is the attenuation of the chopped signal before the R_S , R_D network.

A useful definition of the signal to noise ratio is the ratio of the change in equilibrium output voltage for a small fractional change in g (the diode conductance), divided by e_N , i.e. $\frac{S}{N} \alpha \frac{\partial e^o}{\partial g} \cdot \frac{g}{e_N}$. From (6) and (15) we have

$$\frac{S}{N} \alpha V_o\left(1 - \frac{V_o}{e^o}\right) \tag{16}$$

This suggests that the operating range of e^o should be restricted to $e^o > 4V_o$. The best compromise between sensing signal and noise is obtained by using the lock-in on its 200 μv scale which has the best intrinsic signal to noise ratio.

When the lock-in contributes no filtering action to the circuit, one can show that the response to a step function change in R_D is proportional to $(1 - e^{-t/\tau'})$ where $\tau' = \tau_f/\alpha$. As this is usually very short, the actual limitation on step function response is the recorder filter.

Summarizing our results, we have optimum stability conditions if a) no lock-in filter is used; b) Q is set at approximately ten; c) $f_o V_o > \frac{AR}{4\pi\tau_f}$. For our system with the "output level" control of the lock-in fully counter-clockwise, $A = 20$, $\tau_f = 1{,}5$ sec , $R = 4$ volts and $f_o V_o > 4$. For optimum noise conditions the lock-in should be used on its 200 μv scale and e^o should be restricted to values greater than $4V_o$.

IV. SPECIFIC OPERATING RECOMMENDATIONS AND PERFORMANCE SPECIFICATIONS

In the light of the results of the analysis in the previous section and from operating experience, the following operating procedures are suggested as a guide to the proper use of the differentiator.

Initially, the instrument should be found in the set-up condition, with the attenuator setting at maximum attenuation (100:1) and with the mode switch in the I-V position, and should always be left in this condition after completing a measurement.

a) I-V curves.

The first measurement on an unknown sample should be the current-voltage characteristics. These can be plotted directly on the X-Y recorder by choosing values of R_S and Y channel sensitivity to determine the current scale and by adjusting R_B and the bias sweep magnitude to attain the suitable range over which the I-V curves are to be plotted. From the I-V curves both the magnitude and the expected variation of the incremental resistance R_D can then be estimated as an aid to the set up procedure for conductance or resistance measurements.

b) $\frac{dI}{dV}$ - V curves.

The set up procedure should be approximately as follows:

1) Set R_S and $R_B \geq 10\ R_D$ (estimated).

2) Check that the set up-operate switch is in the set-up position and that the attenuator is set at maximum attenuation (100:1).

3) Set the lock-in sensitivity at the desired level (< 500 μv and usually 200 μv), and change the mode switch to "phase-set." Next decrease the attenuator setting until an output reading is obtained on the meter of the lock-in. Then adjust the phase of the lock-in to maximize the output in the negative direction. Now change the mode switch to $\frac{dI}{dV}$ and readjust the attenuator to obtain an output of approximately 0.4 of full scale. If it is known that the reactive component of the sample impedance is small the $\frac{dI}{dV}$ position may be used directly instead of the phase set position when phasing the lock-in amplifier.

4) Switch from set-up condition to operate condition. After a transient the lock-in output will be altered to 0.4 full scale and will remain constant.

5) Adjust output offset, recorder Y – scale sensitivity and sweep time to obtain a suitable conductance scale on the X-Y recorder.

6) Having obtained and plotted a suitable $\frac{dI}{dV}$ curve this curve may be directly calibrated using a decade resistance box connected to the "R_{cal}" jacks. To accomplish this the decade resistance box should be preset to the estimated value of R_D and the function switch changed to the "cal." position. The recorder Y scale may then be calibrated directly by varying the decade box in desired steps.

c) $\frac{dV}{dI}$ - V curves.

The set-up, operate and calibrate conditions are essentially the same as for the $\frac{dI}{dV}$ mode with the exception of the first step. This is modified to $R_S \leq 10\ R_D$ in order to satisfy the balance conditions as discussed earlier.

V. PERFORMANCE CHARACTERISTICS

In the statement of the performance of the system we are primarily interested in three characteristics: the sensitivity of the system to detect small variations in conductance or resistance, in the linearity of the system, and in its dynamic range. The sensitivity of the system is best stated in terms of that percentage change in the measured conductance or resistance which equals the amplitude of the noise in the output of the system. This of course will be a function of both the output filter time constant and of the lock-in input sensitivity. Using the 200 μv input, resulting in an 80 μv rms sampling signal, and the 0.1 sec. time constant filter position the detection sensitivity is better than 0.3% while 0.1% detection sensitivity or better is possible for filtering time constants of 0.3 secs. and larger.

The results of a test of the linearity and dynamic range of the system are shown in fig. 9. With proper set up conditions, the linearity can be maintained at better than about 5% over the entire range of output voltage below about 8 volts, a dynamic range of nearly three orders of magnitude. The high end of the range is limited by decreasing incremental loop gain (cf. p. 12) and by the saturation of the operational amplifier. The lower limit of the dynamic range is fixed by the choice of series resistor during set up as somewhere between five and one hundred millivolts. The criterion of this choice is the stability of the circuit as the incremental loop gain increases and as the lock-in noise level becomes comparable to the chopper voltage (cf. p. 18 top).

Examples of some measurements obtained with the system are shown in figs. 10 and 11. Fig. 10 is a combined plot of the current-voltage and

conductance voltage characteristics of a silicon backward diode showing the familiar phonon structure of these devices and also an anomaly, a conductance minimum at zero bias. Fig. 11 is a combined plot of the current-voltage and conductance voltage characteristics of a $NbSe_2$ - Nb oxide - Pb junction. The low resistance junction shows completely anomalous structure including symmetric regions of negative resistance which is strongly magnetic field dependent. The negative resistance disappears with the application of several kilogauss of magnetic field and both the magnitude and position of the conductance peaks and dips are strongly field dependent. Presently, however, this structure is completely anomalous and is not yet understood.

VI. SUMMARY AND CONCLUSIONS

An all electronic feedback differentiation system, built around a PAR-HR8 lock-in amplifier, a high gain operational amplifier and a transistor chopper has been described and discussed. An analysis of the balance conditions, stability conditions and noise figure has been presented. It is found that the particularly useful applications of this system are in the measurement of dynamic conductance of very low resistance devices such as encountered in the study of zero bias and magnetic anomalies and superconducting tunneling and in the measurement of $(\frac{dV}{dI})$ for very high impedance samples (MOS devices). In the intermediate impedance ranges $\frac{dI}{dV}$ and $\frac{dV}{dI}$ can be measured with equal ease and this system represents some improvement over the conventional system primarily by allowing a convenient choice of either $(\frac{dV}{dI})$ or $(\frac{dI}{dV})$ and by giving slight improvement in the noise figure and hence the sensitivity.

On the other hand this system represents an attractive and

improved alternative to the more conventional servo motor feedback differentiator, not only because of its all electronic operation and lower cost, but also because of the relative simplicity of the system and its amenity to an exact analysis. This leads to greater confidence in the data retrieved with this system.

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D. E. Thomas and J. M. Rowell, Rev. Sci. Instr. 36, 1301, 1965.
G. R. Branner, E. M. Friar and G. Medicus, Rev. Sci. Instr. 34, 231, 1963.

APPENDIX

The general case of ϕ arbitrary is not particularly profitable. However, for completeness we note that

$$e_i = \frac{e_o R_D}{\sqrt{(R_D+R_S)^2 + (R_D R_S X)^2}} \sin(\omega t+\phi') \ ;$$

$$\phi' = \tan^{-1}\left(\frac{R_D R_S X}{R_S + R_D}\right)$$

The "phase selector" chooses the direct current component of $e_i \cdot \sin(\omega t+\phi)$. Since

$$\sin(\omega t+\phi') \sin(\omega t+\phi) = \frac{1}{2}\left[\cos(\phi-\phi') - \cos(2\omega t+\phi+\phi')\right]$$

we have

$$e_o = A(R - \frac{He_o R_D \cos(\phi-\phi')}{\sqrt{(R_D+R_S)^2 + (R_D R_S X)^2}}$$

$$= \frac{AR}{1 + \frac{HAR_D \cos(\phi-\phi')}{\sqrt{(R_D+R_S)^2 + (R_D R_S X)^2}}}$$

For $HA >> 1$

$$e_o \alpha \left(\frac{1}{R_D}\right) \sqrt{(R_D+R_S)^2 + (R_D R_S X)^2} \ \sec(\phi-\phi')$$

To maximize the lock-in gain by setting $\phi = \phi'$ does not lead a useful form for e_o.

FIGURE CAPTIONS

Figure 1 : Block diagram of the differentiator system.

Figure 2 : Circuit diagram of the differentiator system.

Figure 3a: Circuit diagram of the power supply for the differentiator system.

Figure 3b: Circuit diagram of the swept d.c. power supply.

Figure 4a: Equivalent circuit for the analysis of balance conditions for the $\frac{dI}{dV}$ mode.

Figure 4b: Equivalent circuit for the analysis of the balance conditions for the $\frac{dV}{dI}$ mode.

Figure 5 : Equivalent circuit for the stability analysis of the differentiator.

Figure 6 : Magnitude and phase of the normalized transfer function $(\tilde{H})$ of a portion of the feedback loop including the chopper, sample and the lock-in mixer.

Figure 7a: Nyquist stability plot of the feedback system with no lock-in filtering.

Figure 7b: Nyquist stability plot of the feedback system with 6 db/oct. and 12 db/oct. lock-in filtering.

Figure 8 : Equivalent circuit for the noise analysis of the feedback differentiator.

Figure 9 : Measured dynamic range and linearity of the feedback system in the conductance mode (fo = 500 Hz).

Figure 10 : Current-voltage and conductance-voltage characteristics of a silicon backward diode at 4.20 K , showing the familiar phonon structure. Conductance curve was obtained at fo = 500 Hz.

Figure 11 : Current-voltage and conductance-voltage characteristics of an $NbSe_2$ - oxide - Pb superconducting tunnel structure.

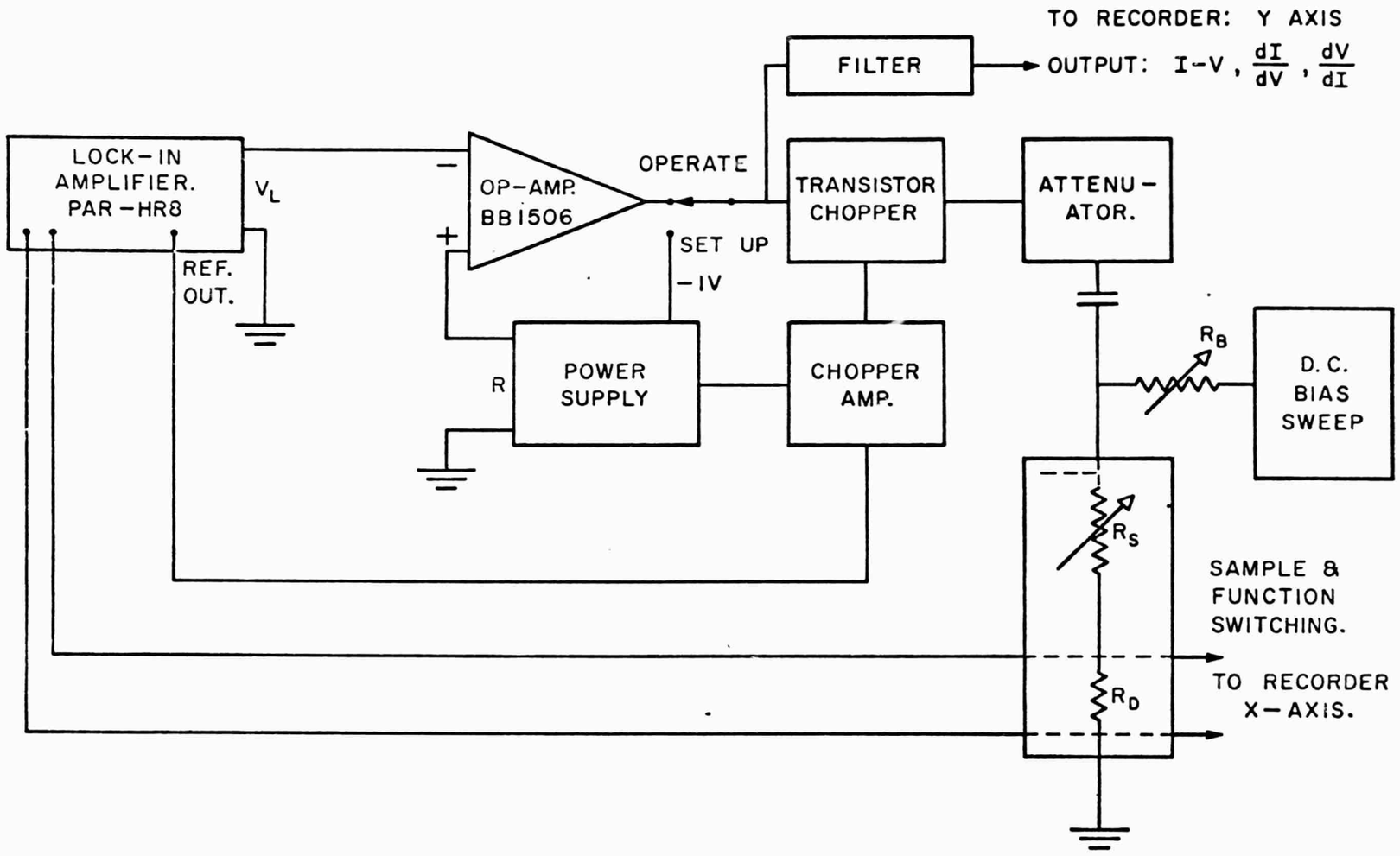
TO RECORDER: Y AXIS
FILTER
OUTPUT: I-V, dI/dV, dV/dI
LOCK-IN AMPLIFIER. PAR-HR8
V_L
REF. OUT.
OP-AMP. BB1506
OPERATE
SET UP
-IV
TRANSISTOR CHOPPER
ATTENU-ATOR.
R
POWER SUPPLY
CHOPPER AMP.
R_B
D.C. BIAS SWEEP
R_S
SAMPLE & FUNCTION SWITCHING.
R_D
TO RECORDER X-AXIS.

FIGURE 1

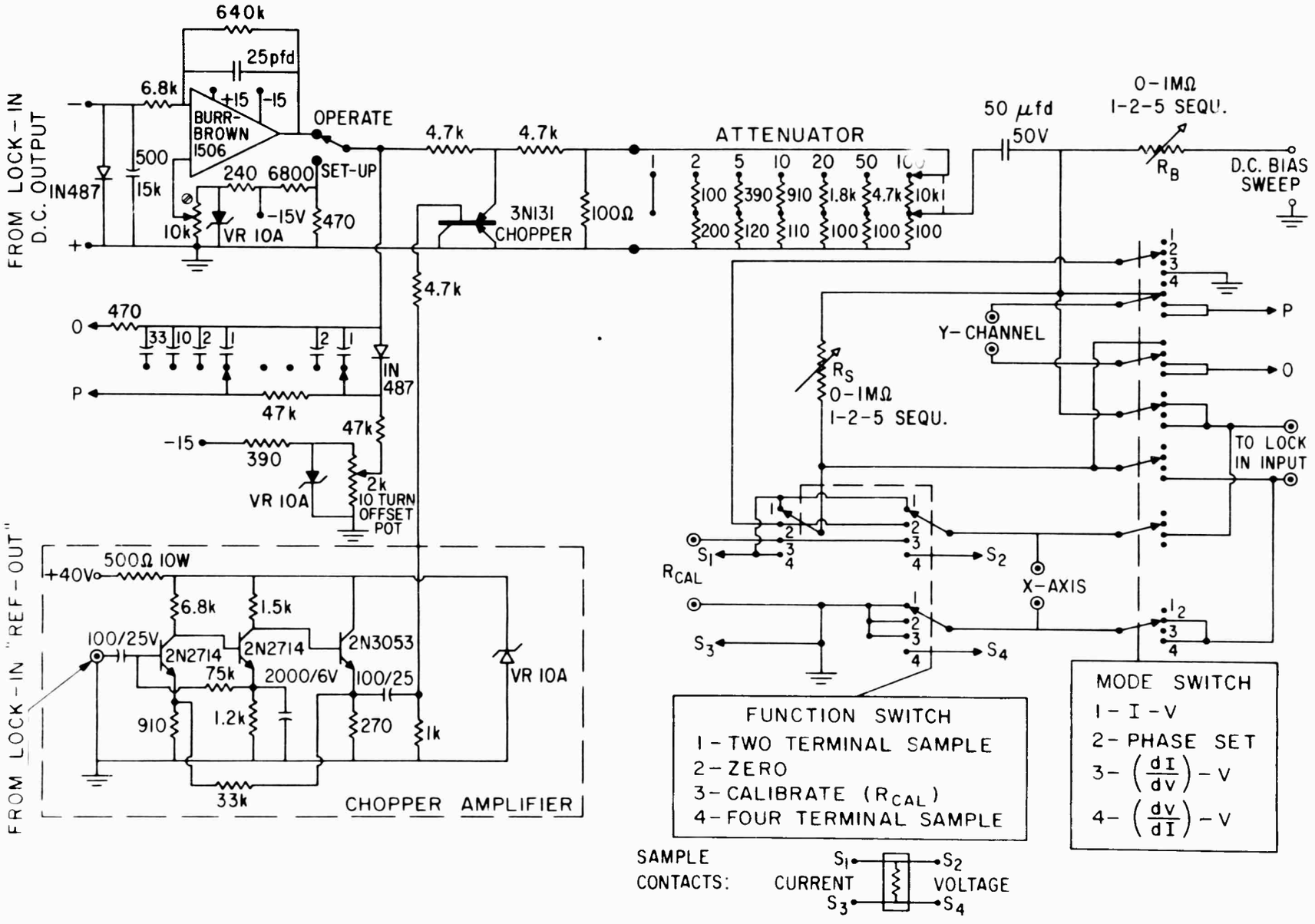
640k
25pfd
6.8k
+15
-15
BURR-BROWN 1506
OPERATE
4.7k
4.7k
ATTENUATOR
50 μfd
50V
0-1MΩ
1-2-5 SEQU.
FROM LOCK-IN D.C. OUTPUT
IN487
500
15k
240
6800
SET-UP
10k
VR 10A
-15V
470
3N131 CHOPPER
100Ω
1 2 5 10 20 50 100
100 390 910 1.8k 4.7k 10k
200 120 110 100 100 100
R_B
D.C. BIAS SWEEP
4.7k
470
0
33 10 2 1 2 1
IN 487
P
47k
47k
-15
390
VR 10A
2k 10 TURN OFFSET POT
Y-CHANNEL
R_S
0-1MΩ
1-2-5 SEQU.
TO LOCK IN INPUT
S_1
S_2
R_{CAL}
X-AXIS
S_3
S_4
I_2
FROM LOCK-IN "REF-OUT"
500Ω 10W
+40V
6.8k
1.5k
100/25V
2N2714
2N2714
2N3053
75k
2000/6V
100/25
VR 10A
910
1.2k
270
1k
33k
CHOPPER AMPLIFIER
FUNCTION SWITCH
1 - TWO TERMINAL SAMPLE
2 - ZERO
3 - CALIBRATE (R_{CAL})
4 - FOUR TERMINAL SAMPLE
MODE SWITCH
1 - I - V
2 - PHASE SET
3 - $\left(\frac{dI}{dV}\right)$ - V
4 - $\left(\frac{dV}{dI}\right)$ - V
SAMPLE CONTACTS:
S_1
S_2
CURRENT
VOLTAGE
S_3
S_4

FIGURE 2

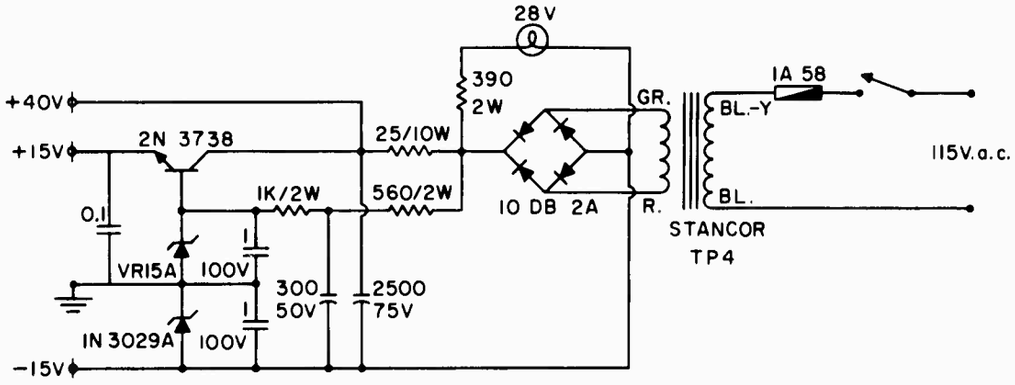

FIGURE 3a

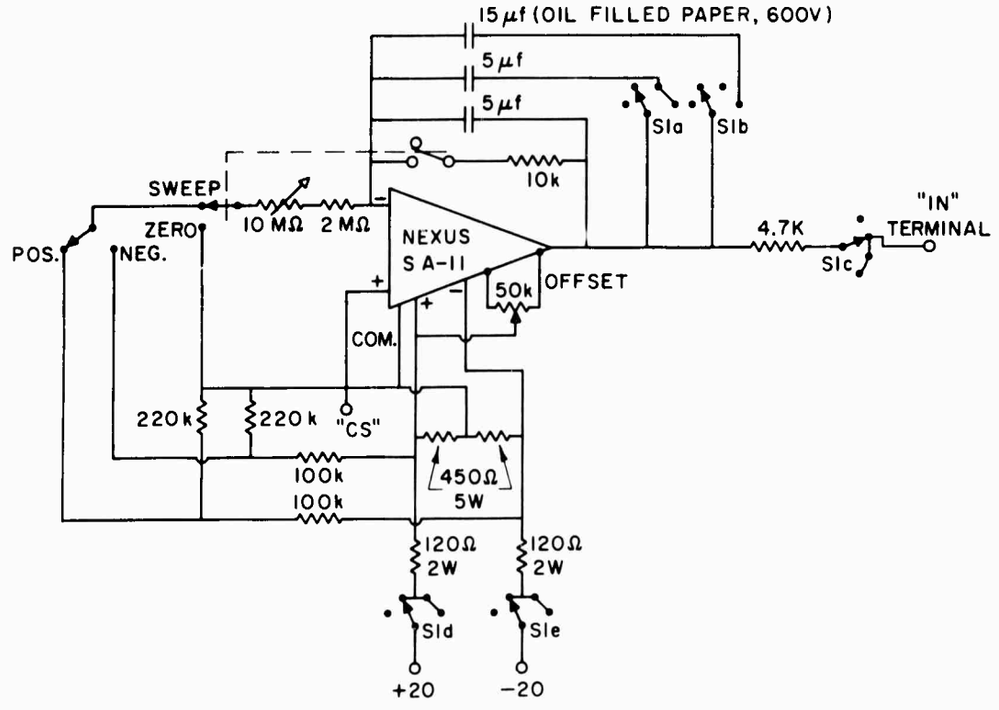

FIGURE 3b

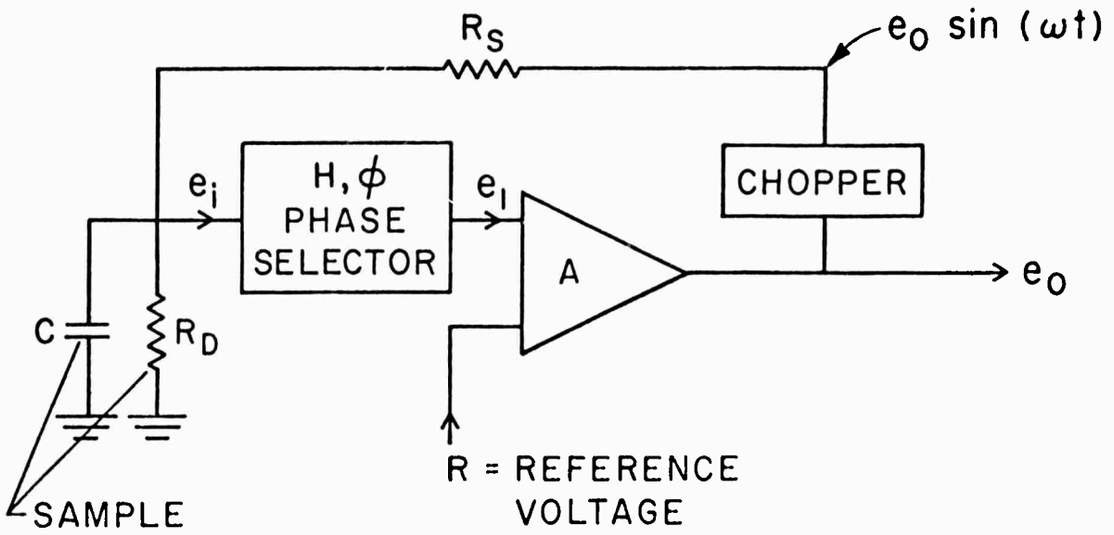

FIGURE 4a

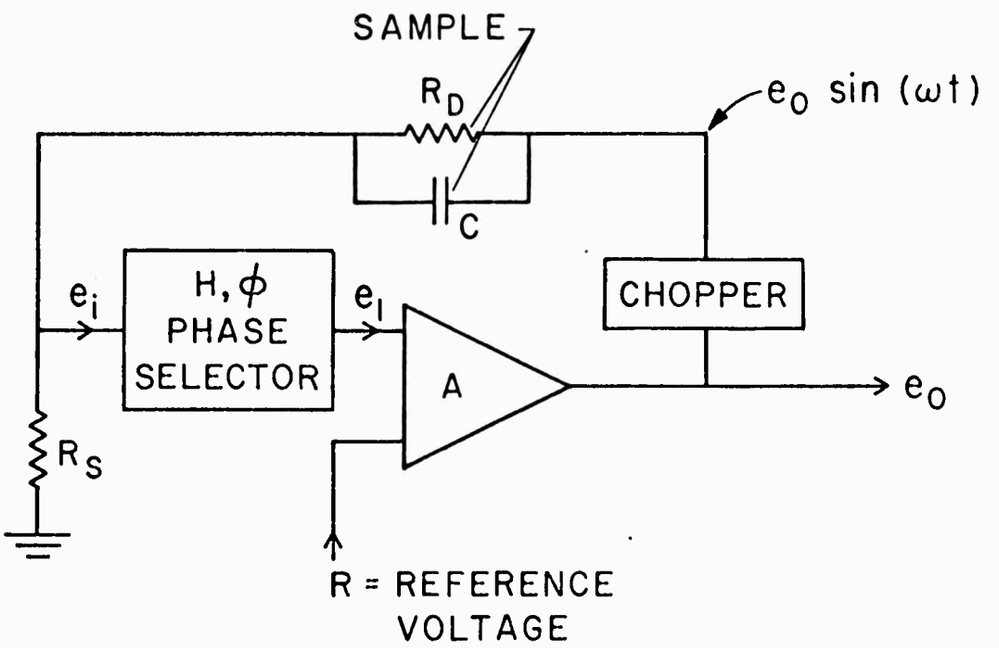

FIGURE 4b

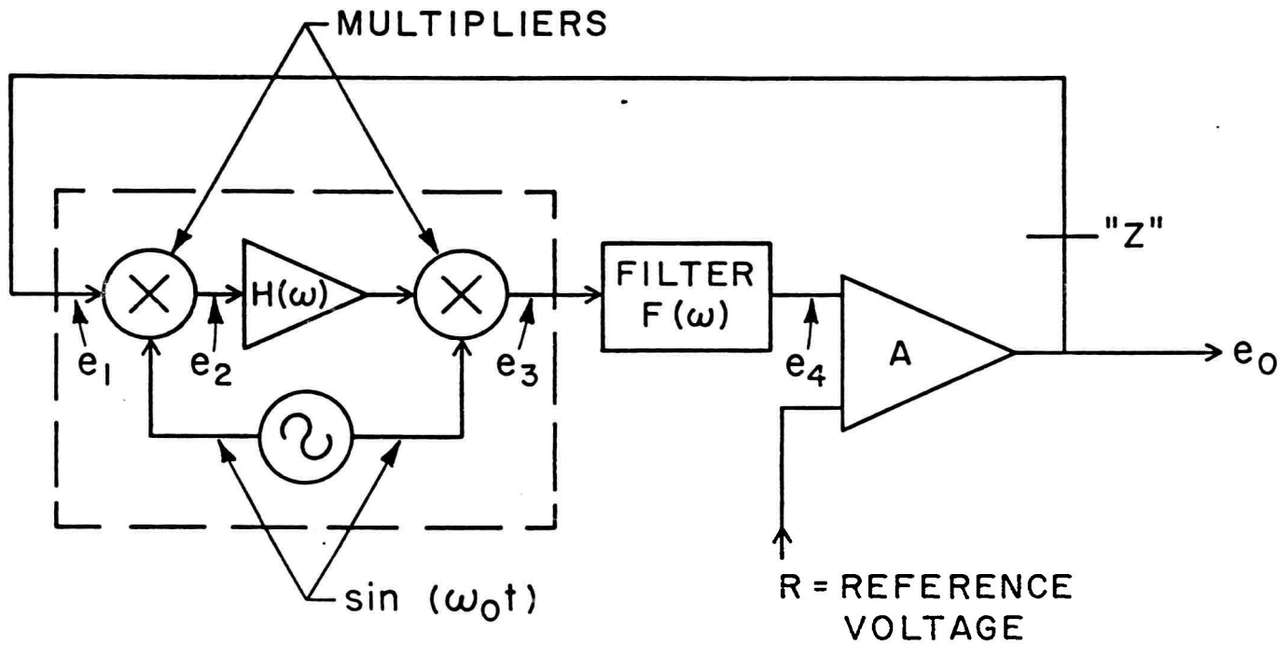
MULTIPLIERS
H(ω)
FILTER
F(ω)
A
"Z"
e1
e2
e3
e4
eo
sin (ω0t)
R = REFERENCE
VOLTAGE

FIGURE 5

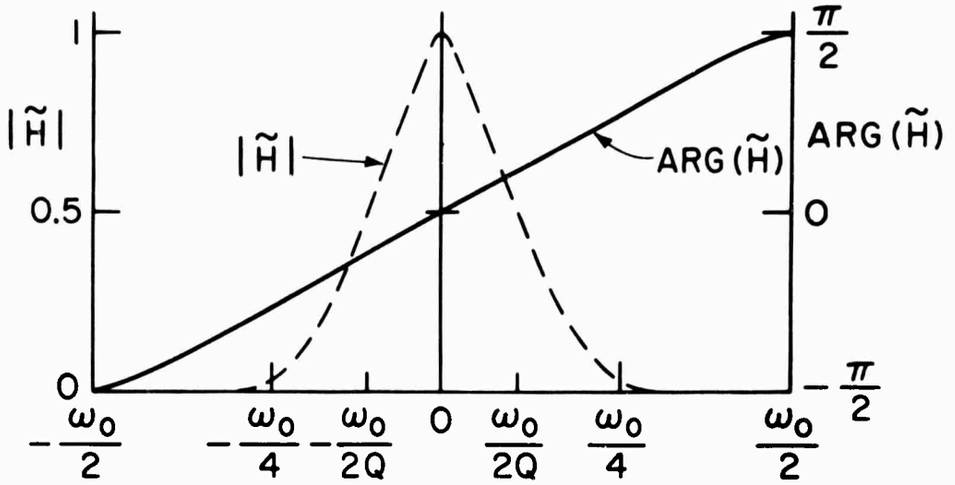

FIGURE 6

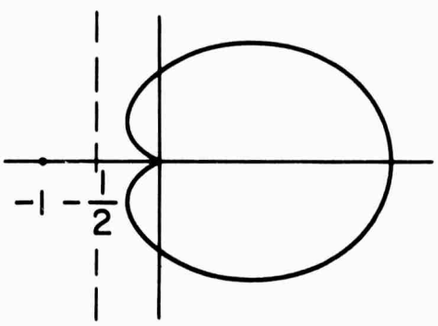

FIGURE 7a

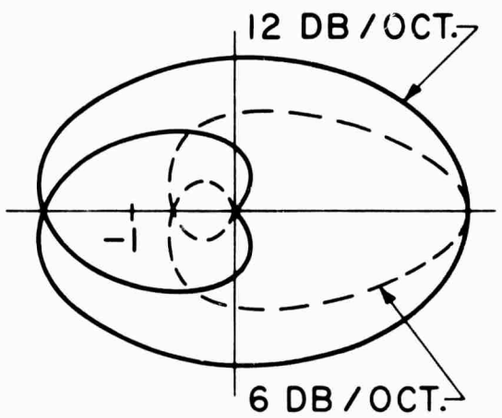

FIGURE 7b

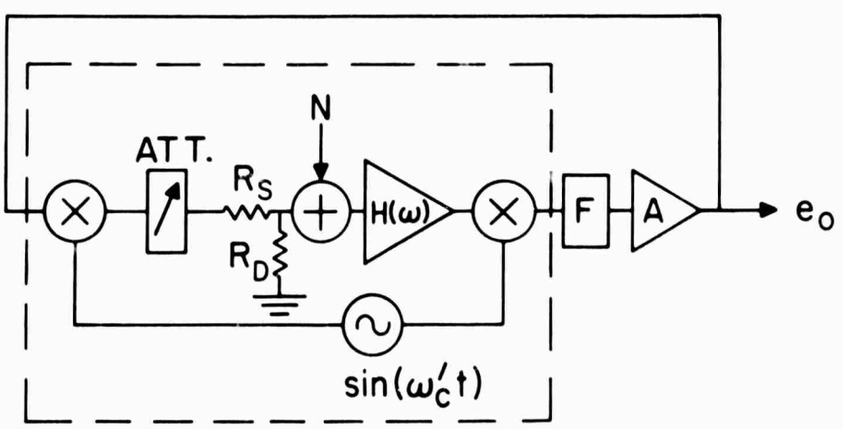

FIGURE 8

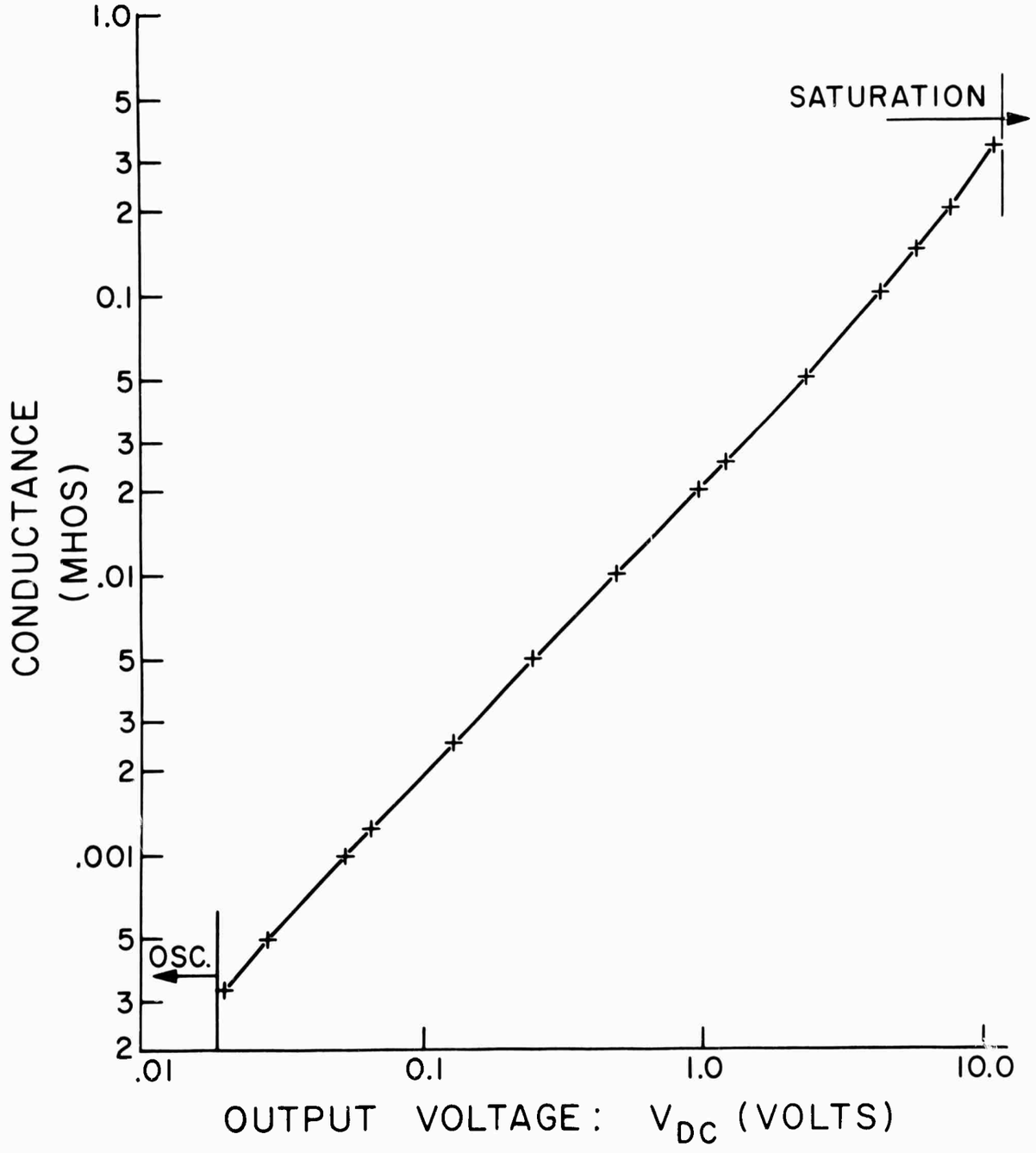
1.0
5
3
2
0.1
5
3
2
.01
5
3
2
.001
5
3
2
SATURATION
OSC.
.01
0.1
1.0
10.0
CONDUCTANCE (MHOS)
OUTPUT VOLTAGE: V_{DC} (VOLTS)

FIGURE 9

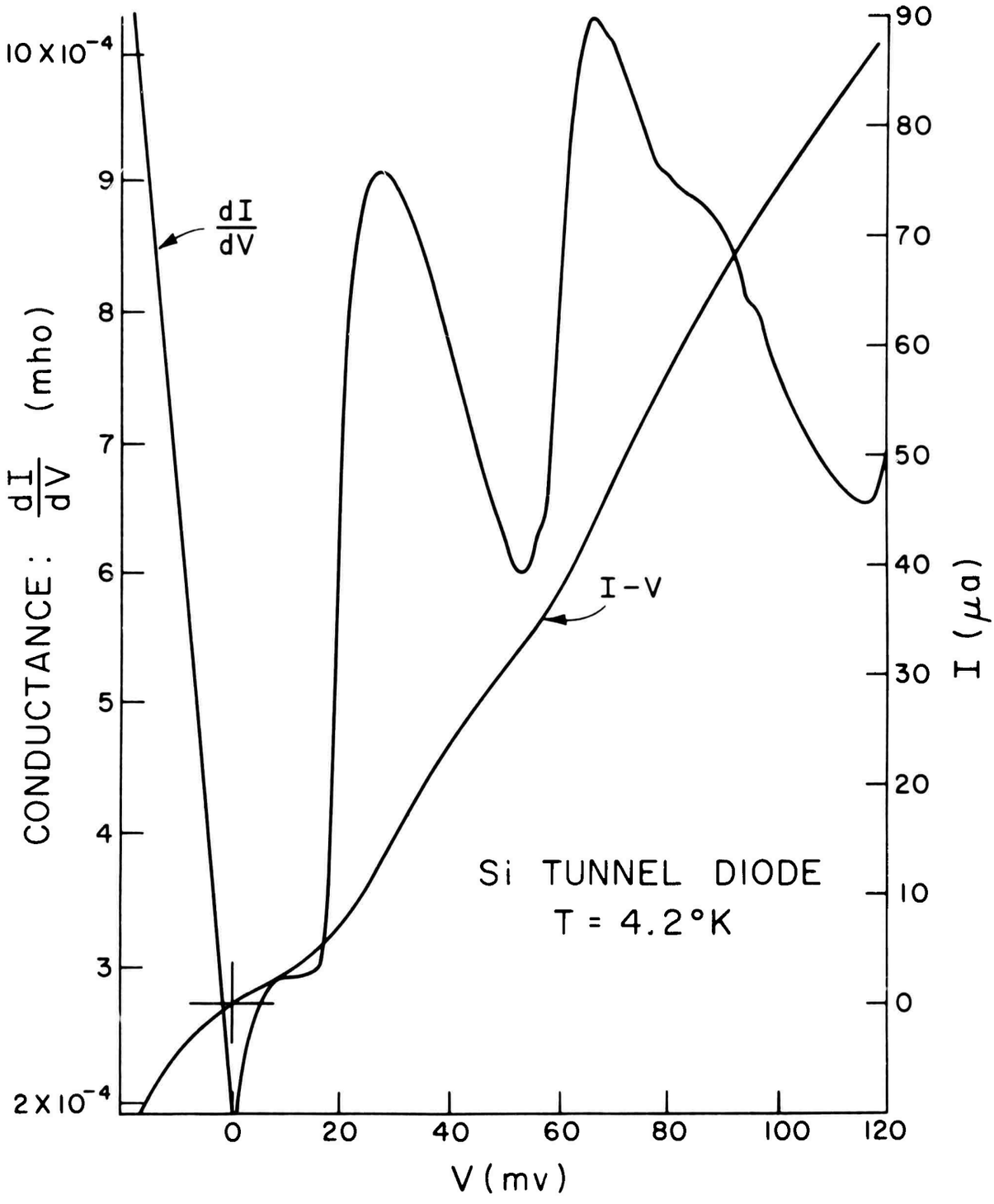
10 X 10⁻⁴
9
8
7
6
5
4
3
2 X 10⁻⁴
CONDUCTANCE: dI/dV (mho)
dI/dV
I-V
Si TUNNEL DIODE
T = 4.2°K
90
80
70
60
50
40
30
20
10
0
I (μa)
0
20
40
60
80
100
120
V (mv)

FIGURE 10

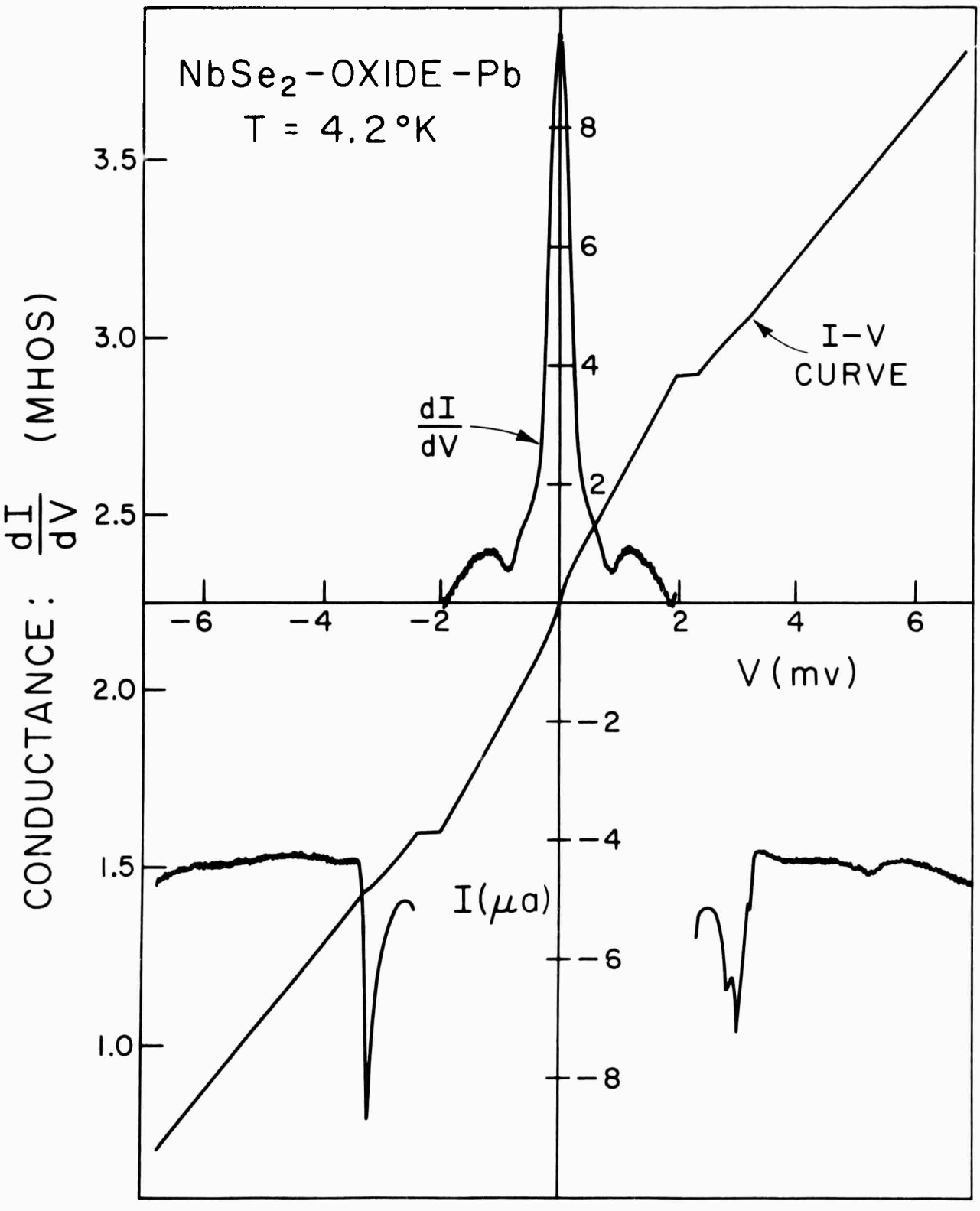
NbSe2 - OXIDE - Pb
T = 4.2°K
CONDUCTANCE: dI/dV (MHOS)
3.5
3.0
2.5
2.0
1.5
1.0
8
6
4
2
-2
-4
-6
-8
dI/dV
I-V CURVE
-6
-4
-2
2
4
6
V (mv)
I(μa)

FIGURE 11