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HISTOGRAM BEARING ANALYZER

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Rome Air Development Center
Air Force Systems Command
Griffiss Air Force Base, New York

HISTOGRAM BEARING ANALYZER

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FOREWORD

This report was prepared by Mr. Vincent J. Nardozza, (EMITG), Rome Air Development Center. The author wishes to express his appreciation to Messrs. J. Snodgrass and J. Palermo of Rome Air Development Center and to Mr. L. Van Doren of Smyth Research Associates for their assistance in this program.

The data herein presented was obtained from an "in-house" program conducted under Project 4505 to test and evaluate the Experimental Model Radio Direction Finding (RDF) Histogram-Time Average Processing System. The experimental model was built by Smyth Research Associates under the direction of RADC. The report summarizes the degree of improvement offered by the experimental model over more conventional DF read-out systems.

The development of the Experimental Model Histogram Bearing Analyzer was funded under RADC's Laboratory Directors' Fund (DI-68-1).

This technical report has been reviewed by the Office of Information (EMLS) and is releasable to the Clearinghouse for Federal Scientific and Technical Information.

This technical report has been reviewed and is approved.

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ABSTRACT

The Experimental Model Radio Direction Finding (RDF) Histogram-Time Averaging Processing System (Histogram Bearing Analyzer) and the data collection program conducted to determine its performance characteristics are described. Data comparing the capability of the Histogram Bearing Analyzer with a more conventional HF/DF read-out system are presented. Recommendations for improvements in the model's performance and continued experimentation are suggested.

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I. INTRODUCTION

The Histogram Bearing Analyzer (HBA) was developed as a supplemental read-out console for high frequency direction finding (HFDF) systems. It is intended to provide existing DF systems with a capability to make more accurate bearing estimates upon HF signals whose angles of arrival are being subjected to a relatively high degree of variation.

The propagation media and local topography are often responsible for deviations in the arrival angle of electromagnetic energy transmitted from one point (on the earth's surface) to another. This is especially true of high frequency (HF) skywave signals whose propagation paths are continually influenced by ionospheric variations, as well as the terrain features in the vicinity of a DF system attempting to measure their angle of arrival. Since a major objective of a DF measurement is to determine the bearing of an RF emitter from the arrival angle of its radiated energy, the observed deviations must be resolved to a single value which most accurately represents the true bearing of the emitter. Without the aid of sophisticated recording and processing systems, most Direction Finders in the past have had to rely upon aperture averaging, time averaging and signal strength as the sole criteria for determining emitter bearing from a series of unstable DF measurements.

II. GENERAL DESCRIPTION

The Histogram Bearing Analyzer presents a real time series of discrete radio direction finder measurements in the form of a histogram whose envelope represents the cumulative distribution of those measurements made within a selectable time period. In addition to showing the distribution of measurements, an appropriately scanned visual display (cathode-ray tube oscilloscope) of the histogram has an inherent advantage of showing the growth rate or time synthesis of the repetitive direction finder measurements. The model is readily adaptable to any radio direction finder system in which the measured angle of arrival can be represented as a bearing dependent voltage. This voltage is applied to a series of exclusive gates whose input voltage limits are established by the azimuthal resolution (direction finder accuracy) of the radio direction finder system or the desired display resolution. Associated with each gate is a cumulative event counter which registers each direction finder measurement that falls within the limits of its gate. The number of gate-counter channels required is directly related to the direction finder resolution required and the azimuthal sector over which it is desired to display the distribution of measurements. The rate at which the direction finder measurements

are sampled by array of gate-counter channels can be selectable (limited by the fundamental time constant of the direction finder system) while the accumulation period over which the counters are allowed to accumulate events before being reset, can be determined by a selectable time interval (clock) or by the number of events accumulated (counter).

The following description of Histogram Bearing Analyzer concept has been extracted in part from an RADC patent application entitled: "A Radio Direction Finding Histogram Processing System."

DESCRIPTION OF PREFERRED EMBODIMENT

This invention can be incorporated into any direction finder or bearing measurement system in which the measured angle of arrival can be represented as a bearing dependent voltage. It is uniquely suited for high frequency direction finder systems to complement their existing readout or display consoles. The cumulative distribution can be presented on an existing direction finder system display on a time share basis, on a "call-up" basis or continuously on a separate display.

The AZ-Track console of RADC's High Frequency Luneberg Lens Direction Finder (HFLLDF), has an auxiliary output which represents the measured angle of arrival of an intercepted signal within any 10° azimuthal sector as a linear voltage (±10VDC). The 10° sector is centered at multiples of 10° in azimuth with the above voltage range corresponding to a $\pm 5^{\circ}$ range from sector centers. The following description is based upon the assumption that the input signal to the Histogram Bearing Analyzer is derived from a system similar to RADC's HFLLDF.

Referring to Figure 1, the direction finder system bearing dependent voltage source is fed into gated voltage distribution network 19 which samples the direction finding voltage at a fixed clock rate. In the case explained, 50 level sensors collectively denoted as 21 of distribution network 19 are calibrated to pass voltages within their exclusive 20 VDC range (-10.0 to -9.8, -9.8 to -9.6, -9.6 to -9.4...+9.6 to +9.8, +9.8 to +10.0). Each time the direction finder system bearing dependent voltage is gated by clock 23 into distribution network 19 only one level sensor is activated to increment one of the 50 cumulative counters collectively denoted as 24. After a counter 24 is incremented, a pulse from clock 23 via delay 25 initiates a scan cycle of commutator 27 which samples the outputs (number 1, number 2, etc.) of each of the 50 cumulative counters 24. The same pulse triggers the horizontal sweep of cathode-ray

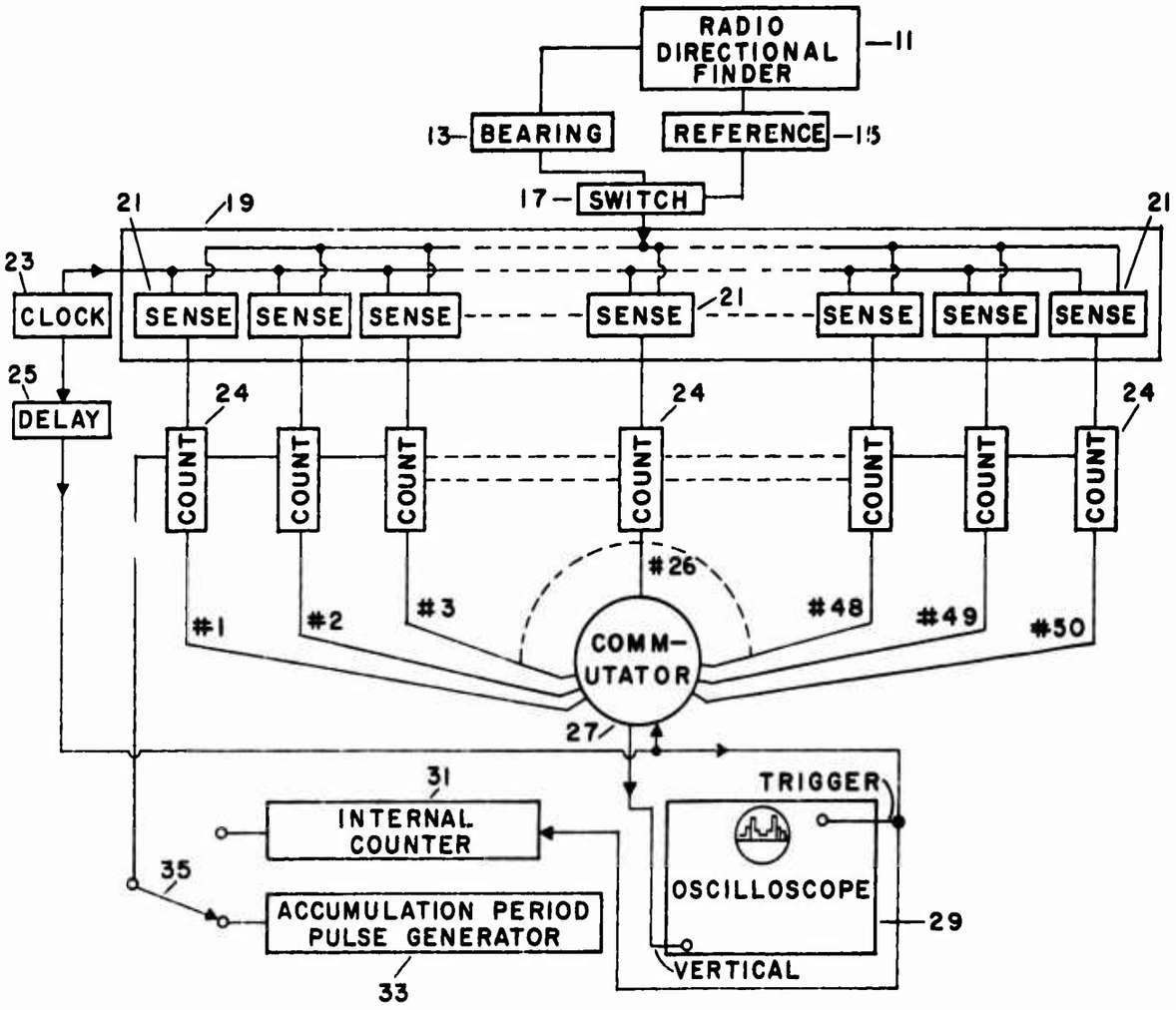


Figure 1. Preferred Embodiment

oscilloscope 29 whose vertical input voltage is derived from the output voltage of commutator 27.

The accumulation period can be determined by the time interval between the successive pulses of a variable pulse repetition frequency of pulse generator 33 which is also capable of simultaneously resetting all cumulative counters 24. By activating switch 35, the accumulation period can be controlled by interval counter 31 which initiates a reset voltage after a predetermined number of accumulated events, the accumulated events being the direction finder measurements."

III. EXPERIMENTAL MODEL PHYSICAL DESCRIPTION

The experimental model was fabricated to a great extent with modified modular sub-assemblies originally designed for use in Smyth Research Associates (SRA) Digitest Equipment. The SRA Digitest (digital Information Transmission Error Statistics Analyzer) was designed as an instrument for communications engineering to facilitate real time information bandwidth measurements of communications circuits through error rate analysis of digital signals. Under Air Force contracts F30602-68-C-0313 and F30636-68-N-3501, SRA adapted portions of their Digitest Equipment to satisfy the requirement of the Histogram Bearing Analyzer experimental model. This approach to the fabrication phase of this effort resulted in a substantial cost savings with only minor departures from the embodiment described above.

The experimental model consists of five logic chassis and a standard rack-mounted CRT oscilloscope. The five logic chassis are completely solid state and modularized. The experimental model is shown in Figure 2. All three chassis located in the left-hand turret and the top chassis in the right-hand turret are similar. They each contain twelve 8-bit binary counters and a power module. The two remaining binary counters to provide a 50 channel configuration, are located in the control chassis which is situated at the bottom of the right-hand turret. Also contained in the control chassis are the scanner and clock modules with their associated power module. The display shown in the center of the right-hand turret is a standard Hewlett Packard model 122AR oscilloscope.

The counter channels on each chassis are interconnected serially by 4 each 50 pin rear panel mounted patch cables. All cabling for the display unit is located between the front panel of the control chassis and the rear panel of the oscilloscope.

The front panel of one of the four digital average counter

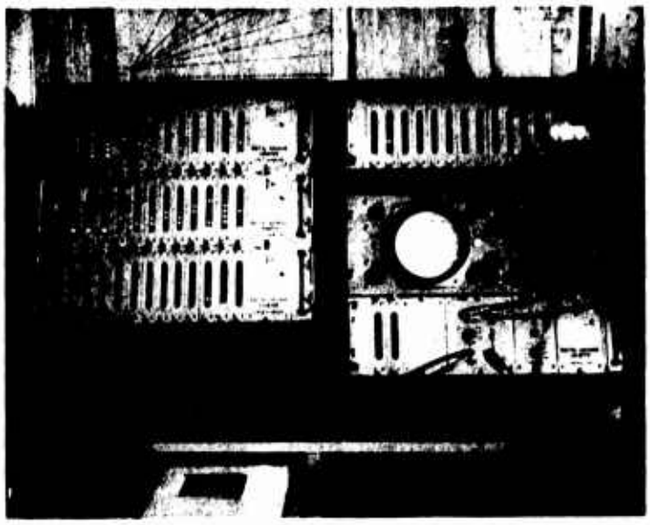


Figure 2a. Experimental Model Histogram Bearing Analyzer

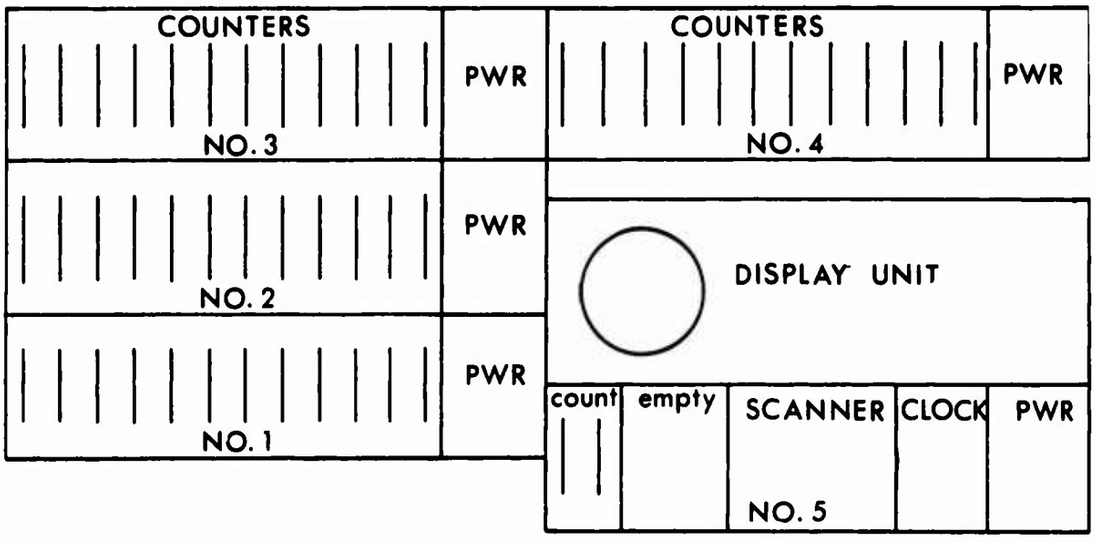


Figure 2b. Experimental Model Histogram Bearing Analyzer

chassis is shown in Figure 3. The twelve each 8-bit counters located to the left of the PWR module have light indicators, which display the accumulated count in each unit as a binary number. The PWR module has an on-off toggle switch, pilot lamps and appropriate test jacks. The control chassis front panel is shown in Figure 4. From left to right, the modules in this unit are;2 each counter channel, unused section, scanner module, clock module, and the control chassis PWR module.

IV. TECHNICAL DESCRIPTION

It is convenient to divide the experimental model into three basic units in describing its technical functions; the digital average counters (DAC), the Clock module and the Scan Module.

The digital average counters consist of the distribution network for the bearing dependent voltage derived from the direction finder and the 50 binary counter channels used in the model. Figure 5 is a block diagram of two adjacent counter channels. The bearing dependent voltage or DF signal is applied to all counter channels simultaneously for comparison with a discrete reference voltage associated with each channel. In Figure 5 it can be seen that the discrete reference voltages Vn, Vn+1 1 are derived from a voltage REF applied across a resistive string comprised of equal value precision resistors Rn, Rn+1. In the lower channel depicted in this figure, the input signal is compared to reference level Vn in comparator COMPn. If the signal level exceeds Vn, COMPn generates high state output level V'nwhich satisfies one input condition for "AND" gate, ANDn. The DF signal is simultaneously compared to reference level Vn+1 in comparator COMPn+1. If the DF signal does not exceed Vn+1, the low state output of COMPn+1 which is V'n+1 is inverted by INVn+1 to yield a high state output V"n+1. The high input condition of ANDn allows a clock pulse (clock) to increment counter COUNTn by one unit. Had the DF signal level exceeded the reference level Vn+1 in COMPn+1, then the high state of V'N+1 would have been converted to a low state INV"n+1. The second input condition of ANDn would not have been satisfied and the clock pulse would not be passed to COUNTn. In this manner, only one counter is allowed to increment for each pulse from the system's clock. Each counter is allowed to increment linearly until it receives a reset pulse or shift pulse. The reset pulse can be entered manually from the Clock and Scan Control Unit at any time to simultaneously reset all counters to zero. The shift pulse is generated automatically after every 125 clock pulses. The shift pulse simultaneously shifts all counters down by one bit which results in reducing the accumulated value in each counter by 1/2. Since the maximum value which could be recorded in each 8 bit counter is 225 counts,

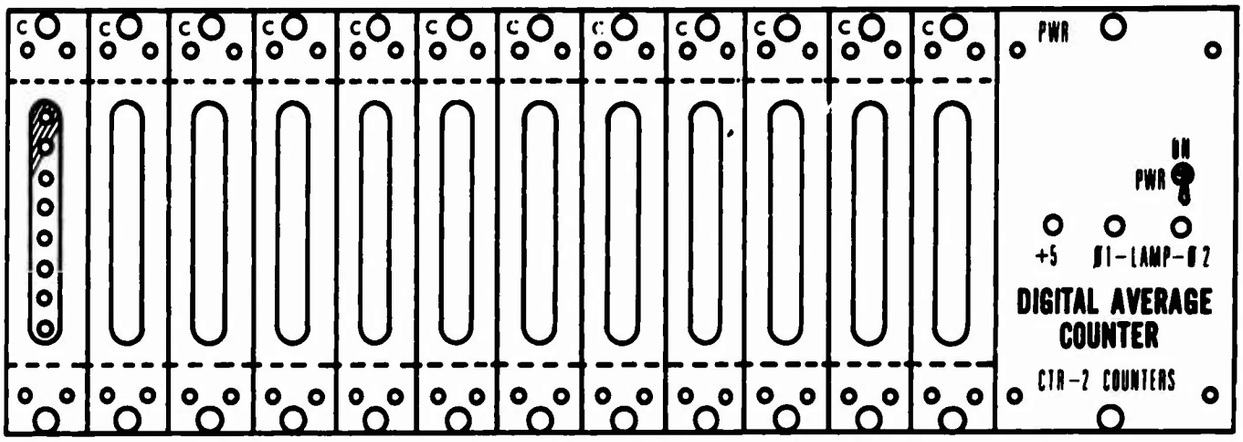


Figure 3. Front Panel Digital Average Counter Unit

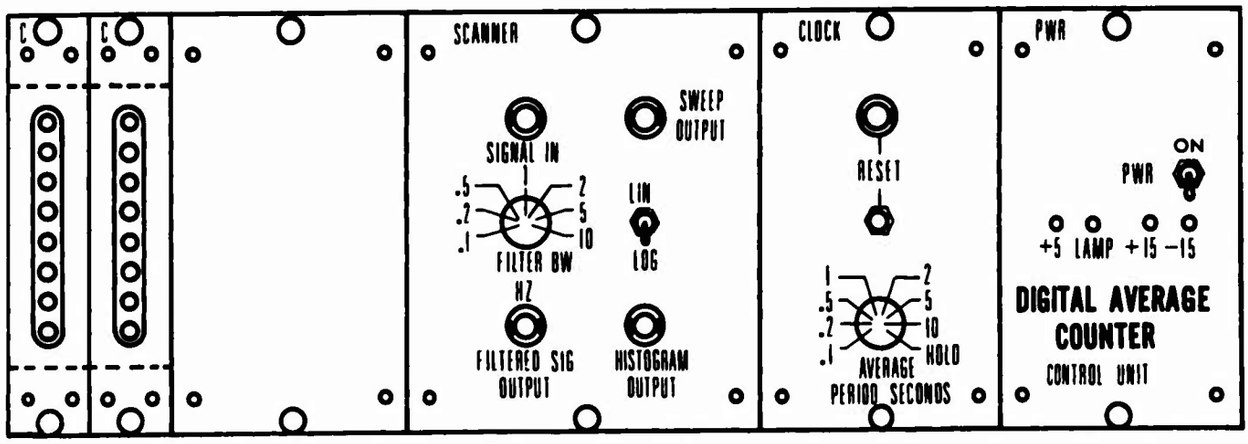


Figure 4. Front Panel Clock and Scan Control Unit

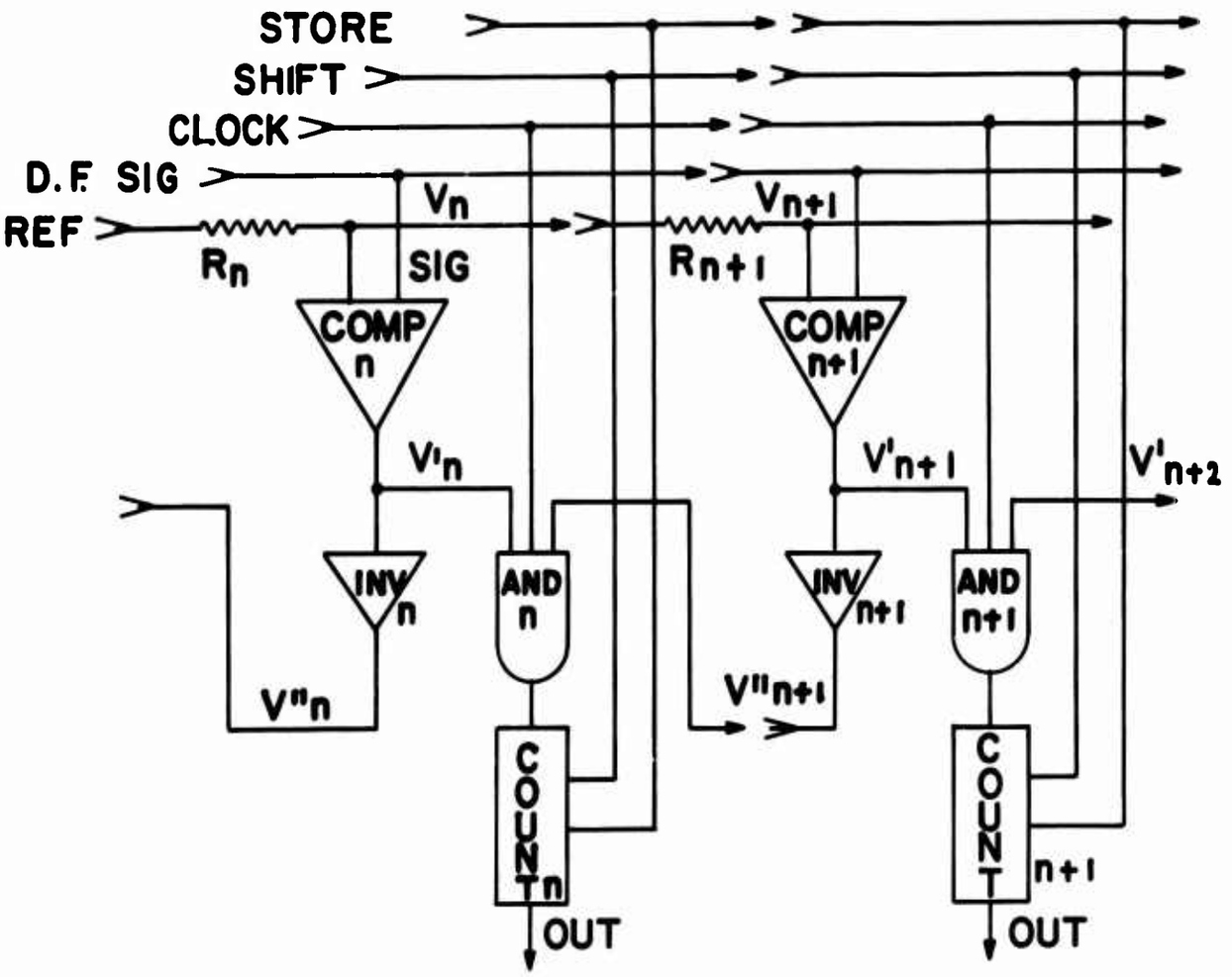


Figure 5. Digital Average Counter Block Diagram

this scheme prevents the system counters from saturating during any period of accumulation.

In addition to the shift and reset functions, a store function is provided which holds all counters at their accumulated values.

The clock module contains the crystal controlled multivibrator and bit rate divider logic which generates all the system timing and synchronization. Operating at a 200KHz rate, the multivibrator is divided down to produce a 10 KHz signal to drive the scanner. This 10 KHz is further divided to provide the CLOCK, SHIFT, and STORE frequencies shown in Table 1. It was shown in the preceding discussion that the CLOCK pulses are used to increment the appropriate counter channel after each DF signal sample has been distributed. By dividing down this CLOCK rate by 125 to generate the SHIFT and STORE rates, all counters will be periodically shifted (reduce accumulated values by 1/2) after an accumulation of 125 samples. The average period, or time period over which the 125 samples are accumulated, is simply the reciprocal of the SHIFT and STORE frequencies.

TABLE I

HISTOGRAM BEARING ANALYZER
TIMING

AVERAGE PERIOD (T)	SHIFT and STORE FREQUENCY (1/T)	CLOCK FREQUENCY (125/T)
.1 sec	10 Hz	1250 Hz
.2	5	625
.5	2	250
1	1	125
2	.5	62.5
5	.2	25.0

All counters can be RESET by inhibiting the CLOCK pulse at the DAC and applying the 10 KHz signal simultaneously to all SHIFT and STORE LINES of the COUNTERS. This RESET action clears all counters in less than 0.8 ms. The HOLD function, which holds all counters at their accumulated values is accomplished by inhibiting the CLOCK and SHIFT pulses at the counters. The HOLD is convenient for making a static examination of the display and for photographing the displayed Histogram.

The Scanner Module performs a multiplicity of functions. Within this unit, the ±10V DF input signal is scaled down to a ±2V range which is consistent with the incremental reference voltages distributed across the DAC input computers. It also divides the basic 10 KHz clock frequency down to the 20 Hz sweep rate for the Scanner, as well as digitally synthesizing a sweep voltage for the display by generating a 500 level staircase functioning with a Digital-to-Current Converter. The scan numbers, which sequentially address the counter channel output lines, and the subsequent Digital-to-Analog conversion of the counters is accomplished in this unit. Between the scan of successive counters, the analog output of the D/A converter is "boot strapped" to 0 volts to provide a bar-like appearance to the displayed Histogram. The output from the D/A converter can be presented directly to the display as a linear function or diverted through a Log Amp to yield a vertical logarithmic scale for the displayed Histogram. Finally, an entirely separated signal processing path is available which provides selectable bandwidth filtering for the DF input signal. The filtered signal processing path is available at a separate output connector on the front panel of the scanner, without altering the DF input signal bandwidths introduced to the DAC's.

A complete circuit description, extracted from the Instrumentation Manual delivered under F30602-68-C-0313, has been added as Appendix I to this report.

V. TEST PROGRAM

The test program established under this effort had three basic objectives. These were: 1. to determine the experimental model's compliance with the specifications of the contracts under which it was fabricated; 2. to verify that the integrity of the techniques is preserved when the model is interfaced to the HFLLDF electronics; and 3. to provide a sufficient amount of data upon which the capabilities of the technique could be evaluated.

A. Acceptance Tests

The acceptance test procedures for the experimental model were prepared by Smyth Research Associates, under contract F30602-68-C-0313 and approved by RADC. These test procedures and the data sheets compiled during the final acceptance tests conducted at RADC and the experimental model's specifications list are contained in Appendix II.

During this phase of the testing, circuit failures occurred in one of the model's fifty counter channels and in the 15 volt DC supply module of the Clock and Scan Control Unit. Both failures were attributed to faulty components and were subsequently corrected with replacements provided by Smyth Research Associates.

Close examination of the SWEEP OUT voltage used to provide horizontal drive for the model's display unit, revealed a third circuit malfunction. This 5V ramp voltage is simulated by a 500 increment staircase function derived from a digital to current converter. A two (2) bit error in the converter caused a shifting of the center portion of the output wave form which is illustrated in Figure 6 a. A photograph of one of the two points of discontinuity in the ramp function is shown in figure 6 b. As a result of these discontinuities, the widths of the 21st and 41st segments of the displayed histogram were compressed and expanded respectively by approximately 20% on their intended width. The two segments affected are illustrated in figure 7. It was determined that these non-linearities, which could be adequately compensated for by rescaling the display graticule, did not warrant an additional 3-6 week delay required to have the converter unit repaired by its manufacturer. The soundness of this decision was verified by the fact that no inconveniences were noted in the subsequent use of the rescaled graticule on the display unit.

Finally, it should be noted that the Clock and Scan Control Unit, which was purchased as a standard item, scanned the counter channels in decreasing order (i.e., +10.0 -+9.6, +9.6, -+9.2.... -9.6 --10.0 VDC). As a result, the displayed sector's horizontal scale shows decreasing azimuthal values from left to right (+5° to -5°). Again, after a very brief period of familiarization, this reversed display did not cause any appreciable inconvenience in routine use of the experimental model.

The experimental model was found to comply with all contract requirements and was accepted in August 1968.

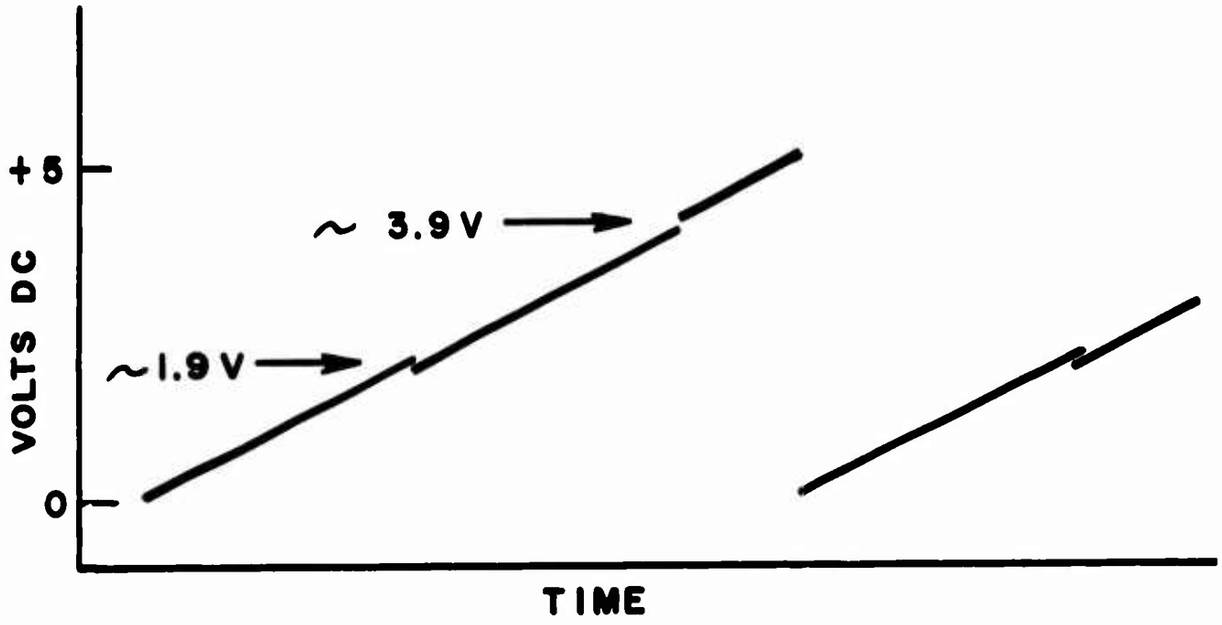
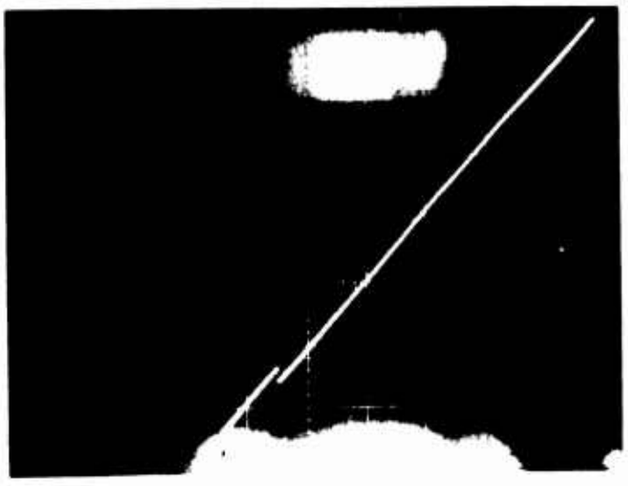


FIG. 6A DIGITAL TO CURRENT CONVERTER RAMP FUNCTION

VERTICAL
0.2V/ DIVISION



HORIZONTAL 2 M SEC/DIV

FIG 6B LOWER DISCONTINUITY (RADAR)

Figure 6. Sweep Voltage Waveform

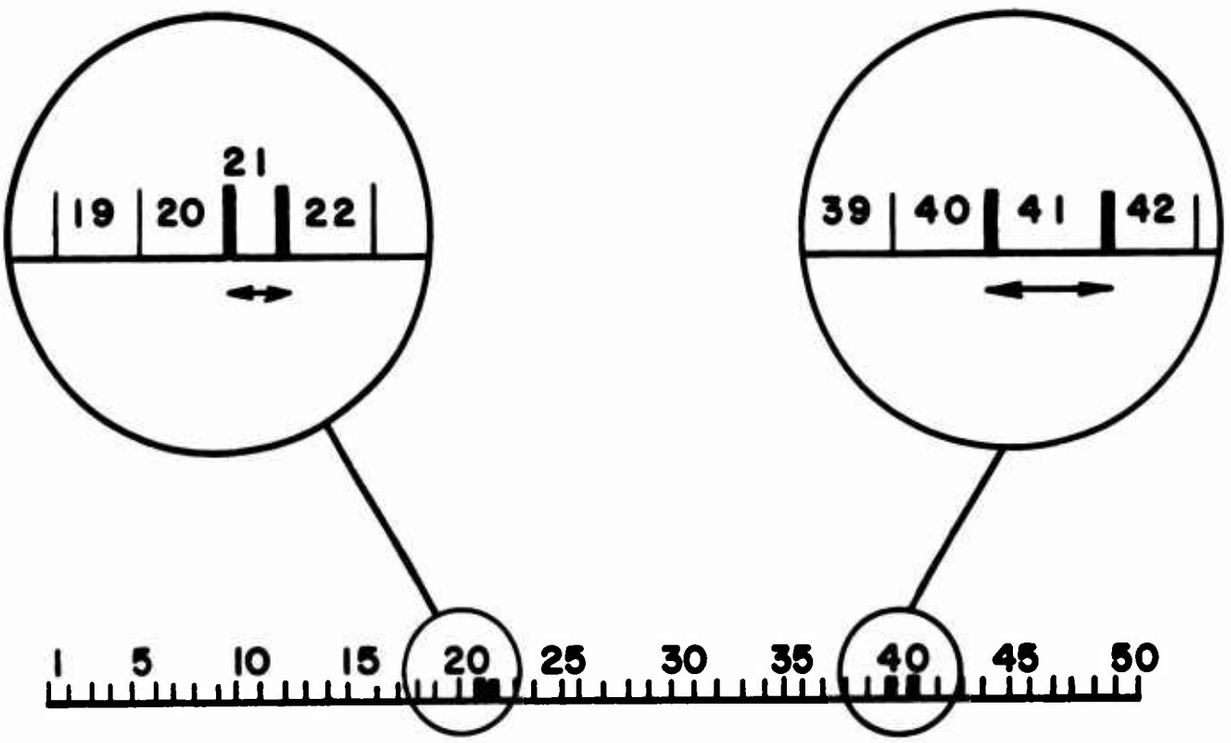


Figure 7. Sweep Voltage Waveform Distortion

B. HBA Display Interface

The AZ-Track console of the HFLLDF resolves the angle of arrival of an incoming signal to a single value within the 10° azimuth sector being examined by the direction finder. This resolved angle is displayed on the CRT of the AZ-Track console as a radial line strobe. The AZ-track console also generates a linear voltage ±10 VDC which is proportional to the resolved DF value. It is this voltage which serves as the signal input to the H B A experimental model.

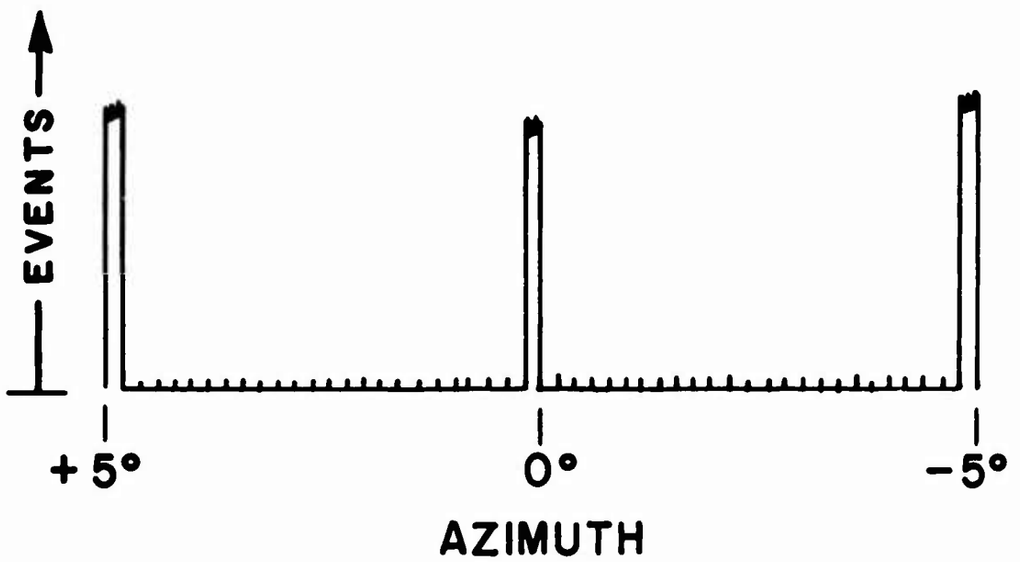


Figure 8. Calibration Display

To calibrate the Histogram Display, calibration signals were introduced to the Direction Finder which simulated arrival angles within the sector being examined at relative azimuths of -5°, +5°, and 0°. The three calibration signals were allowed to accumulate in the counters of the model to give a histogram with the envelope illustrated in Fig 8.

The time constant of Clock and Scan control unit was then switched to "HOLD" position to retain the accumulation in the three counter channels. With these three bars, the display could be centered and scaled on the display unit graticle. Since the resolution of the histogram display is 0.2°, the 20% distortion of the two segments noted in the previous section (amounting to only a .4% nonlinearity across the 50 segments) does not have any noticeable effect upon the horizontal scaling of the display unit.

C. Skywave Data Collection Program

The Histogram Bearing Analyzer was developed as a supplemental measurement console for existing HF/DF systems. It was specifically intended to provide such systems with a capability to make more accurate bearing measurements on skywave signals whose angles of arrival were being subjected to a relatively high degree of variation.

The basic thought behind the evaluation of the technique is to provide a data base of several hundred DF measurements made simultaneously with the HBA and the HFLLDF AZ-Track consoles. These measurements were to be made under a variety of operational conditions and then analyzed to determine to what extent and under which conditions the HBA afforded significant improvement over the conventional DF measurement procedures. Unfortunately only a comparatively small number of measurements of this type could be made prior to the deactivation of RADC's HFLLDF facility. The less than seventy usable simultaneous measurements made during this phase of the effort did demonstrate that appreciable improvement in DF accuracy was possible by use of the technique.

To facilitate the continued testing of the analyzer to fully define its capabilities, the experimental model has been recently transferred to another government agency which has access to the resources and facilities necessary to complete the required test and evaluation of the Histogram Bearing Analyzer.

VI. SKYWAVE DATA

The DF measurements obtained during this phase of the program are listed in Tables 2,3,and 4. The geographic location of each transmitter was determined from its station call sign which was related to a specific city or town. The geographic coordinates of this location were then used to calculate the Great Circle Bearing of the emitter from the HFLDF at Clark Hill. These signals were selected on the basis of their availability during each data collection period.

In tables 2,3, and 4 the DF measurements are assigned Intercept Numbers which can be cross-referenced with table No. 4 to identify the city or town in which the transmitter is located. The Radio Frequency of the signal is recorded under FREQ(MHz) and the simultaneous DF measurements made with the conventional HFLLDF console and Histogram Bearing Analyzer are listed under DF Measurement: AZ-Track - Histogram respectively. The TRUE BEARING is the calculated Great Circle bearing of the city or town in which it is assumed that the transmitter is located. A general estimate of the relative variability of the signals arrival angle is listed under VAR. These estimates were made by observing the signal's behavior on the AZ-Track console for a period of several seconds. They were not intended to be anything more than a qualitative indicator of relative stability. The "rule of thumb" for these estimates was:

VAR	
1	variations of 2° or less
2	variations greater than 2° but less than 5°
3	variations greater than 5°

In the last column TRF(SEC), the time required or allowed for each DF measurement is recorded in seconds.

The DF measurements contained in table 2 were made on 17 Sept 68 between 1718 and 1913 hours GMT. The operators were allowed 10 seconds in which to make each of these measurements. With few exceptions, the signals recorded on this day were relatively stable, arriving in the southwest section of the antenna system with RF frequencies between 14 and 29 MHz. Three of the intercepts (1-14, 1-20, and 1-21) could not be properly identified for a Great Circle Bearing calculation, either because their call sign was miscopied or because the coordinates of the transmitter location could not be reasonably identified.

In view of the relatively stable nature of most of the signals examined on 17 Sept, it would not be expected that any comparative summation of DF measurements would establish any significant

TABLE 2

DATA SHEET

TEST: Histogram Bearing Analyzer Evaluation

DATE: 17 Sept 1968
GMT TIME: 1718-1913 Hrs

Clark Hill HFLLDF

INTERCEPT NUMBER	FREQ (MHZ)	DF MEASUREMENT AZ-TRACK / HISTOGRAM		TRUE BEARING	DF ERROR AZ-TRACK / HISTOGRAM		VAR	TFF SEC
1-1	14.282	263.0	263.8	261.6	1.4	2.2	3	10
1-2	14.263	265.5	265.7	265.7	-0.2	0.0	2	10
1-3	14.273	212.0	212.0	234.3	-22.3	-22.3	1	10
1-4	14.230	226.0	226.4	226.0	0.0	0.4	2	10
1-5	14.227	287.0	287.4	268.7	18.3	18.7	1	10
1-6	14.243	266.0	265.6	268.9	-2.9	-3.3	2	10
1-7	21.310	225.5	226.2	226.1	-0.6	0.1	2	10
1-8	21.320	253.8	253.6	242.9	10.9	10.7	2	10
1-9	21.402	262.3	262.4	261.6	0.7	0.8	1	10
1-10	21.420	244.6	244.4	245.7	-1.1	-1.3	1	10
1-11	21.308	200.8	200.4	200.4	0.4	- 0 -	1	10
1-12	21.296	290.0	291.4	263.4	27.6	28.0	1	10
1-13	21.288	294.6	294.8	293.7	0.9	1.1	1	10
1-14	21.378	292.3	293.0	-	-	-	1	10

TABLE 2 (cont'd)

DATA SHEET

INTERCEPT NUMBER	FREQ (MHZ)	DF MEASUREMENT AZ-TRACK/HISTOGRAM		TRUE BEARING	DF ERROR AZ-TRACK/HISTOGRAM		VAR	TFF SEC
1-15	21.364	202.4	202.6	239.8	-37.4	-37.2	1	10
1-16	21.364	204.5	204.6	239.8	-35.3	-35.2	1	10
1-17	21.354	194.5	194.6	194.4	0.1	0.2	1	10
1-18	21.288	296.4	294.4	293.7	0.9	0.7	1	10
1-19	28.550	-	108.4	102.0	-	6.4	3	10
1-20	28.549	103.4	103.2	-	-	-	1	10
1-21	28.800	296.6	269.6	-	-	-	1	10
1-22	28.654	263.7	263.7	277.1	-13.6	-13.3	1	10
1-23	28.807	263.7	263.6	263.2	0.5	0.4	1	10
1-24	28.610	100.5	100.6	96.2	4.3	4.4	1	10
1-25	14.308	202.0	202.6	235.3	-33.3	-32.7	3	10
1-26	14.266	258.8	258.4	260.8	-2.3	-2.4	1	10
1-27	14.266	257.9	258.4	260.8	-2.9	-2.4	1	10
1-28	14.231	260.5	261.0	269.4	-8.9	-8.4	1	10

difference between the DF errors associated with the two measurement systems being examined.

It is considered to be of particular significance, that the high degree of variability associated with intercept No. 1-19 prevented the AZ-TRACK console operator from attempting to estimate the signal's arrival angle. During this same period, however, the Histogram display readily identified the most prevalent arrival angle for that same signal to be within 6.4° of the emitter's calculated bearing. It is exactly for this type of situation that the Histogram Bearing Analyzer was developed.

Intercepts 1-3, 1-5, 1-12, 1-15, 1-16, and 1-22 were relatively stable signals arriving at angle significantly different from their calculated Great Circle bearings. The sector limitations of the HFLLDF masked any activity along the signal's Great Circle routes, confining both DF measurement consoles to an examination of the same "wrong" 10° sector. The relative errors associated with the two measurements made on each of these signals are, therefore, considered to be of questionable value. Intercept No. 1-25, though more unstable than the above, is considered invalid for the same reason.

It was noted earlier, that little difference could be expected between the summarized errors associated with the two DF measurement techniques under relatively stable conditions such as those which were generally observed for data contained in Table No. 2. This is verified by the fact that the average absolute error for the remaining seventeen intercepts listed was 2.3° for both sets of measurements. Intercept 1-19 was excluded from this summary since no finite value could be assigned to the AZ-TRACK error associated with this intercept.

The average absolute error was selected as criteria for comparison of DF errors for two reasons. First, since both systems operate upon the same bearing dependent voltage provided by the HFLLDF, we would not expect to see a difference in the systematic bias associated with the two sets of measurements. And secondly , because the sample sizes which we are examining are relatively small, the significance of the summary value can be easily related to the magnitude of the individual errors observed.

The intercepts contained in table No. 3 were obtained with procedures that differed somewhat from those under which the data in table No. 2 were collected. The console operators were given as much time as they felt was necessary to examine the displayed DF signal information before estimating the bearing angle. It should be noted from the VAR indexes that the signals observed during this data collection period displayed a greater degree of variation.

TABLE 3

DATA SHEET

TEST: Histogram Bearing Analyzer Evaluation

DATE: 4 Dec 1968
GMT TIME: 1500-1818 Hrs

Clark Hill HFLLDF

INTERCEPT NUMBER	FREQ (MHZ)	DF MEASUREMENT AZ-TRACK/HISTOGRAM		TRUE BEARING	DF ERROR AZ-TRACK/HISTOGRAM		VAR	TFF SEC
2-1	15.360	105.0	104.6	101.8	+3.2	+2.8	3	15/5
2-2	15.320	72.3	73.0	68.5	+3.8	+4.5	2	9/8
2-3	15.070	-	54.6	52.0	-	+2.6	3	80/20
2-4	15.330	237.0	238.6	242.2	-5.2	-3.6	3	10/8
2-5	15.195	56.0	55.8	52.0	+4.0	+3.8	3	8/8
2-6	17.820	70.0	70.2	68.5	+1.5	+1.7	1	3/3
2-7	17.800	72.0	72.4	71.3	+0.7	+1.1	2	11/6
2-8	17.855	72.0	73.0	73.3	-1.3	-0.3	2	9/9
2-9	17.690	59.0	57.2	-	-	-	3	8/8
2-10	17.710	187.5	197.4	192.0	-4.5	-4.6	2	5/5
2-11	17.775	186.4	186.2	192.0	-5.6	-5.8	1	5/5
2-12	21.495	70.0	70.4	-	-	-	1	15/4
2-13	21.900	69.5	70.4	71.3	-1.8	-0.9	1	7/7
2-14	21.535	103.8	101.4	101.8	+1.0	+0.4	3	10/10

TABLE 3 (cont'd)

INTERCEPT NUMBER	FREQ (MHZ)	DF MEASUREMENT AZ-TRACK/HISTOGRAM		TRUE BEARING	DF ERROR AZ-TRACK/HISTOGRAM		VAR	TFF SEC
2-15	21.790	102.8	103.2	101.8	+1.0	+1.4	3	7/7
2-16	11.725	72.5	71.6	68.5	+4.0	+3.1	2	10/7
2-17	11.960	73.0	73.6	73.3	-0.3	+0.3	3	20/10
2-18	11.960	197.5	197.6	198.5	-1.0	-0.9	3	6/6
2-19	15.320	67.2	66.2	68.5	-1.3	-2.3	1	2/2
2-20	15.070	56.8	56.6	52.0	4.8	4.6	3	5/5
2-21	15.330	242.7	242.2	242.2	+0.5	0	2	12/12
2-22	17.820	70.3	69.8	68.5	+1.8	+1.3	1	25/10
2-23	17.800	71.8	71.8	71.3	+0.5	+0.5	1	8/8
2-24	17.710	190.9	189.8	192.0	-1.1	-2.2	3	10/10
2-25	17.775	190.0	190.2	192.0	-2.0	-1.8	3	10/10

The locations of the emitters for intercepts No. 2-9 and 2-12 could not be identified. Intercept No. 2-3 represents another instance in which the variability of the signal angle of arrival prevented the AZ-Track operator from attempting an estimate of the bearing angle, while the same signal was resolved to within 2.6° of its true bearing by the Histogram Bearing Analyzer.

The time required by each operator to make his DF measurement is recorded in the TFF Sec column. The AZ-Track time is located on the left side of the slash and the HBA time is located on the right side. For a total of nine of the twenty-three usable measurements made during this period, the AZ-Track operator required more time to make his measurements than was required by the HBA operator. For nine out of eleven measurements made upon signals whose variability was classed as condition 3, the HBA provided more accurate bearing estimates.

The average absolute error for both sets of measurements was 2.3°. In evaluating this summary, however,due consideration must be given to the fact that the AZ-Track operator used more time to make his estimates and even with additional time was unable to resolve intercept No. 2-3.

Figure 9 contains four typical HBA display presentations. The horizontal axis of each photograph covers an azimuthal range of +5° to -5° from left to right, each major division being 1°. The vertical scale is logarithmic with three major divisions representing approximately 125 accumulated events. Figure 9a shows a unique distribution of arrival angles covering the 10° sector from 55° to 65°. The -4.2° interval or 55.8° is readily identifiable as the dominant arrival angle. In Figure 9b, the majority of arrival angles are clustered about the selected arrival angle of 103.2° (+3.2° in the 95°-105° sector). The accumulation of events at -4.2° is assumed to be an interfering local signal or an unusual short term propagation phenomena since it immediately disappeared after this photograph was taken, and was not observed again. The high accumulation of events in +5.0° segment which will be noted in some of the photographs in Figure 10 is an intrumentation problem which will be identified in Section VII of this report. Figures 9c and 9d show the type of display generated by signals with relatively stable arrival angles.

The data listed in Table #4 was obtained only from signals which demonstrated a high degree variation (VAR-3) in their arrival angles. Both operators were allowed 10 seconds in which to make their estimates. Six of the recorded intercepts could not be identified (3-5, 3-7, 3-16, 3-17, 3-19, and 3-21).

An examination of the remaining nineteen intercepts shows that in every case, the accuracy of the Histogram Bearing Analyzer

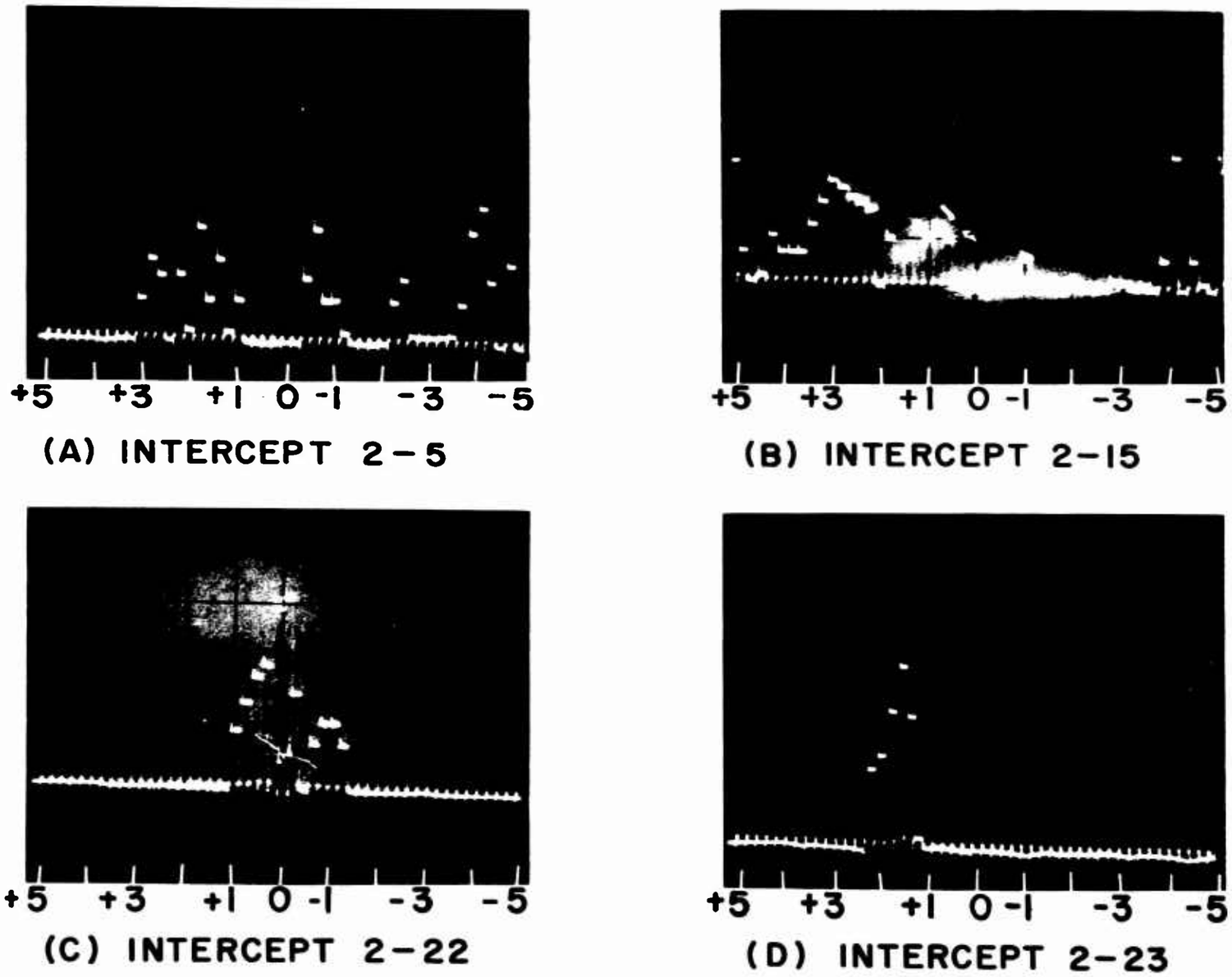


Figure 9. Histogram Bearing Analyzer Display

TABLE 4

DATA SHEET

TEST: Histogram Bearing Analyzer Evaluation

DATE: 20 Jan 1969
GMT TIME: 1545-1900 Hrs

Clark Hill HFLLDF

INTERCEPT NUMBER	FREQ (MHZ)	DF MEASUREMENT AZ-TRACK/HISTOGRAM		TRUE BEARING	DF ERROR AZ-TRACK/HISTOGRAM		VAR	TFF SEC
3-1	15.320	70.2	69.4	68.5	1.7	0.9	3	10
3-2	15.360	103.0	101.6	101.8	1.2	0.2	3	10
3-3	15.320	70.0	69.0	68.5	1.5	0.5	3	10
3-4	15.070	54.3	53.6	52.0	2.3	1.6	3	10
3-5	15.330	234.0	233.6				3	10
3-6	15.330	243.0	242.4	242.2	0.8	0.2	3	10
3-7	15.195	67.0	66.0				3	10
3-8	17.800	73.5	72.6	71.3	2.2	1.3	3	10
3-9	17.855	73.7	73.2	73.3	0.4	-0.1	3	10
3-10	21.495	71.1	70.1	68.5	2.6	1.6	3	10
3-11	21.495	66.0	69.2	68.5	-2.5	0.7	3	10
3-12	21.700	69.5	69.8	71.3	-1.8	-1.5	3	10
3-13	21.535	103.8	102.4	101.8	-2.0	-0.6	3	10

TABLE 4 (cont'd)

INTERCEPT NUMBER	FREQ (MHZ)	DF MEASUREMENT AZ-TRACK/HISTOGRAM		TRUE BEARING	DF ERROR AZ-TPACK/HISTOGRAM		VAR	TFF SEC
3-15	11.760	189.2	189.6	192.0	-2.8	-2.4	3	10
3-16	11.795	57.0	56.4				3	10
3-17	11.855	51.0	49.2				3	10
3-18	15.070	53.0	51.8	52.0	1.0	-0.2	3	10
3-19	15.300	197.5	198.4				3	10
3-20	15.320	69.2	68.4	68.5	0.7	-0.1	3	10
3-21	17.885	201.7	201.6				3	10
3-22	15.070	53.0	52.6	52.0	1.0	0.6	3	10
3-23	15.070	53.0	52.4	52.0	1.0	0.4	3	10
3-24	15.360	103.0	102.2	101.8	1.2	0.6	3	10
3-25	15.360	103.0	102.2	101.8	1.2	0.6	3	10

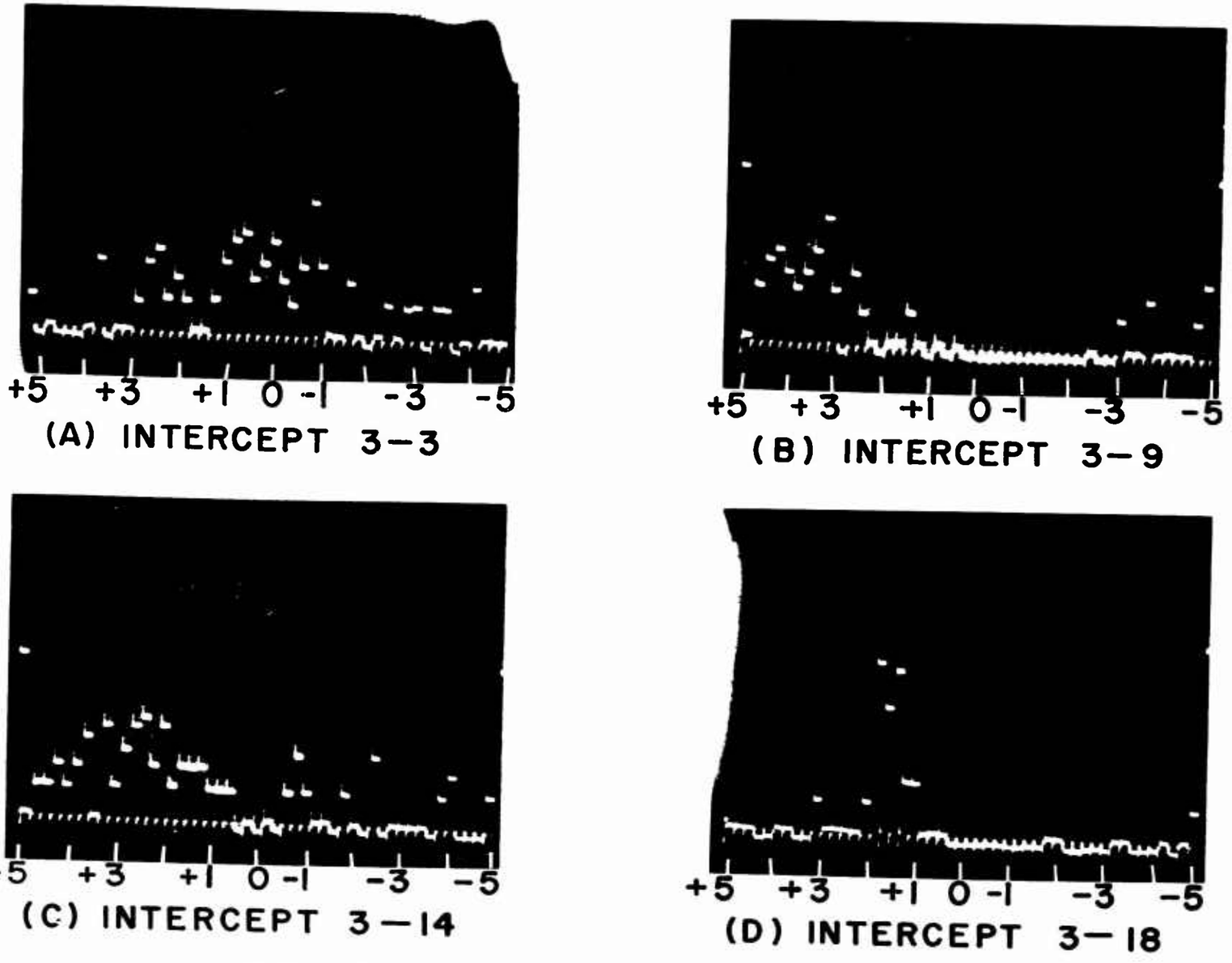


Figure 10. Histogram Bearing Analyzer Display

exceeded that of the measurements made from the AZ-Track Console. The average absolute error associated with the AZ-Track console was 1.8° while the Histogram DF error was only 0.8°

In Figures 10a, b,and c the variability of arrival angles is apparent. Again, the erroneous accumulation of events in the +5.0° segment should be disregarded in Figs. 10b and c. The photograph in figure 10d was taken shortly after Intercept No. 3-18 was recorded. While the variability during the measurement period was classed as VAR-3, it is obvious that during the period it was photographed it appeared to be a relatively stable signal.

VII. CONCLUSIONS

The Histogram Bearing Analyzer can provide existing direction finding systems with a capability to make more accurate bearing estimates upon signals whose angles of arrival are being subjected to a relatively high degree of variation. The limited amount of data (fewer than seventy DF measurements) collected and summarized under this effort have demonstrated that a significant improvement in DF measurement accuracy can be realized by incorporating the HBA as a supplemental read-out device for High Frequency Direction Finders.

While it is very tempting to quantitively analyze the degree of improvement offered by the HBA on the basis of the data contained in table 4, a much broader data base must be obtained before such an analysis can be justified.

The collection program under which this broadened data base is obtained must be designed to provide:

a. A basis of comparing the HBA measurements with the DF values obtained by averaging the DF input signal over selectable time periods. During the collection program conducted under this effort, the HBA display was allowed to accumulate and display a two-second "history" of continuously updated DF measurements. The AZ-Track Console, however, was operating at its fundamental display time constant of .03 seconds, charging the operator with the responsibility of mentally averaging and retaining the "history" of measurements over a period of several seconds. While it may be questionable as to which system was at a disadvantage under these operating procedures, a comparison on the basis of identifiable integration time periods should be made.

b. Very closely associated with (a) above is the requirement to more definitely identify the amount of signal

TABLE 5

TRANSMITTER LOCATIONS

INTERCEPT NO.	LOCATION	INTERCEPT NO.	LOCATION
1-1	Albuquerque, N.M.	1-27	Peoria, Ill.
1-2	Moline, Ill.	1-28	Mead, Neb.
1-3	Augusta, Ga.	2-1	Myertown, S. Africa
1-4	Chattanooga, Tenn.	2-2	Sackville,Canada
1-5	Downey, Cal.	2-3	Daventry, Eng.
1-6	L.A., Cal.	2-4	Bethany, Ohio
1-7	New Orleans, La.	2-5	Denby, Eng.
1-8	Ponca City, Okla.	2-6	Scakville,Canada
1-9	Albuquerque, N.M.	2-7	Sao Gabriel,Port.
1-10	Ft. Worth, Texas	2-8	Tangiers,Morocco
1-11	Punta Corda, Fla.	2-9	(Book) V.A.R.
1-12	Phoenix,Ariz.	2-10	Greenville, N.C.
1-13	Vaughan, Wash.	2-11	Greenville, N.C.
1-15	Pleas. Rock, Ky.	2-13	Sao Gabriel,Port.
1-16	Pleas. Rock, Ky.	2-14	Myertown, S.Africa
1-17	Miami, Fla.	2-15	Myertown, S.Africa
1-18	Vaughan, Wash.	2-16	Sackville,Canada
1-19	Bakersfield, S. Af.	2-17	Tangiers,Morocco
1-22	Salt Lake City, Ut.	2-18	Havana, Cuba
1-23	Scottsdale, Ariz.	2-19	Sackville,Canada
1-24	Luanda, Angola	2-20	Daventry, Eng.
1-25	Carlisle, Ky.	2-21	Bethany, Ohio
1-26	Peoria, Ill.	2-22	Sackville,Canada

TABLE 5 (Cont'd)

TRANSMITTER LOCATIONS

INTERCEPT NO.	LOCATION
2-23	Sao Gabriel, Port.
2-24	Greenville, N.C.
2-25	Greenville, N.C.
3-1	Sackville,Canada
3-2	Myertown,S. Africa
3-3	Sackville, Canada
3-4	Daventry, Eng.
3-6	Bethany, Ohio
3-8	Sao Gabriel, Port.
3-9	Tangiers,Morocco
3-10	Sackville,Canada
3-11	Sackville,Canada
3-12	Sao Gabriel, Port.
3-13	Myertown, S. Africa
3-14	Greenville, N.C.
3-15	Greenville, N.C.
3-18	Daventry, Eng.
3-20	Sackville, Canada
3-22	Daventry, Eng.
3-23	Daventry, Eng.
3-24	Myertown, S. Africa
3-25	Myertown, S. Africa

variation being observed during each of the simultaneous DF measurement periods. The three classes of signal variability used in this phase of the effort appear to have been inadequate; it is possible that they should be extended to a greater number of classes with consideration given to the frequency of variation.

c. Finally, an attempt should be made to obtain data over as broad a range of operating conditions as is possible. The data contained in tables 2,3, & 4 was obtained for the most part over daylight paths, on generally non-fading AM-voice signals in the 14-28 MHz band. Consideration should be given to signals at lower frequencies, and other forms of modulation, observed during periods of diurnal transition.

In addition to expanding the data base, the following modifications to the experimental hardware are recommended to improve the performance of the HBA model:

a. The present distribution logic of the model, allows excursions of the bearing dependent voltage in excess of $\pm$10V to be accumulated in the 50th counter channel. Such an accumulation gives an erroneously high indication of activity in the azimuthal segment of +4.8° to +5.0°. Additional comparator logic should be employed to inhibit the model's clock when the DF signal exceeds the +10V limit thus preventing such accumulations.

b. There is an ambiguity associated with the zero volt region of the HFLLDF bearing dependent voltage which serves as the input signal to the HBA experimental model. The HBA accepts the zero voltage level as an indication that the arrival angle of the RF signal is at the center of the 10° sector being examined ($\pm$10V = +5°). This voltage will also go to zero, however, when the RF signal level falls below the sensitivity of the HFLLDF receivers. The HBA should, therefore, be provided with threshold (RF Amplitude) logic which will inhibit all counter channels when the RF signal level approaches the DF system's sensitivity, thus preventing an erroneous accumulation of 0° events during deep RF signal level fades.

APPENDIX I

CIRCUIT TECHNICAL DESCRIPTION

Extracted from

"Instruction Manual for Digital Average Counter" July 1968.
Smyth Research Associates
San Diego, California

Prepared for

F30602-68-C-0313
Rome Air Development Center
Griffiss Air Force Base
New York

CIRCUIT TECHNICAL DESCRIPTION

The following discussion treats the circuitry on a board-by-board basis, describing in detail the function of each of the major components on the different circuit boards.

A. PWR 2B, Drawing No. 11

The line voltage from the chassis is switched through S1 to the isolation and step-down transformer, T1. The secondary windings are paralleled to provide up to 3A of current. CR1 is a fullwave bridge rectifier followed by an LC filter consisting of T2 and C1. A voltage doubler consisting of CR2, CR3, C2 and C3, develops a higher voltage which supplies power to the reference and regulator circuitry. A constant current circuit (R1, R3, CR4, CR5, Q1) provides bias for the reference, Q2. This transistor is connected such that the collector-base diode is forward biased and the base-emitter diode is reverse biased to break down. This connection provides a temperature compensated +6.7 volts. R2 and CR7 regulate the supply voltage for Amplifier A1 to be +18V. Operational amplifier, A1 is connected as a voltage follower with its input at Pin 3. The output Pin 7, drives the emitter follower string Q3 and Q4. The output of Q4 passes through R10, to the positive output at Pin C. Pin 3 is the output sensing lead which, when connected to Pin C, provides negative feed-back through R7 to A1 input, Pin 2. Transistor Q5 senses the output current by measuring the voltage across R10. When this voltage forward biases the base-emitter junction of Q5, the transistor conducts, thus removing the drive to the emitter follower string. The maximum current is approximately 3A. Lamp DL1 is used to provide a visual display that the voltage is not excessive or that the supply is not in current limit.

Transformer T3 steps the line voltage down to a level sufficient to drive the displays. This power is half-wave rectified to provide two phases of lamp power with a maximum load of 1A on each phase.

B. PWR 3B, Drawing No. 12

The line voltage from the chassis is switched through S1 to the isolation and step-down transformer, T1. The secondary windings are connected to two identical 15 V regulator circuits. The outputs of these regulators are connected such that plus and minus 15 volts are provided at the outputs. Since these two regulators are identical, only the +15 V section will be discussed. The 1-3 secondary is connected to the bridge rectifier, CR3, and the rectified power is filtered by Capacitor C4. A voltage doubler (DR1, DR2, and C2 and C3) provides power for the

reference supply and the amplifier. Q1 is used as a 6.7 volt zener diode to bias Q2 as a constant current generator. The output of Q2 is regulated to +30 volts by diode CR7. Q3 is used as a zener diode to provide bias for Q4 which delivers a constant output current into Q5 which is also used as a temperature compensated zener diode. The voltage at the collector of Q5 is used as the reference voltage for Pin 3 of the operational amplifier, A1. The closed loop gain of A1 is controlled by the divider network, R6, R9, and R10. The output of A1 drives the emitter follower string Q6 and Q7. The output current of Q7 flows through R12, for current sensing, then to output, Pin 1A. The output voltage is set by Resistor R9. When the output current exceeds 1 amp, Q8 begins to conduct and the drive current is removed from the emitter follower string. Display lamp DL1 is provided as an indication of proper supply operation.

C. Clock PCB, Drawing No. 13

The CLOCK PCB contains a crystal controlled multivibrator, a frequency divider to develop the clock frequencies, dividers and pulse forming circuits to develop the store and shift pulses and the reset circuit. The clock frequencies were initially chosen on the basis of the following design.

1. The 8-bit counter has a maximum count of 225 and cannot be counted beyond this level without losing information. It must be shifted prior to this time.

2. If a counter is shifted (divided by two) every Nth clock pulse, it cannot count beyond 2N.

3. Select 2N to be 250 thus N=125=5x5x5, which is a convenient number to divide by. The clock frequency will then be 125 times higher than the store and shift rates.

4. By definition, the "averaging period" is the time required for the counter to decay to .5 rather than .37 as in an RC circuit. This period then is the period of the store and shift rates.

5. The desired average periods and resulting frequencies are as follows:

AVERAGE PERIOD (T)	SHIFT and STORE FREQ (/T)	CLOCK FREQ (125/T)
.1 sec	10 Hz	1250 Hz
.2	5	625
.5	2	250
1	1	125
2	.5	62.5
5	.2	25.
10	.1	12.5

The multivibrator uses two nand gates (M1A and M1B) as amplifiers with resistive bias (R1 and R2) and the crystal (Y1) to close the positive feed-back loop. The output at Pin 6 is then a square wave at a frequency of 200 KHz. This frequency is divided by two (IC1), then by ten (IC2) to provide 10 KHz. 10 kHz is buffered (M2A) and provided as an output to drive the scanner. 10 kHz also is divided by four (IC3), then by two (IC4) to become 1250 Hz, one of the clock frequencies. Integrated circuits IC5, IC6 and IC7 continue this division process to yield the clock frequencies shown at the input to AVERAGE PERIOD switch S1. The HOLD position of this switch stops the clock and shift pulses to allow comparison of the counter contents and the HISTOGRAM display.

The output of Switch S1 is fed to the buffer M2C and then is differentiated in C4 and the input network of A1. The negative pulse is amplified and limited by A1 to produce a positive going 0.7 microsecond pulse. This pulse is inverted and buffered to produce the 5 coherent CLOCK outputs.

The output of A1 also goes to IC8, IC9 and IC10, where its rate is divided by 125. If there is no RESET command then this frequency is passed through M11 to the pulse forming networks, each generating a 7 microsecond pulse, with each pulse being successively delayed in time. The first pulse out, from A2, is buffered (M12), then provided as the SYNC pulse for the scanner. The second pulse out, from A3, is inverted and buffered to become the five STORE' pulses. The third pulse out, from A5, is delayed 7 microseconds by A4 and is buffered to become the five SHIFT' pulses.

If the RESET switch is depressed or if a RESET pulse is received, the gates M10 and M11 switch 10 kHz in as the store and shift rate which clears the counters in less than 0.8 ms.

The diodes, CR1, CR2, CR3 and CR4 are provided voltage

dropping devices since the uL900 and uL914 power requirements are +3.6 V rather than +5 V.

D. SCANNER PCB, Drawing No. 14

The SCANNER consists of a counter, a BCD-to-10 line decoder, and a BCD-to-analog decoder. The counter consists of two BCD decode dividers (IC2 and IC3) and a BDC divide-by-five network (IC1). The input frequency of 10 kHz when divided by 500 yields 20 Hz, the sweep frequency. IC4 and IC5 decode the tens and hundreds of the counter into ten-line outputs which are buffered to become the SCAN numbers.

The DIGIT-TO-CURRENT CONVERTER decodes all bits of the counter to produce a current out of Pin SP (summing point) which is proportional to the BDC contents of the counter. Amplifier A1 converts this current into a voltage which is inverted and buffered to provide the SWEEP OUTPUT. Note that since the SCAN Nos. are derived from only IC1 and IC2, and the sweep includes IC3, that the scanning of any one counter occurs for 10 counts of the 10 kHz input. Pin 11 of IC3 is used as the BAR command and is in the one state for the last 20 percent (or two counts) of each counter scan. The BAR command therefore chops the HISTOGRAM OUTPUT to zero after each counter is scanned to produce the bar graph appearance in the histogram display.

E.LOGARITHMIC AMPLIFIER, Drawing No. 15

For the purpose of clarity the log amp will be discussed as three separate circuits;the inverter, A1 and A2; the log circuit, A3, A4, A5 and A6; and the output circuit, A7 and A8.

The inverter circuit is used to provide a positive input to the Log circuit when the input sign is negative. Amplifier A1 is a thermally stabilized differential pair of transistors used as a preamplifier to drive the differential input operational amplifier, A2. Feed-back is provided around A1 and A2 to insure a gain of -1.00. The inverter is switched in or out of the circuit as needed by the INPUT SIGN Switch S1.

The log circuit utilizes a high gain amplifier with exponential current feed-back to obtain a logarithmic transfer function. The high gain amplifier consists of the thermally stabilized transistor pair, A3, followed by the operational Amplifier,A4. The change in base-emitter voltage drop of the feed-back transistor (in A5) is proportional to the collector currents of the transistor pair in the following manner:

$V_{be} = (kT/q)\ln(K_C/I_{C2})$. This base emitter voltage drop is amplified by the operational amplifier, A6, to provide a

voltage at TP7, V_7, which is related to the input by approximately: $V_7 = 8-2^7 \log_{10} (V_{in}/1mV)$ volts. Trimming of the circuit is used to provide exactly this function.

The output circuit translates, inverts, and adjusts the gain to provide the function: $V_0 = 20\ (SLOPE) \log_{10} (V_{in}/THRESHOLD)$. When the ratio V_{in}/THRESHOLD is less than unity and approaching zero the output would attempt to reach negative infinity. To prevent saturation of several amplifiers, the output amplifier, A7, and amplifiers A4 and A6 are diode clamped and limited, thus providing zero output for V_{in}/THRESHOLD less than unity. Amplifier A7 performs inversion and gain selection by the Switch S3. Amplifier A8 provides a selected offset or translation by Switch S2, thus setting the THRESHOLD.

F. BUFFER and D/A PCB, Drawing No.16

This board contains the input buffer and amplitude scaling circuit, the references for the divider string, the active filter, and output digital-to-analog decoder. The input buffer amplifier, A1, provides unity gain and inversion by utilizing negative feed-back (R3) around a high gain operational amplifier. The gain is set by the ratio of R1 to R3, which are precision resistors. The signal is re-inverted in Amplifier A2 and divided by 5 to provide a swing of +2 volts at the SIG OUTput for a ±10 volts swing at the SIGNAL IN jack. The gain of A2 is set by the ratio of R5 into the parallel combination of R9 and R13. Positive and negative 2 volt references are supplied by a resistive divider consisting of R14, R15, R16, R17 and the precision divider resistors in the counters.

The active filter consists of FET operational Amplifier A3, input Resistor R18, and Feed-back Components R19, and C11 to C17. The DC gain of the filter is the ratio of R18 to R19 and is unity. The bandwidth is set by one of the capacitors having a reactance equal to R19 at the corner frequency. The bandwidth is selected by Switch S1.

The digital CARRY inputs from the counters are decoded into an analog current in the DIGIT-TO-CURRENT CONVERTER. This current is transformed into a voltage at the output of Amplifier A4. This voltage ranges from zero, at all zeros in, to -5 volts for all ones in. This voltage is inverted with unity gain by Amplifier A5, the gain being the ratio of (R30 + R31)/(R28 + R29) The output of A5 becomes the LINear HISTOGRAM OUTPUT and the input to the LOG AMP. This voltage is periodically chopped to zero by Q1 to provide the histogram bars. Switch S3 selects the OUTPUT from either A5 or the LOG AMP output.

G. CTR-2 PCB, Drawing No. 17

This board contains one channel of the Digital Average Counter. It consists of the COMPARATOR and gate circuit, the COUNTER and display section, the STORAGE REGISTER, the SHIFT GATES, and the OUTPUT SCANNER network.

The COMPARATOR, A1, accepts its reference from Pin 15 which is connected to PIN (DIV) of the previous counter. The signal input is from Pin 14R. When the signal exceeds the reference (more positive) then the COMPARATOR output, Pin 6, goes to zero. If the signal has not exceeded the reference of the preceding counter, then 'N+1' is a one, thus allowing the CLOCK to pass through M12 and M13C to become the COUNT pulse. The dual flip-flops, FF3, FF4, FF5 and FF6 comprise the 8-bit binary ripple COUNTER. The outputs of the COUNTER drive transistors Q1 to Q8 which, in turn, control the display lamps DL1 to DL8.

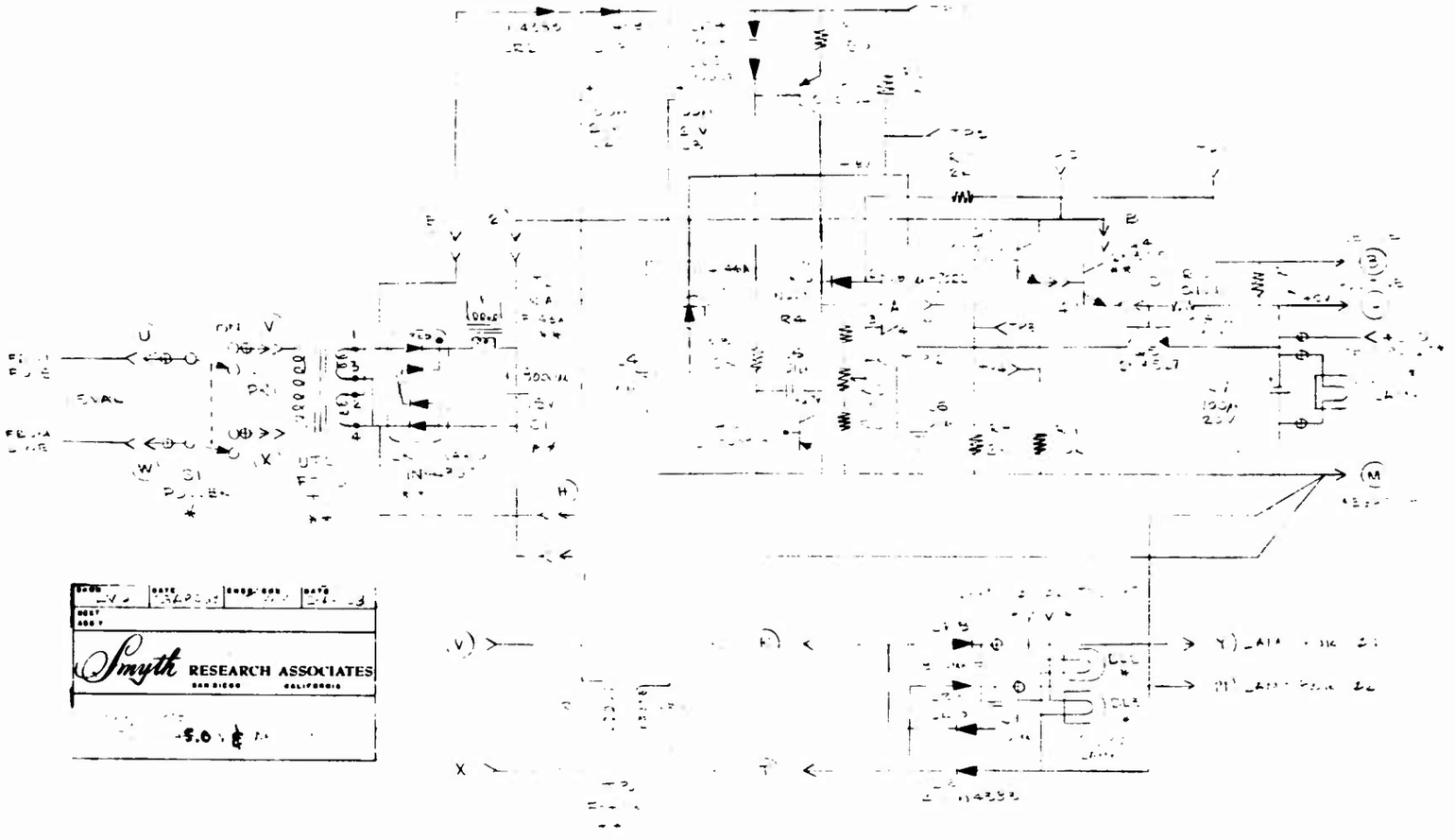
The outputs of the COUNTER are also fed back to the STORAGE REGISTER, FF1 and FF2. These two IC's contain four storage flip-flops each. The STORE'PULSE Pin 19W, is inverted and buffered in M1A to become the STORE command. Upon receipt of this command FF1 and Ff2 assume the states of the COUNTER with the exception that the REGISTER is wired with its inputs shifted down one bit.

Following the STORE'PULSE is the SHIFT'PULSE, Pin 18V, which is inverted and buffered in M12A to become the SHIFT command. Upon receipt of the SHIFT command the SHIFT GATES reset the COUNTER to the states of the STORAGE REGISTER. The COUNTER then proceeds to count on receipt of the next COUNT pulse.

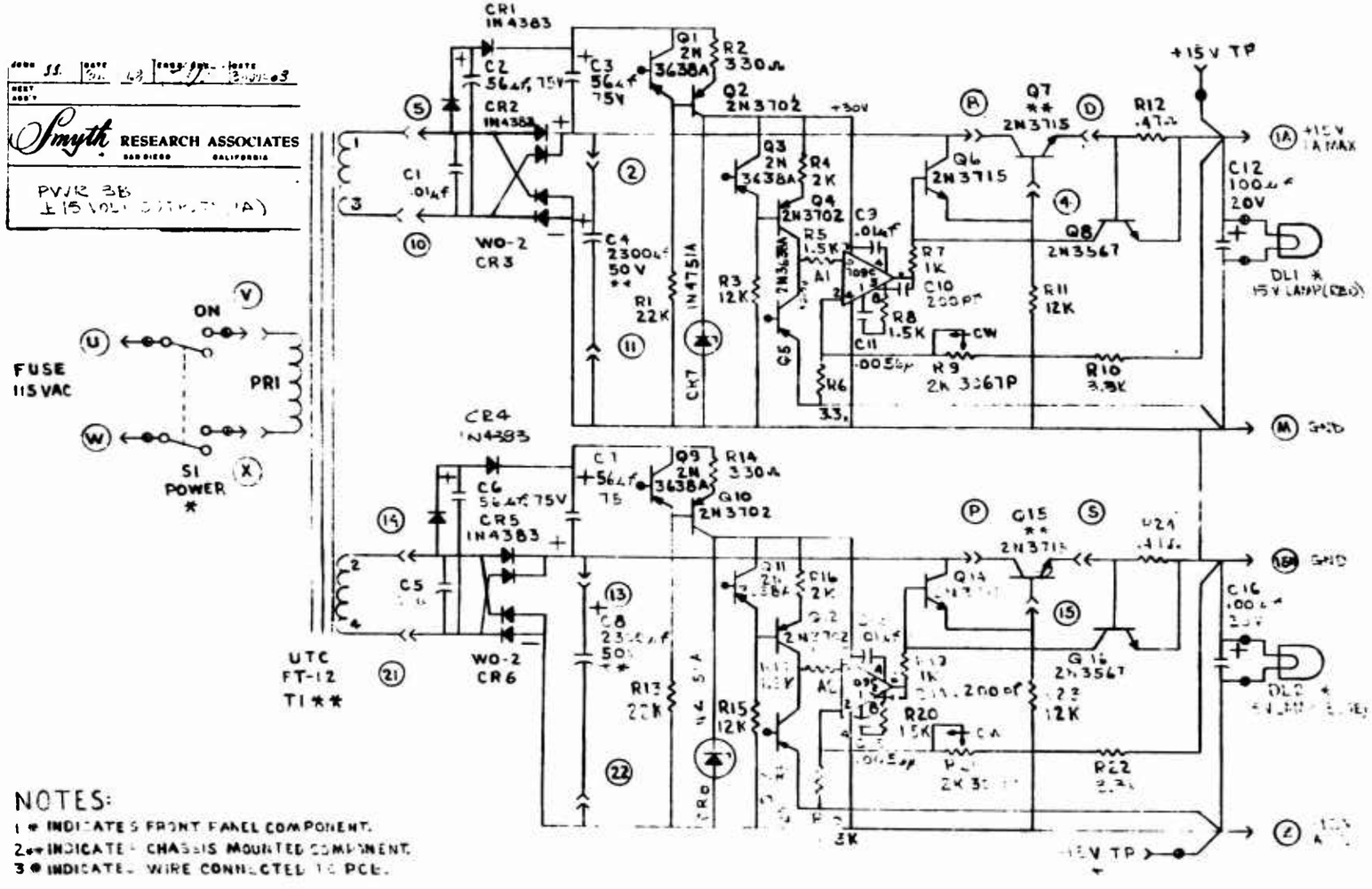
The COUNTER outputs are also connected to eight exclusive-nor gates, M4 to M7, in the OUTPUT SCANNER. The outputs of these gates are inverted in M2 and M3 to become the eight OUTputs. The transfer function of these gates is the following:

$$OUT\ n = CARRY\ n + SCAN \cdot BIT\ n$$

The SCAN command is generated in the gate M1B and M1C from the SCAN Nos. Only one SCAN command is generated among all the counters at any given time. Thus the SCAN command gates the counter bits to the OUTputs. These OUTputs are connected to the CARRY's of the next counter and gated on through it. The bits from the counter being scanned finally appear at the OUTput of Counter No. 49, where they are converted into the histogram display by the SCANNER module.



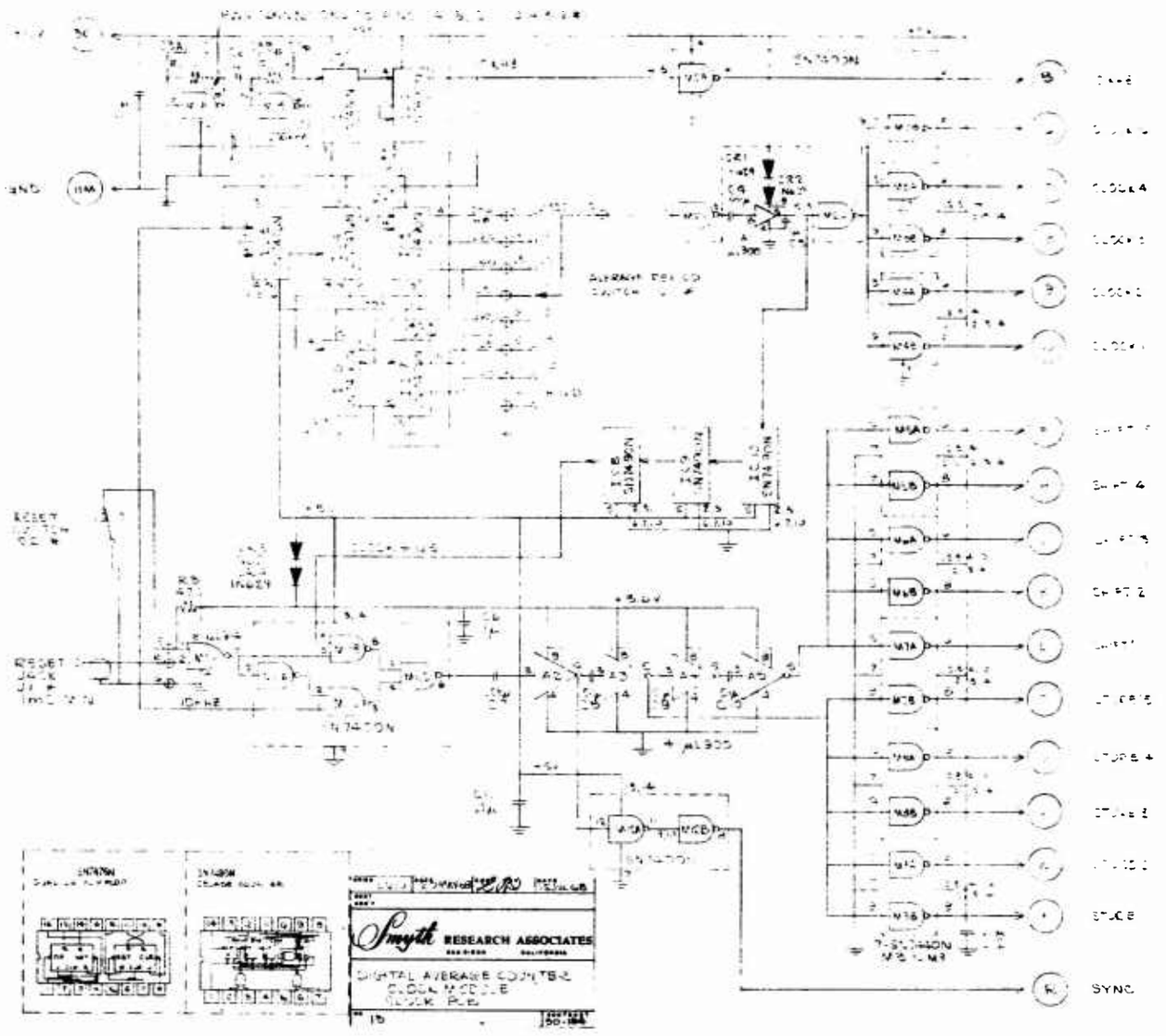
PWR 2B, Drawing No. 11



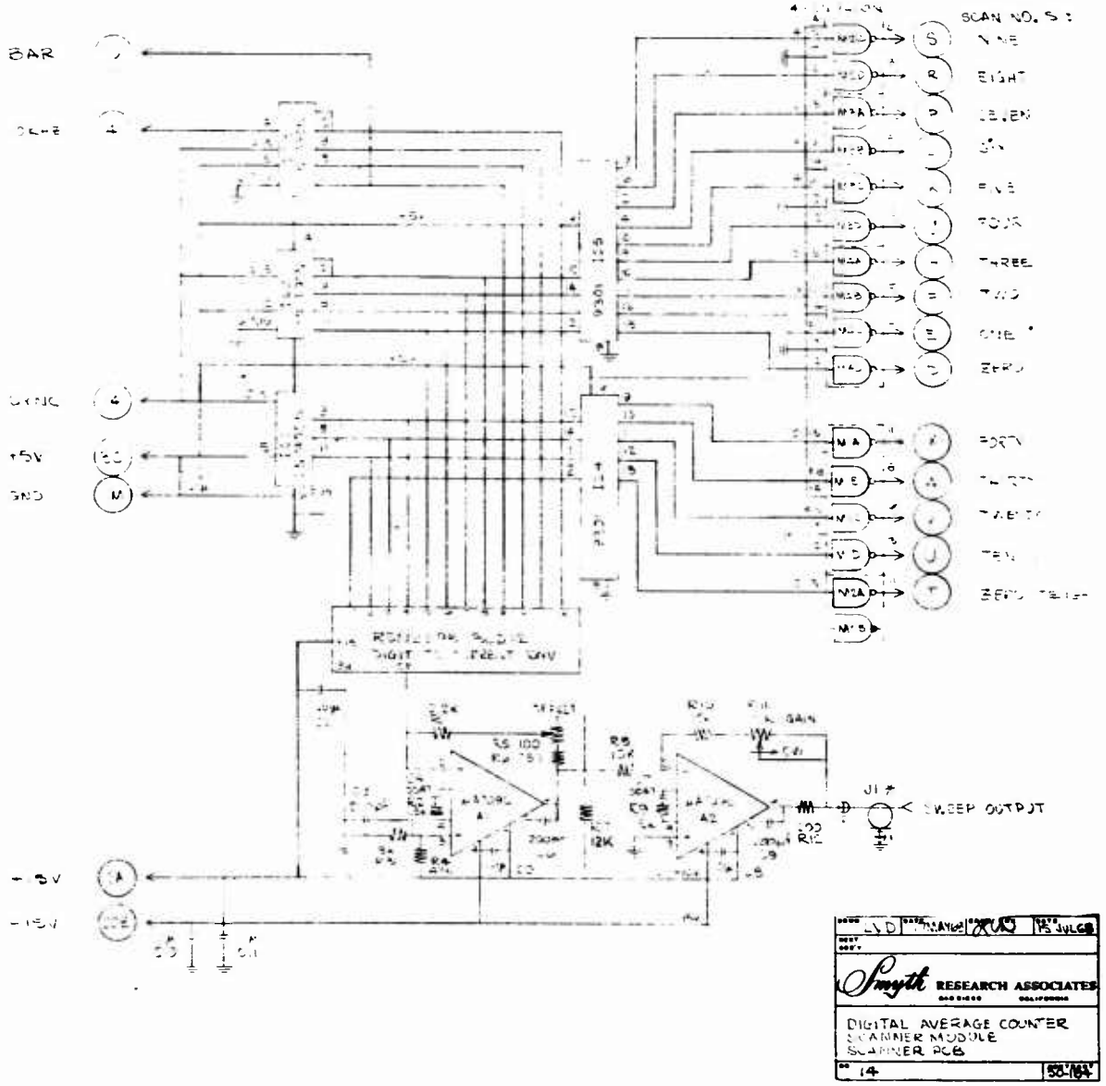
NOTES:

1 * INDICATES FRONT PANEL COMPONENT.
2 ** INDICATES CHASSIS MOUNTED COMPONENT.
3 * INDICATES WIRE CONNECTED TO PCB.

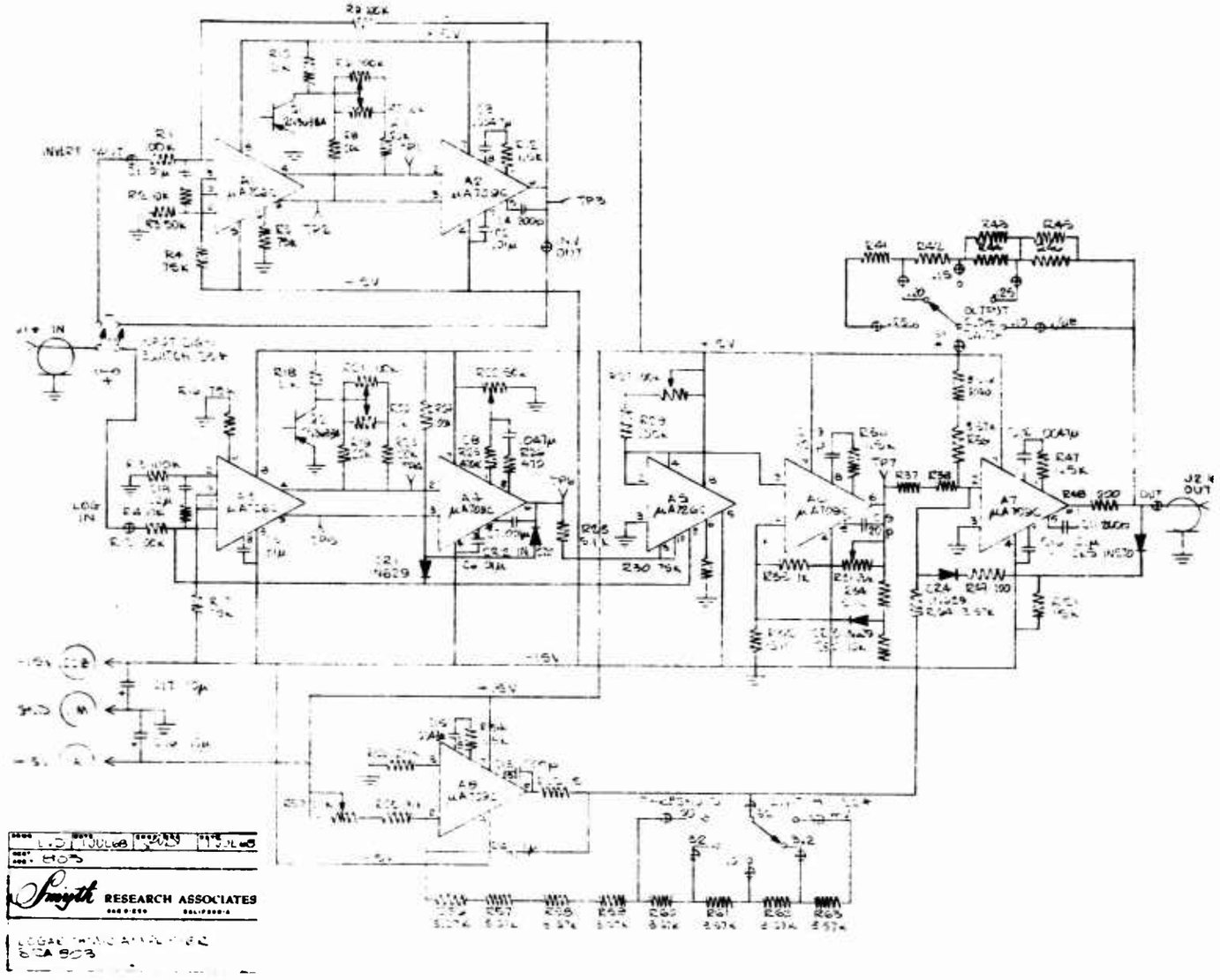
PWR 3B, Drawing No. 12



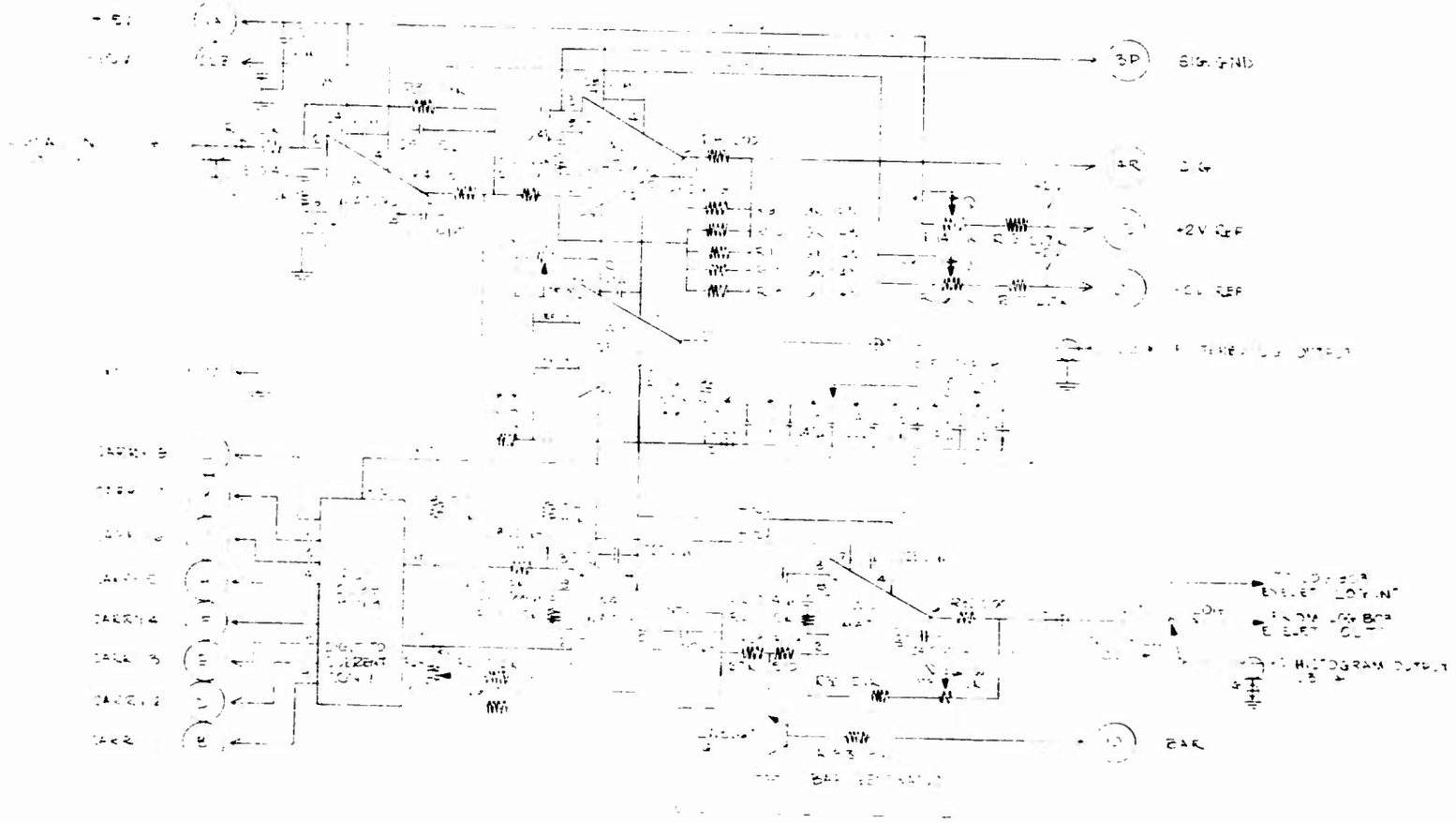
CLOCK PCB, Drawing No. 13



SCANNER PCB, Drawing No. 14



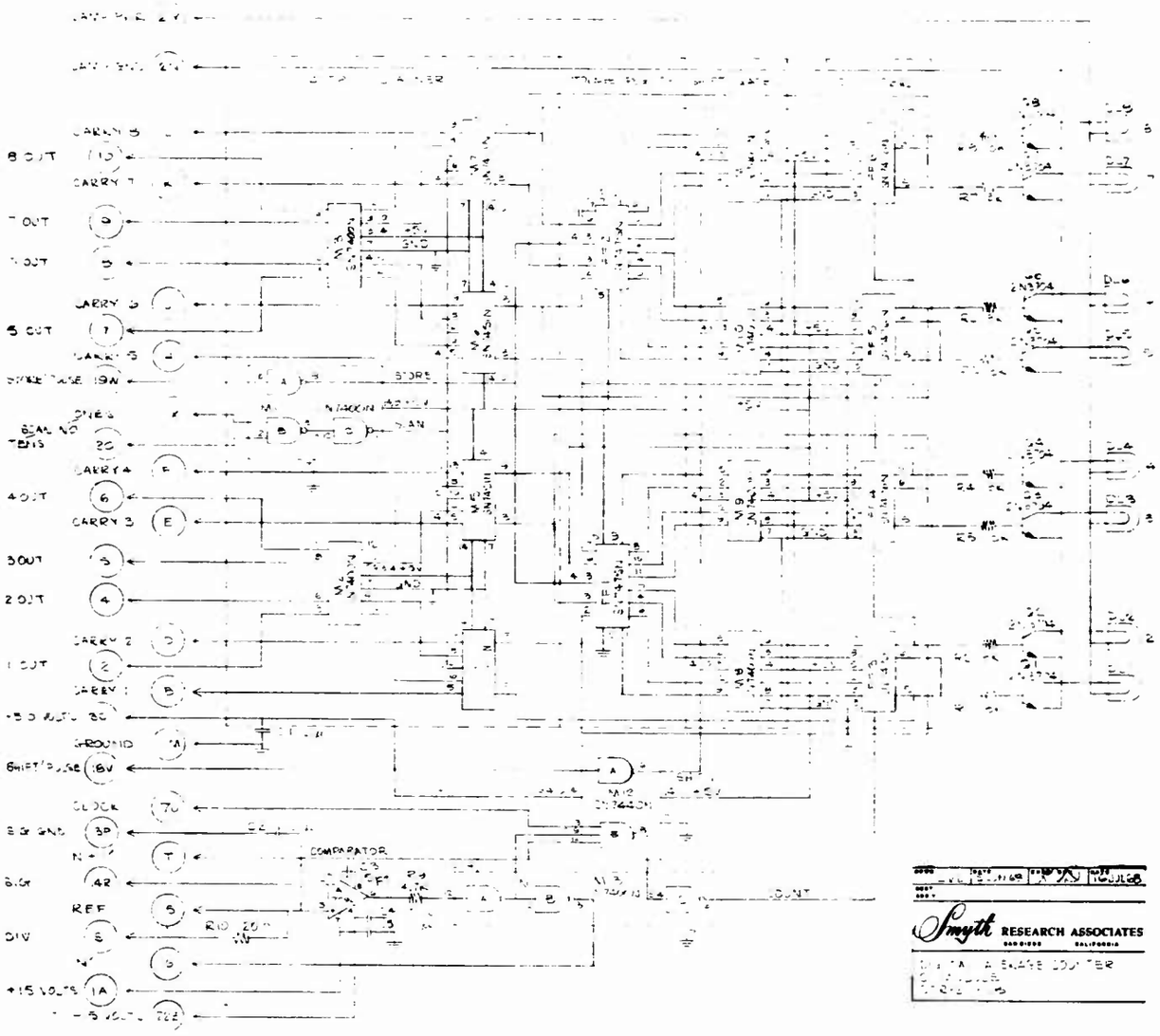
LOGARITHMIC AMPLIFIER,
Drawing No. 15



Smyth RESEARCH ASSOCIATES

DIGITAL AVERAGE COUNTER
SCANNER MODULE
BUFFER & D/A PCB

BUFFER and D/A PCB,
Drawing No. 16



CTR-2 PCB, Drawing No. 17

APPENDIX II

"Acceptance Test Procedures"
and Results June 1968

Prepared by

Smyth Research Associates

For

F30602-68-C-0313
Rome Air Development Center
Griffiss AFB, NY

APPENDIX II

I. INTRODUCTION

The following test procedures cover the Digital Average Counter Unit being constructed for this contract, and also cover the testing of the Clock and Scan Control Unit which is an integral part of the Digital Average Counter System. When the system passes the following tests it will comply with its specifications.

II. TEST PROCEDURES

Place the five chassis in a suitable rack and attach the four jumper cables. Place the POWER switch of each chassis in the off position. Plug the line cords into a 115 VAC, 60 cycle power source.

A. Power Supply Test

Place the POWER switch of each chassis in the ON position. Using a digital voltmeter or a VTVM calibrated to better than 1% accuracy, measure the voltage at all power test points labeled +5, ±15 or -15 to be +5.0, ±15.0 or -15.0, respectively, within ±2 percent. The voltage of the LAMP test points is approximately +28 volts, unregulated. No tolerance is specified here. The only requirement here is that there is sufficient power to light the lamps in the counter (C) modules.

Use a Variac (model W5MT3 or equivalent) to vary the line voltage ±10 percent around 115 VAC. Observe that all regulated test point voltages vary less than ±1 percent. Using an oscilloscope, verify that the 120 Hz ripple at the regulated power supply test points does not exceed 10 mV peak over the range of input voltages.

B. Reset Test

Apply a 10-volt peak sine wave to the SIGNAL IN jack on the SCANNER module. Use a frequency of 1 Hz. Set the AVERAGE PERIOD switch in the 1 SECOND position. Observe that all 50 counters have some count on the displays. Press the RESET button on the CLOCK module and observe that all counter lamps go out. Apply a +3 volt step at the RESET jack and observe that all counter lamps go out and that the HISTOGRAM OUTPUT is zero volts when all lamps are out. Remove the RESET voltage. Place the AVERAGE PERIOD switch in the HOLD position and check that all counters stop.

C. Average Period Test

Apply zero volts to the SIGNAL IN jack and place the LIN-LOG switch in the LIN position. Observe the Histogram OUTPUT, with an oscilloscope, to be a pulse. The height of the pulse should drop to one-half at a rate equal to the switch selected AVERAGE PERIOD (10, 5, 2, 1, 0.5, 0,2, or 0,1 seconds).

D. Filtered Signal Output Test

Apply a sinusoidal signal to the SIGNAL IN jack. Using an oscilloscope observe the FILTERED SIG OUTPUT jack to check that the low frequency gain is 1.0 $\pm$2% and that the gain drops to 0.7 at the switch selected FILTER BW (bandwidth) of 10, 5, 2, 1, 0.5, 0.2, or 0.1 Hz.

E. Linear Histogram Test

Connect the SWEEP OUTPUT to the horizontal input of an oscilloscope and connect the HISTOGRAM OUTPUT to the vertical input of the oscilloscope. Adjust scope sensitivities for a full screen display (approximately 5 volts p-p). Set the AVERAGE PERIOD switch in the 2 SECOND position; set the LIN-LOG switch in the LIN position. Make the following tests on each channel as the input signal is manually varied continuously from +10.0 to -10.0 volts:

1. Verify that the operating counter is in sequence (top to bottom and left to right).

2. Verify that the histogram display of the counter contents is in sequence (left to right).

3. Verify that the display rises linearly and falls to one-half every two seconds.

4. Verify that the previous counter display falls to one-half every two seconds until it reaches zero.

F. Logarithmic Histogram Test

Place the LIN-LOG switch in the LOG position. Observe that the operating counter display rises rapidly and decays in equal steps.

SPECIFICATIONS

SIGNAL INPUT RANGE (VOLTS).....±10

INPUT IMPEDANCE (K ohms).....19

NUMBER OF CHANNELS.....50

RESOLUTION OF EACH CHANNEL.....1 part in 250

CHANNEL COUNT BINARY DISPLAY (BITS).....8

SWEEP RATE (HZ).....20

SWEEP OUTPUT RANGE (VOLTS).....0 to +5

SWEEP OUTPUT CURRENT (mA max).....5

HISTOGRAM OUTPUT RANGE.....
LIN, count 255 (volts).....+5
count 0 (volts).....0
LOG, count 255 (volts).....+5.4
count 0 (volts).....0
slope (volts/6 dB)..... .75

HISTOGRAM OUTPUT CURRENT (mA max).....5

FILTERED SIG. OUTPUT RANGE (VOLTS).....±10 V

FILTERED SIG. OUTPUT CURRENT (mA max).....5

FILTERED SIG. OUTPUT BANDWIDTH (Hz)..... .1, .2, .5, 1, 2, 5, 10

AVERAGE PERIOD (SECONDS)..... .1, .2, .5,
(HOLD position stops all counting)..... 1, 2, 5, 10

RESET INPUT IMPEDANCE (ohms).....500

RESET INPUT VOLTAGE (max).....+5
(min).....+1

RESET PULSE WIDTH (ms - min).....1

POWER REQUIREMENTS
VOLTAGE (±10%).....115
FREQUENCY (Hz).....60
POWER (PER CHASSIS - WATTS).....100

PHYSICAL DIMENSIONS (5 CHASSIS)
26 1/4" H x 10" D x 19" W - rack mounting

Table II-1

DAC ACCEPTANCE TEST DATA SHEET

IIA. Power Supply Test

CH NO.	LINE VOLTAGE				TEST POINT
	104 RIPPLE	104 DC TEST	115 DC TEST	127 VAC DC TEST	
1	5mVp	4.99	5.00	5.00	+5V
		-	13	-	01
		-	13	-	02
2	10	4.97	5.00	5.00	+5V
		-	13	-	01
		-	13	-	02
3	7	4.98	5.01	5.01	+5V
		-	13	-	01
		-	12.6	-	02
4	5	4.96	5.01	5.01	+5V
		-	13	-	01
		-	13	-	02
5	2	5.00	5.01	5.01	+5V
		-	13	-	LAMP
	1	15.00	15.02	15.02	+15V
	1	-15.02	-15.02	-15.02	-15V

IIB. Reset Test

MANUAL RESET	ok
ELECTRONIC RESET	ok
HOLD	ok

IIC. Average Period Test

PERIOD: 10 SEC	ok
5	ok
2	ok
1	ok
.5	ok
.2	ok
.1	ok

IID. Filtered Sig Output Test

DC GAIN	1.00	(1.00 ±02)
BANDWIDTH	9	(10 Hz)
	2.7	(5)
	1.4	(2)
	0.7	(1)
	0.28	(.5)
	0.14	(.2)
	0.06	(.1)

IIE. Linear Histogram Test

COUNTER NO.	TEST NO. 1 2 3 4	COUNTER NO.	TEST NO. 1 2 3 4
0	_ _ok _	25	_ _ok _
1	_ _ok _	26	_ _ok _
2	_ _ok _	27	_ _ok _
3	_ _ok _	28	_ _ok _
4	_ _ok _	29	_ _ok _
5	_ _ok _	30	_ _ok _
6	_ _ok _	31	_ _ok _
7	_ _ok _	32	_ _ok _
8	_ _ok _	33	_ _ok _
9	_ _ok _	34	_ _ok _
10	_ _ok _	35	_ _ok _
11	_ _ok _	36	_ _ok _
12	_ _ok _	37	_ _ok _
13	_ _ok _	38	_ _ok _
14	_ _ok _	39	_ _ok _
15	_ _ok _	40	_ _ok _
16	_ _ok _	41	_ _ok _
17	_ _ok _	42	_ _ok _
18	_ _ok _	43	_ _ok _
19	_ _ok _	44	_ _ok _
20	_ _ok _	45	_ _ok _
21	_ _ok _	46	_ _ok _
22	_ _ok _	47	_ _ok _
23	_ _ok _	48	_ _ok _
24	_ _ok _	49	_ _ok _

IIF. Log Histogram Test

ok

ADDITIONAL DATA:

TRANSITION VOLTAGES (CLOCK SPLIT BETWEEN TWO ADJACENT COUNTERS):

+9.63	+4.80	-0.01	-4.83	-9.67
9.22	4.41	-0.40	-5.24	-10.01
8.82	4.00	-0.82	-5.64	
8.39	3.60	-1.22	-6.05	
7.99	3.21	-1.64	-6.47	
7.62	2.80	-2.02	-6.86	
7.21	2.40	-2.43	-7.27	
6.80	2.01	-2.83	-7.64	
6.41	1.60	-3.24	-8.06	
6.01	1.19	-3.64	-8.47	
5.58	0.79	-4.02	-8.85	
5.21	0.39	-4.42	-9.26	

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13. ABSTRACT

The Experimental Model Radio Direction Finding (RDF) Histogram-Time Averaging Processing System (Histogram Bearing Analyzer) and the data collection program conducted to determine its performance characteristics are described. Data comparing the capability of the Histogram Bearing Analyzer with a more conventional HF/DF readout system are presented. Recommendations for improvements in the model's performance and continued experimentation are suggested.

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	ROLE	WT	ROLE	WT	ROLE	WT
Display, Histogram, DF Read-out Console						

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