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# STRESS INDUCED INTERMITTENT FAILURES IN ENCAPSULATED MICROCIRCUITS

DE-69-3

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# STRESS INDUCED INTERMITTENT FAILURES IN ENCAPSULATED MICROCIRCUITS

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DE-69-3

# FOREWORD

This report represents some results of an in-house microcircuit testing and failure analysis program partially funded under RADC Discretionary Fund Project DE-69-3, entitled, "Reliability Physics Studies on Integrated Circuits."

The test method "Monitored Thermal Cycle," included as appendix B, will be submitted for military and industrial coordination for inclusion in MIL-STD-883 "Test Methods and Procedures for Microelectronics."

This technical report has been reviewed by the Office of Information (RAI) and is releasable to the Clearinghouse for Federal Scientific and Technical Information.

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# ABSTRACT

The problem of temperature intermittent operation in encapsulated integrated circuits is discussed, and a technique presented which has been effective in detecting potential failures resulting from metallization, bond or lead wire temperature intermittents. These are the main causes of intermittent operation in encapsulated microcircuits at present, and this technique should lead to improvement in encapsulated device reliability if implemented as a screening or qualification test.

The instrumentation used at RADC for this technique, called the Monitored Thermal Cycle Test (MTC), is presented and a proposed standard test method, based on this test, is included as an Appendix. Several representative device failure analysis summaries illustrate the cause of typical encapsulated integrated circuit intermittents resulting from failure of the lead wire-bond-interconnect system.

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## 1.0 INTERMITTENCY IN INTEGRATED CIRCUITS

The objective of this report is to present a screening technique for eliminating potential intermittent failures in microcircuits. Thermal intermittency, in particular, has been a problem especially prevalent in encapsulated devices. The major cause of thermal intermittency in encapsulated devices has been used as the basis for a Monitored Thermal Cycle (MTC) test. The test has proved to be a very effective screen for eliminating potential thermal intermittent failures in encapsulated microcircuits. Devices which tested electrically good after a previous stress history were found to be failures on the Monitored Thermal Cycle test, and a representative failure analysis is presented for several typical failures.

### 1.1 CHARACTERIZATION OF INTERMITTENT FAILURES

The thermal intermittent integrated circuit is a major reliability problem at present. It fails in a system; then retests satisfactorily prior to failure analysis. Although it is usually very difficult to trace such failures, they can be characterized by one of two major classes. The first class, parameter drift, can cause a device to fail at certain temperatures. If the characteristics of a particular component or group of components on a chip change sufficiently with time and temperature, the integrated circuit will cease its normal operation as required by the system. This first class includes such things as increased leakage current, changes in breakdown voltage, transistor current gain degradation, and similar related mechanism.

The second class of failures includes the general problem of continuity from the external lead through the lead frame, through various bonds and wires, through the deposited metallization, and, finally, to the chip connection itself. This results in device failure at specific temperatures due to poor bonding, intermetallic formation, poorly placed lead wires, metallization problems, and any other weak areas in the interconnection system influenced by thermal or mechanical stresses.

Various screening and burn-in tests have been developed to weed out potential failures of the first class, which are caused by increased leakage current beta drift, breakdown voltage reduction, and related mechanisms.[1] Although these tests are not 100 percent effective, they can detect a large number of potential failures before a device is shipped from the plant. The second class of failures is presently of main concern because of the increasing volume of plastic encapsulated microcircuits being produced. Tests, such as bond pulling, visual inspection, mechanical shock, vibration, and centrifuge have finally become effective for high reliability hermetic microcircuits. These lot qualification and screening tests are for the most part ineffective or of limited value when applied to plastic encapsulated devices which are presently being considered for high reliability application.

### 1.2 THERMAL INTERMITTENCY PROBLEM

In failure analysis, the failure mechanism characteristic of the second class of failures has often been traced to a lead or bond which makes pressure type of contact at one temperature, but opens at another due to thermal expansion and contraction. This is the major mechanism in the second class of failures, other than transients and electrical overstresses (ZAPs), which are not device related problems, but rather equipment design problems. With the increasing use of plastic encapsulated integrated circuits, this problem of temperature intermittency has become serious. Since the internal leads are completely surrounded by a rigid or semirigid material of different thermal expansion characteristics, it is even more likely that a lead may be pulled from a bonding pad or lead frame as the temperature is changed. Also, the normal molding operation may result in excessive stresses in the lead which could increase chances of eventual failure, either because of the injection pressure during fabrication or by shrinkage during the cure. Based on results or various high stress tests, metallization corrosion and bond breakage due to thermal mismatch were found to be the main failure mechanisms of encapsulated microcircuits[2].

In some cases, the device power dissipation raises the temperature enough to cause a failure which automatically corrects itself when power is removed. Sometimes a failure can occur at lower than ambient temperature. In all these instances, the overall effect is to produce a system which may be intermittent in operation, a situation which makes it very difficult to localize the problem. The solution to this is to monitor the individual integrated circuit parameters over the temperature range of the device (not just at temperature extremes, since some devices are failures only over a narrow band of elevated temperature) before the device is put into use.

### 1.3 DETECTION OF POTENTIAL THERMAL INTERMITTENTS

Electrical characterization at temperature extremes (without even considering the possibility of measurements over the complete temperature range) is impractical from an economic standpoint. This is due to the large number of measurements possible, the difficulty of maintaining the devices and associated test socket at the required temperature, and the need to test one device at a time even with an automatic system. Since a large percentage of thermal intermittency failures has been attributed to opening of the lead, bond, contact cut, etc. (rather than chip/circuit functional failure), a simple test was implemented to monitor a group of integrated circuits as they are cycled thermally and detect any open leads using a threshold type of measurement. This technique, which is called the "Monitored Thermal Cycle Test (MTC)," is presently being used as an evaluation tool for plastic encapsulated integrated circuits, and is also being considered as a possible screening procedure. It has been proposed as a periodic sampling qualification test for plastic microcircuits.

## 2.0 IMPLEMENTATION OF MONITORED THERMAL CYCLE TEST

The problem of detecting thermally intermittent integrated circuits can be divided into two major parts. The first part is the equipment required to cycle the devices through the temperature range of interest. This may be any one of several commercially available, programmable temperature cycling chambers, capable of operation both below and above room temperature. The second part is the instrumentation used to monitor the operation of a large number of integrated circuits as they are cycled over the selected temperature range. This instrumentation can be of any configuration that will provide useful information on a circuit over the duration of test. Several possible approaches are available to the test design engineer. The procedure used by RADC and described below should serve to set operating limits and furnish general guidance rather than as a firm system/equipment requirement.

Figure 1 shows a block diagram of the system used by RADC to perform the tests presently being used in one of the many phases of plastic encapsulated

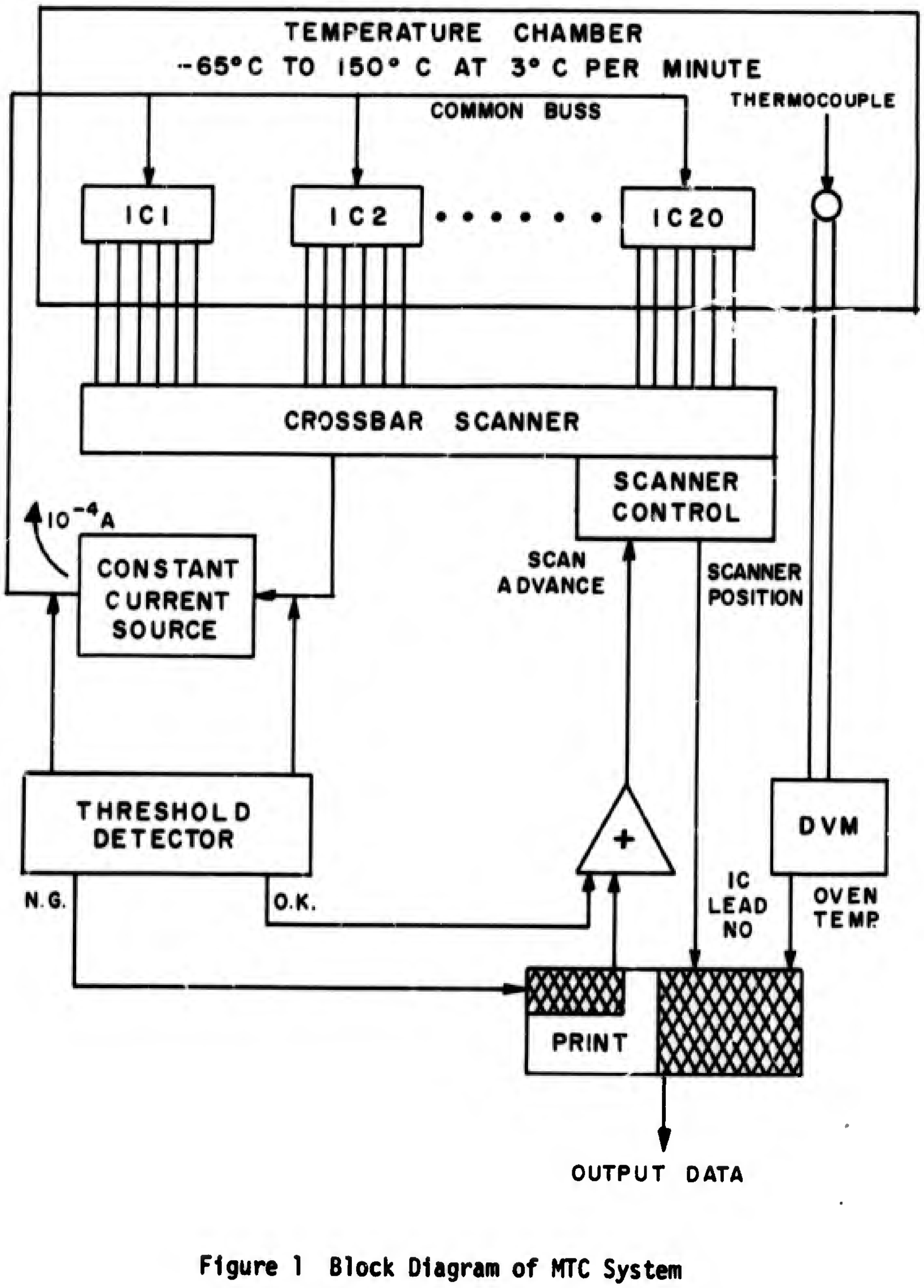


Figure 1 Block Diagram of MTC System

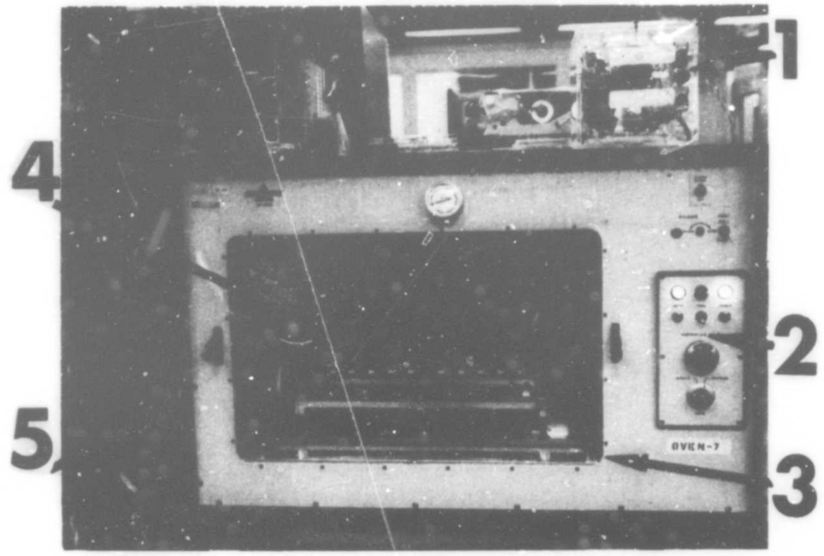
integrated circuit evaluations. The two main sections of the system are the temperature chamber with its associated control circuitry, and the instrumentation used to monitor the integrated circuits being cycled.

## 2.1 OVEN TEMPERATURE CYCLING

The chamber used for the temperature cycling must be capable of going to both the high and low temperature extremes of the test, and the temperature must be capable of being programmed to a specific rate of change. The chamber presently being used by RADC uses a combination of liquid nitrogen cooling and electric heating to cover the temperature range from -65°C to +150°C. A photograph of this section of the system (Figure 2) clearly indicates the specific items used. The chamber temperature controller is programmed externally through the use of a variable resistance. By using a potentiometer and changing its resistance with a reversing motor and the proper gear drive, the temperature in the chamber (at the integrated circuits) is made to cycle from room temperature to -65°C to +150°C, then back to room temperature again, at a rate of about 2°C per minute, as shown in Figure 3.

The most important point about the rate of change of temperature is that it should be slow enough to minimize thermal shock damage to the integrated circuit and also allow the monitoring equipment to check the circuit performance at reasonably small temperature increments of no more than 5°C.

Since the sensor for the chamber temperature controller is not located at the integrated circuits, the temperature at the circuit lags the chamber temperature as determined by the changing resistance of the programming potentiometer. The temperature at the integrated circuits is monitored by a separate thermocouple placed in direct contact with one of the devices to



1. Temperature Programming Unit.
2. Manual Controls
3. Temperature Chamber itself with door removed.
4. Integrated Circuit Sockets - Note Plug-in-jumper for common line.
5. Plug connecting sockets to crossbar scanner.

Figure 2. Temperature Cycling Chamber

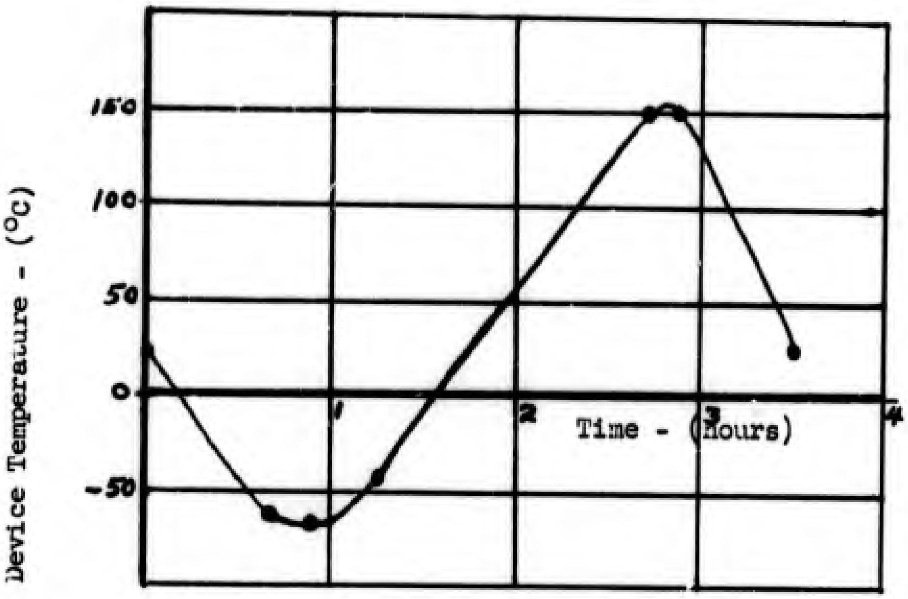


Figure 3. Typical Temperature Cycle

allow determination of the exact integrated circuit package temperature. This enables the temperature cycling range limits to be set at the desired extremes of -65°C and +150°C circuit temperature. This same thermocouple is used during the temperature cycling to obtain an accurate indication of the package temperature, which is included in the data when a failed pin is detected.

## 2.2 DEVICE MONITORING EQUIPMENT

Several alternate methods of monitoring a device may be used for the MTC test. Various device parameters may be used, as well as an operational test of the integrated circuit. The method used presently by RADC was chosen because of its relative simplicity, versatility, and its ability to yield much useful information with a minimum of equipment and instrumentation problems.

The technique used is based on the assumption that the majority of presently unscreenable temperature intermittents are due to opens in the conductor system leading from the external package to the chip circuit connections. Basically, the technique consists of forcing a low level current into each circuit pin, in sequence, with respect to the substrate connection and monitoring the voltage developed across the device. A threshold which has been set to a predetermined value, depending on the type of device, is then checked. If a voltage exceeding this threshold is observed, an open is detected and its location and temperature of occurrence are printed out.

There are several advantages in using this threshold type of measurement which led to its selection over various other techniques. First, it is possible to test almost any type of integrated circuit with only a simple change of threshold and common substrate connection. Also, several types of circuits may be tested simultaneously. The high cost and complex wiring required for parameter type measurements are eliminated, thus making this technique more attractive economically. Another advantage is that it is possible to cycle to temperatures higher than those permitted by the integrated circuit chip operational limitations. Use of only a single current limited source prevents any device damage at temperatures exceeding use temperature. This allows a check of the integrated circuit conductor system over an extended temperature range, thus increasing the probability of detecting a potential operating temperature failure.

The instrumentation used for the device monitoring, shown in block diagram form in Figure 1, consists of all of the items shown except the temperature chamber. All of the circuits to be tested are inserted in sockets in the temperature chamber, with each lead wired to the input of a crossbar scanner which connects to each lead sequentially. Depending upon the type of circuit in each socket, a common buss in the oven is connected to the common or substrate pin of each integrated circuit, using a simple plug-in jumper wire.

The constant current source supplies a set level of current (usually $10^{-4}$ ampere, with a voltage limit set at the lowest feasible level consistent with the characteristics of the device being tested). The current is fed into the common pin, through the integrated circuit and then returned through the pin selected by the crossbar scanner. The voltage developed across the integrated circuit is monitored with a threshold detector. If the voltage exceeds a preset value, the particular integrated circuit pin being checked is considered a failure, and its location and the oven temperature at time of failure are punched out on a high-speed punch for computer analysis. The scanner is then allowed to advance and check the next pin. If the voltage developed across the integrated circuit is below the present threshold, the pin is considered good. In this case no data are punched out, and the scanner is allowed to advance and check the next pin.

The sequence of operations required to accomplish the scanning and testing of the integrated circuits is shown in Figure 4. The current source is always disabled during scanner advance so that each pin, when it is contacted, is connected with zero volts to eliminate any possibility of integrated circuit damage which could occur from the higher voltage levels developed as the current source is opened during transfer of crossbar scanner contacts. The current and voltage are then allowed to build up from zero before the threshold measurement is taken at each pin.

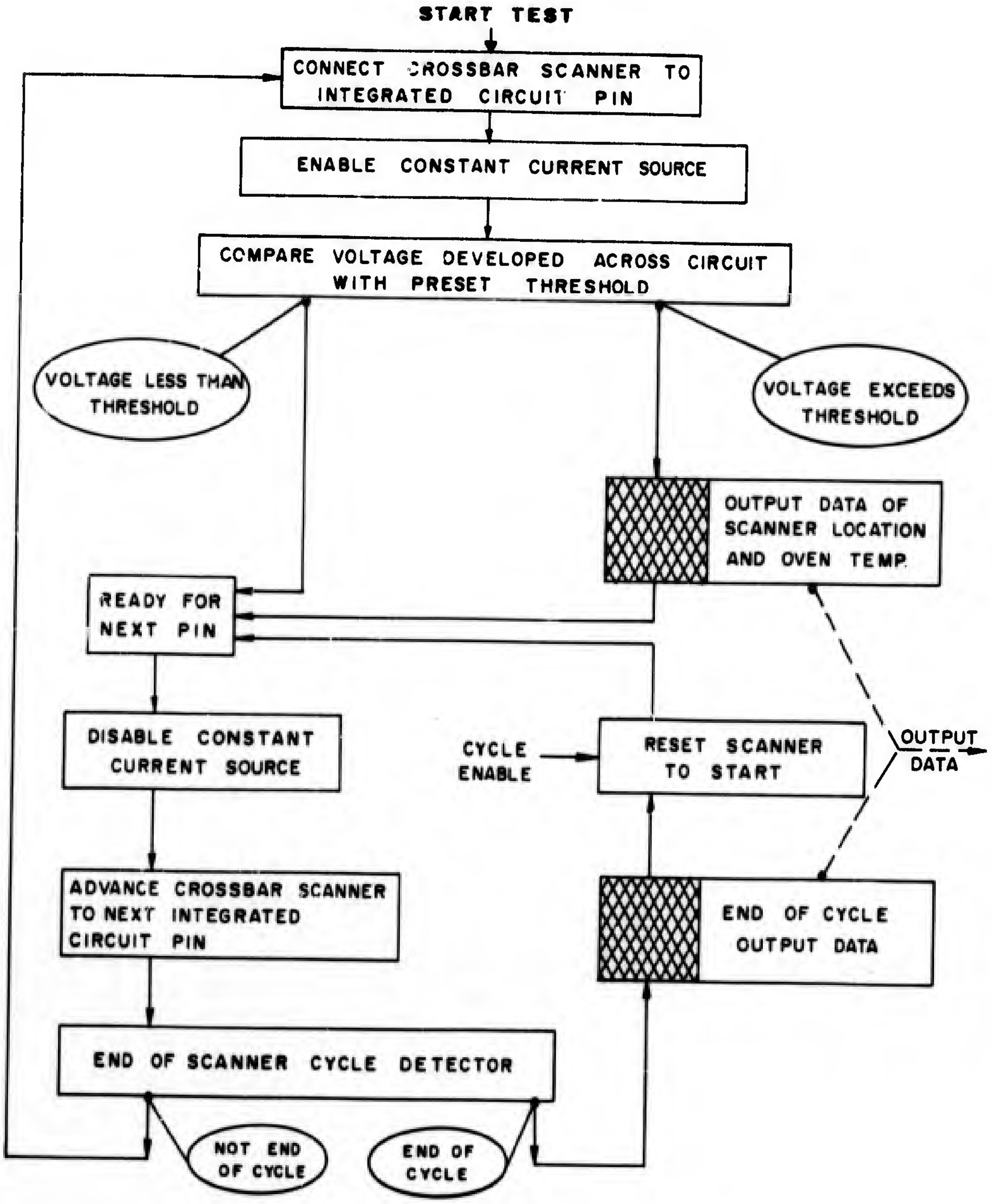
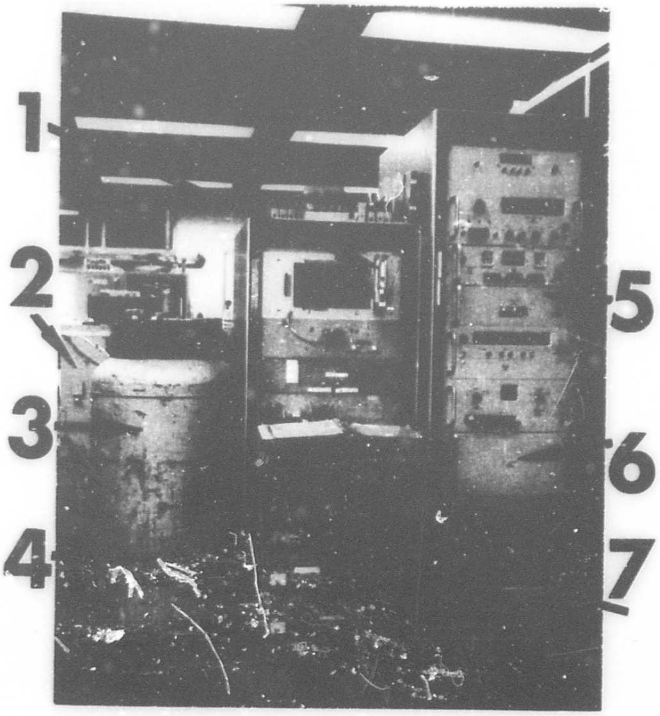


Figure 4. Sequence of Operations for MTC Threshold Measurements

A code is punched out at the end of each complete scanner cycle to enable the computer to recognize the interval of each cycle during its analysis of the data. The circuits are continuously scanned and monitored in this manner as the temperature chamber cycles from room temperature to -65°C, then up to +150°C and back to room temperature again. The removal of the cycle-enable command signifies completion of the test, and the scanner stepping is allowed to halt at the end of the cycle in progress. Figure 5 is a photograph of the complete system presently being used at RADC with the various sections labeled as shown.

## 2.3 COMPUTER DATA ANALYSIS

The output data of the MTC test consist of a long string of numbers representing failed integrated circuit pins and the temperature of failure with numbers to indicate the end of each scanner cycle. To interpret this list of numbers by hand, as on the initial MTC runs, turned out to be a formidable task, especially when several failed pins were detected. To ease the task of data analysis, a computer program was written for use on a time-shared system with remote teletype terminal. This program listing is given and explained in Appendix A. The results of a sample run using this program are shown in Figure 6. This example also serves to illustrate several different types of previously observed, intermittent failures. It is easy to see from these examples why some intermittents are difficult to detect with ordinary room temperature measurements, or even temperature extreme parameter measurements.

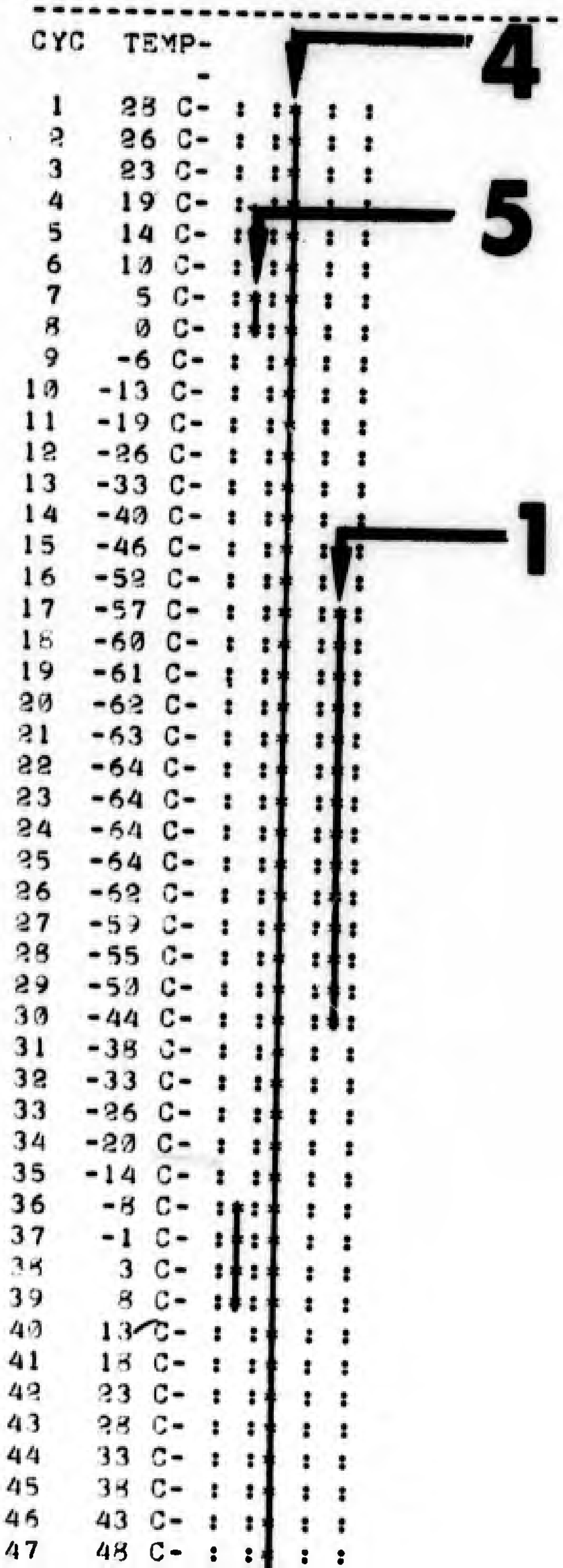


1. Current Source - Voltage Comparator - Control Program - and Thermocouple Input.
2. Back of Temperature Cycling Chamber.
3. Liquid Nitrogen for Temperature Cycling Chamber.
4. DC Power Supplies for Control Circuits.
5. Data Acquisition and Scanner Control.
6. Crossbar Scanner.
7. Output Data - Paper Tape Punch

Figure 5. Labeled System Photograph/Temperature Chamber

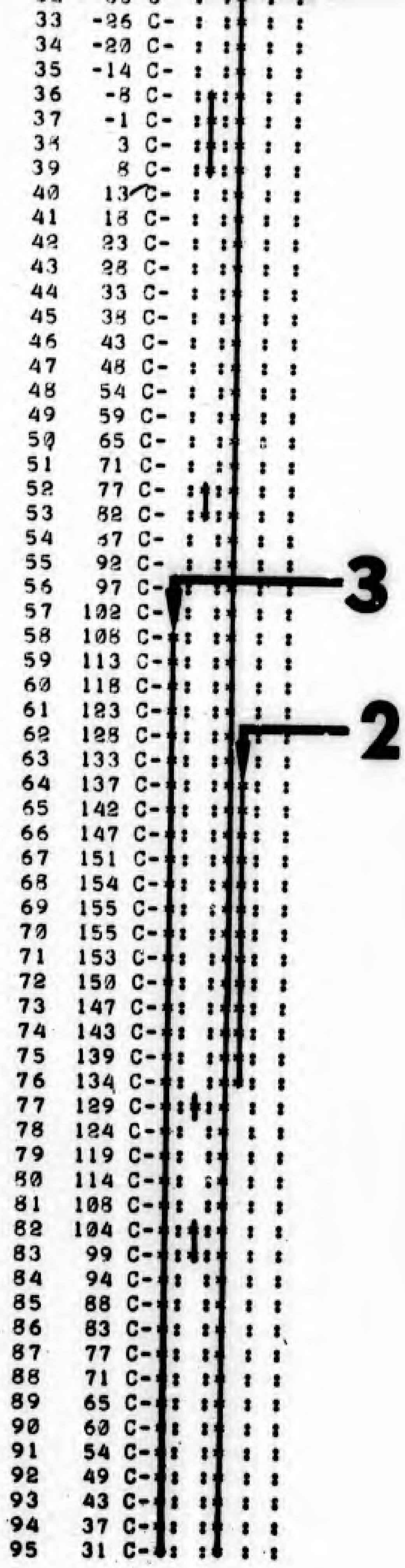
A

```
READY
$FORT A


MONITORED THERMAL CYCLE RUN OF 06/17/70 16.035
                               ---------------

 ANY BAD SCANNER POINTS TO BE DELETED FROM OUTPUT TABLE
 TYPE 999 IF NONE OR NO MORE=999

 # OF CYCLES=          95
 # OF FAILED PINS=            5
 # OF TERMS NOT IN SCAN RANGE=          0

IC         -0:0:11:1:
NUMBER     -3:7:66:9:
           - : :  : :
           - : :  : :
PIN        -1:0:01:1:
NUMBER     -1:3:40:1:
```



```
-----------------------------------------------------------------------------
CYC    TEMP-
           -
  1    28 C- : :* : :
  2    26 C- : :* : :
  3    23 C- : :* : :
  4    19 C- : :* : :
  5    14 C- :*:* : :
  6    10 C- :*:* : :
  7     5 C- :*:* : :
  8     0 C- :*:* : :
  9    -6 C- : :* : :
 10   -13 C- : :* : :
 11   -19 C- : :* : :
 12   -26 C- : :* : :
 13   -33 C- : :* : :
 14   -40 C- : :* : :
 15   -46 C- : :* : :
 16   -52 C- : :* : :
 17   -57 C- : :* :*:
 18   -60 C- : :* :*:
 19   -61 C- : :* :*:
 20   -62 C- : :* :*:
 21   -63 C- : :* :*:
 22   -64 C- : :* :*:
 23   -64 C- : :* :*:
 24   -64 C- : :* :*:
 25   -64 C- : :* :*:
 26   -62 C- : :* :*:
 27   -59 C- : :* :*:
 28   -55 C- : :* :*:
 29   -50 C- : :* :*:
 30   -44 C- : :* :*:
 31   -38 C- : :* : :
 32   -33 C- : :* : :
 33   -26 C- : :* : :
 34   -20 C- : :* : :
 35   -14 C- : :* : :
 36    -8 C- :*:* : :
 37    -1 C- :*:* : :
 38     3 C- :*:* : :
 39     8 C- :*:* : :
 40    13 C- : :* : :
 41    18 C- : :* : :
 42    23 C- : :* : :
 43    28 C- : :* : :
 44    33 C- : :* : :
 45    38 C- : :* : :
 46    43 C- : :* : :
 47    48 C- : :* : :
```

B



```
 33   -26 C-
 34   -20 C-
 35   -14 C-
 36    -8 C-
 37    -1 C-
 38     3 C-
 39     8 C-
 40    13 C-
 41    18 C-
 42    23 C-
 43    28 C-
 44    33 C-
 45    38 C-
 46    43 C-
 47    48 C-
 48    54 C-
 49    59 C-
 50    65 C-
 51    71 C-
 52    77 C-
 53    82 C-
 54    87 C-
 55    92 C-
 56    97 C-
 57   102 C-
 58   108 C-
 59   113 C-
 60   118 C-
 61   123 C-
 62   128 C-
 63   133 C-
 64   137 C-
 65   142 C-
 66   147 C-
 67   151 C-
 68   154 C-
 69   155 C-
 70   155 C-
 71   153 C-
 72   150 C-
 73   147 C-
 74   143 C-
 75   139 C-
 76   134 C-
 77   129 C-
 78   124 C-
 79   119 C-
 80   114 C-
 81   108 C-
 82   104 C-
 83    99 C-
 84    94 C-
 85    88 C-
 86    83 C-
 87    77 C-
 88    71 C-
 89    65 C-
 90    60 C-
 91    54 C-
 92    49 C-
 93    43 C-
 94    37 C-
 95    31 C-

PROGRAM STOP AT 1990

READY
```

COMPUTER PRINT-OUT OF SAMPLE MTC RUN

Figure 6

The computer output may be interpreted as follows: first, the computer asks for any pins which are not to be printed in output table. These pins include known bad pins (such as broken pins), or bad socket contacts, or crossbar scanner contact closure problems which are not desired in the output table. Next, the computer prints a tabulation of the MTC test characteristics: first, the total number of scanner cycles which have been done during the single MTC temperature cycle; and next, the total number of failed pins encountered during the test, counting the occurrence of each pin once and only once. The third printed total applies specifically to the system wiring which utilizes only a portion of crossbar scanner contacts and allows an indication if any of these points should show up erroneously in the raw data.

The plot of the MTC output data is printed next. The heading across the top is of all the failed integrated circuits, and specific pin numbers read vertically with each separate integrated circuit separated by double dots. The heading down the left side of the plot represents the scanner cycle during which a failure is detected. The corresponding chamber temperature (actual device temperature) is also printed for each cycle, and represents the temperature at the end of that cycle in degrees centigrade. A failure during a cycle is then printed as an asterisk on the horizontal line representing that cycle for each integrated circuit pin which was detected as an open during that cycle. A continuous vertical line of asterisks represents a temperature range during which the pin listed at the top of that column was found to be open. A red line has been drawn connecting these asterisks to make interpretation of the plot easier.

Several types of failures can be seen on the sample given in Figure 6. Failure #1 (in this case Pin #11 of IC #19) is a pin which is open during only the cold temperature extreme of the MTC test. Failure #2 is a pin which is open only in the maximum temperature extreme. Failure #3 is a pin which opened at the maximum temperature extreme and stayed open during the remainder of the test back to room temperature. All of these types of observed failures would not have been detected by room temperature measurements. If these devices are of the 0-85°C operating temperature range class, they would not even have been detected by operating temperature extreme measurements, and these potential failures would get into equipment. Failure #3 could have caused equipment malfunction if it had seen even a short interval of 150°C storage, or perhaps some thermal cycling at lower levels.

Failure #4 represents still another type of failure; however, we are not concerned with this type since it is a failure at room temperature and is easily detected with any electrical test at room temperature. This pin was open at room temperature, and remained open during the entire duration of the MTC test. Still another type of thermal problem has been observed where a device fails for a short range of temperature between the ambient and the extremes of the MTC test, but is good both at room temperature and also at the extremes. This type of failure would be similar to Failure #5, where a particular pin shows up at several random points, and is usually due to an intermittent sliding type of contact between a bond and the integrated circuit metallization.

Because of the nature of the test configuration, a minor inconvenience occurs if the common (ground) lead of a device opens. If at any time during the MTC test, the common lead should open, it would be impossible to force the required current into any lead of the integrated circuit, and all pins would appear open. However, the failure would definitely be detected by the MTC test since all integrated circuit pins would print out as failed. Thus, when all pins of a particular integrated circuit print out, it is presumed that the common lead is the cause of failure.

By the preceding examples, it can be seen how the MTC test is able to detect thermal intermittent devices, which are failures at other than room temperature, without the need of extensive parameter measurements. This test is not able to detect thermal intermittent malfunctions of the integrated circuit chip itself. At present, however, the majority of thermal failures, especially in plastic packaged devices, fall into the category easily detected by this MTC technique. This technique also allows electrical checking of the continuity of the metal conductor system of the integrated circuit over the complete storage temperature range of the device (often much greater than the operating range of temperature). Many thermal failures, especially in the encapsulated integrated circuits, have been found at temperatures exceeding the device operational temperature, although within specified package limitations. These devices are very poor reliability risks, since storage or operational temperature cycling could cause eventual failure of the device at its use temperature. Thus, it is very desirable from a reliability standpoint to eliminate these potential failures which would not even be noticeable at normal room or temperature extreme measurements. Also, the randomly intermittent type of failure which only occurs over very narrow temperature ranges, perhaps even within the operating temperature range, is very difficult to detect with any commonly used parameter measurements. This type of failure also poses a very serious reliability threat when it gets into operating equipment.

Almost any of the failures detected by the MTC test could have passed any combination of existing stress tests such as thermal shock, temperature cycling, mechanical shock, etc., when used in conjunction with conventional electrical testing techniques. It is very important, therefore, if the true value of these environmental tests as they influence device reliability evaluation is to be realized, that they be followed by an MTC type of test. This MTC testing, while very useful by itself as an evaluation technique of one aspect of integrated circuit reliability, is even more beneficial if used in connection with the various stress test/parameter measurement techniques presently in use.

## 3.0 RESULTS OF THE MONITORED THERMAL CYCLE PROGRAM

The monitored thermal cycle technique for the evaluation of thermal intermittent problems connected with integrated circuits has resulted in some very interesting data. Since this technique was implemented as part of a plastic encapsulated integrated circuit reliability program, some improvement has been seen in the ability of the various encapsulated devices to pass this test. The MTC test has been used by itself and as a monitoring technique for other stress tests such as thermal shock. Devices passing standard electrical parameter measurement, after various stress tests, have quite often exhibited opens on the MTC test.

Test results have also indicated that some lots and date codes of a manufacturer are better than other lots and date codes of an identical device, thus indicating poor quality control or possibly a process change. Besides the control of the encapsulation process which could cause differences such as these, some evidence is present that lot wire bonding variability has been a significant factor influencing the relative difference in thermal intermittency failures seen in various lots. The transfer molding process commonly used for encapsulating these devices puts a stress on the bond wires and the bond itself, thus requiring even better consistency in bonds than is required in conventional devices. Often, this stress is not enough to break the bond, but upon thermal cycling or shock, a weak bond can easily pull loose and become intermittent.

Large differences have also been seen on devices made by different manufacturers using different molding compounds and processes. Detailed information on these variables at any particular time is not easy to obtain, making any reliability correlation to the specific technique used not possible ordinarily.

Some general types of encapsulated devices have been shown significantly more reliable than others under various applied stresses. In some cases, one package may hold up well on one type of environmental test and fail on a second; a different manufacturer's packaged device may behave in just the opposite manner on the two tests.

One problem associated with encapsulated integrated circuits occurs when moisture penetrates the package, usually along the lead frame, and causes corrosion of the metallization which usually starts at the bonding pad[2,3].

This can also cause the bond to break loose and effect intermittent contact resulting in an unreliable device. Use of the monitored thermal cycle test at intervals in moisture resistance stressing (cycled temperature humidity) has detected several failures of this type before they could be located by using the conventional electrical parameter measurements.

The monitored thermal cycle test has also been used in conjunction with thermal shock stress tests. When the MTC test was done at various intervals during thermal shock testing, it was commonly found that the MTC test could locate a failure that would not be detected by room temperature parameter measurements for more than 100 additional cycles of thermal shock.

### 3.1 LISTING OF SOME MTC FAILURES

The evaluation program for plastic encapsulated microcircuits has resulted in many failures on the monitored thermal cycle test. Some of these failures have seen previous stress and others have failed the first MTC with no previous stress history other than shelf storage. Figure 7 is a partial listing of the device failures observed on MTC. Several pertinent items about each device and its history are listed, and only failures not detectable using the routine room temperature parameter measurements are included.

Depending on the previous history, several predominant modes of failures are commonly observed. MTC failures occurring on a device with no previous history are usually opens between the bond and bonding pad because of a poor initial bond. Devices which have seen previous thermal shock stressing usually break at the necked down region of the bond or at some spot along the length of the wire where damage or usually high stresses may have occurred.

| MANUFACTURER | SERIAL #<br>DATE CODE | PREVIOUS STRESS | DIP PACKAGE TYPE | MTC FAILURE INDICATION |
|---|---|---|---|---|
| P1 | 36/823 | 200 cyc T.S.<br>520 cyc T.S.* | Phenolic | pin 11: +98° → EOT |
| P1 | 40/823 | 200 cyc T.S.<br>520 cyc T.S.* | Phenolic | all: +8 → -65 → +8 |
| P3 | 33/6810A | 200 cyc T.S.<br>520 cyc T.S.* | Epoxy | pin 10: +101 → EOT |
| P2 | 37/833 | 44 cyc T.S. | Silicone | pin 6: +137 → +103 |
| P2 | 1180/833 | 20 cyc T.S. | Silicone | all: +20 → -62 → +20 |
| P4 | 30/6847 | 285 cyc T.S. | Silicone | pin 12: +36 → +71 |
| P4 | 38/6847 | 285 cyc T.S. | Silicone | pin 8: +142 → EOT |
| P4 | 41/6847 | 285 cyc T.S. | Silicone | pin 9: +14 → EOT<br>pin 8: +117 → EOT |
| P1 | 11/812 | 20 P.C. | Phenolic | pin 2: +64 → +80 |
| P2 | 192/833 | 20 cyc T.S. | Silicone | pin 6: +98 → EOT |
| P1 | 40X/840 | 2700 hrs CTH | Phenolic | pin 8: +137 → EOT |
| P2 | 12X/809 | 2700 hrs CTH | Silicone | pin 3: +80 → EOT |
| P5 | 1-5/6923 | new ckt | Silicone w/bubble | pin 3: random opens |
| P5 | 1-5/6923 | new ckt | " | pin 11: +129 → +140 → +120 |
| P5 | A-14/6923 | 75 cyc T.S. | " | pin 9: +47 → +150 → +47 |
| P5 | C-20/6923 | 45 cyc T.S. | " | pin 9: random opens |
| P5 | A-12/6923 | 135 cyc T.S. | " | pin 12: random opens |

T.S. = Thermal shock -65 to +150
T.S.* = Thermal shock -65 to +100
CTH = Cycled Temperature Humidity
P.C. = Power Cycling
EOT = End of Test

Figure 7. Monitored Thermal Cycle Failures

If a device fails after a history of moisture resistance stress tests, the failure mode is usually corrosion of the metallization at the gold aluminum bond region, resulting in an open. A stress history of high temperature, steady-state power dissipation usually results in MTC failures attributed to bond degradation. In most of these situations, the monitored thermal cycle test can detect a failure before normal parameter measurements will indicate that any of the mentioned problems are present.

## 3.2 FAILURE ANALYSIS OF SOME TYPICAL MTC FAILURES

Most of the failures on the MTC test have been analyzed to obtain the exact mechanism of the failure where possible. Usually, electrical and curve tracer measurements were performed to verify the failure, then the device was depotted using any one of several techniques, depending on the type of encapsulating material. Extreme care was always taken to prevent any disturbance of the leads so that a valid observation of the exact condition of the bonds and metallization could be obtained.

The best decapsulation results were obtained on devices with a resilient bubble surrounding the chip. These devices were ground on a belt sander until the bubble just started to show, then the bubble was dissolved using either J-300 or Uresolve Plus to expose the chip and lead wires surrounding it. After analysis of the chip, if the cause of failure is not found, complete decapsulation must be done to expose the lead frame and its associated bonds. The following examples are the results of failure analysis on several devices listed in the table given in Figure 7:

## Failure Analysis No. 1

Device Type - 709 - Operational Amplifier
Manufacturer - P5
Package Type - DIP
Lead Wire - Au
Circuit Metallization - Al
Previous History - New Device - 8 Months Shelf Storage

This device failed on monitored thermal cycle run after initial electrical operational test. The circuit exhibited random intermittent opens on pin #3 over the elevated temperature range of the MTC test. After the MTC test, the device was again subjected to an operational transfer test and was found to be unstable. A curve tracer verification of pin #3 to substrate exhibited a very high resistance which jumped randomly to various slopes instead of the normal junction characteristic. This pin, which is used for the input compensation, could explain the oscillation observed on electrical testing.

The device was then carefully depotted, using the procedure outlined earlier. Careful visual inspection of this device revealed no immediately obvious problems, except possibly a scratch in the aluminum metallization. Micromanipulators were used to verify electrically the continuity between the bonding pad and the other side of the scratch. Continuity was also verified from the external IC pin and the ball of the ball bond. However, an open was seen between the external IC pin and the aluminum bonding pad.

The bond was carefully pushed aside and the condition of the aluminum bonding pad was as shown in Figure 8 at pin #3. It can be seen that this was a very poor bond initially, resulting in the intermittent characteristic seen as the device was cycled thermally. A bond puller was then used to test the bond strengths of the remaining bonds on this circuit, and those of a similar device in the same group which also failed. Several of the bonds pulled at less than one gram and exhibited the poor alloying characteristic shown previously. The adjacent bond at pin #4 in Figure 8 was also a poor bond. Most of the good bonds on the same device exhibited pull strengths in excess of four grams and usually resulted in a wire break rather than a bond pulling off the bonding pad. The bonds that did pull from the pad at the higher pull strength all exhibited normal uniform alloying characteristics.

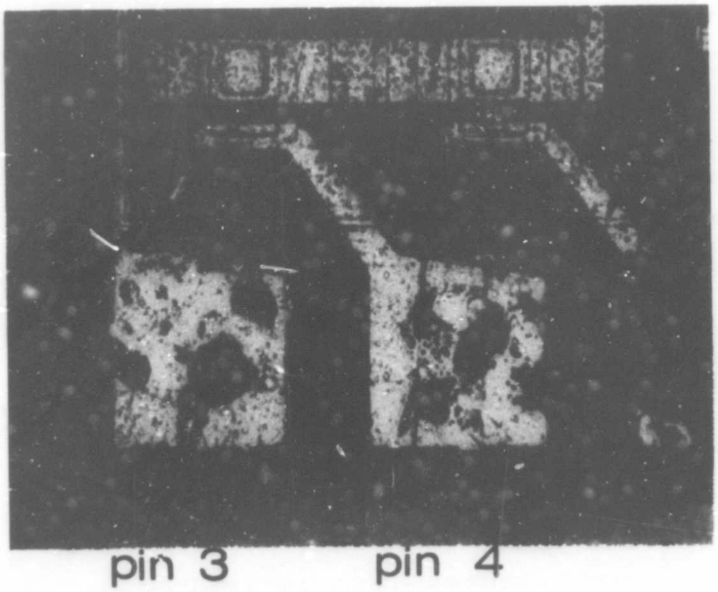


Figure 8. Failure Analysis #1 - Open Due to Bad Bond

## Failure Analysis #2

Device Type - DTL Gate
Manufacturer - P1
Package Type - DIP
Lead Wire - Gold
Circuit Metallization - Aluminum
Previous History - 2700 Hours Cycled Temperature/Humidity

This device had undergone 2700 hours of cycled temperature, humidity, and moisture resistance stress testing (MIL-STD-883, Method 1004) before the MTC technique was implemented. The device was run through the monitored thermal cycle test during one of the standard electrical test intervals, and pin #8 was found to be open from +137°C of the up temperature cycle to +150°C and back to room temperature again. At the conclusion of the MTC test, the lead was verified open by a curve tracer measurement at room temperature. Decapsulation of the circuit revealed that the cause of the problem was corrosion at the bonding pad of pin #8, as shown in Figure 9, which resulted in the eventual open. It should be noted that it was not necessary to remove the resilient chip coating from this device since it was a clear compound. By grinding the package to this transparent bubble and putting a drop of water and a cover glass over the bubble, it was possible to see the chip clearly without having to risk chip damage by removing the bubble.

The 2700 hours of moisture resistance had caused considerable corrosion of this pin, but had not produced a failure at room temperature on the +65° high temperature extreme of the temperature/humidity stress test. When the device was subjected to the MTC test, it failed open at +137°C (well above the

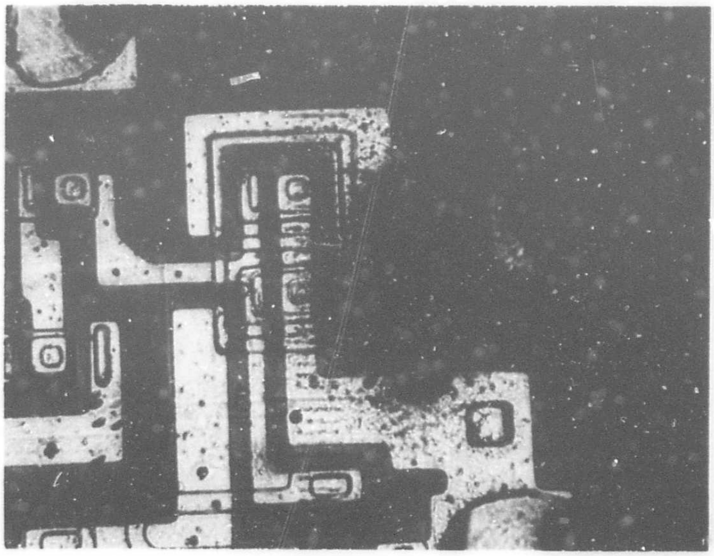


Figure 9. Failure Analysis #2
Open at Bond Due to Corrosion

stress temperature, but easily within the storage temperature rating of the device), and did not return to normal, even at room temperature. The MTC test had provided an elevated temperature within device ratings which caused the failure to make itself known by accelerating the already existing corrosion to such an extent that it open circuited at the recorded temperature. It is likely that this device would have failed completely after more time on the cycled temperature/humidity test after the corrosion had continued under those conditions. The MTC test made it possible to detect this potential failure before continued corrosion completely destroyed the conduction path. It would have been extremely valuable if no further stress testing were planned.

## Failure Analysis #3

Device Type - DTL Dual 4-input NAND Gate
Manufacturer - P2
Package Type - DIP
Lead Wire - Gold
Circuit Metallization - Aluminum
Previous History - 2700 Hours Cycled Temperature/Humidity

This failure is similar to failure #2 and occurred under exactly the same conditions. The device failed the MTC test after 2700 hours of temperature/humidity cycling. On this device, pin #3 failed open on the up cycle in temperature at +84°C, and remained open to +150°C and back to room temperature again. After electrical verification, the device was depotted (on this device, completely to the chip) and the result of corrosion is seen on the pin #3 bonding pad after the lead had been moved aside (see Figure 10). Again, the device had not failed at the +65°C upper limit of the temperature/humidity test, but the higher temperature of the MTC test caused eventual and permanent failure of this already weak bond. Both of these failures (#2 and #3) show the effect of moisture when it penetrates the plastic package, usually along the lead frame and lead wire to the chip.

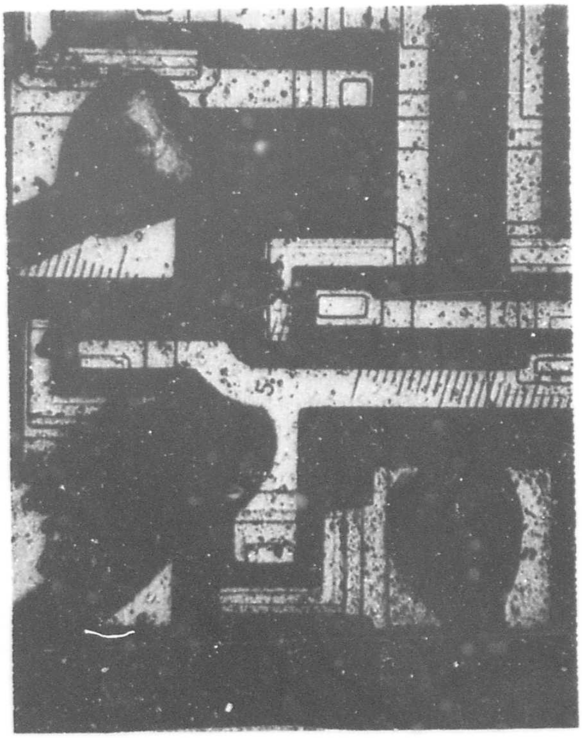


Figure 10. Failure Analysis #3 - Open at Bond Due to Corrosion

## Failure Analysis #4

Device Type - 709 Operational Amplifier
Manufacturer - P5
Package Type - DIP Silicone
Lead Wire - Gold
Circuit Metallization - Aluminum
Previous History - 135 Cycles Thermal Shock -65 to +150°C

This device had undergone 135 cycles of the thermal shock, as per MIL-STD-883, Method 1011, Test Condition C. The device failed on MTC with pin #10 open at the high temperature extreme. The device was depotted and the bubble removed. Figure 11 shows the result of this failure analysis as an open at the necked down region above the ball bond. This represents still another common type of failure.

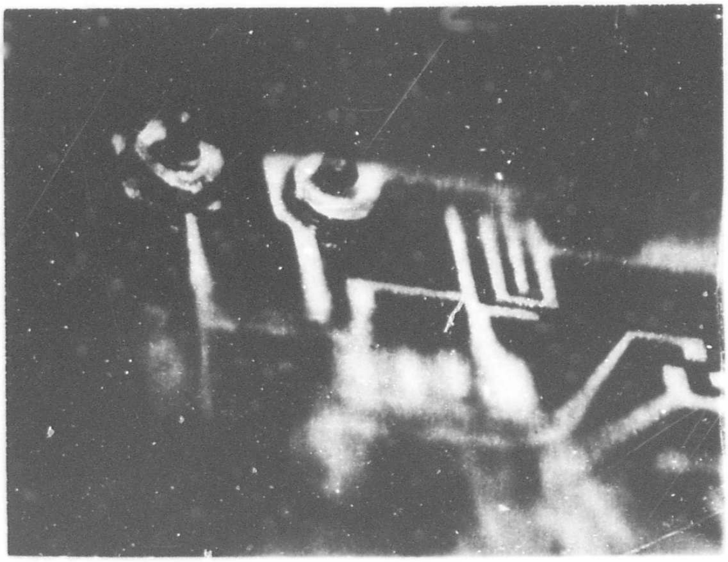


Figure 11. Failure Analysis #4
Open at Necked Region Due to Thermal Shock Stress

## Failure Analysis #5

Device Type - 709 Operational Amplifier

Manufacturer - P5

Package Type - DIP Silicone

Lead Wire - Gold

Circuit Metallization - Alumimum

Previous History - 210 Cycles Thermal Shock -65 to +150°C

This device had undergone 210 cycles of thermal shock as per MIL-STD-883, Method 1011, Test Condition C. The device failed with pin #9 open in the bond wire passing through the bulk of the resilient potting bubble (see Figure 12). Note that there is no slack in this particular lead.

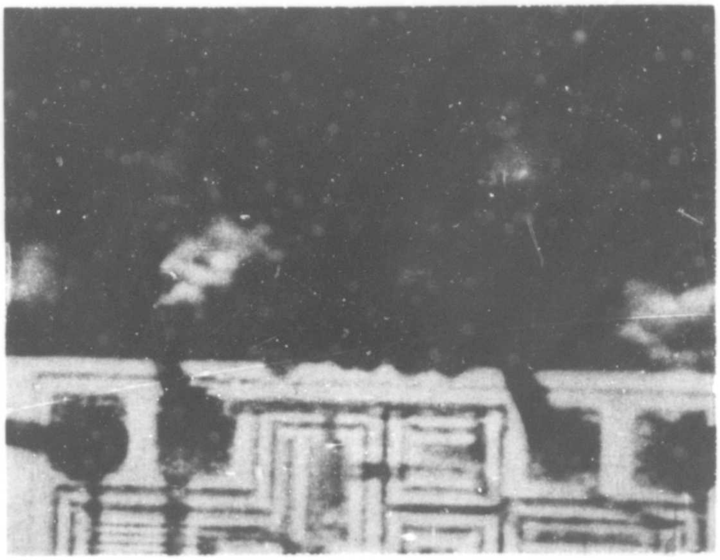


Figure 12. Failure Analysis #5
Wire Break in Encapsulating Material

## Failure Analysis #6

Device Type - 709 Operational Amplifier

Manufacturer - P5

Package Type - DIP Silicone

Lead Wire - - Gold

Circuit Metallization - Aluminum

Previous History - 135 Cycles Thermal Shock -65 to +150°C

This device had undergone 135 cycles of thermal shock as per MIL-STD-883, Method 1011, Test Condition C. The device failed with pin #12 intermittent over the temperature range of the MTC test. Depotting to the bubble and probing revealed no opens at the chip. The device was then depotted to expose the lead frame where the open at pin #12 was found to be an open at the lead frame bond (see Figure 13). Close inspection of this bond indicated that the failure was probably the result of an over-bonded condition existing at the bond.

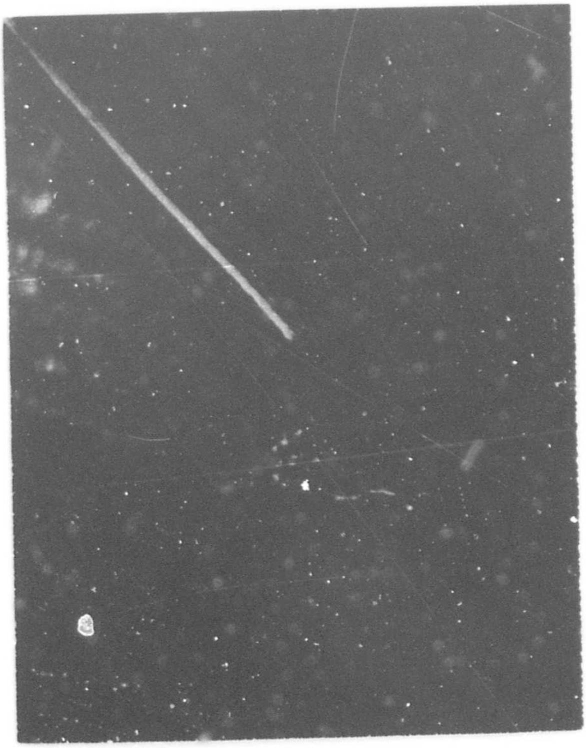


Figure 13. Failure Analysis #6 - Open At Lead Frame Bond

## 4.0 CONCLUSIONS AND FUTURE WORK

The Monitored Thermal Cycle technique has proved to be very valuable for detecting thermal intermittent failures in integrated circuits. By itself, as an evaluation test to assess the relative susceptibility to thermal intermittents of encapsulated integrated circuits, or in conjunction with more conventional stress and environmental tests, the technique allows identification of otherwise undetectable weak devices. Because of the large variability from one package type to another, and even from one lot to another of the same device and package type, this technique, when used as a qualification test, can provide very useful information to aid in obtaining the reliable devices. The present implementation of the MTC test utilizes only a single upper threshold. An extension of the technique to provide a variable upper and lower threshold limit, which would be automatically selected depending on the IC pin being checked, could yield even more sensitivity to device changes and is being considered. Also, a broad program has been initiated for the evaluation of encapsulated linear integrated circuits, which will make extensive use of the MTC test and should provide more data as to the effectiveness of this technique.

## APPENDIX A

## COMPUTER ANALYSIS OF MTC DATA

This section describes the detailed implementation of a computer program for analysis of the data obtained during Monitored Thermal Cycle testing. The program is written in Fortran and has been designed to be run on a GE 645 Time Sharing system. There are two main sections which will be covered separately: first, the format and entry of data; second, the actual computer program.

### 1. DATA FORMAT AND ENTRY INTO COMPUTER

The data obtained, representing the results of the monitored thermal cycle testing, contain information indicating the temperature at which a specified integrated pin is a failure. The technique used to detect open pins is described in Section 2 of this report. As the devices cycle over the complete temperature range during a period of about 3.5 hours, each pin is checked for continuity at about 5°C intervals. When an open is detected, the data acquisition equipment punches on a paper tape, the scanner position (representing the IC and pin number) at which the open has been detected, and the temperature (millivolts thermocouple output), followed by the line-ending characters of carriage return, line feed, rub-out, rub-out.

Sample data to illustrate the format used is shown in Figure A1. The first three characters on each line represent the scanner position at which a failure is detected. This corresponds to the IC and pin number of a detected failure. The space is then followed by four digits which represent the temperature of failure as the thermocouple output in millivolts followed by a fifth digit which represents the thermocouple polarity, with one as positive and two as negative. The nonprinting line-ending characters mentioned before

```
1\ $RELEASE MTCDATA
2\
   READY
3- $ENTER MTCDATA

4\ READY
5- 599 00101
   315 00051
   599 00052
   315 00082
   599 00142
   315 00172
   599 00272
   315 00332
   599 00452
   315 00512
   599 00652
   315 00712
   599 00852
   206 00862
   315 00912
   599 01072
   206 01082
   315 01132
   599 01282
         |
         |
         |
         |
         |
         |
         |
         |
         |
         |
         |
         |
         |
   599 01041
   315 00981
   432 00901
   599 00811
   315 00751
   432 00681
   599 00581
   315 00511
   432 00431
   599 00321
   315 00251
   432 00181
6\ 599 00081
   600 11111
7/ $SAVE MTCDATA,(NOSORT)
```

SAMPLE OF DATA INPUT

Figure A1

complete each line. After the continuity of each integrated circuit pin has been checked once (about 5°C temperature change), a code is punched out to indicate the end of a complete scanner cycle. This code is 599 with the corresponding chamber (integrated circuit) temperature.

After the temperature cycling has been completed (about 3.5 hours), the data tape is then fed into the time-shared computer data file via a standard teletype terminal.

Referring to Figure A1, the sequence of operations for data entry after connection has been made to the computer is as follows: the solid underlined lines represent manually entered user responses; the dashed lines represent computer replies; the remainder of the material is entry from the perforated data tape. First, the old data file (MTC DATA) is removed (Step #1) and the computer replies ready (Step #2). Then the tape reader is prepared for entry (Step #3) and the computer replies ready (Step #4). The paper tape is then started (Step #5). When the tape is completely read, a line is manually entered so that the analysis program can easily recognize the end of the data (Step #6); then the file is saved (Step #7).

Only a small number of scanner cycles are shown (indicated by consecutive 599's). Typically, there would be about 100 scanner cycles required for a complete MTC run.

## 2. DATA ANALYSIS PROGRAM

After the data have been entered into a data file and saved as just outlined, the computer program shown in Figure A2 is then called to plot the integrated circuit pin opens as a function of temperature. The results of this program are shown in Figure 6 in the main part of the report.

The program is designed to plot the failed integrated circuit pin numbers as a function of temperature, with the specific crossbar scanner-to-temperature chamber wiring used in obtaining the input data. The crossbar scanner scans 600 points, of which only 280 are wired to sockets. The rest are wired to the temperature chamber common, as only 20 sockets are being used. Any other input scheme would require slight modifications to the program to convert from crossbar scanner number to the representative integrated circuit pin number.

NOT REPRODUCIBLE

```
00010 ASCII Q(2)
00020 FILENAME MTCDATA
00030 COMMON A(200)
00040 COMMON B(1000,2)
00050 DIMENSION C(14),E(14)
00060 COMMON F(50,2)
00070 DIMENSION IBAD(10)
00080 C(1)=20;C(2)=50;C(3)=80;C(4)=120;C(5)=150
00090 C(6)=180;C(7)=220;C(8)=250;C(9)=320;C(10)=350
00100 C(11)=420;C(12)=450;C(13)=520;C(14)=550
00110 E(1)=1;E(2)=7;E(3)=13;E(4)=2;E(5)=8;E(6)=14;E(7)=3
00120 E(8)=9;E(9)=4;E(10)=10;E(11)=5;E(12)=11;E(13)=6;E(14)=12
00130 PRINT: " "
00140 PRINT: " "
00150 PRINT: " "
00160 CALL DATE*TIM(Q,Z)
00170 PRINT 2,Q,Z
00180 2 FORMAT (" MONITORED THERMAL CYCLE RUN OF",1H ,2A4,F7.3," ")
00190 PRINT: "                                       ----------------"
00200 PRINT: " "
00210 PRINT: " "
00220 PRINT:" ANY BAD SCANNER POINTS TO BE DELETED FROM OUTPUT TABLE"
00230 PRINT:" TYPE 999 IF NONE OR NO MORE"
00240 DO 12 IB=1,10
00250 READ 14,IBAD(IB)
00260 14 FORMAT (I3)
00270 IF (IBAD(IB)-999)12,13,12
00280 12 CONTINUE
00290 13 IB=IB-1
00300 K=0
00310 MISC=0
00320 LIM=0
00330 MA=0
00340 DO 39 I=1,2000
00350 READ ("MTCDATA",20)MSCAN,MDATA,MPOL
00360 20 FORMAT (I3,I5,I1)
00370 DO 21 ID=1,IB
00380 IF (MSCAN-IBAD(ID))21,39,21
00390 21 CONTINUE
00400 IF (MPOL-2)22,23,24
00410 22 IF(MDATA-210)16,17,17
00420 16 MTEMP=30+(MDATA)*(50./210.)
00430 GO TO 15
00440 17 MTEMP=80+(MDATA-210)*(80./390.)
00450 GO TO 15
00460 23 IF (MDATA-130)18,18,19
00470 18 MTEMP=(130-MDATA)*(30./130.)
00480 GO TO 15
00490 19 MTEMP=-80+(400-MDATA)*(80./270.)
00500 GO TO 15
```

NOT REPRODUCIBLE

```
00510 24 PRINT: " DATA ERROR--DVM FUNCTION NOT + OR -"
00520 MTEMP =999
00530 GO TO 15
00540 15 IF (MSCAN-599)25,38,40
00550 25 DO 26 J=1,25
00560 IF (MSCAN-C(J))27,26,26
00570 26 CONTINUE
00580 27 IF (MSCAN-C(J)+21)29,29,28
00590 29 MISC=MISC+1
00600 GO TO 39
00610 28 K=K+1
00620 B(K,1)=MSCAN-C(J)+21
00630 B(K,2)=E(J)
00640 DO 31 M=1,50
00650 IF (B(K,1)-F(M,1))33,34,33
00660 34 IF (B(K,2)-F(M,2))33,39,33
00670 33 IF (M-MA)31,32,32
00680 31 CONTINUE
00690 32 MA=MA+1
00700 F(MA,1)=B(K,1)
00710 F(MA,2)=B(K,2)
00720 GO TO 39
00730 38 K=K+1
00740 LIM=LIM+1
00750 A(LIM)=K
00760 B(K,1)=599
00770 B(K,2)=MTEMP
00780 39 CONTINUE
00790 40 LIM=LIM-1
00800 MB=1
00810 IF (MA-1.)200,50,41
00820 41 MC=MB+1
00830 DO 49 M=MC,MA
00840 IF (F(MB,1)-F(M,1))49,43,42
00850 43 IF (F(MB,2)-F(M,2))49,44,42
00860 44 PRINT:" THERE IS MORE THAN ONE OF EACH # IN FAILED DEVICE LIST-F"
00870 42 FA=F(MB,1)
00880 FB=F(MB,2)
00890 F(MB,1)=F(M,1)
00900 F(MB,2)=F(M,2)
00910 F(M,1)=FA
00920 F(M,2)=FB
00930 49 CONTINUE
00940 MB=MB+1
00950 IF (MB-MA)41,50,50
00960 50 DO 59 LB=1,LIM
00970 IF (A(LB)-A(LB+1)+2)51,51,59
00980 51 LC=A(LB)+1
00990 LD=A(LB+1)-1
01000 54 LE=LC+1
```

NOT REPRODUCIBLE

```
01010 DO 58 LF=LE,LD
01020 IF (B(LC,1)-B(LF,1))58,55,57
01030 55 IF (B(LC,2)-B(LF,2))58,56,57
01040 56 PRINT:" LIST -B- DATA FAULT--TWO NUMBERS IN A CYCLE ARE IDENTICAL"
01050 57 BA=B(LC,1)
01060 BB=B(LC,2)
01070 B(LC,1)=B(LF,1)
01080 B(LC,2)=B(LF,2)
01090 B(LF,1)=BA
01100 B(LF,2)=BB
01110 58 CONTINUE
01120 LC=LC+1
01130 IF (LC-LD)54,59,59
01140 59 CONTINUE
01150 PRINT: " # OF CYCLES=",LIM
01160 PRINT: " # OF FAILED PINS=",MA
01170 PRINT: " # OF TERMS NOT IN SCAN RANGE=",MISC
01180 PRINT 60
01190 60 FORMAT ("-IC        -")
01200 DO 69 J=1,MA
01210 Y=F(J,1)/10.
01220 PRINT 64,INT(Y)
01230 64 FORMAT ("&",I1)
01240 JA=J+1
01250 IF (F(J,1)-F(JA,1))65,69,65
01260 65 PRINT 66
01270 66 FORMAT ("&:")
01280 69 CONTINUE
01290 PRINT 70
01300 70 FORMAT (" NUMBER    -")
01310 DO 79 J=1,MA
01320 JY=F(J,1)
01330 PRINT 74,JY
01340 74 FORMAT ("&",I1)
01350 JA=J+1
01360 IF (F(J,1)-F(JA,1))75,79,75
01370 75 PRINT 76
01380 76 FORMAT ("&:")
01390 79 CONTINUE
01400 DO 89 JB=1,2
01410 PRINT 80
01420 80 FORMAT ("          .  -")
01430 DO 88 J=1,MA
01440 PRINT 84
01450 84 FORMAT ("& ")
01460 JA=J+1
01470 IF (F(J,1)-F(JA,1))85,88,85
01480 85 PRINT 86
01490 86 FORMAT ("&:")
01500 88 CONTINUE
```

```
01510 89 CONTINUE
01520 PRINT 90
01530 90 FORMAT (" PIN        -")
01540 DO 99 J=1,MA
01550 Y=F(J,2)/10.
01560 PRINT 94,INT(Y)
01570 94 FORMAT ("&",I1)
01580 JA=J+1
01590 IF (F(J,1)-F(JA,1))95,99,95
01600 95 PRINT 96
01610 96 FORMAT ("&:")
01620 99 CONTINUE
01630 PRINT 70
01640 DO 109 J=1,MA
01650 JY=F(J,2)
01660 PRINT 104,JY
01670 104 FORMAT ("&",I1)
01680 JA=J+1
01690 IF (F(J,1)-F(JA,1))105,109,105
01700 105 PRINT 106
01710 106 FORMAT ("&:")
01720 109 CONTINUE
01730 PRINT 110
01740 110 FORMAT (" ------------------------------------------------------")
01750 PRINT 112
01760 112 FORMAT (" CYC  TEMP-")
01770 PRINT 114
01780 114 FORMAT ("            -")
01790 DO 150 L=1,LIM
01800 LA=B(A(L+1),2)
01810 PRINT 116,L,LA
01820 116 FORMAT (1XI2,I5," C-")
01830 LB=A(L)+1
01840 LC=A(L+1)-1
01850 DO 140 LD=1,MA
01860 IF (ABS(F(LD,1)-B(LB,1))+ABS(F(LD,2)-B(LB,2)))141,143,141
01870 141 PRINT 142
01880 142 FORMAT ("& ")
01890 GO TO 148
01900 143 PRINT 149
01910 149 FORMAT ("&*")
01920 LB=LB+1
01930 148 LE=LD+1
01940 IF (F(LD,1)-F(LE,1))144,140,144
01950 144 PRINT 145
01960 145 FORMAT ("&:")
01970 140 CONTINUE
01980 150 CONTINUE
01990 STOP
02000 200 PRINT:" NO FAILURES--NUMBER OF CYCLES -",LIM
02010 END
```

The program consists of several basic sections, as listed in the following description referring to Figure A2.

| | | |
|---|---|---|
| a. | Lines 00010 - 00070 | Initial file designations. |
| b. | Lines 00080 - 00120 | Constants used for conversion from crossbar scanner number to integrated circuit pin number in Section i. |
| c. | Lines 00130 - 00210 | Prints date and time on output table. |
| d. | Lines 00220 - 00280 | Allows entry of known bad scanner prints or broken IC pins to minimize stored data. |
| e. | Lines 00300 - 00330 | Sets initial condition. |
| f. | Lines 00340 - 00360 | Reads in data from data file "MTC DATA." |
| g. | Lines 00370 - 00390 | Checks to see if data number is to be deleted as entered in Section d. |
| h. | Lines 00400 - 00540 | Calculates temperature in °C from thermocouple, using linear approximation for each data line inputed. |
| i. | Lines 00550 - 00600 | Calculates value of j from which each IC number and pin number is obtained using constants in Section b. |
| j. | Lines 00610 - 00630 | Fills list B with failed IC number as B(K,1) and pin number as B(K,2) for each scanner cycle. |
| k. | Lines 00640 - 00720 | Fills list F such that it contains one each of any failed IC pin number which occurs throughout the temperature cycling. |
| l. | Lines 00730 - 00770 | Fills list B with a 599 and the temperature at the end of each scanner cycle. |
| m. | Lines 00780 - 00950 | Orders list F in ascending order of IC number and pin number. |
| n. | Lines 00960 - 01140 | Orders each scanner cycle in list B in ascending order of IC number, then pin number. |
| o. | Lines 01150 - 01170 | Prints tabulation of shown quantities. |

| | |
|---|---|
| p. Lines 01180 - 01780 | Prints heading for output plot allowing a column for all failures encountered during the entire test. |
| q. Lines 01790 - 01820 | Prints each line heading of the scanner cycle and temperature at the end of that cycle. |
| r. Lines 01830 - 01990 | Steps across each line representing a temperature cycle and compares failed list F to the particular cycle in list B to determine if a failure is present during that cycle and prints an asterisk if a failed pin is present or a space if a given pin is good. |
| s. Line 02000 | Prints if no failures are detected in list F. |
| t. Line 02010 | End statement. |

As mentioned before, this program will result in meaningful output only for this one specific data acquisition system. Basically, the only changes which must be made in the program, if it is to be used with another system, would be to modify the conversion from scanner number to integrated circuit pin number and possibly the data read format. The specific data acquisition output format would dictate the exact program requirements, but the basic techniques used to obtain the plot of integrated circuit pin numbers, as a function of temperature, can be utilized as outlined for any similar system.

# APPENDIX B

## PROPOSED TEST METHOD FOR MONITORED THERMAL CYCLE

### 1. PURPOSE

The purpose of this method is to provide for the implementation of the monitored thermal cycle technique as a high reliability screening and qualification procedure. This procedure is applicable to all bipolar digital and linear integrated circuits. Exceptions are made for dielectric isolation and MOS devices which must be considered on an individual basis in the applicable procurement document. It is recommended that this test be done on a 100 percent basis for all encapsulated devices which must meet the most stringent reliability requirements, and on a lot sampling basis for all normal high reliability encapsulated devices. The monitored thermal cycle (MTC) test should follow any other high stress nondestructive screen tests.

### 2. APPARATUS/METHOD REQUIREMENTS

The following paragraphs outline a suggested equipment configuration. Any alternate configuration which will perform to the required specification is acceptable. Paragraph numbers refer to the interconnection block diagram in Figure B1.

(1) Temperature Chamber: Capable of programmed temperature cycling over the temperature range from room temperature to -65°C, then up to +150°C and back to room temperature again, at a rate not to exceed 3°C/min. This slow rate is required to minimize the possibility of damage by thermal shock effects. The temperature should be monitored by a low mass thermocouple mounted in contact with one of the integrated circuits being tested.

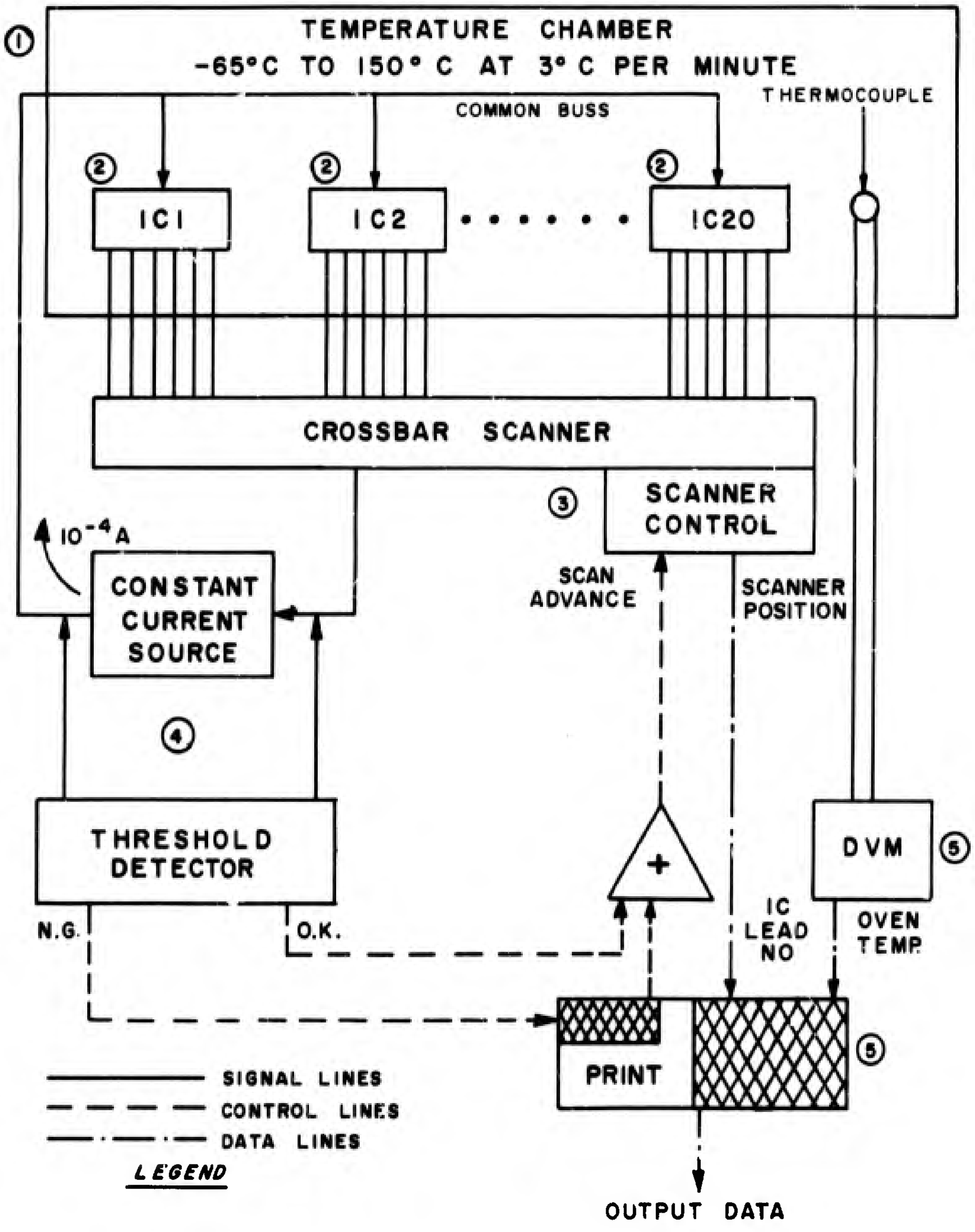


Figure B1. Equipment Diagram

(2) Test Sockets: Test sockets should be mounted in the temperature chamber with the maximum number of sockets determined by the chamber, scanner, or test capacity. The sockets should be of the type to allow easy connection of a plug-in jumper to any pin to establish a common connection to the substrate pin of each device.

(3) Scanner Equipment: Scanner equipment must automatically scan all integrated circuit pins and provide connection to a constant current source. Each pin shall be checked at temperature increments of no more than 5°C. The scanner may be of any form which will accomplish the sequential connection to each successive integrated circuit pin in the test chamber, including crossbar scanners, all electronic scanners, reed relay scanners, etc.

(4) Constant Current Source and Voltage Comparator: A constant current source and voltage comparator shall be used to determine whether continuity exists. The constant current source of 0.1 milliampere or less is connected through the scanner to the integrated circuit pin with current flow in such a direction as to forward bias the substrate junction. The voltage developed across the device will be monitored with a voltage comparator. This voltage comparator, with a preset threshold, will then determine if continuity is established at each pin, direct the system to check the next pin or punch out a failure, and then check the next pin.

The voltage comparator should be set with a threshold typically 1.0 volt higher than the maximum voltage expected to be developed across a good integrated circuit at the specified current level. This value is best established by a curve tracer check of several good circuits, or may be obtained through a complete device circuit analysis. Any time a voltage exceeds this threshold, a failure (open pin) signal is sent to the data acquisition system to punch out the scanner location and integrated circuit temperature. The constant current source should be disabled (shorted) during scanner contact transfer from one integrated circuit pin to the next. The constant current source should also have a voltage limit set at less than 5 volts above the comparator threshold limit.

(5) Data Acquisition System: The data acquisition system will punch data on paper tape upon receipt of a command from the comparator that a failure is present. The data shall include the scanner location of the failure, the temperature of the integrated circuit, and a symbol to indicate the end of each complete scanner cycle, as well as the temperature at the end of each cycle. The data will be in a format consistent with any computer data analysis program used. As an alternative, the entire MTC test may be under computer control, and the required data fed directly into the computer memory.

(6) Computer Data Analysis Program: A computer data analysis program shall be used to enable easy interpretation of the data obtained. Data may be plotted for the failed pins as a function of temperature or printed as a numerical range of temperature over which any pins are failures.

## 3. PROCEDURE

The devices will be placed in a temperature chamber, then cycled form room temperature to -65°C ±5°C then to +150°C ±5°C and back to room temperature again, at a rate not to exceed 3°C/min. During this temperature cycling, the continuity of each IC lead, with respect to the integrated circuit forward biased substrate junction, will be checked at least once during each 5°C change in temperature. The continuity checking circuit shall limit the test current to $10^{-4}$ amperes and the applied voltage to five volts greater than the maximum required to check any pin on a good device of that type. The continuity checking circuit shall be disabled during transfer from one lead to the next.

At the conclusion of the cycling, the test data shall be analyzed for any intermittent leads occurring over a temperature range. Manual verification of a failure may be done if necessary.

## 4. SUMMARY

The following details shall be specified in the applicable procurement document:

a. Temperature cycling characteristics if other than in Section 2, para (1).

b. Test current if other than $10^{-4}$ amperes in Section 2, Para (4).

c. Threshold voltage for rejection in Section 2, Para (4).

d. Parameter measurements to be performed after test.

e. Criteria for lot acceptance or rejection.

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13. ABSTRACT

The problem of temperature intermittent operation in encapsulated integrated circuit is discussed and a technique is presented which has been effective in detecting potential failures resulting from metallization, bond or lead wire temperature intermittents. These are the main causes of intermittent operation in encapsulated microcircuits at present, and this technique should lead to improvement in encapsulated device reliability if implemented as a screening or qualification test.

The instrumentation used at RADC for this technique, called the Monitored Thermal Cycle Test (MTC), is presented and a proposed standard test method, based on this test is included as an Appendix. Several representative device failure analysis summaries are included to illustrate the cause of typical encapsulated integrated circuit intermittents resulting from failure of the lead wire-bond-interconnect system.

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