AD 727803

FINAL REPORT

SYNTHESIS OF COMPOUND SEMICONDUCTING MATERIALS AND DEVICE APPLICATIONS

July 1, 1970 - June 30, 1971

Grant No. DAHC15 70-G-12

CMR-71-13

CENTER FOR MATERIALS RESEARCH

STANFORD UNIVERSITY • STANFORD, CALIFORNIA

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July 1, 1970 - June 30, 1971

Sponsored by
Advanced Research Projects Agency
ARPA Order No. 1644

Program Code Number: POD10

Contractor: Stanford University

Grant No. DAHC15 70-G-12

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Effective Date of Grant: July 1, 1970

Grant Expiration Date: June 30, 1971

Amount of Grant $184,141

Grant Title: Synthesis of Compound Semiconducting Materials and Device Applications

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I. INTRODUCTION

The program initiated at Stanford University on the Synthesis of Compound Semiconducting Materials and Device Applications has two important objectives: 1) the development of high quality GaAs and other mixed III-V semiconductor thin film single crystals for use in microwave and acoustical device research and development, and 2) the development of a coordinated program of research incorporating fundamental research studies relating to materials preparation and characterization, and the design, construction and testing of specific devices.

Gallium arsenide and the mixed III-V semiconductors were chosen for study because of their widespread importance in optical and electronic devices. New applications for these materials, such as in microwave devices, infrared optics, luminescent displays, are being discovered. For the purposes of our own device interests, epitaxial thin films hold the greatest promise. The materials presently available however, are frequently of lower overall quality than that required for these more advanced applications. The pivotal part of the program therefore is materials preparation.

The epitaxial crystal growth section has concentrated on the production of GaAs films of high purity with controlled surface morphology to allow complex electrode geometries, and with thicknesses varying from less than 1μm to 30μm. The material studies program has placed strong emphasis on the fundamentals of crystallization and interfacial phenomena in the Ga-As system, the influence of post growth annealing upon the properties of compound semiconductors including precipitation phenomena in Zn doped GaAs, and the relationship between dislocations and the mechanical and electronic properties of these materials.

The device group has been interested in using epitaxial layers in essentially three types of devices: 1) a unilaterial Gunn amplifier 2) an improved GaAs FET amplifier and 3) a surface acoustic wave amplifier.

At the completion of the first year of this program several significant advances were made. In the area of materials preparation and epitaxial growth high quality GaAs can be prepared. Liquid phase epitaxy techniques were expanded through the use of controlled temperature gradients to yield almost

perfectly smooth, uniform layers, achieved prior to this work only by vapor techniques. Typical layers produced by liquid phase epitaxy yield lower carrier densities and higher mobilities than vapor grown films. Techniques for substrate preparation were substantially improved and uniform films from 3 to 30 microns thick have been produced. Wafers suitable for device fabrication are now being produced and supplied to the microwave section. Some devices have been fabricated and the results are given in the text along with details of the work to produce high quality ohmic contacts.

During the first six months the materials studies program was involved with the construction of relevant equipment and the development of specific techniques required for each phase. During the latter part of the program preliminary data has been obtained and is described in the following report.

II. EPITAXIAL CRYSTAL GROWTH

R.S. Feigelson, B.L. Mattes, R.K. Route, and J. Yen

A. PROGRAM OBJECTIVE

The epitaxial crystal growth effort is directed toward developing and evaluating liquid and vapor phase methods to prepare high quality layers of III-V semiconductors. This section of the program is coordinated with the other sections to prepare materials with specific dimensions and properties and to interact on problems of mutual concern and interest.

The principal device requirement has been the preparation of high quality, uniform and reproducible layers of GaAs with n-type carrier densities in the mid 10^{14} cm^{-3} range, room temperature mobilities of 7000 cm^2/v-sec, thicknesses in the 1-30 μm range, and optically smooth surfaces. Considerable emphasis this period has been placed on obtaining layers that are optically smooth and less than 10 μm in thickness. These objectives have expanded into the development of new methods for growth, the study of variables that control growth, techniques to prepare and handle the materials involved in growth, and methods to evaluate the growth and its properties.

The future effort will extend the present objectives on III-V semiconductors to include the preparation of reliable ohmic contacts on these high purity layers and to grow epitaxial layers on piezoelectric substrates.

B. PROGRESS

1. Achievements

High quality GaAs epitaxial layers have been grown with carrier denaities as low as 10^{14} cm^{-3}, room temperature mobilities as high as 7700 cm^2/v-sec, and thicknesses as thin as 3 μm. In addition, layers have been grown that are nearly optically smooth with no terraces. The latter has been achieved by imposing a

temperature gradient normal to the liquid-solid interface and by improving the substrate polishing techniques. These objectives were achieved by liquid phase epitaxial methods of growth. During this period, over 100 GaAs layers were grown on both n+ and semi-insulating GaAs substrates.

The methods of growth, techniques of preparation, and measurement of properties used to meet these objectives will be described in the remainder of this report.

2. Growth Methods

It has been established that liquid phase epitaxial (LPE) methods of growth can meet all the present requirements for high quality GaAs layers. Since layers in the 1-10 μm range have been grown by LPE methods, the vapor phase epitaxial (VPE) method of growth was not developed during this period.

Several improvements have been made on the LPE methods of growth described in the first Semi-Annual Technical Report.[1] The most significant modifications were made to the horizontal tilt process. A cell that will induce a temperature gradient normal to the solid-liquid interface was designed and constructed out of high purity graphite, as shown in fig. II-1. The cell operates in a homogeneous temperature region in the furnace. The temperature gradient is induced by removing heat from the liquid Ga reservoir underneath the growth cell. The growth end of the cell has a very thin bottom (.03 inches) between the substrate and liquid Ga reservoir. This localizes and promotes heat transfer in this region. The heat is drawn out of the liquid Ga reservoir by forcing He gas or water through the immersed quartz heat transfer tube. The liquid Ga reservoir serves two purposes: (1) to gain good thermal contact between the heat transfer tube

and the growth cell, and (2) to improve the temperature uniformity over the bottom plane of the growth region. The same tilting technique is used to saturate the liquid Ga with As and to roll the saturated Ga onto the substrate for growth. The temperature gradient, however, is not induced until a minute before the growth tilt. This allows the temperature gradient to build up but minimizes a drastic reduction of the substrate temperature to below the source temperature. This procedure is still subject to changes that will be dictated by future detailed temperature measurements in the growth region. The temperature gradient has not been measured, however, it was found that He gas, rather than N_2 gas, was required to establish a sufficient temperature gradient to stabilize the growth interface.

The other changes in the horizontal tilt process, without a temperature gradient, include the following: (1) The liquid Ga is prebaked prior to saturation on the GaAs source. This eliminates undissolved GaAs from previous growths in the As-saturated Ga before it is rolled onto the source. (2) For fast cooling rates (200 to 600° C/hr) the furnace is shut off immediately before the As-saturated Ga is rolled onto the substrate. This gives an abrupt decrease in the temperature at nearly a constant rate and yields more consistent growths.

No major changes in the vertical cell process [1] have been made. The new Poco Graphite cell is in use, fig. II-2. The substrate is more easily loaded and unloaded than in the initial design. The steady state process, [1] using the same cell, has not been attempted yet because of the new developments in the horizontal tilt processes.

3. Substrate Preparation

Significant improvements in the preparation of GaAs substrates have been made that yield reproducible and defect free growths. The two areas that have been perfected are in the polishing and the final cleaning procedures before growth. The lapping and polishing procedures are all carried out with 3 to 6 substrates bonded with carnuba wax to a 4 inch diameter stainless steel plate, fig. II-3. The procedures are as follows:

a) A rough lap to remove all saw marks on both sides of the substrate is done with 5 μm silicon carbides on a flat glass plate.

b) A fine lap to remove all traces of a) on the side of the substrate to be polished is done with 0.3 μm alumina on a rotating "Pellon" pad.

c) A polish is started with 0.3 μm alumina on a rotating "Polytex Supreme" pad.

d) A final mechanical polish is done with 0.3 μm alumina on a rotating "Polytex Supreme" pad coated with paraffin.

e) A chem-mechanical polish is done with 10% "Clorox" solution on a rotating "Polytex Supreme" pad, fig. II-4.

f) A rinse of the substrates for a minimum of 10 min. is done with deionized water.

The substrates are then removed from the stainless steel plate and cut to the desired dimensions. Before cutting, a protective layer of wax is coated over the polished surface. The substrates are cut with a wire saw and slurry or cleaved along a (110) direction. For the vertical cell, round discs are cut with the end of a rotating cylinder and slurry.

Prior to growth the substrates are cleaned and handled by the following procedure:

a) The wax is removed with trichloroethlyene.

b) The weight of the substrate is recorded.

c) The surfaces are washed with an "Aquet" solution and lightly scrubbed with a "Q-tip".

d) The substrate is boiled sequentially in trichloroethylene, acetone, and methanol.

e) The substrate is rinsed 3 times with isopropanol.

f) The substance is rinsed at least 4 times with doubly distilled deionized water.

g) The substrate is withdrawn from the doubly distilled water with the water clinging uniformily to the polished surface.

h) The water is gently blown off the substrate with N_2 onto a supporting filter paper.

The substrate is then loaded into the cell without any further treatment.

4. Growth Results

The results obtained from over 100 epitaxially grown GaAs layers in the horizontal homogeneous temperature and temperature gradient processes, and vertical process are summarized in Tables II-I, II-II, and II-III, respectively. The general features of the early growths, as discussed in the first Semi-Annual Technical Report[1], indicated the importance of substrate preparation and a need for controlled stabilization of the liquid-solid interface. The problems that arose then have now been virtually eliminated with the improved substrate preparation

procedures, figs. II-6a and b. The essential features to note are the absence of scratch and stain deliniations in the layers and second, the virtual absence of terraces when a steep temperature gradient (magnitude to be determined) is used.

The temperature gradient stabilizes the growth interface for cooling rates greater than 100° C/hr for (100), (111)-A, and (111)-B orientations. Figures II-7a and b show the dramatic effect for the (100) orientation. Note the absence of cellular growth with a steep temperature gradient and there is slight evidence of terraces. These results are in agreement with the results of Andre and LeDuc[2] who used a secondary heater over the As saturated Ga. With this process it was also observed that the terraces became finer as the cooling rate was increased.

The temperature gradient also reduces the amount of GaAs that forms on top of the liquid Ga during growth. This indicates that there is a temperature gradient in the liquid Ga that drives more of the As towards the substrate. Attempts to roll the liquid Ga off the substrate during and after growth, however, have still failed, even with less GaAs crust and smoother epitaxial surfaces.

Thin uniform epitaxial layers, thicknesses less than 10 μm, have been achieved by lowering the saturation temperature, holding the amount of liquid Ga constant. Saturation temperatures as low as 575°C have produced 2-3 μm layers. Thinner layers are definitely possible on the (111)-B orientation, but nucleation on the (111)-A orientation is a problem without a temperature gradient. Triangular and elongated hexagonal hillocks are observed on the (111)-A orientation, figs. II-8a and b. It is interesting to note the two types of hillocks formed and their uni-

formity in size. The smaller hexagonal shaped hillocks appear to be nuclei forming on the substrate. The larger triangular hillocks are all attached to the substrate by a y-shaped web, as shown in fig. II-9, where the hillock was cleaved off the substrate. The thinner films, as yet, have not been attempted in the temperature gradient cell.

The vertical cell process has yielded growths that show a slight peak at the center of the layer surrounded by terraces, fig.II-10. The occurrence of the peak appears to be independent of orientation. From the symmetry of the cell this is probably caused by a radial temperature gradient in the furnace. Again as in the horizontal temperature gradient process, there is no GaAs crust formed on top of the liquid Ga, but there is considerable crust formed along the side of the tube, becoming thicker towards the substrate.

5. Electrical Properties

Schottky barrier and van der Pauw measurements are used to evaluate the electrical properties of the GaAs layers. The results are summarized in Tables II-I, II-II and II-III. Good agreement is found between the measurements by both techniques.

The procedure used to prepare the layers for these measurements is as follows:

a) The Ga is thoroughly removed from the layer, after growth, with warm HCl.

b) The layer is rinsed in deionized water and then doubly distilled deionized water.

c) The layer is withdrawn from the distilled water with a uniform layer of water clinging to it.

d) The water is gently blown from the layer with dry nitrogen onto a supporting filter paper.

e) Four small In beads are pressed onto the layer at four corners, and then the layer is placed in a vacuum furnace at 400°C, for 5 minutes.

Van der Pauw measurements are done at this stage at 77°K and 300°K, in a magnetic field of 2 kgauss. Following this measurement the layer is degreased and steps 2) through 4) are repeated. Either Al or Au electrodes are then evaporated onto the layer through a 425 μm or 1000 μm perforated mask. The Schottky barrier measurements are made at 1 MHz with a capacitance bridge and a dc bias supply.

The analysis of the Schottky barrier capacitance measurements, to obtain the carrier density, is shown in figs. II-11 to 13. In fig.II-11, an extrapolation is made to determine a capacitance CO, where the Schottky barrier capacitance is zero for an infinite bias. The value of CO represents not only the stray capacitances in the leads but also the shunting capacitances within the layer from the Schottky barrier electrode to the ohmic electrode e.g., the edge capacitance. The measured capacitance values minus CO are then plotted as $1/C^2$ vs. V, fig.II-12, to obtain the slope that is proportional to the carrier density. Note that CO is not a fudge factor to obtain a constant slope since the small reverse bias voltage data are not used, fig. II-11. The data, as plotted in fig. II-11, is very non-linear in this bias range because the bias is comparable to the forward bias breakover voltage. Figure II-13 shows the carrier density vs. depletion

about twice as great as the jig and lead capacitance.

This technique for analyzing the Schottky barrier capacitance data appears to be a reliable means of determining the carrier density profiles of samiconducting layers deposited on semi-insulating substratas. Tha technique essentially corrects the measured data to fit tha ideal parallel plate capacitance conditions.

C. PROPOSED FUTURE WORK

The advantage achieved in developing several methods to grow epitaxial layers of III-V semiconductors is the ability to better understand tha machanism of growth and to prepare high quality thin films. Thera ara several tachniquas that will be explored to provide additional information on the growth and properties of epitaxial films and to facilitate their use in davices, namaly 1) differential thermal analysis to determine the effects of As saturation in Ga on supercooling and nucleation; 2) ion microprobe analysis to determine impurity profiles in these layers and interface regions; 3) photo-luminescence measurements to detect and identify deep level traps in these layers; 4) Berg-Barrett type x-ray measurements to study dislocation networks associated with lattice mismatches between the layer and substrate; 5) vapor phase growth methods to grow thinner layers with an adaptability to prepare these layers on insulating piazoelectric substrates; 6) development of techniques to prepare reliable ohmic contacts, such as n^+n contacts to the low carrier density materials; and 7) development of new substrate preparation techniques such as r.f. sputtering.

The results from differential thermal analyses, ion microprobe analyses and photo-luminescence measurements will yield information on nonequilibrium distribution coefficients during crystallization. These coafficiants limit or accentuate the impurities that come out of solution at tha liquid-solid interface.

layer depth for several values of CO. Note that the extrapolated value of CO does give the best overall uniformity in carrier density. When CO is too small there is an apparent gross nonuniformity in carrier density near the surface, and for CO too large the nonuniformity appears deep in the layer. The use of the extrapolated value of CO for fig. II-11 yields a carrier density that is in agreement with the van der Pauw measurements. It should be noted that the CO extrapolation technique works only in a bias region where there is a uniform carrier density.

To show that CO depends on the edge capacitance or some other capacitive effect in the layer, the value of CO was plotted vs. the carrier density, fig. II-14. Note that as the carrier density increases, CO does increase, in agreement with the increased polarizability of the layer. The method of determining CO was found to work for layers on both semi-insulating and n+ substrates.

A further check on the CO extrapolation method, for correcting the data to determine the carrier density, was done by increasing the electrode diameter from 425 μm to 1000 μm. The zero bias capacitance increased by the ratio of $(1000/425)^2$, but there was no discernable change in CO and the carrier density came out to the same value. Why the value of CO changed for thin layers, fig. II-14, is not known, However, the field lines due to edge effects may be greatly exaggerated in thin layers on semi-insulating substrates. In general, CO increases slightly for Schottky barrier electrodes close to the ohmic electrode.

For layers with low carrier densities ($< 3 \times 10^{14} cm^{-3}$), it was possible to directly measure the capacitance between two ohmic contacts on the layer. For thick layers the measured capacitance was about the same as CO, a value that is

The apparatus for thermal differential analysis and photo-luminescence measurements are available in the CMR facilities. The ion microprobe analysis will be carried out at a commercial analytical facility. This analysis is unique in that every element and isotope in the periodic table can be detected. The analysis will give a three-dimensional scan of these elements through the thickness of a layer with resolutions approaching 40 Å and detectable concentrations under certain conditions approaching 10 parts per billion.

The analysis of dislocations and their networks will give information on the mechanical defects propagated from substrate to the layer, lattice mismatch between substrate and layer, and junctions between different nuclei during initial stages of growth on the substrate. The dislocation networks may, in part, be responsible for terraces observad at the surface of the layers. The x-ray, transmission and acanning electron microscopes are available in the CMR facilities for such measurements.

Since the main effort is to grow epitaxial thin films and the approach is to develop high quality films by attacking the problem through different methods of growth, the vapor phase method effort will be developed. The vapor phase method is suitable for the growth of 1 to 10 μ layers on dissimilar substrates, preparation on n^+n contacts and is adaptable to most of the III-V compounds.

The substrate preparation effort will be expanded to include r.f. sputtering techniques, vapor phase etching and polishing, pre-deposited base layers, and general handling techniques to minimize contamination prior to growth. The surface condition has considerable effect on the properties and surface features of the layer. The ultimate goal will be the preparation of optically flat parallel layers on optically flat substrates.

There will be a continued effort to improve the liquid phase methods for growth, especially for other III-V semiconductors. The emphasis will be placed on lower background impurity levels to achieve liquid nitrogen mobilities that will appraoch 2 x 10^5 cm^2/V. sec.

REFERENCES

II-1. Semi-Annual Technical Report, "Synthesis of Compound Semiconducting Materials and Device Applications", AD-718 878, ARPA Contract No. DAHC 15-70-G-12, Stanford University, July 1, 1970 - December 31, 1970.

II-2. E. Andre and J.M. Le Duc, Mat. Res. Bull. 3, 1 (1968).

TABLE I

GROWTHS FROM HORIZONTAL TILT PROCESS

GROWTH NO.	$\mu(300^\circ K)$ / $\mu(77^\circ K)$	CARRIER TYPE/ DENSITY	SUBSTRATE ORIENTATION	SATURATION TEMP. / COOLING RATE	RESULTS AND COMMENT	CHANGES
29.			(111) - A	750°C / 15°C/hr.	Smooth layer with light terracing, 2.0 mils thick. Sharp I-V breakdown.	Added additional S_n to melt for n-type material.
30.			(111) - B	750°C / 50°C/hr.	Incomplete nucleation, hexagonal hillocks. Probably due to inadequate cleaning of substrate.	Increased cooling rate.
31.			(111) - B	750°C / 15°C/hr.	Terraces with large dendritic growth along edges.	Normal cooling rate. Roughly lapped substrate with no subsequent polishing.
32.		n-type	(111) - B	750°C / 7°C/hr.	Terraces surrounded by heavy dendritic growth.	Clean reactor tube. Improved substrate cleaning procedure with chem.-mechanical polish. Floating substrate. Reduced cooling rate.
33.			(111) - A	750°C / 7°C/hr.	Layer accidentally grown on roughly-lapped back side of substrate. Incomplete nucleation with many holes.	Floating substrate.
34.		n-type	(111) - B	760°C / 15°C/hr.	Incomplete nucleation with petal-like terracing.	Chem.-mechanically polished substrate pitted with air-abrasive to increase nucleating sites. Submerged substrate. Clean reactor spade.
35.		n-type	(111) - B	760°C / 10°C/hr.	Relatively good layer, 2.0 mils thick, with several minor flaws near the center. Light terracing.	Floating substrate.
36.		n-type	(111) - B	760°C / 10°C/hr.	Good layer with light terracing.	Cleaned system. Submerged substrate.
37.			(100)	750°C / 10°C/hr.	Overlapping, irregular terraces.	
38.		2×10^{14} cm^{-3}	(111) - B	750°C / 10°C/hr.	Sharply defined terraces, plateau in corner. No dendritic growth along edges of layer. Major improvement!	Used square "picture frame" carbon mask to prevent dendritic growth around edges.
39.		3×10^{14}	(111) - B	760°C / 10°C/hr.	Very good layer with fine terracing. Plateau in corner.	Cleaned system. Used fresh charge of Ga. Substituted halocarbon grease for silicone grease in glass-glass seals.
40.		3×10^{14}	(111) - B	650°C / 10°C/hr.	Light terracing. Carbon mask improperly aligned causing some dendritic growth along edge.	Reduced saturation temperature from 750°C to 650°C to reduce layer thickness.

TABLE I (CONT'D)

GROWTHS FROM HORIZONTAL TILT PROCESS

GROWTH NO.	$\mu(300^\circ K)$ / $\mu(77^\circ K)$	CARRIER TYPE/ DENSITY	SUBSTRATE ORIENTATION	SATURATION TEMP. / COOLING RATE	RESULTS AND COMMENT	CHANGES
41.		2×10^{15}	(111) - B	650°C / 10°C/hr.	Medium terracing. Otherwise smooth layer, approximately 15 microns thick.	
42.	6,800 / 68,000	3×10^{14}	(100)	650°C / 10°C/hr.	Smooth layer with fine terracing. Incomplete nucleation in local region - probably due to inadequate cleaning.	
43.		p-type	(100)	760°C / 10°C/hr.	Poor layer due to inadequate substrate preparation and movement of mask during initiation of growth.	Cleaned system. Increased saturation temperature.
44.		p-type	(100)	760°C / 10°C/hr.	Fine terracing with one significant plateau.	
45.		p-type	(100)	650°C / 250°C/hr.	Excellent layer, very fine terracing, few pock marks.	Increased cooling rate to 250°C/hr.
46.		10^{15}	(111) - B	660°C / 300°C/hr.	Excellent layer, smoother than #45.	Added Sn to Ga melt to produce n-type material. Increased cooling rate with fan.
47.	7,200 / 40,000	7×10^{14}	(100)	660°C / 300°C/hr.	Good surface except for acetone stained region.	Changed cleaning procedure (acetone as final rinse instead of isopropyl alcohol).
50.			(111) - B	660°C / 300°C/hr.	Very irregular surface with overall etch-back.	No mask used.
52.	6,300 / 30,000	2×10^{15}	(111) - B	660°C / 300°C/hr.	Uniform surface, fine terracing, no plateau.	System cleaned, baked out at 850°C, mask used.
53.			(100)	660°C / 300°C/hr.	Closely packed square hillocks.	Specimen #45 reused as substrate.
55.			(100)	660°C / 400°C/hr.	Closely packed rectangular hillocks. Some polishing scratches show through epi layer.	
56.			(311)	650°C / 200°C/hr.	Irregular surface features.	Hand polished substrate on silk screen with 0.3μ powder.

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TABLE I (CONT'D)

GROWTHS FROM HORIZONTAL TILT PROCESS

GROWTH NO.	$\mu(300^\circ K)$ / $\mu(77^\circ K)$	CARRIER TYPE/ DENSITY	SUBSTRATE ORIENTATION	SATURATION TEMP. / COOLING RATE	RESULTS AND COMMENT	CHANGES
59.			(100)	675°C / 200°C/hr.	Moderate, irregular terracing. Square hillocks in one corner.	
60.			(100)	690°C / 200°C/hr.	Petal-like terracing. Polishing scratches show through epi layer.	
62.			(100)	690°C / 200°C/hr.	Uniform surface, fine terracing. At high mag. fine protrusions can be seen all over surface particularly along terrace steps.	No mask used. Mechanically polished substrate.
63.			(111) - A	690°C / 250°C/hr.	Isosceles triangular and connected triangular hillocks over perfectly smooth surface. All triangles are similarly oriented. Source rolled over with Ga.	Chem.-mechanically polished after hand polishing on silk screen. No etching.
66.			(111) - A	660°C / 250°C/hr.	Widely spaced flat terracing, very shapely defined. Scratches visible through layer. Source rolled over with Ga.	10 gm Ga baked out at 850° over week-end, 1 mg S_n added. No mask used
67.			(111) - A	660°C / 250°C/hr.	Increased density of features as in #63. Source rolled over with Ga.	No etch. All fans and blowers shut down during growth, low vibration condition.
71.	4,800 / 14,000	3×10^{15}	(111) - A	650°C / 250°C/hr.	Uniform, moderate terracing. Source rolled over with Ga.	Mask used. Etched in very weak Br for 20 min. Minor room vibration during growth.
73.			(111) - A	660°C / 250°C/hr.	Triangular hillocks evenly spaced over surface.	System filled with H_2, but no H_2 flow during growth. Chem.-mech. lapped by dripping method. No etch. No mask used. All fans and blowers off. Additional GaAs added to system to increase As partial pressure.
75.			(111) - A	650°C / 250°C/hr.	Irregular triangular hillocks. Less densely scattered along one side of substrate.	Chem. polished with 16:1 H_2SO_4-H_2O_2 after chem.-mech. lapping. 45 sec. etch in 2% Br-Methanol.
76.			(111) - B	660°C / 250°C/hr.	Irregular terracing.	
77.			(111) - B	660°C / 250°C/hr.	Similar to #76.	No crushed GaAs in spade. New source used. Room very quiet during growth period.

TABLE I (CONT'D)

GROWTHS FROM HORIZONTAL TILT PROCESS

GROWTH NO.	$\mu(300^\circ K)$ / $\mu(77^\circ K)$	CARRIER TYPE/ DENSITY	SUBSTRATE ORIENTATION	SATURATION TEMP. / COOLING RATE	RESULTS AND COMMENT	CHANGES/FURNACE SYSTEM
78.			(111) - A	680°C / 300°C/hr.	Very uniform, fine, irregular terracing with plateau near one corner.	30 minute saturation period.
79.			(111) - A	650°C / 150°C/hr.	Off-center plateau with irregular terracing encircling it. Terraces become finer toward edge.	Circular substrate used, no masking, no etch.
81.	4,800 / 25,000	7×10^{14}	(111) - B	688°C / 15°C/hr.	Mask shifted during growth. Plateaus on all sides, medium terraces and several polishing defects.	Moved from Microwave Lab to McCullough Bldg. All systems and components thoroughly cleaned. New C-15D H_2 purifier installed. Boat and mask baked out. New Ga baked out. Doubly distilled deionized water used for final rinse of substrate. / N-2
82.		2×10^{14}	(111) - A	654°C / 15°C/hr.	Mask did not rest on substrate due to irregular boat bottoms. Coarse, irregular terraces.	Boat rested in lowest possible position in reaction tube. / N-2
83.			(111) - A	650°C / 150°C/hr.	Triangular hillocks on a perfectly smooth layer.	Increased cooling rate. / N-2
84.	3,400 / 9,000	3×10^{14}	(111) - A	650°C / 50°C/hr.	Uniform distribution of coarse terraces.	New Ga and source used. False carbon bottom added to boat and baked out at 850°C. / N-2
85.		2×10^{15}	(111) - B	670°C / 15°C/hr.	Irregularly shaped coarse terraces.	Reactor tube cleaned. Mask, lid and false bottom used. / N-1
86.	7,700 / 62,000	2×10^{4}	(111) - A	822°C / 15°C/hr.	Medium terraces with a plateau and an irregular growth area.	Increased saturation temperature. / N-1
87.	3,700 / 5,500		(111) - A	660°C / 500°C/hr.	Fine, irregular terraces surround one small plateau.	16:1 chemical polish used. Saturated Ga with GaAs crunch in center of boat, then rolled Ga onto source for 15 min. Used fan to cool reaction tube. / N-2
88.	7,000 / 53,000		(111) - B	899°C / 15°C/hr.	Medium terraces with large plateau. Ga did not roll off substrate.	Lid placed beneath boat to raise boat in tube. Tried to roll Ga off substrate at 812°C. / N-1

TABLE I (CONT'D)

GROWTHS FROM HORIZONTAL TILT PROCESS

GROWTH NO.	$\mu(300^\circ K)$ / $\mu(77^\circ K)$	CARRIER TYPE/ DENSITY	SUBSTRATE ORIENTATION	SATURATION TEMP. / COOLING RATE	RESULTS AND COMMENT	CHANGES/FURNACE SYSTEM
89.			(111) - B	658°C / 400°C/hr.	Very uniform, extremely fine terraces.	Repeat of Growth 87, but on B surface. / H-2
90.	7,500 / 42,500		(111) - A	801°C / 15°C/hr.	Medium terraces with two plateaus. Ga did not roll off substrate.	Repeat of Growth 88, but with lid on boat. / H-1
91.			(111) - A	658°C / 200°C/hr.	Fine, uniform terraces, no plateau.	Repeat of Growth 87 at slower cooling rate. / H-2
92.	3,200 / 10,600		(100)	640°C / 600°C/hr.	Very distinct, rectangular, cellular growth, uniform distribution.	Repeat of Growth 87, but on (100) at fast cooling rate. / H-2
93.			(111) - A	586°C / 15°C/hr.	Very small, elongated, hexagonal hillocks in-between large, triangular hollocks, no layer former.	Mask baked out. Lid baked out after contamination with rubber glove. Broken mask used. / H-1
94.			(111) - B	612°C / 15°C/hr.	Very large, irregular, partially separated terraces.	Boat replaced with boat, mask and lid from H-1. / H-2
96.			(111) - B	600°C / 200°C/hr.	Large, irregular, partially overlapping terraces and fine, irregular terraces on bevelled substrate.	Repeat of Growth 87, but on (111)-B surface and a lower saturation temperature. / H-2
97.			(111) - B	600°C / 600°C/hr.	Fine, uniform terraces.	Repeat of Growth 96 at a faster cooling rate. / H-2
99.	700 / 950		(111) - B	599°C / 10°C/hr.	Large, noneverlapping terraces extending upwards from substrate surface with very small terraces in between large ones.	Repeat of Growth 96 at a very slow cooling rate. / H-2
102.			(100)	594°C / 200°C/hr.	Irregular, patal-like terraces.	Repeat of Growth 96, but on a (100) . / H-2
104.		7×10^{15}	(111) - A	608°C / 15°C/hr.	Very fine, even terraces. Mask floated off substrate, but layer remained uniform.	Reactor tube cleaned. Spade broke and replaced with one from H-1. Leaking valve cleaned. Baked out at 850°C. Mask used. / H-2
107.	2,900 / 4,300		(100)	618°C / 20°C/hr.	Medium terraces, several polishing defects.	Repeat Growth 104, but on (100) . / H-2

TABLE I (CONT'D)

GROWTHS FROM HORIZONTAL TILT PROCESS

GROWTH NO.	$\mu(300^\circ K)$ / $\mu(77^\circ K)$	CARRIER TYPE/ DENSITY	SUBSTRATE ORIENTATION	SATURATION TEMP. / COOLING RATE	RESULTS AND COMMENT	CHANGES/FURNACE SYSTEM
109.		2×10^{16}	(111) - A	618°C / 25°C/hr.	Medium terraces, concentric about plateau. Very small grooves appeared in triangular arrangements on several of the terraces.	Repeat of Growth 104 . / H-2
114.	4,900 / 15,600	5×10^{15}	(111) - B	700°C / 600°C/hr.	Very fine terraces.	Replaced spade and baked out with Ga at 850°C. H-1 and V-1 valved off and H_2 supply purged for 4 hr. No mask used. / H-2
115.		5×10^{15}	(100)	678°C / 600°C/hr.	Very fine, uniform terraces. A few polishing defects still present.	Politex "Supreme" pad used for chemical mechanical polish. n^+ substrate. / H-2
116.			(100)	625°C / 600°C/hr.	Very fine terraces with a few Ga inclusions. A few polishing and stain defects.	Repeat Growth 115, but at lower saturation temperature. / H-2
117.	3,200 / 4,200	10^{16}	(111) - B	595°C / 500°C/hr.	Fine, uniform terraces. No polishing or stain defects.	New Ga used and baked out at 850°C. Substrate cut from large slice after polishing. / H-2
118.			(100)	595°C / 600°C/hr.	Fine, irregular terraces with numerous fine Ga inclusions.	Repeat Growth 117, but on (100) . / H-2
119.	2,260 / 3,200	10^{16}	(111) - B	566°C / 600°C/hr.	Fine, uniform terraces. No preparation defects.	Repeat Growth 117, but at lower saturation temperature. / H-2
120.	3,900 / 7,900	8×10^{15}	(111) - B	694°C / 600°C/hr.	Very fine terraces with few polishing defects.	Reactor tube cleaned. / H-2
121.	5,900 / 19,500	10^{16}	(111) - B	755°C / 600°C/hr.	Very fine terraces. Numerous stain defects.	New Ga used and baked out at 800°C. / H-2
122.	4,700 / 11,000	10^{16}	(111) - B	694°C / 600°C/hr.	Very fine terraces. Numerous small stain defects.	Leak found in hydrogen purifier C-15B. Replaced H_2 purifier with C-5B. New Ga, baked out overnight at 800°C. / H-2
123.	4,200 / 8,800	10^{16}	(100)	604°C / 15°C/hr.	Very fine terraces. Numerous polishing and stain defects.	Changed orientation. Lowered cooling rate. / H-2
124.	4,450 / 16,500		(111) - B	699°C / 15°C/hr.	Extremely fine, uniform, parallel terraces. Several polishing defects.	Changed orientation. Increased saturation temperature. / H-2

TABLE I (CONT'D)

GROWTHS FROM HORIZONTAL TILT PROCESS

GROWTH NO.	$\mu(300^\circ K)$ / $\mu(77^\circ K)$	CARRIER TYPE/ DENSITY	SUBSTRATE ORIENTATION	SATURATION TEMP. / COOLING RATE	RESULTS AND COMMENT	CHANGES/FURNACE SYSTEM
125.	6,000 / 37,000		(100)	700°C / 200°C/hr.	Very fine terraces. Numerous stain defects.	New Ga baked out at 850°C. Boat lid removed. / H-2
126.	5,000 / 29,000	10^{15}	(100)	700°C / 200°C/hr.	Very coarse terraces with Ga inclusions along steps.	Cold trap baked out. Reactor tube cleaned. Carbon boat and false bottom vacuum fired. Tube and boat baked out overnight at 850°C. New Ga, baked out at 850°C. / H-1
127.	5,500 / 26,000	3×10^{15}	(111) - B	695°C / 600°C/hr.	Medium terraces.	Repeat of Growth 126 at faster cooling rate. / H-1
128.	5,700 / 24,000	2×10^{15}	(111) - B	697°C / 600°C/hr.	Very fine terraces.	Replaced reactor tube (spectrasil). Cleaned cold trap and valve, baked out. Vacuum-fired lid, false bottom. Oil in bubbler changed. New Ga, baked out at 850°C . / H-1
129.	5,050 / 10,000		(111) - B	697°C / 600°C/hr.	Very fine terraces.	Liquid H_2 trap was [illegible] filled. Reversed procedure in fin[illegible] [illegible]ming: "Alconox" wash followed degrease rinse.
130.	4,600 / 18,000		(111) - B	700°C / 600°C/hr.	Fine, irregular terraces. One polishing defect.	Cold trap and "Nupro" valves degreased, cleaned, and baked out. / H-1
131.			(100)	746.5°C / 15°C/hr.	Very irregular layer of coarse terraces. Ga would not roll off substrate during growth.	No false bottom. Source replaced with crushed GaAs which stayed in Ga puddle during deposition. / H-2
132.	5,200 / 16,000	10^{16}	(111) - B	689°C / 600°C/hr.	Fine, irregular terraces. No stains or polishing defects.	Thoroughly cleaned stainless tubing from liquid H_2 trap to H_2 purifier. System V-1 disconnected from purifier. Purge valve added to input to purifier. New Ga, baked out at 850°C. / H-1
133.	5,600 / 30,000	3×10^{15}	(111) - B	700°C / 600°C/hr.	Medium but very irregular terraces.	Used Ga from new bottle. Baked out with source and seed at 850°C. / H-1
134.	5,800 / 27,000	5×10^{15}	(111) - B	700°C / 600°C/hr.	Extremely fine and even terraces with a few polishing defects.	New carbon boat, vacuum-fired and baked out at 850°C. Removed false bottom. New Ga, baked out at 850°C. Iso-propanol used as final rinse for seed and source. / H-1

TABLE I (CONT'D)

GROWTHS FROM HORIZONTAL TILT PROCESS

GROWTH NO.	$\mu(300^\circ K)$ / $\mu(77^\circ K)$	CARRIER TYPE/ DENSITY	SUBSTRATE ORIENTATION	SATURATION TEMP. / COOLING RATE	RESULTS AND COMMENT	CHANGES/FURNACE SYSTEM
135.	4,600 / 15,700		(111) - B	702°C / 200°C/hr.	Very fine terracing. Several small Ga inclusions.	New GE 204 reactor tube. Completely recleaned system. He leak checked. "Alconox" wash followed degreasing of substrate. / H-2
136.	5,700 / 30,000	3×10^{15}	(111) - B	694°C / 200°C/hr.	Very fine terracing. Several stain and scratch defects.	"Aquet" replaced "Alconox" wash, followed by standard degrease and rinse procedures. 5:1:1 etch used on substrate. Boat and Ga baked out at 850°C. / H-2
137.			(111) - B	697°C / 200°C/hr.	Medium, irregular terraces.	"Aquet" wash followed by standard preparation of substrate without etch. / H-2
138.			(111) - B	700°C / 200°C/hr.	Uniform Ga inclusions in layer on an apparent stained or oxidized substrate.	Repeat of Growth 137, but without H_2. System was evacuated continuously with a "Vac-Sorb" pump. / H-2

TABLE II

GROWTHS FROM HORIZONTAL TILT TEMPERATURE GRADIENT PROCESS

GROWTH NO.	$\mu(300^\circ K)$ / $\mu(77^\circ K)$	CARRIER TYPE/ DENSITY	SUBSTRATE ORIENTATION	SATURATION TEMP. / COOLING RATE	RESULTS AND COMMENT	CHANGES
95.	4,200 / 6,000		(111) - B	695°C / 200°C/hr.	Irregular, fine terraces, interlaced with polishing defects.	Used temperature gradient cell for first time. Ga reservoir cooled with N_2 gas.
98.	4,300 / 7,200	5×10^{15}	(100)	700°C / 200°C/hr.	Very fine, even terraces with small plateau. No polishing or stain defects.	Iso-propanol used for final rinse. Repeat of Growth 95, but on a (100).
100.	5,050 / 16,700	2×10^{15}	(100)	700°C / 300°C/hr.	Mainly an excellent layer with extremely fine terraces. Large area however has defects due to a stain on substrate. Polishing defects show clearly through fine terraces.	Repeat of Growth 98 with distilled water rinse of substrate and Ga reservoir cooled with He gas.
101.	4,450 / 15,600	2×10^{15}	(111) - B	700°C / 200°C/hr.	Excellent layer with extremely fine terraces. Polishing defects are very distinct.	Repeat of Growth 100, but on a (111)-B.
103.	4,400 / 11,200		(111) - B	715°C / 200°C/hr.	Medium terraces.	Reactor tube cleaned. Spade broken and repaired. Baked out at 850°C. Repeat of Growth 101, but He turned off at 380°C.
105.		7×10^{15}	(111) - B	600°C / 350°C/hr.	Best surface features yet. No distinct terraces observable under microscope. Polishing defects are very distinct.	He turned on for 2 min. before tipping furnace.
106.			(111) - B	650°C / 350°C/hr.	Very fine terraces. Considerable evidence of substrate stains or incomplete polishing in some areas.	Repeat of Growth 101. n^+ substrate.
108.			(111) - B	750°C / 300°C/hr.	Very fine terraces. Numerous polishing defects.	Repeat of Growth 105. n^+ substrate.
112.	2,000 / 3,000		(111) - B	700°C / 15°C/hr.	Medium, irregular terraces with plateau. Some dendritic growth around edges of substrate.	No mask. New Ga put in and baked out at 850°C. Ga reservoir cooled with N_2 .

TABLE III

GROWTHS FROM VERTICAL CELL PROCESS

GROWTH NO.	$\mu(300^\circ K)$ / $\mu(77^\circ K)$	CARRIER TYPE/ DENSITY	SUBSTRATE ORIENTATION	SATURATION TEMP. / COOLING RATE	RESULTS AND COMMENT	CHANGES
48.			(100)	650°C / 250°C/hr.	Rectangular hillocks. Possibly due to acetone residue on substrate surface.	System cleaned in standard manner prior to first growth.
49.		n-type	(111) - B	750°C / 300°C/hr.	Sharply defined terraces and 2 plateau. Some etch-back where clamped in holder.	Iso-propyl alcohol rinse, increased cooling rate.
51.	5,300 / 11,000	4×10^{16}	(100)	750°C / 250°C/hr.	Fine terracing, one side very rough.	Boat emptied and crunch removed from melt. He heat sinked used to increase temperature gradient near substrate interface.
54.			(111) - B	750°C / 10°C/hr.	Fine and coarse terracing. Two large flaws in center. Cell contaminated due to temperature profiling.	Specimen #49 lapped off and reused as substrate.
57.			(111) - B	750°C / 50°C/hr.	Some polishing scratches visible on substrate before loading. Smooth layer with fine, even terracing.	#32 lapped, cut, and reused as substrate. Chem.-mech. lapped substrate.
58.			(100)	750°C / 50°C/hr.	Fairly smooth layer with fine terracing accentuated in centre.	Hand polished substrate on silk screen. Terminated growth at 650°C.
61.			(111) - B	750°C / 50°C/hr.	Moderate, irregular terracing.	Substrate mechanically polished on silk, no etch before growth.
64.			(111) - B	750°C / 50°C/hr.	Moderate terracing.	Chem.-mechanically polished substrate with no chemical etch during preparation.
65.			(111) - B	750°C / 50°C/hr.	Moderate terracing, very similar to #64.	
68.			(111) - A	750°C / 50°C/hr.	Irregular terraces plus many scratch-like features paralleling substrate scratches.	
70.			(111) - A	750°C / 250°C/hr.	Dense triangular hillock growth. Some lack of nucleation on substrate.	Removed considerable amount of substrate surface with long chem.-mechanical lap. Lightly etched with very dilute Br-methanol. Reduced system vibration to minimum.

TABLE III (CONT'D)

GROWTHS FROM VERTICAL CELL PROCESS

GROWTH NO.	$\mu(300^\circ K)$ / $\mu(77^\circ K)$	CARRIER TYPE/ DENSITY	SUBSTRATE ORIENTATION	SATURATION TEMP. / COOLING RATE	RESULTS AND COMMENT	CHANGES
72.			(111) - A	750°C / 50°C/hr.	Petal-like terraces. Probably due to substrate contamination during cleaning procedure.	Slower cooling rate, otherwise repeat Growth 70.
74.			(111) - A	750°C / 50°C/hr.	Irregular terracing with noticeable randomness in a single central core area.	Terminate growth at 600°C.
80.			(111) - A	750°C / 50°C/hr.	Large plateau surrounded by irregular terracing. Terracing becomes coarser towards edge.	Used chemical polish as final step (new procedure). Add additional heating coil to furnace to steepen temperature gradient in the region of the substrate interface.
110.	4,000 / 3,200		(100)	720°C / 600°C/hr.	Fine, slim, elongated terraces with slight peak at center of layer.	New Poco cell and quartz holders. System thoroughly cleaned and baked out at 800°C. Poco cell was used as received and given the above bake out.
111.	4,000 / 3,200		(111) - B	720°C / 400°C/hr.	Medium, irregular terraces with Ga inclusion pits near center of layer	Recleaned source. Repaired crack in furnace tube. Cleaned tube, baked out at 850°C. Put in new Ga and baked out at 850°C. Secondary heater stabilized temp. at 500°C when furnace was turned off.
113.			(111) - B	710°C / 900°C/hr.	Very fine, petal-like terraces surround peak at center.	Repeat of Growth 111, but furnace door opened when turned off, with secondary heater on.

14K

Figure Captions

Figure II-1. The temperature gradient cell used in the horizontal tilt system. A temperature gradient is induced, normal to the substrate, by removing the heat with He gas forced through a quartz heat transfer tube. The liquid Ga reservoir provides good thermal contact between the heat transfer tube and the cell, and improves the temperature uniformity over the plane of growth. The cell assembly is constructed from high purity graphite.

Figure II-2. The new vertical cell is constructed from high purity graphite and designed to ease the loading of the substrate, and to improve the temperature and temperature gradient uniformity. The end caps are shown partially screwed onto the cell body.

Figure II-3. GaAs substrates are shown bonded with "Carnubo" wax to a stainless steel plate for lapping and polishing procedures.

Figure II-4. Chem-mechanical polishing apparatus used for the final polishing of the substrates. A 10% "Chlorox" solution is siphoned from the beaker through a cotton wick, drop by drop, onto a rotating "Polytex Supreme" pad.

Figure II-5. (a) Growth No. 108 shows the presence of substrate preparation defects. These defects are generally not visible prior to growth. (b) Growth No. 117 shows no defects and was achieved by the outlined preparation techniques.

Figure II-6. (a) Growth No. 88 is a typical growth obtained on a (III)-B substrate without a temperature gradient to stabilize the growth interface. (b) Growth No. 105 was achieved in the temperature gradient cell. Note the absence of terraces and plateaus. The layer is extremely uniform in thickness because the liquid Ga reservoir beneath the growth area improved the temperature uniformity.

Figure II-7. (a) Growth No. 92 shows cellular growth structure that was obtained at a cooling rate of 600°C/hr with no temperature gradient. (b) Growth No. 100 dramatically shows the effect of a temperature gradient on eliminating cellular growth at a cooling rate of 700°C/hr. The irregular areas and streaks are due to stains and polishing defects introduced during substrate preparation.

Figure II-8. (a) Growth 93 shows triangular hillocks that are found on (III)-A oriented substrates when cooled rapidly without a temperature gradient. In this case the saturation temperature was 575°C and no layer formed underneath the hillocks. (b) This is a scanning electron micrograph that shows elongated hexagonal hillocks formed in between the large triangular hillocks of (a). The hexagonal hillocks may be small nuclei for the epitaxial layer.

Figure II-9. This shows a triangular hillock that is attached by a Y-shaped web to the epitaxial layer of Growth No. 83, on a (III)-A substrate. The hillock was cleaved from the layer to expose the web. Infra-red micrography shows that all triangular hillocks on (III)-A substrates are similarly attached, but not the hexagonal hillocks of fig. 8 (b).

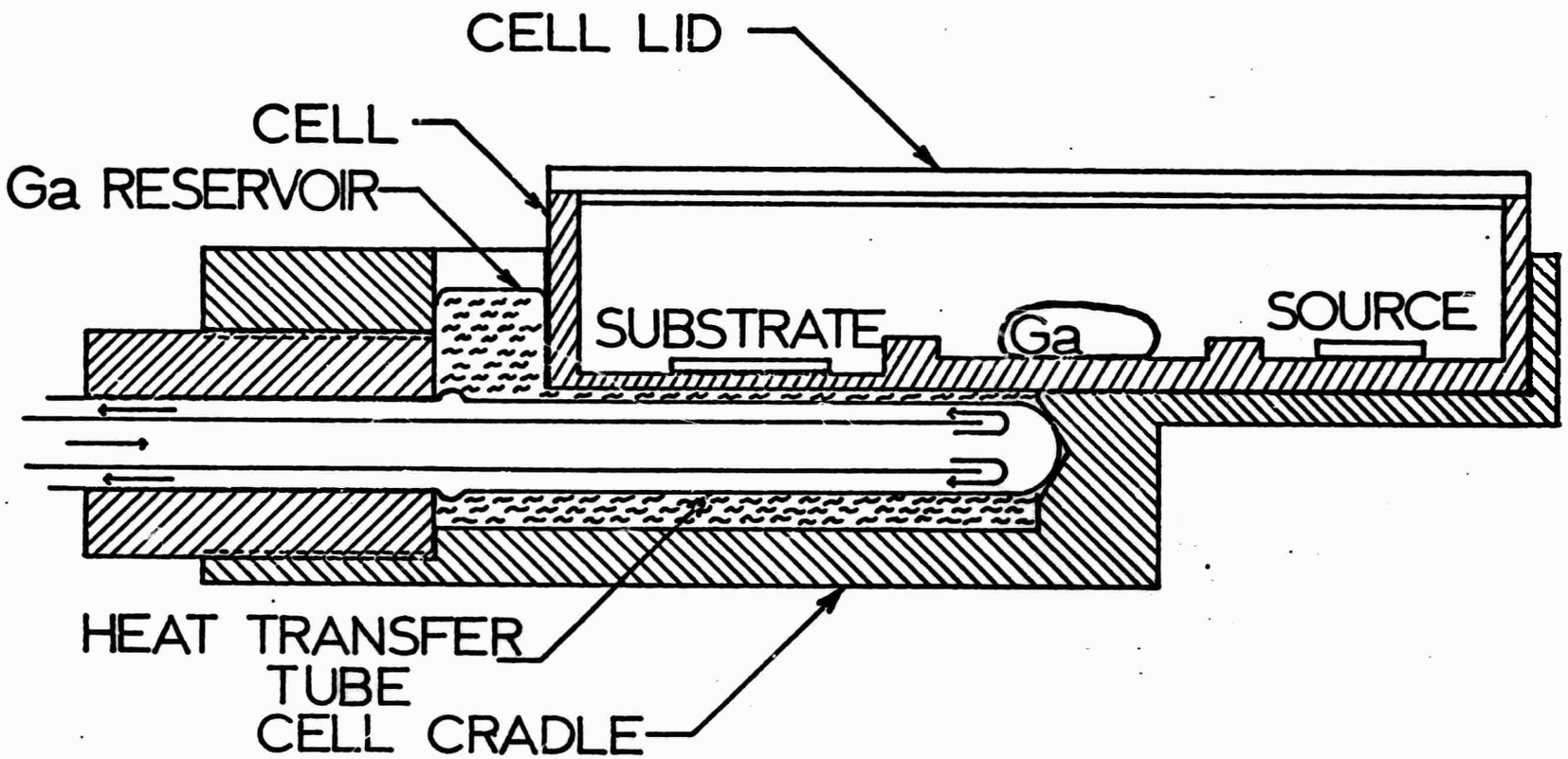
Figure II-10. Growths from the vertical cell process exhibit a slight peak at the center of the layer on both (100) and (III)-B orientations, growth Nos. 110 and 113, respectively. This peak is probably caused by a radial temperature gradient in the furnace.

Figure II-11. An extrapolation of Schottky barrier capacitance measurements to determine CO, a capacitance that arises from not only jig and lead capacitances but from edge capacitance and other shunting effects within the layer and substrate. This plot shows data from three different diodes on Growth No. 71.

Figure II-12. A Schottky barrier plot of the corrected capacitance measurements from three different diodes on Growth No. 71. The slope is proportional to the carrier density.

Figure II-13. This plot demonstrates the influence of CO on carrier density and depletion layer depth for diode No. 1 on Growth No. 71. For CO = 4.8 pf. the carrier density is in best agreement with van der Pauw measurements.

Figure II-14. This plot summarizes the variation of CO with carrier density, electrode diameter and epitaxial layer thickness (numbers beside data points, in μm). There appears to be a correlation of CO with each of these variables, in particular, large changes occur for large diameter electrodes on thin layers. This might indicate that there is considerable distortion of the depletion boundary associated with edge capacitance effects. The same effects are also shown for a few layers on n^+ substrates.



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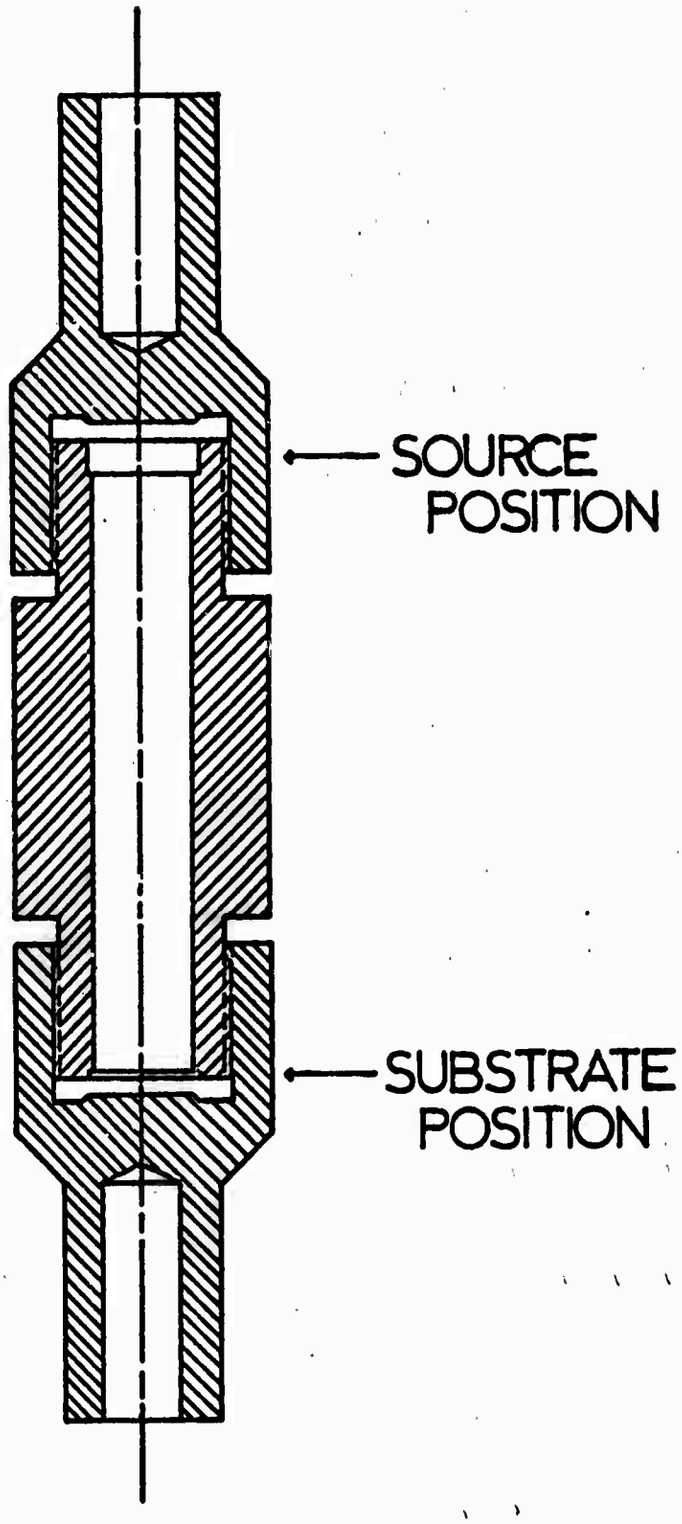

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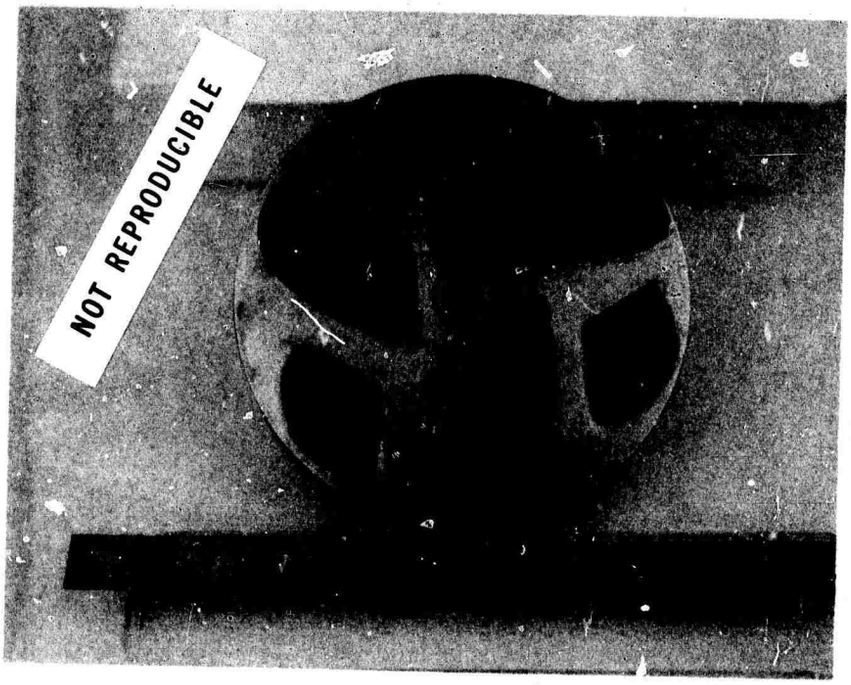

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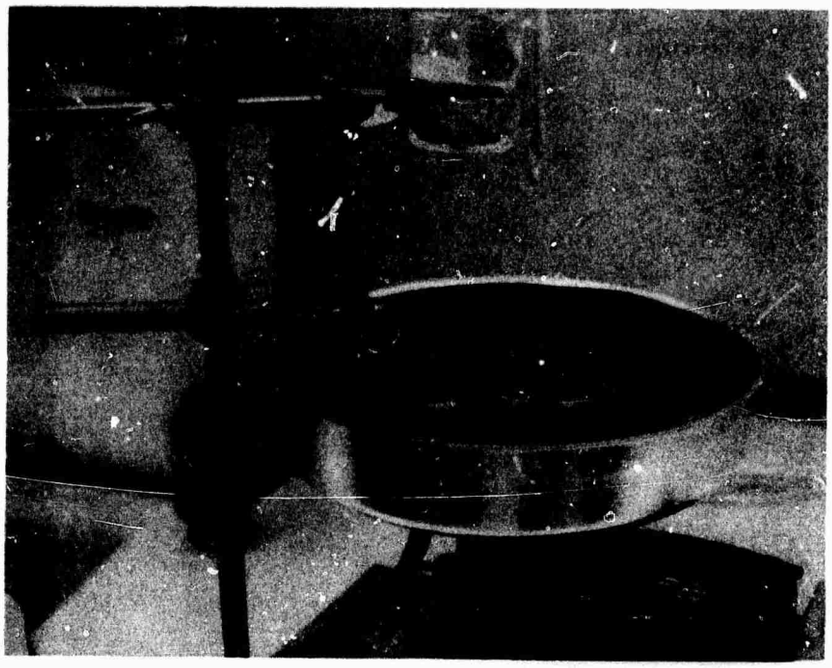

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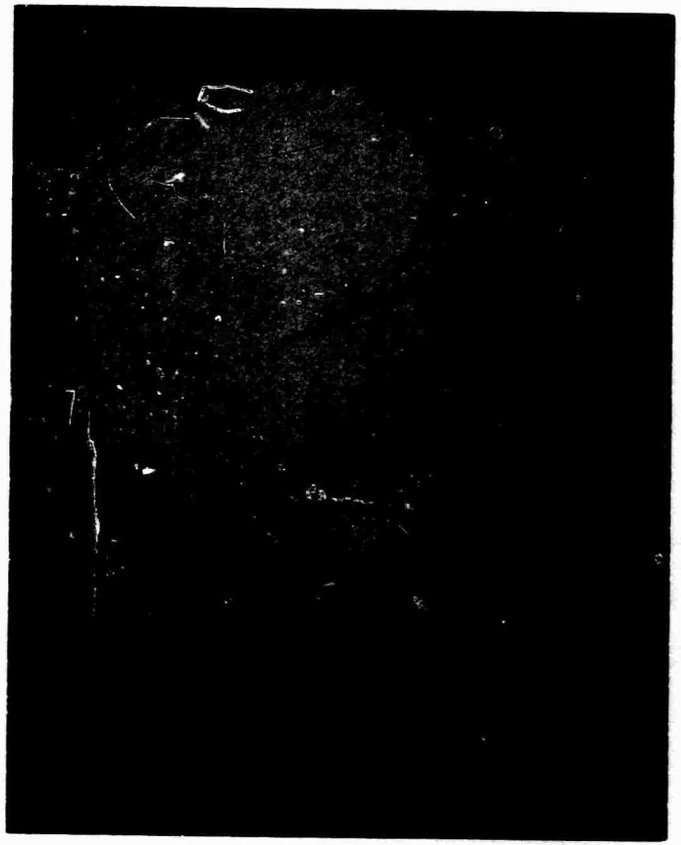

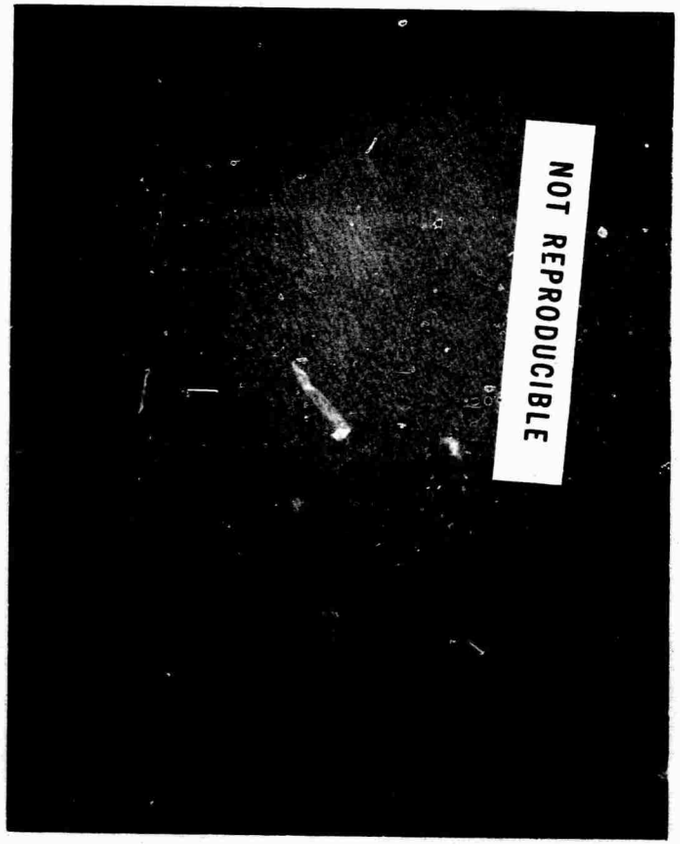

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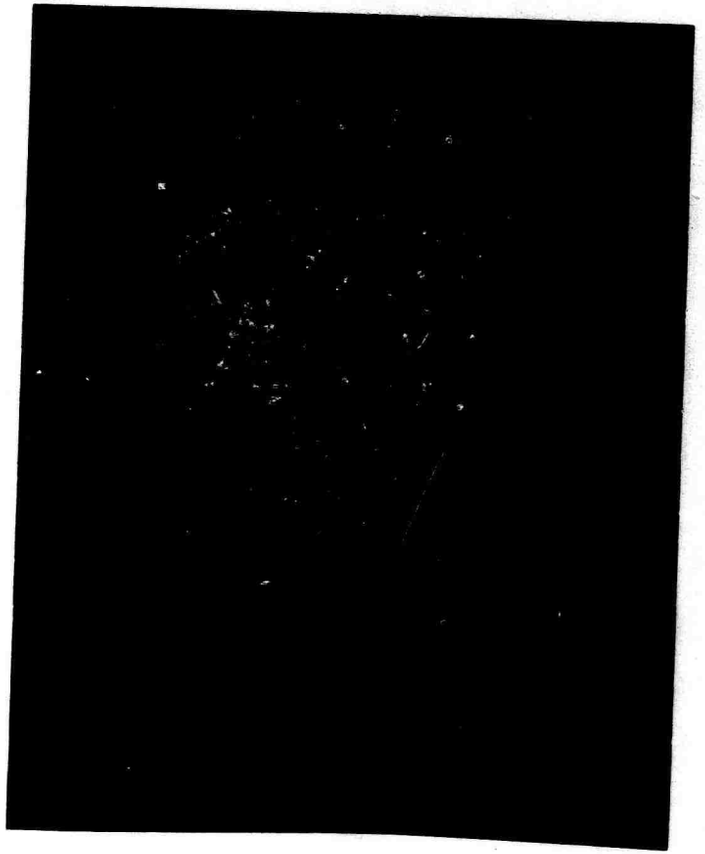

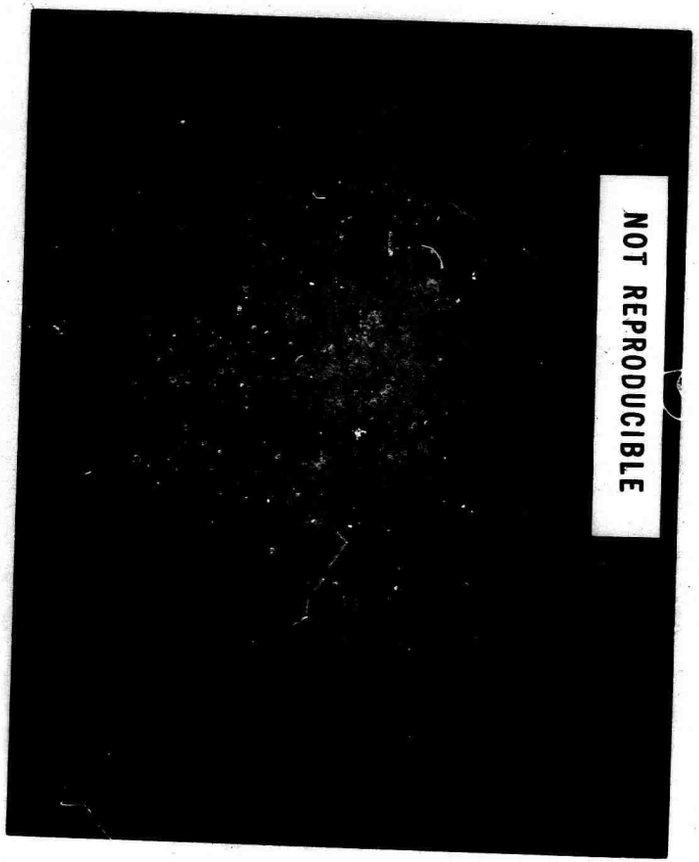

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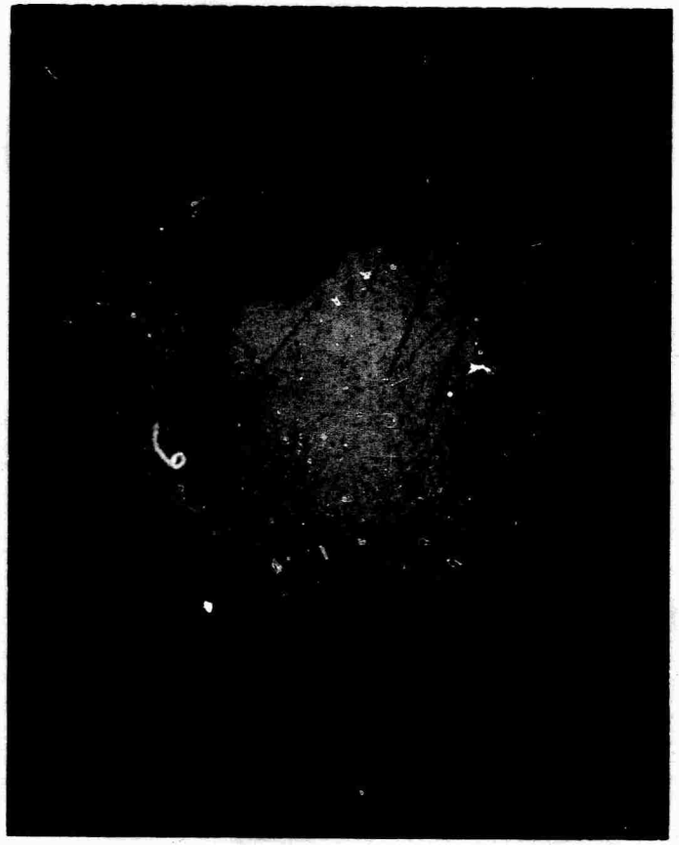

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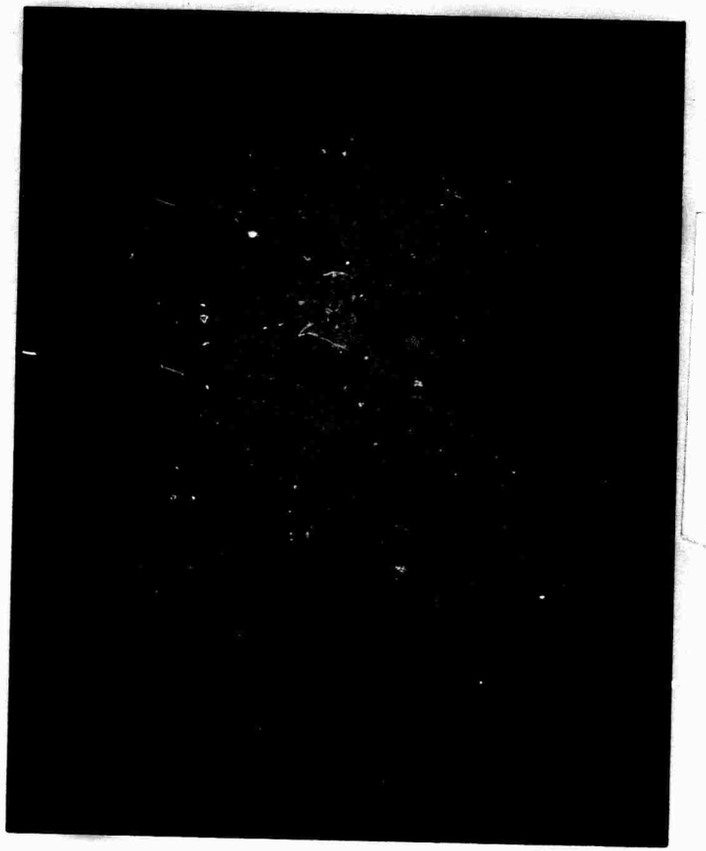

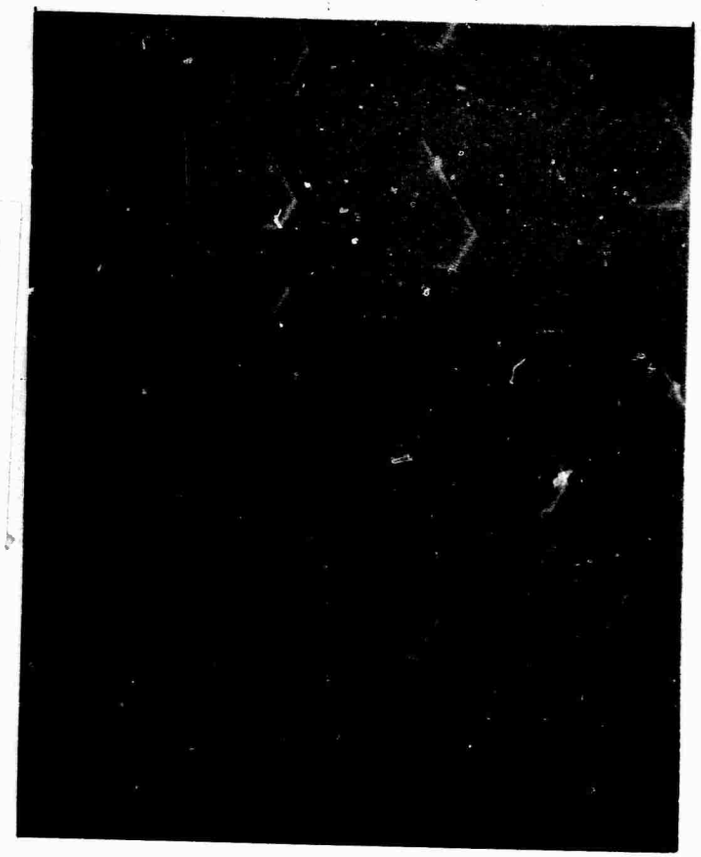

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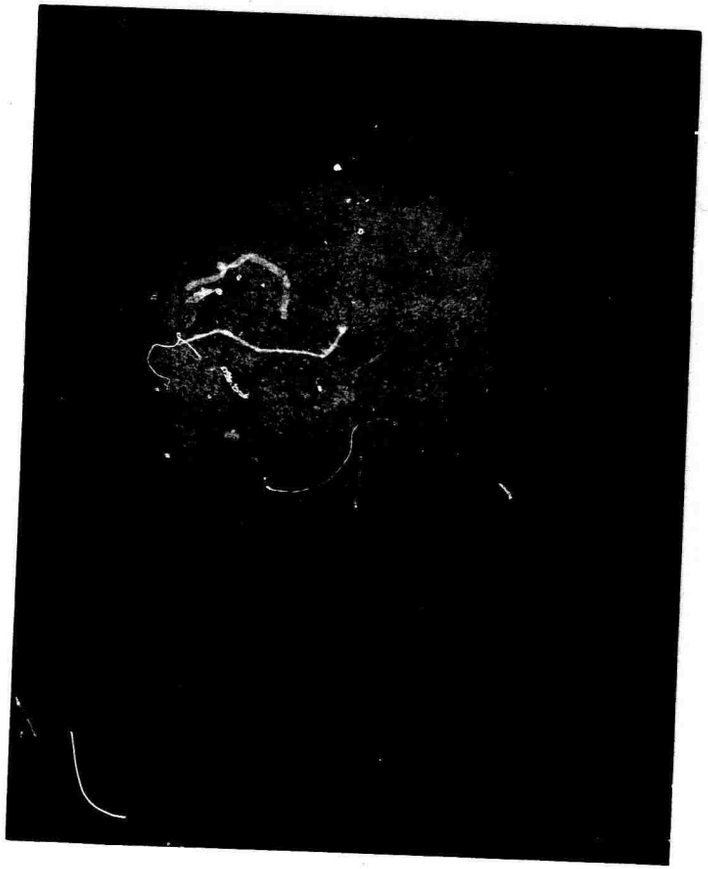

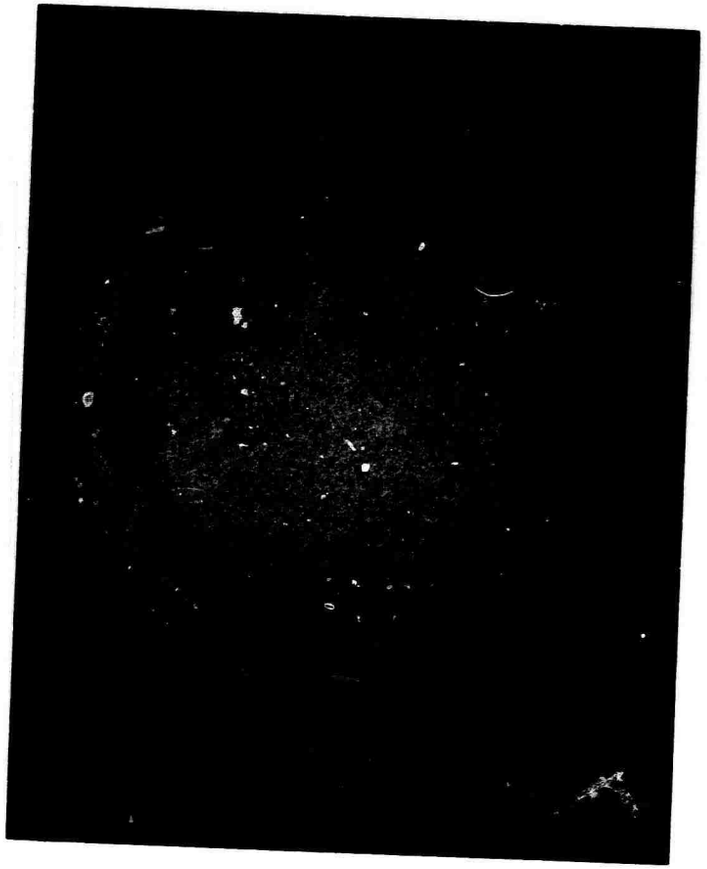

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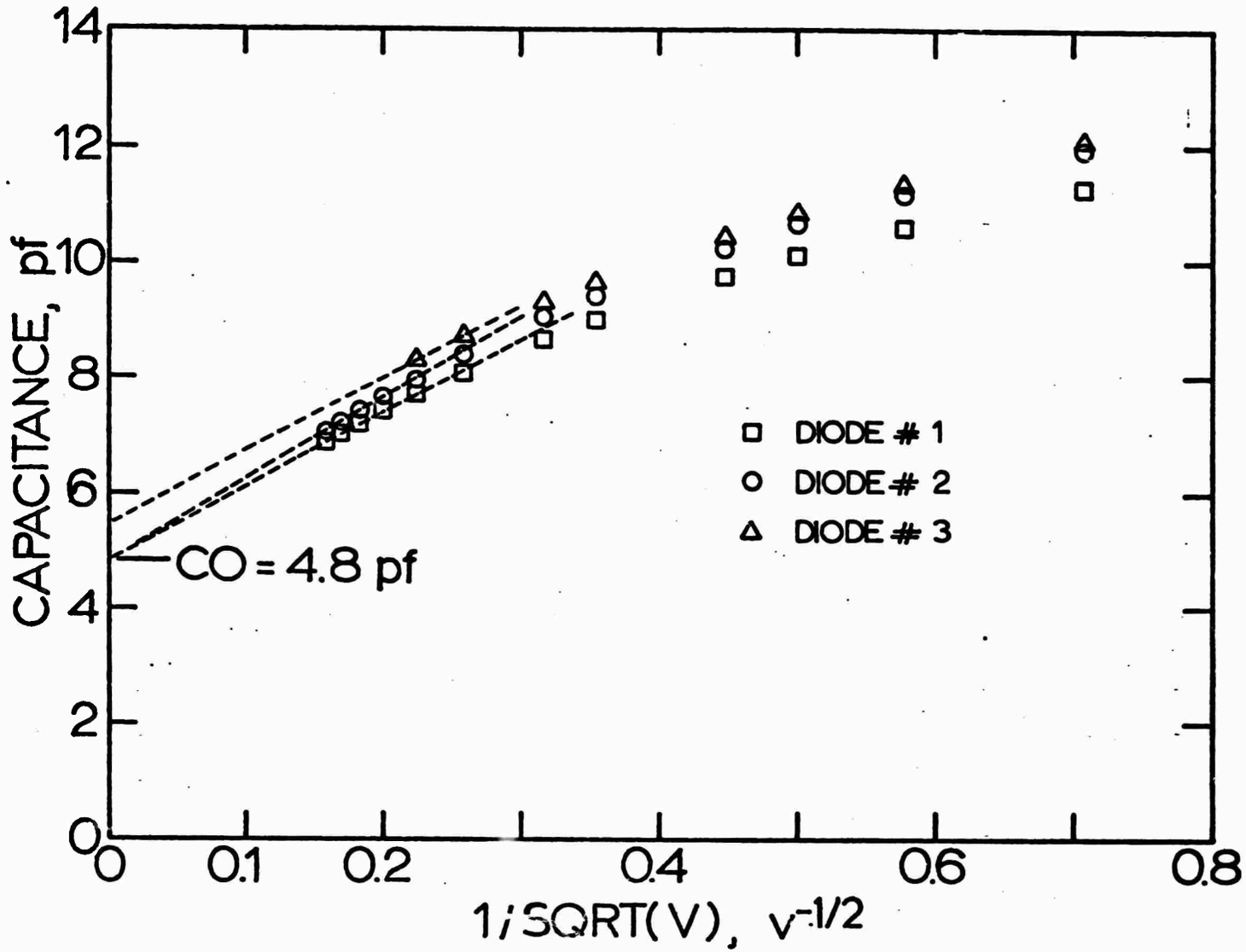

Figure II-11. An extrapolation of Schottky barrier capacitance measurements to determine CO, a capacitance that arises from not only jig and lead capacitances but from edge capacitance and other shunting effects within the layer and substrate. This plot shows data from three different diodes on Growth No. 71.

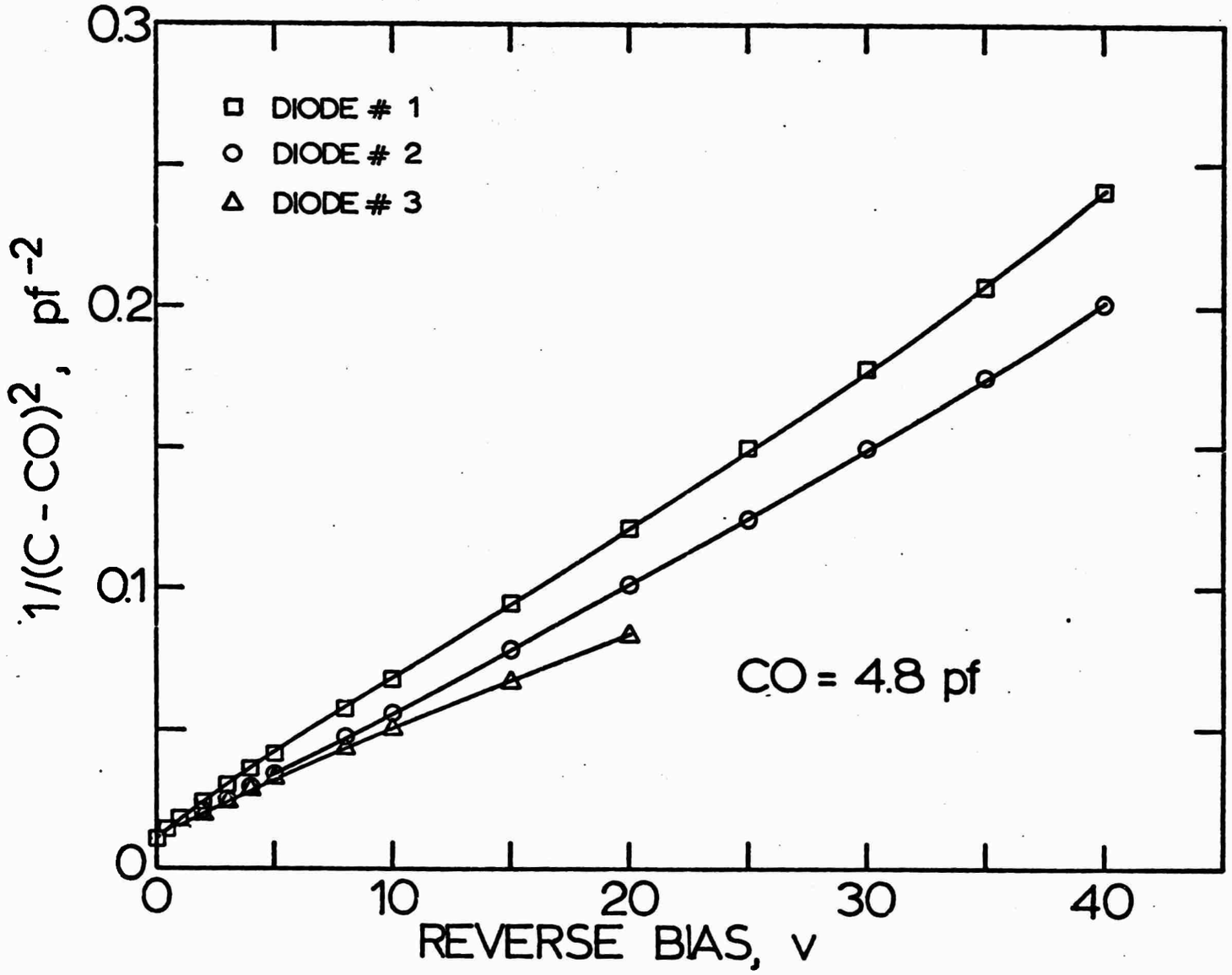

Figure II-12. A Schottky barrier plot of the corrected capacitance measurements from three different diodes on Growth No. 71. The slope is proportional to the carrier density.

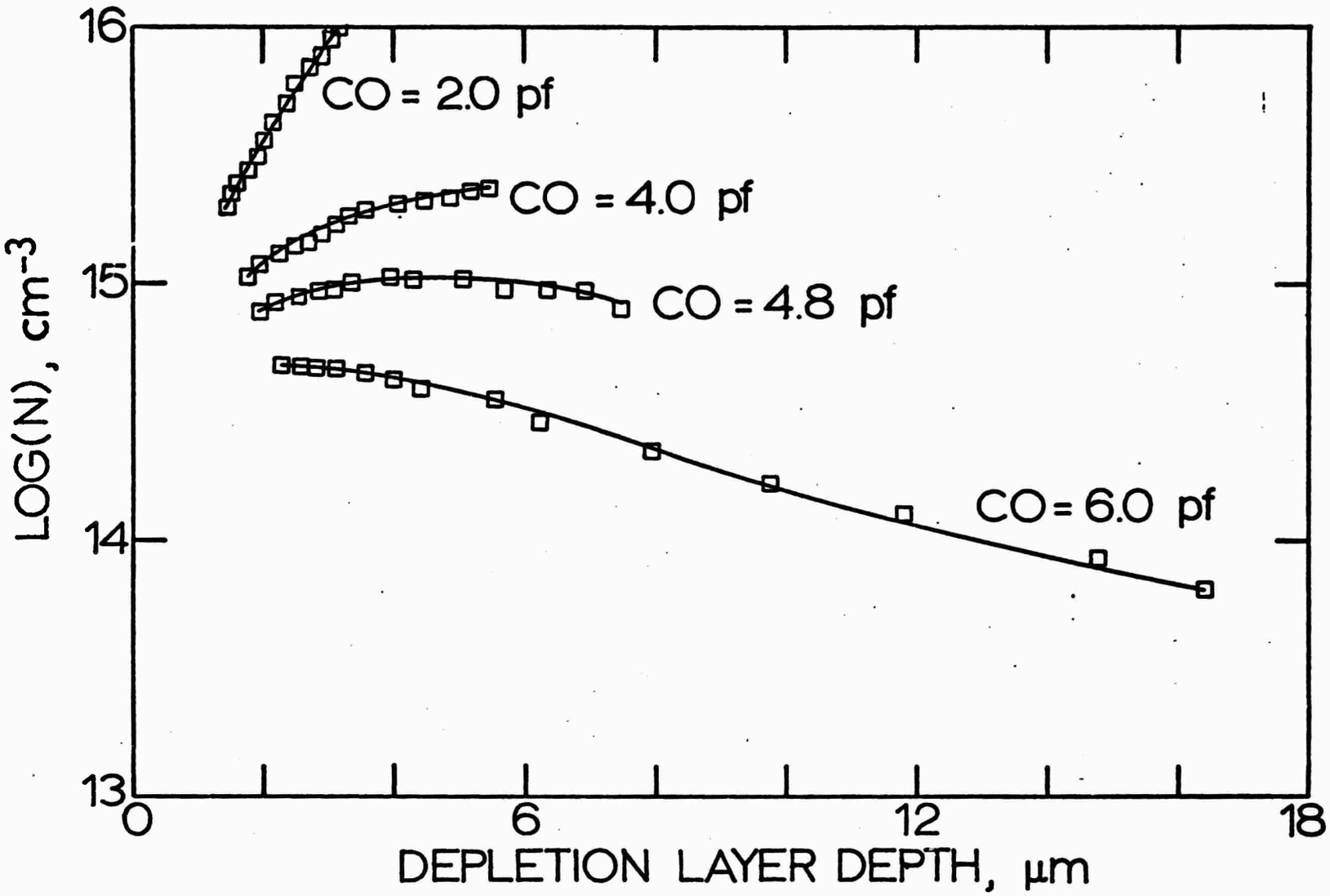

Figure II-13. This plot demonstrates the influence of CO on carrier density and depletion layer depth for diode No. 1 on Growth No. 71. For CO = 4.8 pf. the carrier density is in best agreement with van der Pauw measurements.

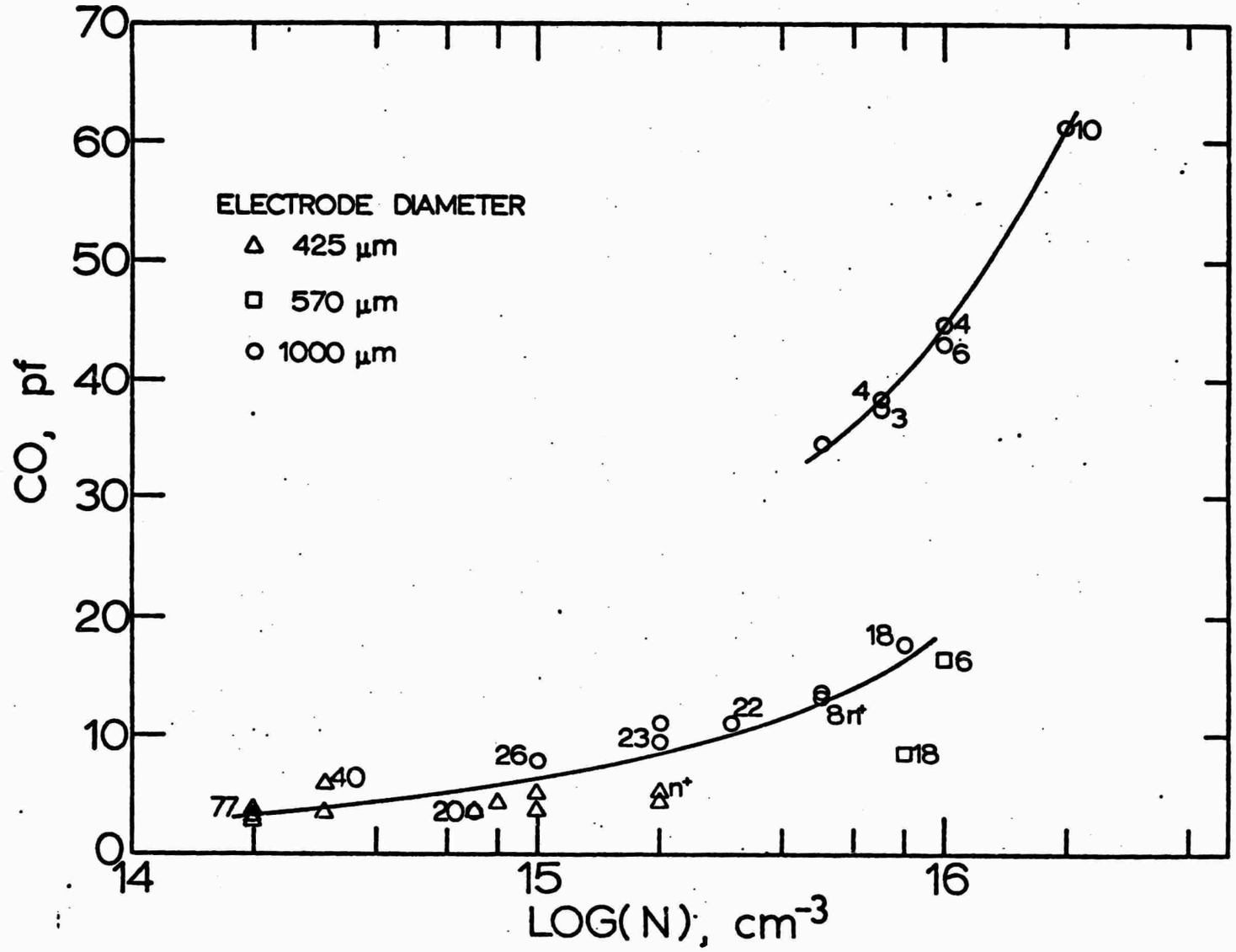

Figure II-14. This plot summarizes the variation of CO with carrier density, electrode diameter and epitaxial layer thickness (numbers beside data points, in μm). There appears to be a correlation of CO with each of these variables, in particular, large changes occur for large diameter electrodes on thin layers. This might indicate that there is considerable distortion of the depletion boundary associated with edge capacitance effects. The same effects are also shown for a few layers on n^+ substrates.

III. APPLICATIONS OF COMPOUND SEMICONDUCTOR MATERIALS

G.S. Kino, M. Bini, G.R. Bisio, S. Ludvik

A. PURPOSE OF WORK

The aim of this work is to design and fabricate planar microwave and acoustic devices from epitaxial GaAs layers. Of principal interest are a unilateral Gunn space-charge amplifier, an improved GaAs FET amplifier-transducer, and an acoustic surface wave amplifier-delay line. Being surface oriented devices, they require high quality thin films of semiconducting GaAs deposited on semi-insulating GaAs substrates. The design and fabrication of these devices requires a detailed analysis of the electric field distributions within the device configurations, and the ability to make reliable ohmic and Schottky-barrier contacts to the epitaxial material.

B. PROGRESS TO DATE

We are interested in using GaAs epitaxial layers in three kinds of devices: (1) a unilateral Gunn amplifier, (2) an improved GaAs FET amplifier, and (3) a surface acoustic wave amplifier. All three of these devices make use of epitaxial layers in the 10-30 μm range, with carrier densities typically 10^{14}-10^{15} cm^{-3} and room temperature mobilities of 6000-8000 $cm^2V^{-1}sec^{-1}$. Common to all three of these devices is the problem of obtaining both good quality ohmic and Schottky barrier or insulated-gate contacts to this material for the control of space charge. Hence our first experiments with the liquid-phase epitaxial material produced here involved the examination of contacting methods.

1. Contacts: There are certain difficulties in obtaining very thin contacts with well-controlled size on planar surface oriented devices. Liquid phase epitaxially regrown n+ contacts have proven to be unsatisfactory in this program because of the inherent problem in precisely controlling their shape and size, using masking and chemical etching techniques. We have therefore concentrated on alloyed contacts. Most of our work has been devoted to the study of Au-Ge contacts which have been fairly satisfactory in the past, providing the alloying time is kept short and the surface of the GaAs is kept extremely clean before contacting. The process involves the evaporation of a Au-Ge alloy onto the GaAs surface with subsequent short alloying times of the order of 30 seconds to 1 minute. Originally, the samples were chemically cleaned, coated with the Au-Ge in a vacuum chamber, and then alloyed in a hydrogen furnace. This method has the disadvantage that chemical cleaning tends to be imperfect and oxidation could occur before the samples were annealed. Alternatively, if alloying were carried out within the vacuum chamber, it would be difficult to keep the alloying time short enough because of the difficulty in rapidly cooling the substrate. We have therefore reconstructed the vacuum chamber with the following modifications: (1) provisions to rf sputter-clean the sample in a pure Argon atmosphere, (2) a provision for rapidly cooling the substrate holder with cold water, and (3) instrumentation to obtain good temperature control of the substrate at any time. With the new vacuum system, we were able to obtain satisfactory contacts, as measured by the shape of the I-V characteristic, on material with a carrier density of $5 \times 10^{14} cm^{-3}$.

A second fabrication problem arose from surface terraces for the material grown by liquid phase epitaxy. We were concerned about the effect of the terraces on masking and with the quality of the contacts. However, during the year the surface finish was improved, and the depth of terracing became negligible. Polishing techniques have also been developed that enable us to use material with coarse terraces and achieve high quality surfaces.

2. GaAs Unilateral Gunn Amplfier and FET Amplifier: The configuration of the GaAs unilateral amplifier is shown in fig. III-1. The amplifier is essentially an FET transistor. The gate gives control of the dc operation of the device and acts as a shield for the rf signal, reducing the direct coupling between input and output. The preparation of the samples is done by an integrated circuit technique that we developed in our laboratory for this purpose. The procedure we follow consists of three basic steps: a high vacuum deposition of a Au-Ge layer for making ohmic contacts to the material; the deposition of an insulating layer of SiO_2 by a sputtering process; and the vacuum deposition of an Al layer to form the gate. At each step, the pattern of the layer is properly shaped by depositing photoresist on top, exposing it through a mask and selectively etching away the unwanted materials. Using this FET configuration, we have made up to 50 Gunn amplifiers at a time from material of the order of 15 μm thick, with diode lengths varying between 20 μm and 100 μm, and gate lengths 8 μm shorter than the diode length between contacts. The samples were tested by looking at the shape of the I-V characteristic. Their behavior was satisfactory - fairly linear at low voltages, then saturating and breaking into oscillations at higher voltages. Initially, there

had been some concern about a possible depletion of the GaAs near the insulating substrate because of electrons from the semiconductor going into traps in the insulating material. We had therefore chosen to use material somewhat thicker physically than we expected it to be electrically. As it turned out, the quality of the liquid epitaxial material used appears to be better than we had expected so that the electrical and physical thicknesses are comparable as far as we can tell. Consequently, the diodes did not operate properly as amplifiers. Instead most of them oscillated as Gunn oscillators, an unsatisfactory situation from the point of view of a device application.

With improved technology we have constructed diodes of reduced thickness to supress the Gunn oscillations. Extensive tests on these devices has led to the conclusion that the simple theory used in the design of the amplifier in which the dc field is assumed to be uniform with the semiconductor is not adequate. Typically, the amplifiers we constructed either exhibited net loss or tended to break into oscillation. We have therefore been carrying out extensive theoretical studies to understand the detailed nature of the dc field distribution in these amplifiers and the effect of this field distribution on the gain. We feel that we now understand the dc and rf behavior much better and are in a position to redesign the amplifiers to obtain net gain. In the dc field theory, we worked on a basis of two possible extreme assumptions: (i) very high surface state density, such that the dc field component normal to the region where mobile carriers are present near the surface is nearly zero, i.e., there is a depletion layer present between the surface charge layer and the bulk; (ii) absence of surface states.

The conclusions of these studies can be summarized as follows:

Case (I)

In a semiconductor which exhibits negative differential mobility the dc electric field is nonuniform, and when biased above threshold ($V > \ell E_t$) there can be regions where the dc electric field is below threshold and the differential mobility is positive. These regions of low electric field are located near the cathode and their extension depends both on the value of the dc electric field at the cathode and the current density. Therefore a calculation of the total gain of an rf space charge wave based on the assumption of a uniform dc field is not necessarily accurate. Using a purely analytic approach, we took into account the nonuniform dc bias conditions and derived a simple expression for the total gain in terms of only the current density and the input and output carrier wave velocities. From this expression it became clear that for a unilateral carrier wave amplifier biased above threshold the input signal must be injected at a point where the carrier drift velocity is larger than the dc velocity at the output of the diode. This implies that the dc charge density at the input must be smaller than the dc charge density at the output. Hence, if a signal is injected just at the cathode, where the dc charge density can be assumed to be infinite, there must be net loss. In practice, however, the electric field goes above threshold a short distance from the cathode, and the injection of the carrier wave can be over a comparatively wide region or at a point sufficiently far from the cathode to have gain.

Figure III-2 shows curves of the gain vs. the bias voltage for different

lengths of the sample, assuming that the input signal is excited just where the dc field goes above the threshold. These curves are based on a model of a semiconductor of infinite cross section. It can be demonstrated, however, that it is a good approximation to assume that with finite cross section the gain is reduced by a constant factor but retains the same dependence on the bias voltage. It is apparent from fig. III-2, that if a sample is oscillating it is practically impossible to quench the oscillations by changing the bias voltage and still have some gain. Thus some modification of the cathode condition is required for optimum performance.

Case (II)

In the region under the gate the electric field can only be above the threshold a very short distance near the anode end of the gate. A qualitative picture of the electric field distribution along the sample is given in fig.-III-3. It is apparent that, without modifying the gate region by using a semiconductor or insulator of wedge-shaped rather than uniform thickness, it is not possible to obtain gain with the normal gate lengths.

This model, without surface states, predicts a sensible modulation of the dc current by the gate voltage. So far we have seen neglible modulation of the current in our experiments. Coupled with the information that is available on the number of surface states in GaAs ($> 10^{13}(eV)^{-1}cm^{-2}$) it is therefore fairly certain that the dc behavior depends mainly on the surface states, and not on the potential of the gate. This conclusion suggests that we use another approach, for example a Schottky barrier gate, instead of an insulated gate to achieve control on the dc behavior. If we put a Schottky barrier gate

a few microns long in front of the cathode, we can expect to vary the longitudinal dc electric field at the cathode by varying the potential of the gate. More precisely we expect to be able to keep the longitudinal dc electric field at the entrance of the gate (cathode side) below threshold and the dc electric field at the output of the gate just above threshold. Under these conditions, if we inject a carrier wave at the input to the gate we can achieve large gain without suffering domain oscillations, for the thermal noise which gives rise to domains is now generated in a positive differential mobility region.

We are now constructing a computer program to give a two dimensional solution of Poisson's equation and the equation of motion of the carriers. This will enable us to obtain a precise picture of the field distribution in the semiconductor. The program, which is based on techniques that we developed in the past for electron guns, is being designed to take into account the velocity-field characteristic of GaAs in the range above threshold. Its use should make it possible to carry out an accurate design of GaAs FET's which operate in the region where the field over part of the device is above threshold.

3. Acoustic Surface Wave Amplifiers and Delay Lines

In this project we are concerned with acoustic wave propagation and the interaction of these waves with carriers drifting in n-type epitaxial layers of GaAs. This type of surface oriented configuration is of particular importance in acoustic amplifiers and delay lines, where the fine transducer geometries required for high frequency operation can be fairly readily obtained using photomasking techniques. The use of GaAs in these devices is motivated by a combination of two of its properties - high room temperature mobility and

piezoelectric properties. The high mobility is desirable since it means that large acoustic gains can be achieved at relatively low electric fields, producing a device with a long delay and only a small dc input power requirement.

The epitaxial layers used for this study have carrier concentrations ranging from 10^{14} to 10^{15} cm^{-3} and thickness of about 10 μm. The carrier density limits arise at the lower end because of the difficulty in making good ohmic contacts, and at the upper end because the frequency of maximum acoustic gain exceeds present transducer capabilities. Here, the acoustic wave is propagated along the ⟨110⟩ direction on (001) oriented substrates. For this direction, it is possible to obtain a 3 μs/μm delay using a form of the Rayleigh surface wave which can be excited by a longitudinal electric field.

In the Semi-Annual Technical Report, some initial experiments were described in which it was shown that surface waves could be generated and detected by means of a novel type of transducer which is essentially an FET structure. The emphasis of our work since then has been in refining the geometry of the transducers to increase their frequency range. Some advance has also been made in improving the conversion loss of the detecting transducer. By operating it in a two terminal mode where the detecting region is biased near the Gunn threshold field (3 KV/cm), the acoustic signal appears as a modulation of the current between the two contacts, bringing out an interesting new phenomenon associated with the acousto-electric interaction at high fields.

The basic transducer used for generating acoustic waves consists of a three terminal structure, in which the two outer contacts (source/drain) are ohmic while the center contact (gate) is a Schottky barrier, fig. III-4. The

configuration is like that of a conventional FET except that the spacing between the contacts is comparable with the acoustic wavelength. The acoustic signal is excited by applying an rf signal at the gate contact. Figure III-4 shows such a transducer with a 1μm wide gate contact; this dimension is about 1/6th of the corresponding length of the previous device. Several of these transducers are spaced along a conducting channel which has been etched on the epitaxial layer. Construction of the devices involves the following three stages: (1) Source/drain contacts; (2) Etching of conducting channel; and (3) Gate contact. For obtaining the metal film pattern required in both step (1) and (3), the process employs a photoresist mask over which the metal film is evaporated. The desired configuration is then produced by lifting the photomask. An alternative procedure has been tried using an etching method, where the metal film is evaporated first and than the photomask is used to protect the desired pattern while the remaining film is etched away. We have found however that the lifting technique generally provides a better-defined metal pattern.

The ohmic contact material employed here is an alloy of Ag-In-Ge (90:5:5% by weight) which is evaporated as a mixture, and after the patterns have been obtained, is then alloyed for about 5 minutes, at 500°C, in an H_2 atmosphere. For carrier concentrations in the mid $10^{14}cm^{-3}$ region, this alloy was found to produce more consistent ohmic contacts than the other commonly used material, Au-Ge (88-12%), which often produces a rectifying contact. Both of these methods have been reported in the literature but there appears to be no consensus on their suitability for low $10^{14}cm^{-3}$ epitaxial material. Although, at concentrations in excess of about $10^{15}cm^{-3}$, the Au-Ge alloy is usually satis-

factory. One possible disadvantage of the Ag-In-Ge alloy is the diffusion of In into t e epitaxial layer, either by a long term aging effect or else under the influence of high electric fields. This feature has so far not been a problem with the device behavior. The Schottky barrier gate contact is made from Al which is a particularly convenient material because of its good adhesive properties in the photomasking process. The channel on the epitaxial layer is etched before overlaying the gate in order to remove the active layer from underneath the gate contacting pad avoiding excess input capacitance. A typical current-voltage characteristic for the FET transducer is shown in fig. III-5. The dc transconductance is about 0.2 mA/V and is consistent with the low carrier concentration of the epitaxial layer. We find a difference between the pulsed and dc characteristics for this type of structure, the pulsed transconductance being greater. This difference has been noted by other investigators and has been attributed to the formation of a depletion region at the interface between the layer and the semi-insulating substrate. Variations in this depletion region become apparent only near dc conditions, where the charging currents must flow through the high resistance substrate.

Preliminary results of acoustic wave propagation in these devices have been obtained and the operating frequency has been found to extend to the 130-250 MHz range. Some frequency dependence has been observed, however the main geometrical factors producing this behavior have not yet been isolated.

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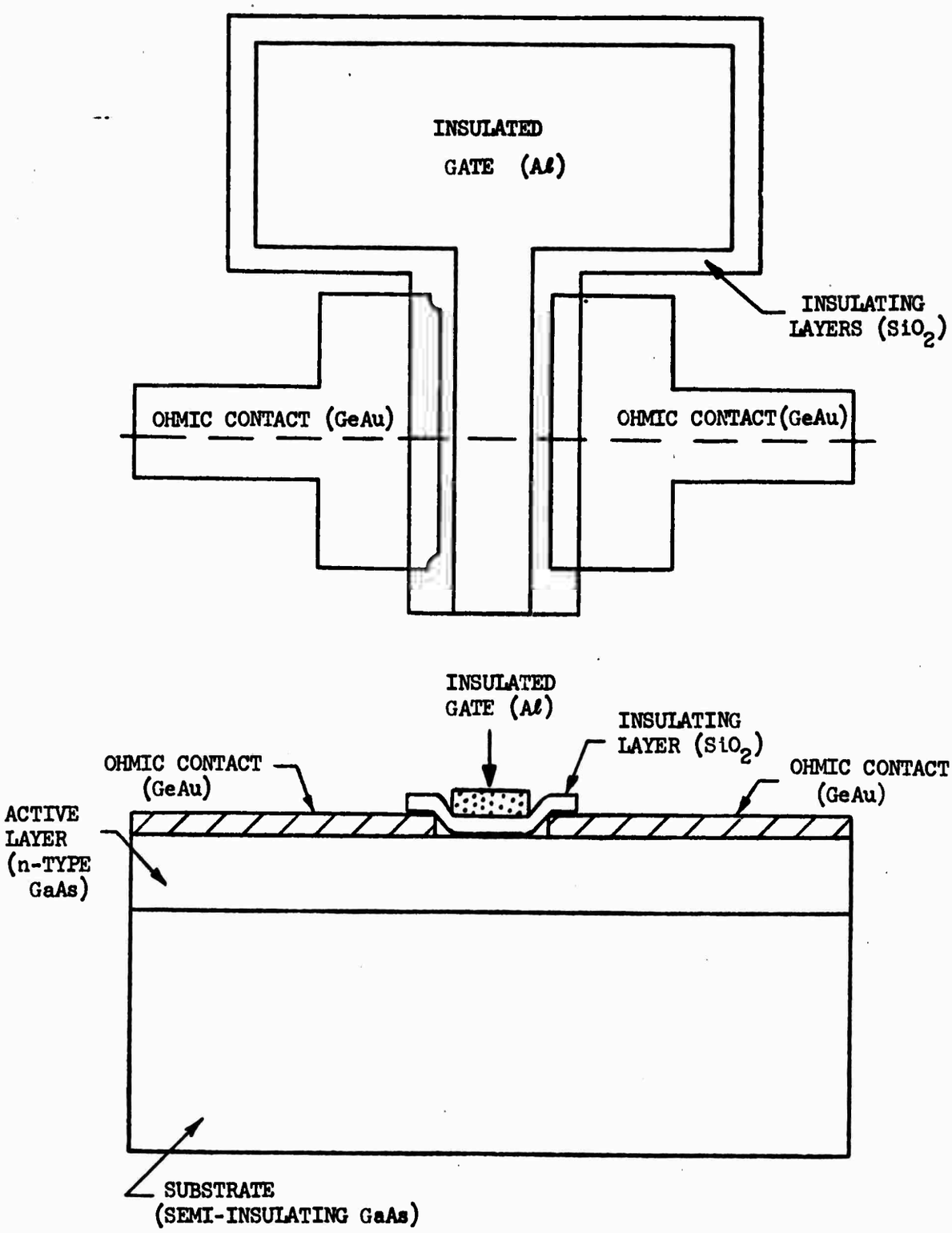

Figure III-1. Schematic diagram of a typical FET Gunn amplifier. Essentially similar configurations are used for both the unilateral amplifier and the more conventional FET amplifier.

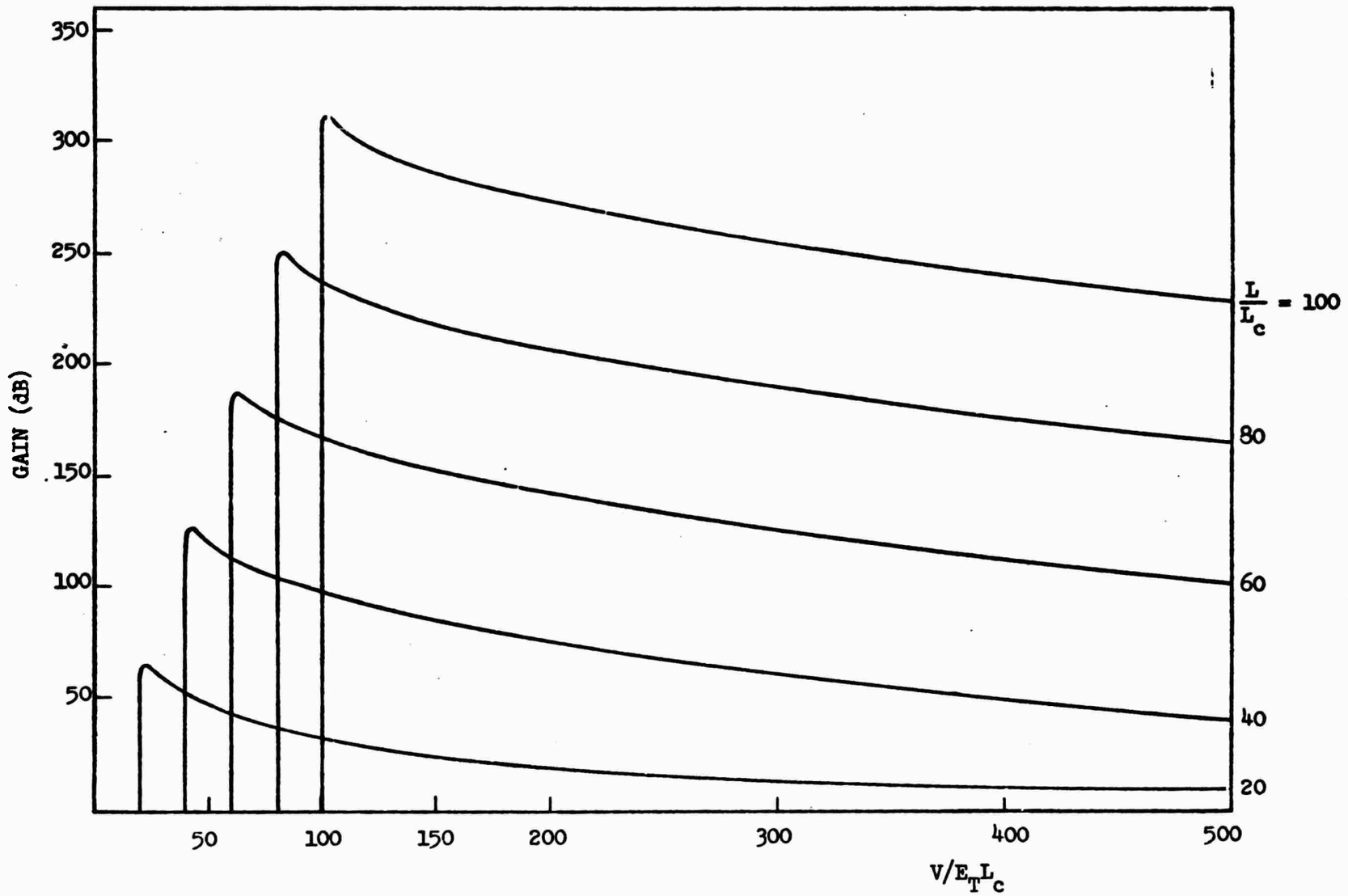

Figure III-2. Gain vs applied voltage for various sample lengths. The voltage is normalized to the threshold field E_t and to the characteristic length $L_c = \epsilon E_t/\rho d$. The rf signal is supposed to be injected at the point where the dc electric field reaches E_t .

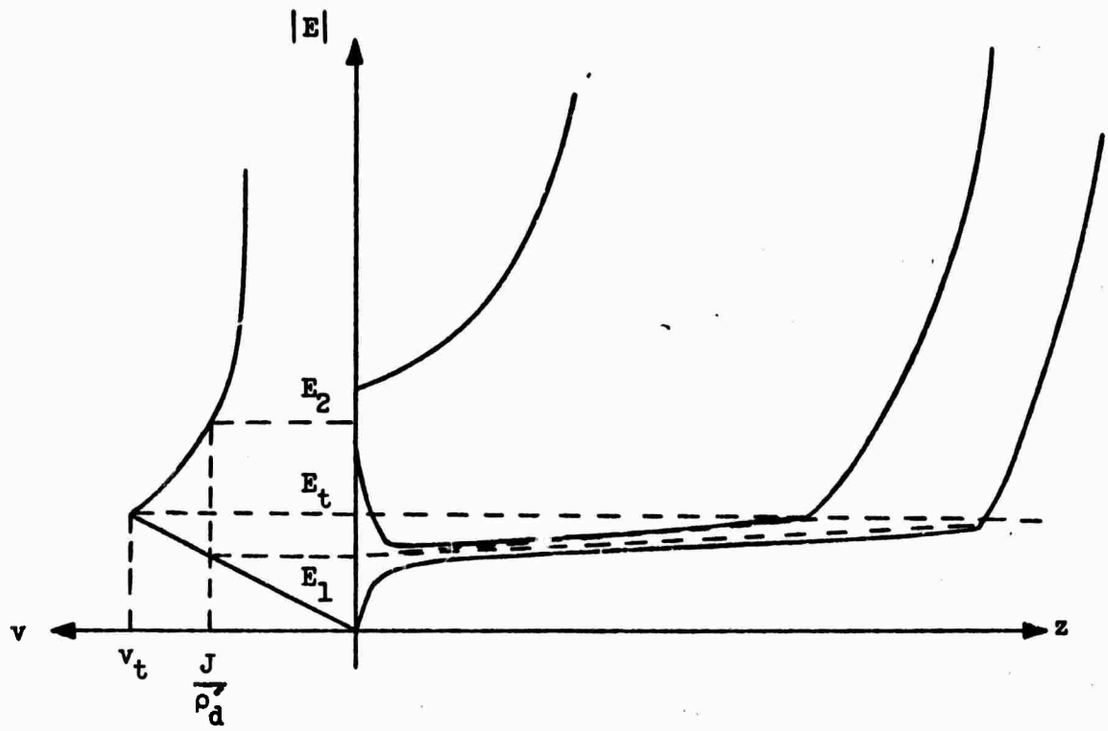

Figure III-3. Qualitative behavior of the longitudinal electric field [E] vs distance z in a sample without surface states, biased above threshold for different values of [E] at z = 0 . The diagram at the left gives the dependence of the electron mean velocity v vs the electric field in GaAs.

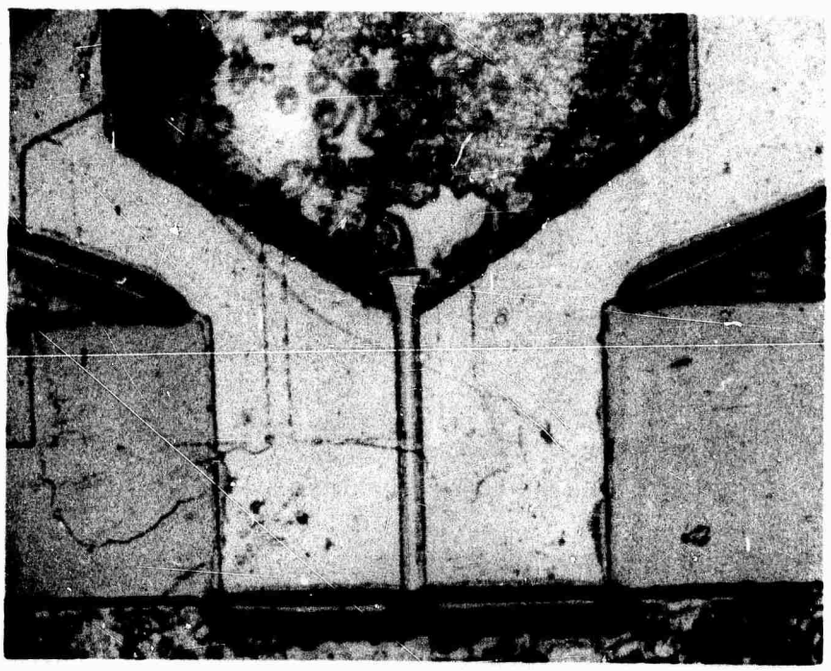

Figure III-4. FET transducer. The outer contacts are ohmic and the central electrode is a Shottky barrier.

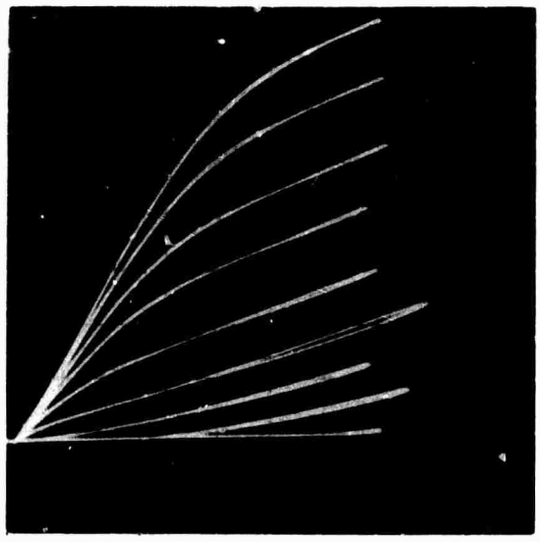

Figure III-5. Current voltage characteristics for FET transducer. Layer thickness: 6 μm; $N_D = 5.3 \times 10^{14}$ cm^{-3}; $\mu = 7300$ cm^2/V sec. Vertical scale = 0.2mA/div. Horizontal scale = 1V/div.

IV. RELATIONS BETWEEN DISLOCATIONS AND MECHANICAL PROPERTIES AND THE PRODUCTION AND CHARACTERIZATION OF DEFECT STRUCTURES IN COMPOUND SEMICONDUCTORS

R. H. Bube, W. D. Nix, B. Liebert, and A. L. Lin

A. EFFECT OF MECHANICAL DEFORMATION ON ELECTRONIC PROPERTIES OF UNDOPED n-TYPE GaAs

An experimental program of research is in progress to study the effects of dislocations and dislocation arrays produced by plastic bending at high temperatures on the electronic properties of undoped n-type GaAs. In the past year most of our effort has been devoted to the construction of an apparatus for heating and bending GaAs single crystals. Since other studies have shown that heat treatment alone can have profound effects on the electronic properties of GaAs,[1-4] it was concluded that the bending process should involve as little time at temperature as possible. For this reason our crystals are resistance heated directly. Since subsequent annealing seems desirable (to straighten the dislocation arrays) the effects of annealing at high temperatures will be studied. A preliminary experiment along these lines has been carried out and is reported below.

The ability to achieve a constant and uniform temperature during the bending process was one of our main concerns initially. Eight chromel-alumel thermocouples were used to check the temperature variation of the bending and control samples. The results indicate a $\pm$ 10°C variation in temperature along the length of the sample in the center region when the crystal is held at temperatures between 500 and 600°C. This small variation should be of little consequence in our bending experiments. The sample rests on two graphite blocks which act as heat sinks. Consequently the ends of the sample are considerably cooler compared to the central region. However the center of the sample, between the two knife edges, is the region of interest since this is where the dislocation density is expected to be uniform.

The temperature of the control sample is somewhat cooler than the sample to be bent. However due to the short times for heating, bending, and cooling and the fact that these samples will be annealed subsequently, this temperature difference should not be important.

As indicated above, previous studies indicate that heat treatment alone can produce large changes in the electrical properties of GaAs. Therefore, in our work it is necessary to separate the effects of annealing from those of bending.

In an attempt to determine the order of magnitude change in resistivity due to annealing, a sample was enclosed in a quartz ampoule along with crushed GaAs and placed in a furnace at 980°C for 63 hours. During the heat treatment the sample decreased in weight by 9% apparently due to evaporation. Because of the high arsenic vapor pressure, it is expected that heating in an evacuated tube will produce excess As vacancies, especially near the crystal surface. If As vacancies act as acceptors, as suggested by others[1], the resistivity of our crystals may be expected to increase during annealing. Other authors have suggested that heat treatment of GaAs introduces Cu impurities which act as acceptors.

Subsequent measurements on the sample direct from the furnace did in fact show an increase in resistivity of almost two orders of magnitude (from 0.03 to 2.6 ohm-cm). The sample was then mechanically ground to remove about 500 microns from all surfaces. If the increase in the resistivity was due primarily to arsenic vacancies near the surface then the resistivity of the subsurface region should be unaffected by heat treatment. The resistivity of the interior region did show the expected decrease, (down to 1.87 ohm-cm), however not down to the preanneal level of 0.03 ohm-cm. Further research is needed before the As vacancy/Cu impurity question can be settled.

The dislocation configurations produced by bending, are also being studied. Preliminary work has shown that the x-ray absorbtion coefficient of GaAs is too high to use the Lang x-ray topographic technique as originally proposed. The dislocation configurations can, however, be imaged with Borrmann x-ray topography. This technique will be supplemented with infrared microscopy and standard etch pitting techniques. The etch pitting method has been used to determine the polarity of the crystals and the nature of dislocations in bent crystals[5].

B. EFFECT OF MECHANICAL DEFORMATION ON ELECTRONIC PROPERTIES OF SEMI-INSULATING GaAs:Cr

Preliminary experiments were performed to test the effects of mechanical deformation on the electronic properties of semi-insulating GaAs:Cr crystals. The technique of deformation used is simple 4-point bending. Three samples were prepared: (1) as-grown, (2) control sample that passes through the same heating as the bent sample, and (3) the sample to be mechanically deformed.

A 4-point bending apparatus was used which was constructed entirely of quartz to minimize the possibility of contamination by metallic impurities. The initial temperature chosen for bending was 700°C, since the most uniformly distributed dislocation arrays were reported for deformation carried out at a very slow rate and relatively high temperature.[6] After initial tests to check the effect of various loads, the sample to be deformed, Sample (3), was bent in argon with 1.2 Kg for 20 min, after a 10-min pre-heating to temperature. The control sample, Sample (2), was placed adjacent to the sample being bent. The distance between the bending points was 0.85 cm, and the distance between the supports was 1.6 cm.

After mechanically polishing and chemically polishing, all three samples were cleaned in reagent grade trichloroethylene, acetone, distilled water, and methyl alcohol. Ohmic indium contacts were applied by alloying in H_2 at 375°C.

The following kinds of measurement were made for each of these three samples: (a) spectral response of photoconductivity at 300° and 77°K; (b) dark conductivity vs. temperature; (c) photoconductivity excited by white light vs. temperature; (d) thermally stimulated conductivity. Results are summarized graphically in Figures 1 and 2.

In Figure 1, the short wavelength (high energy) peaks correspond to the intrinsic photoconductivity; the position of this peak shifts from 0.87 to 0.82 micron with a decrease in temperature from 300° to 77°K because of the temperature dependence of the bandgap. The long wavelength (low energy) peaks and the onset of photoconductivity between 1.6 and 2.0 microns corresponds to extrinsic photoconductivity.

From the data of Figures 1 and 2, it appears as if the effects of bending were to partly compensate for changes induced in the sample by heating alone. Only the dark conductivity (e.g., at 300°K: Sample (1) - 1.9×10^{-9} $(\text{ohm-cm})^{-1}$; Sample (2) - 1.6×10^{-8} $(\text{ohm-cm})^{-1}$; Sample (3) - 3.3×10^{-8} $(\text{ohm-cm})^{-1}$)shows an additional effect of bending in the same direction as the effect caused by heat treatment alone. On the other hand, the magnitude of the extrinsic photoconductivity peak and the behavior of the photoconductivity vs. T both show that the bent sample lies intermediate between the as-grown and control samples.

Some of the questions raised by the change in dark conductivity above are the following. Since it is expected that heat treatment of GaAs will produce acceptor defects, why does the conductivity increase in an n-type sample such as we have? After etching the (111) face of the bending sample, we find that the bending should have created excess Ga-like dislocations; since this kind of dislocation is also an acceptor, again the problem of the dark conductivity change arises. More detailed Hall and thermoelectric measurements on the samples is expected to shed some light on the appropriate interpretation.

Another approach is to minimize the effects of heat treatment alone by carrying out the deformation at as low a temperature as possible. By changing the distance between the supports from 1.6 to 2.0 cm, keeping the distance between bending points of 0.85 cm, we found it possible to bend a sample at 580°C with a load of 1.4 Kg in 1 hr, producing a radius of curvature of about 3.8 cm. Bending at this lower temperature will be investigated.

Since 1960, many people have tried to solve the problem of heat treatment induced changes in GaAs.[3,4,7] One group believes that arsenic vacancy acceptors are generated by heating GaAs over 800°C for a short time, these acceptors being formed within 1-10 microns of the surface for a heating time of 15 min. A second group believes that the acceptor induced by heat treatment is due primarily to the movement of Cu impurities from dislocations or from the surfaces; subsequent annealing permits the Cu impurities to diffuse back to the dislocations. This kind of heat-treatment effect can be eliminated by etching the surface after heat treatment and/or by

annealing the sample after heating. We are investigating the effects of these treatments now in order to define better the reference conditions for the bending effects. The fact that our heat-treatment effects are in the opposite direction to these acceptor-producing hypotheses also suggests that we may be dealing with a precipitation of the Cr acceptors in the GaAs.

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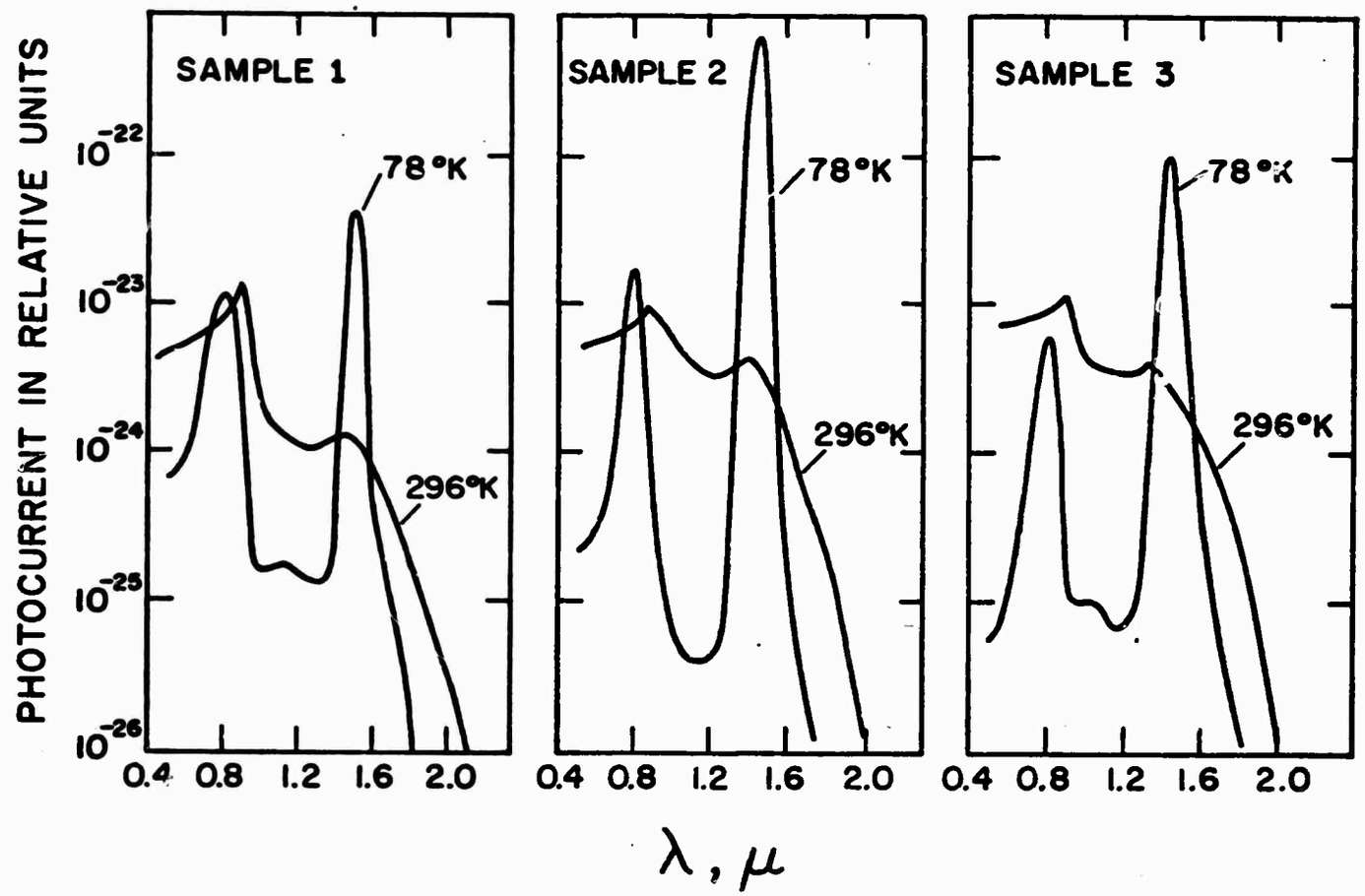

Figure IV-1. Spectral response curves at 296°K and 78°K for sample 1 (the as-grown sample), sample 2 (the control sample), and sample 3 (the bent sample).

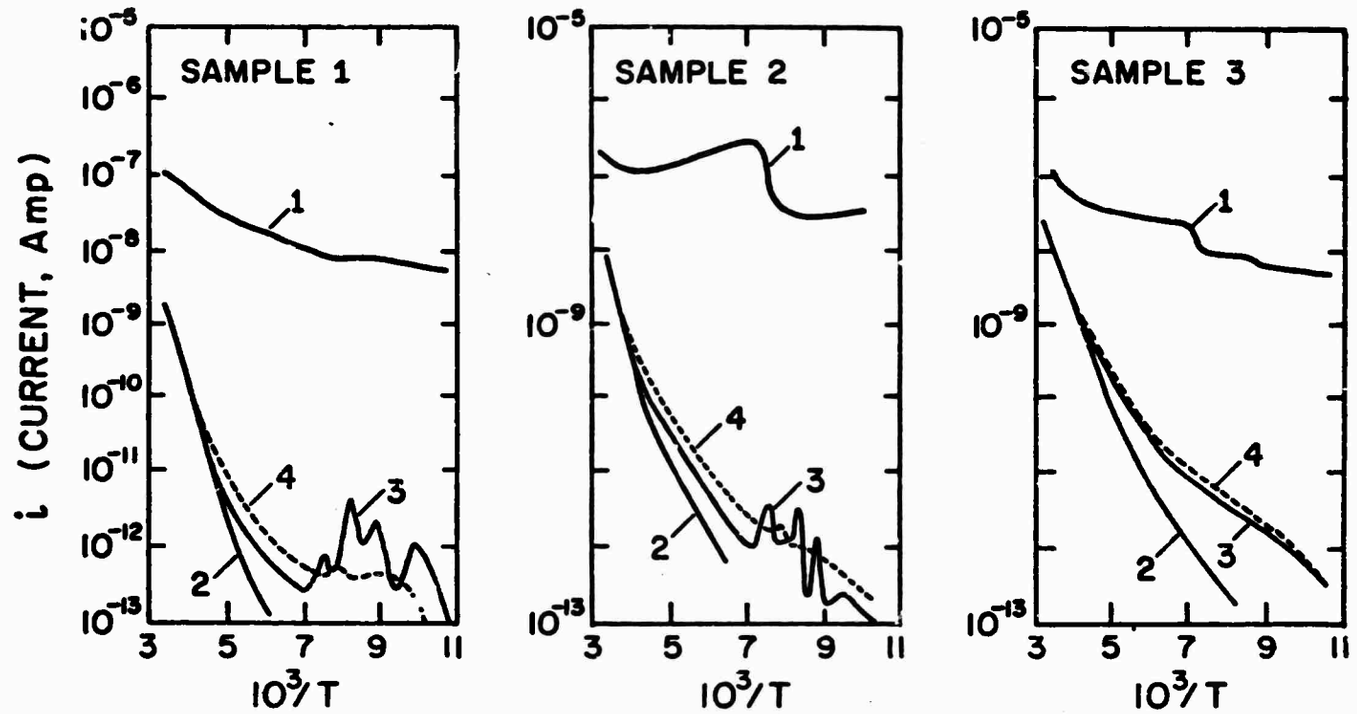

Figure IV-2. 1-Photocurrent (with white light) v.s. temperature; 2-Dark current v.s. temperature; 3-Thermally stimulated current (excitation at low temperature only) v.s. temperature; 4-Thermally stimulated current (excitation during cooling) v.s. temperature.

V. ANNEALING AND PRECIPITATION STUDIES IN COMPOUND SEMICONDUCTORS

D. A. Stevenson, W. D. Callister and W. C. Rhines

The present research program concerns the influence of post growth annealing upon the properties of compound semiconductors. Two topics have been studied: the influence of component pressure on the equilibrium concentration of electrically active defects; the mechanism of precipitation in compound semiconductors and the influence of precipitation upon physical properties. A brief description of research progress is given below.

A. THE POINT DEFECT STRUCTURE OF SOME II-VI COMPOUNDS

The high temperature defect equilibria in CdTe, ZnTe, and CdSe have been investigated by measuring the electrical transport properties at equilibrium conditions. Measurements were performed as functions of temperature and component pressure on undoped CdTe and CdSe, Al-doped ZnTe, as well as Cu- and In-doped CdSe; all specimens were single crystals.

For undoped CdTe in Cd-rich atmospheres and at temperatures between 620 and 802°C, the electron concentration varies as $P_{Cd}^{1/3}$, from which it is concluded that the dominant electrically active defects are doubly ionized native donors, either Cd interstitials or Te vacancies.

The conductivity type of ZnTe was changed from p to low resistivity n between 700 and 925°C and in Zn-rich atmospheres by the addition of 6×10^{18} cm^{-3} Al donors. A two-carrier treatment of the transport measurements yielded

$$n \propto P_{Zn}^{+0.4} .$$

It is concluded that the impurity donors are totally compensated by doubly ionized native acceptors, possibly Zn vacancies, based upon the following: 1) the Zn pressure dependence of the concentration of the charge carriers, 2) the magnitude of the concentration of the charge carriers, and 3) the value of the native acceptor incorporation constant.

The electron concentration for undoped CdSe varies as

$$n \propto P_{Cd}^{1/3}$$

at temperatures between 650 and 850°C and in Cd-rich vapors. This

behavior is interpreted on the basis of the dominance of doubly ionized donors, either Cd interstitials or Se vacancies; the incorporation energy of this defect was found to be 1.90 eV.

B. OBSERVATION OF PRECIPITATES INDUCED IN GaAs BY Zn DIFFUSION

Several investigators have reported lattice damage and precipitation caused by the inward diffusion of Zn into GaAs.[1-7] In most cases the evidence is indirect, i.e. the attack by etchants on diffused zones of the observed infrared absorption is considerably larger than that generated by Zn free carrier absorption[4]. Efforts to resolve the precipitates in single crystals of GaAs with x-ray topography, electron microprobe analysis, and optical and infrared microscopy have failed. Black and Jungbluth, however, were able to coarsen the precipitate to a size of about 10 μm by using polycrystalline GaAs and extended diffusion times[5]. This technique revealed grain boundary precipitates whose identity could be determined only as "Zn-rich".

In our current work, we have produced precipitates by Zn diffusion into single crystals of GaAs, and have observed them in foils by transmission electron microscopy. Wafers of n-type, (100), undoped GaAs, 10X4X1 mm^3, with carrier concentrations of $7.50 \times 10^{14} cm^{-3}$, mobilities of 6170 $cm^2/V \cdot sec$, and dislocation densities of $2.50 \times 10^3 cm^{-2}$, were mechanically polished, cleaned in a series of organic solvents, polished with 1% Br in methanol, and rinsed in doubly distilled water. Each wafer was placed at one end of a quartz ampoule containing 1.4 mg/cc of 99.999% Zn evacuated to 10^{-6} torr, and sealed. After diffusion annealing at 810°C for 70 hours the ampoule was quenched to room temperature within 15 seconds. Discs were ultrasonically cut from the wafers and then thinned using a modified jet polisher with 0.5% Br in methanol.

Both diffusion annealed samples and control samples, taken from the same boule but without the diffusion treatment, were examined in the electron microscope, with comparative results shown in Figures 1 and 2. As noted, there is no evidence of precipitation in the control sample, whereas definite evidence of precipitation is present in the annealed sample.

The precipitates range in size up to 0.1 μm with an average spacing of 1 μm. The precipitates appear to have a high electron density compared to the GaAs matrix, as indicated by their dark appearance. Examination by tilting the specimen stage at various angles showed no evidence of strain fields around the precipitates. The precipitates appear to be multi-faceted and, have clearly acquired a uniform Widmanstätten orientation from the GaAs matrix. Dislocations appear to terminate on precipitate particles in many cases. A cross section of the diffusion front after etching shows a definite band, typical of reaction diffusion phenomena. In summary, the following significant observations were made on the precipitation induced by Zn diffusion: 1) the precipitates have a definite morphology, 2) they exhibit a Widmanstätten structure, 3) dislocations often terminate on the particles, and 4) there is a clearly defined reaction front in the region in which precipitates form.

Observation of precipitates of this size and distribution gives further evidence for the Black and Jungbluth hypothesis that such precipitates are responsible for the anomalously high infrared absorption of Zn-doped GaAs If the precipitates are opaque to infrared, or even if their index of refraction differs from that of GaAs, one would expect their near 1 μm spacing to cause significant infrared attenuation.

V-1. C. H. Ting, Tech. Rep. No. 511-2, Stanford Electronics Laboratories, August 1968, p. 31.

V-2. J. F. Black and E. D. Jungbluth, J. Electrochem. Soc. 114, 181 (1967).

V-3. J. F. Black and E. D. Jungbluth, J. Electrochem. Soc. 114, 188 (1967).

V-4. J. F. Black and E. D. Jungbluth, J. Electrochem. Soc. 114, 297 (1967).

V-5. J. F. Black, J. Electrochem. Soc. 114, 1292 (1967).

V-6. M. Maruyama, Jap. J. Appl. Phys. 7, 476 (1968).

V-7 M. S. Abrahams and C. J. Buiocchi, J. Appl. Phys. 37, 1973 (1966).

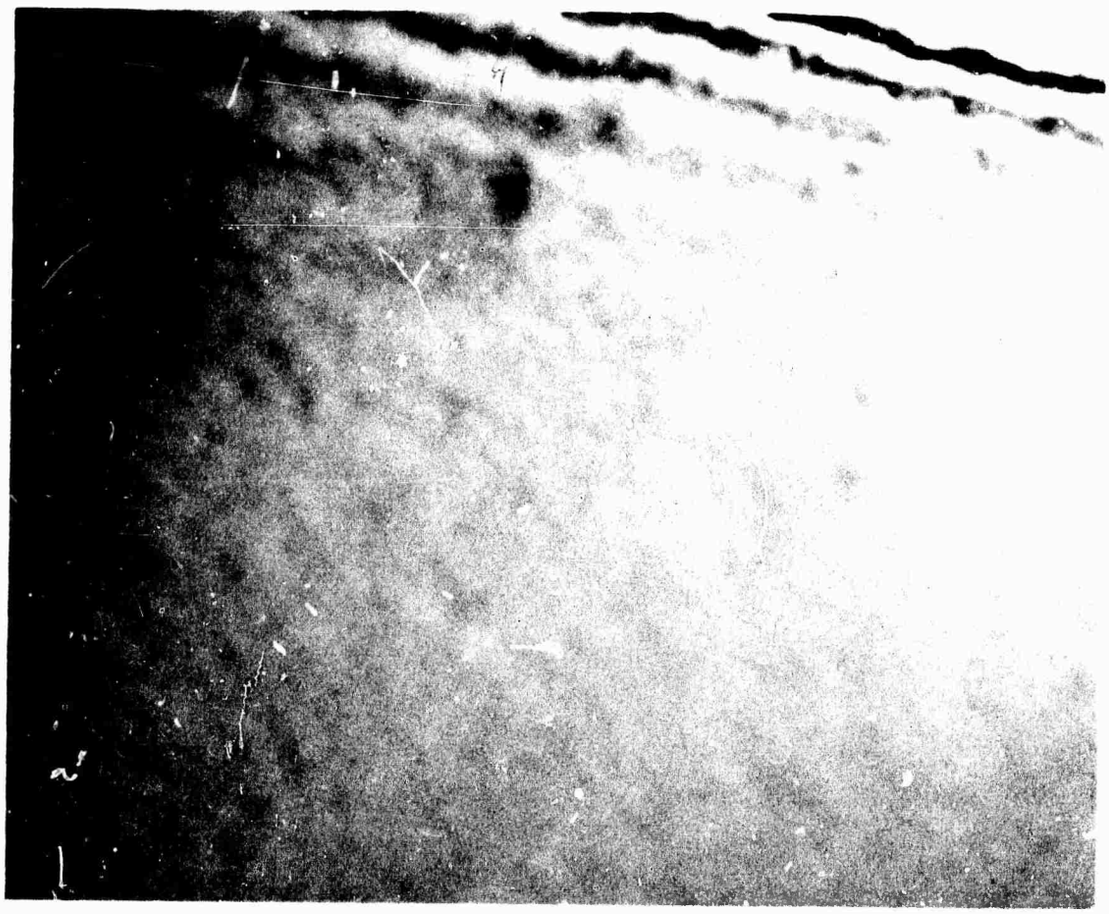

Figure V-1. GaAs, undoped, n-type, (100), 87,000x

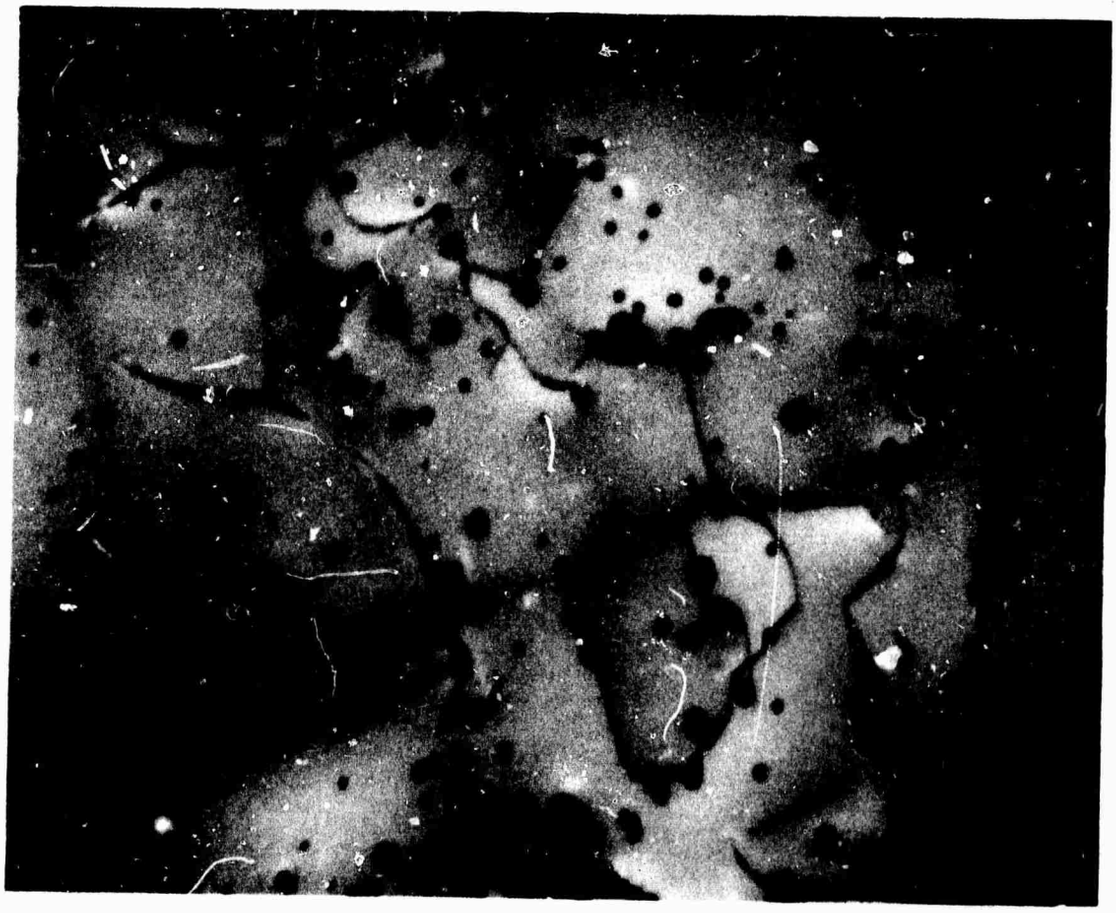

Figure V-2. GaAs, (100), Zn doped, 800°C, 70 hrs., 87,000x.

VI. INTERFACIAL PHENOMENA AT THE SOLID-LIQUID INTERFACE IN THE Ga-As SYSTEM: CALCULATION OF THE SOLID-LIQUID INTERFACIAL ENERGY IN THE Ga-As SYSTEM. QUASI-CHEMICAL CONTRIBUTION OF THE PLANAR PERFECT INTERFACE.

W. A. Tiller, B. Jindal and Hyo-Sup Kim

The objective of this investigation is to develop an understanding of the important interfacial parameters which govern the growth of GaAs crystals. The study includes the structure and energetics of GaAs solid-Ga-As liquid solution interface as a function of the (a) orientation of the solid GaAs and (b) concentration of the liquid phase. The basic approach is to determine separately the following contributions: (a) quasi-chemical terms, (b) interface adsorption and (c) electrostatic terms.

Previously, we investigated the nature of the interaction energies between the atoms in the Ga-As system. Suitable functions had been determined that describe the interatomic interactions in this system. Next, we have gone on to determine the quasi-chemical terms.

The quasi-chemical terms refer to the excess bond energies associated with the creation of solid-liquid bonds at the interface compared to solid-solid and liquid-liquid bonds in the bulk phases. These terms are a major contribution to the total interfacial energy. For this reason, the interfacial energy can usually be approximated by the quasi-chemical term alone. In the Ga-As system, however, other contributions could be expected to be important because of the differences in the nature of the atomic interactions and the atomic and electronic structures of the two phases.

To calculate the quasi-chemical terms, the formal broken bond method has been applied. The quasi-chemical term can be expressed as

$$E_{quasichem} = \sum_i n_{SL,i} \cdot \epsilon_{SL,i} - \frac{1}{2}\left\{ \sum_i n_{SS,i} \cdot \epsilon_{SS,i} + \sum_i n_{LL,i}\, \epsilon_{LL,i} \right\}$$

where

$n_{SL,i}$ = bond density of ith nearest neighbors of solid-liquid interaction at the interface.

$n_{SS,i}$ = bond density of ith nearest neighbors in bulk solid phase.

$n_{LL,i}$ = bond density of ith nearest neighbors in bulk liquid phase.

$\epsilon_{SL,i}$ = bond energy (or interaction energy) of ith nearest neighbors of solid-liquid interaction at the interface.

$\epsilon_{SS,i}$ = bond energy of ith nearest neighbors in bulk solid phase.

$\epsilon_{LL,i}$ = bond energy of ith nearest neighbors in bulk liquid phase.

The bond energies were calculated by using the interatomic potential functions determined previously. The bond densities have been calculated by examining the structures of the crystal and liquid.

A quasi-lattice model has been employed for the structure of the liquid phase, which was assumed to be uniform density and uniform solute concentration. The solid-liquid interaction energies have been calculated by applying the Fowke's summation method of plane sheet model. To do this, at first, a general summation form for the interphase interaction energy was derived in terms of the parameters of the Morse potential function. All the calculations of the interaction energies in the bulk phases and the phase to phase have been included up to the eighth nearest neighbors interactions.

The calculated values of the quasi-chemical terms of GaAs crystal-50%Ga-50%As liquid solution at the melting point of GaAs crystals are given as follows:

(Crystal Orientations)

	(100)	(110)	(111A)	(111B)
$E_{quasichem}$	1488 (erg/cm^2)	1058 (erg/cm^2)	828 (erg/cm^2)	939 (erg/cm^2)