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FINAL REPORT

PART II

ANALYSIS OF ADVANCED DATA TRANSMISSION TECHNIQUES

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SEPTEMBER 1962

TO FEDERAL AVIATION AGENCY

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GENERAL DYNAMICS | ELECTRONICS-ROCHESTER

Rochester, New York

September 1962

to
FEDERAL AVIATION AGENCY

Contract No. FAA/BRD-80

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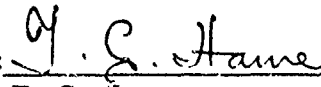

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INTRODUCTION - PART II

The following pages, comprising Part II of the final report on FAA/BRD-80 "Analysis of Advanced Data Transmission Techniques," consist of detailed information relating to Sections 3 and 4 of Part I, accordingly numbered Sections 3 and 4, and a supplementary group of schematics and block diagrams designated Section 9. Part II contains no intervening sections.

The report has been divided in this way to separate its total bulk into two roughly equal parts and to improve its utility. For those primarily interested in circuit design and layout and operating details relating to the Test Facility and experimental converters, Part II will serve as a convenient reference.

SECTION 3.0 TEST FACILITY (PART II)

3.1 Introduction

The Test Facility was designed as a complete FSK binary information link with provision for performance evaluation. Operation is based upon optimized circuit conditions with the ability to present various data for each of several test parameters. It has been constructed on standard relay racks with a plug-in circuit breadboard design. A description of the Facility and Keyer-Converter along with their function, layout, logic and operating procedure follows. Fig. 3.0 is a picture of the Test Facility and associated test equipment.

3.2 Function

The function of the Test Facility is to generate, transmit, and receive a 6 bit test signal and to make a comparison of the transmitted and received forms of that signal. The system is designed to be used with Keyer-Converters capable of accepting pulse lengths of 1 to 30 milliseconds. Included in the Facility are provisions for error correction and null evaluation along with bit error rate and character error rate measurement. These functions are performed by 8 counters as indicated in Fig. BD-10.

3.3 Signal

The signal generated by the Facility is a repetitive 6 bit character with odd parity injected in the sixth bit. The pulse length can be varied in six steps: 1 ms, 2 ms, 5 ms, 10 ms, 20 ms, and 30 ms.

30 ms. The message can be selected for any mark-space code by the 5 bit-selection switches. In addition to the message block, transmitter and receiver timing pulses are generated for use in the logic circuits. These pulses, along with their position in respect to the signal, are shown in Fig. 3.1.

3.4 Layout

The Test Facility has been constructed on two standard relay racks. Pictorial layouts appear in Fig. BD-C and Fig. BD-D, showing rack area designations, their function, corresponding circuit block diagrams, circuit and card functions, and locations.

The main relay rack containing the Facility is designated by areas coded A-1 through A-7. These areas include the clock pulse generator, mechanical counters, shift registers and comparators, pattern generator, and transmit-receive pulse generator. The auxiliary relay rack is designated area A-8 and contains the optimized FSK Keyer-Converter portion of the system.

The Test Facility uses standard X-Y coding nomenclature for layout location. See Fig. BD-A. Each eyelet, circuit board, and area can be described by reference to a 9 digit code, based on a combination of letters and numerals. Example designations are shown with their proper locations on the area pictorial Fig. BD-A.

3.5 Diagrams

The operation of the Test Facility is covered in the block diagrams Fig. BD-1 through Fig. BD-12. The coding of circuits on these block diagrams is given in Fig. BD-B. In addition, area, location, and eyelet designations are given on each block to facilitate locating circuits and circuit interconnections. Each block is marked with a reference schematic number "S", which refers to a schematic diagram in the schematic section.

3.6 Power Requirements

The Test Facility requires external DC power for operation.

The voltage and current requirements are as follows:

+ 10 volts @ 500 ma

- 10 volts @ 2 amps

In addition, an external audio noise source and an audio RMS voltage reading instrument are necessary for adjusting SNR ratios in the Keyer-Converter section for test purposes.

3.7 Facility

The operation of the Facility is covered in Fig. BD-12, a Master Block Diagram of the Test Facility. Each major section will be considered separately.

3.7.1 Clock Pulse Generator

The Clock Pulse Generator is located in Area A-1 and is covered on block diagrams in Fig. BD-1 and Fig. BD-2.

The function of the Clock Pulse Generator is to create a series of transmit and receive timing pulses with the proper delays at six selectable bit rates.

The circuit operates from a stable crystal oscillator (S-12) which produces a 4 kc square wave output. The pulse Length Selector Switch SW-1A selects this output or a submultiple for use in creating the TB and RB pulses. The TB pulses are formed directly by a countdown of 4 and the proper differentiation, gating, and inversion. The formation of the RB pulses is identical with that of the TB pulses with the exception of three input pulse delay circuits.

Fractional Bit Delay Switch SW-2 (S-19) controls the input to Shift Registers 1 and 2, allowing the RB pulses to be shifted in four $1/4$ bit steps. The $1/8$ Bit Delay Switch SW-16 (S-12) provides an additional $1/8$ bit delay in all positions of the Fractional Bit Delay Switch. The Variable DMV-1 (S-13) is controlled by the second section of (SW-1B), the Bit Length Selector Switch, and has a vernier control continuous delay of 0 to 7.5 milliseconds. The combination of these delay circuits is sufficient to produce the required delay in the receiving pulses to correspond with the delay in the Keyer-Converter used with the system.

The following bit lengths are generated in the system with the Pulse Length Selector Switch in the position indicated:

<u>Position</u>	<u>Bit Length</u>
1	1 ms
2	2
3	5
4	10
5	20
6	30

The TB and RB pulse lengths do not exceed 20 microseconds in any position of the Pulse Length Selector Switch.

3.7.2 Transmit Character Pulse Generator

The Transmit Character Pulse Generator is located in Area A-7 and is covered on the block diagram in Fig. BD-3. The function of the Transmit Character Pulse Generator is to create the TL pulses (Fig. 3.1) from the TB_0 pulse.

The TB_0 pulse is sent through a series of 3 counters and is NOR gated in 6 combinations. This result is AND gated with TB_2 to set the transmit TL pulses in the center of the selected bit. The outputs of the generator are tied to SW-4, the Phase Delay Selector

Switch on BD-4.

3.7.3 Receive Character Pulse Generator

The Receive Character Pulse Generator is located in Area A-7 and is covered on the block diagram in Fig. BD-4. The function of the Receive Character Pulse Generator is to create the RL pulses from the TL pulses.

Phase Delay Selector Switch SW-4 selects a TL pulse for triggering FLip-Flop-1 (S-18). RB_0 is used to reset F/F-1 and shift the signal from Shift Register-4. AND gating with the proper RB pulse produces the required character rate receive pulses. The Phase Delay Selector Switch provides proper selection of system character timing.

3.7.4 Pattern Generator

The Pattern Generator is located in Area A-6 and is covered on the block diagram in Fig. BD-5. The function of the Pattern Generator is to generate a 5 bit pattern and to inject odd parity in the 6th bit.

Manual pattern switches are provided to code into the NOR gates a mark or space (ground or -10 volts). At time TL_{62} these levels are gated and inverted and passed into the Transmit Shift Register. Odd parity (mark) is injected in the 6th time slot as a function

of Counter C-14. The output of C-14 is sampled at TL_{52} and gated into the Shift Register SR-15 at TL_{62} , which resets C-14 and reads the next character code into the shift registers.

The outputs of the Pattern Generator Transmit Register are sent to the keyer and 1 Bit Comparator-1. The coded input levels are sent to the 5 Bit Comparators.

3.7.5 Receiving Register and Comparators

The Receiving Register and Comparators are located in Areas A-4 and A-5 and are covered on block diagrams Fig. BD-6 and Fig. BD-7. The function of the receiving registers is to place the incoming signal timing in the correct phasing for comparison with the transmitted signal and to provide logic outputs for the various counters. The comparators receive the signal from the receiving registers and compare it with the transmitted code.

The signal from the detector (decision circuit) is center sampled and shifted out of Shift Register SR-18 by RB_0 and into the receiving registers of 5 Bit Comparator-1. The output of this Comparator (COMP 1') is negative when the comparison is correct.

If a null occurred during any bit the output of One Bit Comparator COMP-2 will be inverted with respect

to the signal from the detector and this output will be shifted through Correction Register SR-19 to the receiving register of 5 Bit Comparator-2 by RB_0 . The output of this Comparator (COMP 2') is negative when the comparison is correct.

Null count logic is provided by COMP-3 output, sampled at RB_1 ' in AT-19. Bit error count is made by a one bit comparison with the transmitted signal in COMP-1 and sampling by RB_1 ' in AT-17. The number of marks occurring are counted in C-15 and provide ERROR and ERROR' outputs. ERROR is negative for 1, 3, or 5 marks in a 6 bit block (odd parity check). A ONE NULL signal is also provided from N-16 for use in the Mechanical Counter section.

3.7.6 Mechanical Counters

The Mechanical Counters are located in Area A-2. Their associated logic and driving circuitry is located in Areas A-3 and A-4. The circuitry is covered in the block diagram on Fig. BD-8. The function of this section is to count mechanically the various logic circuit outputs.

The mechanical counter units operate in the plate circuits of 35C5 pentodes (S-9). Each 35C5 is driven by a 2N597 transistor driver (S-7) which operates from a DMV (S-7), furnishing a 15 to 20 millisecond driving

waveform. Three Counters (MC-1, MC-2, and MC-3) contain divide-by-10 counters on their DMV inputs for high speed operation. The remaining counters have direct driven DMV's. The mechanical counter unit has a self contained Power Supply (S-1).

The function of the remaining logic circuits can best be explained by consideration of the input requirement for each counting operation separately in Counter Function Table, Fig. 3.2.

3.7.7 Divide-by-10 Decimal Decoder and Meter Indicator

The divide-by-10 Decimal Decoder and Meter Indicator circuits are located in Areas A-3 and A-4 and are covered on the block diagram in Fig. BD-9. The function of this circuitry is to provide high speed operation of Counters MC-1, MC-2, and MC-3 by dividing the inputs by 10 and providing a units readout meter.

The counters operate with the logic as indicated in the logic diagram on Fig. BD-9. Automatic reset is provided by RL_{13}' . A momentary toggle switch is provided for manual resetting. Readout currents are controlled by individual fixed resistors in the counter outputs A', B', C', and D'. A meter adjust vernier is provided to control the meter current to give approximately linear indications.

3.8 Facility Logic and Counter Functions

The Facility logic is shown in Fig. BD-10. Counter locations are given in the pictorial provided. Reference should be made to Master Block Diagram, Fig. BD-12, and Counter Function Table, Fig. 3.2, for a complete analysis of system operation.

The ten counting functions shown in Fig. BD-10 are performed by 8 mechanical counters and two simple arithmetic calculations. If tests are being performed at high bit rates and low SNR ratios, electronic counting must be used to supplement the mechanical counters for accurate count. These may be connected into the system at the inputs to DMV's 2 through 9. See Fig. BD-8.

3.9 Facility Operating Procedure

The following operating procedure covers the Test Facility Areas A-1 through A-7 and all controls located therein. It assumes a complete and functioning Keyer-Converter, as described in Section 3.10 of this report, and proper input and output connections to the Facility.

- 1 - Apply power to all circuits by operating the external supplies and the self-contained mechanical counter supply in A-2.
- 2 - Select the proper pulse length for transmission with Switch SW-1 (A1L52).
- 3 - Select a message on the 5 bit Code Selection Switches SW-5 through SW-9 (A6L23). See pictorial on Fig. BD-5.

- 4 - Adjust 1/4 Bit Delay Switch SW-2 (A1L62), 1/8 Bit Delay Switch SW-16 (A1L11R056), and variable control on DMV-1 (A1L33R033) for center sampling of the received signal by RB₀ at SR-18 (A4L12), using an oscilloscope to monitor the adjustment.
- 5 - Adjust Phase Delay Selector Switch SW-4 (A7L52) for RL₁₃ reset at Counter C-15 (A4L73) to occur during the parity (6th) bit. (Note: Proper adjustment of SW-4 will permit only Message Blocks with No Error (MC-1) to count with a noise-free signal from the detector and a message other than alternate mark-space).
- 6 - Switch SW-10 is provided as an ON-OFF Test Switch (A3L12) and should be operated to start and stop the test.
- 7 - Switch SW-17 (A6L71) should be placed in keyed position for Test.

The Facility is now properly adjusted for Keyer-Converter evaluation. Supplementary checks and adjustment of Counters C-16, C-17, and C-18 can be made with the controls provided (R156 on Divide-by-10 Counter) for proper digits read-out on Counters MC-1, MC-2, and MC-3. All counters should be reset with the switches provided before each test.

3.10 Keyer and Converter

The Test Facility is provided with a complete matched set of

tone keyers and optimized converters located in Area A-8. The circuit parameters are based on those discussed in General Dynamics/Electronics-Rochester Preliminary Report for Task I and Interim Report for Task II, "Analysis of Advanced Data Transmission Techniques," Section 5.1.

A block diagram of the Keyer-Converter is shown in Fig. BD-11. The series of plug-in units provided will adapt the unit for operation at 6 different bit rates. Fig. 3.3 presents the pertinent keyer and filter data for the test parameters. Each block of Fig. BD-11 is referenced to a schematic "S" number. Interconnections are shown on Fig. BD-11.

An external noise generator and RMS reading voltmeter must be used with the system for evaluation.

3.10.1 Keyer

The Keyer, shown on Schematic S-24, is a feedback oscillator with provision for accepting plug-in tank circuits (S-23). The tank circuits are so constructed that a keying signal (-10 volts) into the keyer will short the keying capacity to ground and so lower the frequency of oscillation. Voltage feedback stabilizes the keyer output. Six tank circuits are provided with the Keyer (Fig. 3.3) and are tuned to give optimum performance and balanced converter outputs.

3.10.2 Band Pass Filters

Two identical Band Pass Filters are provided for each bit length (Fig. 3.2) and their basic configuration is shown on Schematic S-26. These filters serve two purposes in the operation of the converter.

Band Pass Filter #1 follows the Mixer Amplifier and defines the system bandwidth, rejecting all noise components outside this band. The design criteria for this filter will be discussed in Section 4.

Band Pass Filter #2 follows Limiter #3 and provides a matched phase characteristic with that of Filter #1 at the center of the passband (within 2°). In addition, Filter #2 contributes a phase shift characteristic throughout the band which contributes to converter operation by establishing a reference channel.

3.10.3 90° Phase Shift Integrator

The 90° Phase Shift Integrator (S-28) is a modified operational amplifier with capacitive feedback. This amplifier provides a constant 90° phase shift over the frequency of operation, thereby completing the phase shift necessary in the reference channel for driving the phase detector. The system phase table of Fig. 3.4 explains the phase relationship between the signal and reference channel after the signal has passed through

the band pass filters and the 90° Phase Shift Integrator.

Fig. 3.5 shows the phase detector driving waveforms for center frequency and the two keyed frequency conditions.

3.10.4 Limiter Amplifiers

The Limiter Amplifiers (S-27) provided with the converter are operated in cascade to provide a high system gain. Each Limiter is an operational amplifier with voltage feedback in each section to provide a large dynamic range of input for a constant square wave output amplitude of approximately 1 volt peak-to-peak. The Limiters provide gain sufficient to operate the converter with input levels (measured at the output of BPF #1) of less than 1 millivolt.

3.10.5 Driver Amplifiers

The Driver Amplifiers (S-29) receive the outputs of the Limiter Amplifiers #4 and #6 and boost this waveform to an amplitude of 7 volts peak-to-peak for use in driving the AC coupled feedback power amplifiers.

3.10.6 Power Amplifiers

The Power Amplifiers (S-33) used in the converter are transformerless complementary symmetry feedback amplifiers capable of furnishing a 4 volt peak-to-peak driving waveform into the 8 ohm primary winding of the phase detector transformer. Peak powers of over 250 milliwatts can be

provided during detector conduction cycles. The output gain control is in the feedback loop.

3.10.7 Phase Detector

The Phase Detector (S-30 and S-17) combines the signal and reference channels by transformer coupling in a manner to provide diode conduction on a positive going reference and signal waveform combination. Fig. 3.6 shows the basic detector waveforms for a center frequency condition. Phase detector outputs are obtained by the net difference in voltage developed across C_1 and C_2 (S-17) over the period of a bit. This integrated waveform is referenced to + 5 volts and adjusted (gain control on the Power Amplifiers) for ± 5 volts output in respect to this reference. The reference waveform is maintained at an amplitude greater than one-half that of the signal waveform.

3.10.8 Low Pass Filter & Emitter Follower Driver

The Low Pass Filter (S-31) is driven by the phase detector and its output is referenced to + 5 volts. Six plug-in Low Pass Filters are provided for operation at each pulse length (Fig. 3.3). The Emitter Followers (S-32) provide isolation and current gain for driving the decision circuitry without shifting the reference potential significantly.

3.10.9 Decision Circuit

The Decision Circuit (S-32) is designed to provide a mark-space (Gnd. or - 10 volts) output, switched each time the incoming waveform crosses the reference potential (+ 5 volts). Fig. 3.7 shows the waveforms present in the decision circuitry on an alternate mark-space code. In addition to a signal output, the decision circuit has an adjustable null detection network, which provides an output (Gnd.) when the signal fails to pass a preset level (positive or negative in respect to the reference voltage). Signal and Null outputs are used to drive the receiving registers where they are center sampled by RB_0 .

3.10.10 Mixer Amplifier

The Mixer Amplifier (S-25) provides a means of mixing noise and signal and the necessary isolation for SNR measurements. Switches SW-14 and SW-15 (Fig. BD-11) select noise or signal inputs separately. The mixer gain control is located in the feedback loop and controls the amount of signal and noise driving BPF #1.

3.11 Noise Feedback Control

An external noise source must be used with the keyer-converter to provide a white noise spectrum for SNR evaluation of the system. General Radio Random Noise Generator type 1390B or similar type audio noise source is recommended for use with the system.

The noise source should be fed through an external bandpass filter

adjusted for a passband of ± 1.2 kc at the center frequency used. The output of this filter is fed to the BNC connector input of the Noise Amplifier on A8L11 as shown on Schematic S-38. This high gain amplifier has been shielded and decoupled to provide maximum isolation from supply line transients, associated circuitry, and stray fields.

The noise input to the amplifier must be sufficient to provide a nominal feedback voltage of 1.7 volts at point "X". A typical input using the GR 1390B is 2 volts, read on the instrument output meter. A feedback loop is provided to stabilize RMS noise amplitude without destroying the Gaussian characteristics of the noise.

A noise output, obtained at A8L11R086 and fed through a banana jack R051, is amplified by the Buffer Amplifier (S-34) on A8L23 with its input on R015. The output of this Operational Amplifier (R043) is fed through a Bandpass Filter (A8L33). Four filters (S-35) are provided for this function. They are used as follows:

<u>Noise Filter</u>		
<u>Pulse Length</u>	<u>Center Freq.</u>	<u>Bandpass</u>
1 ms	8 kc	900 c/s
2	4	450
5	1.6	190
10	1.6	190
20	1.6	47.5
30	1.6	47.5

The Noise Feedback Filter output is fed to Band Limited Noise

Amplifier No. 1 (S-36) (A8L43R017), and its output (R028) is taken to Band Limited Noise Amplifier No. 2 (S-37) (A8L23R016). Both amplifiers are operational amplifiers. The output of Amplifier No. 2 (R047) is taken to R065 via banana plug R041 and transformer coupled to a Bridge Rectifier (S-38). The DC output of this rectifier is filtered by a long time constant L-C network and DC coupled to an emitter-follower. The output of this emitter-follower is point "X" and provides a feedback voltage, which is a function of the noise in a limited pass-band.

Results show that this system of noise control appears to be the only feasible means of making long term narrow band noise measurements. A Flow Corporation Random Signal Voltmeter type 12A1 was used for noise measurements. This instrument has a time constant of 16 seconds.

No gain controls are provided in the noise control system. After adjustment of noise input level from the noise source for the nominal DC feedback voltage at point "X", all measurements are based on the existing noise level present out of the Mixer Amplifier.

3.12 Keyer and Converter Operating Procedure

The Keyer and Converter are supplied with six sets of plug-in cards for operation of the system as indicated in Fig. 3.3. These plug-in units consist of the following:

1. Keyer Tuned Circuit
2. Two Identical Band Pass Filters
3. Low Pass Filter

Each of the circuits has been adjusted for optimum conditions under actual operation and test. The phase detector RC time constant has been included on the Low Pass Filter card and has been selected to minimize non-linearities existing in the system under noise conditions. The keyer tuned circuit has been adjusted to provide a specified shift and a reference (+ 5 volts) output from the phase detector on alternate mark-space code.

The following procedure should be followed to place the Keyer-Converter into operation or in changing from one set of plug-in units to another:

1. Place plug-in cards in their proper positions as follows:

<u>Position</u>	<u>Card</u>
L 31	Keyer Tuned Circuit
L 71	Signal Filter
L 13	Reference Filter
L 62	Low Pass Filter

2. Apply power to the system.
3. With Jumper J-1 removed adjust the decision circuit for reference (+ 5 volts) output (A8L72R041).
4. Adjust the variable null control (A8L72R026) for

the null width desired by measuring between R015 and R016.

5. Adjust the amplitude of the output of Power Amplifiers #1 and #2 to provide ± 5 volts (with respect to the reference) at the output of the Low Pass Filter with switch SW-17 (A6L71) in mark and space positions, respectively (maintain reference output greater than $1/2$ signal output). Return this switch to keyed position after adjustment has been completed.
6. Connect an audio noise source to the BNC connector provided on L11 through an external bandpass filter with a bandpass of ± 1.2 kc/s of the center frequency of operation. Using the correct Noise Feedback Filter in L33, (see Section 3.11) adjust the noise source output to give 1.7 volts DC at point "X" in the Noise Amplifier.
7. Adjust the Test Facility as instructed in Section 3.9.

Measurement of SNR ratio can be carried out at the output of Band Pass Filter #1 (A8L7LR041) with a long term averaging RMS reading voltmeter. Amplitudes can be controlled by the output control on the keyer and mixer. It is advisable, however, since input noise levels are limited by the feedback loop, to set the mixer control fully clockwise (maximum) and to adjust SNR ratios by using the keyer output control. Switches SW-14 and SW-15 are provided for convenience in making system measurements. These switches apply signal and noise independently to the mixer amplifier.

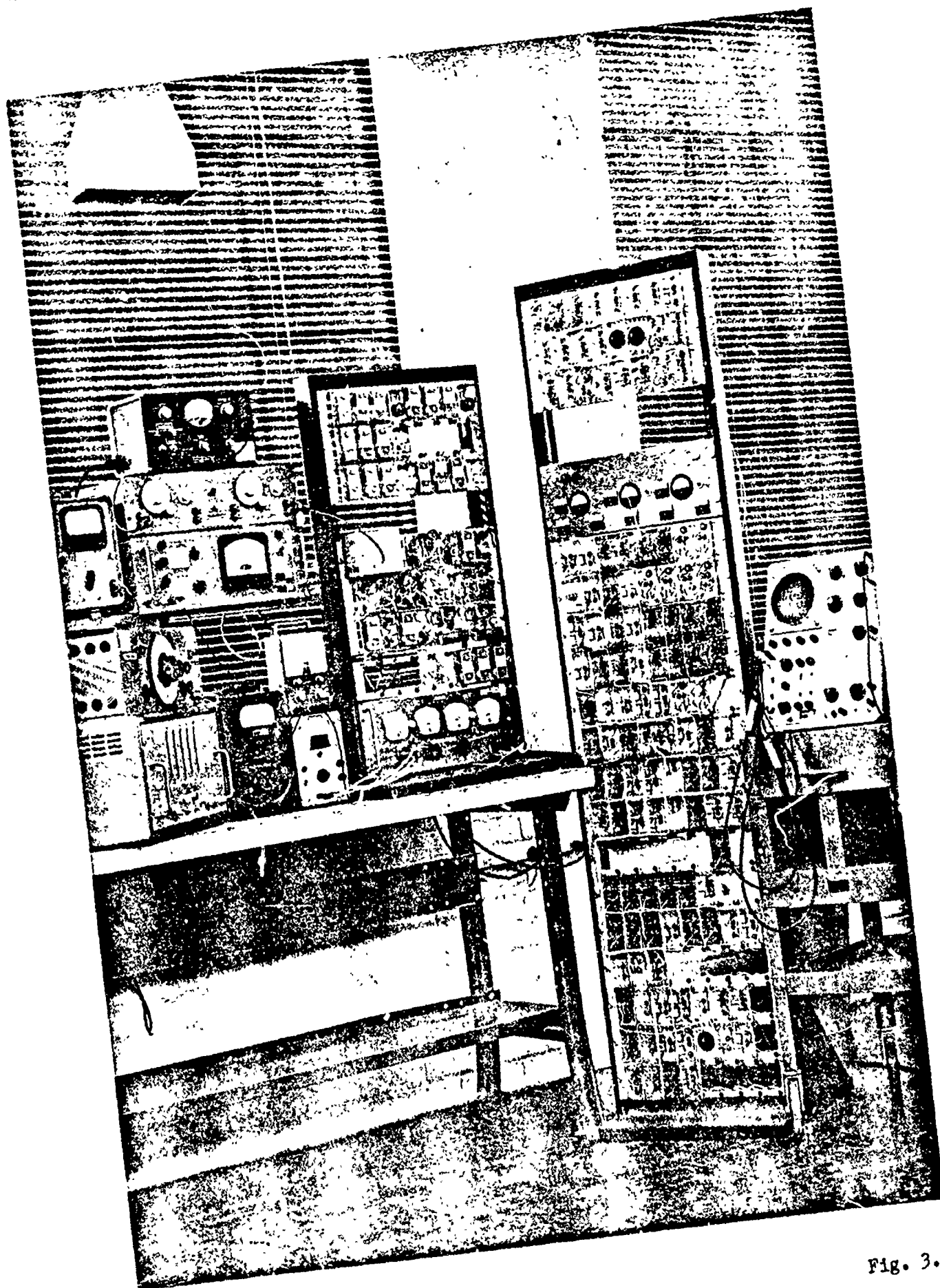
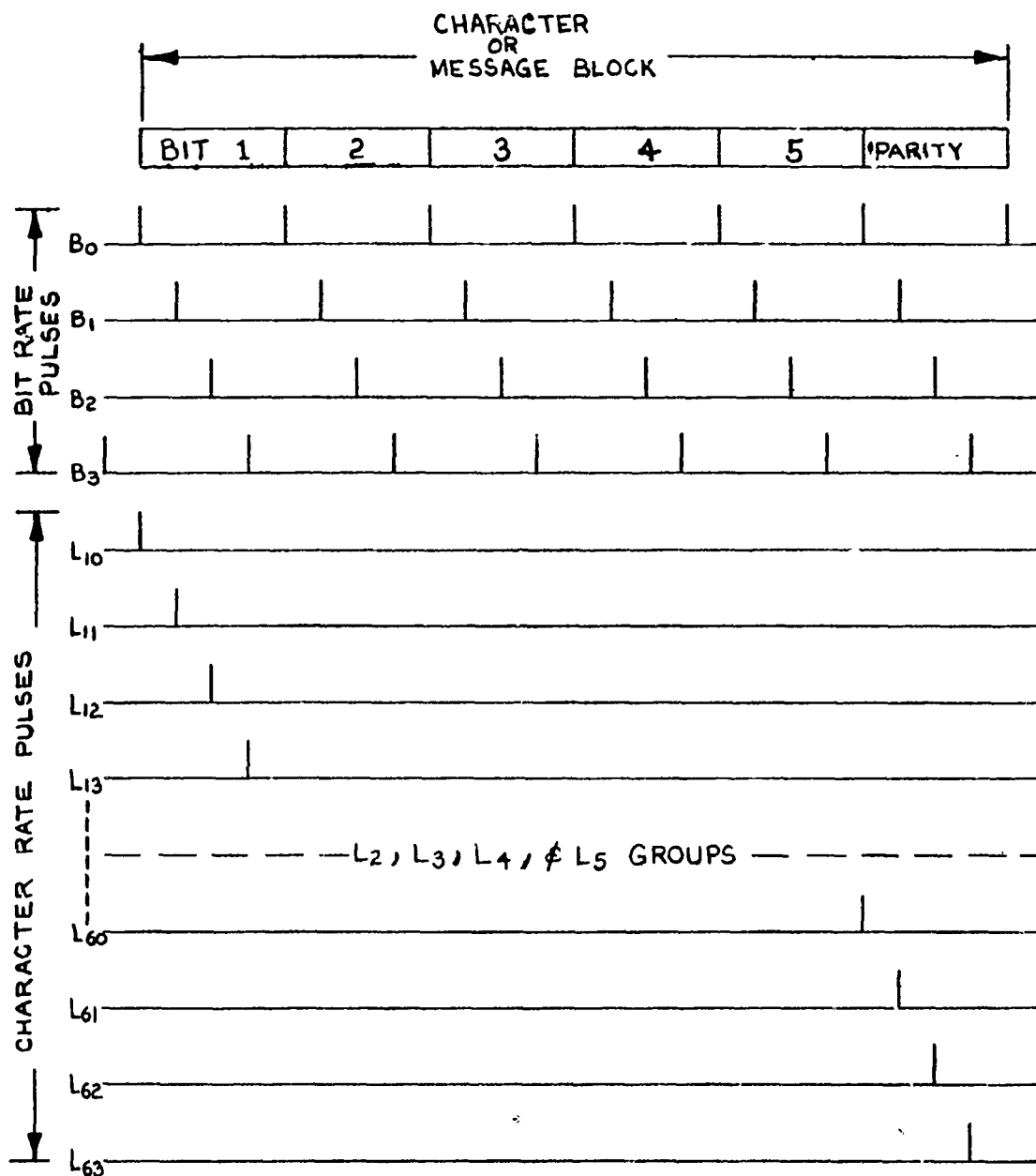


Fig. 3.0



PULSES ARE PREFIXED WITH T IN THE TRANSMIT PORTION OF THE FACILITY AND WITH R IN THE RECEIVE SECTION, i.e. TB_0 , RB_0 , ETC. PRIMED PULSES ARE OBTAINED BY INVERSION, i.e. $B_0(\text{INVERTED}) = B_0'$

PULSE SEQUENCE
DIAGRAM

FIG. 3.1

COUNTER FUNCTION TABLE

<u>Counter</u>	<u>Counting Function</u>	<u>Input Required for Count</u>
1	Message Blocks with No Error	ERROR', COMP 1', and RL ₁₂
2	Bit Errors	Output from AT-17
3	Nulls	Output from AT-19
4	Message Blocks with Parity Error	ERROR and RL ₁₂
5	Message Blocks with Errors other than Parity	ERROR', Not COMP 1', and RL ₁₂
6	Successful Corrections	Parity Error, ONE NULL', and COMP 2'
7	Correction Failures	Parity Error, ONE NULL', and Not COMP 2'
8	No Nulls or 1 Null	Parity Error and Not ONE NULL'

Fig. 3.2

KEYER AND FILTER TABLE

<u>Pit Length</u>	<u>Bit Rate</u>	<u>Center Freq.</u>	<u>Freq. Shift</u>	<u>Optimum Filter BW*</u>	<u>Low Pass Filter 3 DB#</u>
1 ms	1000 b/s	8000 c/s	700 c	1500 c	750 c/s
2	500	4000	350	750	375
5	200	1600	140	300	150
10	100	1600	70	150	75
20	50	1600	35	75	37.5
30	33 1/3	1600	23.3	50	25

* BW = 3/2 Bit Rate

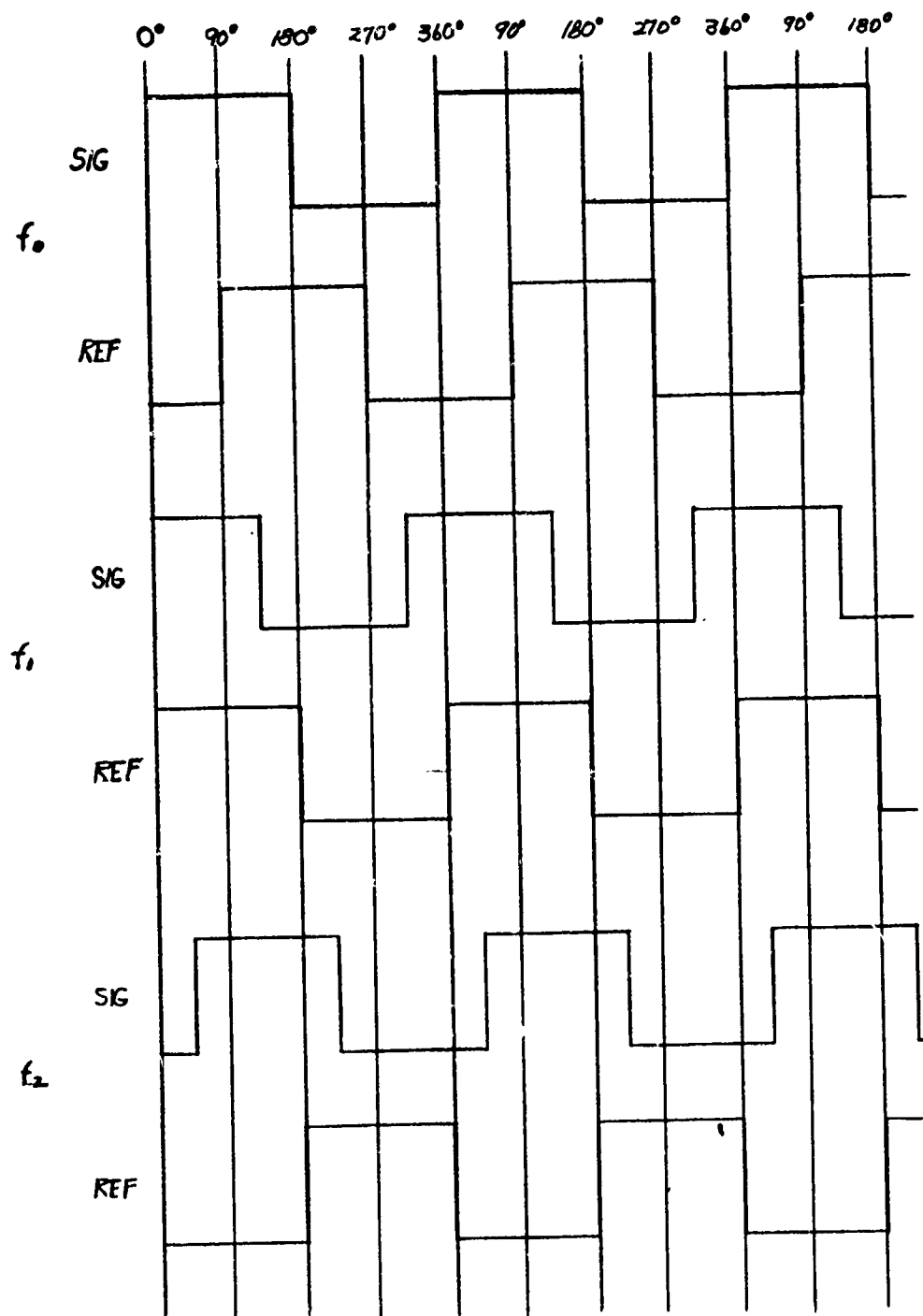
DB cutoff = 3/4 Bit Rate

Fig. 3.3

SYSTEM PHASE TABLE

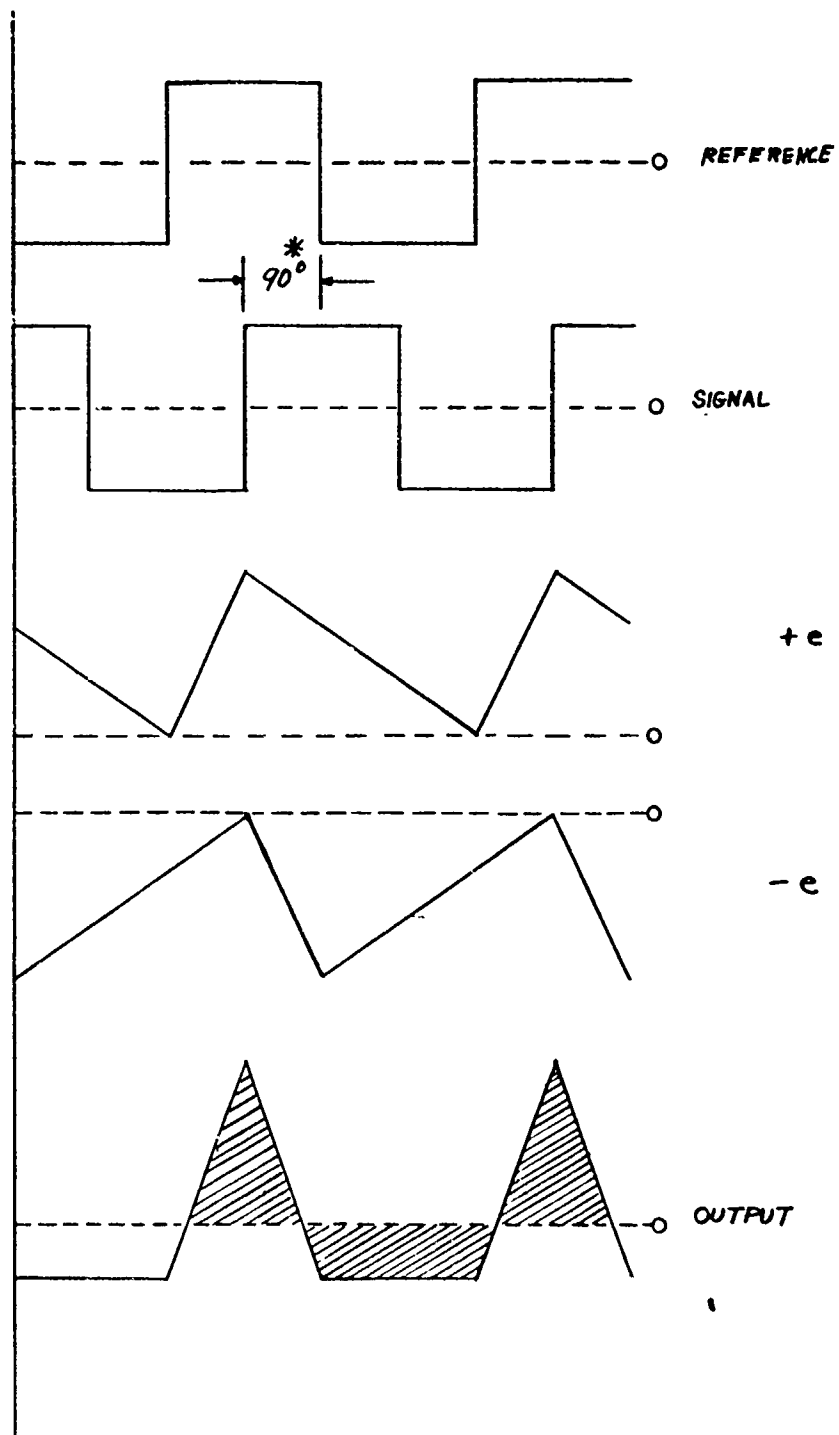
Referred to Input of Band Pass Filter 1

REFERENCE CHANNEL		SIGNAL CHANNEL	
Circuit Providing Phase Shift	Phase Angle at Frequency	Circuit Providing Phase Shift	Phase Angle at Frequency
	f_1 f_c f_2		f_1 f_c f_2
BPF #1	-45° 0° +45°	BPF #1	-45° 0° +45°
BPF #2	-45° 0° +45°		
90 P.S. INT	+90° +90° +45°		
Total Reference Phase Change	0° +90° +180°	Total Signal Phase Change	-45° 0° +45°
Reference Phase Relative to Signal	+45° +90° +135°		



SYSTEM PHASE CHARACTERISTICS

FIG. 3.5



BASIC PHASE DETECTOR WAVE FORMS

* CENTER FREQUENCY CONDITIONS

FIG. 36

DECISION CIRCUIT WAVEFORMS

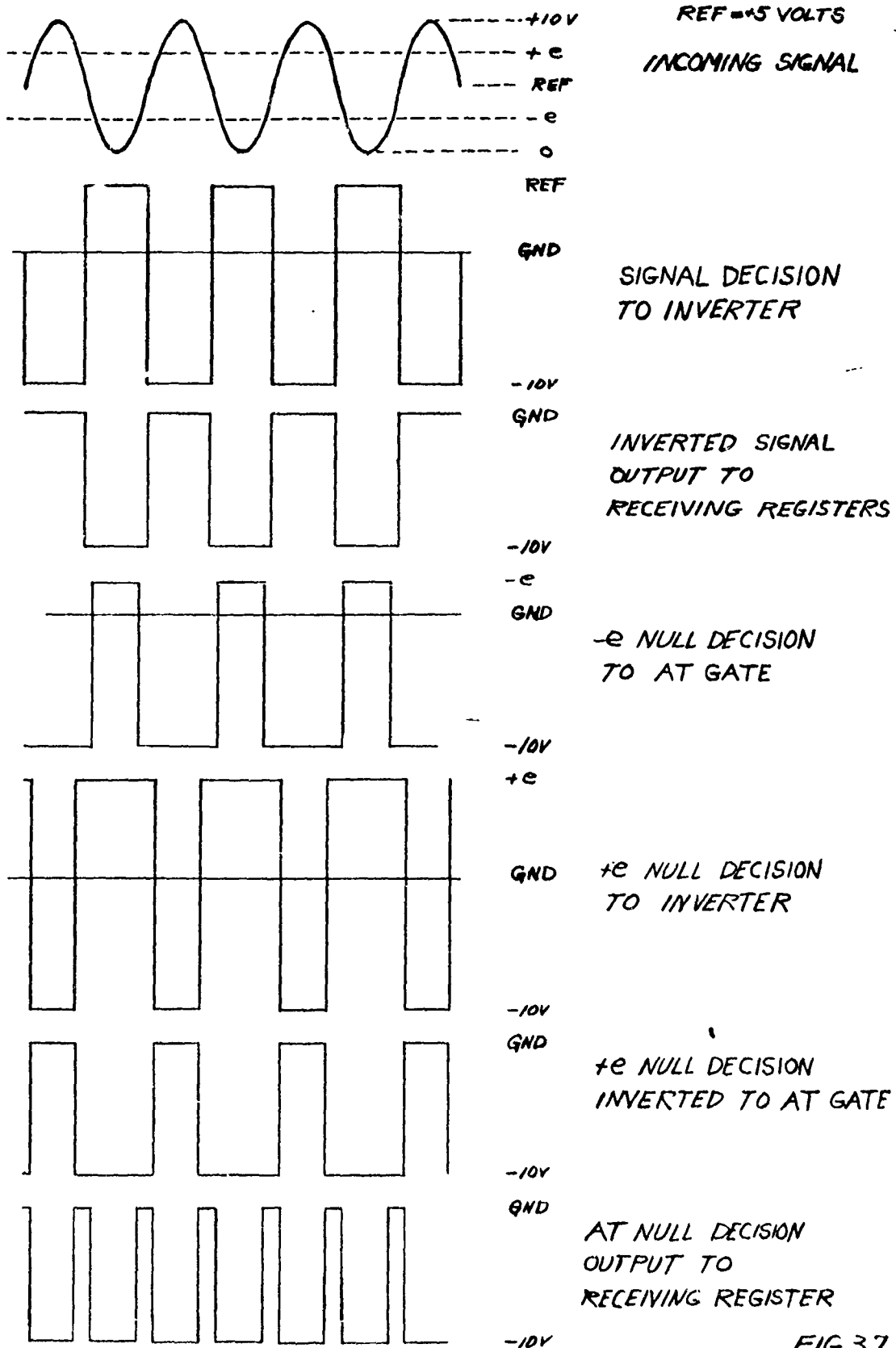


FIG 3.7

SECTION 4.0 CONVERTER DESIGN (PART II)

4.1 Introduction

The converter section (Fig. 4.8) of the Test Facility was designed to test the predictions of Montgomery³ and to provide a set of optimized data at each of six pulse lengths. In order to accomplish this task, it was necessary to provide keys able to accept an input code and generate an FSK signal with the prescribed frequency shift. A source of white noise was also necessary to correlate the results with predicted performance. A highly detailed analysis of the converter is outside the scope of this report; presented in this section are some of the more important design considerations.

4.2 Converter Operation

Signal and noise can be selected individually by Switches S_1 and S_2 (Fig. 4.8) and their levels measured at point A, where the values of signal-to-noise power ratio in the system bandwidth are defined. After three stages of limiting, providing gain at low input levels squaring action at high inputs, the signal splits into the signal and reference channels. In the signal channel more gain is provided through another limiter, a driver amplifier, and a power amplifier to drive the signal winding of a phase detector. In the reference channel the phase shift filter alters the phase of the signal, causing lead or lag of a magnitude proportional to the difference between the signal frequency and the center frequency of the phase shift filter. The reference signal now passes through

an integrator, which produces a 90° phase shift in the reference signal, and, after two stages of limiting, it is applied through a driver amplifier and a power amplifier to the reference winding of the phase detector.

At center frequency the signal and reference square waves are 90° out of phase at the input to the phase detector and there is no output. As the frequency moves above and below the center value, the phase shift in the reference channel varies and the detector output will go positive and negative, accordingly. A low pass filter removes the carrier and a decision circuit centered about zero output from the phase detector gives mark or space output, as the frequency at the input varies above or below the center frequency.

4.3 Converter Circuit Design

4.3.1 The Mixer Amplifier

In order to perform converter SNR measurements, a circuit was required to mix signal and noise in a linear manner so that each one could be measured separately and then added to obtain the combined effect without change in the measured value of either. The mixer amplifier was required to drive a bandpass filter with a purely resistive source impedance of 600 ohms. These requirements led to the selection of an operational amplifier (Fig. 4.1A) to sum signal and noise. Fig. 4.1B shows the amplifier modified for use as a mixer. Fig. 4.1C shows the basic circuit of the operational amplifier.

This amplifier will supply voltage gains of 20 db, which are independent for signal and noise. The output impedance is of the order of 1 ohm and, therefore, the use of series resistance provides ideal matching for all loads.

4.3.2 The Bandpass Filters

Fig. 3.3 shows a table of data pertinent to the design specifications of the bandpass filters. Section 4.3, Part I, discusses the design criteria for these filters. The response characteristics are shown in Fig. 4.2A through Fig. 4.2F. The filters (S-26) are two branch L-C units with bandwidths shown on each curve to the 3 db points. These filters provide phase shift characteristics of $\pm 90^\circ$ across the bandpass. The first bandpass filter of Fig. 4.8 defines the noise bandwidth of the converter and maximizes SNR ratio. The second bandpass filter is matched to within 2° of the first and establishes a reference phase (Fig. 3.4).

4.3.3 Limiters

The function of a limiter amplifier in an FM system is to remove amplitude variations from the received signal. Two requirements for a limiter are operation over a wide range of input voltages and maintenance of a symmetrical waveform over this dynamic range. A circuit which meets these requirements is a modified operational amplifier with a non-linear feedback network, consisting of two diodes in parallel with opposite polarity. Fig. 4.3A shows the basic circuit con-

figuration.

The diode selected for the feedback network was chosen for a minimum forward voltage drop change for a given change in current. The 1N816 diode used for this function exhibits a forward voltage change of 0.4 volts to 0.8 volts (2X) for a change in current from 10 microamps to 10 milliamps (1000X). At very low levels the circuit acts as a simple amplifier. As the input is increased, limiting starts to take place and with further increases very little change in peak-to-peak output will occur. The slope of the leading and trailing edge of the waveform will increase to the limit of the circuit elements when limiters are cascaded. These amplifiers are responsible for the sensitivity (less than 0.5 millivolts at all pulse lengths) and wide dynamic range (70 db voltage gain) of the converter.

4.3.4 Integrator

The function of the integrator in the converter is to provide a fixed 90° phase shift throughout the frequency range of operation. The basic operational amplifier with a capacitive feedback loop was selected to perform this function. Fig. 4.3B shows a schematic of this amplifier. R_1 was made equal to 600 ohms to terminate the filter correctly, and $1/\omega C$ was made equal to 600 ohms at 8 kc, giving unit gain at that frequency and a gain of 5 at 1.6 kc. The phase shift through the integrator was within 2° of 90° over the frequency

range of operation.

4.3.5 Driver and Power Amplifiers

The output of the limiter amplifiers after squaring is only 1.2 volts peak-to-peak, which is inadequate to drive a saturating transistor stage directly. The driver amplifiers were designed for use at this point in the system to provide a gain of approximately 6 and an output centered about ground. The power amplifiers are complementary-symmetry emitter-follower output devices with the ability to furnish a 4 volt peak-to-peak output into 8 ohms for driving the phase detector.

4.3.6 The Phase Detector

The phase sensitive detector is shown in Fig. 4.4A with reference symbols. Fig. 4.5 presents wave form diagrams for a square wave input, total signal and reference amplitudes, and a linear charge and discharge characteristic assumed for the capacitors. As the phase of the reference and signal changes from the 90° (center frequency) condition depicted, longer or shorter charge and discharge times will apply for the Capacitors C_1 and C_2 , and a net DC level change in the output E with respect to F will take place in an amount proportional to the phase change. Transformer coupling is necessary in a detector of this description for two major reasons: (1) to provide a step-up and summing effect large enough to give the desired output voltage swing and (2) to

enable the insertion of a convenient reference voltage level on the output.

An investigation of the circuit after design showed some peculiarities of loading on the power amplifiers. It was determined that Capacitors C_1 and C_2 were continuing to charge long after such charge should have ceased. Fig. 4.4B shows a sketch of the expected voltage function and the actual voltage function observed at point A when point D is grounded. Ringing shown was due to lack of load on the transformer and is apparently not detrimental. The reasons for the effect shown were not immediately obvious, but experiment showed that a reduction in the capacitive load cut down this excess charge time. Too small a capacity was undesirable since the maximum voltage would then be reached with an exponential curve. A compromise of values was effected so that near-linearity was obtained with very little excess charge time showing. The excellent linearity of the resulting phase detector is shown for one set of parameters (30 ms) by the output voltage vs. frequency input curve in Fig. 4.6.

4.3.7 The Low Pass Filter

A simple two element low pass filter was designed for each pulse length, assuming zero source impedance and a 10 K load resistance. The filters were designed for the 3 db

cutoff shown in Fig. 3.3 and were constructed to have no over-shoot in their frequency characteristic. Response curves for these filters are shown in Fig. 4.7A through Fig. 4.7F.

The low pass filter and the phase detector are referenced to +5 volts, established by a bleeder in the decision circuitry. A pair of emitter followers are used for isolation and to minimize reference level changes due to the loading of the decision circuit.

4.3.8 The Decision Circuit

The decision circuit is a voltage comparator circuit designed to give a mark-space or space-mark output change as the signal from the detector crosses the reference potential e_0 (+5 volts). A potentiometer is provided for adjusting the voltage comparator to provide an output which is neither mark nor space under no signal conditions. A second control provides adjustment of a null zone e_w from 0 to 70% of the peak-to-peak signal amplitude centered about e_0 .

4.4 The Noise Source

A General Radio Random Noise Generator type 1390B was used as a noise source. Examination of the output of this generator in a narrow bandwidth showed amplitude fluctuations of a magnitude that made setting up for a long test run impossible. Examination of the characteristics of random noise showed that the envelope of the out-

put of a narrow band Gaussian random process contains frequency components down to very low values and that these components were causing variations in the RMS voltmeter readings, even though the unit employed (Flow Corporation Random Signal Voltmeter Model 12A1) had a time constant of 16 seconds.

It was determined that the output of a low pass filter following rectified narrow band Gaussian random noise is a function of the RMS value of input. Therefore, if a bandpass filter output were rectified and fed through a low pass filter with a time constant of one second, the resulting output could be used to control the gain in the noise channel. Variations less than 1 c/s would be greatly reduced, depending upon the gain in the feedback loop.

This system of feedback control (Fig. 4.9) was used with good success. The necessary amplifiers were employed in conjunction with an available bandpass filter to furnish a narrow band AC noise voltage to a bridge rectifier and low pass filter. A large time constant (several seconds) was used in the low pass filter and the resulting DC voltage was used to control the gain of a linear amplifier.

A commercial bandpass filter (Spencer Kennedy Laboratories Variable Electronic Filter Model 302) was used to limit the bandwidth of the noise source. The filtered output was fed through the gain controlled amplifier to the mixer. Reduction in the noise bandwidth allowed operation at a much higher noise level without clipping

and eliminated self-resonant responses of the main system filter at undesired high frequencies. With a noise bandwidth out of the commercial filter 2.4 kc/s centered about the converter bandpass mid-frequency and a level of 680 millivolts, the resistive attenuator at the noise feedback bandpass filter was adjusted to give -1.7 volts bias to the main noise amplifier at point "X" (S-38). Under these conditions, changes of -50% and +100% in noise produce an output change measured after the main system bandpass filter of less than $\pm 4.0\%$

4.5 Initial Converter Set Up

A single tone signal was fed through the mixer at the approximate working level of the converter and the waveforms at the output of the power amplifiers in each channel were examined. Adjustments of DC operating level were made at point A and point B (Fig. 4.8) so that the waveform on both channels was symmetrical. These adjustments were effected by means of bleed resistors to the power supply lines and were made once only, at the beginning of tests. Noise alone was fed into the system and the output of the low pass filter was examined on a DC meter with a long time constant. In general, the reading was not zero, and the resistors in the two halves of the phase detector were unbalanced slightly to produce a mean reading of zero.

A keyed signal consisting of alternate mark-space tones was applied which approximated the right amount of shift (Fig. 3.3). The low pass filter output was examined with the DC meter. The keyed fre-

quencies were adjusted to give the right amount of shift and zero output from the low pass filter. Each of the two keyed frequencies was fed in separately and the gain of the power amplifiers was adjusted to give a maximum deviation of ± 5 volts out of the low pass filter. The converter was then considered ready for operation at the chosen message rate.

4.6 Converter Waveforms

The operation of the converter is shown in a series of waveform pictures taken under actual operating conditions at a pulse length of 20 ms. Center frequency f_0 for this set of filters is 1.6 kc/s with mark f_1 and space $f_2 \pm 17.5$ c/s of center frequency. A description of the photographs follows:

Fig. 4.10 a1 Input and output of the first bandpass filter at f_0 with SNR = 20 db.

Fig. 4.10 a2 Input and output of the first bandpass filter at f_0 with SNR = 0 db.

Fig. 4.10 a3 Output of limiter #4 at f_0 with SNR = 0 db and 20 db, respectively. Output amplitude is 1.2 volts peak-to-peak.

Fig. 4.10 b1 Input and output of first bandpass filter at f_0 (no amplitude scale preserved).

Fig. 4.10 b2 Input to limiter #1 at f_0 with $e_{in} = 0.5$ volts peak-to-peak and output from limiter #2 with output voltage $e_o = 1.2$ volts peak-to-peak.

Fig. 4.10 b3 Input and output of 90° phase shift integrator at

f_0 (no amplitude scale preserved).

- Fig. 4.10 c1 to c3 Output from limiter #4 at f_0 for six SNR conditions from top to bottom: No noise, 20 db, 15 db, 10 db, 5 db, and 0 db, respectively.
- Fig. 4.10 d1 to d3 Output waveforms from power amplifiers for f_0 , f_1 , f_2 , respectively, with $e_{out} = 3$ volts peak-to-peak.
- Fig. 4.11 a1 to a3 Output (mark) of decision circuit for No noise, SNR = 20 db, and SNR = 15 db, respectively (leading and trailing edges of waveform shown only).
- Fig. 4.11 b1 to b3 Output (mark) of decision circuit for SNR = 10 db, SNR = 5 db, and SNR = 0 db, respectively (leading and trailing edges of waveform shown only).
- Fig. 4.11 c1 Output of low pass filter and decision circuit for mark, mark, space, space, mark, space and 10 volt amplitude.
- Fig. 4.11 c2 Output of phase detector at f_0 and output of signal power amplifier.
- Fig. 4.11 c3 Phase detector waveforms across diodes D_1 and D_2 .
- Fig. 4.11 d1 to d3 Null circuit, decision, and sampling waveforms for null widths of 50%, 30%, and 10%, respectively.
- Fig. 4.12 a1 to a3 Integrated output waveform of phase detector vs. input signal and reference waveforms for f_0 , f_1 , and f_2 , respectively.
- Fig. 4.12 b1 to b3 Phase detector diode waveforms for f_0 , f_1 , and f_2 , respectively, where total amplitude is 60 volts peak-to-peak.

4.7 Conclusions

This section has presented some of the more important design considerations and methods used to cope with them. A description of the overall operation of the converter was given with special emphasis on the more difficult concepts. Several waveforms were photographed and appear here to demonstrate operation of the converter and show the effects of noise. Although design of the circuits is limited in many respects, proper adjustment of the system will yield results which are close to the ideal.

The relationship between SNR ratio and pulse edge jitter (fortuitous distortion) is shown in a qualitative way in Fig. 4.11a and 4.11b.

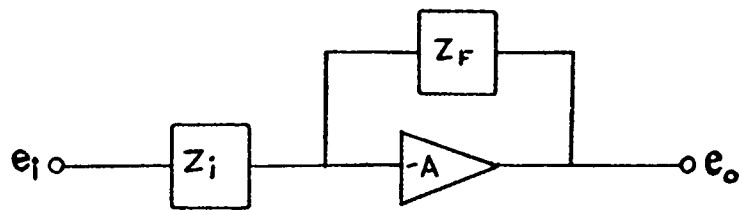


FIG. 4.1 A

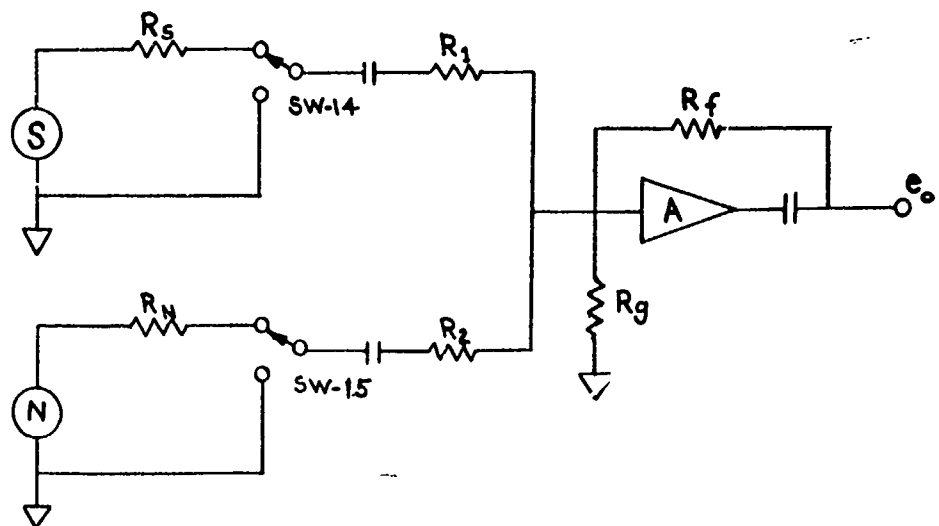


FIG. 4.1 B

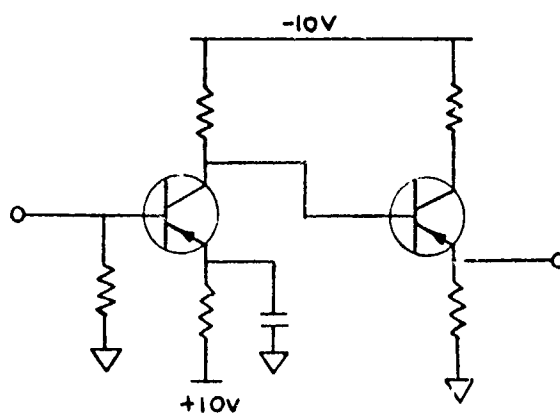
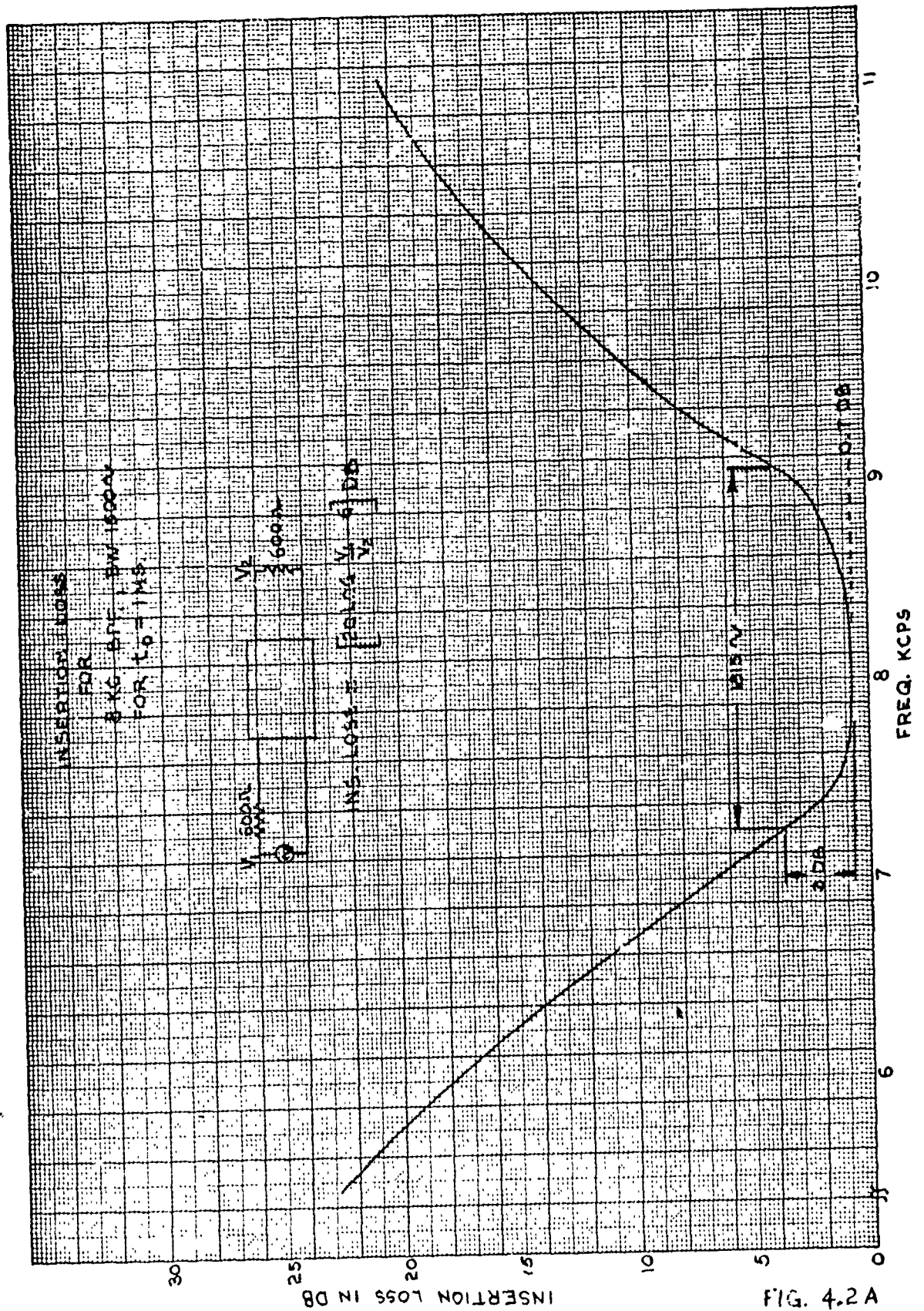
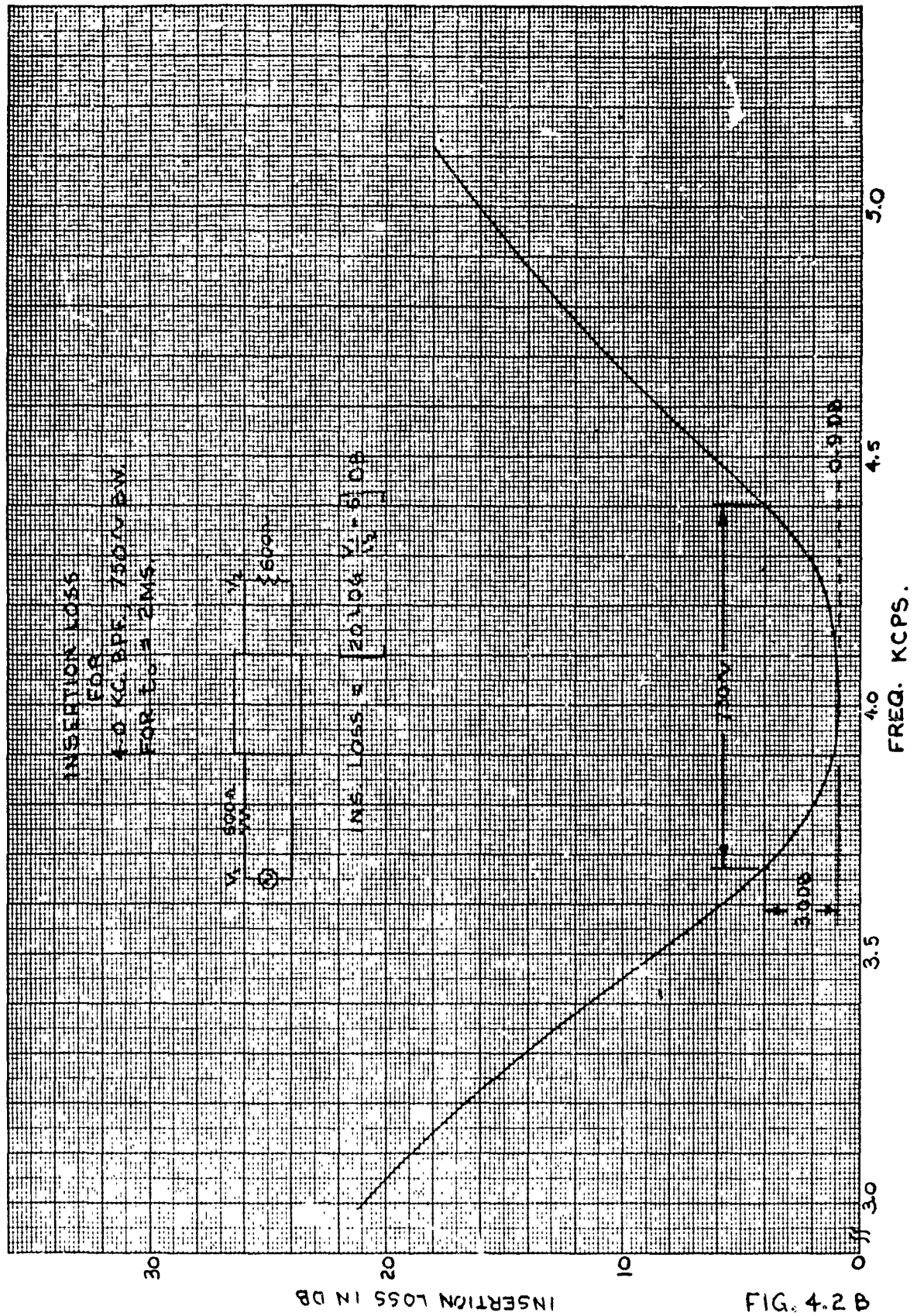
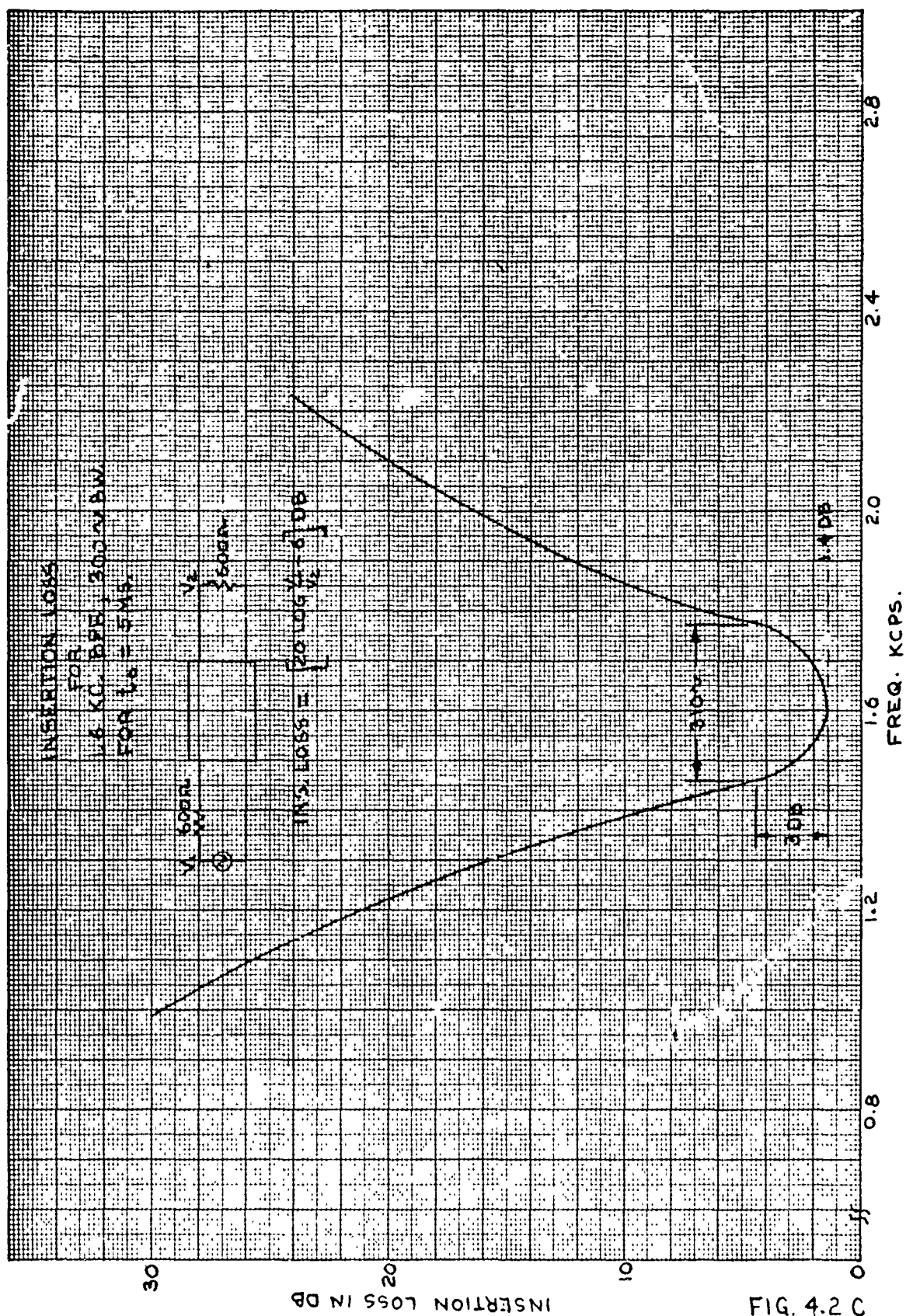
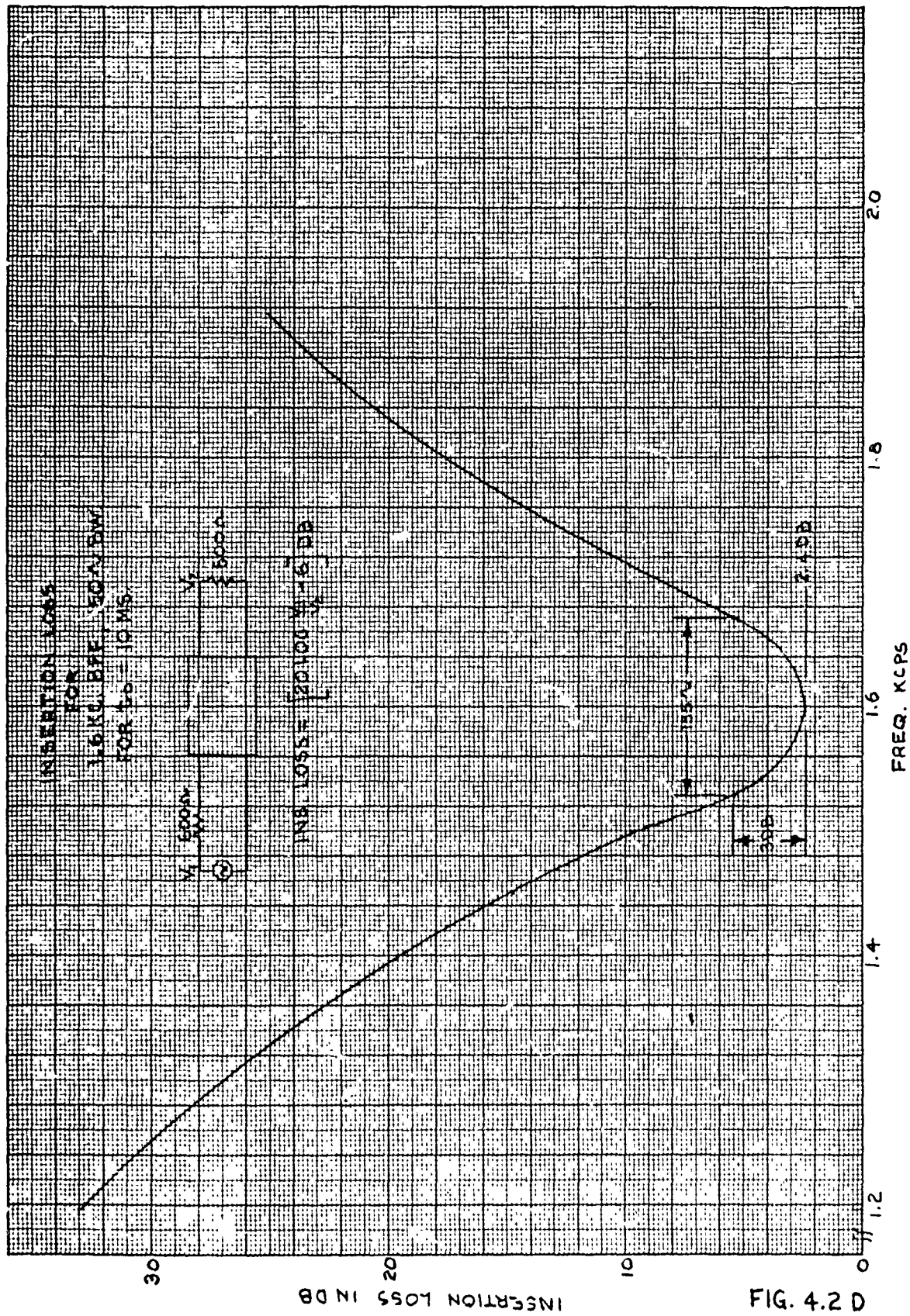


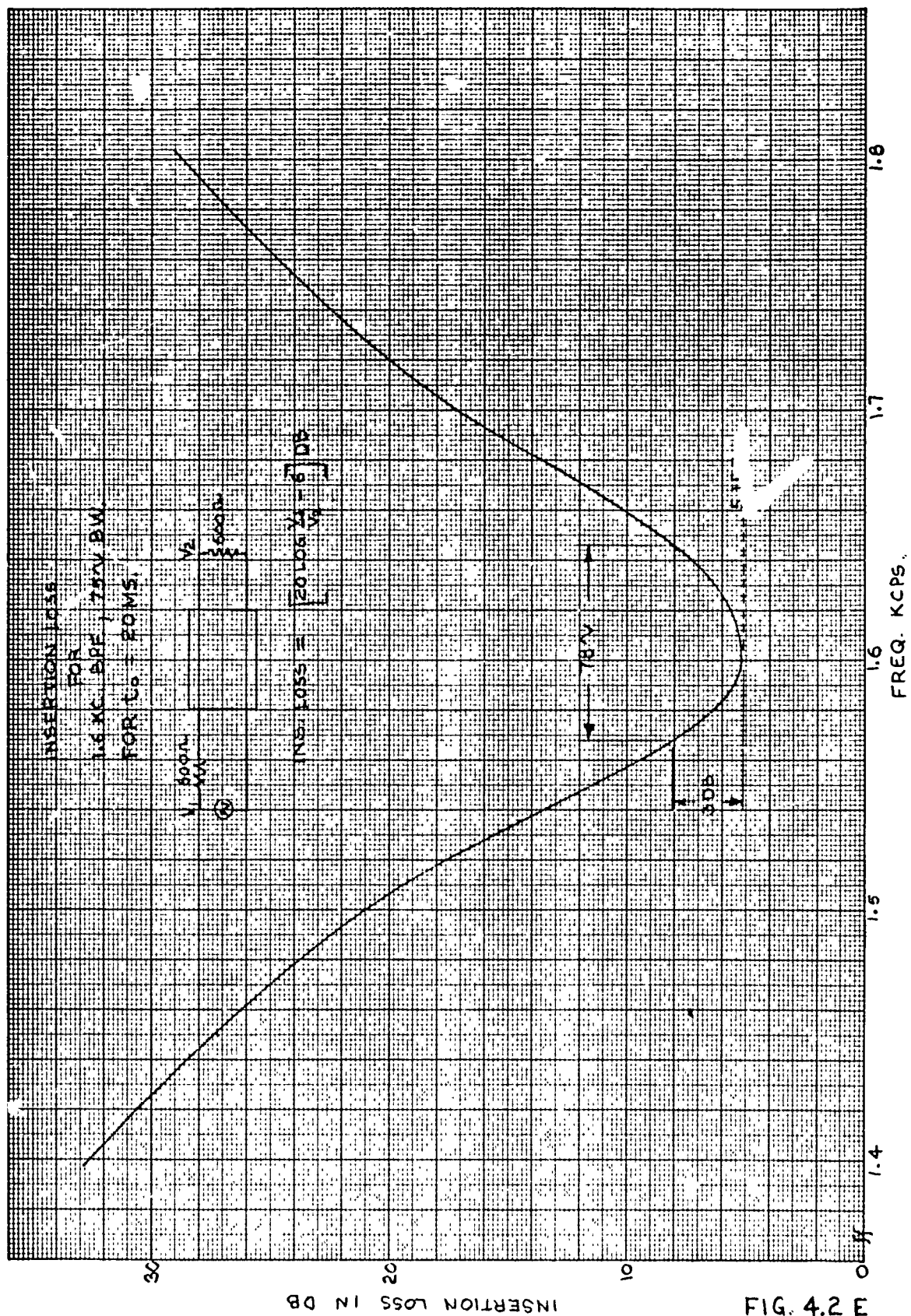
FIG. 4.1 C











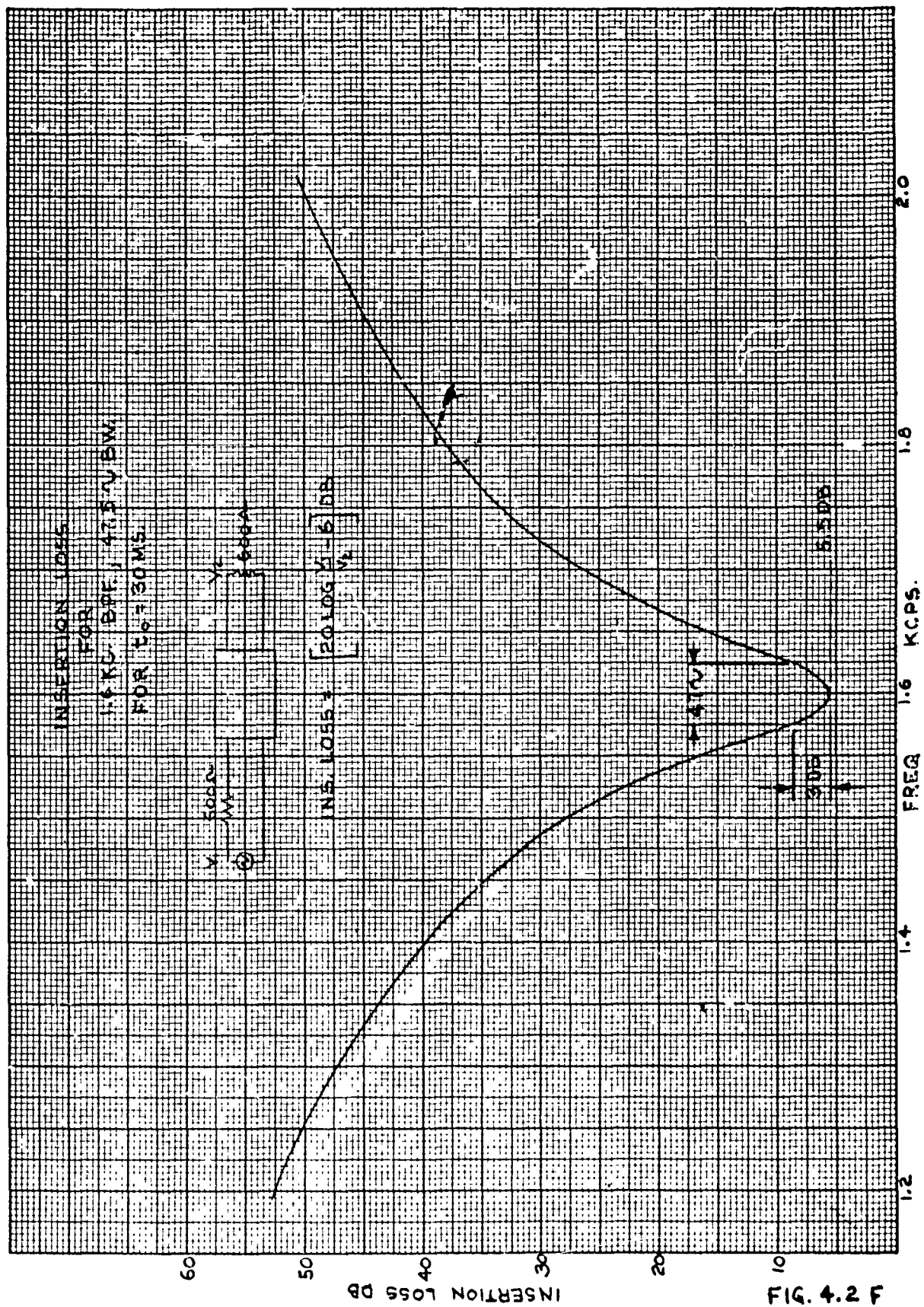


FIG. 4.2 F

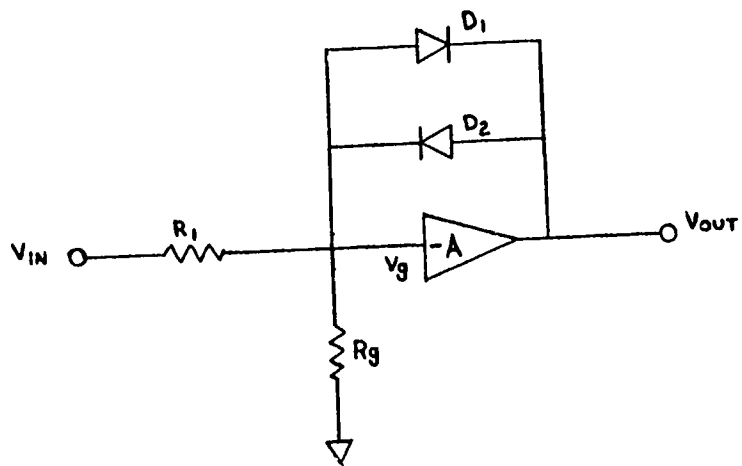


FIG. 4.3 A

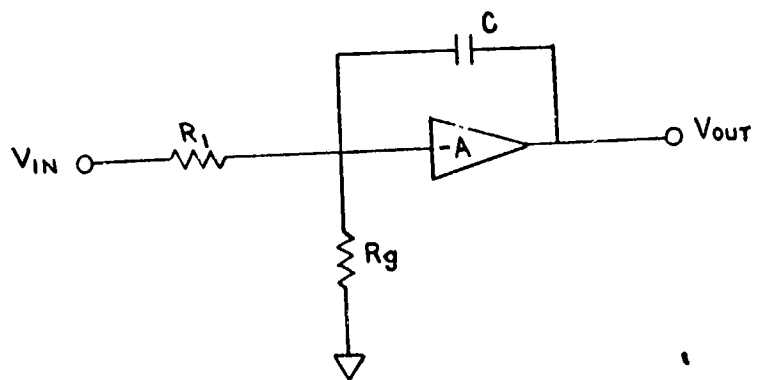


FIG. 4.3 B

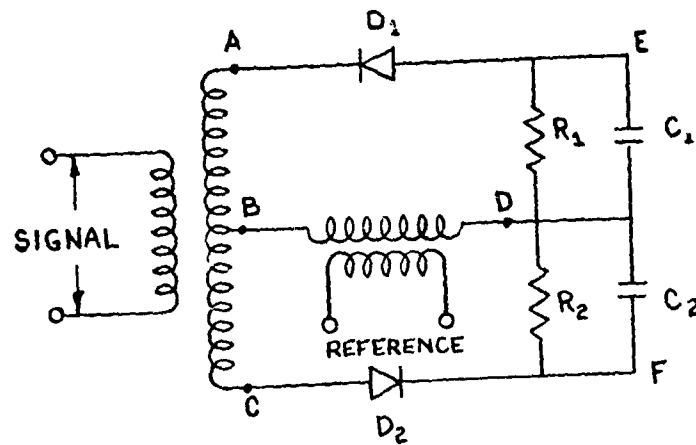


FIG. 4.4 A

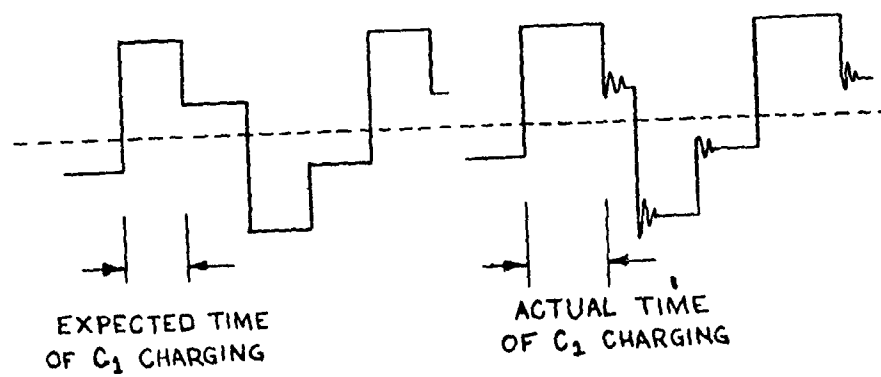
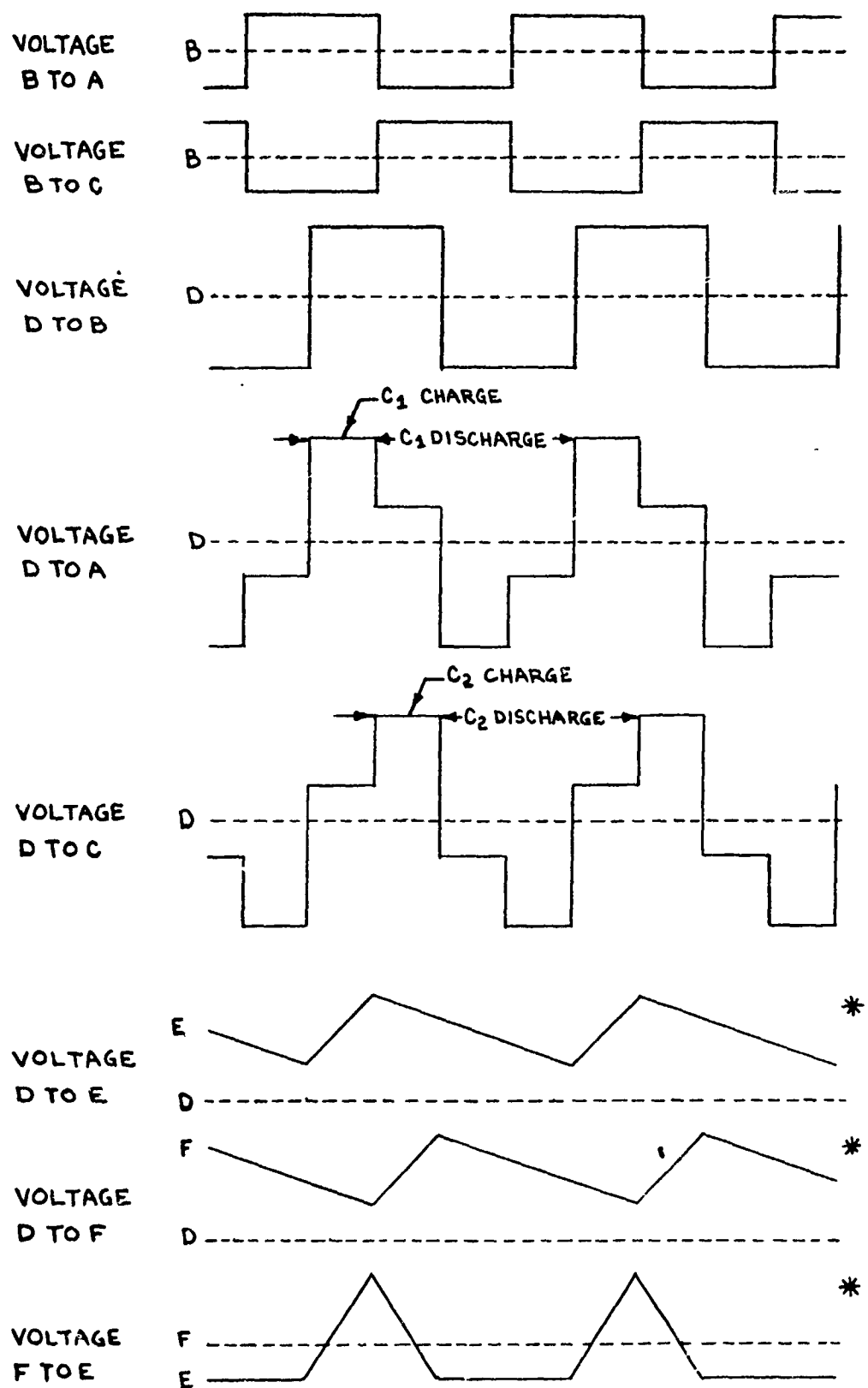


FIG. 4.4 B



* OPTIMIZED WAVEFORMS NOT DRAWN TO SCALE.

Fig. 4.5

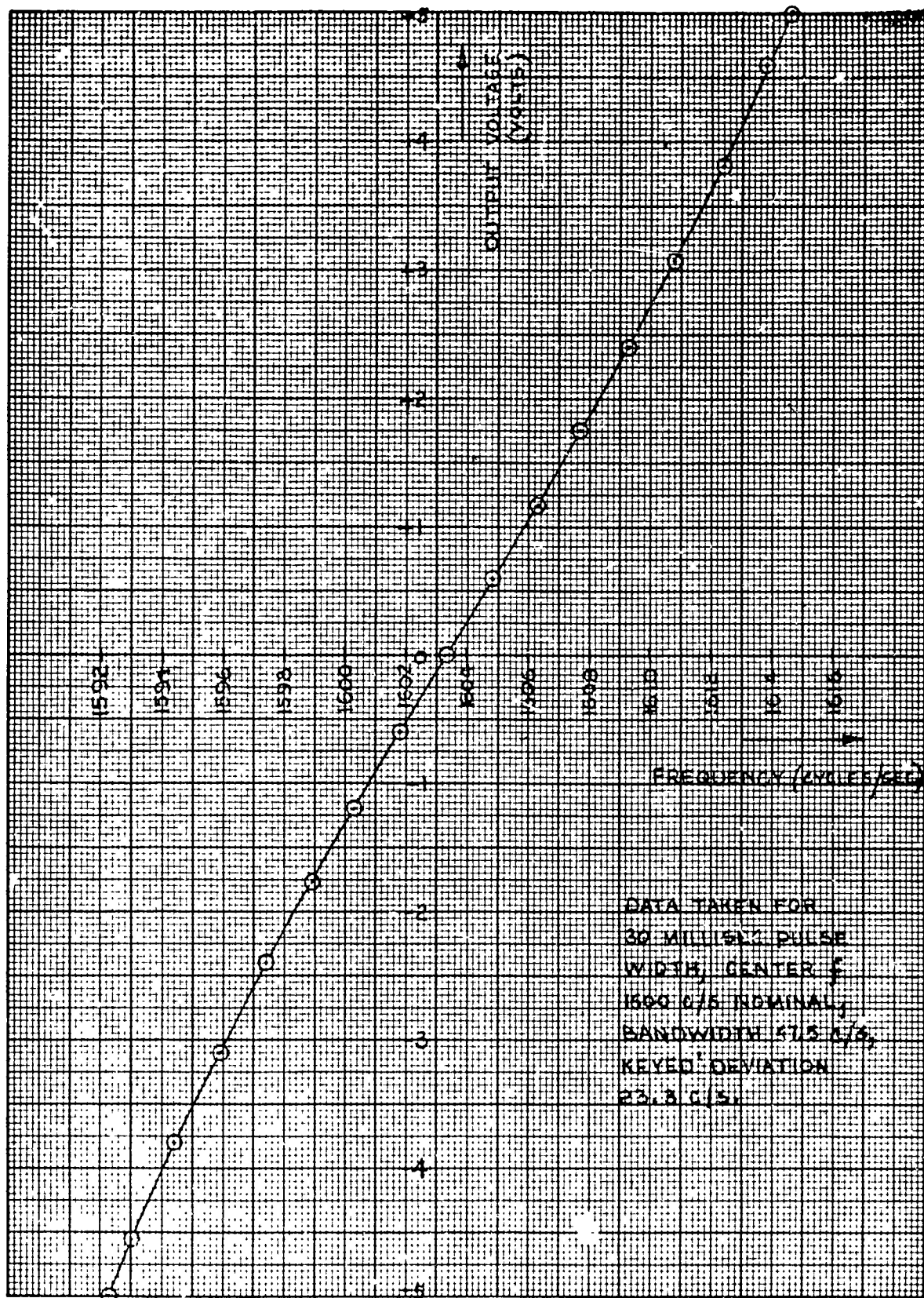


FIG. 4.6

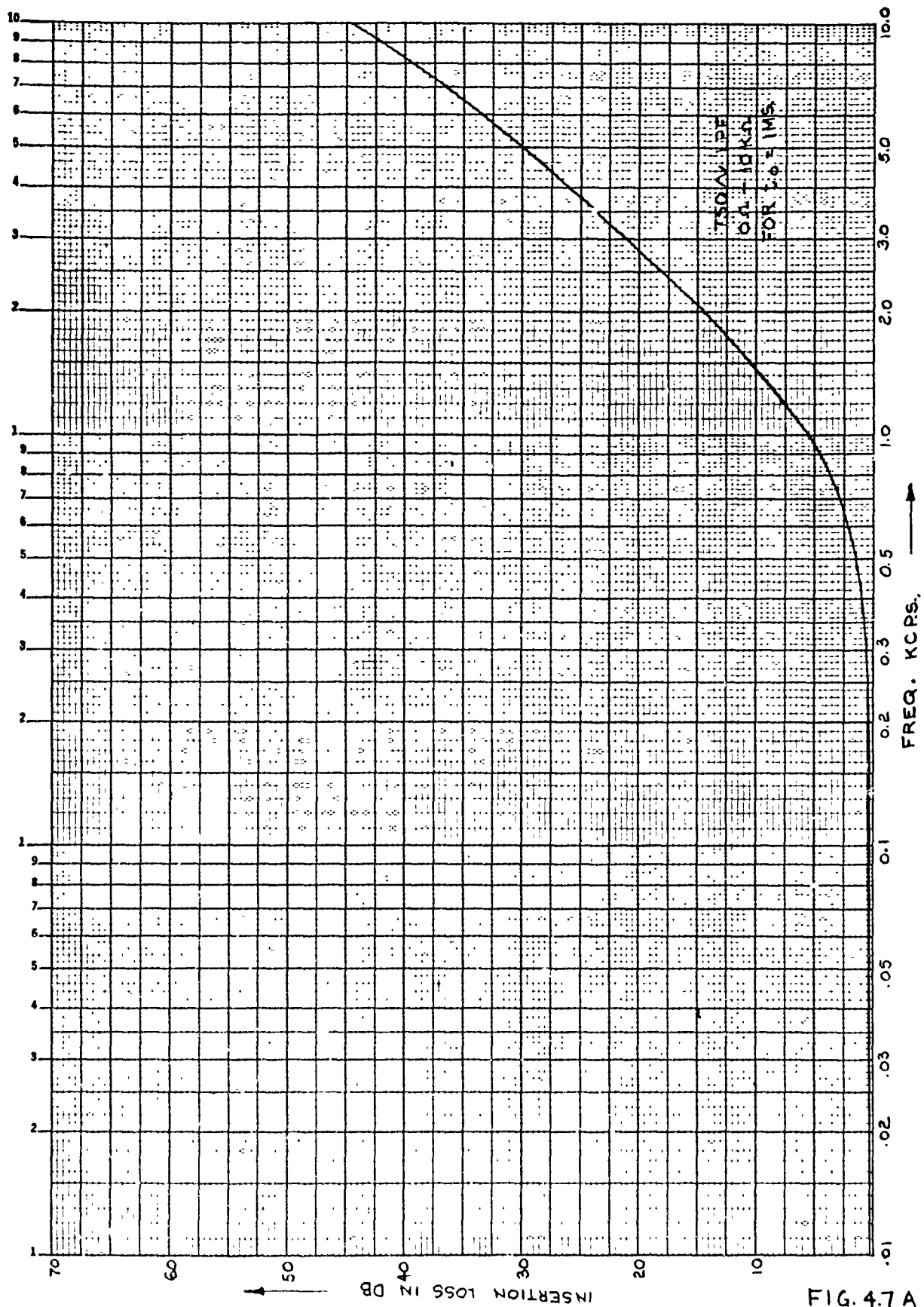


FIG. 4.7A

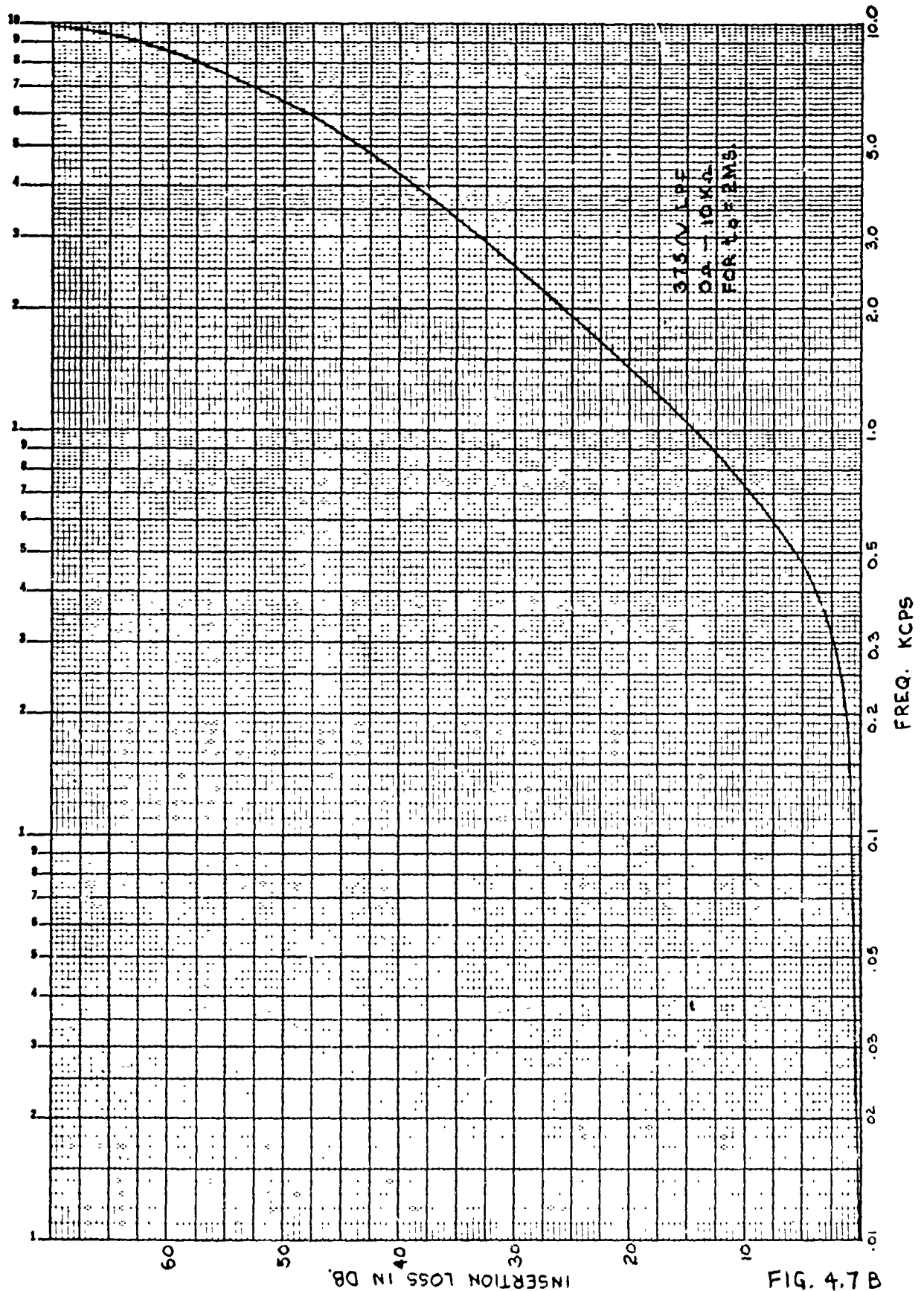


FIG. 4.7 B

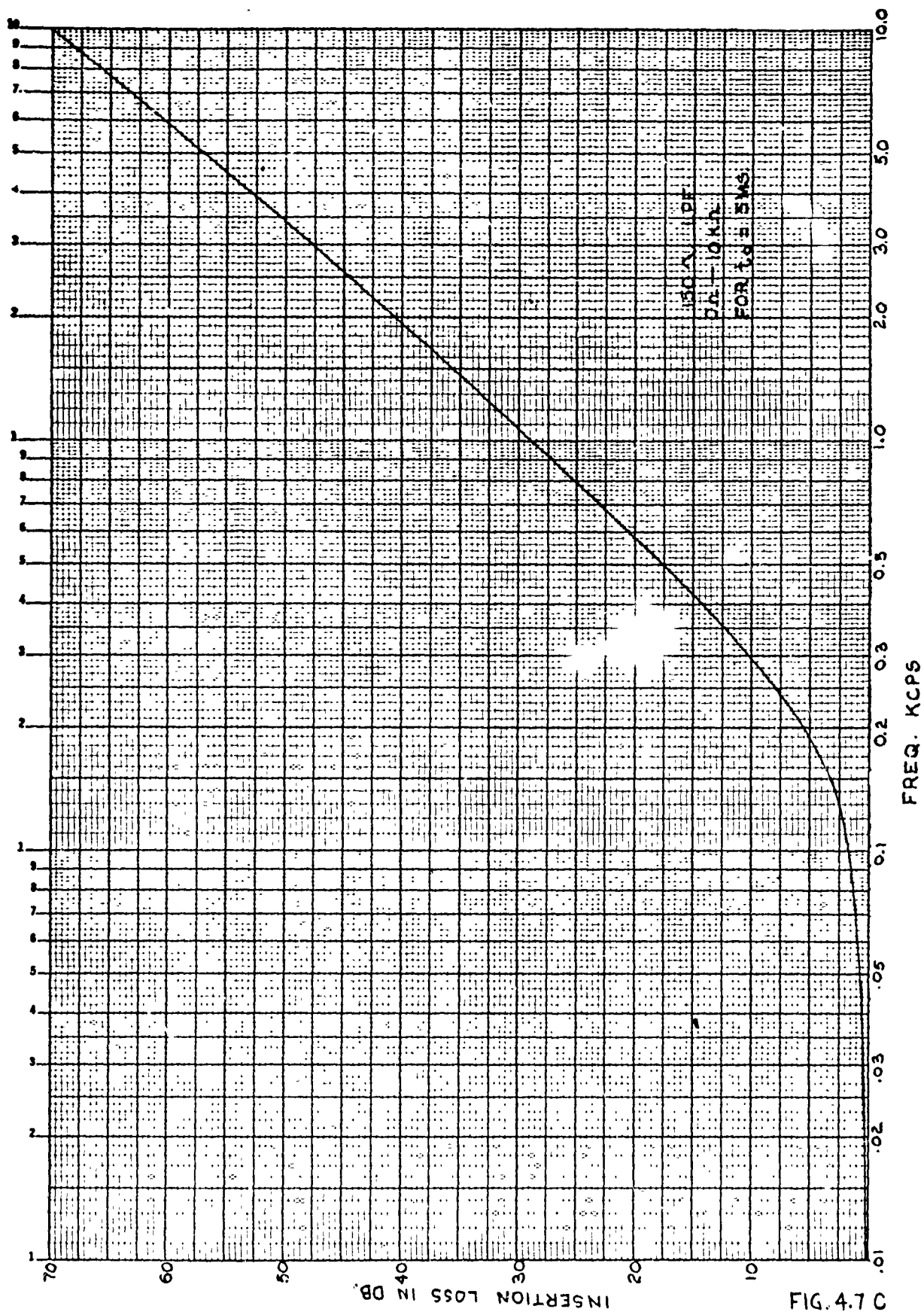
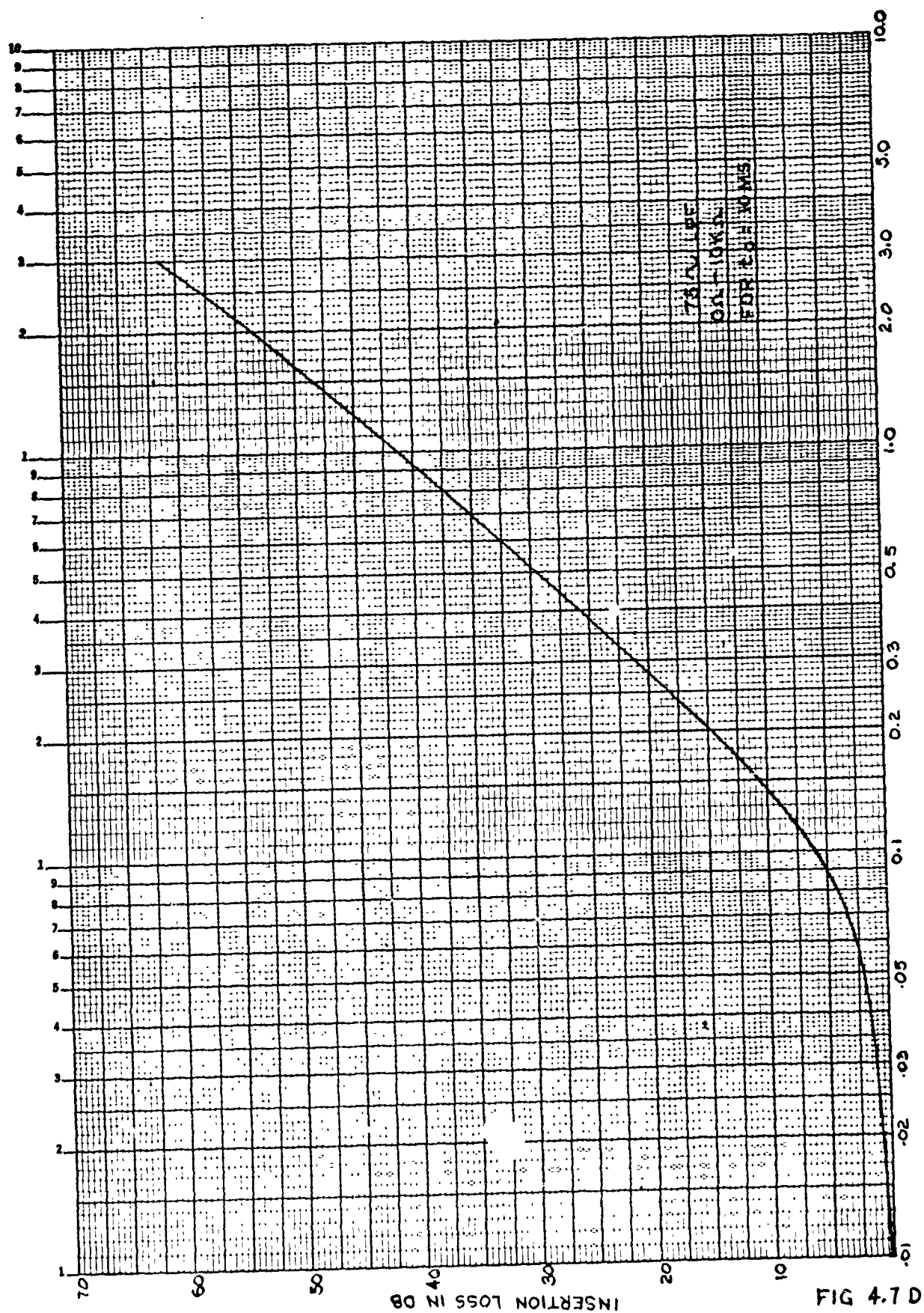


FIG. 4.7 C



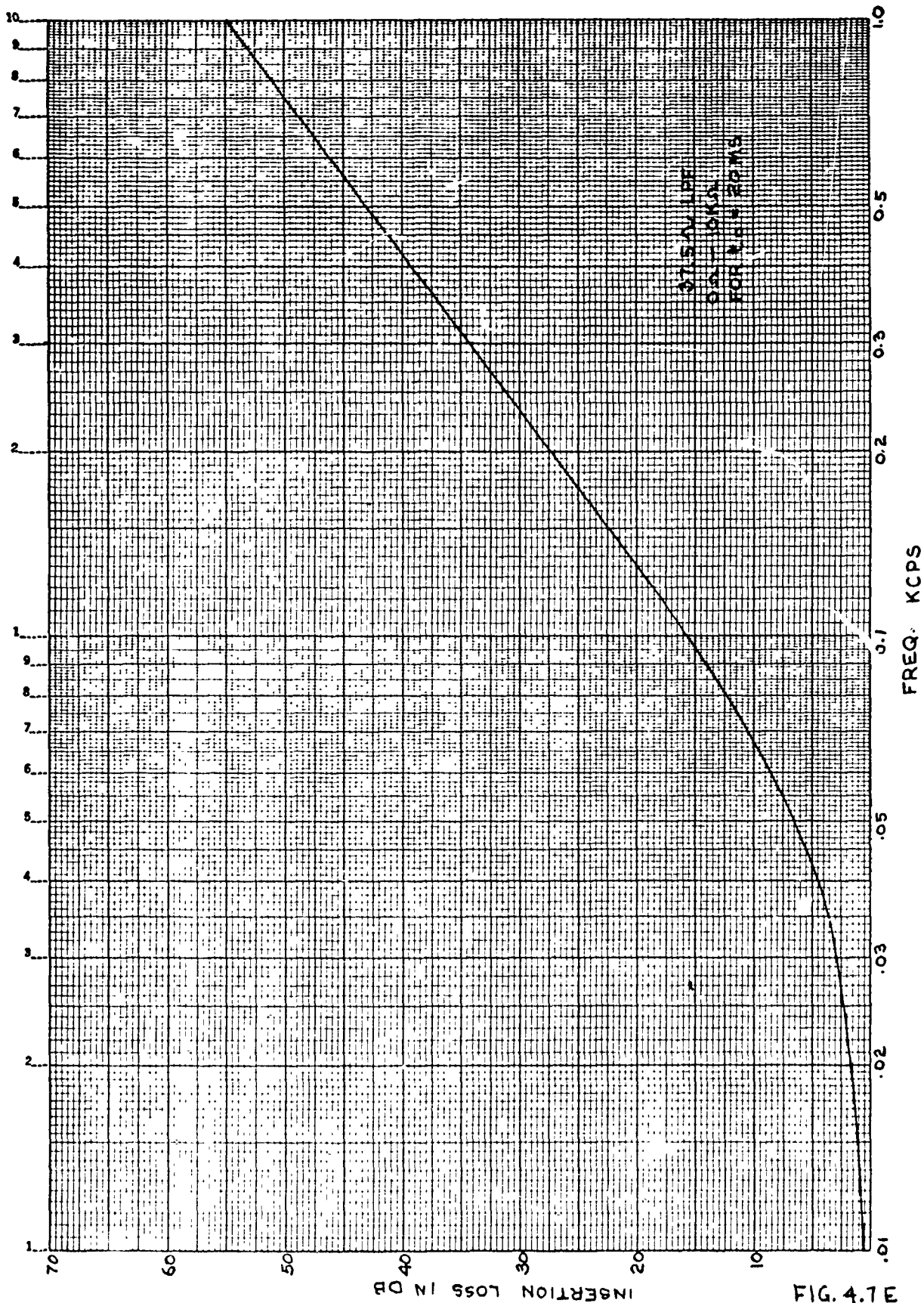
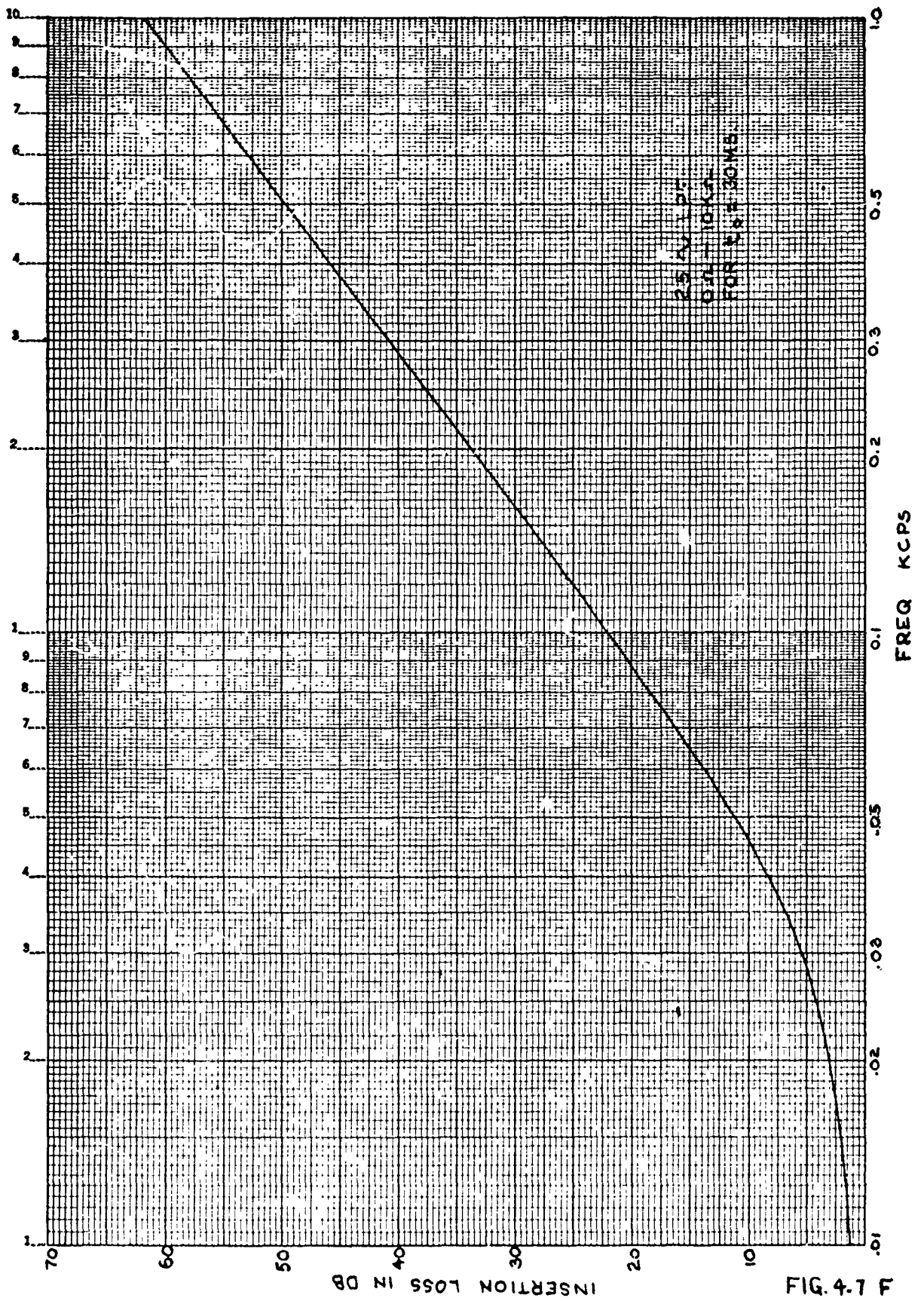
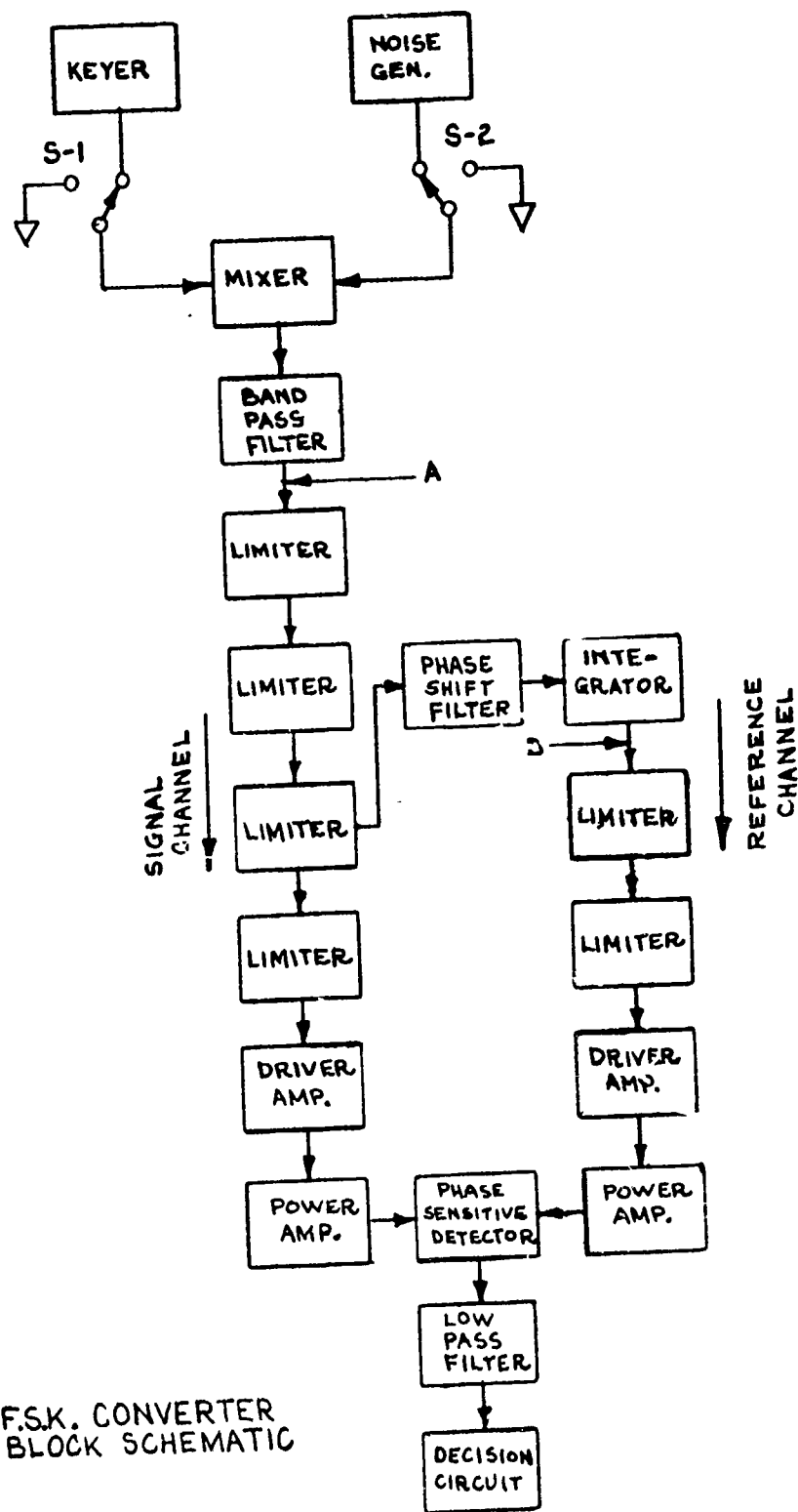


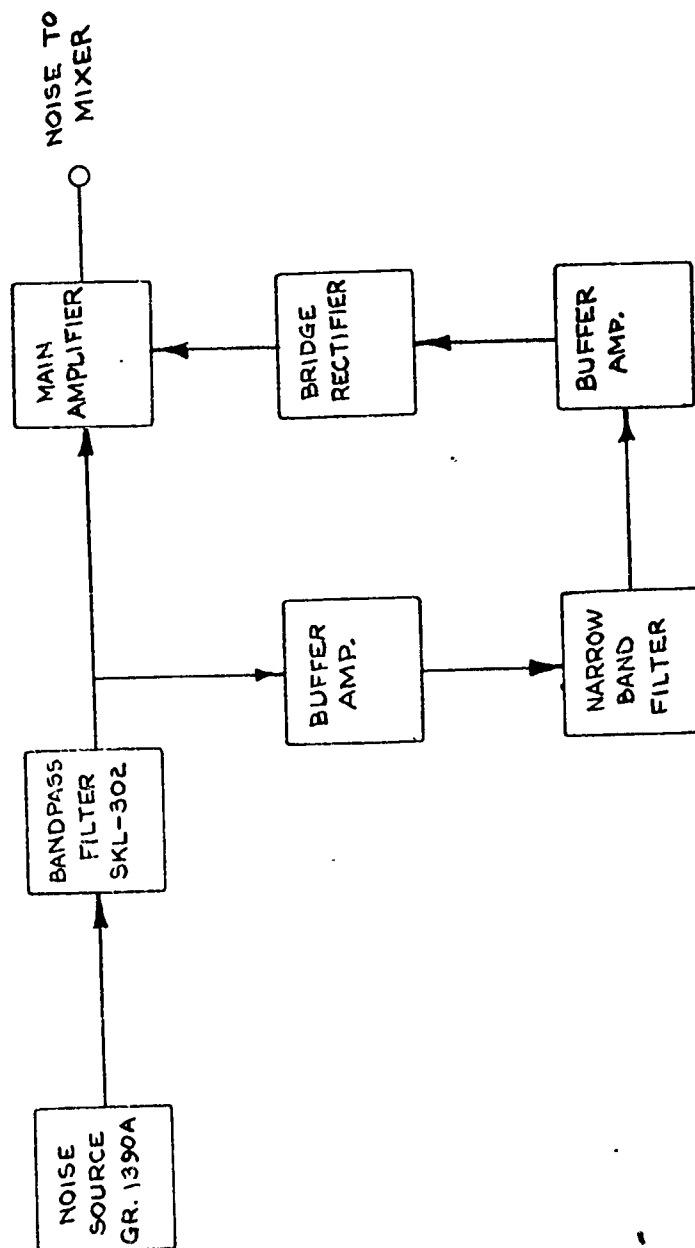
FIG. 4.7E





F.S.K. CONVERTER
BLOCK SCHEMATIC

FIG. 4.8



NOISE FEEDBACK CONTROL

FIG. 4.9

Fig. 4.10 a



Fig. 4.10 b

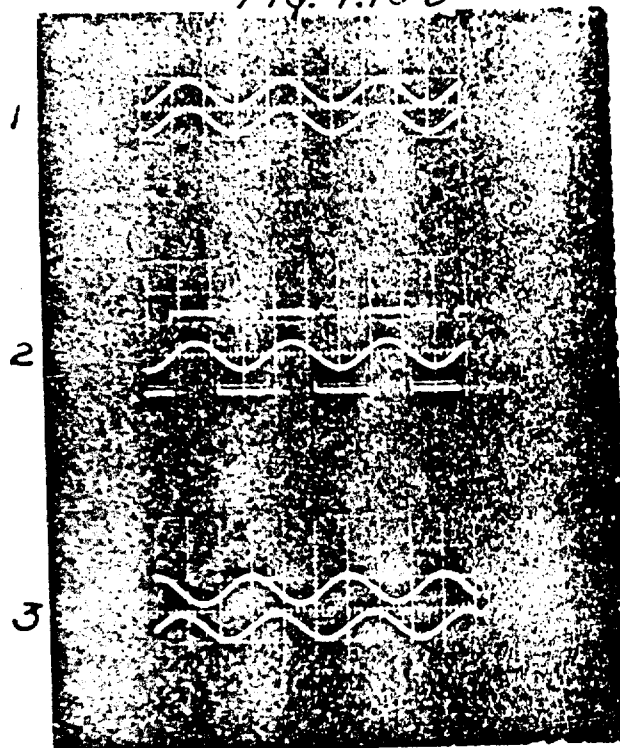


Fig. 4.10 c

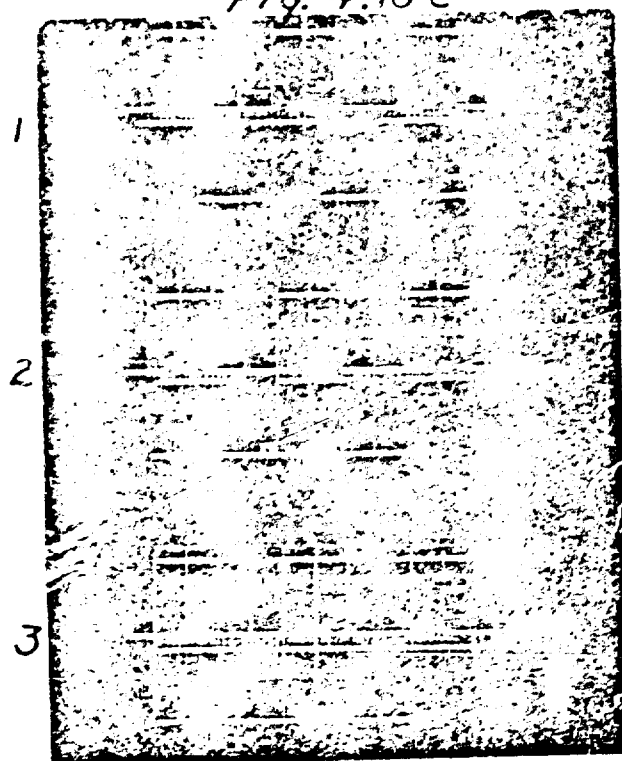


Fig. 4.10 d

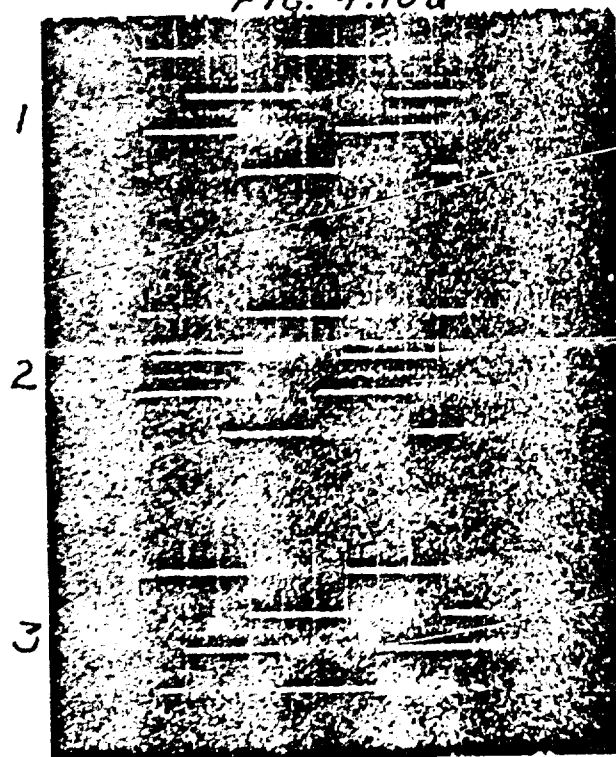


Fig 4.11a

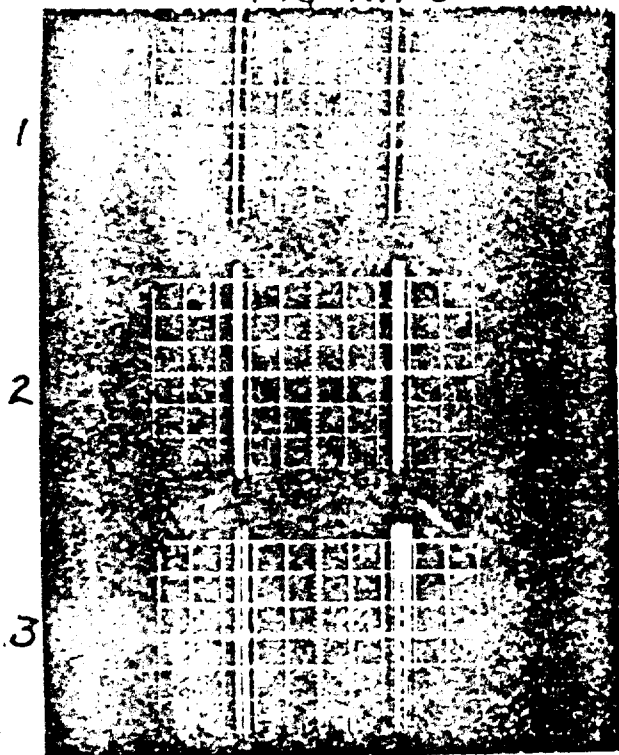


Fig. 4.11b

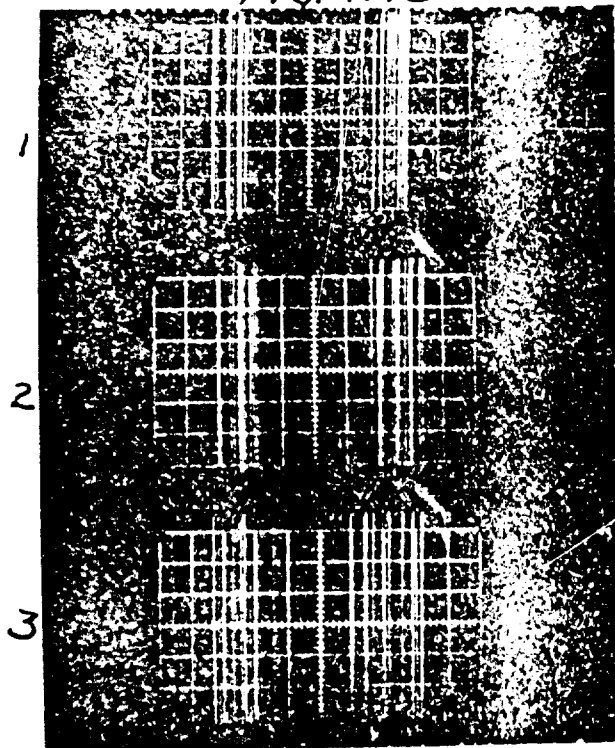


Fig. 4.11c

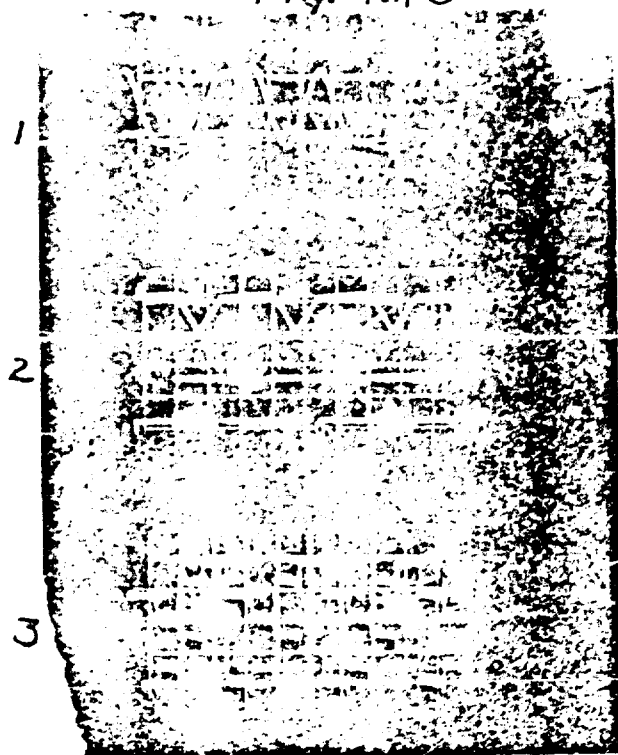


Fig. 4.11d

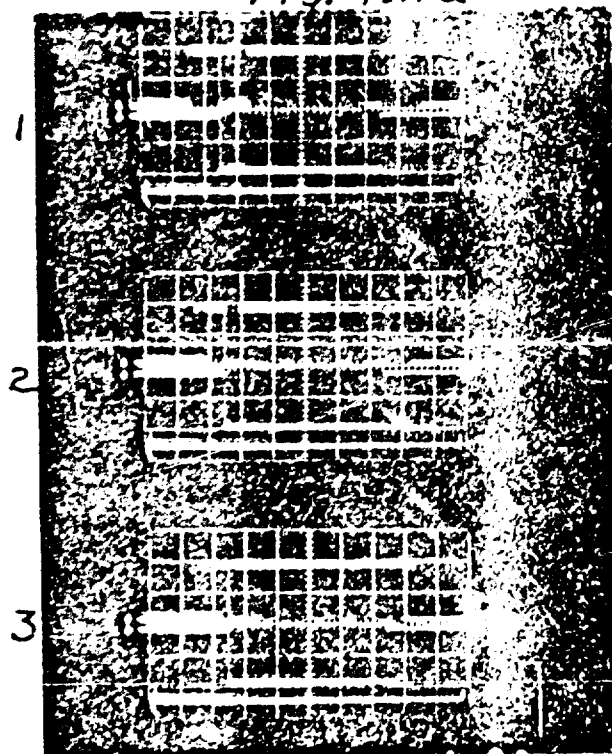


FIG. 4.12 a

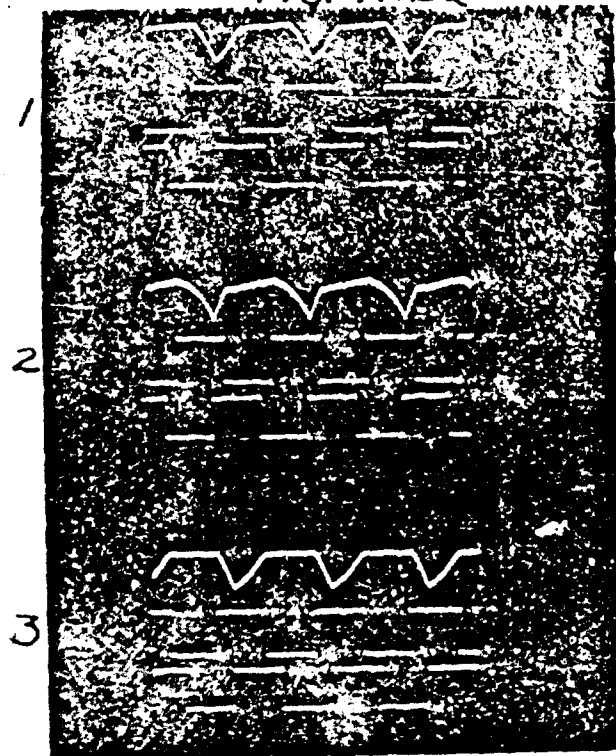
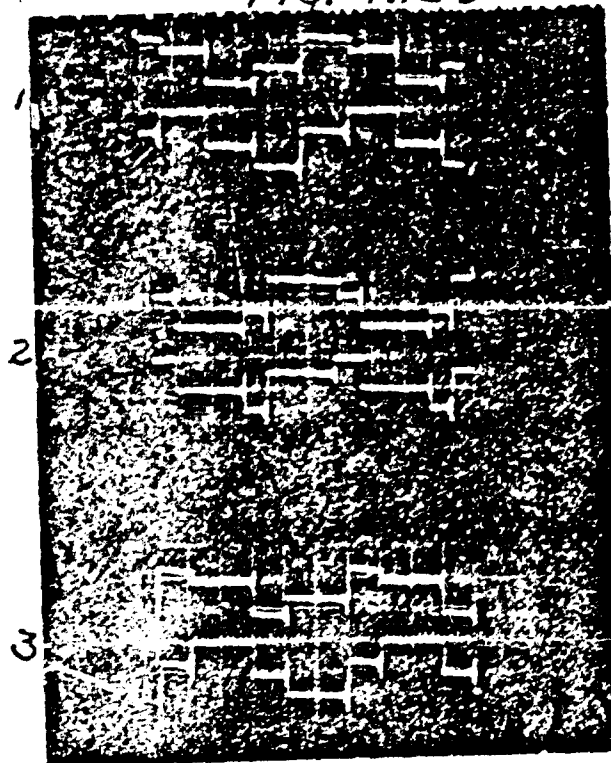
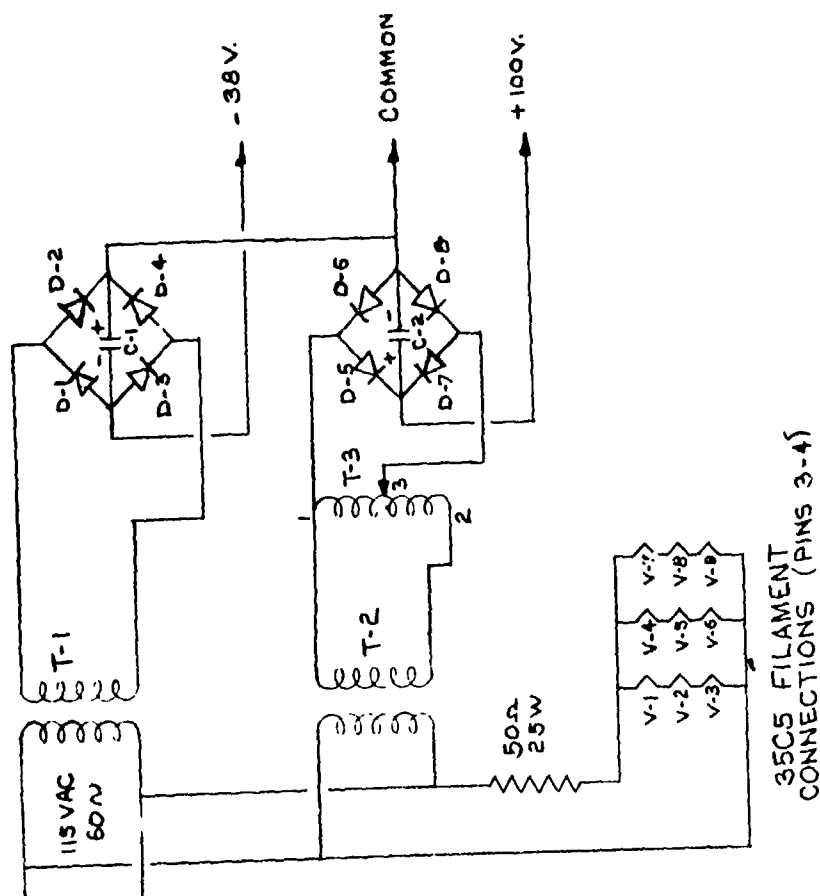


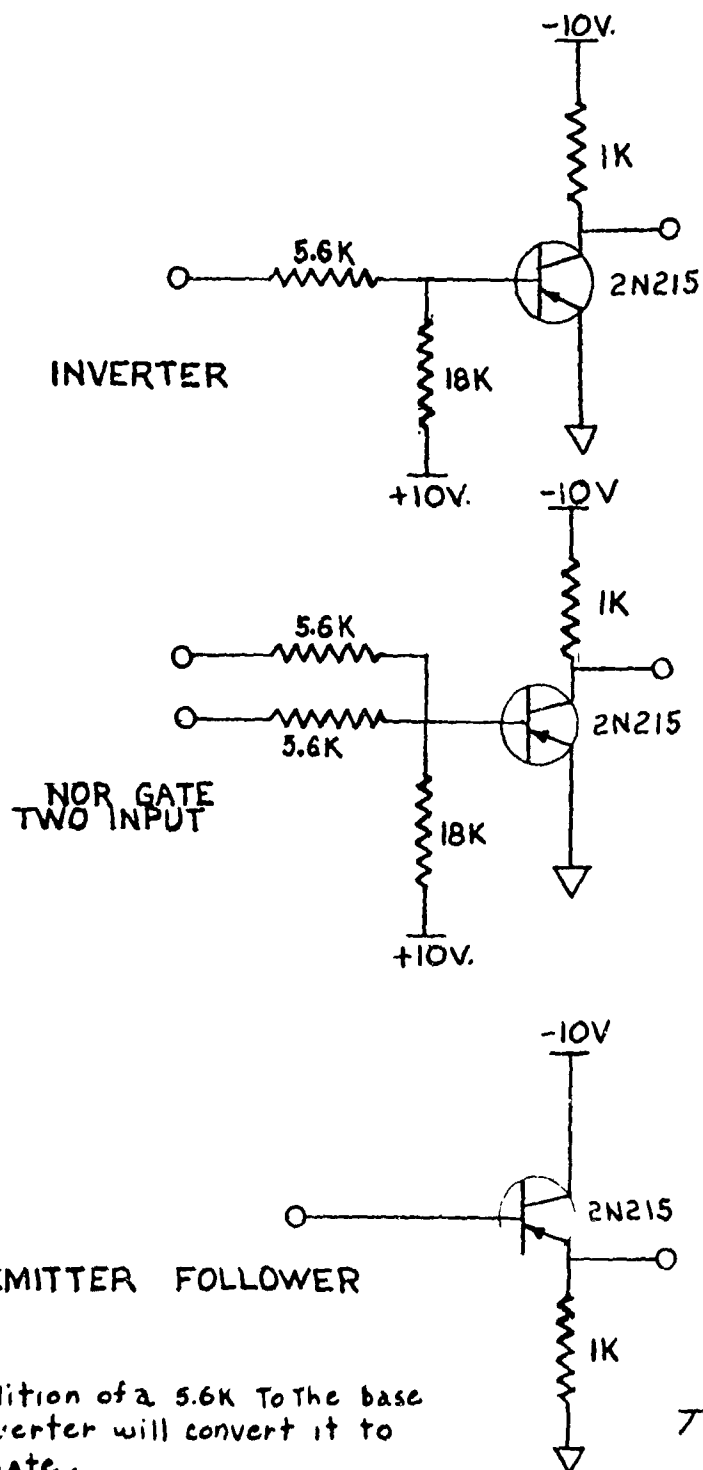
FIG. 4.12 b





TEST FACILITY
M.C. POWER SUPPLY

C-1	400 MFD.
C-2	25.2V.
T-1	P6410 STANCOR ISOLATION TRANSFORMER 115V. TO 115V. 60W. 30VA.
T-2	P6469 STANCOR FILAMENT TRANSFORMER PRI. 117V. 60W SEC. 25.2V. @ 1AMP.
T-3	POWERSTAT TYPE 10B SUPERIOR ELECTRIC CO. 120V. 50/60W 1-2 0-120V 1.75A. 1-3
D-1	RECTIFIER TYPE F-4
D-8	SARKES TARZIAN



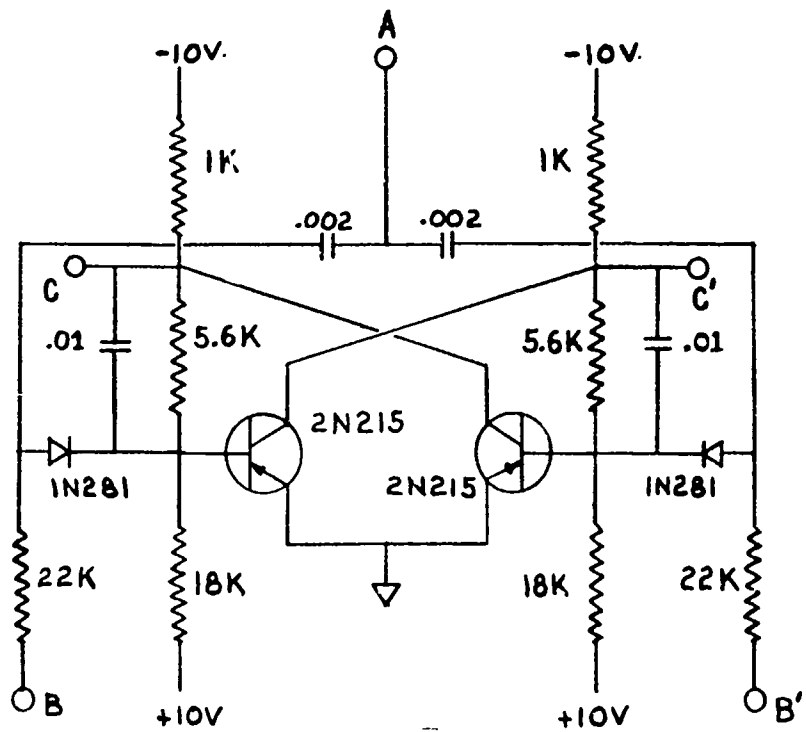
NOTE

The addition of a 5.6K To The base of an inverter will convert it to a Nor Gate.

The possible combinations for card S-2 are:

- (1) Two inverters
- (2) inverter - nor gate
- (3) Two nor gates
- (4) Any combination of inverters, nor gates, or emitter followers.
- (5) Special transistors or requirements will be so marked. S-2

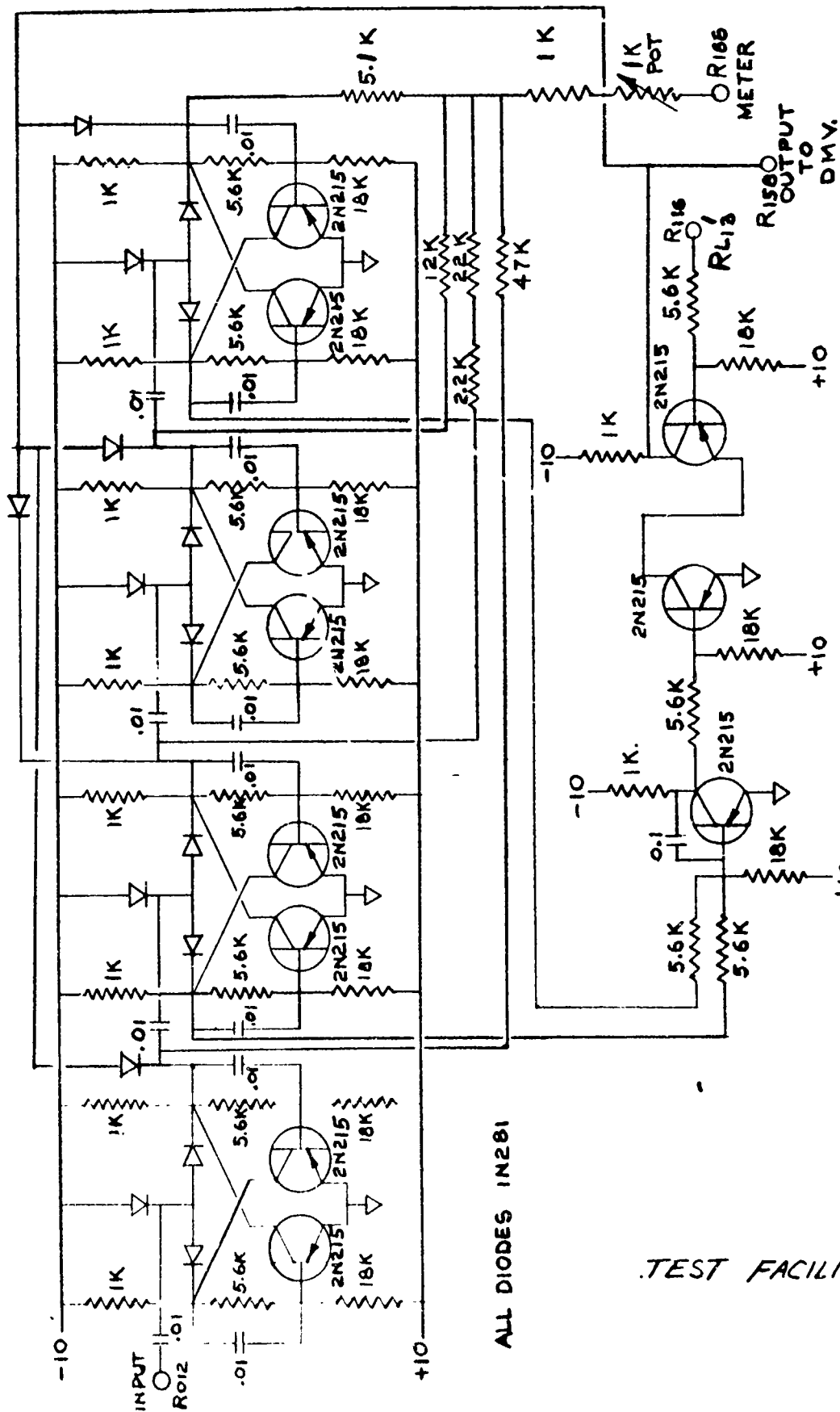
TEST FACILITY

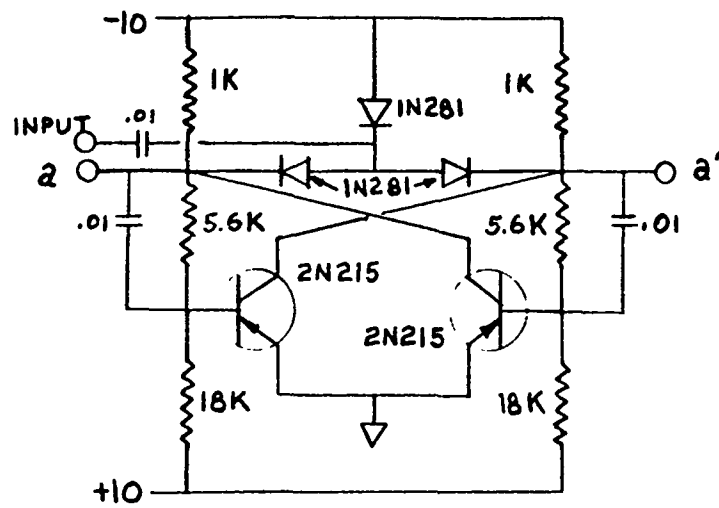


SHIFT REGISTER

TEST FACILITY

S-3

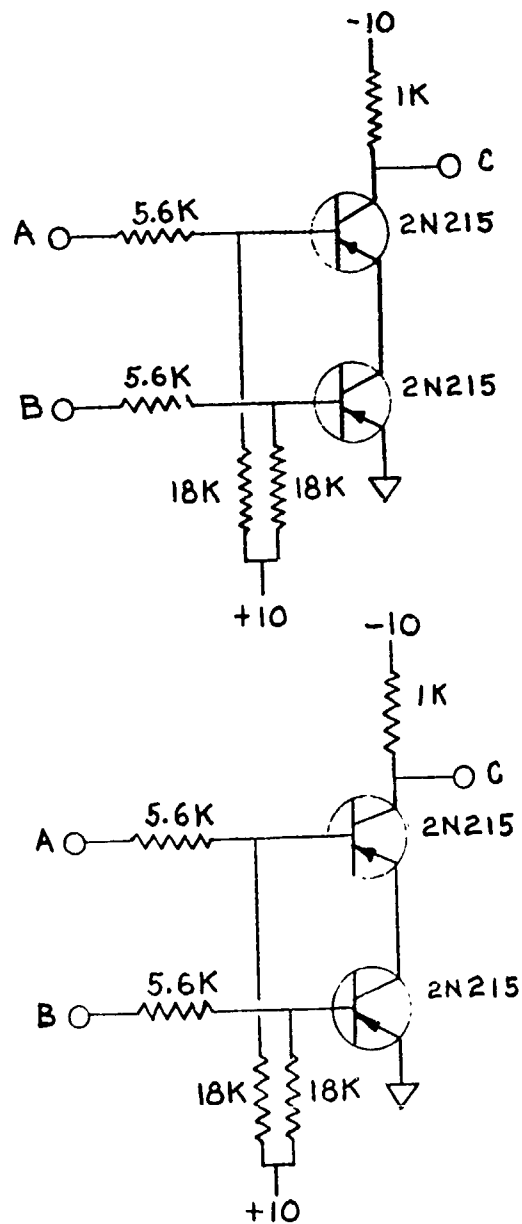




DIVIDE BY 2

TEST FACILITY

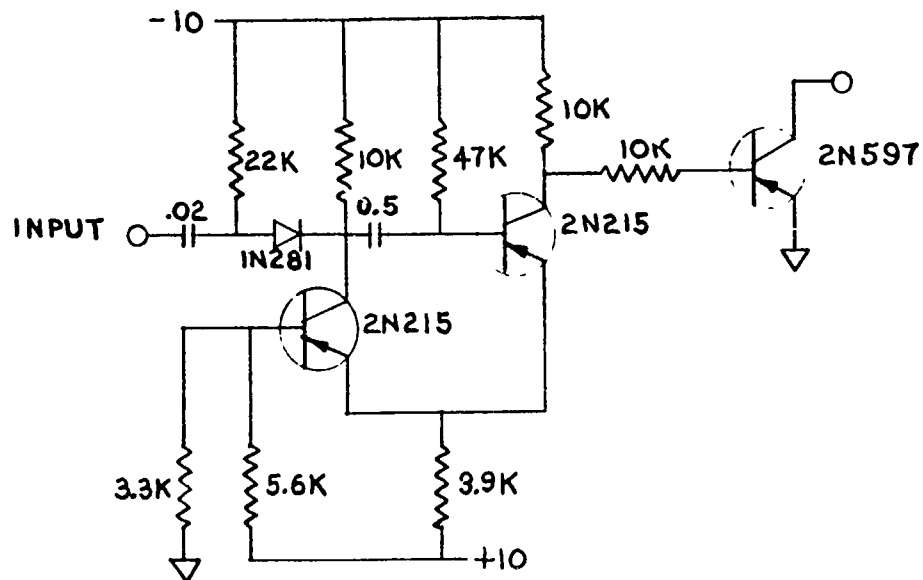
S-5



AND TRANSISTOR GATES (TWO)

TEST FACILITY

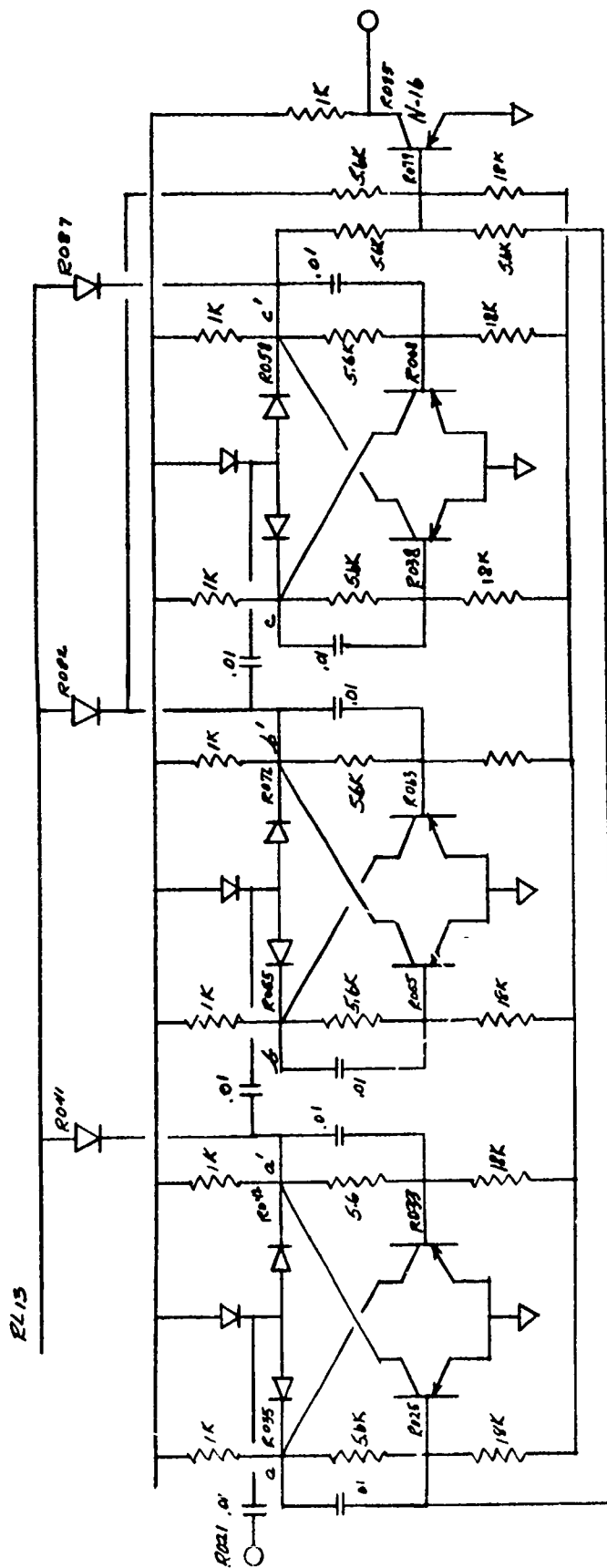
S-6



DMV. AND DRIVER

TEST FACILITY

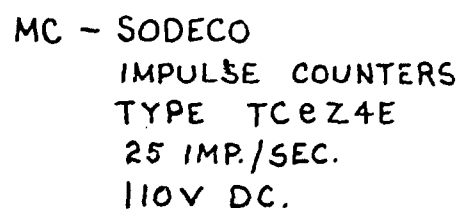
S-7



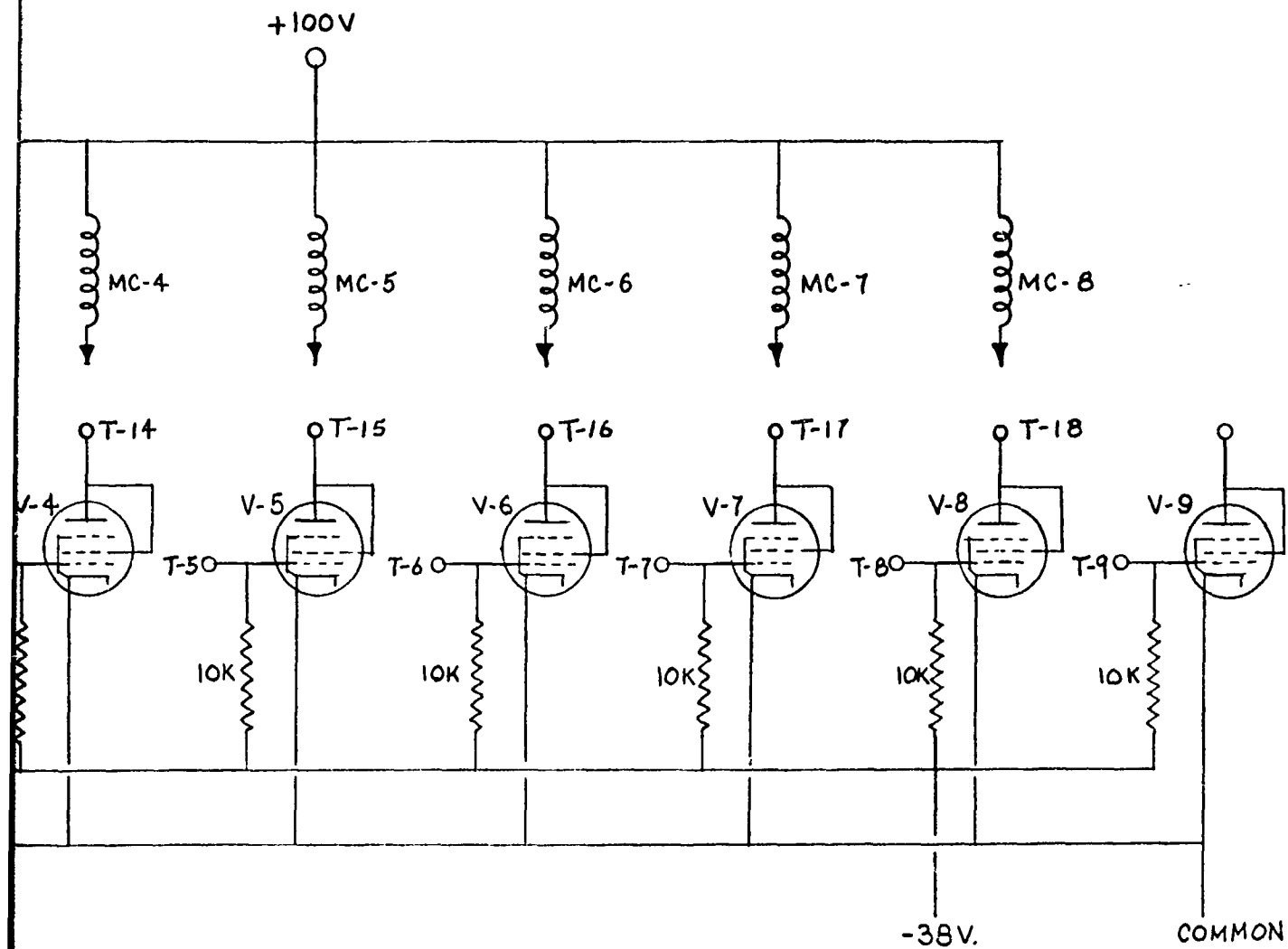
TEST FACILITY

÷ 8 + 1 NOR

S-8

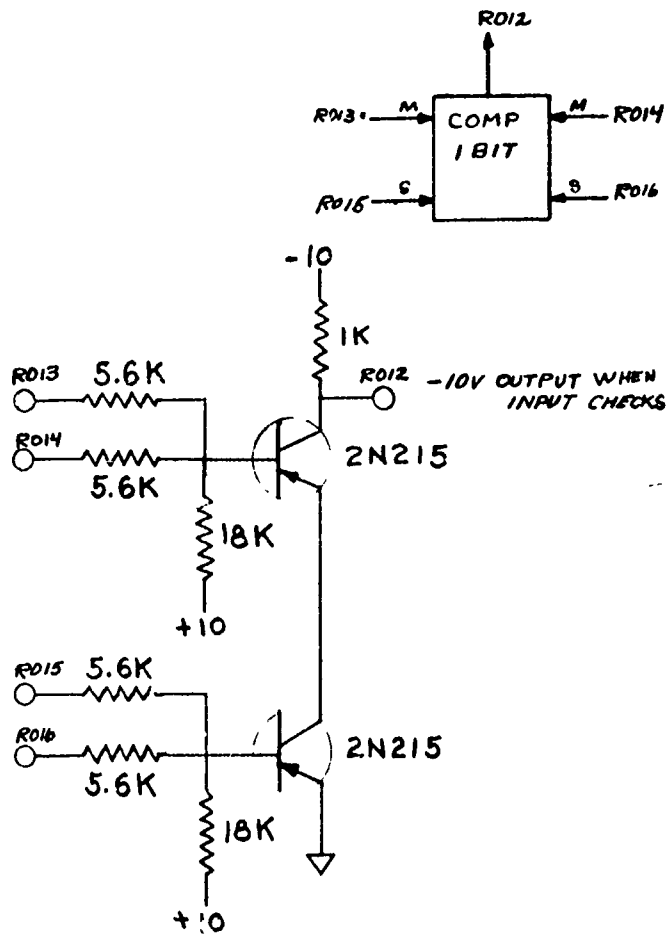


T - TERMINAL STRIP



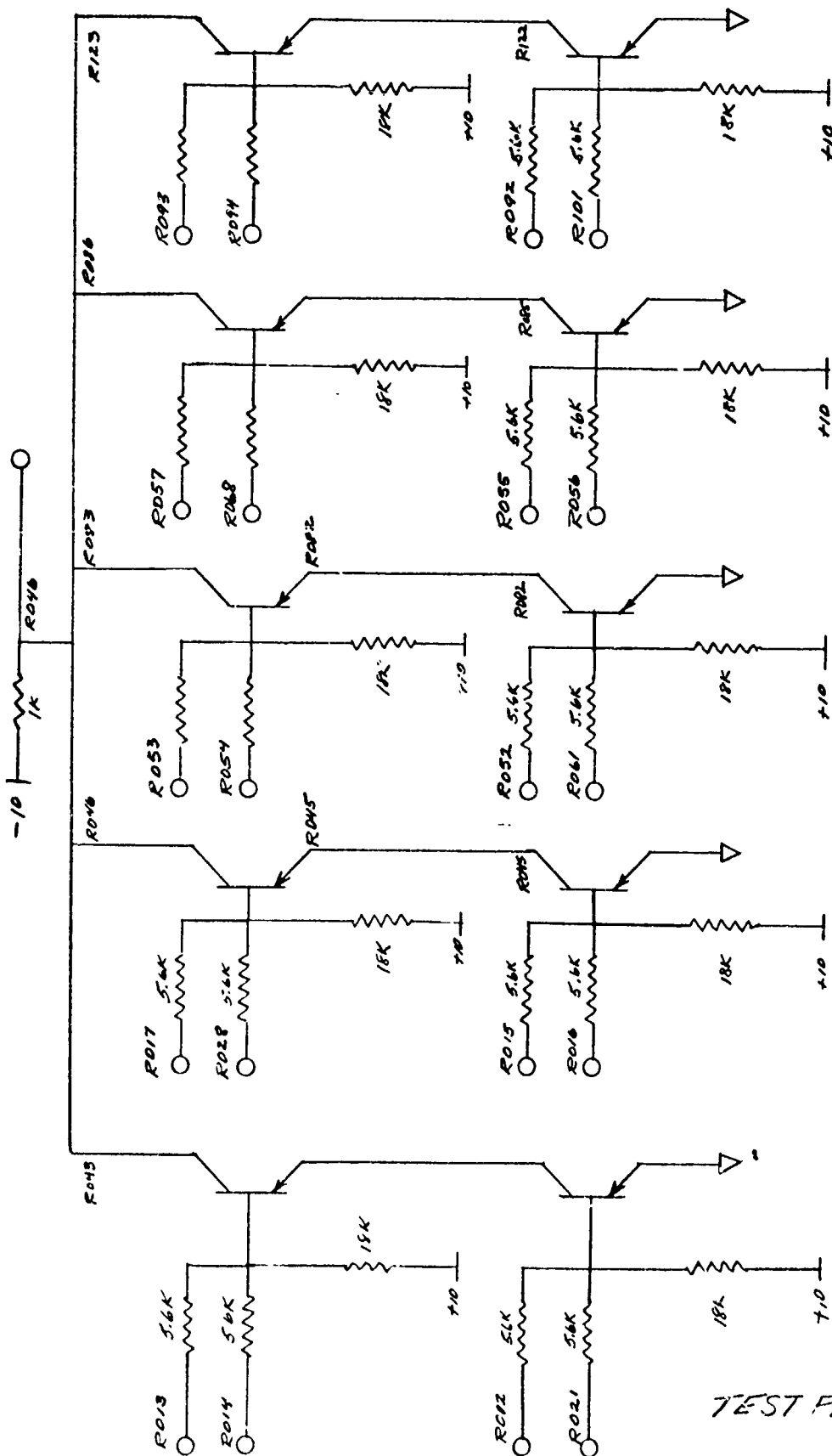
TEST FACILITY
MECHANICAL COUNTER UNIT

S-9



COMPARATOR 1 BIT

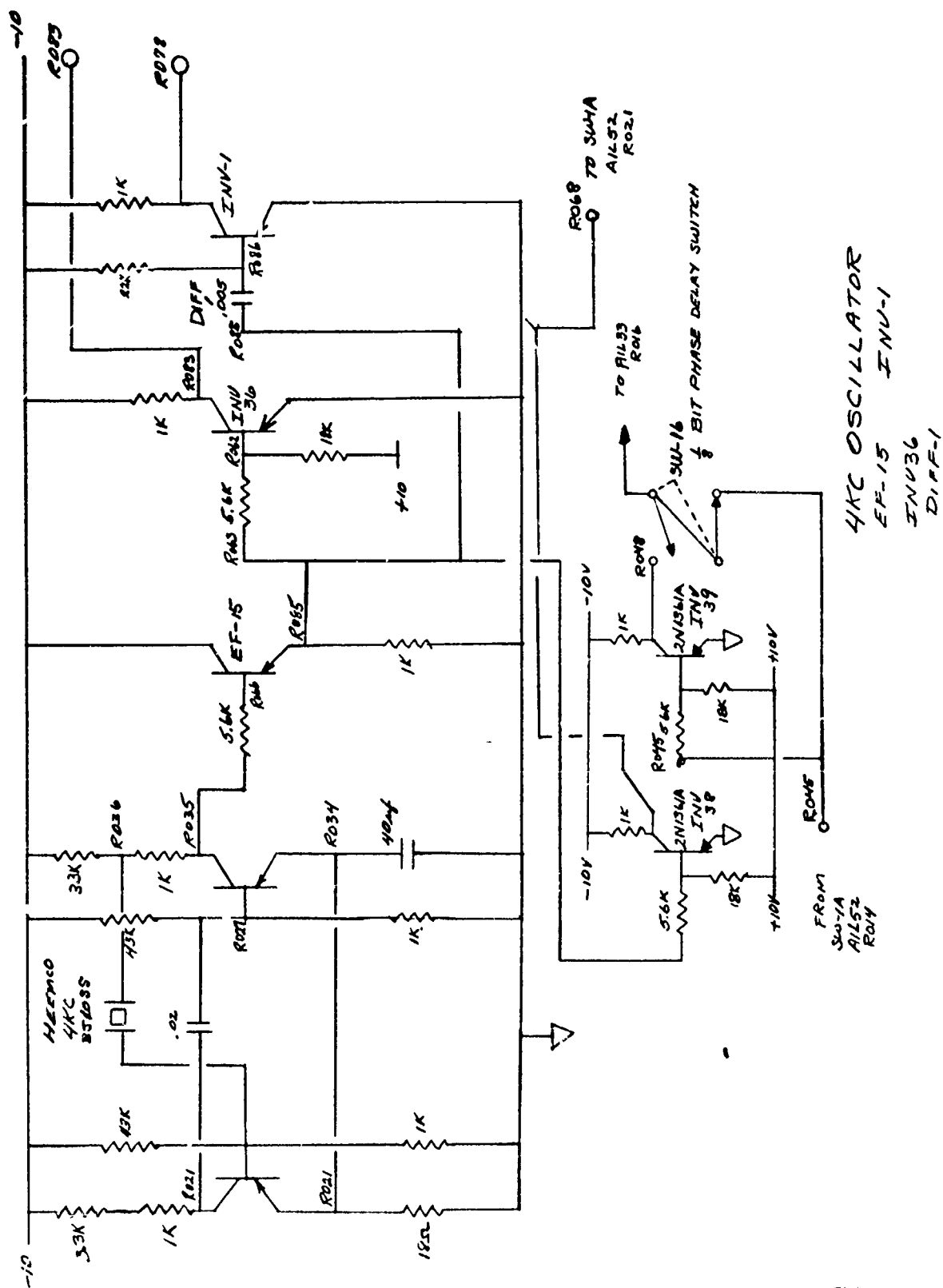
TEST FACILITY



COMPARATOR 5 BIT

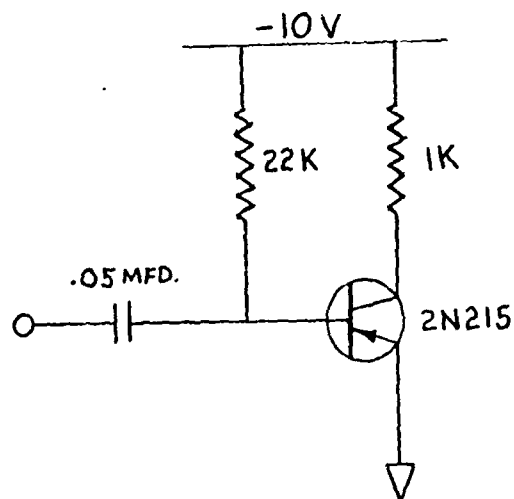
TEST FACILITY

S-11





VARIABLE DMV.



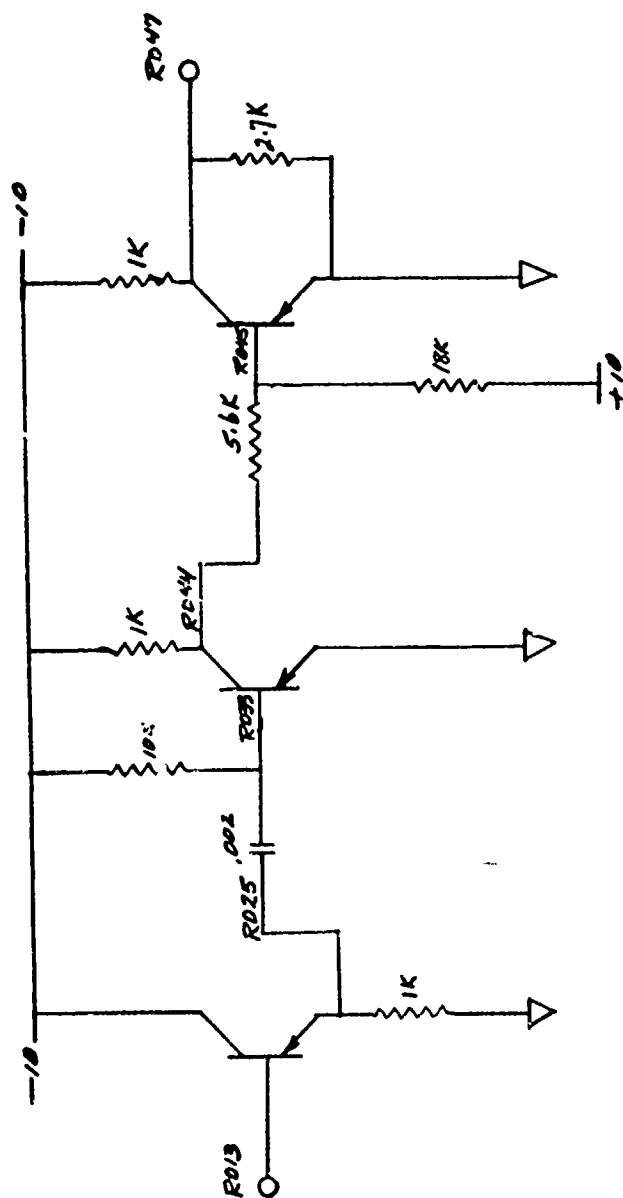
DIFFERENTIATOR

NOTE

The rest of the circuits, which are labeled S-14, can be found by referring to the appropriately named schematics

TEST FACILITY

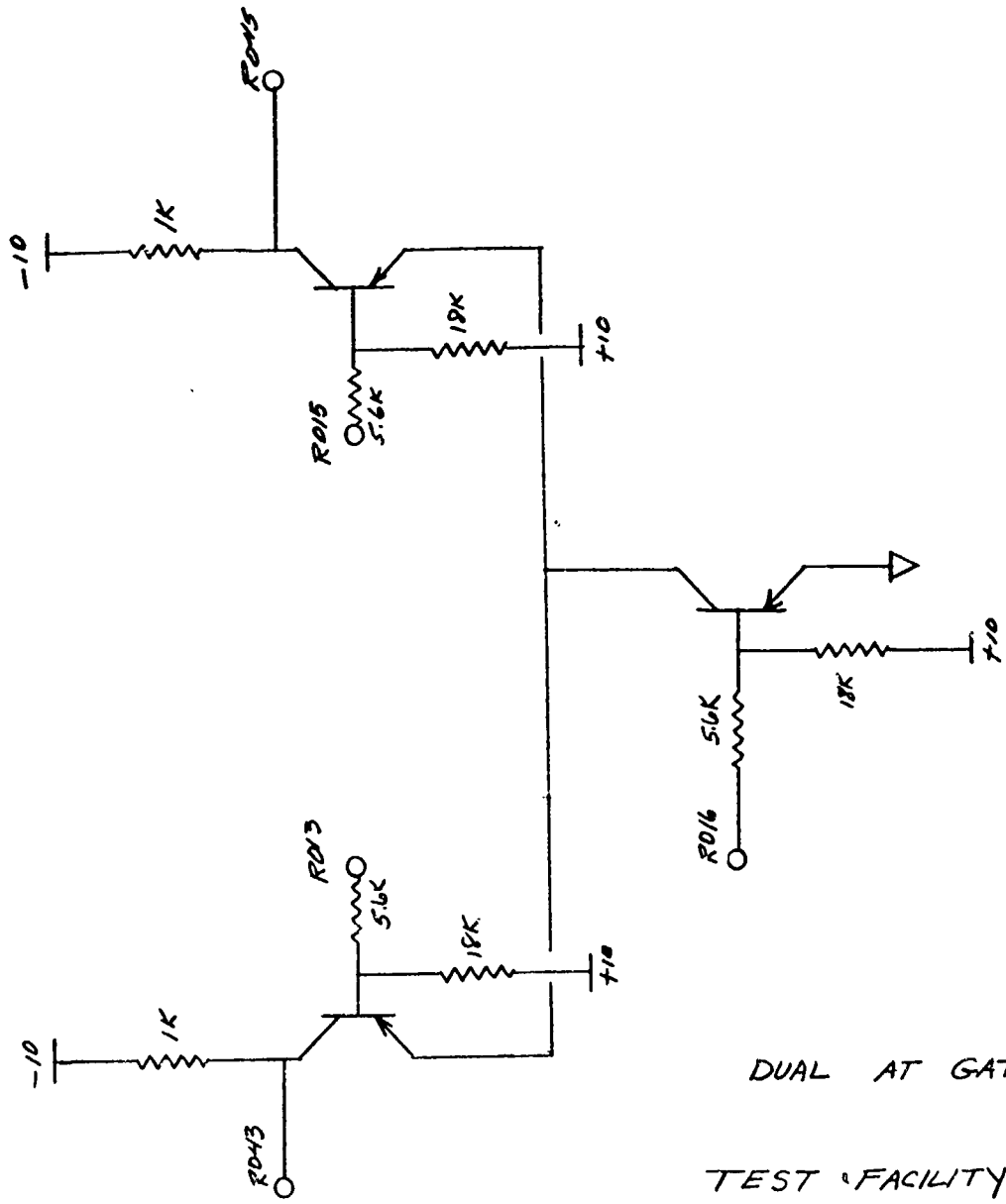
S-14



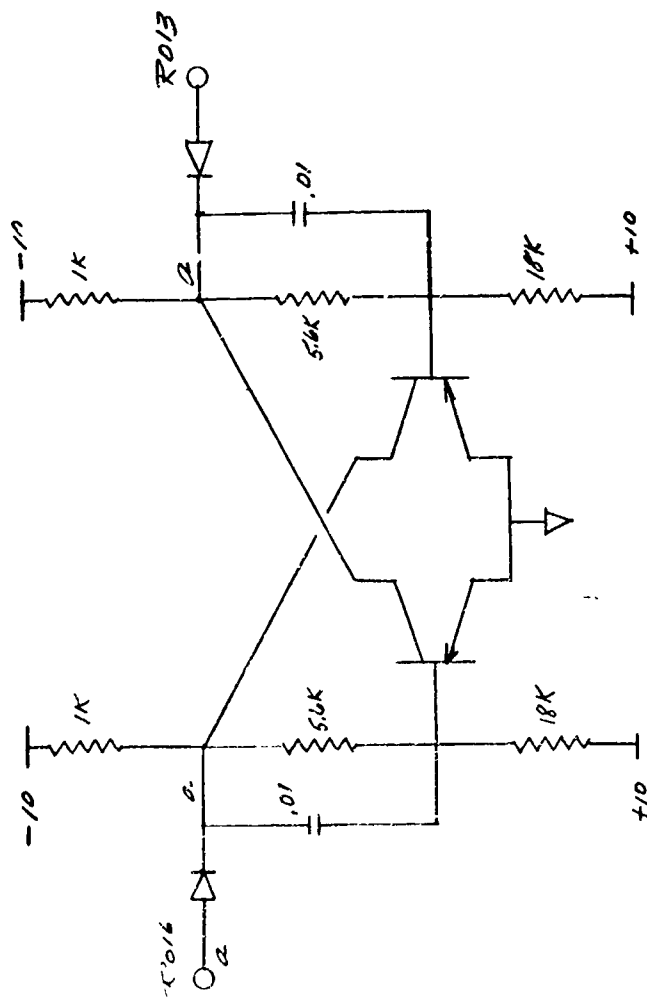
SHAPER

TEST FACILITY

S-15



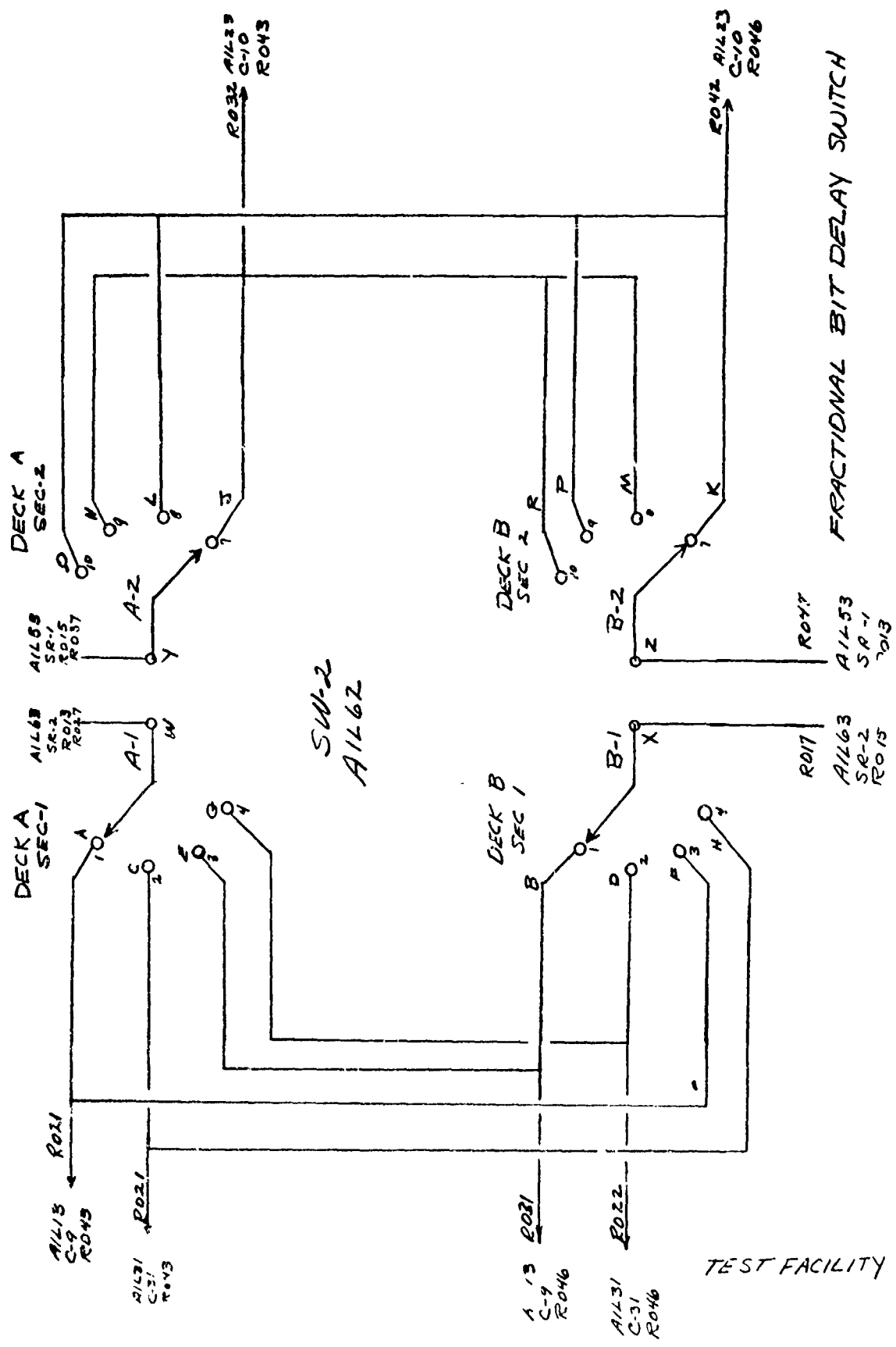
S-16



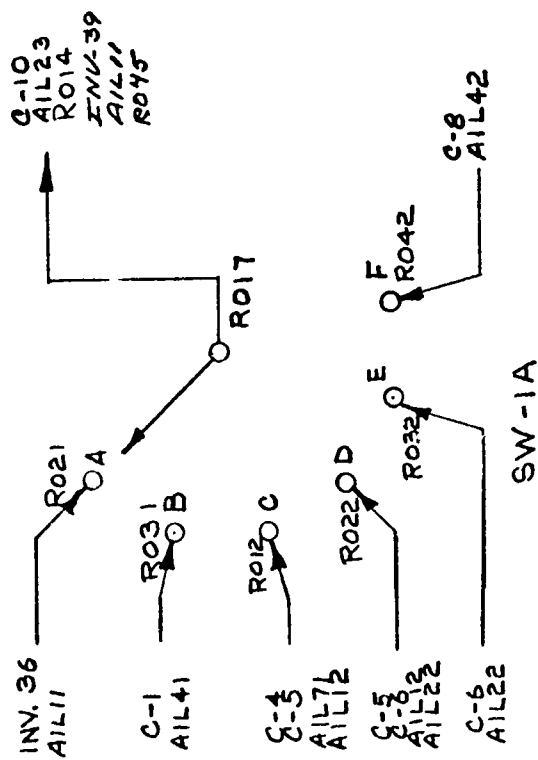
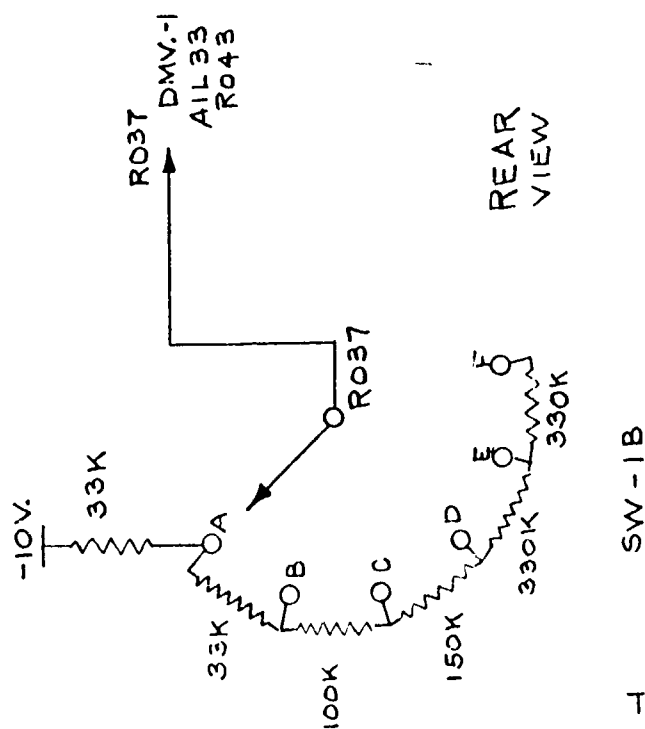
FLIP FLOP

TEST FACILITY

S-18

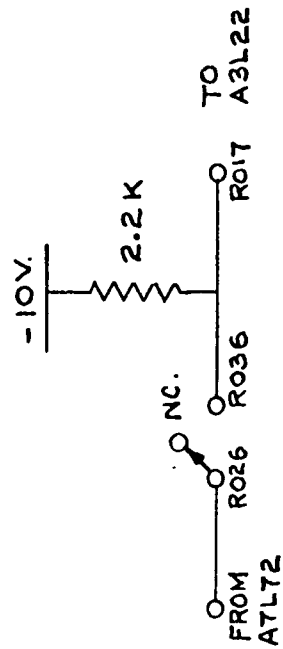
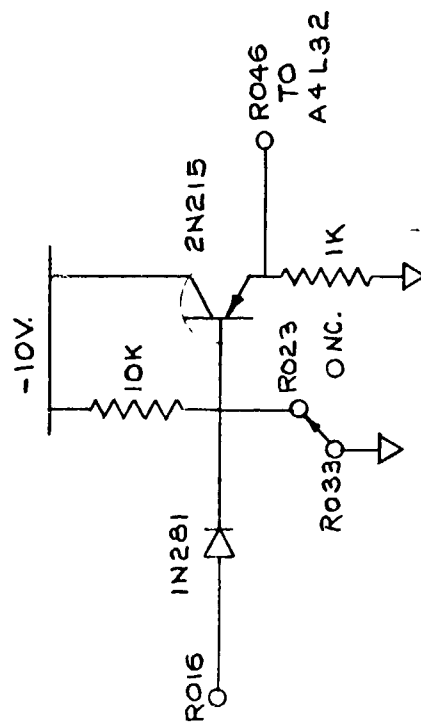


FRACTIONAL BIT DELAY SWITCH



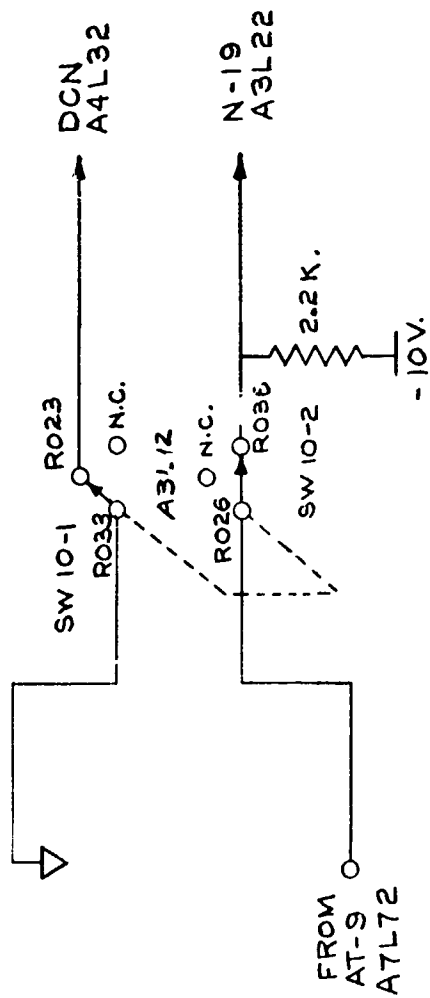
MANUAL DELAY SWITCH SW-1

TEST FACILITY



TEST FACILITY

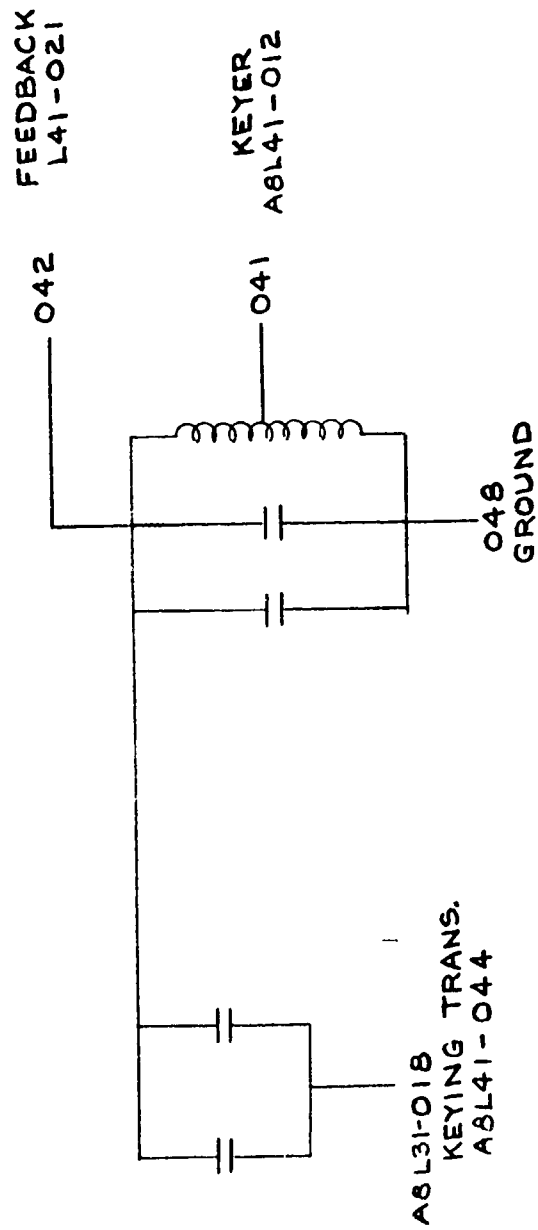
S-21



ON-OFF TEST SWITCH
SW-10-1/-2

TEST FACILITY

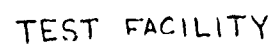
S-22



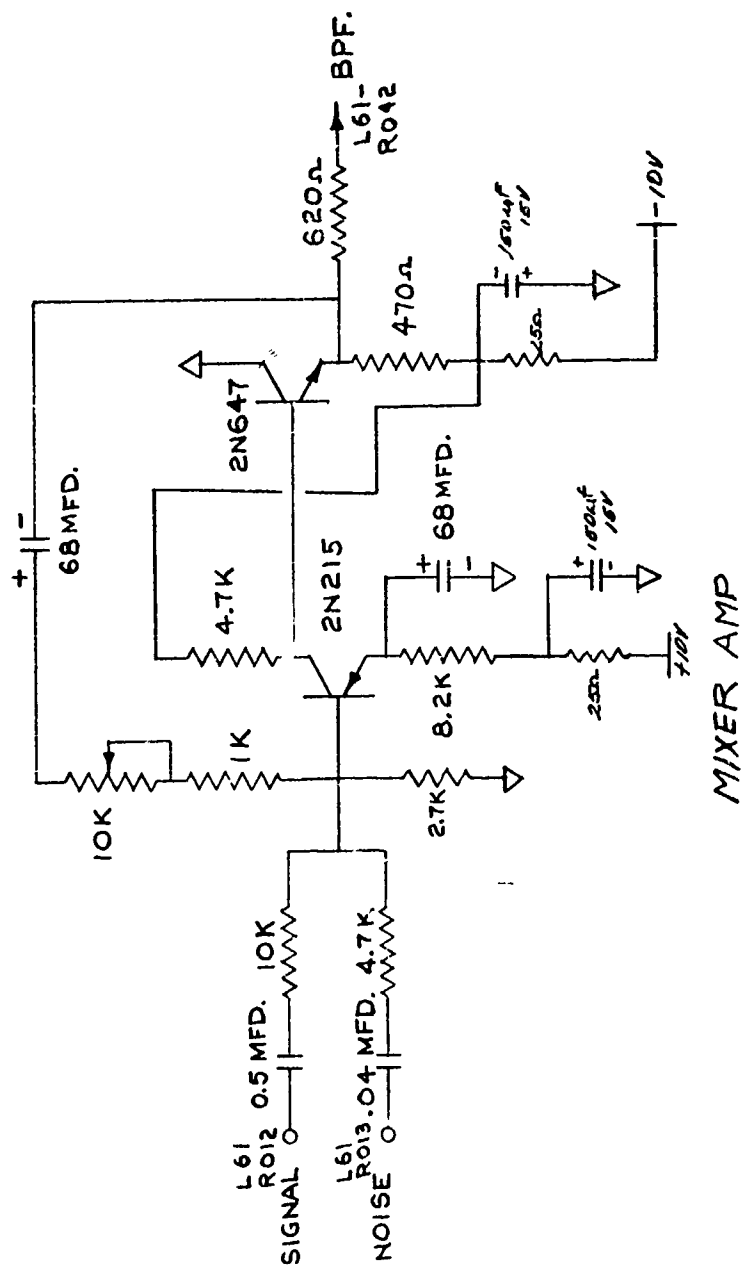
KEYER TUNED CKT.

TEST FACILITY

S-23

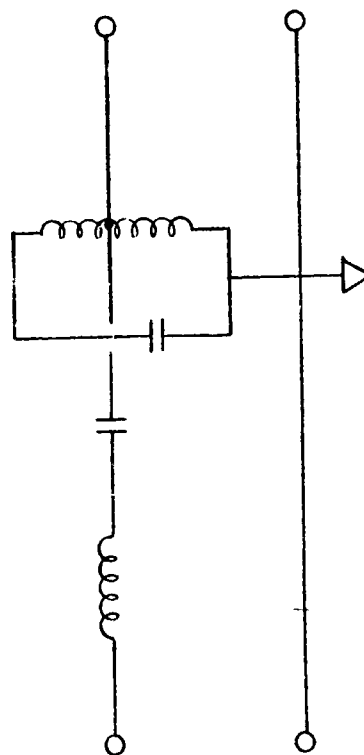


S-24



TEST FACILITY

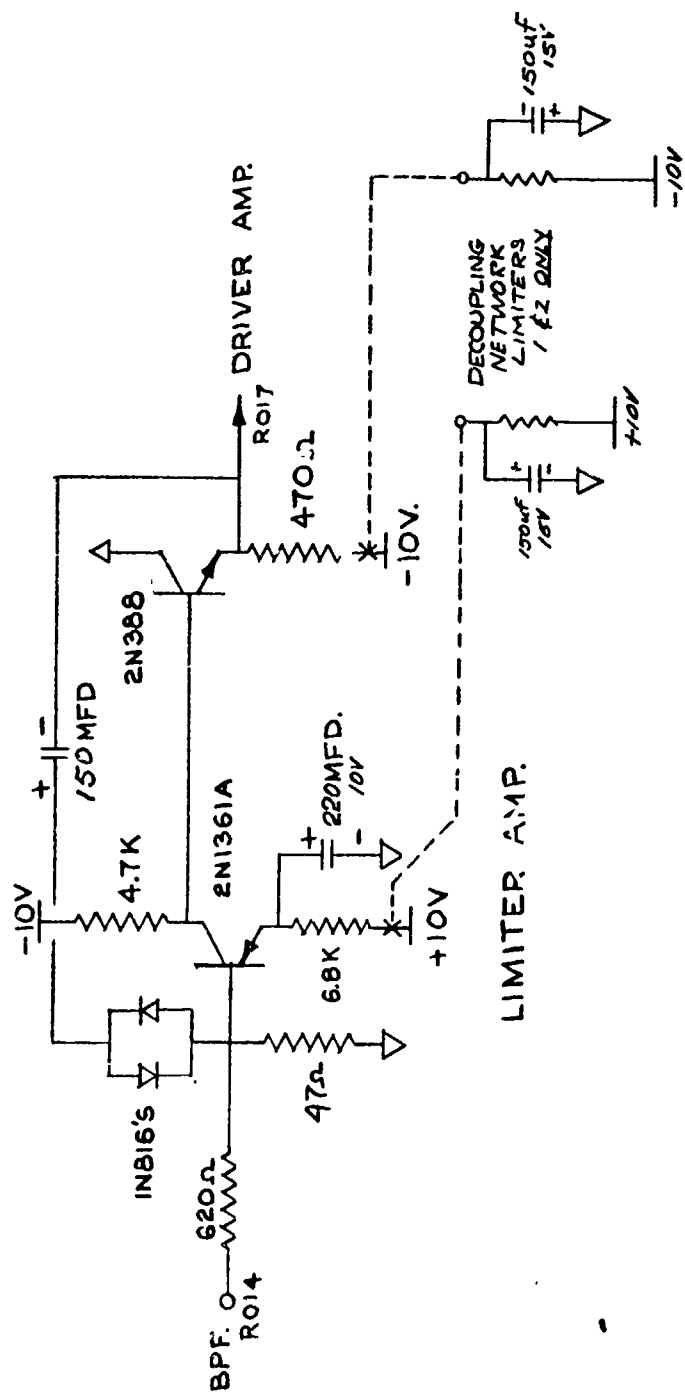
S-25



BAND PASS FILTER

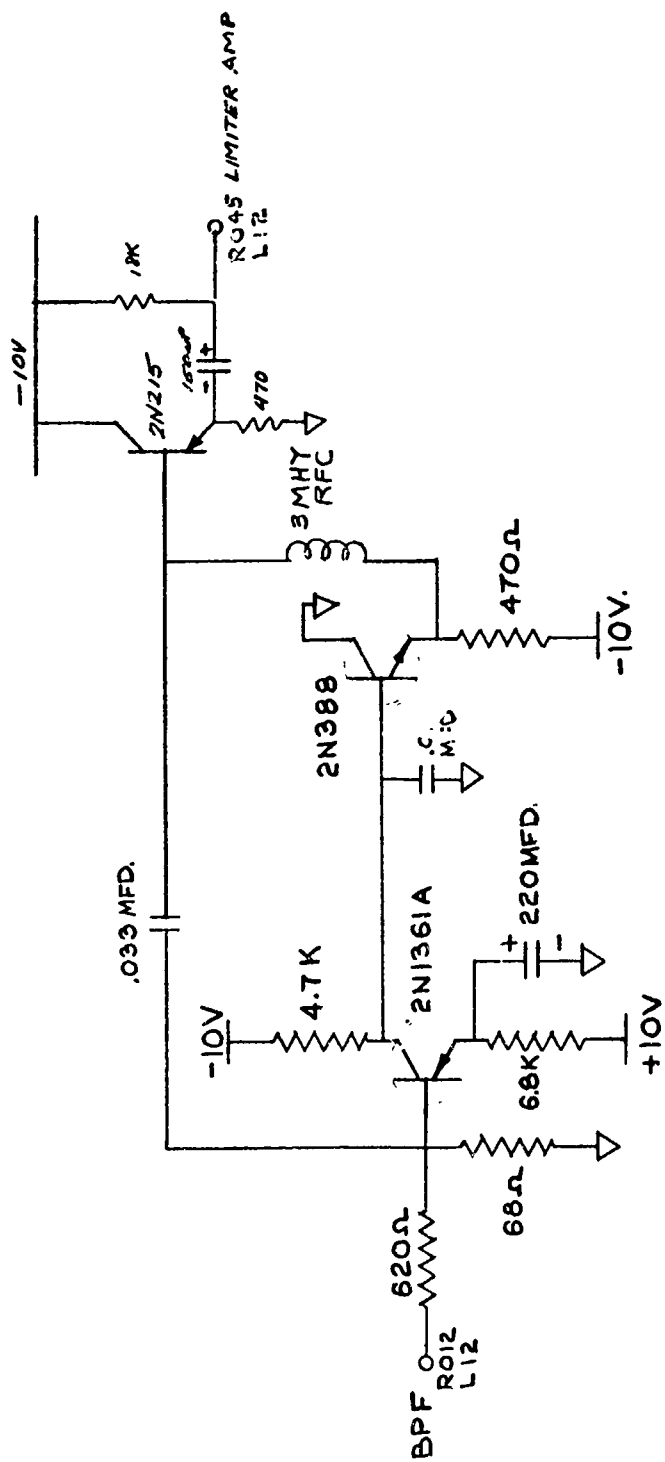
TEST FACILITY

S-26



TEST FACILITY

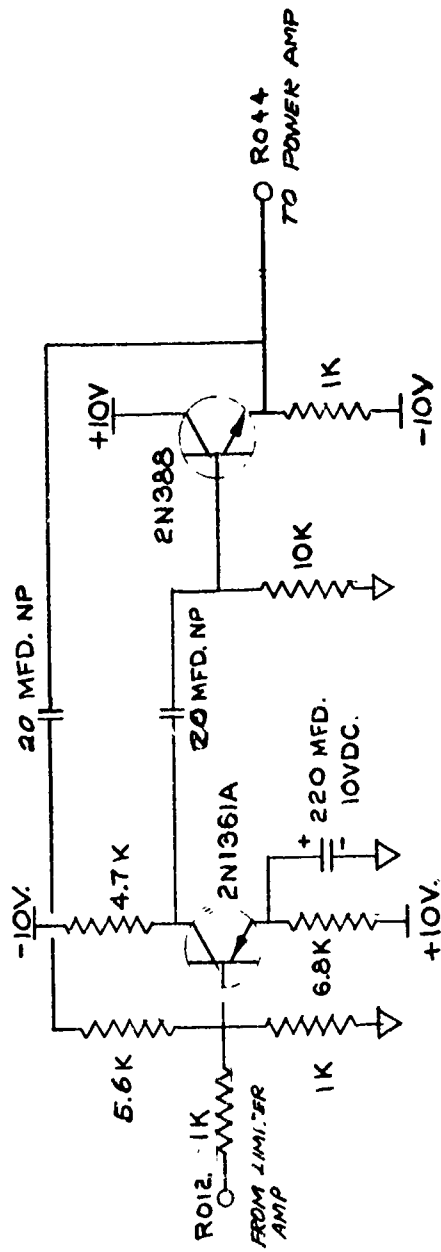
S-27



90° PHASE SHIFT INTEGRATOR

TEST FACILITY

S-28

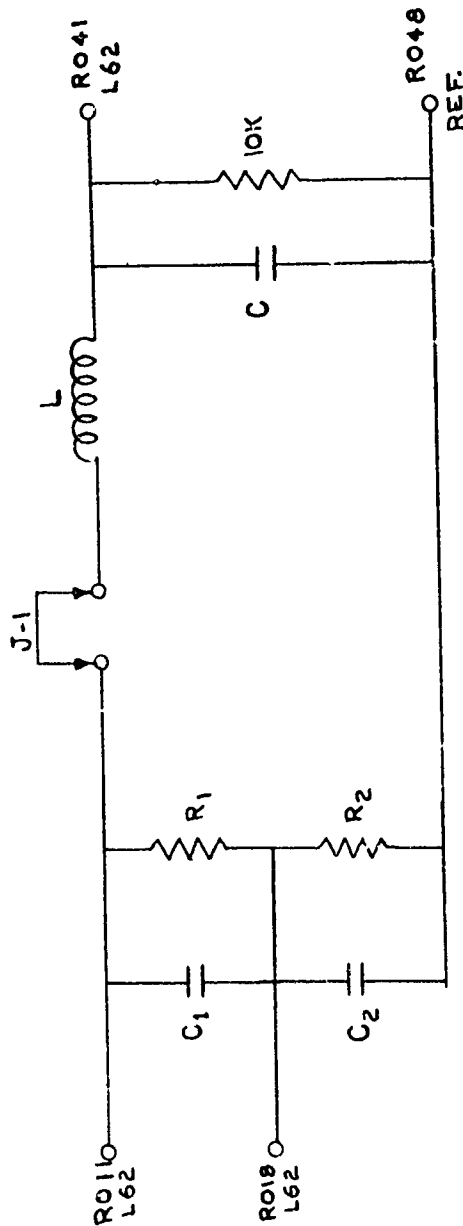


DRIVER AMPLIFIER

TEST FACILITY



160



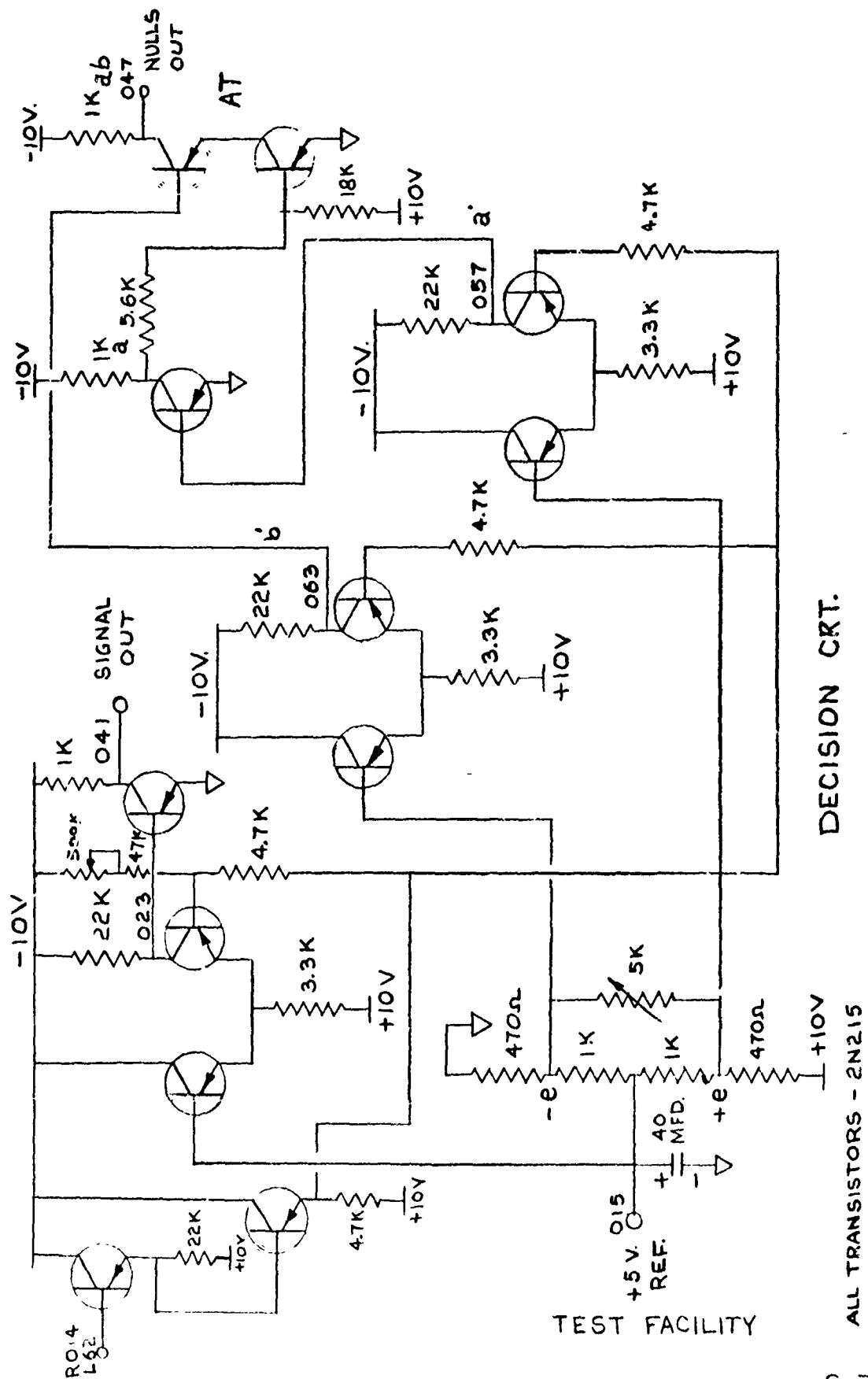
	$C_1 = C_2$	R_1	R_1 PADDED	R_2	LOW PASS FILTER f_o *
1MS	0.1 MFD	6.8K	33K	6.8K	750 c/s.
2MS	0.5 MFD	5.6K	220K	5.6K	375 c/s
5MS	1.0 MFD	4.7K	100K	4.7K	150 c/s
10MS	1.0 MFD	4.7K	—	4.7K	75 c/s
20MS	1.0 MFD	4.7K	100K	4.7K	37.5 c/s
30MS	1.0 MFD	4.7K	27K	4.7K	25 c/s

* f_o = 3DB POINT

LOW PASS FILTER

TEST FACILITY

S-31

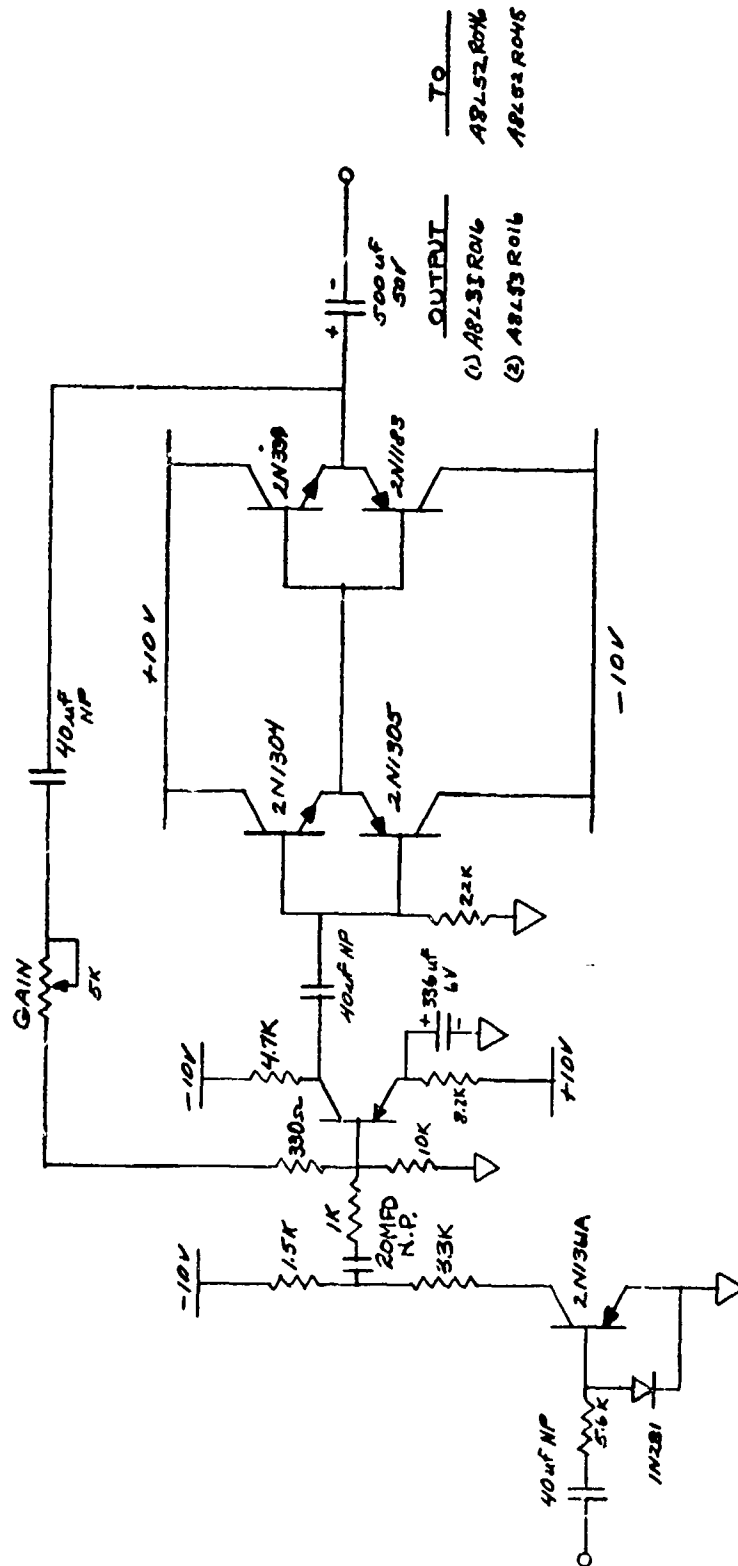


DECISION CRT.

ALL TRANSISTORS - 2N215

S-32

TEST FACILITY



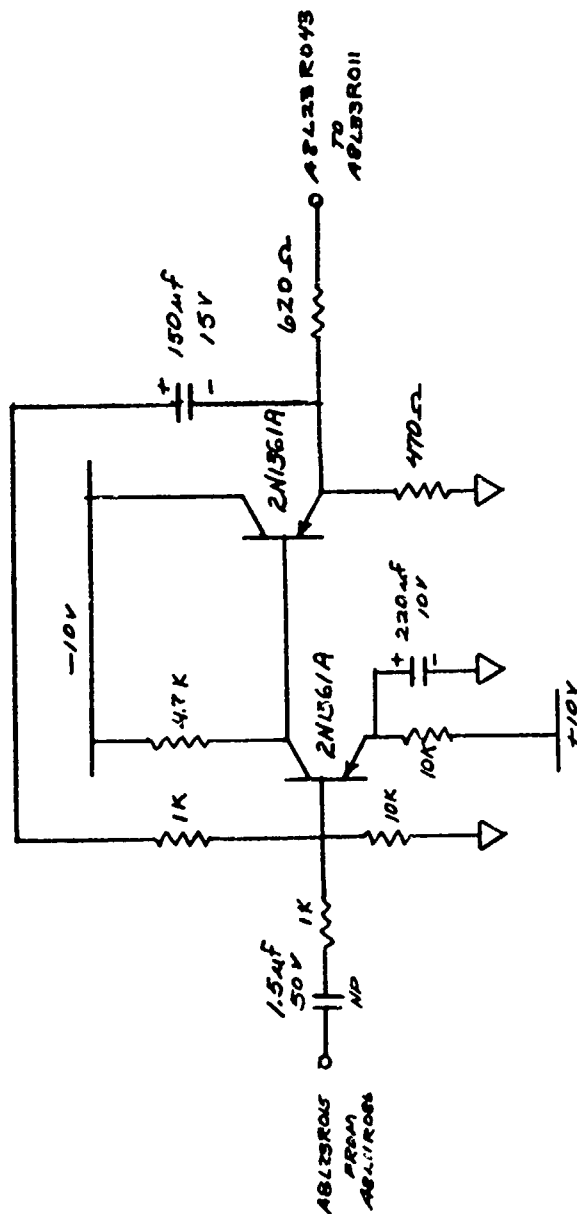
POWER AMP 1 & 2

INPUT	SOURCE
(1) AB233R071	AB232R044
(2) AB253R071	AB242R044

OUTPUT	TO
(1) AB233R016	AB252R016
(2) AB253R016	AB252R016

TEST FACILITY

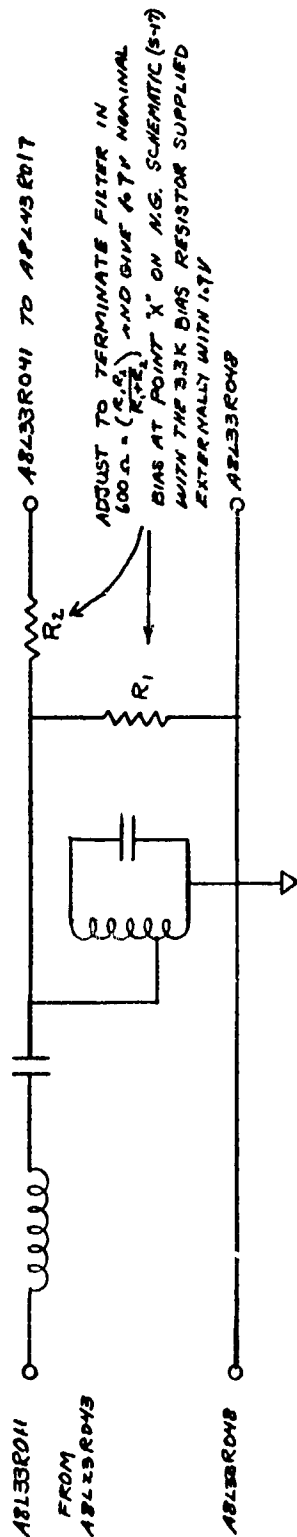
S-33



BUFFER AMP

TEST FACILITY

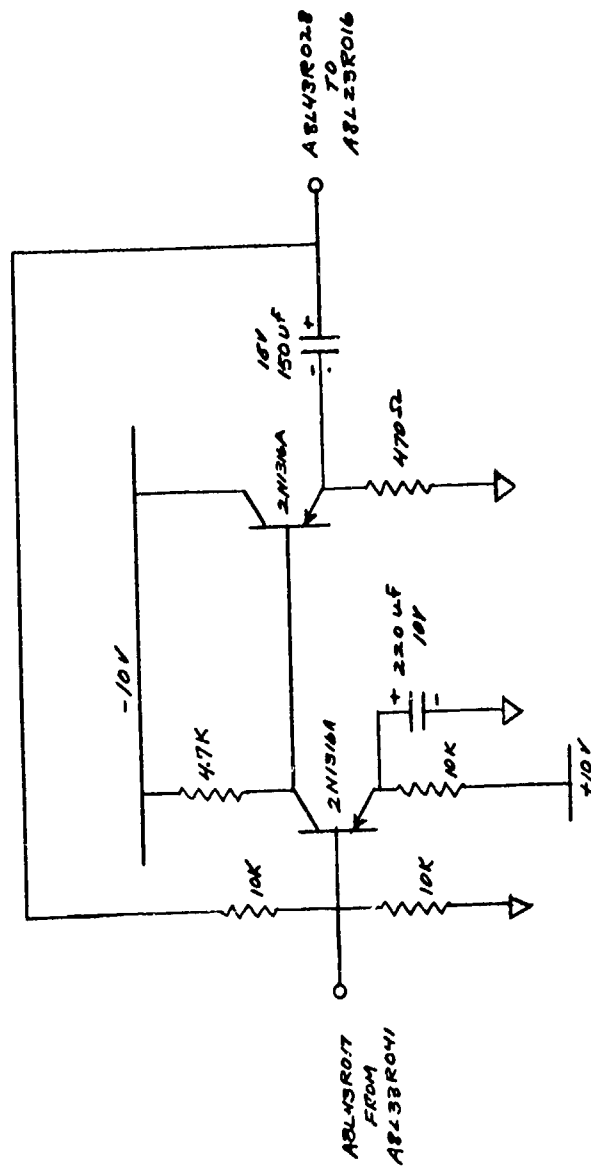
S-34



NOISE FEEDBACK BPF

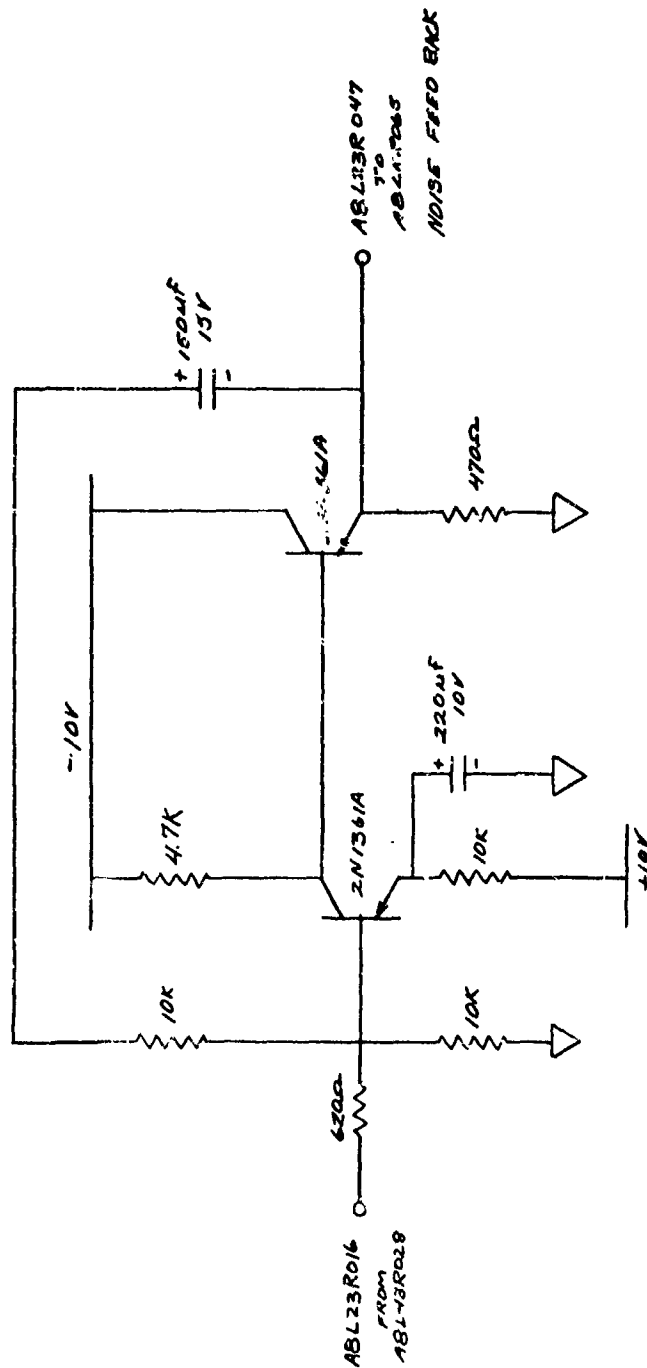
TEST FACILITY

S-35



BAND LIMITED NOISE AMF #1

TEST FACILITY
S-36

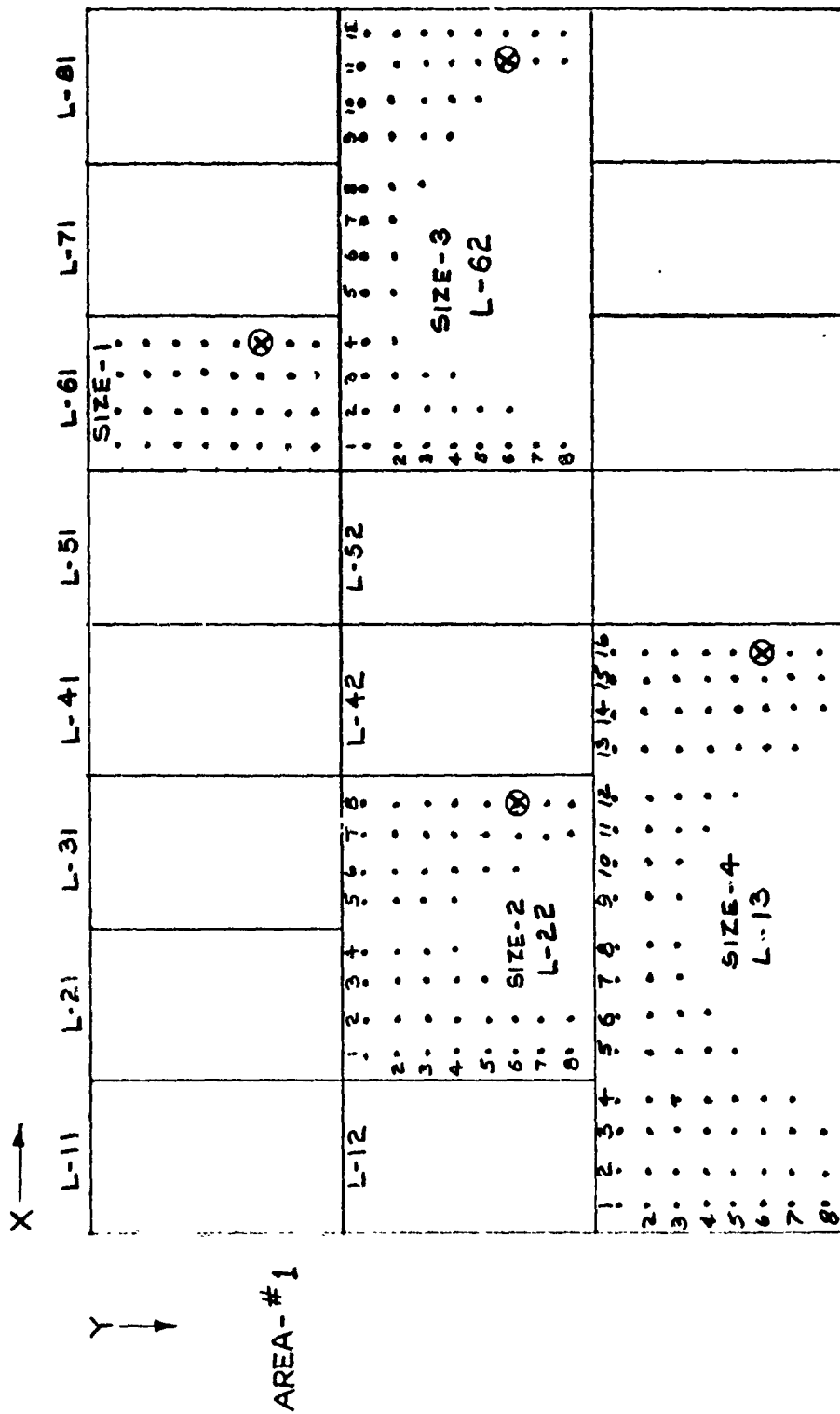


BAND LIMITED NOISE AMP #2

TEST FACILITY
S-37

EXAMPLE

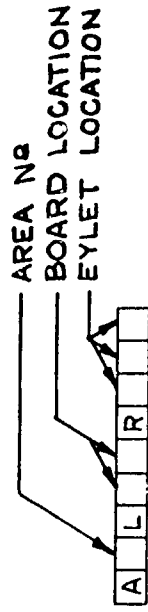
BOARD SIZE	LOCATION NUMBER
1	A1L61K046
2	A1L22R086
3	A1L62R116
4	A1L13R166

[illegible]

TEST FACILITY

ELEMENT CODING SYSTEM RACKS ARE DIVIDED INTO AREAS. THESE AREAS ARE DIVIDED INTO A POSSIBLE 24 LOCATIONS. EACH LOCATION IS A CIRCUIT BOARD. THERE ARE 4 SIZED CIRCUIT BOARDS. BOARD LOCATIONS AND EYLET LOCATIONS ARE DESIGNATED ON THE X-Y BASIS.

FORMAT



NOTE 1

SPECIAL CRTS. ARE SO NAMED ON BLOCK
DIAGRAMS AND SCHEMATICS.

NOTE 2

NUMBER AND LETTER COMBINATIONS APPEARING
IN OR ADJACENT TO CRT. ELEMENTS, BLOCK
DIAGRAMS, SCHEMATICS AND RELATED DATA
REFER TO LOCATIONS AS TO AREA, BOARD,
EYELET LOCATION AND SCHEMATICS.

CODING APPEARING ON BLOCK DIAGRAMS

LETTERS APPEARING IN RECTANGLES, SQUARES OR CIRCLES, APPLY TO LOGIC ELEMENTS AS FOLLOWS

AT	AND TRANSISTOR
C	COUNTER (÷2)
EF	EMITTER FOLLOWER
F/F	FLIP - FLOP
INV.	INVERTER
N	NOR GATE
DCN	DIODE COUPLING NETWORK
DIFF	DIFFERENTIATOR
DMV	DELAYED MULTIVIBRATOR
SR	SHIFT REGISTER
DR	DRIVER
COMP	COMPARATOR
CV	CONVERTER

A-5	20	21	22	23	24	BD-1
	SR	SR	SR	SR	SR	
	25	26	27	28	29	
A-6	10	11	12	13	14	BD-5
	SR	SR	SR	SR	SR	
	15	16	17	18	19	
A-7	10	11	12	13	14	BD-3, 4,
	SR	SR	SR	SR	SR	
	15	16	17	18	19	

- A-1 CLOCK PULSE GENERATOR
A-2 PANEL, METERS, AND COUNTER ASSEMBLY
A-3 COUNTERS, DRIVERS, ETC.
A-4, A-5 RECEIVING REGISTER AND COMPARATORS
A-6 PATTERN GENERATOR & TRANSMIT REGISTER
A-7 TRANSMITTER A-7 RECEIVE PULSE GENERATOR

TEST FACILITY
RACK AREA AND CCT.
DESIGNATION LAYOUT 13D-C

	L11	L21	L31	L41	L51	L61	L71	L81
L1	4K100	FF-15	C-	C-	C-	C-	C-	AT-1
	SW-16	SW-15	31	1	2	3	4	AT-2
L12	C-	C-	C-	C-	SW-14	SW-10	SW-2	TB
	5	6	7	8	SW-10	SR	SR	RB
L13	C-	C-	DMV	SHADE	SR	SR	SR	RB
	9	10	1	1	1	2	2	

BD-1, 2

FRAMEL, METERS, AND COUNTER ASSY

A-17	I-20	←	÷10	(OK)	→	DMV-2	DMV-3
N-18	I-21					DR-1	DR-2
SW-10-1	I-22	I-23	I-25	DMV-4	DMV-5	DMV-6	DMV-7
SW-10-2	N-19	N-20	I-26	DE-3	DR-4	DR-5	DR-6
AT-20	I-24	N-21	I-28	←	÷10	(C-17)	→
		N-22			BY ERROR		
I-15	SR	SR	COMP	←	÷10	(C-18)	→
I-16	16	17	1		NULLS		
SR	EF-12	EF-14	AT-19	AT-17	DMV-8	DMV-9	
18	EF-13	DNC	EF-17	AT-18	DR-7	DE-8	
I-17	COMP	SR	← ÷8	→	COMP	C-	EF-10
I-18	2	11	N-16		3	15	EF-11

BD-8

BD-8, 6

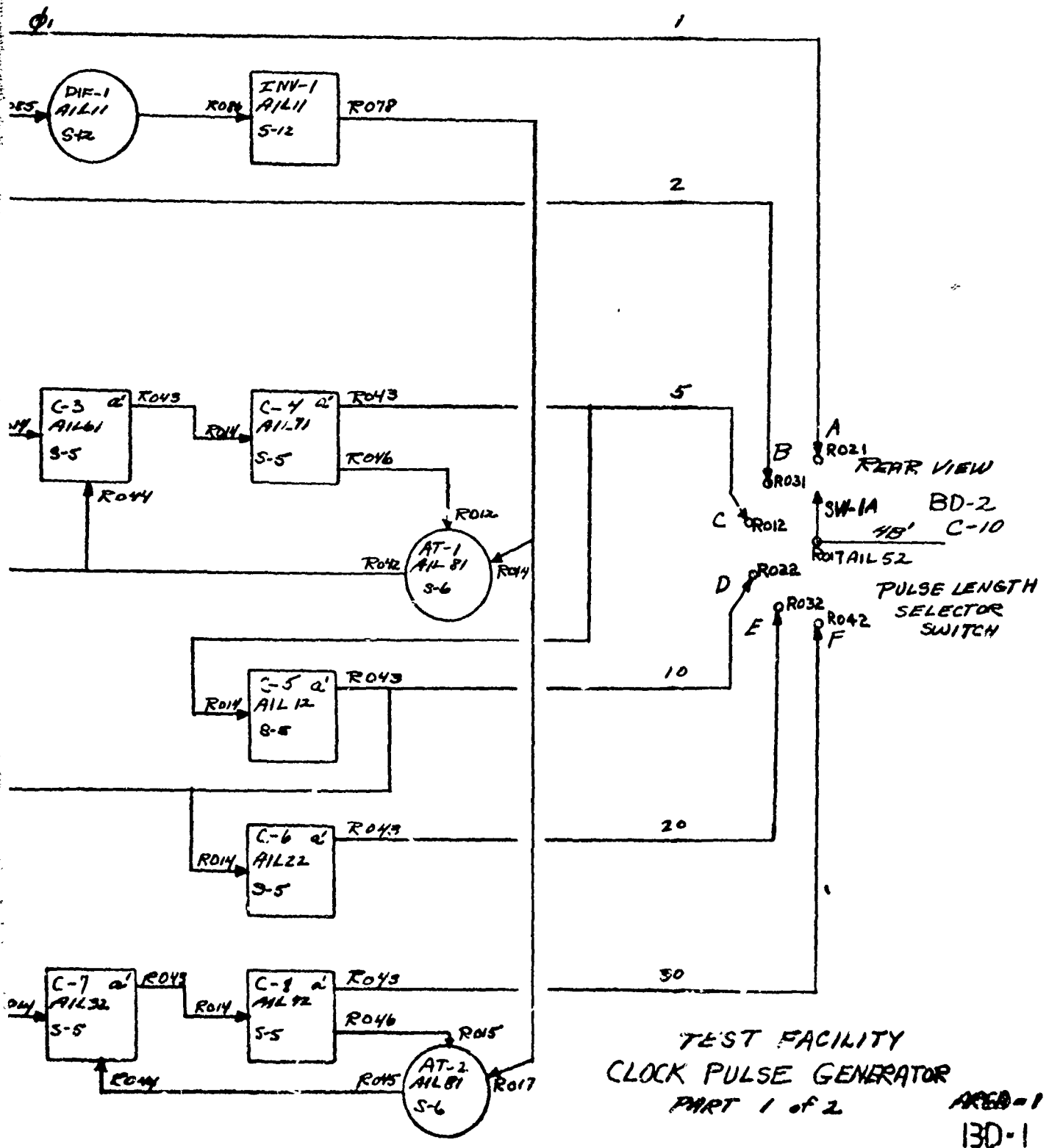
A-1

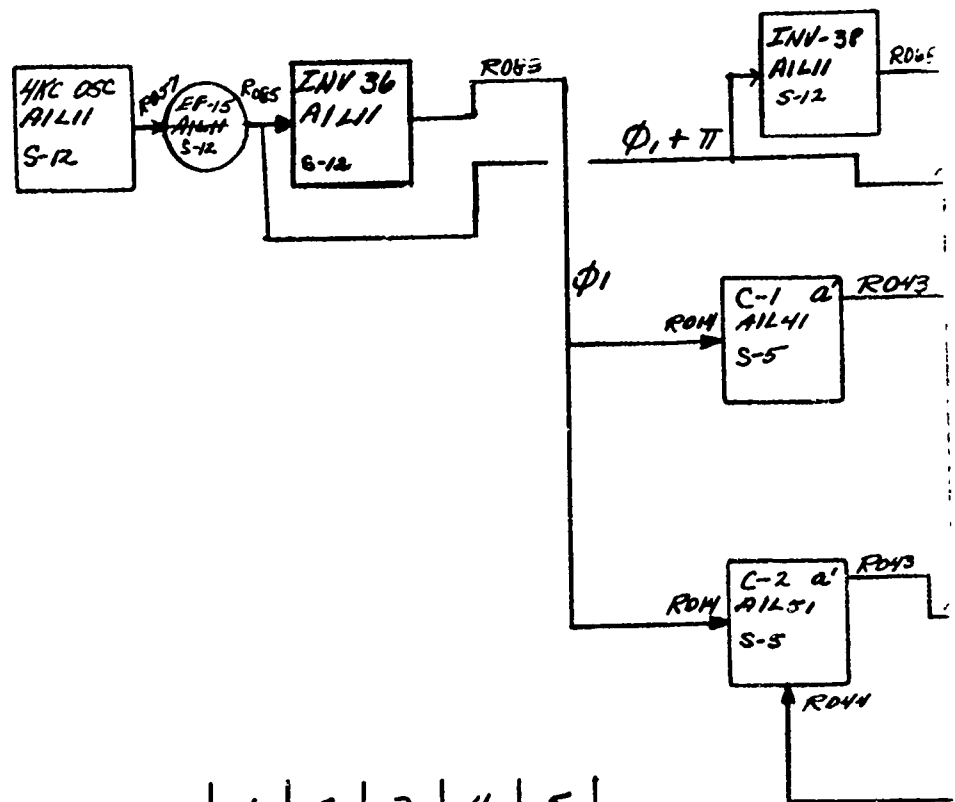
A-2

A-3

A-4

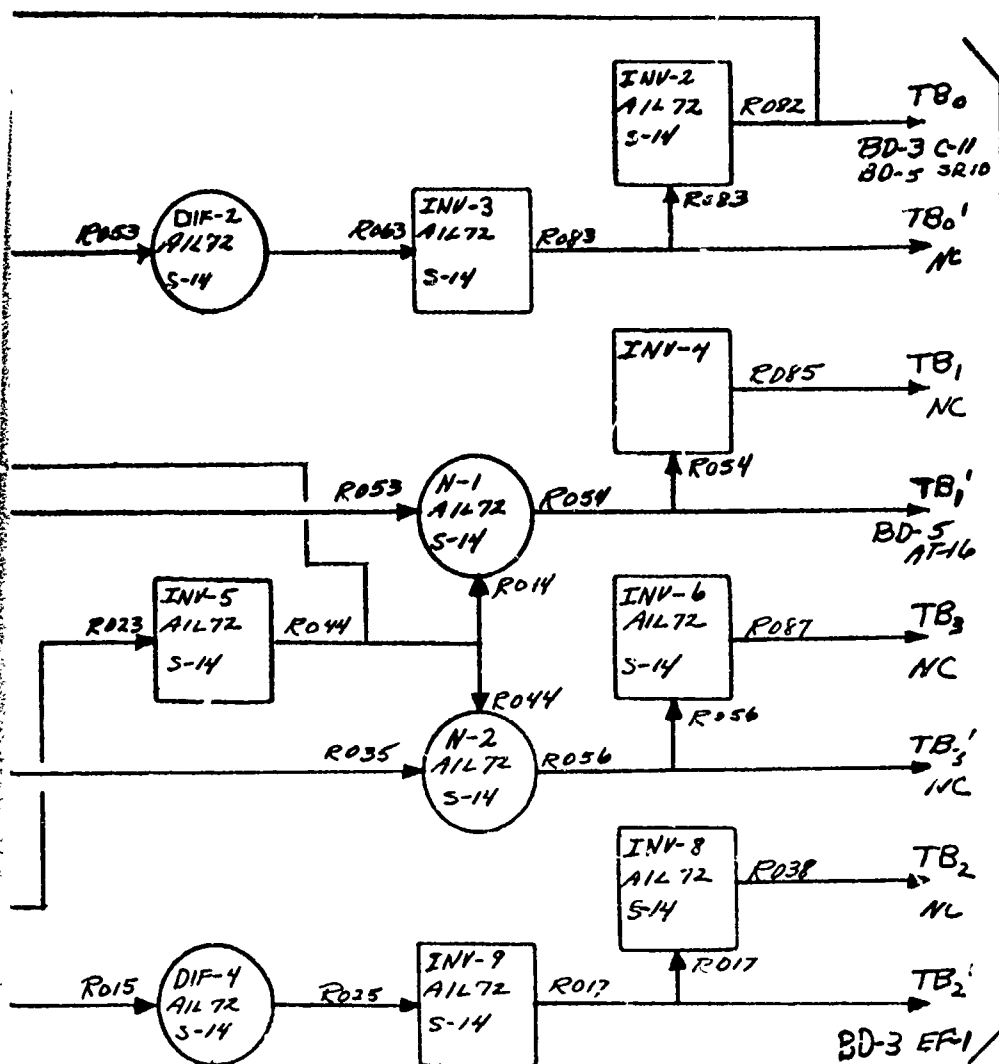
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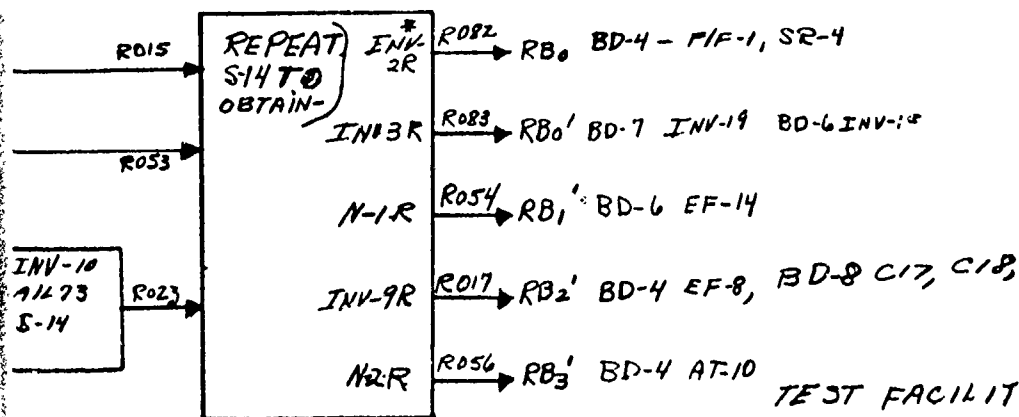


	1	2	3	4	5	
a	0 1	0	1	0	1	0
b	0 1	0	0	1	1	0
	0 0	1	1	1	1	0

	1	2	3	
	0 1	0	1	0
	0 0	1	1	0

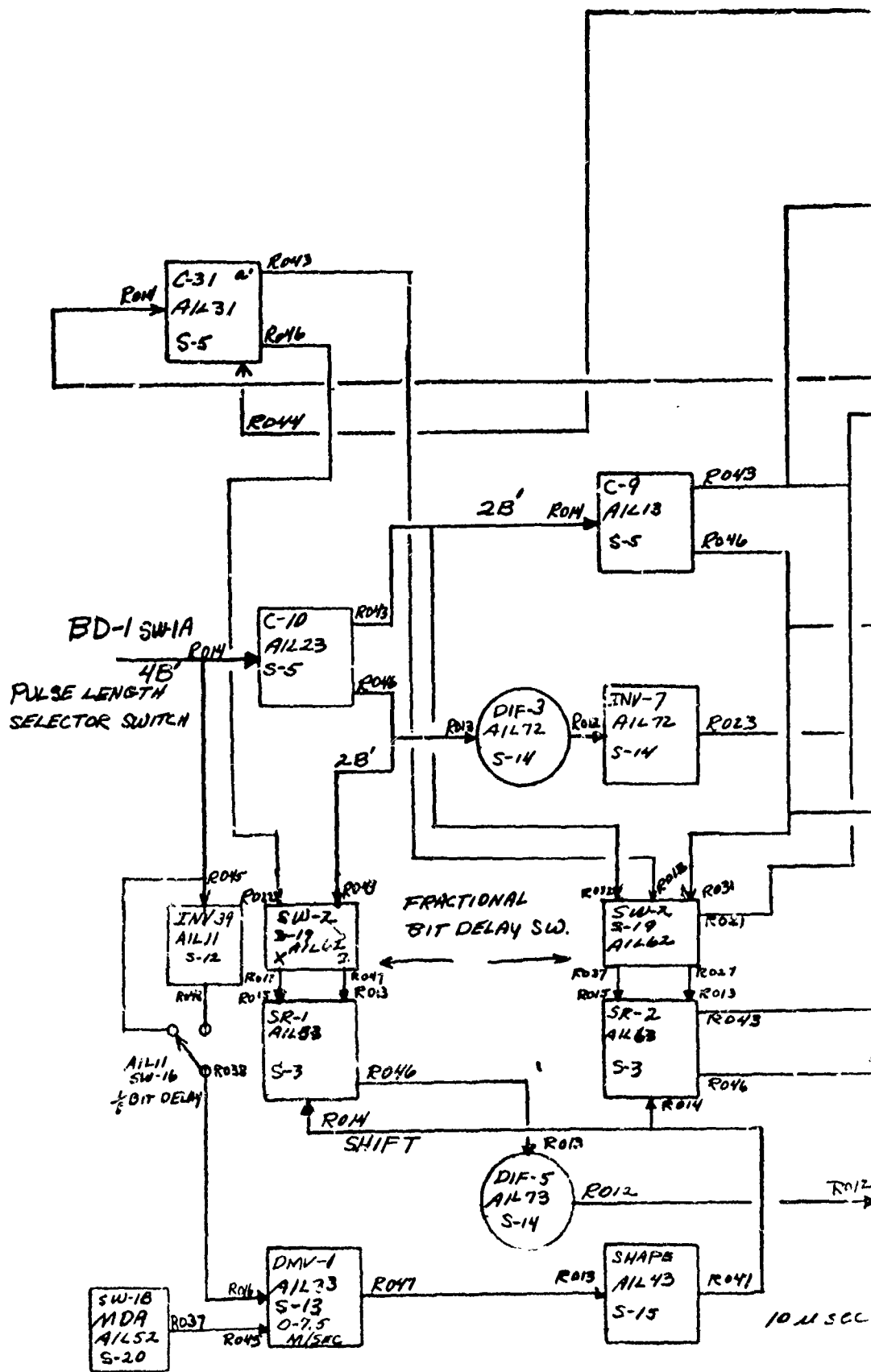


INV-2R
* NOTE: 5.6K RESISTOR TO GRD IN INV. 2R COLL Ckt.

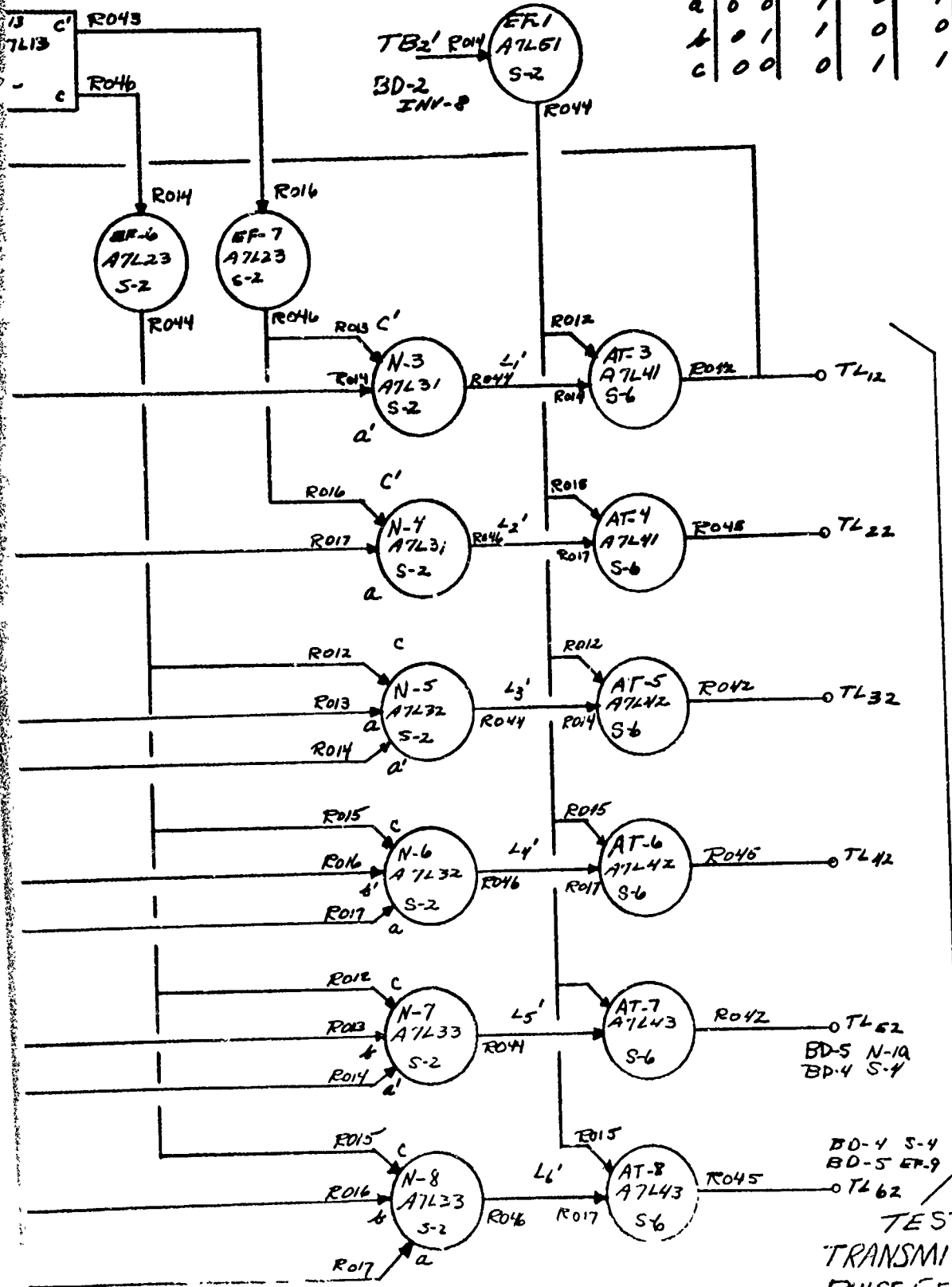


TEST FACILITY
CLOCK PULSE GENERATOR
PART 2 of 2

AREA-1
BD-2



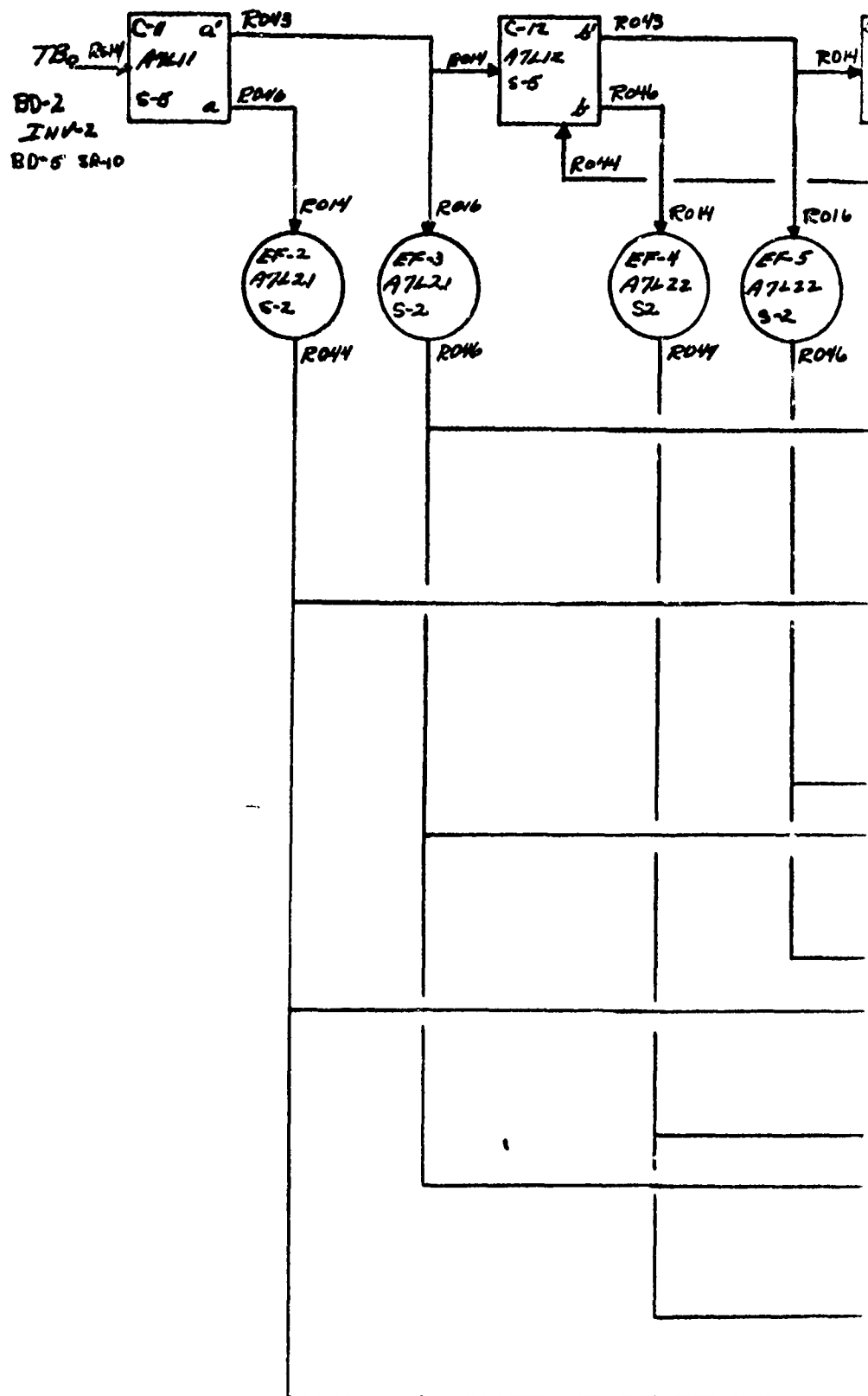
	1	2	3	4	5	6	
a	0	0	1	0	1	0	1
b	0	1	1	0	0	1	0
c	0	0	0	1	1	1	0



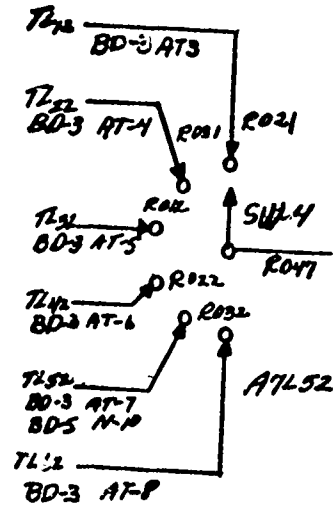
BD-4
SW-4

AREA-7

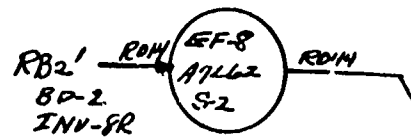
TEST FACILITY
TRANSMIT CHARACTER
PULSE GENERATOR
BD-3



PHASE DELAY
SELECTOR SW.



RBO
BD-2 INV-2R



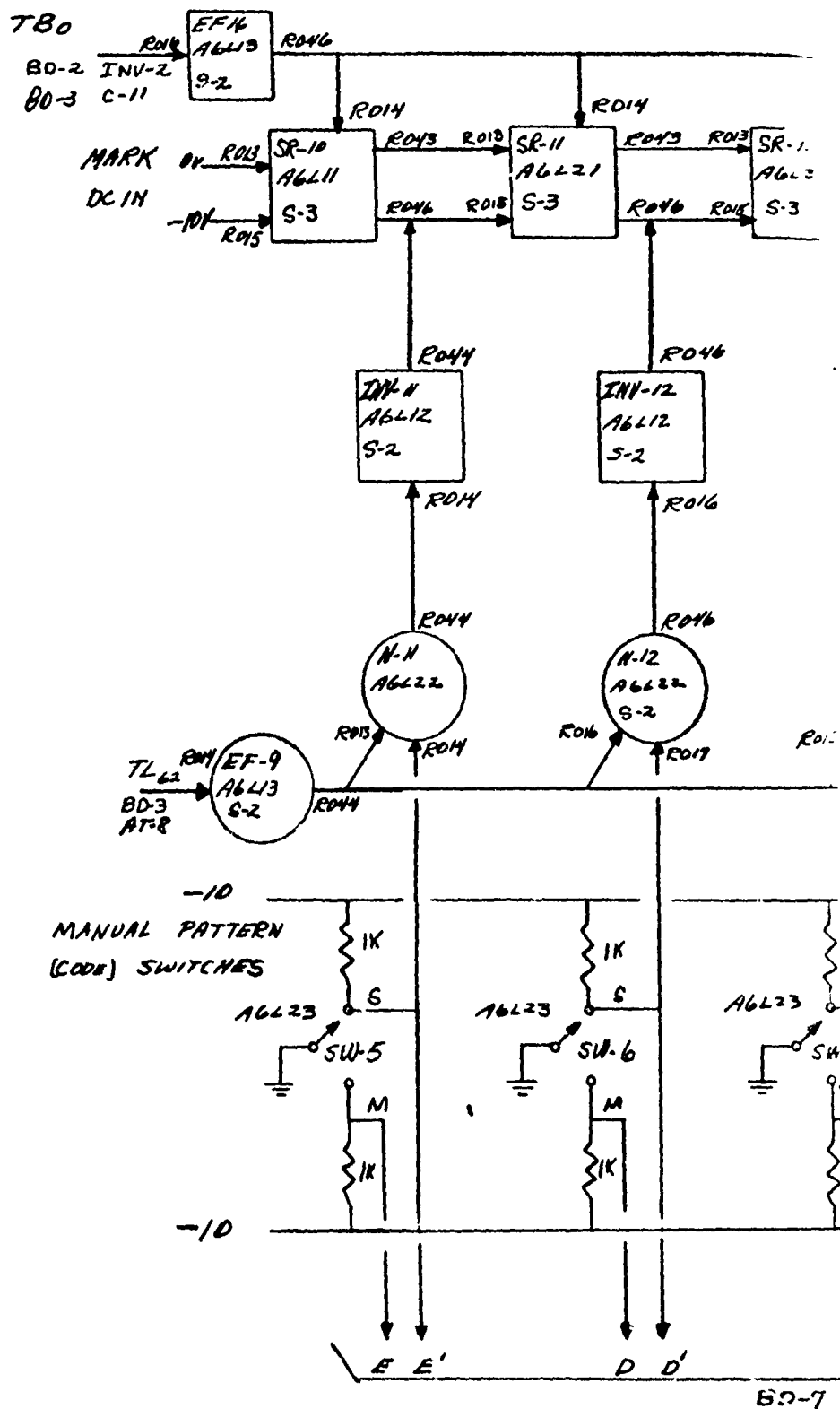
R03'
BD-2
N-2R

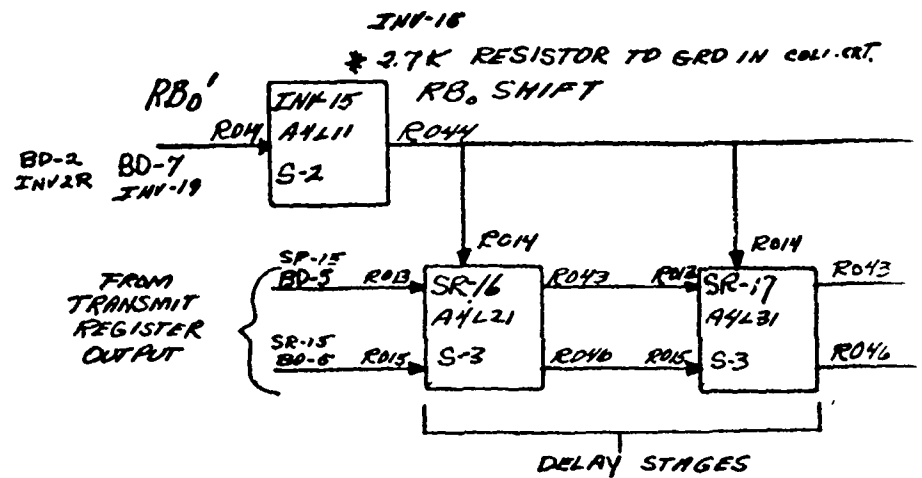
BD-2
SIO-2

USE DUAL

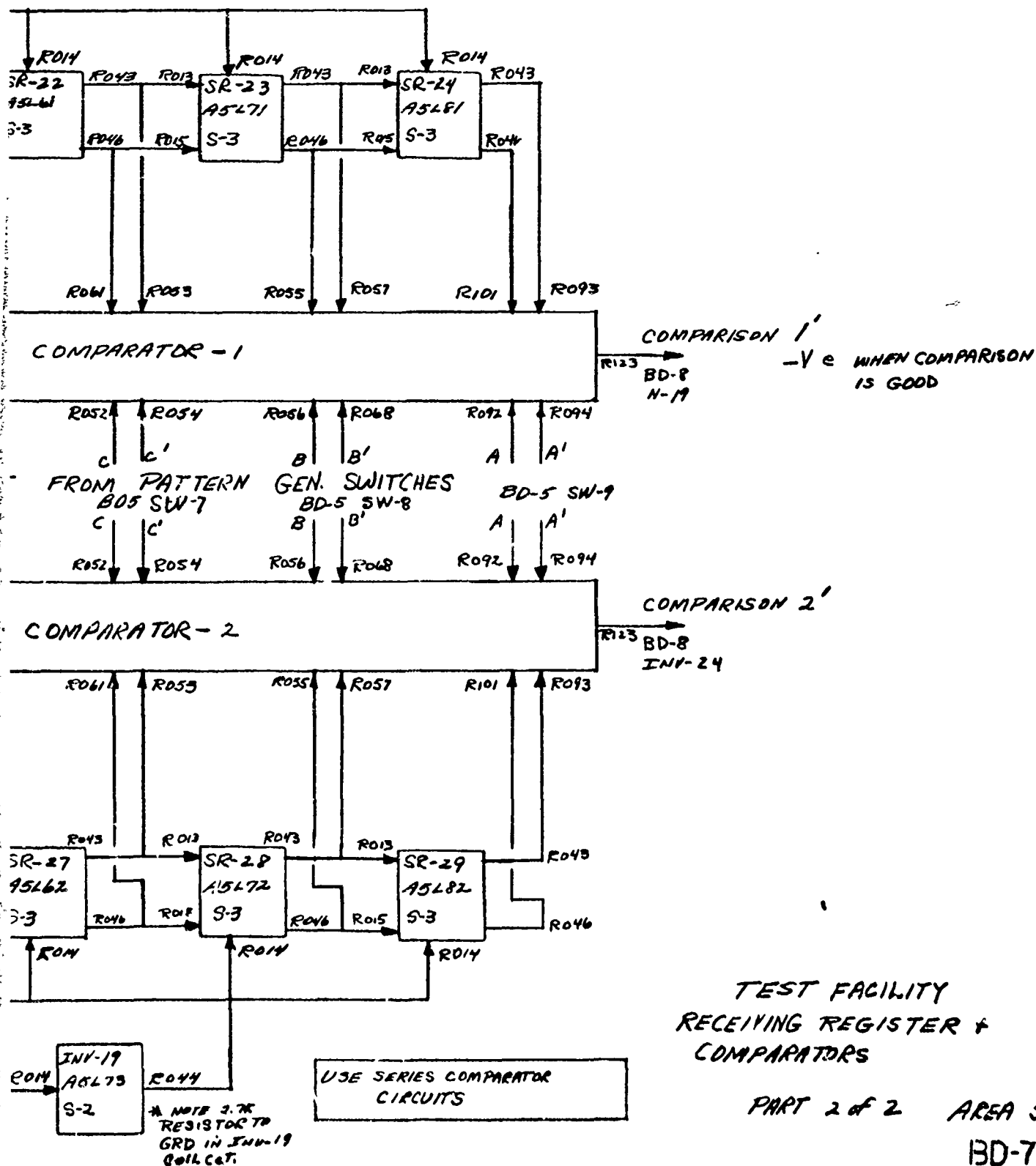
OTHER GATES AS REQUIRED

NOTE: EF-16 USES NPN 2N647

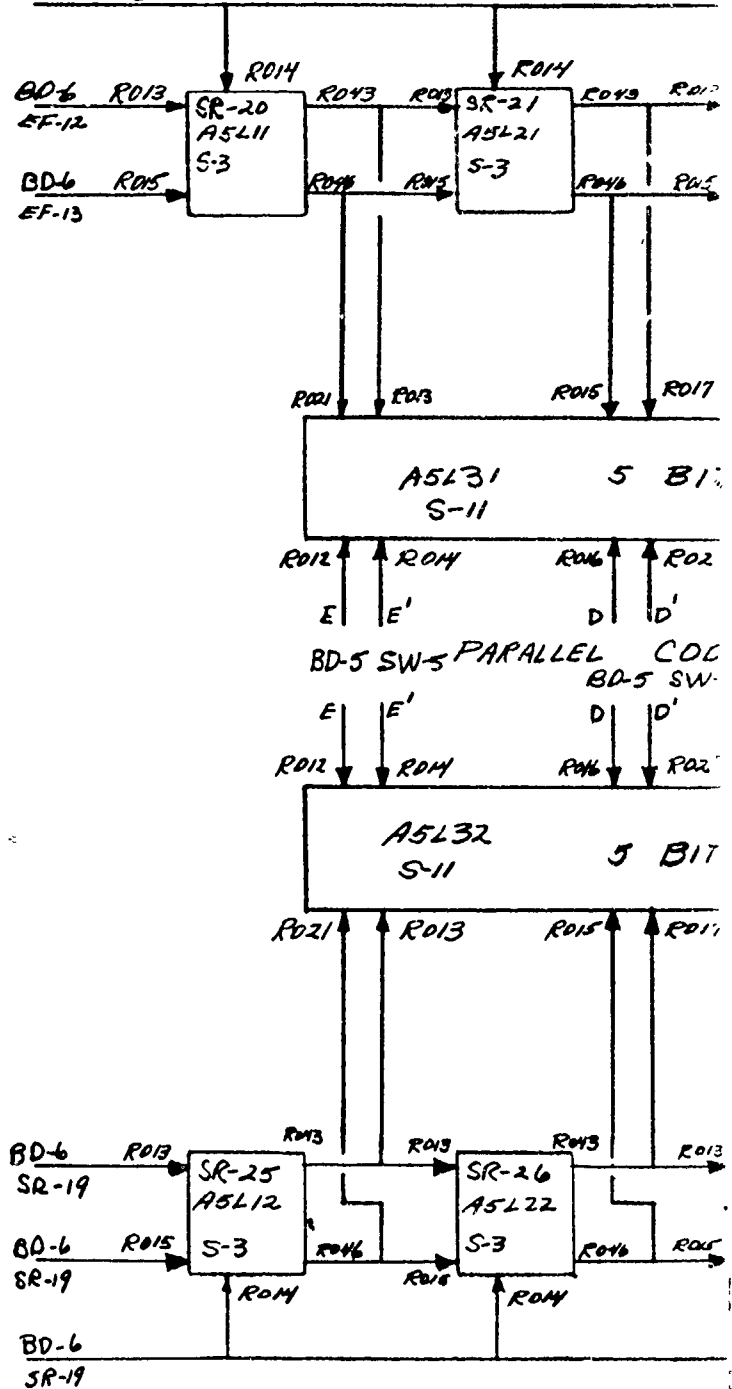




SIGNAL		NULL	TO CORRECTION REGISTER	
S	0	0	S	0
M	1	0	M	1
S	0	1	M	1
M	1	1	S	0



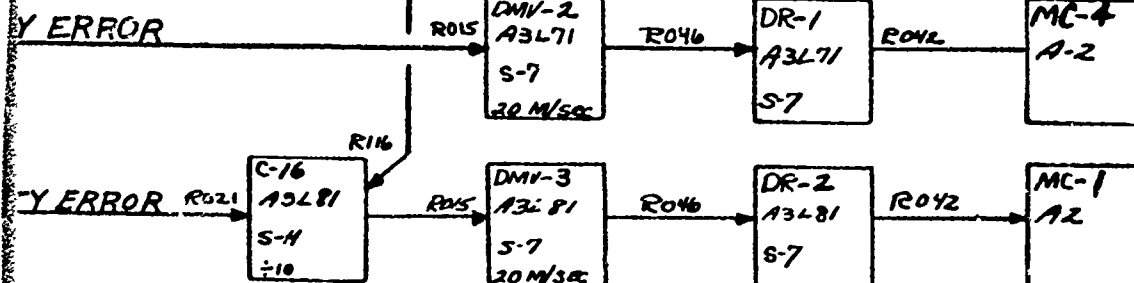
RB₀ SHIFT BD-6 SR-18



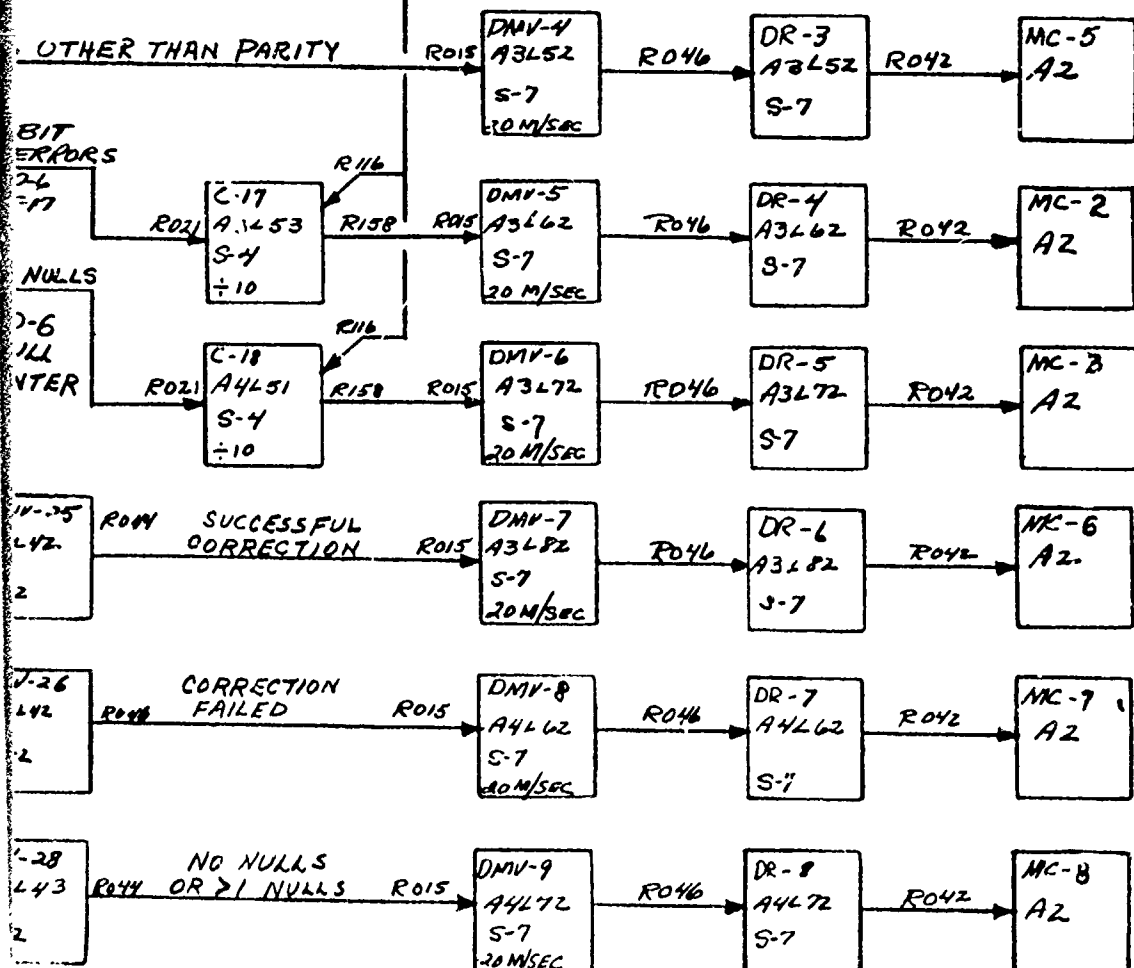
RB₀'

BD-6 BD-2 INV-3R
INV-15

RL13 RESET BD-4 INV-37
BD-9 AT-21



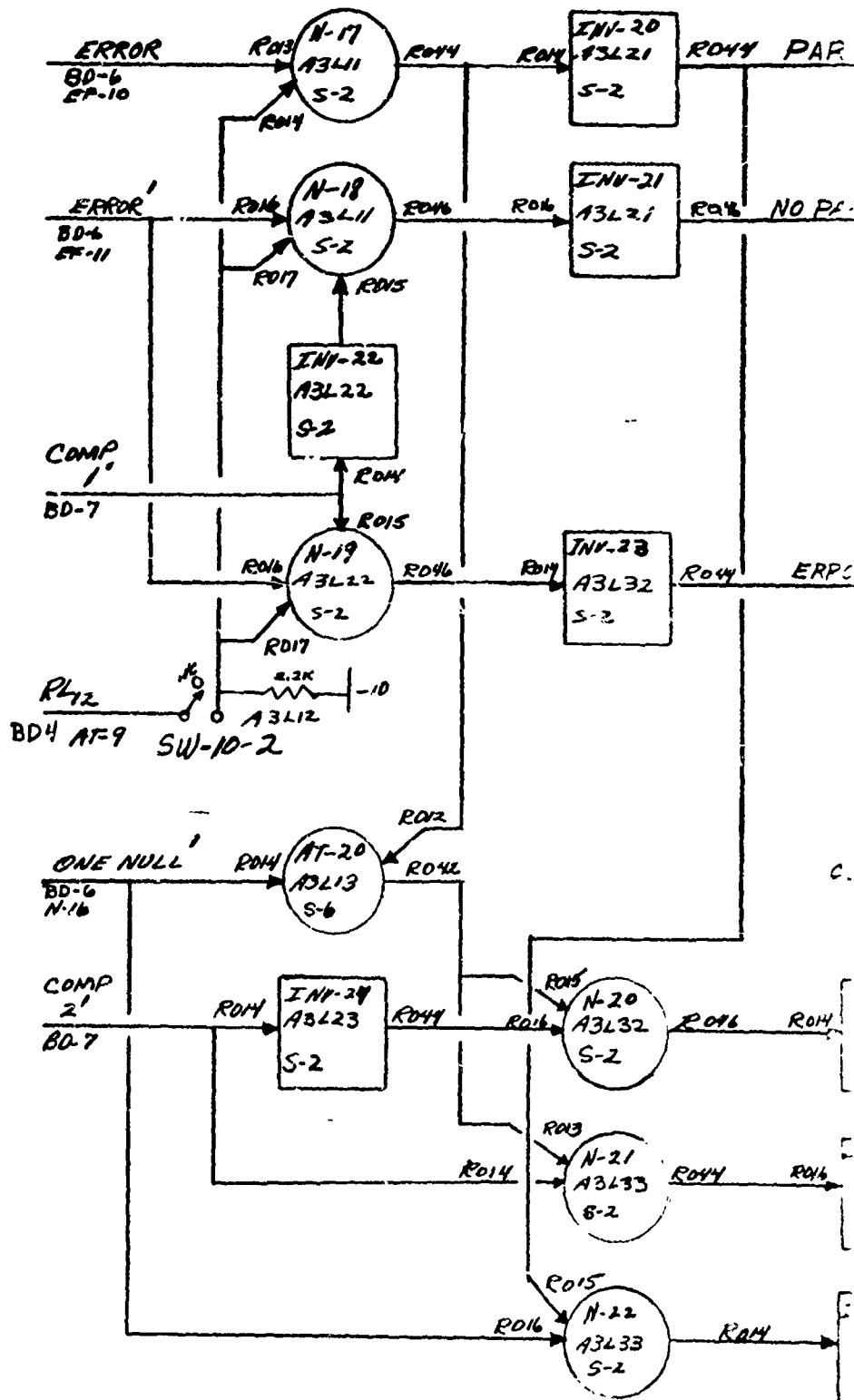
RB2'
INV-9R
BD-2 BD-9
AT-21

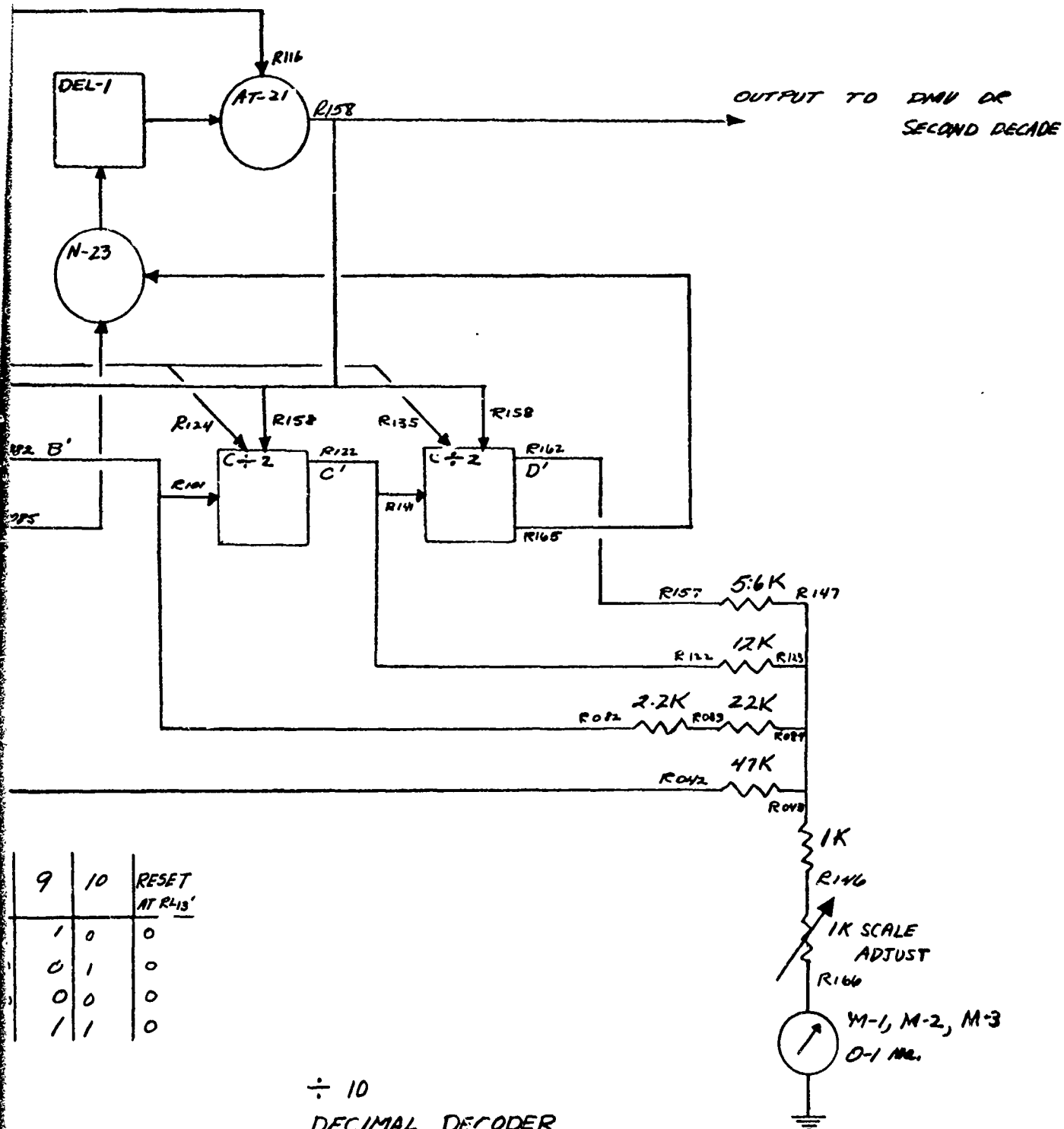


AREA-3
-4

TEST FACILITY
MECHANICAL
COUNTERS

13D-8





÷ 10
DECIMAL DECODER
& METER INDICATOR

13D-9

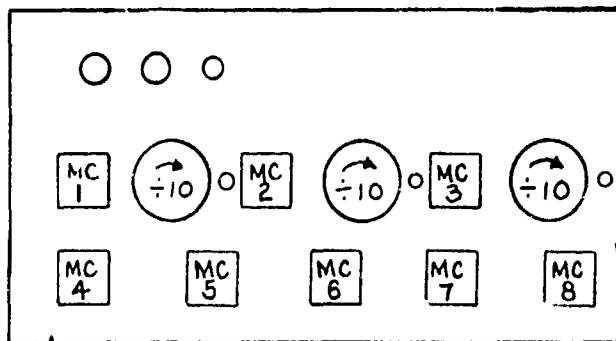
BIT MC-2
ERRORS

4
ERRORS OTHER
THAN PARITY
MC-5

NO NULLS OR
>1 NULLS MC-8

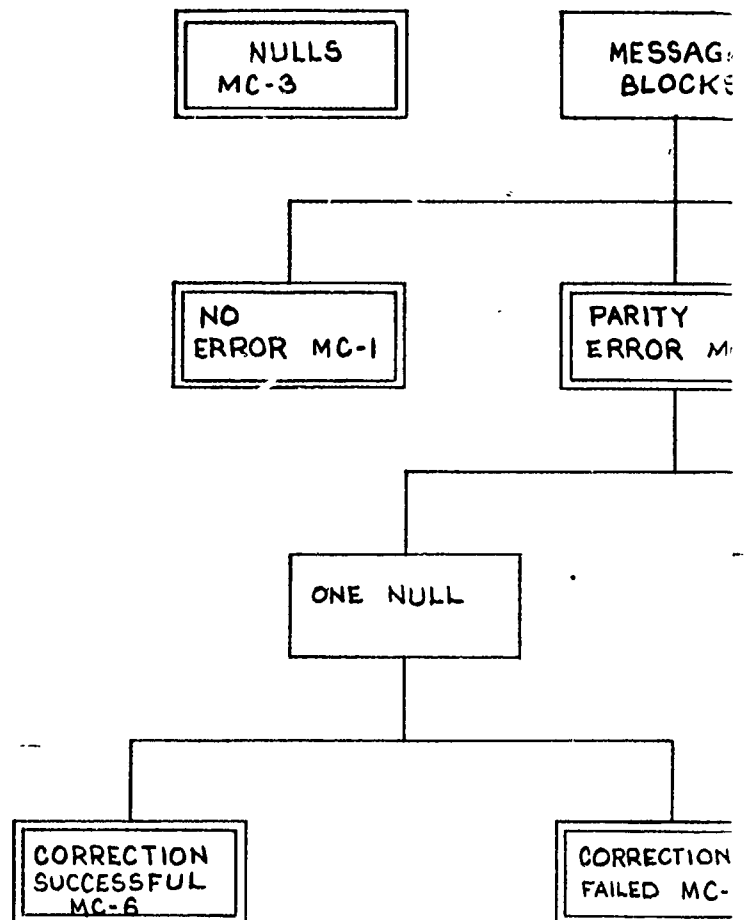
RACK LOCATION AREA-2

MECHANICAL COUNTERS

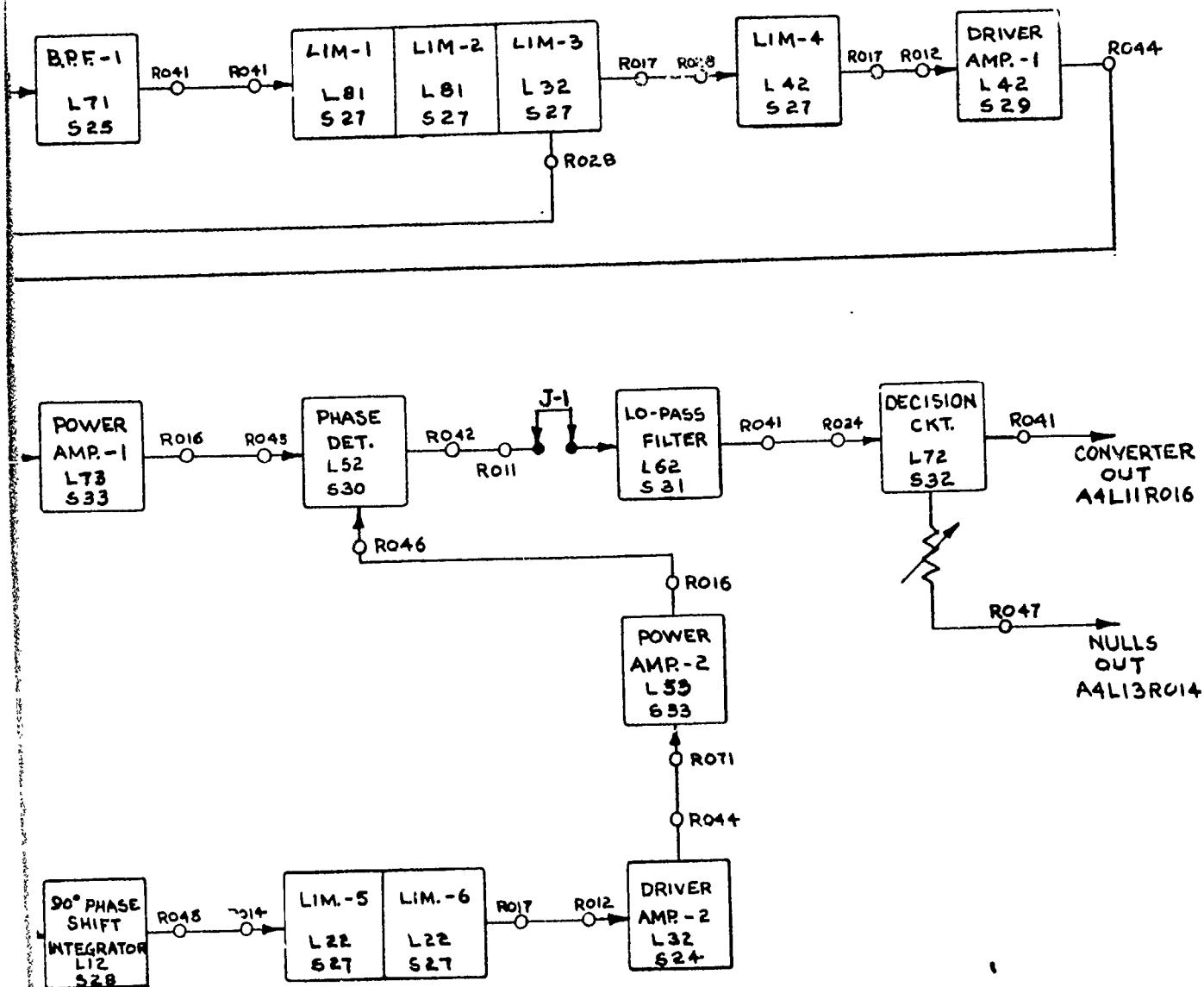


TEST FACILITY
COUNTER FUNCTIONS

13D-10

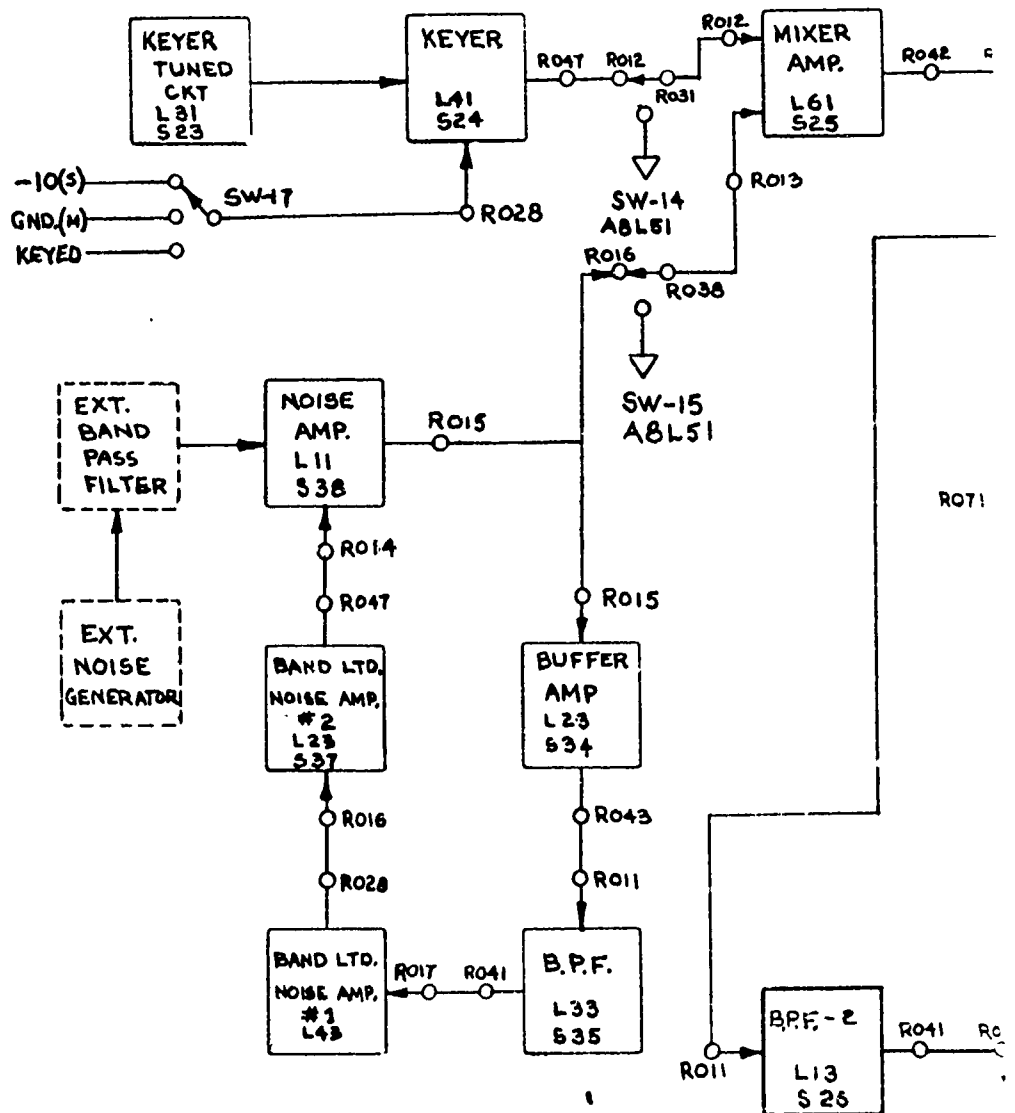


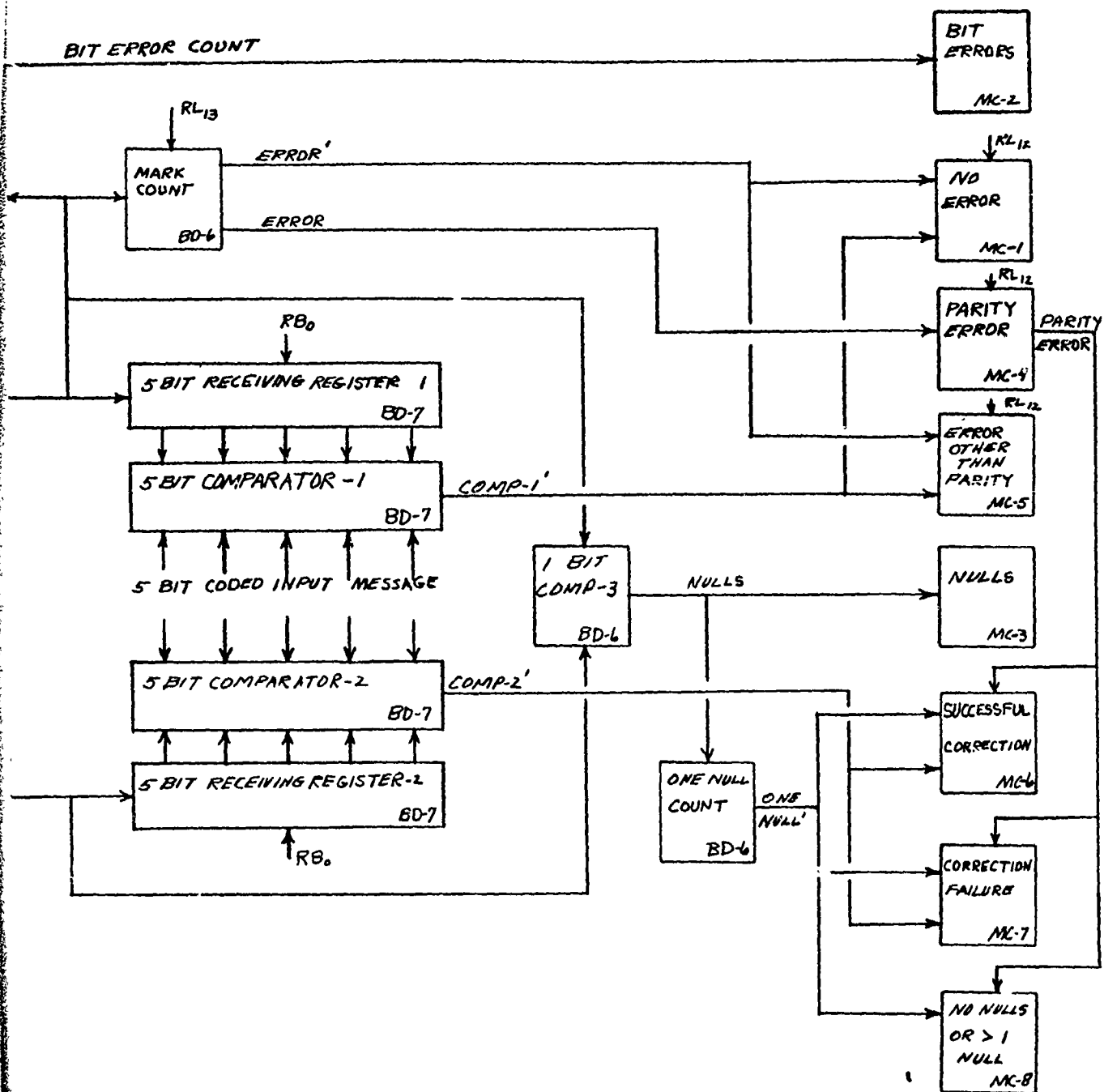
DOUBLE OUTLINED BLOCKS REPRESENT MESSAGE CORRECTION STATUS



FSK. KEYER & CONVERTER AREA-B

13D-11





TEST FACILITY
MASTER BLOCK DIAGRAM

13D-12

