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INVESTIGATION OF HIGHLY-DOPED SCHOTTKY-BARRIER FIELD-EFFECT TRANSISTORS

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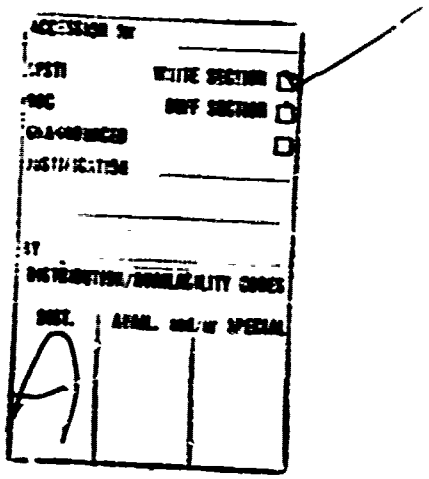

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ABSTRACT

The electrical properties of Schottky-barrier field-effect transistors realized in silicon and GaAs technology have been investigated in the medium and high doping range ($10^{17}cm^{-3}$ to $10^{18}cm^{-3}$) for the conducting channel. This report summarizes the present status of work and describes the significant steps taken in the optimization of microwave properties. In the first chapter design parameters are discussed. The second chapter reports on measured microwave properties as obtained on our best 1 μ silicon and GaAs Schottky-barrier field-effect transistors. The third chapter deals with future improvements expected to be attained. The last chapter summarizes the most important steps taken in GaAs technology to achieve optimal device properties and describes the latest results obtained on transistors with high doping concentrations in the conducting channel.

Introduction

Investigation of the electrical properties of Schottky-barrier field-effect transistors with the main emphasis on devices with high doping concentration in the conducting channel has been the topic of this effort. Transconductance, speed limitations and noise behavior have been of main interest in the study of transistors realized in the one-micron structure for gate length and contact separation in silicon and gallium-arsenide technology. The theoretical background of this work is presented in Scientific Reports AFCRL-69-0072, AFCRL-69-0376, AFCRL-70-0446 and AFCRL-71-0251. Best experimental results obtained on silicon MESFET's (MEtal-Semiconductor FET) in the $10^{17}/cm^3$ doping range are a transconductance g_m = 40 mmho per mm gate width, a maximum frequency of oscillation f_{max} = 15 GHz and a noise figure F_0 = 5 db measured at 6 GHz.

In silicon technology it was difficult to realize well-operating transistors in the $10^{18}/cm^3$ doping range because of breakdown problems. A solution however was found with a sandwich structure for the channel, where the highly-doped conducting layer was covered by a very thin undoped layer. The result of this work is described in the Scientific Report AFCRL-70-0446.

In GaAs technology best high-speed Schottky-barrier field-effect transistors were realized in the 10^{17} doping range with a transconductance g_m = 100 mmho per mm gate width, a maximum frequency of oscillation f_{max} = 40 GHz (extrapolated value) and a noise figure F_0 = 5 db measured at 10 GHz. Doping in excess of $10^{18}/cm^3$ could be achieved here in standard technology.

This report deals with the most important problems which had to be solved during the course of this work and the approaches taken in the realization of optimal Schottky-barrier field-effect transistors.

Microwave Properties of Schottky-Barrier FET's

In this chapter a summary of the microwave properties of Schottky-barrier field-effect transistors is presented. Recently, a maximum frequency of oscillation of 40 GHz was achieved with a GaAs MESFET having a 1μ gate; this value is in excess of what has been obtained with bipolar transistors or other types of FET's. Also the noise figure of the GaAs MESFET is quite low.

The chapter is divided into three parts. In the first, it is discussed how some of the important figures of merit like the gain-bandwidth product depend on device parameters such as geometry, doping, etc. The second part gives measured microwave results on the best of our 1μ Si and GaAs MESFET's. Finally, possible improvements of MESFET's in the future are described.

I Device Design Parameters

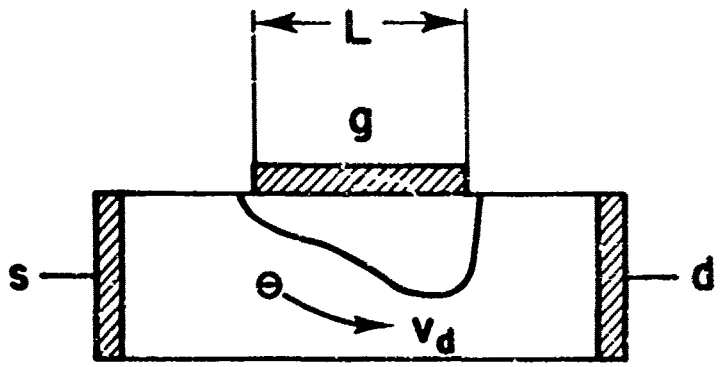
In this section an outline will be given how the intrinsic MESFET has to be designed to give desirable microwave properties. To this end it is necessary to relate the microwave properties to the device structure. In a very approximate way this can be relatively easily accomplished for the gain-bandwidth product ω_0, the unilateral power gain U, and the optimum noise figure F_0.

A. Gain-bandwidth product ω_0

The gain-bandwidth product ω_0 for FET's is defined as the ratio of transconductance g_m and gate-capacitance C_g:

$$\omega_0 = \frac{g_m}{C_g} \quad .$$

In an RC-coupled cascaded amplifier, $\omega_0/2\pi$ is the frequency at which the voltage gain per stage has decreased to unity. In switching applications $1/\omega_0$ is roughly the gate charge and discharge time constant if driven by another



CURRENT I THROUGH DEVICE

$$I = \frac{Q}{\tau}$$

Q = MOBILE CHARGE BELOW GATE

τ = CARRIER TRANSIT TIME BELOW GATE

TRANSCONDUCTANCE g_m

$$g_m = \frac{\delta I}{\delta V_g} = \frac{\delta Q}{\delta V_g} \cdot \frac{1}{\tau} + \frac{\delta \frac{1}{\tau}}{\delta V_g} \cdot Q \approx \frac{C_g}{\tau}$$

VOLTAGE GAIN – BANDWIDTH PRODUCT ω_o

$$\omega_o = \frac{g_m}{C_g} \approx \frac{1}{\tau} = \frac{\bar{v}_d}{L}$$

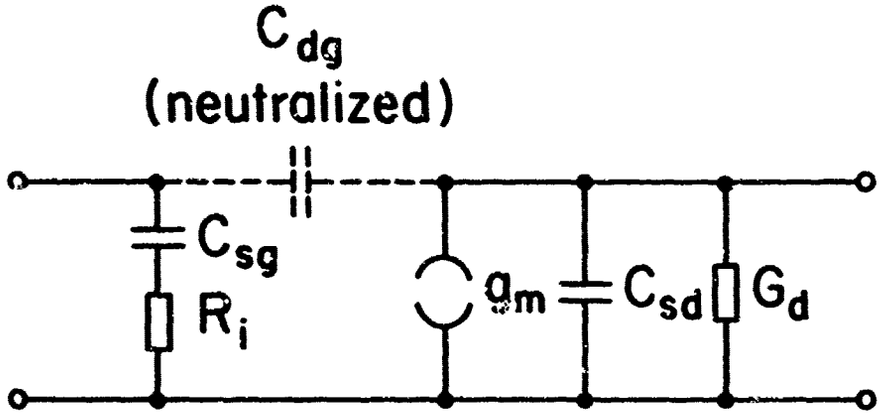
FIG. 1 Derivation of the gain-bandwidth product ω_o of FET's.

FET. In Fig. 1 a derivation of ω_0 is sketched. To first order, the modulation of the drift velocity by the gate voltage can be neglected, therefore the gate voltage controls the drain current almost entirely by changing the mobile charge in the channel. Under these circumstances ω_0 is about equal to the reciprocal of the transit time of the mobile carriers in the channel below the gate electrode. This result is true for all types of FET's and is found in a similar form for other charge-controlled devices, like bipolar transistors.

High ω_0 requires high drift velocities and small gate-lengths L. The implications of these requirements will be discussed later.

B. Unilateral power-gain U

One of the simplest definitions of power gain is the unilateral power-gain U. It is obtained if first the feedback reactance in the device is neutralized and then input and output matched to signal source and load. The derivation of U for a simplified equivalent circuit of a FET is given in Fig. 2.[1,2] The main assumption made in the derivation is that the absolute value of the transconductance g_m is practically independent of frequency. This is well-fulfilled for FET's in their useful operating range. As shown in the figure, U depends on $1/\omega^2$. This means that U decreases by 6 dB if the frequency is doubled. At the (angular) frequency $\omega = \omega_{max}$ the power gain is unity, up to this frequency the device can be used as amplifier or oscillator, therefore ω_{max} is called the (angular) maximum frequency of oscillation. It is important to note that ω_{max} is proportional to ω_0, therefore a short transit time is also beneficial for the power gain. In addition, resistive losses at the input and output have to be kept so small by having a small resistance in the channel R_i and a small output conductance G_d. For the MESFET's, ω_{max} is usually about two to five times ω_0.



Unilateral power gain U:

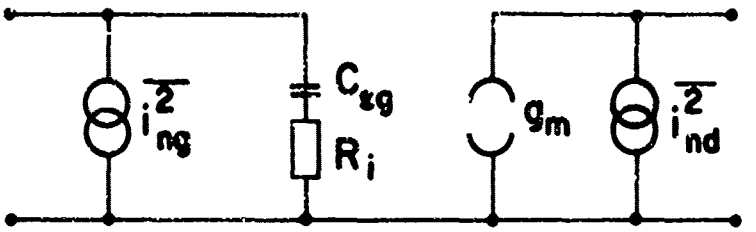
$$U = \frac{|Y_{21}|^2}{4\,\mathrm{Re}\,Y_{11}\,\mathrm{Re}\,Y_{22}}$$

$$\approx \frac{g_m^2}{4\omega^2\,C_{sg}^2\,R_i\,G_d} = \left(\frac{\omega_{max}}{\omega}\right)^2$$

Maximum frequency of oscillation:

$$\omega_{max} = \frac{g_m}{2C_{sg}}\,\frac{1}{\sqrt{R_i\,G_d}} = \frac{\omega_0}{2}\,\frac{1}{\sqrt{R_i\,G_d}}$$

Fig. 2 Simplified derivation of the unilateral power-gain U of FET's.



Channel noise:

$$\overline{i_{nd}^2} = 4kT\,\Delta f\,R_n^{-1}$$

$$R_n^{-1} \approx g_m$$

Induced gate noise:

$$\overline{i_{ng}^2} = 4kT\,\Delta f\,g_{11}$$

$$g_{11} \approx \omega^2 C_{sg}^2 R_i$$

Noise figure (noise match):

$$F \approx 1 + 2\sqrt{R_n g_{11}} = 1 + 2\frac{\omega}{\omega_0}\sqrt{R_i \cdot g_m}$$

$$(\omega \ll \omega_0)$$

FIG. 3 Noise sources in a FET (simplified theory).

C. Optimum noise figure F_0

As shown in Fig. 3, there exist two noise sources in a FET,[3] the channel noise, roughly proportional to g_m, and the induced gate noise, which depends on the gate-capacitance C_{sg} and the effective resistance R_i of the channel. For a certain admittance of the signal source, the noise figure reaches its minimum value F_0. As follows from the figure, low values of F_0 are obtained if ω_0 is high. In addition, the effective channel-resistance R_i should be small. This derivation neglects hot-electron effects which are of importance in GaAs devices and which will be dealt with later.

The previous discussions have shown that a short carrier-transit time τ in the channel is of prime importance for the gain-bandwidth product ω_0, the power-gain U, and the noise-figure F_0. Furthermore, small values of the effective channel-resistance R_i and the output conductance are beneficial, especially for U and F_0. How these requirements can be met will be discussed in the following sections.

D. The transit-time

As follows from Fig. 1, the transit-time τ is given by

$$\tau = \frac{L}{\bar{v}_d} \quad ,$$

where L is the gate length, and $\bar{v}_d$ a mean value of the drift velocity in the channel. Short transit times are obtained by small gates and high drift velocities. However, both quantities are limited, L by the technology and v_d by the semiconductor material. In Fig. 4, the drift velocity versus electric field for three n-doped semiconductors is shown. The drift velocity in Ge and Si saturates at high fields with Si having a somewhat higher v_d than Ge. In GaAs with increasing field the drift velocity first reaches a peak and then decreases, the behavior giving rise to the Gunn effect.

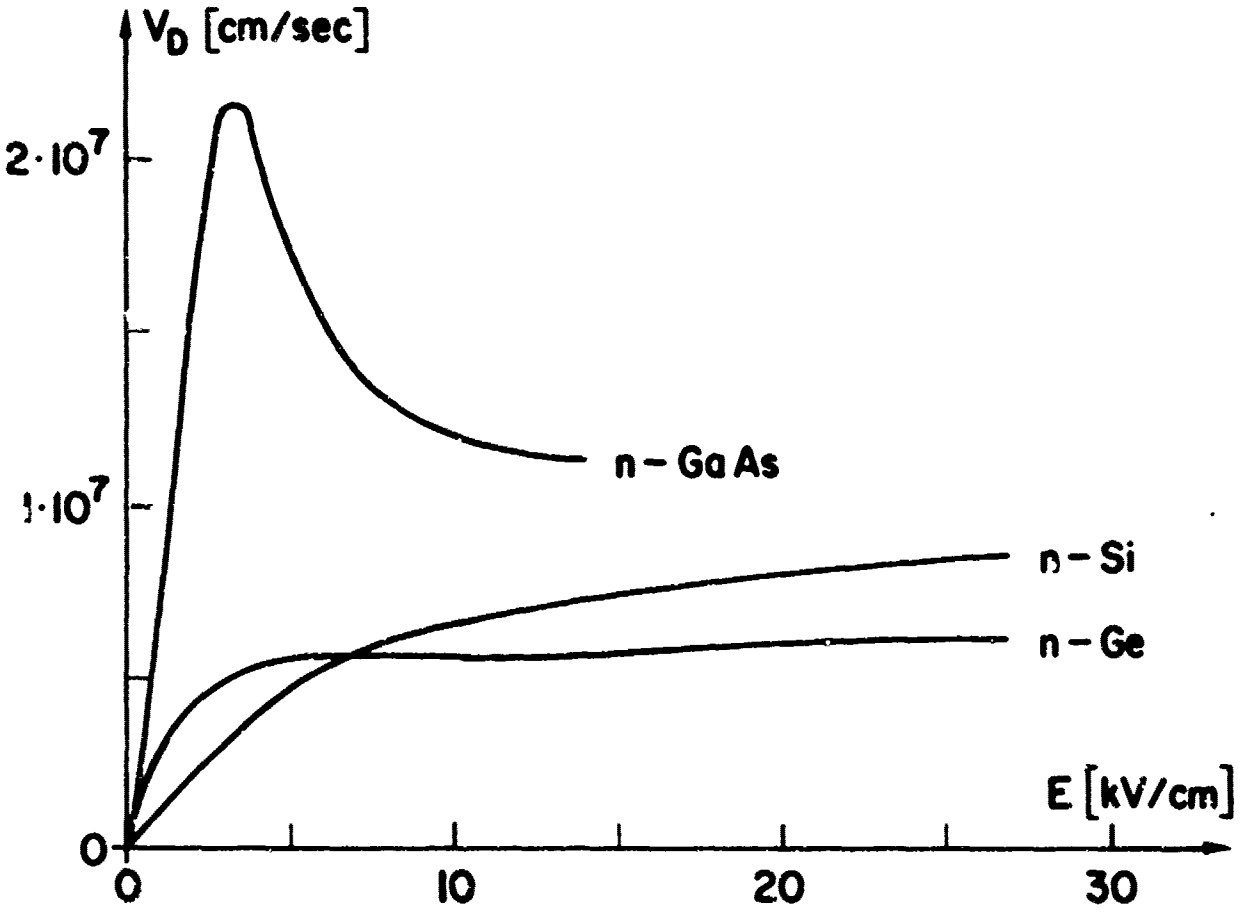


FIG. 4 Drift velocity versus field for three n-doped semiconductors.

For FET's the peak drift velocity is of importance, accordingly GaAs is about two times better than Si. Moreover, the mobility of GaAs and its breakdown voltages are superior to those of Si, therefore GaAs is more suited for FET's especially with high doping concentrations in the channel. In our laboratory MESFET's have been made with Si as well as GaAs.

In order to make full use of the available drift velocity, the transistors have to be designed to have sufficiently high electric field in the channel. The field in the channel can be adjusted with the pinch-off voltage W_0. Very roughly, the mean-field E_m is given by

$$E_m \approx W_0/L \quad .$$

For 1μ gates, values of W_0 of the order of 1 volt are required to reach drift-velocity saturation. The pinch-off voltage W_0 depends on the channel thickness a and the doping N_D:

$$W_0 = \frac{eN_D}{2\varepsilon\varepsilon_0} a^2 \quad .$$

To obtain the desired value of W_0 the product $N_D \cdot a^2$ has to be properly adjusted. Experimentally[2] and theoretically[4] it turns out that it is advantageous to make the channel-thickness a small and the doping high. This not only gives high transconductance but also relatively small output conductance and small influence of the feedback capacitance. Because of breakdown of the gate diode, doping is limited to about $10^{18}\,cm^{-3}$, which leads to a channel thickness of the order of 0.1 micron.

For a FET for the X-band region, in addition to making full use of the finite drift velocities, the gate length has to be made small, about 1 micron. This is still difficult to achieve with conventional photolithography. With the use of the projection printing technique[5] it was possible to fabricate 1 μ gates.

E. Device structure

For a gate in a FET it is required that it should be insulated in some way from the channel, but still be able to control the charge density there. This can be accomplished by insulated gates and junction gates, as shown in Fig. 5:

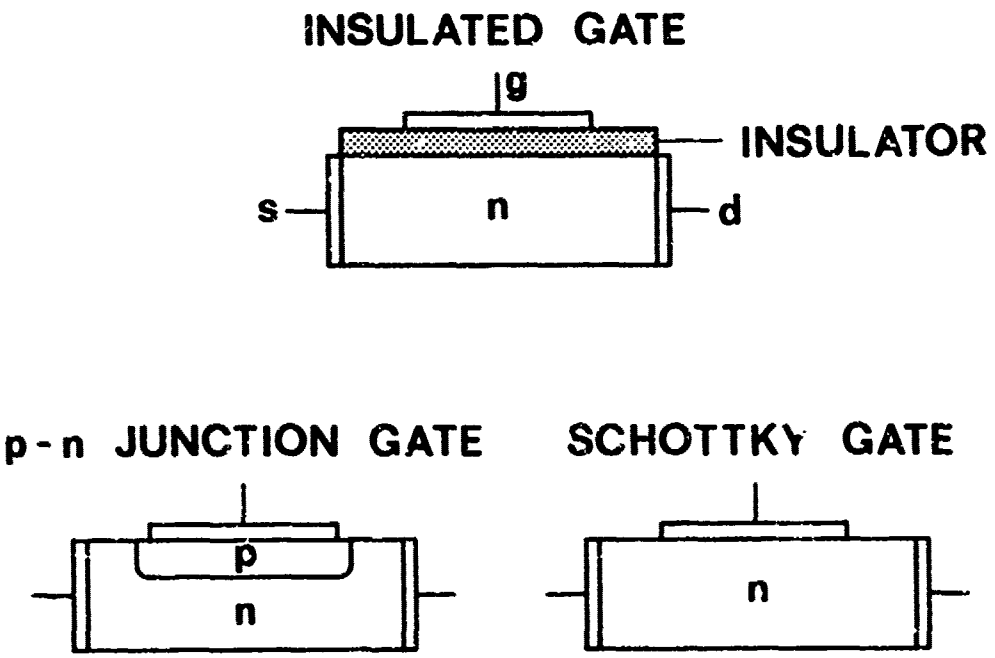


FIG. 5 Possible gate types for FET's.

The best-known insulated gate is the MOS structure. For junction gates there are two possibilities, the p-n junction gate and the Schottky gate. We have chosen the latter for two reasons. First, it is very simple to fabricate by evaporating a suitable metal on a semiconductor. This is important if one works close to the limits of the photolithographic techniques, where simple structures are needed. Second, Schottky contacts

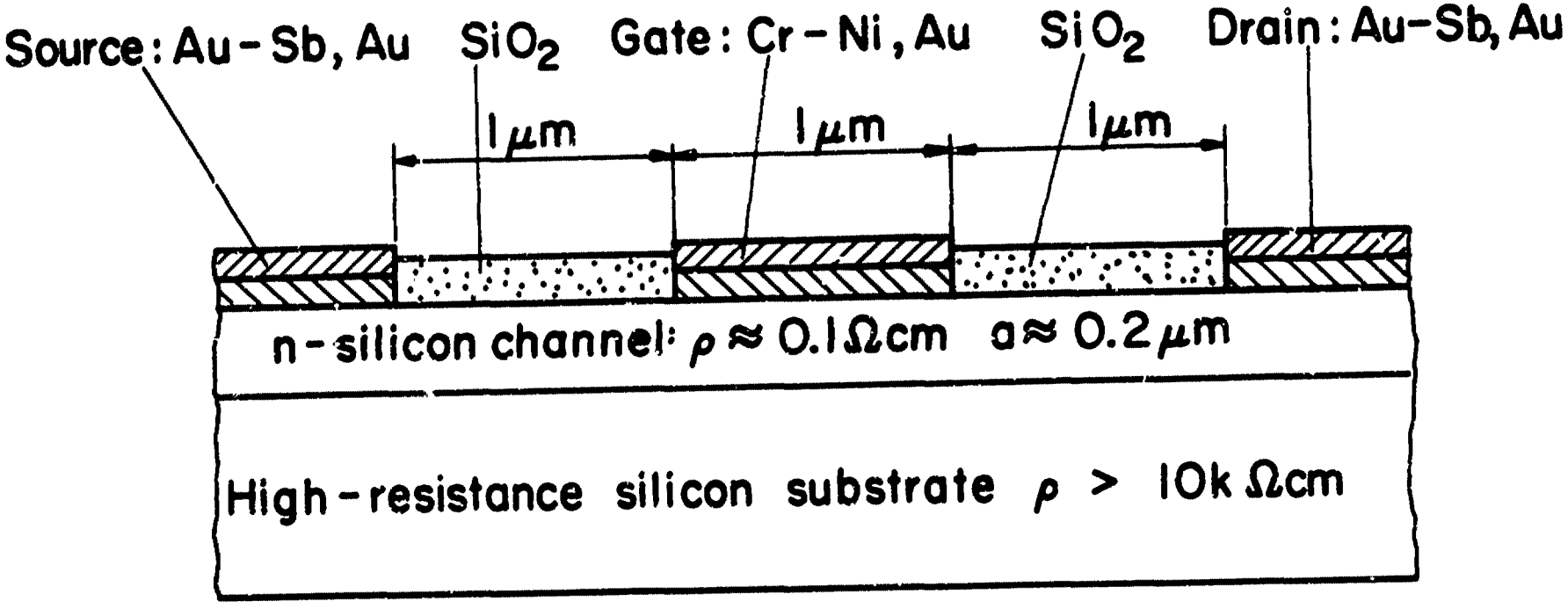


FIG. 6 Cross section of Si MESFET's.
GaAs MESFET's are very similar.

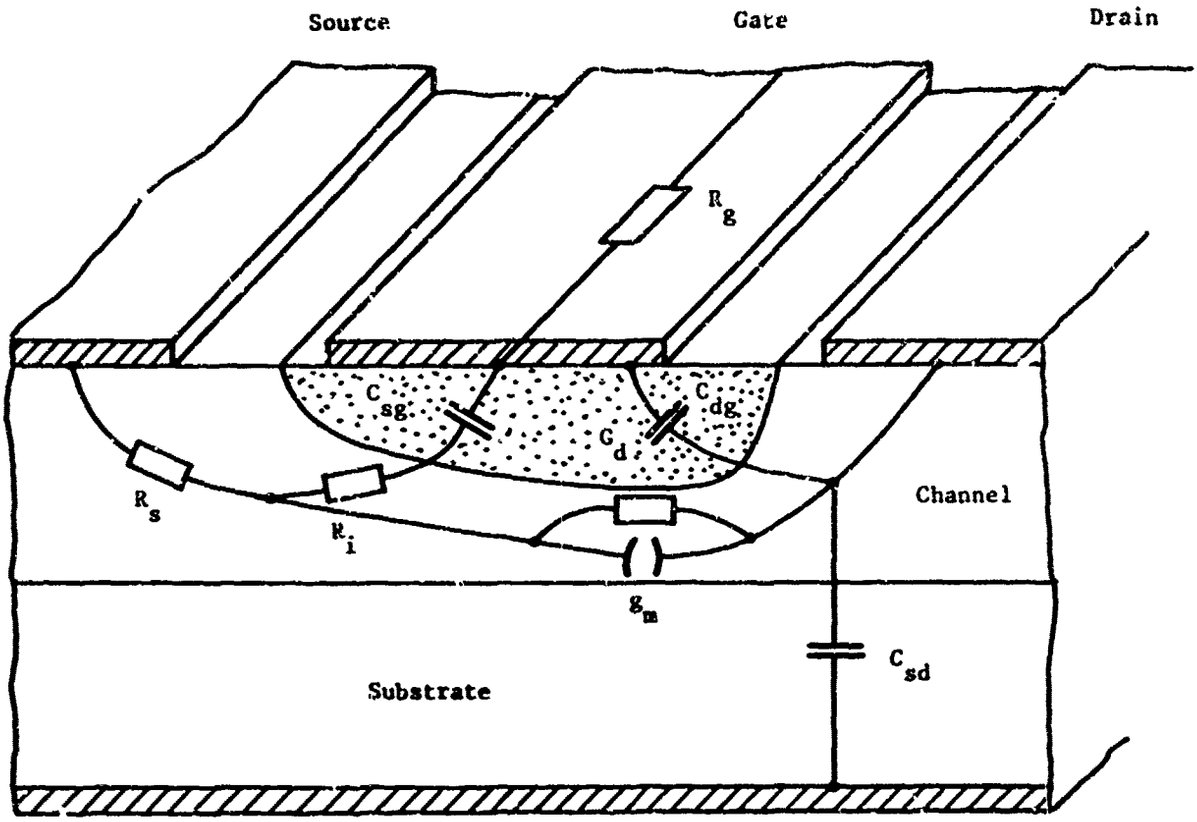
are possible on many semiconductors. For instance, no satisfactory insulated gate exists on GaAs, but it is quite easy to obtain good Schottky gates.

The cross section of our MESFET's is shown in Fig. 6. The structure is about equal for Si and for GaAs MESFET's. As a substrate, high-resistive silicon[6] or semi-insulating GaAs is used. In this way parasitic capacitances and resistive losses on the drain can be avoided which would be quite large if the more common p-doped substrate were used. The channel is an epitaxially grown layer with a thickness between 0.1 and 0.2 micron and n-doped between $10^{17}cm^{-3}$ and $10^{18}cm^{-3}$. The gate, as already mentioned, is one micron long and has been made of various metal layers: palladium on Si, chromium-rhodium on GaAs, and chromium-nickel on both semiconductors. The ohmic contacts at source and drain are obtained by alloying evaporated gold-antimony to the silicon and gold-tellurium or gold-germanium-tellurium to the gallium arsenide. It should be mentioned that self-aligning ohmic contacts[7] are used, a technique which facilitates the photo-processing considerably. All the initial metallizations are very thin. In order to decrease their resistance they are electroplated with gold.

2. Microwave Properties

Three different set-ups have been used to measure the microwave properties of the transistors. One of them measures the scattering parameters in the range 0.1 GHz to 16 GHz. A second is for direct measurement of the maximum available gain MAG by tuning the transistors at input and output. It operates from 2 GHz to about 18 GHz. Finally, the noise figures of the transistors is measured from 2 GHz to about 15 GHz as a function of the source admittance.

These measurements not only yield the important device parameters like power gain and noise figure, they are also the basis for establishing the equivalent circuit which is a convenient vehicle for device design. The



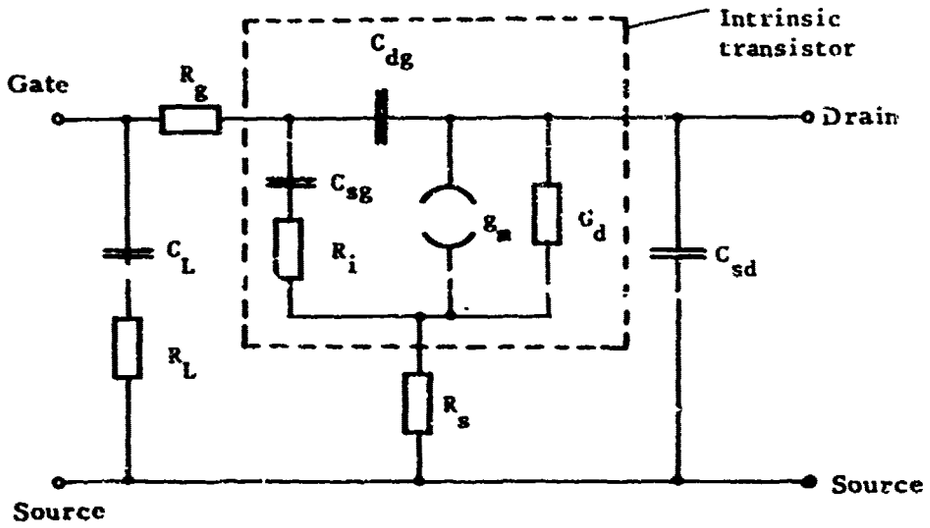


FIG. 7 Equivalent circuit of MESFET's. The upper part of the figure shows the location of the circuit elements in the device structure. Not shown in the structure are the gate pad elements C_L and R_L.

equivalent circuit of Si- as well as GaAs-MESFET's are qualitatively equal. It is shown in Fig. 7 together with the location of the elements in the device structure. To simplify the figure, the noise sources are omitted. The equivalent circuit consists of the intrinsic transistor and the parasitic elements. The intrinsic transistor is considered as that part of the structure below the gate. The most important of its properties have already been discussed. The parasitic elements consist of the series-resistance R_s of the channel in the interelectrode spacing between source and gate, the pad-parasitics R_L and C_L, and the effective-resistance R_g of the gate metallization. To the series-resistance R_s the contact resistance of the ohmic contact at the source has to be added. Considerable efforts were necessary to reduce these parasitics, and the gate-metallization resistance R_g and the pad parasitics were successfully reduced to a small level. The only parasitic element still of significance is the series-resistance R_s.

A. Si-MESFET

A photomicrograph of the best Si-MESFET is shown in Fig. 8. The ring-like structure is the 1μ gate, which has a circumference of 400 μ. The drain is the circular area in the center. The gate can be connected to the outside world by means of four gate pads. The large number was necessary to decrease the parasitic influence of the gate metallization.[2] With better electroplating procedures now available, two pads would suffice. As is also visible in the photograph, the n-conducting epi-layer in the vicinity of the pads has been etched away, therefore the pads are surrounded by the high-resistive substrate only. This measure not only decreased the resistive losses of the gate pads, but also their capacitance.

In Fig. 9 power gain and noise figure are shown. At 7 GHz the maximum available gain MAG is 6 dB, and at 15 GHz the maximum frequency of oscillation f_{max} is reached. Below about 6 GHz the device becomes conditionally unstable, a behavior very often found in FET's with small losses. The optimum noise-figure F_0 is very low. At 6 GHz, 5 dB is found, and at 9 GHz, where the

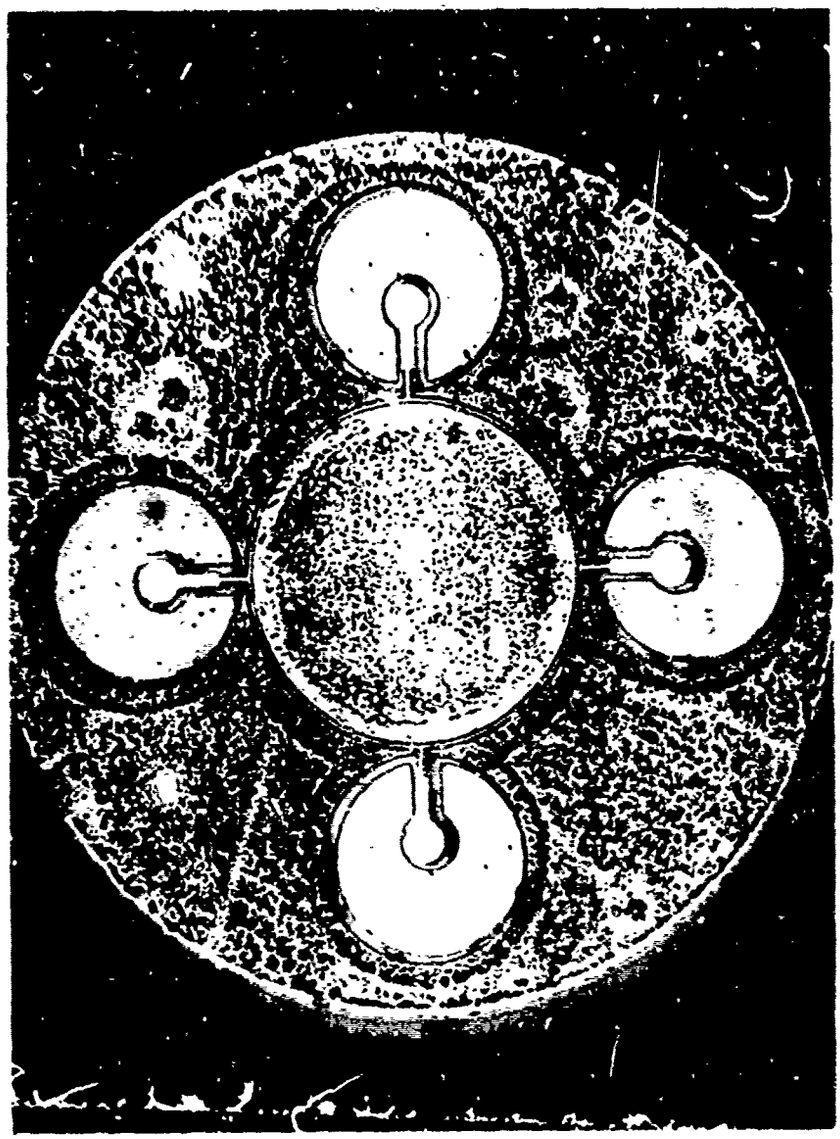


FIG. 8 Microphotograph of a Si-MESFET. The gate is the ring-like structure in the center of the photograph and has the dimensions 1 μ x 400 μ . The drain is the circular area in the center. The areas around the four gate pads are visible where the epitaxial layer has been etched away.

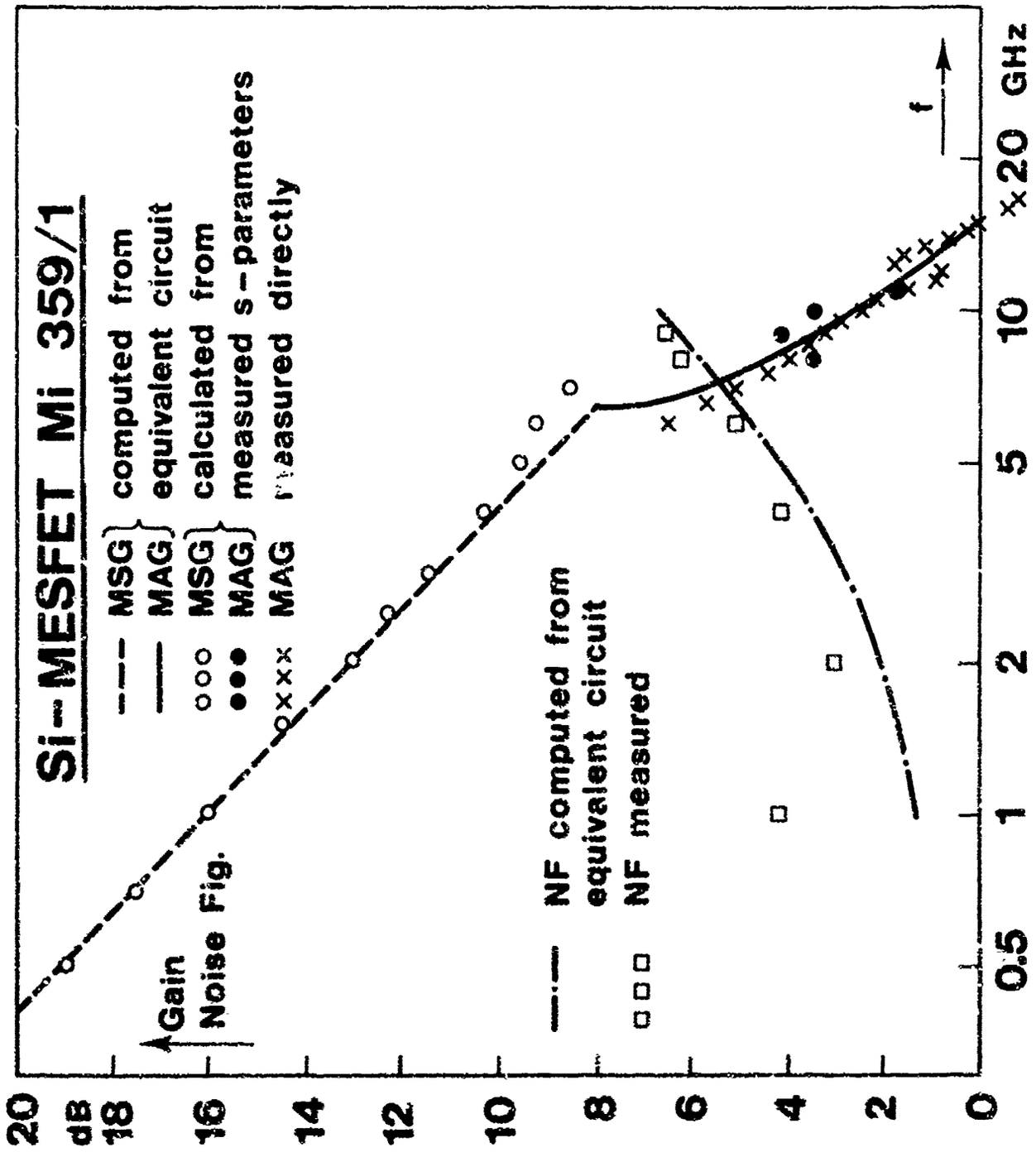


FIG. 9 Power gain and noise figure of a Si-MESFET. The maximum frequency of oscillation is 15 GHz.

gain is already quite small, F_0 is only 6.5 dB. Compared to bipolar transistors the power gain at high frequencies is about equal, however, the noise figure of MESFET's is lower by as much as 2 dB.

B. GaAs-MESFET

As discussed earlier, GaAs is a favorable material for MESFET's because of its high drift velocity. On the other hand, it is a very demanding material from a technological point of view.

A microphotograph of our best 1μ GaAs-MESFET[9] is shown in Fig. 10. The design is very similar to the Si-MESFET. Because of the higher transconductance per unit gate-width of GaAs as compared to Si, it was possible to reduce the gate width to 150μ. This, together with improved electroplating techniques decreased the effective gate-metallization resistance considerably. Therefore, it was feasible to use one gate pad only instead of four as in the Si device. In order to keep pad parasitics low, most of the gate pad is placed on the semi-insulating substrate.

In Fig. 11, the microwave properties of the device are given. The unilateral-gain U, computed from the measured S-parameters is nearly 12 dB at 10 GHz and still 9 dB at our measuring limit of 16 GHz. Therefore the device is well-suited for applications at X-band and the lower K-bands. It is difficult to obtain a precise value for the maximum frequency of oscillation f_{max}, because it is considerably above the frequency limits of our equipment. The straight line extrapolation shown in Fig. 11 gives a value for f_{max} of about 55 GHz. A more careful investigation by means of numerical extrapolations from the equivalent circuit of the device indicates a value of 40 GHz. This means that for the first time a transistor has reached the millimeter region.

The optimum noise-figure F_0 is 2.7 dB at 4 GHz and 5.1 dB at 10 GHz. For comparison, the noise figures of various semiconductor devices in the microwave region are given in Fig. 12. Below about 10 GHz the GaAs-MESFET is better than mixer diodes, and below about 7 GHz better than tunnel diodes.

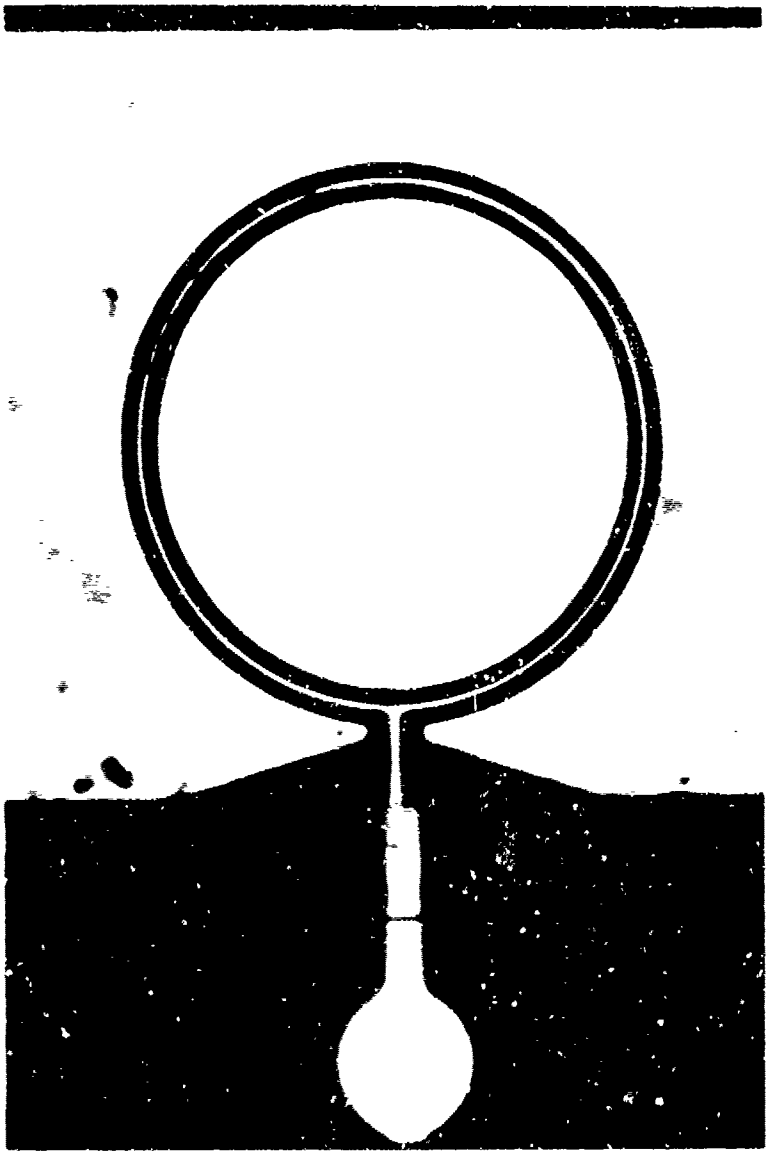


FIG. 10 Microphotograph of a GaAs-MESFET. Gate dimensions are 1[illegible] x 150 micron. The gate pad is placed on the semi-insulating substrate. The dark horizontal line below the metallizations and crossing the gate pad is the boundary between substrate and epi-layer.

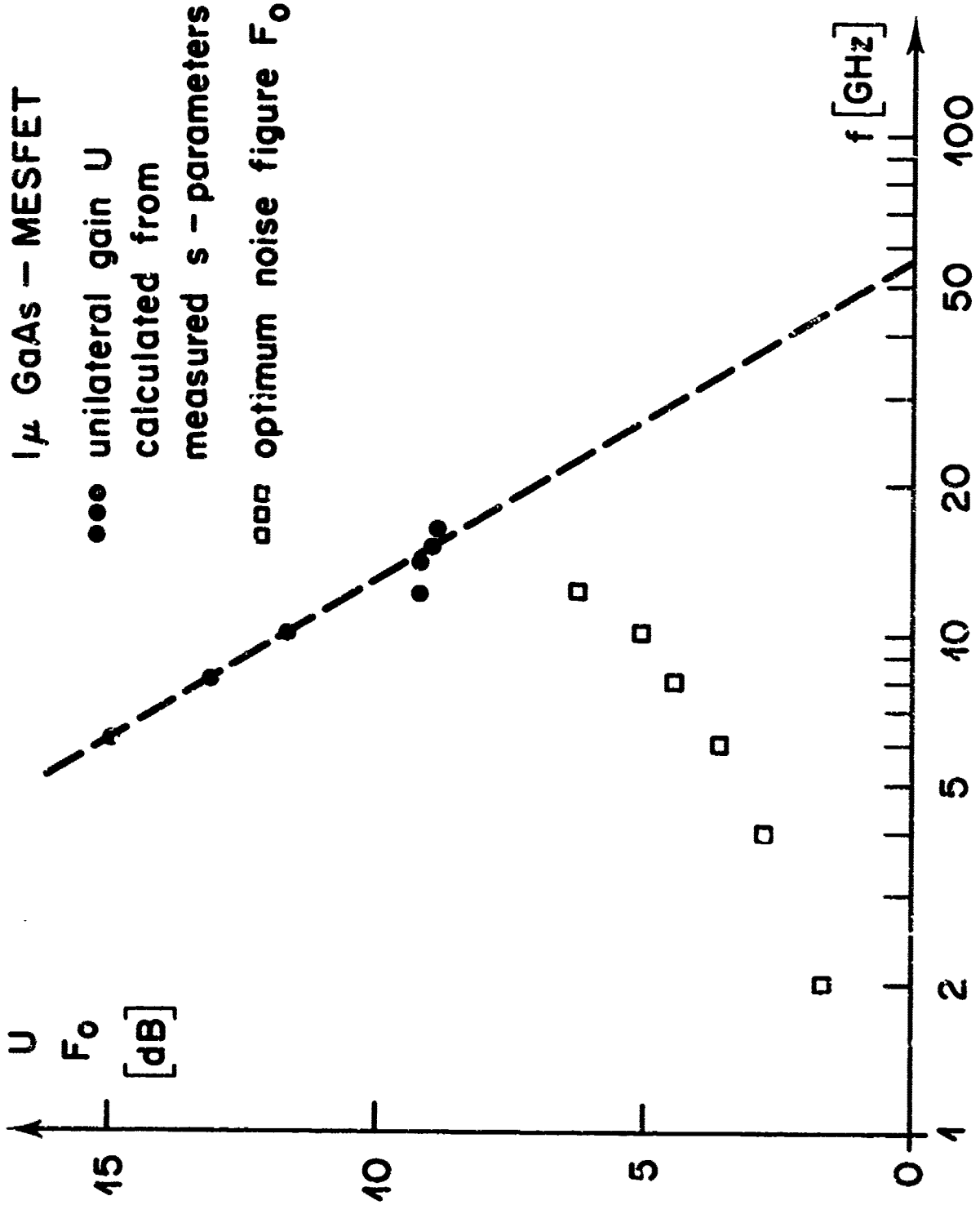


FIG. 11 Power gain and noise figure of a GaAs-MESFET.

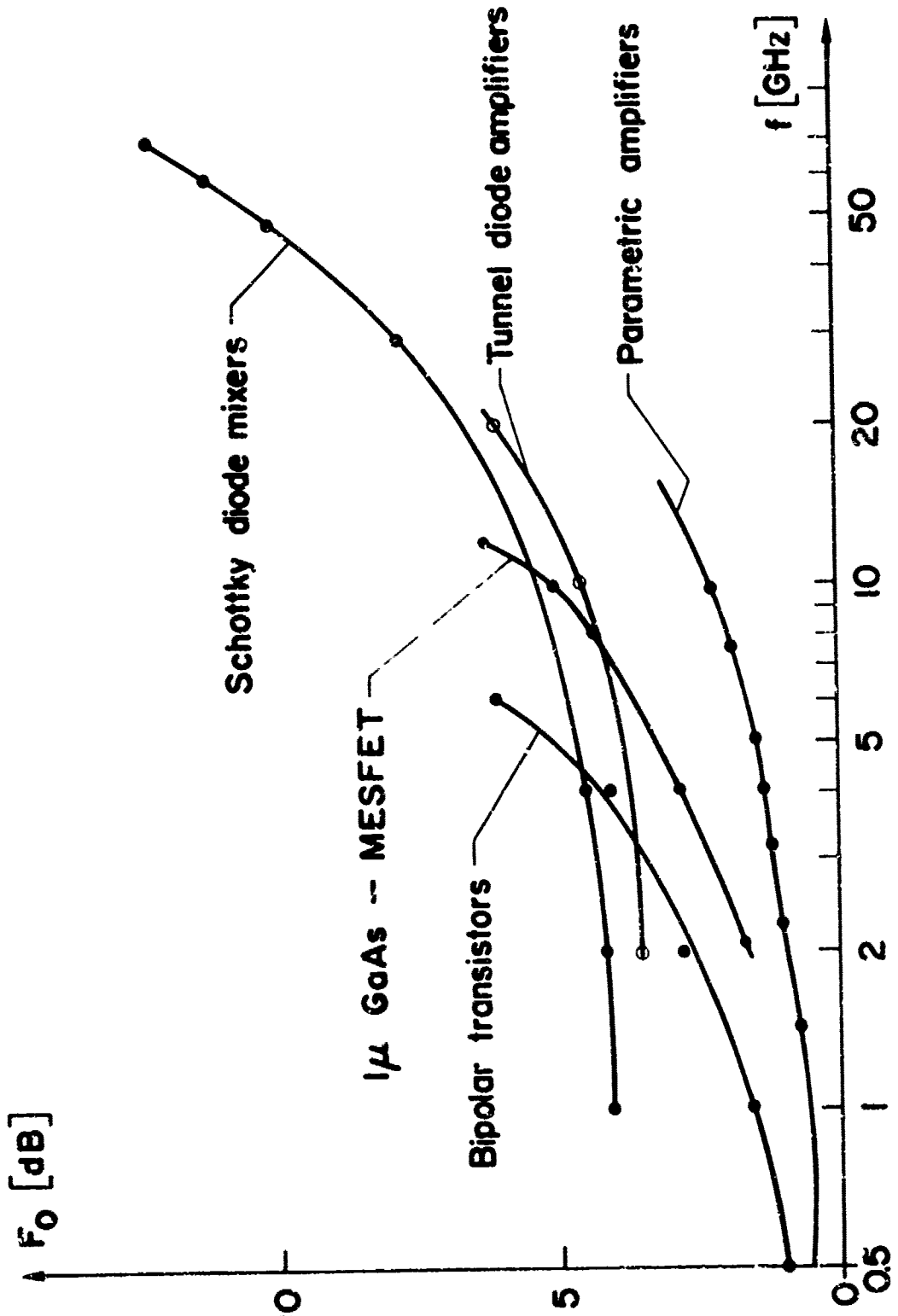


FIG. 12 Noise figure of various solid-state devices. Status at the end of 1971.

Compared to bipolar transistors, GaAs-MESFET's have a similar noise curve but shifted to about twice the frequency. At low frequencies the MESFET is not far away from room-temperature parametric amplifiers. Accordingly, MESFET's are good low-noise devices.

It is not very easy to achieve low-noise operation with GaAs-MESFET's, the reason being that at high fields an excess noise source exists in GaAs which is absent in Si.[10] It is due to the intervalley scattering of electrons between the central conduction valley and the satellite valleys, the same mechanism which gives rise to the Gunn effect. To avoid this excess noise the field in the channel has to be kept low by fabricating devices with a sufficiently small pinch-off voltage W_0 and a large channel aspect ratio L/a. The device discussed here has $W_0 \approx 1.5$ V and $L/a \approx 6$.

3. Possible Future Improvements

The previous section has shown that MESFET's already have quite good microwave properties. Here it will be discussed what improvements might be possible in the future. There are three ways: Reduction of parasitics, use of better semiconductor materials, and smaller gate length.

A. Reduction of parasitics

In present MESFET's the main parasitic element is the series-resistance R_s in the source region (see Fig. 7). It is due to the resistance of the channel in the interelectrode spacing between source and gate, and due to the resistance of the source ohmic contact. Computer simulations show that without R_s the Si-MESFET would have an f_{max} of about 35 GHz.

The series resistance can be decreased by either increasing the doping in the source-gate spacing or by decreasing the spacing itself. The former might be possible with some additional technological steps but perhaps at the expense of the simplicity of the device fabrication.

The latter is possible too, but if such an improved masking technique is available then it might be advantageous to decrease the gate length too. This will be discussed later.

In GaAs, in principle, R_s should be quite small because of the high mobility of this material. Unfortunately, in our present devices the mobility is about a factor of two below its bulk value. Moreover, the resistance of the ohmic contact at the source electrode contributes significantly to R_s. However, these problems can be solved eventually and f_{max} is expected to reach values of about 60 GHz. In addition the noise figure should decrease.

B. Use of better semiconductor materials

A semiconductor material for FET's should have drift velocity, mobility and breakdown voltage as high as possible. Unfortunately, for many semiconductors not all of these parameters are known. Exceptions are Si, Ge and some of the III-IV compounds. From the knowledge available on the latter, it is clear that better materials than GaAs exist. For instance, InP seems to have 1.5 times the peak drift velocity of GaAs. A considerable increase of the drift velocity should occur if In is alloyed to GaAs and As to InP.[11] In both cases the central conduction valley is shifted toward the valence band, and the distance between central valley and the satellite conduction valleys increased. Therefore, intervalley scattering is made more difficult, which not only leads to a less-pronounced negative differential conductivity region but to higher peak drift velocity too. Calculated drift-velocity curves for the InAsP ternary alloy series are given in Fig. 13.[11] Nearly a factor of two can be gained in drift velocity as compared to GaAs. Moreover, because intervalley scattering is suppressed, the noise associated with it should disappear. However, a serious drawback of these ternary alloys is the reduced bandgap which results in a smaller breakdown voltage (the breakdown regions are indicated by dotted lines in Fig. 13). For this reason, the two ternary alloys mentioned might not be optimal in every respect for FET use, but they illustrate that by tailoring the band structure

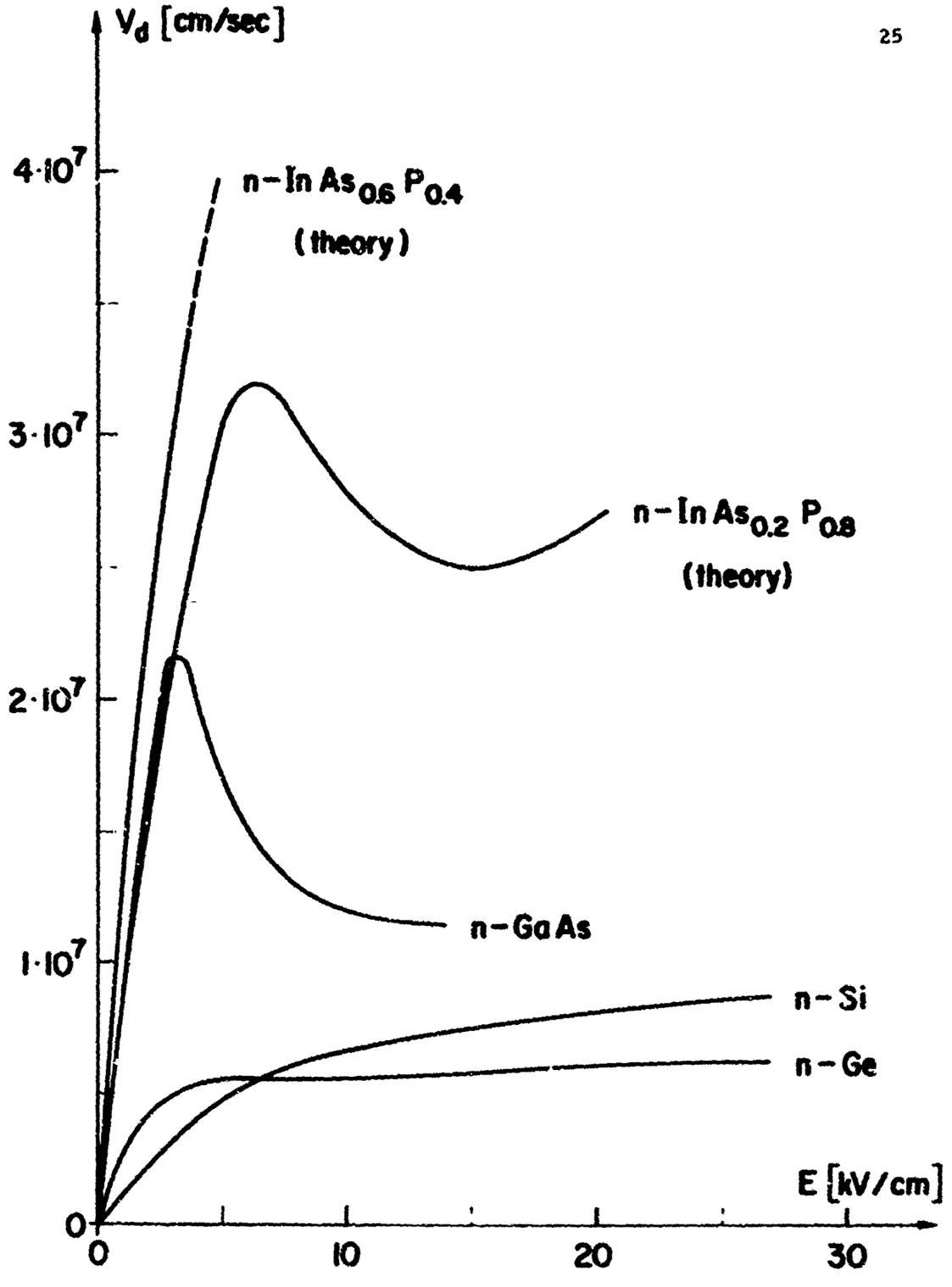


FIG. 13 Theoretical drift velocities of various InAsP alloys. For comparison, drift velocities of Ge, Si and GaAs are also plotted.

of certain semiconductors it might be possible to obtain a more favorable material. To master a new semiconducting compound technologically is a difficult and time-consuming task. Therefore, it is unlikely that such a material might be available in the near future.

C. Smaller gate length

By means of photo-projection printing it was possible to realize structures as small as 0.3 micron,[12] and with electron-beam exposure even structures below 0.1 micron.[13] Accordingly, it is feasible technologically to reduce the gate length to below one micron. However, a recent computer study[4] of submicron FET's indicates that some electrical properties, especially output conductance and open-circuit voltage gain, degrade if only the gate-length L is decreased. To retain desirable electrical properties, the channel-thickness a should be decreased together with L, and the channel doping increased. Because of breakdown due to the increased doping, a lower limit for the reduction of L might be about 0.1 micron. In the near future it should be possible without too much difficulty to decrease the gate length to about 0.5 micron. This might increase the power gain and the maximum frequency of oscillation by roughly a factor of two. Under optimal conditions the Si-MESFET would then have a value of f_{max} of about 30 GHz and the GaAs-MESFET of about 100 GHz. At present it is not clear whether the noise figure would decrease by a similar amount because hot-electron effects which were not too significant for 1 μ structures might become more pronounced, especially if the voltage levels are not reduced.

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GaAs Technology

The results described in the previous section have been achieved with the following technological steps:

a) GaAs epitaxy was performed in a horizontal, two-temperature zone reactor - 800°C at the gallium source and 750°C at the location of the semi-insulating GaAs substrate - using $AsCl_3$ diluted in hydrogen as a carrier gas. In a first step a thin layer (2000 Å) of undoped GaAs (> 100 Ohm cm) was deposited to reduce crystallographic imperfections and to minimize autodoping with chromium in the upper conducting layer. In this way, carrier mobility in the channel was improved from 2500 to about 3000 $cm^2/Vsec$, and the loop effect usually observed in the I/V characteristics of transistors was reduced. The latter effect was more pronounced in the case of very thin conducting layers ($\leq$ 2000 Å) doped up to 10^{18} per cm^3 or higher.

b) Doping of the conducting channel layer was done by admission of H_2S into the reactor instead of H_2Se or SiH_4 or tin doping of the Ga-source. Reproducibility from run to run was improved significantly, especially on ⟨ 111 ⟩ surfaces, where doping concentrations up to 3×10^{18} per cm^3 could be achieved. Reproducibility of epi-layer preparation on ⟨ 100 ⟩ surfaces tried occasionally, was not as good by far as on ⟨ 111 ⟩ surfaces. Maximum doping concentration obtained here was 8×10^{17} per cm^3.

c) To reduce gate-land parasitics, which degrade the intrinsic device properties, the gate lands were placed onto oxide in direct contact with the semi-insulating substrate (without the conducting epi-layer in between). This structure was achieved by selective epitaxy using pyrolytic silicon-dioxide as a local mask. To maintain a planar structure, about 3000 Å of GaAs were etched off in a 0.8% NaOCl solution at 80°C prior to the epi-process.

d) Silicon dioxide used for masking and device protection was deposited pyrolytically. Uniform layers of 1000 to 1500 Å thickness were obtained at 670°C admitting $Si(CO_2H_5)_4$ and purified forming gas (94% N_2, 6% H_2) into a horizontal flow reactor. Adhesion of photoresist was improved by subsequent annealing in hydrogen at 700°C.

e) As a new gate-contact material a sandwich of chromium and rhodium is used instead of chromium nickel. Schottky gate breakdown was improved this way and in addition by strong reduction of all mechanical wafer treatments. Other materials tried as gate-contact materials were: Platinum, which did not allow spreading of gold tellurium in the area of ohmic contacts, and palladium which exhibited a poor ohmic behavior.

f) For the preparation of ohmic contacts a new system was designed which allowed wide variations of the heating cycle for alloying of the contact material into GaAs. The contact resistance of gold tellurium, for example, was reduced and obtained more reproducibly for very short heating cycles.

The system developed is capable of accomplishing wafer heating to the desired temperature of 500°C within 20 seconds. The cooling-down time to about 300°C is 25 seconds. The wafer was kept at the high temperature until microscopical observation showed the onset of alloying. In general, this takes about 10 seconds. The equipment is sketched in Fig. 14.

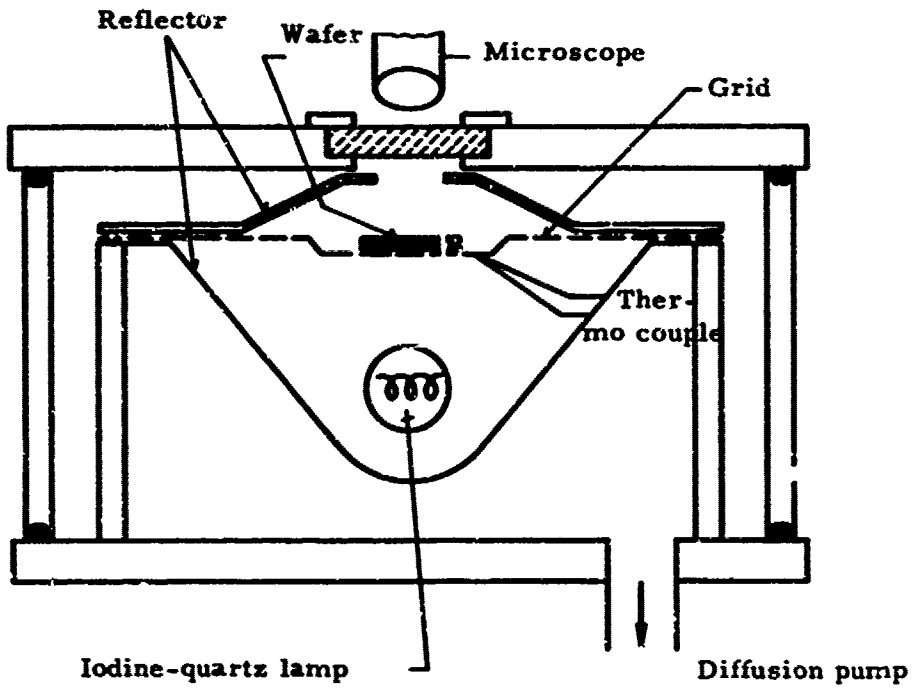

Fig. 14 Experimental set-up for alloying of the ohmic contact material into GaAs.

It consists of a vacuum chamber for pump-down to better than 10^{-4} mm Hg. The wafer with the deposited metal (Au/Te) turned upwards is placed onto a widely-meshed grid. Heating is performed by means of a 250 Watt iodine-quartz lamp. It is controlled by a thermocouple attached close to the wafer. Because of differences in thickness and reflectivity it is important for shortest alloying cycles to observe the wafer through a microscope and to switch-off the lamp as alloying starts.

Compared to the previous procedure, where contact heating was applied, alloying with this system is more reproducible. The contact resistance has a comparably low spread between 10^{-5} and 10^{-6} Ohm/cm^2, which corresponds to best values reported in the literature. The spread still observed can roughly be related to channel doping and thickness. High doping and thickness usually yield lower contact resistances.

Another approach taken in the preparation of ohmic contacts, which yielded lower contact resistances for low doping levels in the channel was taken by deposition of a layer of gold-tellurium-germanium and alloying it into GaAs. The time-temperature heating cycle is less critical here. The maximum temperature can be lowered to about 400°C which reduces leakage problems of the gate contact.

g) Electroplating of gold was performed to reinforce the metallization of the gate and ohmic contacts. Galvanic connections were provided to the gate to avoid gate isolation during the plating process, which is caused by the high diffusion voltage of used metals to GaAs. To reduce widening of the gate a plating-deplating procedure was developed and optimized.

The technological steps taken for device improvement apply just as well for devices with low or medium doping concentration in the channel (10^{17}/cm^3) as for devices exceeding the 10^{18}/cm^3 doping range. More critical for the latter are tolerance problems especially in channel thickness and in carrier distribution within the channel. Drain leakage, a too large pinch-off voltage, and early Schottky gate breakdown are the most usual consequences. Channel doping with sulfur, avoidance of a graded channel profile with high doping towards the surface, the introduction of an undoped transition layer between the semi-insulating substrate and the channel, the use of chromium-rhodium as a gate material and the newly-employed technique for making ohmic contacts have enabled the realization of well-working GaAs Schottky-barrier FET's with channel doping exceeding 10^{18} carriers per cm^3. These devices have not been optimized with

respect to microwave properties. Technology has been kept simple avoiding selective epitaxy for reduction of parasitics and performing gold-plating without additional masking steps to provide galvanic connections to the gate.

Best results obtained with devices prepared under these simplified conditions are a transconductance g_m = 110 mmho per mm gate width and a maximum frequency of oscillation f_{max} = 16 GHz. Noise figures have been measured up to 10 GHz and it turned out that they are by about 5 dB higher than for best microwave MESFET's (F_0 > 10 dB at 10 GHz). Part of the excessive noise is due to gate-land losses, but in addition inter-valley scattering is believed to be more pronounced in case of high doping.

Previous and Related Contracts

Contract No. F 19628-68-C-0343
Schottky-Barrier Transistor
Karsten E. Drangeid
For Air Force Cambridge Research Laboratories, Office of Aerospace Research, United States Air Force, Bedford, Massachusetts 01730.

Contract No. F 19628-70-C-0094
Investigation of Highly-Doped Schottky-Barrier Field-Effect Transistors
Karsten E. Drangeid
For Air Force Cambridge Research Laboratories, Office of Aerospace Research, United States Air Force, Bedford, Massachusetts 01730.

Previously Produced Publications or Articles Resulting from Total or Partial Sponsorship of the Contract

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Dutch PTT, The Hague, The Netherlands, January 21, 1970.

"Rauschverhalten von MESFET's im Mikrowellen-Gebiet"
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