REPORT R-577 JULY, 1972 UILU-ENG 72-2238

CSL COORDINATED SCIENCE LABORATORY

AD 746391

COMPARISON OF QUASI-NEWTON METHODS FOR THE DC ANALYSIS OF ELECTRONIC CIRCUITS

WILLIAM HSIA KAO

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Security Classification

DOCUMENT CONTROL DATA - R & D

(Security classification of title, body of abstract and indexing annotation must be entered when the overall report is classified)

1. ORIGINATING ACTIVITY (Corporate author)

Coordinated Science Laboratory
University of Illinois
Urbana, Illinois 61801

2a. REPORT SECURITY CLASSIFICATION: UNCLASSIFIED

2b. GROUP

3. REPORT TITLE

COMPARISON OF QUASI-NEWTON METHODS FOR THE DC ANALYSIS OF ELECTRONIC CIRCUITS

4. DESCRIPTIVE NOTES (Type of report and inclusive dates)

5. AUTHOR(S) (First name, middle initial, last name)

William Hsia Kao

6. REPORT DATE	7a. TOTAL NO. OF PAGES	7b. NO. OF REFS
July, 1972	75	18

8a. CONTRACT OR GRANT NO. DAAB-07-67-C-0199;
b. NSF GK-31633
c.
d.

9a. ORIGINATOR'S REPORT NUMBER(S): R-577

9b. OTHER REPORT NO(S) (Any other numbers that may be assigned this report): UILU-ENG 72-2238

10. DISTRIBUTION STATEMENT

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11. SUPPLEMENTARY NOTES

12. SPONSORING MILITARY ACTIVITY

Joint Services Electronics Program through U. S. Army Electronics Command, Fort Monmouth, New Jersey

13. ABSTRACT

In the dc analysis of a circuit the capacitors and inductors in the circuit are replaced by open and short circuits, respectively, and the circuit is solved for constant source values (all time-varying signal sources are set to zero). In the analysis and design of electronic circuits the dc solution is called the quiescent, bias or operating point of the circuit and has many uses. For example, the operation of most electronic circuits is critically dependent on the quiescent point and it is important to know its value and its sensitivity with respect to parameter changes such as temperature, etc. In small signal analysis the quiescent point should be determined in order to calculate accurate small signal models. Finally, in transient analysis the initial states of the capacitors and inductors must be known, and this is accomplished by dc analysis.

DD FORM 1 NOV 65 1473

Security Classification

Security Classification

14 KEY WORDS	LINK A		LINK B		LINK C	
	ROLE	WT	ROLE	WT	ROLE	WT
Quasi-Newton Methods						
Colon, Cermak, Bias 3						
Ecap II, Broyden, Brown, Cancer						

Security Classification

UILU-ENG 72-2238

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This work was supported in part by the Joint Services Electronics Program (U. S. Army, U. S. Navy and U. S. Air Force) under Contract DAAB-07-67-C-0199, and in part by the National Science Foundation under Grant NSF GK-31633.

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COMPARISON OF QUASI-NEWTON METHODS FOR THE DC ANALYSIS OF ELECTRONIC CIRCUITS

BY

WILLIAM HSIA KAO
B.S., University of Illinois, 1970

THESIS

Submitted in partial fulfillment of the requirements
for the degree of Master of Science in Electrical Engineering
in the Graduate College of the
University of Illinois at Urbana-Champaign, 1972

Urbana, Illinois

ACKNOWLEDGMENT

The author wishes to thank specially his thesis advisor Professor Timothy N. Trick for his supervision and suggestions, and Dr. Robert F. Colon who provided valuable research guidance and assistance toward the writing of this thesis project.

Sincere appreciation is also due to the secretarial staff of the Coordinated Science Laboratory for typing the manuscript and to the drafting staff for drawing the figures.

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I. INTRODUCTION

In the dc analysis of a circuit the capacitors and inductors in the circuit are replaced by open and short circuits, respectively, and the circuit is solved for constant source values (all time-varying signal sources are set to zero). In the analysis and design of electronic circuits the dc solution is called the quiescent,bias or operating point of the circuit and has many uses. For example, the operation of most electronic circuits is critically dependent on the quiescent point and it is important to know its value and its sensitivity with respect to parameter changes such as temperature, etc. In small signal analysis the quiescent point should be determined in order to calculate accurate small signal models. Finally, in transient analysis the initial states of the capacitors and inductors must be known, and this is accomplished by dc analysis.

Since electronic devices have nonlinear characteristics, the dc solution involves the solution of a set of nonlinear algebraic equations which describe the circuit. One method of solution is the graphical or load line method. In order to illustrate this method consider the circuit in Figure 1.1. First the i-v characteristic of the nonlinear device is measured and sketched as shown by the solid line in Figure 1.2. Next the driving point characteristic of the linear network is determined as function of the variables i and v. Since the network is linear,

$$v = -Ri + E \qquad (1)$$

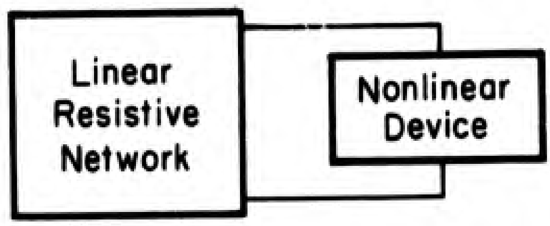


Figure 1.1. A circuit with one nonlinear two-terminal element.

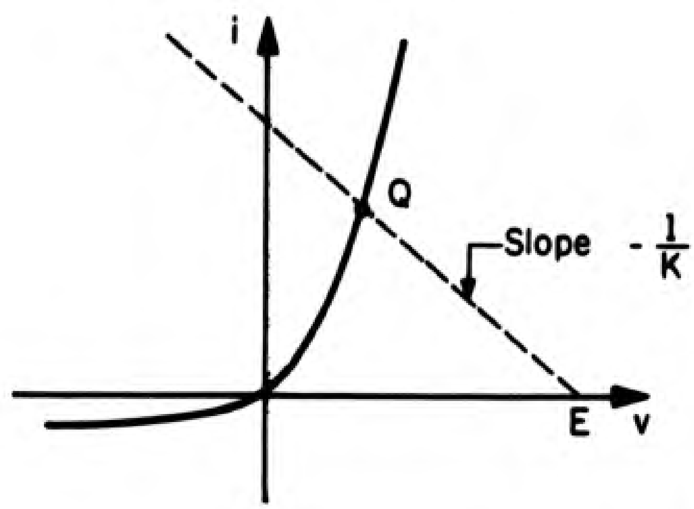


Figure 1.2. Graphical method to obtain solution.

where R is the driving point resistance of the network and E is the Thevenin equivalent voltage. Equation (1) is just the equation for the load line and its intersection with the i-v characteristic of the device determines the quiescent point Q.

In large networks this graphical method is very time consuming, and if more than one nonlinear device is present in the circuit it becomes hopelessly complex. Thus, iterative methods which have been made feasible with the aid of a computer have become increasingly popular. There are many iterative methods available [1] for electronic circuit analysis, but experience has shown that the Newton method and its modifications are the most reliable and efficient [2].

This paper presents a survey of these "Quasi-Newton" methods and compares them in terms of speed, number of iterations and reliability in the dc analysis of transistor circuits. Section II discusses the application of the basic Newton method to the dc analysis of electronic circuits. Also some shortcomings of the Newton method are discussed and suggested modifications to the method for increased reliability and speed are reviewed. In Section III seven different programs for the dc analysis of electronic circuits are introduced. They include the dc programs of ECAP II, BIAS 3, CANCER, the Bell Telephone nonlinear circuit and statistical design program by Cermak and others. Section IV presents the results of the application of these programs to the analysis of a variety of electronic circuits. Finally, in Section V some conclusions are drawn from the comparisons made in Section IV.

II. THE NEWTON METHOD AND ITS MODIFICATIONS

2.1. Circuit Equations

It is assumed that the network contains only linear resistors, constant independent current sources, constant independent voltage sources, diodes, and transistors. The i-v characteristic of the diodes are assumed to be of the form

$$i = I_s(e^{\theta v} - 1) \tag{2}$$

where $\theta = q/kT$. The Ebers-Moll model [3] will be used for the transistor as shown in Figure 2.1 where

$$i_r = I_{cr}(e^{\theta v_{bc}} - 1) \tag{3}$$

and

$$i_f = I_{cf}(e^{\theta v_{be}} - 1). \tag{4}$$

With the given models the network consists of a collection of two terminal elements whose characteristics are linear or exponential. Thus, the network equations can be written in the sparse tableau form [2]

$$A\underline{i} = 0 \quad \text{(Kirchhoff's current law)} \tag{5}$$

$$A^t\underline{e} = \underline{v} \quad \text{(Kirchhoff's voltage law)} \tag{6}$$

$$M\underline{i}_{\ell} + N\underline{v}_{\ell} = \underline{u} \quad \text{(linear branch constraints)} \tag{7}$$

$$\underline{i}_e = \underline{F}(\underline{v}_e) \quad \text{(exponential characteristics)} \tag{8}$$

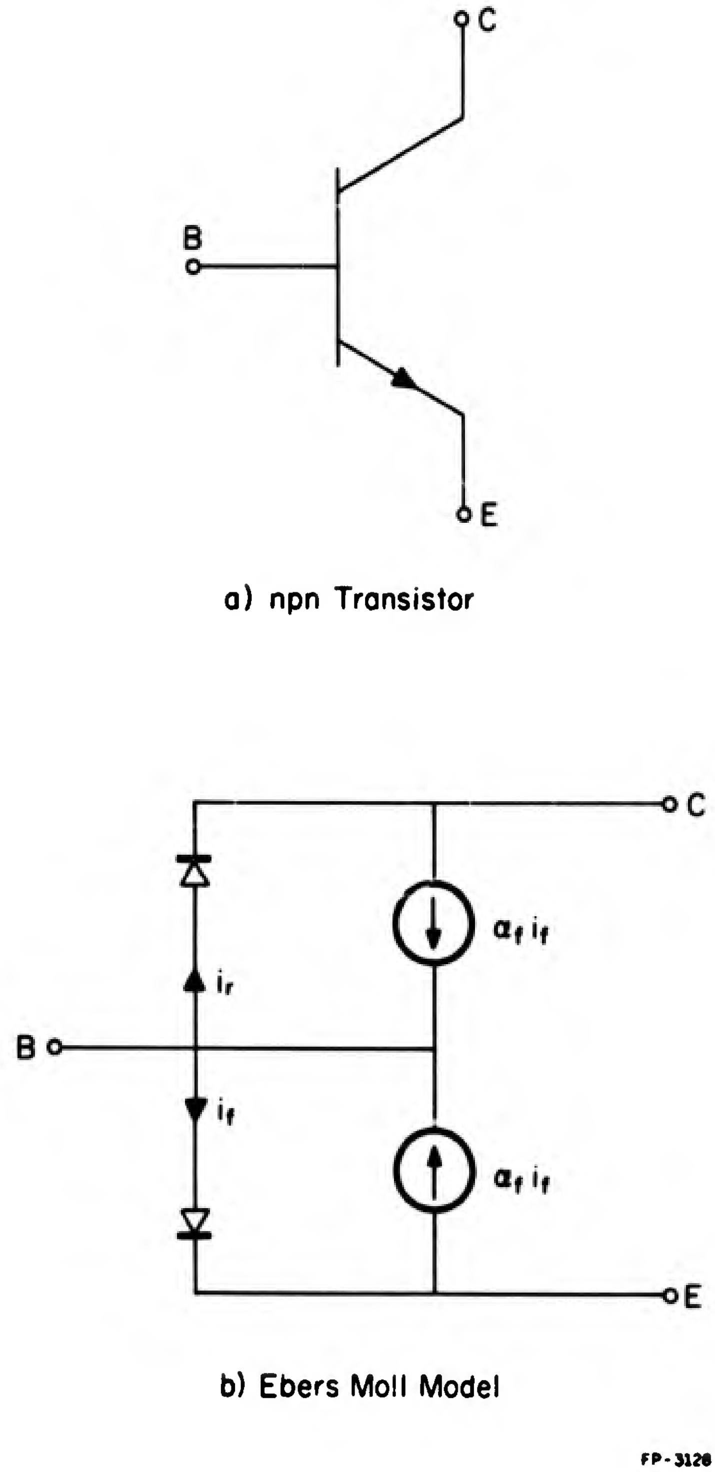


Figure 2.1. Transistor model.

where A is the (n-1) $\times$ b incidence matrix with n = number of nodes, b = number of branches, and superscript t denotes the transpose of a matrix; $\underline{e}$ is an n-1 vector consisting of the node voltages; $\underline{v}$ is a b vector consisting of the branch voltages; $\underline{u}$ is a vector consisting of the independent source values; the vectors $\underline{i} = [\underline{i}_\ell, \underline{i}_e]$ and $\underline{v} = [\underline{v}_\ell, \underline{v}_e]$ are partitioned into the branch currents and voltages associated with the linear elements such as resistors and independent sources and the branch currents and voltages associated with the nonlinear elements such as diodes and transistors

Let the vectors $\underline{i}_e$ and $\underline{v}_e$ be of dimension m (m diodes including diodes in the transistor models). Figure 2.2 illustrates the circuit with the m diodes connected to the m ports of a linear resistive network. This representation will be useful in the next section where the solution of (5)-(8) is discussed.

2.2. The Newton Method

Experience has shown the Newton method with certain modifications to be one of the most efficient methods in the solution of nonlinear networks. The Newton method consists of linearizing the nonlinear characteristics about an assumed solution $(\underline{v}_e^k, \underline{i}_e^k)$ where $\underline{i}_e^k = \underline{F}(\underline{v}_e^k)$. For example consider the circuit in Figure 2.3a. The equations for this circuit are

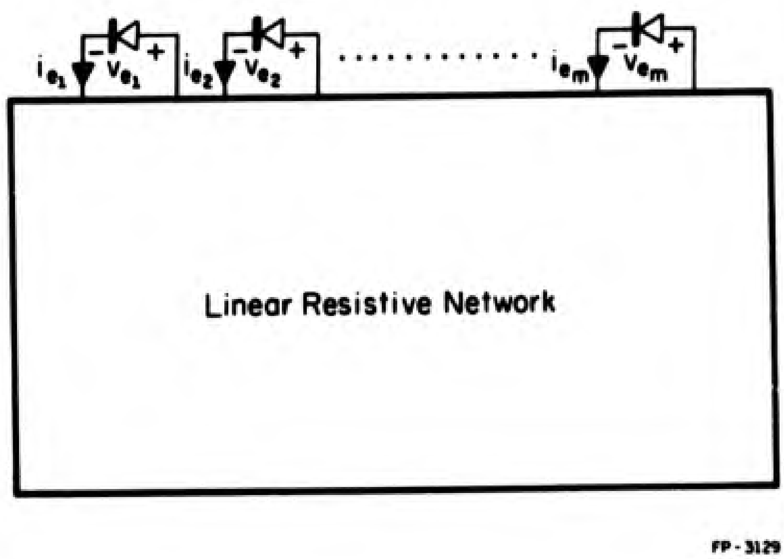
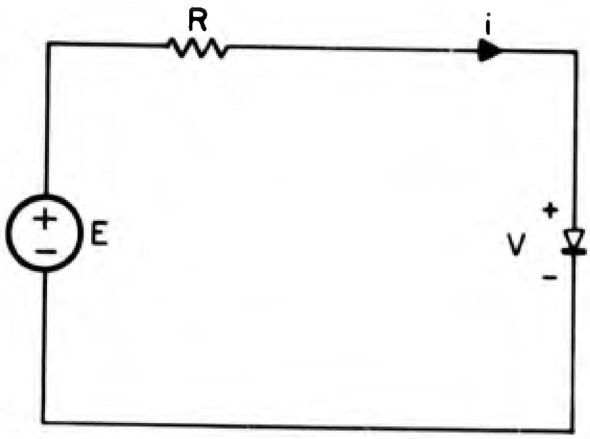
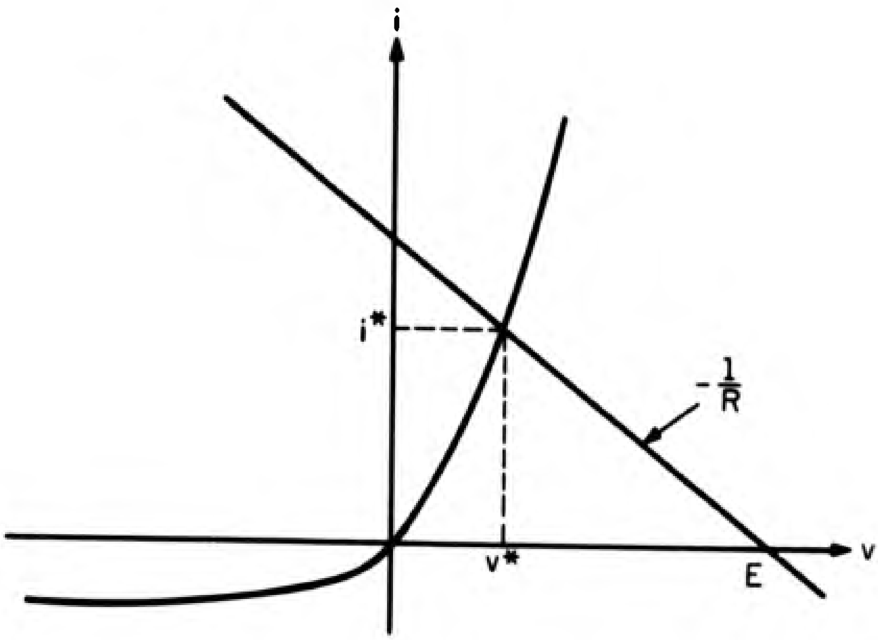


Figure 2.2. Circuit with nonlinear elements removed.



(a) Circuit



(b) Graphical Solution

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Figure 2.3. Solution of a simple diode circuit.

$$Ri + v = E \tag{9}$$

$$i = I_s(e^{\theta v} - 1). \tag{10}$$

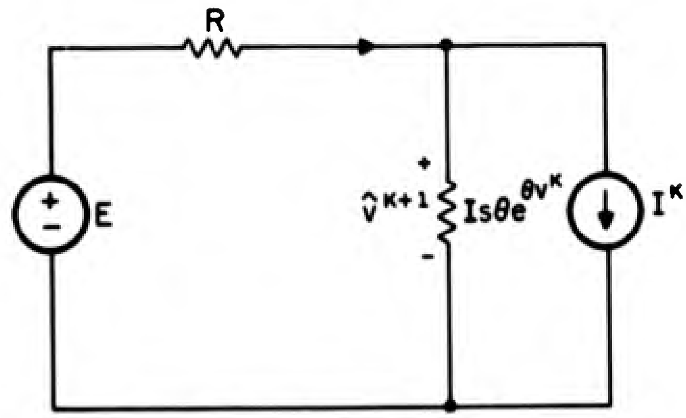
The solution is illustrated graphically in Figure 2.3b. The Newton iterative approach is to expand (10) in a Taylor series about an assumed solution (v^k, i^k).

$$i = I_s(e^{\theta v^k} - 1) + I_s\theta\, e^{\theta v^k}(v - v^k) + r_k \tag{11}$$

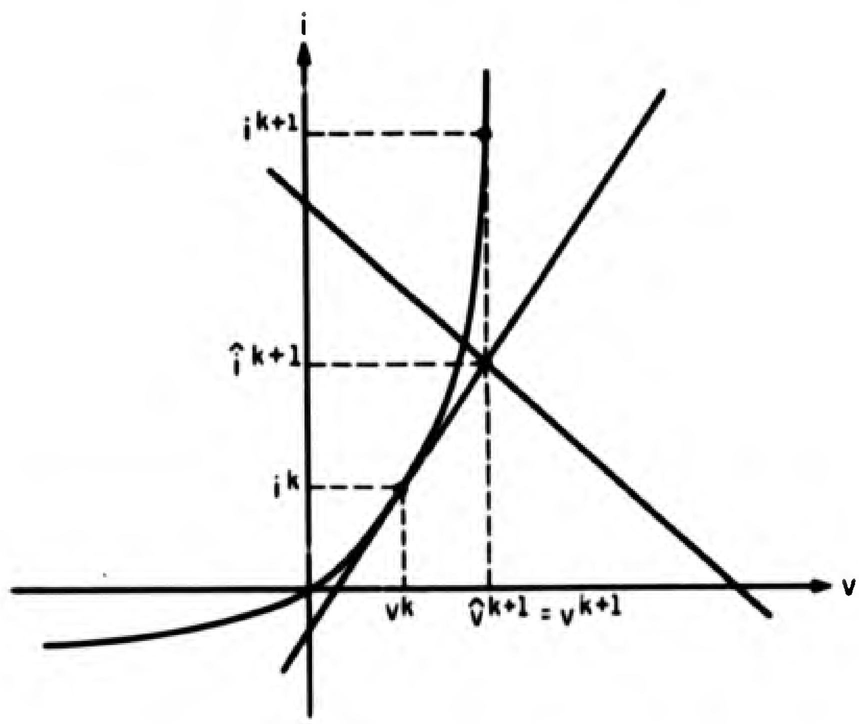
where

$$r_k = \int_{v^k}^{v} (v - \lambda)\, \frac{\partial^2 i}{\partial v^2}(\lambda) d\lambda.$$

Let $r_k = 0$ and solve the linear equations (9) and (11). This method is illustrated in Figure 2.4. In Figure 2.4a note that the diode has been replaced by a linear model with conductance $G^k = \theta I_s\, e^{\theta v^k}$ and a current source $I^k = i^i - G^k v^k$ (see Figure 2.4b). In Figure 2.4b if the point $(\hat{v}^{k+1}, \hat{i}^{k+1})$ does not lie on the i-v characteristic of the diode, then the solution is in error. If we are iterating on voltage then set $v^{k+1} = \hat{v}^{k+1}$ and $i^{k+1} = I_s(e^{\theta v^{k+1}} - 1)$. If we wish to iterate on current, then $i^{k+1} = \hat{i}^{k+1}$ and $v^{k+1} = \frac{1}{\theta} \ln (\frac{i^{k+1}}{I_s} + 1)$. See Figure 2.5 for a graphical illustration of these two types of iteration. The iteration continues until the difference between successive iterates become very small and/or the error which is the distance between the solution of the linear equations and the point for the next iterate on the diode characteristic becomes very small.



(a) Linear Model



(b) Graphical Illustration of Approximate Solution

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Figure 2.4. Iterative solution.

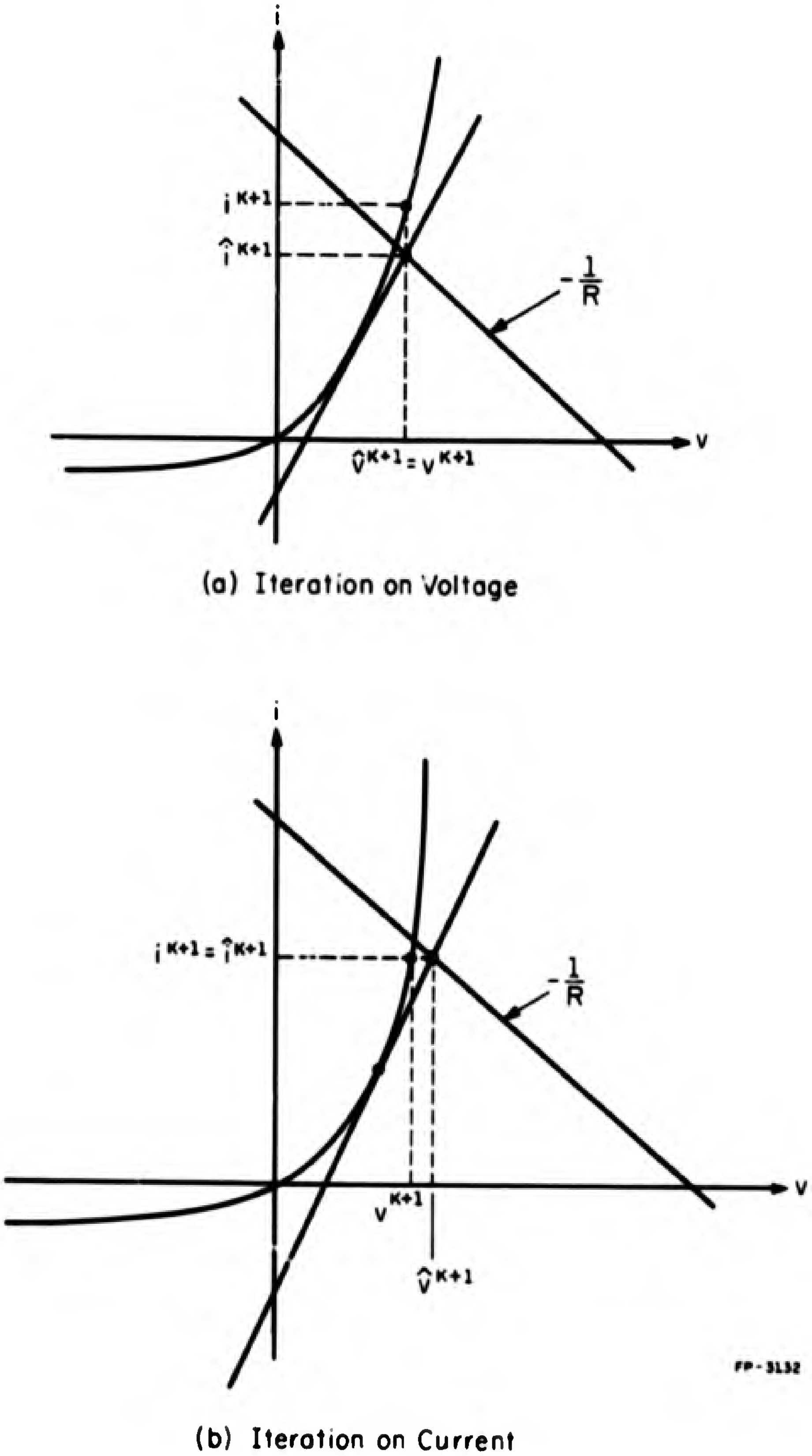


Figure 2.5. Types of iteration.

In observing Figure 2.5 one may ask the question - why always move horizontally or vertically to the diode characteristic curve rather than move back to the diode characteristic with a slope $-\frac{1}{R}$, which would result in the correct solution? Unfortunately, in large networks containing several nonlinear elements the load line is nonlinear and undetermined. However, one could return to the diode characteristic along a line with slope $-\frac{1}{K}$ which passes through the point $(\hat{v}^{k+1}, \hat{i}^{k+1})$ as illustrated in Figure 2.6. To locate point P^{k+1} (the point about which the diode is linearized to begin the next iterate) we first write the linear equation for the dashed line,

$$Ki + v = \hat{v}^{k+1} + K\hat{i}^{k+1} \tag{12}$$

and the diode equation is $i = I_s(e^{\theta v} - 1)$. Also

$$\hat{i}^{k+1} = I_s\theta\, e^{\theta v^k}(\hat{v}^{k+1} - v^k) + i^k. \tag{13}$$

Therefore, (12) becomes

$$KI_s(e^{\theta v} - 1) + v = (v^{k+1} - v^k) + v^k + K[I_s\theta e^{\theta v^k}(\hat{v}^{k+1} - v^k) + i^k] \tag{14}$$

which can be written as

$$KI_s(e^{\theta v} - 1) + v = v^k + (1 + KI_s\theta e^{\theta v^k})(\hat{v}^{k+1} - v^k) + KI_s(e^{\theta v^k} - 1)$$

or

$$KI_s e^{\theta v} + v = v^k + (1 + KI_s\theta e^{\theta v^k})(\hat{v}^{k+1} - v^k) + KI_s e^{\theta v^k}. \tag{15}$$

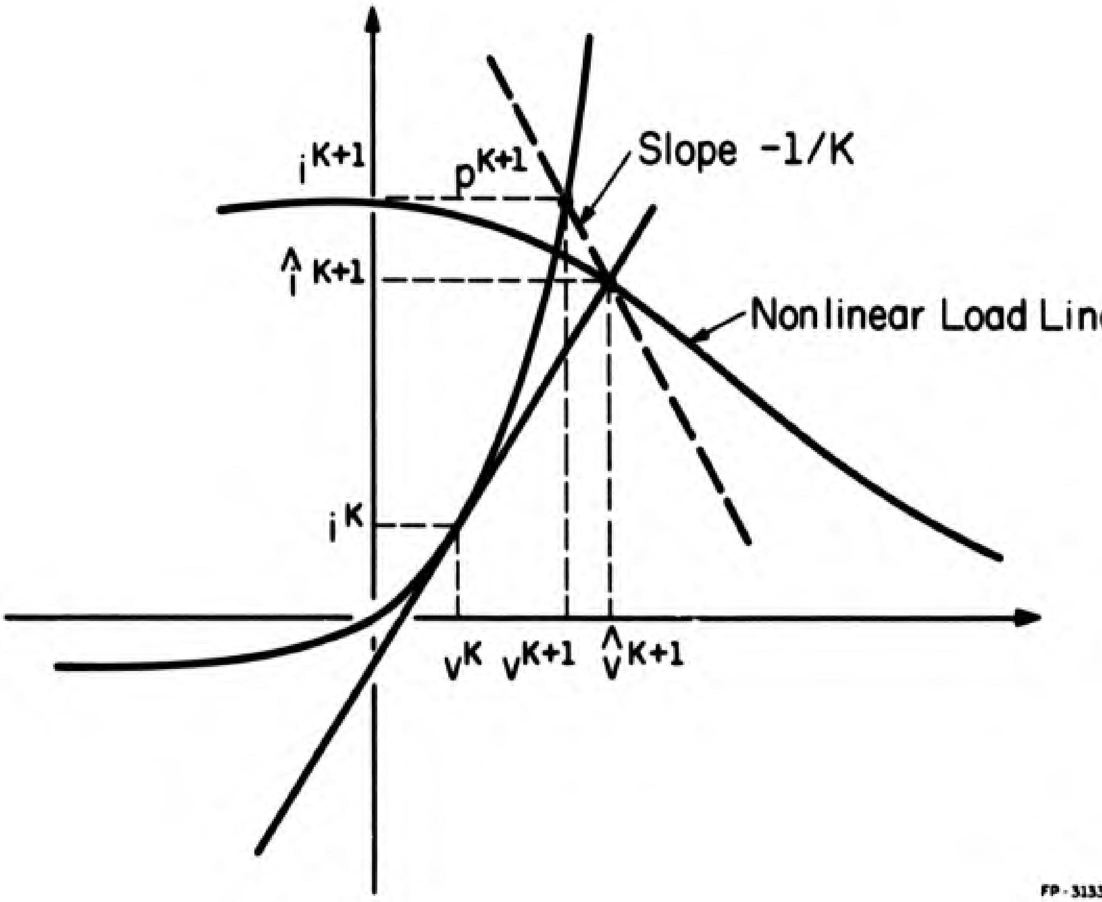


Figure 2.6. Transformation of the point $(\hat{v}^{k+1}, \hat{i}^{k+1})$.

Note that when $K=0$ we are iterating on voltage (moving vertically to the diode characteristic), and when $K \to \infty$ we move horizontally to the diode characteristic (current iteration). However, when $K \neq 0$ (15) is nonlinear and the solution v^{k+1} cannot be expressed explicitly in terms v^k and $\hat{v}^{k+1}$ unless $K \to \infty$. Therefore, for finite, nonzero K let $y = v^{k+1}$ be the solution to (15), then by Newton's method

$$y^{j+1} = y^j - (KI_s\theta e^{\theta y^j} + 1)^{-1} D^k \qquad (16)$$

where $D^k = v^k + (I + KI_s\theta e^{\theta v^k})(\hat{v}^{k+1} - v^k) + KI_s e^{\theta v^k}$. This approach involves an iteration within an iteration and has been frequently discussed as too time consuming. However, Cermak [4] has reported some favorable results with this approach.

Let us return to the circuit with m diodes. From the above discussion we have learned that for a given point $(v_{e_j}^k, i_{e_j}^k)$ on the diode characteristic the diode is replaced by a linear element whose characteristic is the tangent line at the point $(v_{e_j}^k, i_{e_j}^k)$. The linear circuit is shown in Figure 2.7, where

$$G_j^k = I_s\theta e^{\theta v_{e_j}^k} \qquad (17)$$

and

$$I_j^k = i_{e_j}^k - G_j^k v_{e_j}^k, \quad j = 1,2,\ldots,m. \qquad (18)$$

This circuit is solved for $\hat{\underline{v}}_e^{k+1}$, and the next iterate $\underline{v}_e^{k+1}$ is found from the solution of the equation

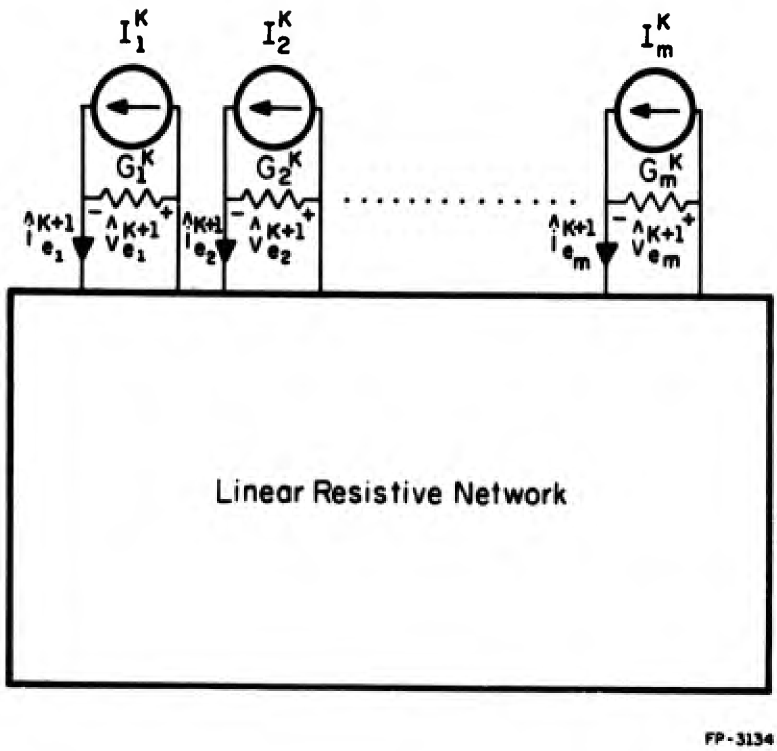


Figure 2.7

$$K_j^k I_{s_j} e^{\theta v_{e_j}^{k+1}} + v_{e_j}^{k+1} = v_{e_j}^k + (1 + KI_{s_j} \theta e^{\theta v_{e_j}^k})(\hat{v}_{e_j}^{k+1} - v_{e_j}^k) + KI_s e^{\theta v_{e_j}^k} \tag{19}$$

for $j = 1,2,\ldots,m$ and where usually $K_j^k = 0$ (voltage iteration) or $K_j^k = \infty$ (current iteration).

The iterates are said to have converged to the solution when the distance between successive iterates and/or the norm of some error function is less than some small number ϵ. For example, the distance between successive iterates can be measured as

$$d_1 = \|\underline{v}_e^{k+1} - \underline{v}_e^k\| / \|v_e^{k+1}\|, \tag{20}$$

$$d_2 = \|\underline{e}^{k+1} - \underline{e}^k\| / \|\underline{e}^{k+1}\|, \tag{21}$$

or

$$d_3 = \|\underline{i}_e^{k+1} - \underline{i}_e^k\| / \|\underline{i}_e^{k+1}\|. \tag{22}$$

The error function can be defined as follows. If at port j in Figure 2.2 the iteration is taken with respect to voltage, then the error is

$$|i_{e_j}^{k+1} - \hat{i}_{e_j}^{k+1}| = \epsilon_j. \tag{23}$$

If $\epsilon_j \neq 0$ then Kirchhoff's current law is violated at port j. If the iteration is on current the error is

$$|v_{e_j}^{k+1} - \hat{v}_{e_j}^{k+1}| = \rho_j, \tag{24}$$

and Kirchhoff's voltage law is not satisfied at port j if $\rho_j \neq 0$. Thus, the total error can be defined as

$$E = \|\underline{x}^{k+1} - \hat{\underline{x}}^{k+1}\| / \|\underline{x}^{k+1}\|, \quad (25)$$

where the jth component of the vector $\underline{x}$ is a current or voltage depending on the type of iteration. If K in (19) is nonzero and finite, then an appropriate error function might be the norm of the distance between the point $(v_{e_j}^{k+1}, i_{e_j}^{k+1})$ and the point $(\hat{v}_{e_j}^{k+1}, \hat{i}_{e_j}^{k+1})$.

2.3. Convergence of the Newton Method

The Newton method is generally said to have converged to a solution when one or more of the numbers in (20), (21), (22), (25) has become very small. If more than one solution exists, then for a given initial condition the Newton algorithm can converge to only one of the solutions and gives no information with regard to the fact that multiple solutions exist. However, usually the designer is aware that multiple solutions exist and can search for them by starting the Newton algorithm with a variety of initial conditions.

If one wants to pursue a more academic study of the problem, Sandberg [5] has given necessary and sufficient conditions for the existence and uniqueness of solutions of semiconductor-device nonlinear-network algebraic equations. In the case when the nonlinear algebraic equations have a global inverse, it can be shown that a Newton type algorithm will always converge to the unique solution [6]. Unfortunately, his conditions for the existence of a global inverse are difficult to check, especially for large networks. Whereas Sandberg's theorem indicates the possibility of no solution, two or more solutions, or that the solution is unique, if a piecewise linear approximation is made to the diodes a program by Chua [7] can be used to actually plot the driving point or transfer function of the network. Again this approach is time consuming so that the present practice is to use a Newton algorithm to search out the solution, and if more than one solution is suspected they are sought by using different initial voltages on the diode junctions to start the Newton algorithm.

2.4. Improvement in the Reliability and Speed of Convergence

Basically there are three pitfalls that any Newton type algorithm must avoid in the analysis of semiconductor networks. (a) There is the problem of exponential overflow, that is, it is not uncommon when iterating on voltage to obtain $v^{k+1} = 10$ volts or more, since $\theta \approx 40$ we must evaluate e^{400} which results in a diode current greater than 10^{100}. Obviously, this will result in overflow in the computer, and the analysis will terminate. (b) When iterating on current it can easily occur that $i^{k+1} < -I_s$. Since $v = \theta^{-1} \ell n(i/I_s+1)$, we are taking the logarithm of a negative number which causes the computer to terminate the analysis. (c) Finally, in the case of the possible existence of multiple solutions the Newton method can oscillate around several of the solutions and never converge or converge unacceptably slowly.

Problem (a) can be avoided by limiting the atep size of the voltage iterates or by using (19) and returning to the diode characteristic with a slope $-1/K$. However, as $K \to \infty$ we begin to iterate strictly on current and this presents the possibility of problem (b) above. Most successful programs use a combination of voltage iteration, current iteration, or finite nonzero K, and some include step size limiting. A third method that is useful in improving the reliability of convergence is source stepping in which the independent sources are increased or decreased in value. However, frequently this method, although usually more reliable, can slow convergence. Other variations for reducing computer cost consist of working with approximations to the linear circuit in Figure 2.7. The above methods are discussed below.

2.4.1. Variable slope transformation. Methods of this type use (19) to transform the point $(\hat{v}_{e_j}^{k+1}, \hat{i}_{e_j}^{k+1})$ into the point $(v_{e_j}^{k+1}, i_{e_j}^{k+1})$ by the following rule. One iterates on voltage $(K = 0)$ unless $\hat{v}_{e_j}^{k+1} > V_x$ where V_x is some constant chosen to prevent overflow and to accelerate convergence. If $v_{e_j}^{k+1} > V_x$, then one iterates on current $(K \to \infty)$. However, one method of this type [4] discussed in the next section uses (19) with $10^2 \leq K \leq 10^4$ and therefore involves an iteration within an iteration. Also note that within the same iteration the value of K_j^k can vary from diode to diode, e.g., one could iterate with respect to voltage on one diode and with respect to current on another. Also K_j^k can vary from iteration to iteration where superscript k denotes the iteration number.

2.4.2. Step size limitation. Usually this approach is used only with voltage iteration or some combination of voltage and current iteration. Let $\Delta\underline{x}^{k+1} = \underline{x}_N^{k+1} - \underline{x}^k$ be the step size made by the Newton method, and let

$$\underline{x}^{k+1} = \underline{x}^{k} + s\ \Delta\underline{x}^{k+1} \tag{26}$$

where the scalar s can be chosen to minimize the error function (25). Usually this is done by fitting the error function with a parabola and finding the value of s for which this parabola has a minimum.

Also, sometimes with voltage iteration step size limitation is used to prevent exponential overflow by means of the equation

$$\underline{x}^{k+1} = \underline{x}^{k} + S\ \Delta\underline{x}^{k+1} \tag{27}$$

where the diagonal matrix $S = \mathrm{diag}[s_1, s_2, \ldots, s_m]$. The parameters S_j are chosen to prevent overflow.

2.4.3. Source stepping. This method originated with Davidenko [8]. One approach to multiply the source vector $\underline{u}$ in (7) by a parameter α. When $\alpha = \alpha_0 = 0$, the solution to (5)-(8) is $\underline{i} = 0$, $\underline{v} = 0$, $\underline{e} = 0$. The parameter α is gradually stepped through a monotonically increasing sequence $\alpha_0, \alpha_1, \ldots, \alpha_K$ where $\alpha_K = 1$. At each level the previous solution for α_{j-1} is used as the initial iterate for the Newton algorithm with $\alpha = \alpha_j$. This method creeps up on the solution and is supposed to prevent violent oscillations usually caused by circuits capable of having multiple solutions.

Another version of this method which can be useful for locating multiple solutions is as follows. Initially assume that the voltage drop across the diode junctions is $\underline{v}_e^o$. This corresponds to a diode current

$$\underline{i}_{ed}^{o} = F(\underline{v}_e^{o}). \tag{28}$$

However, if the diodes in Figure 2.2 are replaced by the voltage source $\underline{v}_e^o$ then

$$\underline{i}_{e_\ell}^i = Gv_e^o + \underline{I}_N \tag{29}$$

where the matrix G is the Norton equivalent conductance matrix of the linear circuit and $\underline{I}_N$ is the short circuit current. The error is then

$$\underline{I}_e = \underline{i}_{e_\ell}^o - \underline{i}_{e_d}^o . \tag{30}$$

If we place a current source I_{e_j} in parallel with the jth diode as shown in Figure 2.8 then $\underline{v}_e^o$ is the solution to this circuit. In order to find the solution to the original circuit, multiply the error vector $\underline{I}_e$ by B, i.e., the source vector $\underline{I}_e$ in Figure 2.8 becomes B $\underline{I}_e$ where initially $B = 1$. The parameter B is then monotonically decreased in a finite number of steps to $B = 0$ and the Newton algorithm is applied at each step with the previous iterate as the initial estimate of the solution

2.4.4. Computation of the Jacobian. At the beginning of each iteration the derivative of equations (5)-(8) must be evaluated at the value of the previous iterate, i.e., the nonlinear equations are linearized about the previous estimate of the solution. The resulting matrix is called the Jacobian. The linear circuit is then solved and (19) is used to determine the value of the next iterate. The solution of these linear algebraic equations involves the LU decomposition of a matrix. It has been suggested that the LU decomposition for the kth iterate could be used for several iterates, that is, the diode conductance remains at G_j^k and is not updated

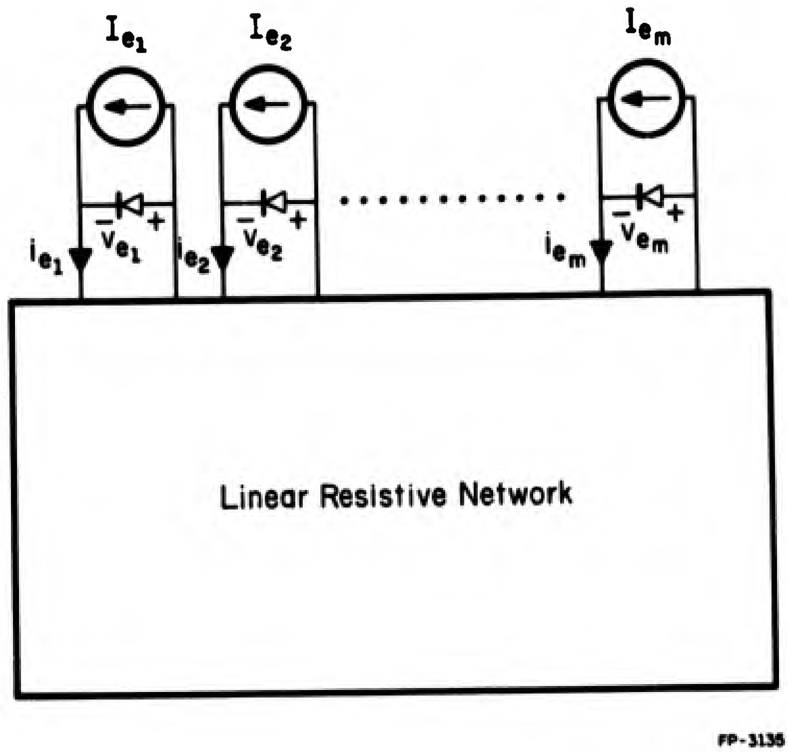


Figure 2.8. Reduction of error to zero by means of external current sources.

for several iterates ($G^{k+\ell} = G^k$), and only the diode current $I_j^{k+\ell} = i_{e_j}^{k+\ell} - G_j^k v_{e_j}^{k+\ell}$ in Figure 2.7 is updated for each iterate. The following error criteria can be used to determine if the Jacobian should be updated (a) if the error function does not decrease, and/or (b) $\|\underline{x}^{k+\ell} - \underline{x}^k\| / \|\underline{x}^{k+\ell}\| > M$ where $\underline{x}^k$ is the solution at the kth iterate when the Jacobian was last updated. A combination of both criteria seems to work best, however the selection of the positive number M can be critical. This method does not seem to save computational time when sparse matrix methods are used and the initial estimate of the solution is far from the correct solution. In fact, it can cause serious convergence problems. However, it can save time in the statistical analysis of circuits when the deviation from the nominal solution is not too great, and in the transient analysis of nonlinear circuits where the variation in the solution from one time step to the next is small.

Finally, Broyden [9] has suggested a method of estimating the Jacobian from iterate to iterate without calculating the derivative of the nonlinear functions. However, this method does not seem to be advantageous since (a) the partial derivatives of the exponential diode characteristics are easy to evaluate, and (b) it can be shown that this method converges to the correct Jacobian if the equations are linear which leads one to suspect that gross errors could be made in the case of exponential functions.

2.5. A Nodal Analysis Program for the Comparison of Modified Newton Algorithms

In the next section several modified Newton algorithms for the dc solution of electronic circuits are compared in terms of speed and reliability. Presently we describe the basic nodal analysis program which is used to make this comparison. Only the logic part of the program which selects the next iterate $(\underline{v}_e^{k+1}, \underline{i}_e^{k+1})$ changes from program to program.

The indefinite admittance matrix approach [2] is used to form the node equations. The nodes are numbered consecutively from 0 (ground node) to n. If a conductance G is connected between nodes i and j then G is added to positions ii and jj, and -G is added to positions ij and ji of the admittance matrix Y where

$$Y\underline{e} = \underline{IS}. \tag{31}$$

If an independent current source has current I_a flowing from node i to node j, then I_a is added to position j and $-I_a$ is added to position i of the source vector $\underline{IS}$. Voltage sources are presently not allowed. At the beginning of each iterate we have an estimate $\underline{v}_e^k$ of the diode junction voltages. Thus the diode is replaced by the linear model illustrated in Figure 2.7, and G_j^k and I_j can be added appropriately to Y and $\underline{IS}$. The linearized model for the Ebers-Moll large signal npn transistor model [3] is shown in Figure 2.9. The indefinite admittance matrix Y_t for the linearized transistor is

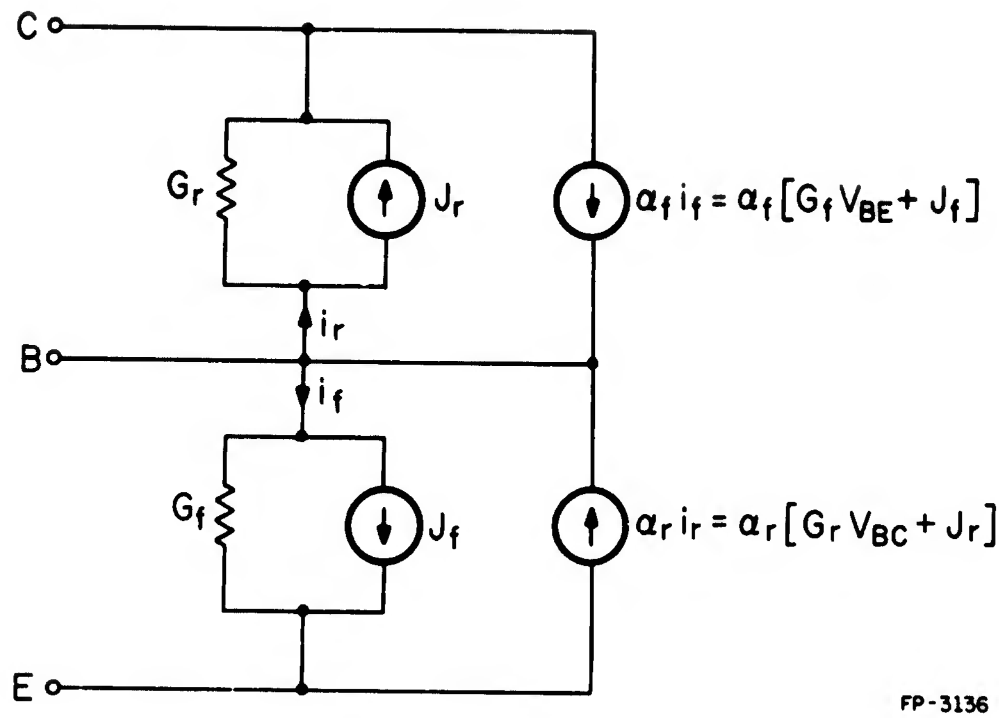


Figure 2.9. Linear transistor model.

$$Y_t = b\begin{bmatrix} G_r & \alpha_f G_f - G_r & -\alpha_f G_f \\ (\alpha_r - 1)G_r & (1-\alpha_f)G_f + (1-\alpha_r)G_r & (\alpha_f - 1)G_f \\ -\alpha_r G_r & \alpha_r G_r - G_f & G_f \end{bmatrix} \tag{32}$$

and

$$\underline{I}_t = \begin{bmatrix} J_r - \alpha_f J_f \\ (\alpha_f - 1)I_f + (\alpha_r - 1)J_r \\ J_f - \alpha_r J_r \end{bmatrix} . \tag{33}$$

A sparse matrix routine similar to Berry's [20] is used to solve (31) for $\hat{e}^{k+1}$ from which the branch voltages $\hat{\underline{v}}_e^{k+1}$ and branch currents $\hat{\underline{i}}_e^{k+1}$ can be computed. Then this point $(\hat{\underline{v}}_e^{k+1}, \hat{\underline{i}}_e^{k+1})$ is mapped into the point $(\underline{v}_e^{k+1}, \underline{i}_e^{k+1})$ which depends on the parameters in (19) and the amount of step size limitation, if any.

Finally if source stepping is used, then (31) can be written as

$$Y\underline{e} = \alpha \underline{I}_i + \underline{I}_d \tag{34}$$

where $\underline{I}_d$ consists of the independent current sources in the linear models for the semiconductor devices, and $\underline{I}_i$ represents the remaining independent current sources, or

$$Y\underline{e} = \underline{I} + B\,\underline{I}_e \tag{35}$$

where $\underline{I}_e$ is the current source vector which reduces the error to zero on the zeroth iterate with the initial estimate of the solution $\underline{e}^o$.

In the next section we will review seven different modifications for improving the reliability and speed of the Newton algorithm. The modifications are drawn from Sections 2.4.1, 2.4.2, and 2.4.3. The modifications suggested in Section 2.2.4 were not programmed for the following reasons. (a) It was felt that these modifications are only successful when the device characteristics are almost linear or the iterates are contained in a region in which the behavior of the devices is nearly linear. (b) If (a) is true then the method of not updating the Jacobian at each step should be equally successful at reducing computer cost for all of the modifications in Sections 2.4.1 - 2.4.3.

III. "QUASI-NEWTON" METHODS

This section describes seven different modifications of the basic Newton algorithm for the dc analysis of solid-state electronic circuits. The nodal analysis method described in the previous section is the basis of each program. In the standard Newton algorithm one assumes an initial set of junction voltages $\underline{v}_e^o$ (corresponding to a set of node voltages $\underline{e}^o$) about which the diodes are linearized. If the junction is forward biased the diode is replaced by a resistor in parallel with a current source as illustrated in Figure 2.7, but if the junction is reversed biased the diode is replaced by a resistor $r_j = v_{e_j}/I_{s_j}$. This linear circuit has an admittance matrix Y^o such that

$$Y^o \underline{e}^o = \underline{I}^o + \underline{I}_e^o \tag{36}$$

where $\underline{I}_e^o$ is the error vector. The next iterate is obtained from the solution of the equation

$$Y^o \underline{e}^1 = \underline{I}^o. \tag{37}$$

The diode junction voltages $\underline{v}_e^1$ are computed as the appropriate differences of the node voltages $\underline{e}^1$. The diodes are linearized and a new admittance matrix Y^1 is obtained. The above process is repeated until

$$\|\underline{e}^{k+1} - \underline{e}^k\| / \|\underline{e}^k\| < 10^{-6}. \tag{38}$$

Unfortunately, exponential overflow usually occurs and the Newton method must be modified. The modifications compared in this work are now described.

3.1. Method ECAP II

The ECAP II algorithm [11] is a step size limiting method with the step size control scalar R chosen so that the norm of the error is reduced from iteration to iteration. In this work the error at the kth iterate is measured as the Euclidean norm of $\underline{I}_e^k$. During the k+1 iterate the node voltage $\hat{\underline{e}}^{k+1}$ is computed from the equation

$$Y^k \hat{\underline{e}}^{k+1} = \underline{I}^k. \tag{39}$$

The final node voltage for the k+1 iteration is computed from the equation

$$\underline{e}^{k+1}(R) = \underline{e}^k + R(\hat{\underline{e}}^{k+1} - \underline{e}^k) \tag{40}$$

where $\underline{e}^{k+1}(1) = \hat{e}^{k+1}$. Associated with the node voltage is the error vector $\underline{I}_e^{k+1}(R)$. Define

$$y^{k+1}(R) = \|I_e^{k+1}(R)\| / \|I_e^k\|. \tag{41}$$

In the case of a linear circuit $y^{k+1}(R)$ is a parabola with an initial slope of -2 and zero minimum at $R = 1$ as shown in Figure 3.1. Thus the method converges in one iteration. In nonlinear problems with a nonsingular admittance matrix the initial slope of y(R) at $R = 0$ is still -2, but the function y(R) is no longer a parabola. Three typical curves labeled A, B, and C are illustrated for the nonlinear problem in Figure 3.1. The scalar R is chosen by the following rule [11].

1) Take full step $(R = 1)$ and evaluate $\underline{I}_e^{k+1}$ (the forward diode junction voltages are limited to 2 volts to avoid exponential overflow).

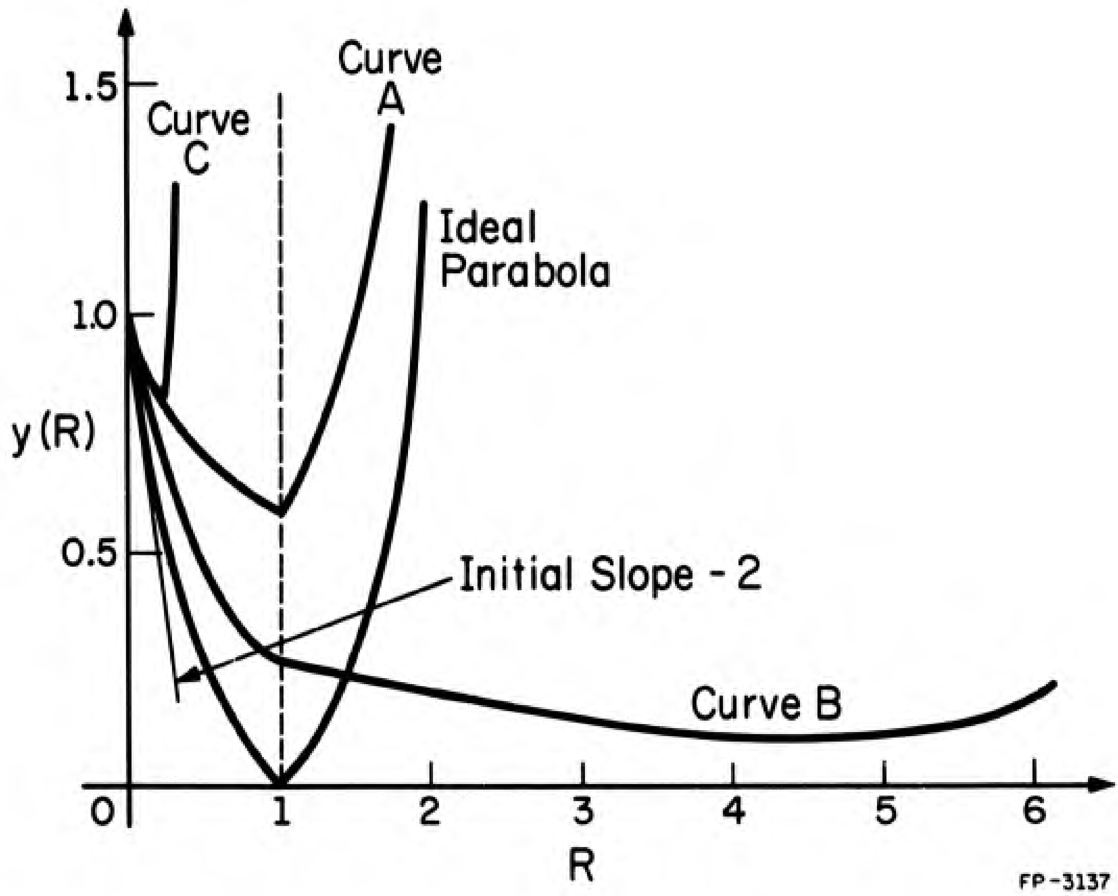


Figure 3.1. Typical curves of y(R) versus R for ECAP II method.

2) Compute y(1).

3) Next, depending on this value of y(1) proceed as follows:

   a) If $y(1) < 0.1$, the full Newton step $(R = 1)$ is taken and continue to the next iterate.

   b) If $0.1 < y(1) < 100$ (curve A), then

      i) Approximate y(R) by a parabola thru (0,1) [y(1),1] and with initial slope (at $R = 1$) of -2.

      ii) Find minimum of parabola $[Y(R_{min}), R_{min}]$.

      iii) Pass a cubic curve thru previous value [y(1),1] and $[Y(R_{min}), R_{min}]$.

      iv) Find the minimum of the cubic curve R_{min}, and compute $\underline{e}^{k+1}(R_{min})$ from (40) as the next iterate.

      v) However, if R_{min} in (iv) is greater than 1 as in curve B then compute y(2), y(4), y(8) .... etc, until the y(R) begins to increase, then fit a parabola thru the last 3 points and obtain R_{min} and $\underline{e}^{k+1}(R_{min})$.

   c) If $y(1) > 100$ as in curve C then

      i) Evaluate y(1/2), y(1/4), y(1/8) ...... etc. until a value less than one is obtained.

      ii) Increase R successively by 10% until curve begins to swing upwards.

      iii) Fit the last 3 points with a parabola and compute R_{min} and $\underline{e}^{k+1}(R_{min})$.

This method converges to the solution in the case when the circuit has a unique solution for all values of the independent sources. However, when the possibility of multiple solutions exists convergence cannot be guaranteed.

3.2. Method BROYDEN

This method is a particular version of Davidenko's algorithm [8] as proposed by Broyden [12]. It is a source stepping method in which the initial error vector $\underline{I}_e^o$ is gradually stepped from one to zero by means of a parameter β, where $\beta_o = 1$, $\beta_1 = .95$, $\beta_2 = .9$, and β_{r+1} is determined as follows.

1. Given $\underline{e}^o$ compute the error $\underline{I}_e^o$.
2. Solve the nonlinear equation

$$Y(\underline{e})\underline{e} = \underline{I}s + \beta_r \underline{I}_e^o \tag{42}$$

for $\beta_1 = .95$ and $\beta_2 = .9$ by the Newton algorithm where iteration on voltage was used except when a junction voltage was greater than zero and exceeded its value on the previous iterate then iteration on current was used. Call these two solutions $\underline{e}^1$ and $\underline{e}^2$ respectively corresponding to β_1 and β_2. (Note e_o^o is the solution with $\beta_o = 1$.)

3. When $\beta_r = 0$ stop
3. Since e is a function of β, approximate the node voltage with the parabola

$$\underline{q}_r(\beta) = \beta^2 \underline{a}_r + \beta \underline{b}_r + \underline{c}_r \tag{43}$$

where $r = 2$ and

$$q_r(\beta_o) = \underline{e}^{r-2},$$

$$q_r(\beta_1) = \underline{e}^{r-1},$$

$$q_r(\beta_2) = \underline{e}^{r}$$

determine the vector $\underline{a}_r$. $\underline{b}_r$, and $\underline{c}_r$.

4. Computer [12]

$$\beta_{r+1} = \beta_r - \frac{\lambda \| 2\underline{a}_r \beta_r + \underline{b}_r \|}{\| \underline{a}_r \|} . \tag{44}$$

Note that the reduction in β is dependent on the reciprocal of the radius of curvature of the parabola. λ is a positive constant.

5. If $\beta_{r+1} < 0.1$, set $\beta_{r+1} = 0$. For the computed value of β_{r+1} estimate $\underline{e}^{r+1}$ from (43). Return to the nonlinear equation (42) with β_{r+1} and compute $\underline{e}^{r+1}$ with the estimate from (43) as the initial iterate.

In the examples $\lambda = 0.5$ seemed to give the best results in the above algorithm.

3.3. Method BROWN

This method was proposed by Brown [13] and is a step size limitation method. A hypersphere of radius r is drawn around the present iterate. If the norm of the difference between two successive Newton iterates falls within the hypersphere, then a full Newton step is taken; however, if it falls outside of it then a new approximation is taken to be on the boundary of the sphere. A good value for r used for bipolar transistors was 1. The method was programmed as follows.

1. Compute $\hat{\underline{e}}^{k+1}$ and $\underline{x} = \hat{\underline{e}}^{k+1} - \underline{e}^k$.

2. Calculate

$$r = \sqrt{\sum_{i=1}^{n} (x_i)^2} .$$

3. Let

$$\underline{e}^{k+1} = \hat{\underline{e}}^{k+1} \quad \text{if } r \leq 1 \text{ (full Newton step)}$$

$$\underline{e}^{k+1} = \underline{e}^{k} + \frac{1}{r}\,\underline{x} \quad \text{if } r > 1$$

This method has simplicity in its favor.

3.4. Method CANCER

This method [14] is actually a further modification of L. D. Milliman's CIRCUS [15] program. Milliman determined the new semiconductor junction voltage $v_{e_j}^{k+1}$ as follows

$$v_{e_j}^{k+1} = v_{e_j}^{k} + \gamma_j(\hat{v}_{e_j}^{k+1} - v_{e_j}^{k}) \tag{45}$$

where $v_{e_j}^{k}$ was the previous value, $\hat{v}_{e_j}^{k+1}$ is the value calculated for the next iterate and $v_{e_j}^{k+1}$ is the actual value chosen for the next iterate. γ_j was called the damping factor (used only for junction voltages greater than 10 V_T, where $V_T = \frac{1}{\theta}$) and had an empirical value of 0.5.

Milliman's method had two main drawbacks:

1) Convergence process is slowed down if the iterative solutions were in the vicinity of the correct solution.

2) If the solutions of two successive iterations differed widely, it still might diverge or oscillate.

To correct these two shortcomings, the CANCER program [14] proceeds in a manner somewhat similar to Brown to obtain the new junction voltage $v_{e_j}^{k+1}$

$$v_{e_j}^{k+1} = \hat{v}_{e_j}^{k+1}, \quad \text{if } \hat{v}_{e_j}^{k+1} < 10\ V_T$$

but if not, then

$$v_{e_j}^{k+1} = \begin{cases} v_{e_j}^{k} + 2\ V_T\ , & \text{if } \hat{v}_{e_j}^{k+1} > v_{e_j}^{k} + 2\ V_T \\ \hat{v}_{e_j}^{k+1} , & v^{k} - 2\ V_T \le \hat{v}^{k+1} \le v_{e_j}^{k} + 2\ V_T \\ v_{e_j}^{k} - 2\ V_T\ , & \hat{v}^{k+1} < v^{k} - 2\ V_T \end{cases}$$

The method is a step size limitation method which controls the diode junction voltages individually as apposed to Brown's method which damps all junction voltages equally.

3.5. Method BIAS 3

The iteration procedure utilized by BIAS 3 [16] for the selection of the next iteration point is dependent on whether the new junction voltage is decreasing or increasing with respect to the junction voltage of the last iteration:

a) If the junction voltage increases, let us say from V_{BEO} to V_1' as seen in Figure 3.2, BIAS 3 updates with current iteration or moving back horizontally to the exponential characteristic. This is done by computing the logarithm of the current corresponding to point 1' and results in the selection of point 1 as the new trial operating point corresponding to the junction voltage V_1 and current I_1 where

$$V_1 = \frac{kT}{q} \ln \left(\frac{I_1}{I_s} + 1\right). \tag{46}$$

b) Now if in the next iteration the voltage decreases, for example in Figure 3.2 from V_{BEO} to V_2, BIAS 3 iterates on voltage by proceeding vertically to a new point on the exponential characteristic. This can be done by straight forward evaluation of the exponential function of voltage

$$I_2 = I_s(e^{qV_2/kT} - 1) \tag{47}$$

and point 2 is selected as the new trial operating point. The voltage iteration is the same as the Newton-Raphson method. In the 3rd quadrant corresponding to negative junction voltages it iterates only on voltage. However the slope of the diode characteristic approaches 0 in the reverse direction and may cause a division by 0. To solve this problem the exponential characteristic is modeled in terms of a line passing thru the trial operating point and the origin rather

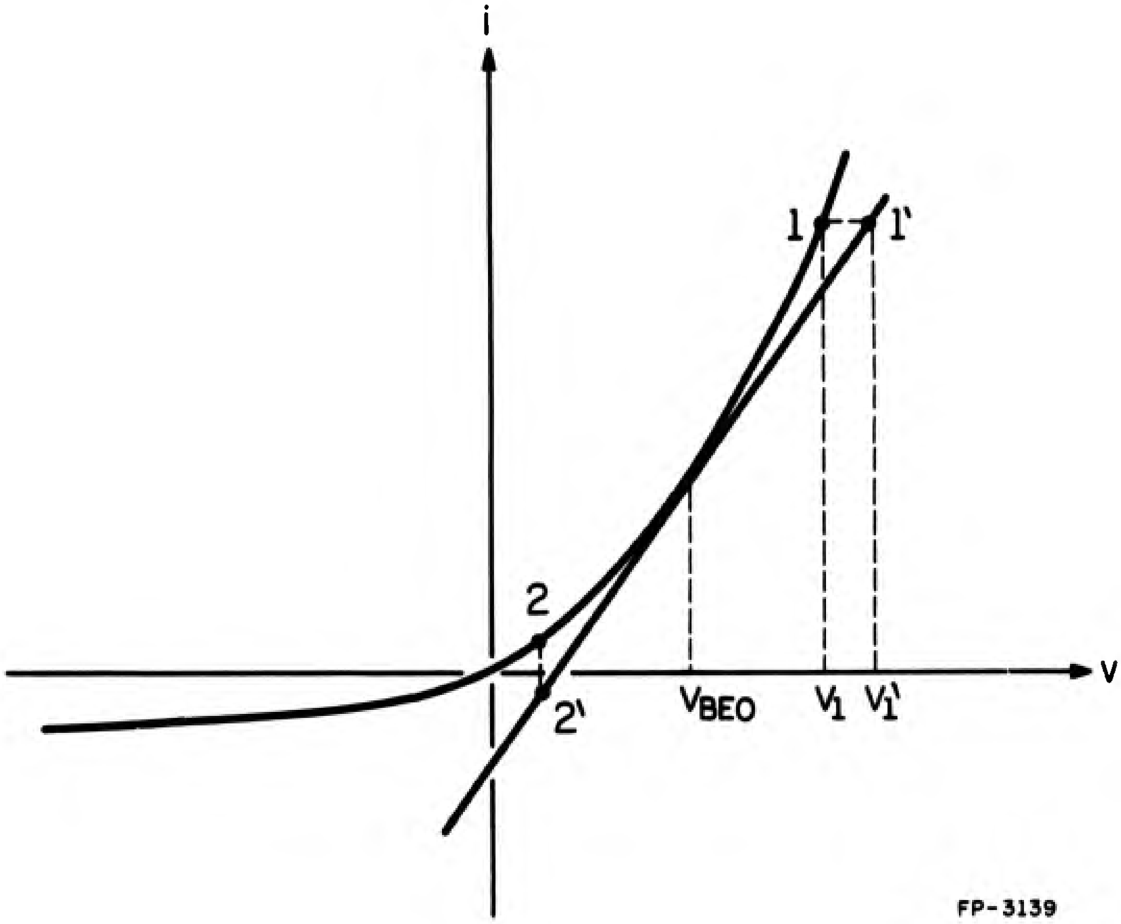


Figure 3.2. Iteration procedure in method BIAS 3.

by a tangent to the characteristic as is done in the other six methods too.

As can be seen this method uses current iteration whenever there is a chance of overflow, which can occur only when the junction voltage increases. However, this also could lead to slower convergence. For instance the usage of voltage iteration even when the voltage was increased (with no danger in overflow), or the usage of current iteration even when the voltage was decreased could have given even better results in some of the cases. For example an improvement of BIAS 3 method by using current iteration while voltage has decreased is illustrated in Figure 3.3.

3.6. Method COLON

This method was proposed by Dr. F. R. Colon associated with the Coordinated Science Laboratory at the University of Illinois and is very similar to BIAS 3 differing only in the criteria of when to iterate on current. In BIAS 3, a current iteration is used whenever we have an increase in junction voltage and the junction voltage is greater than zero. Otherwise, the iterates are taken with respect to voltage.

In COLON's method a slope criterion is used. The program iterates on current whenever the diode conductance of the new iterate has a slope larger than a specified value, and iterates on voltage when the conductance of the new point is less than it. This is illustrated in Figure 3.4.

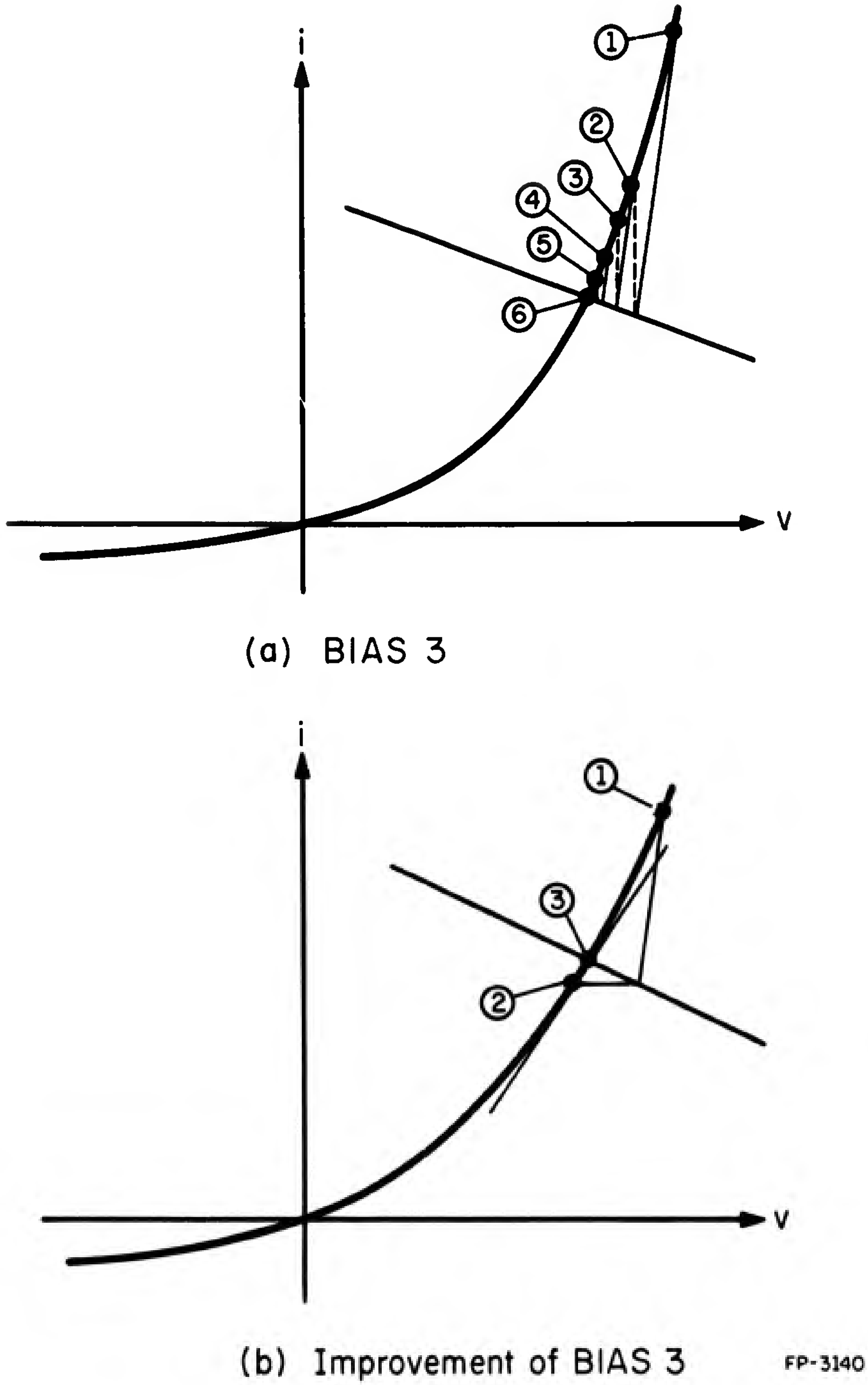


Figure 3.3. Improvement of BIAS 3 by using current iteration while voltage is decreasing.

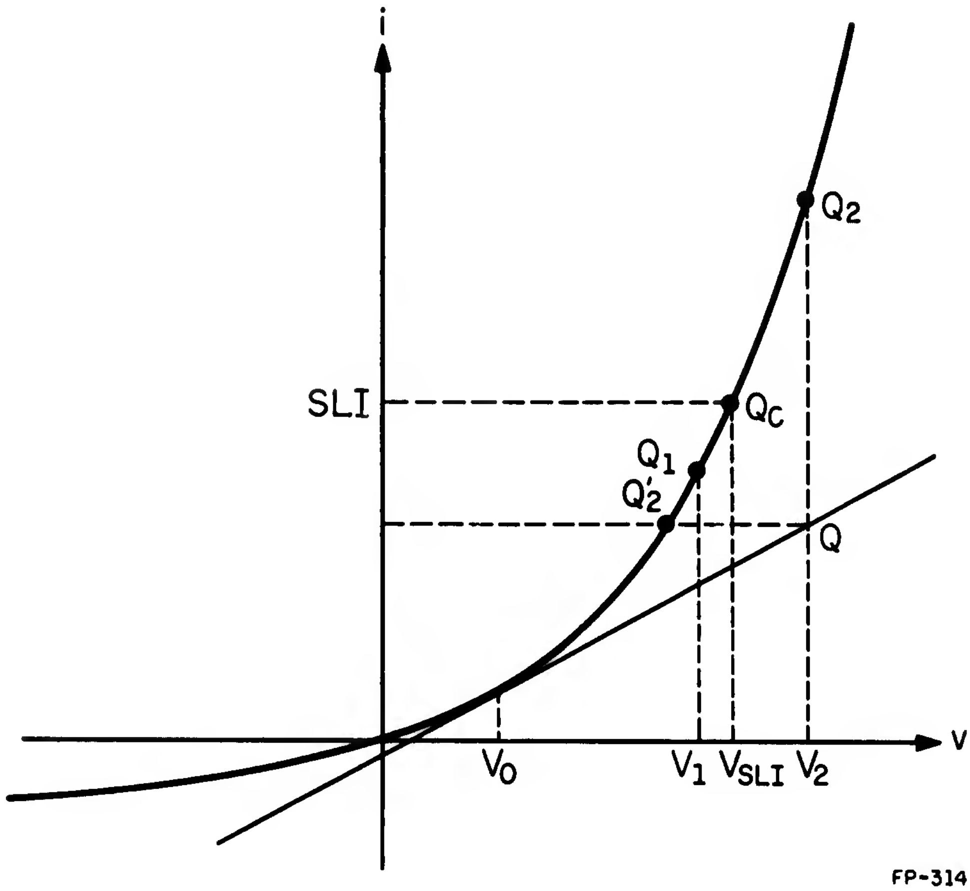


Figure 3.4. Iteration procedure in method COLON.

In the figure V_{SLI} is the critical voltage, SLI is the critical current value and at Q_c the slope has the specified value. It can be seen that all points on the diode characteristic to the left of Q_c have slopes smaller than at Q_c while all points to the right of Q_c have slopes larger than at Q_c. Let v_o be the initial guess for junction voltage and v_1 and v_2 be two possible values for the next iterate. First let us take $V_1 < V_{SLI}$, in this case the conductance $G_{Q_1} < G_{Q_c}$, thus a voltage iteration is used. For $V_2 > V_{SLI}$ we have $G_{Q_2} > G_{Q_c}$ and so we iterate on current to prevent a possible overflow, and we get to the new point Q_z'.

The COLON program iterates on voltage even when the junction voltage is increased as long as the new voltage does not exceed V_{SLI}, while the BIAS 3 program would have iterated on current in this case. Summarizing COLON program

a) iterates on current if $\hat{V}^{k+1} > V_{SLI}$

b) iterates on voltage if $\hat{V}^{k+1} < V_{SLI}$.

Now a value for SLI is chosen, which is the same as giving a value for V_{SLI} since

$$V_{SLI} = \frac{kT}{q} \ell n[\frac{SLI}{I_s} + 1]. \tag{48}$$

Also, this is the same as given the specified slope Q_c, since the diode conductance

$$\frac{\partial i}{\partial v} = \theta I_s e^{\theta V} = \theta(i + I_s)$$

so

$$G_{Q_c} = \theta(SLI + I_s),$$

or (50)

$$G_{Q_c} \approx 40 \text{ SLI}$$

assuming room temperature and $I_s \ll$ SLI.

In the Colon method choice for the optimum value of SLI is critical, and although a value of SLI = 1 ma or G = 40 × 1 ma = 0.04 has been found to work well for most of the circuits, in some cases other choices could have given faster convergence.

3.7. Method CERMAK

This method [4] obtains the DC solution by using a transformation of variable approach with a finite K. Instead of iterating on either voltage or current, this method gives to the next iterate by computing the value of a transform parameter K and then going to the i-v characteristic curve at slope $-\frac{1}{K}$. See Figure 3.5. The parameter $K_j^k = 10/\theta I_{s_j} e^{v_{e_j}^k}$ and in addition is bounded by $10^2 \leq K_j^k \leq 10^4$ and changes from iteration to iteration and from diode to diode. The method follows below.

1. Compute K_j^k corresponding to $v_{e_j}^k$, $j = 1, \ldots, m$.
2. Compute $\hat{\underline{e}}^{k+1}$ and $\hat{\underline{v}}_e^{k+1}$. If convergence is not achieved, go to step 3.
3. Compute D_j^k in (16) for each diode.

$$\text{If} \quad \begin{array}{ll} D_j^k \leq z_j^k + 0.08 & \text{let } y_j^o = D_j^k \\ D_j^k > z_j^k + 0.08 & \text{let } y_j^o = \frac{1}{\theta} \ln D_j^k + z_j^k \end{array}$$

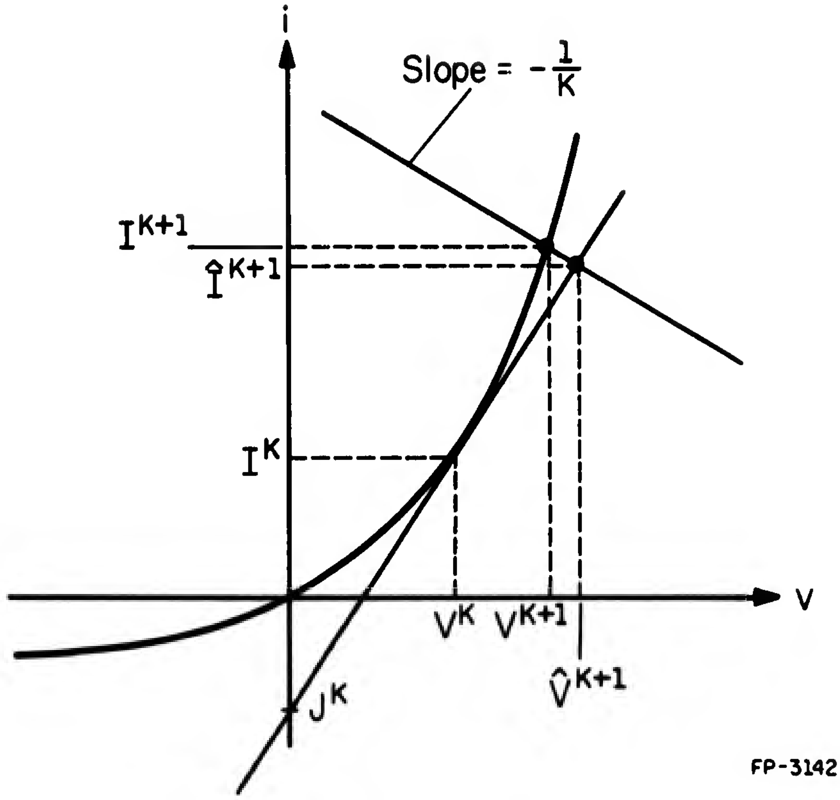


Figure 3.5. Iteration procedure in method CERMAK.

where $z_j^k = -\frac{1}{\theta} \ell n[K_j^k \ I_{s_j}]$.

Solve equation (15) for $v_{e_j}^{k+1}$ by means of (16) with the initial conditions given in step 3. When

$$\frac{|y_j^{n+1} - y_j^n|}{|y_j^n|} < 10^{-6}$$

set $v_{e_j}^{k+1} = y_j^{n+1}$. Solve (16) for each diode junction.

5. Increment k by 1 and return to step 1.

IV. SAMPLE PROBLEMS

In this section a number of examples were solved by all seven of the modifications described in the previous section. Since the nodal analysis program is the basis of all seven methods the solutions of the examples are given in terms of node voltages. All programs were run on the 1604 Control Data Computer of the Coordinated Science Laboratory at the University of Illinois. A brief description of each sample problem together with their circuit configuration will be given in this section. For comparison purposes the number of iterations together with the time it took for each method to converge is given in tabulated form in Table 5.1. Finally, the parameters and the solutions for each circuit is given in the Appendix.

In the COLON program the value of SLI was chosen to be 1 ma, and in the BROYDEN program the value of λ was picked to be 0.5. These values were found to give the best results in the average for the sample problems. As far as initial conditions are concerned, the examples started with all the transistor junction voltages initially set to IC1 (all junction voltages zero) and/or IC2 (base-emitter junction forward biased at 0.4 V and base-collector voltage zero) except for the multibrator and flip flop circuits which have more than one solution, so the initial conditions which resulted in convergence to each particular solution are given in the Appendix in terms of the node voltages.

1. Constant Current Source without r_b, r_c (See Figure 4.1)

This is a constant current source used in a D/A converter. Resistors R1 through R4 are thin film tantalum resistors. R5 represents the load. Analysis of this circuit [4] verified that the output current is essentially insensitive to all parameters except the power supplies and R4. The circuit has six identical transistors.

2. Constant Current Source with $r_b = 100\ \Omega$, $r_c = 10\ \Omega$

With the exception of having r_b and r_c included for each transistor this is basically the same as sample problem 1 (see Figure 4.2).

3. Kilohertz Oscillator

The circuit [17] has seven identical transistors. For dc analysis of the oscillator the capacitors in the twin T feedback network are removed (see Figure 4.3).

4. Three Transistor Inverters with $r_b = 50\ \Omega$, $r_c = 10\ \Omega$

This is a simple circuit with 3 identical transistors connected in cascade (see Figure 4.4).

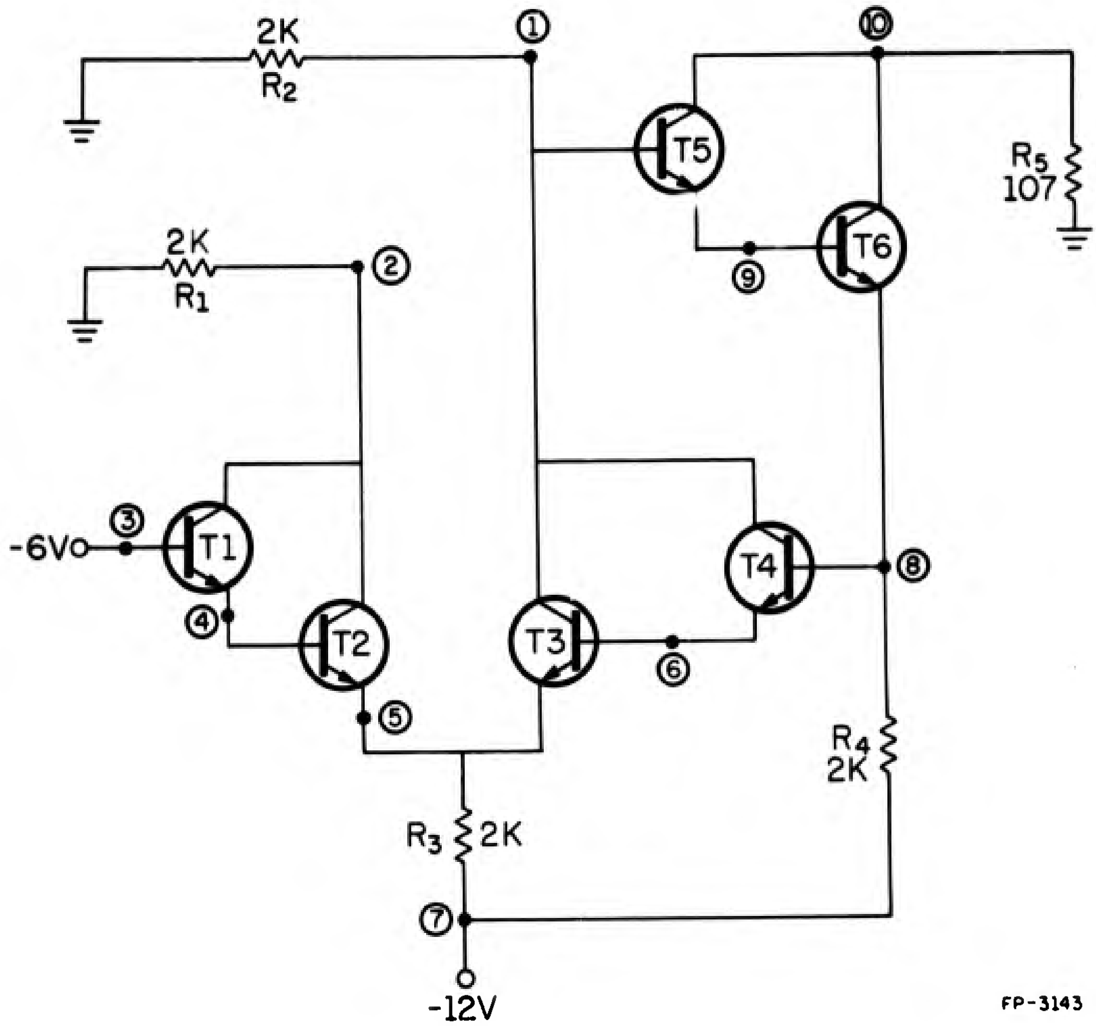


Figure 4.1. Constant current source without r_b, r_c.

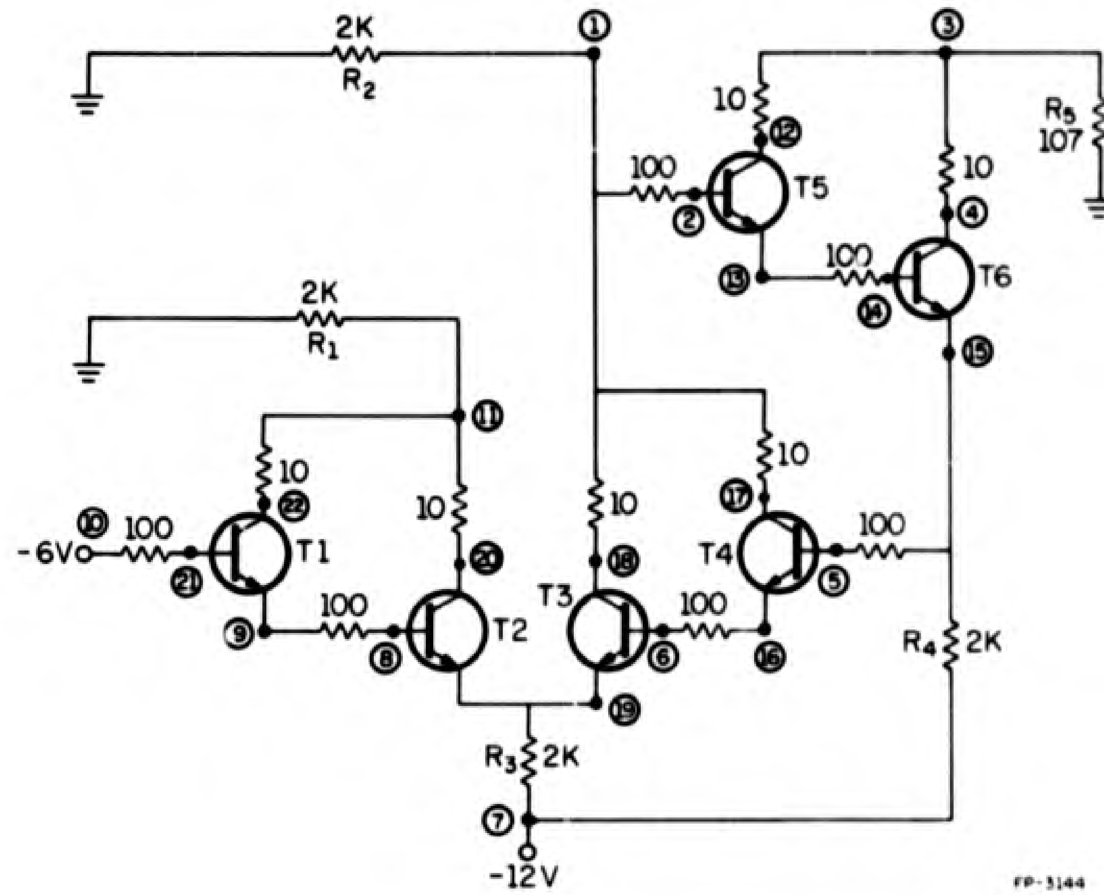


Figure 4.2. Constant current source with r_b = 100, r_c = 10 included.

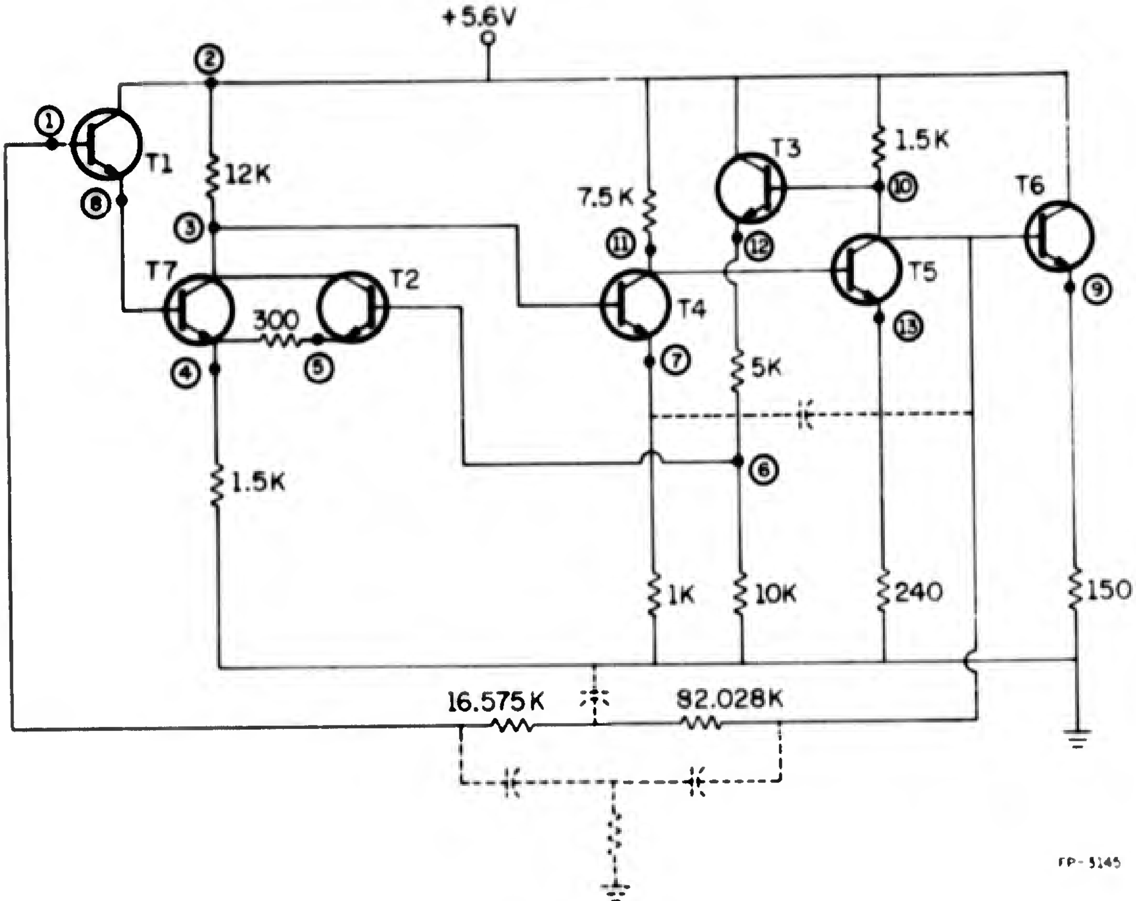
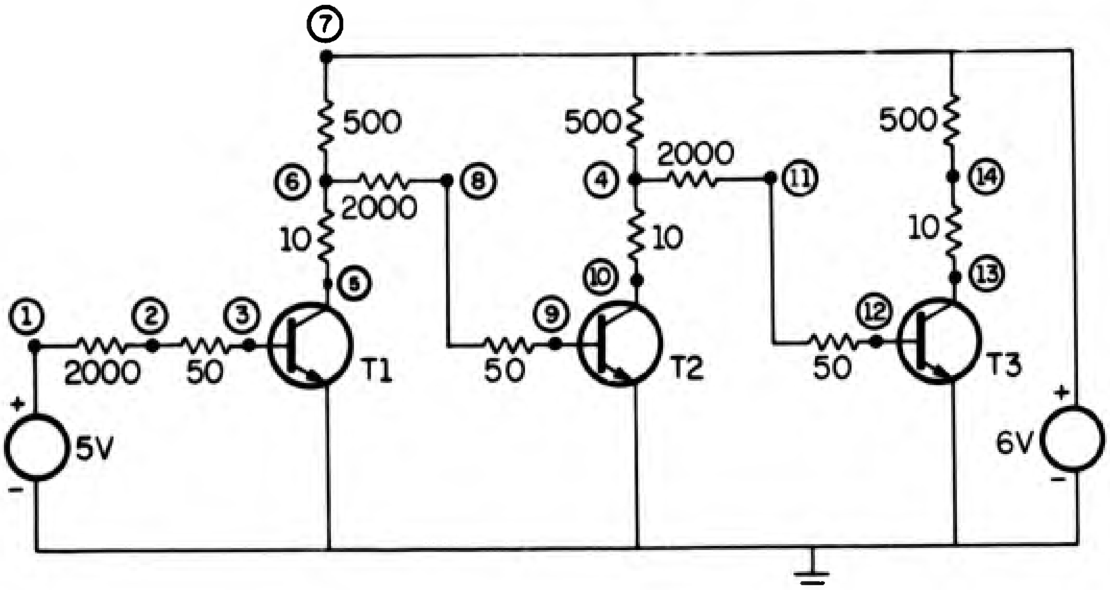


Figure 4.3. 1 KHZ oscillator.



FP-3146

Figure 4.4. Three cascaded transistor invertors.

5. Operational Amplifier

This is a silicon integrated operational amplifier designed at Bell Laboratories [4]. Of interest in this example is the output offset voltage with the inputs grounded. It has 24 identical transistors (see Figure 4.5).

6. μA 733 Differential Video Amplifier (See Figure 4.6)

The μA 733 is a monolithic two stage differential input, differential output video amplifier constructed on a single silicon chip using the Fiarchild planar epitaxial process. Internal series shunt feedback is used to obtain wide bandwidth, low phase distortion, and excellent gain stability. Emitter follower outputs enable the device to drive capacitive loads and all stages are current source biased to obtain high power supply and common mode rejection ratios. It offers fixed gains of 10, 100, 400 without external components, and adjustable gains from 10 to 400 by the use of a single external resistor. No external frequency compensation components are required for any gain option. The device is particularly useful in magnetic tape or disc file systems using phase or NRZ encoding and in high speed thin film or plated wire memories. Other applications include general purpose video and pulse amplifiers where wide bandwidth, low phase shift, and excellent gain stability are required. It has 11 identical transistors.

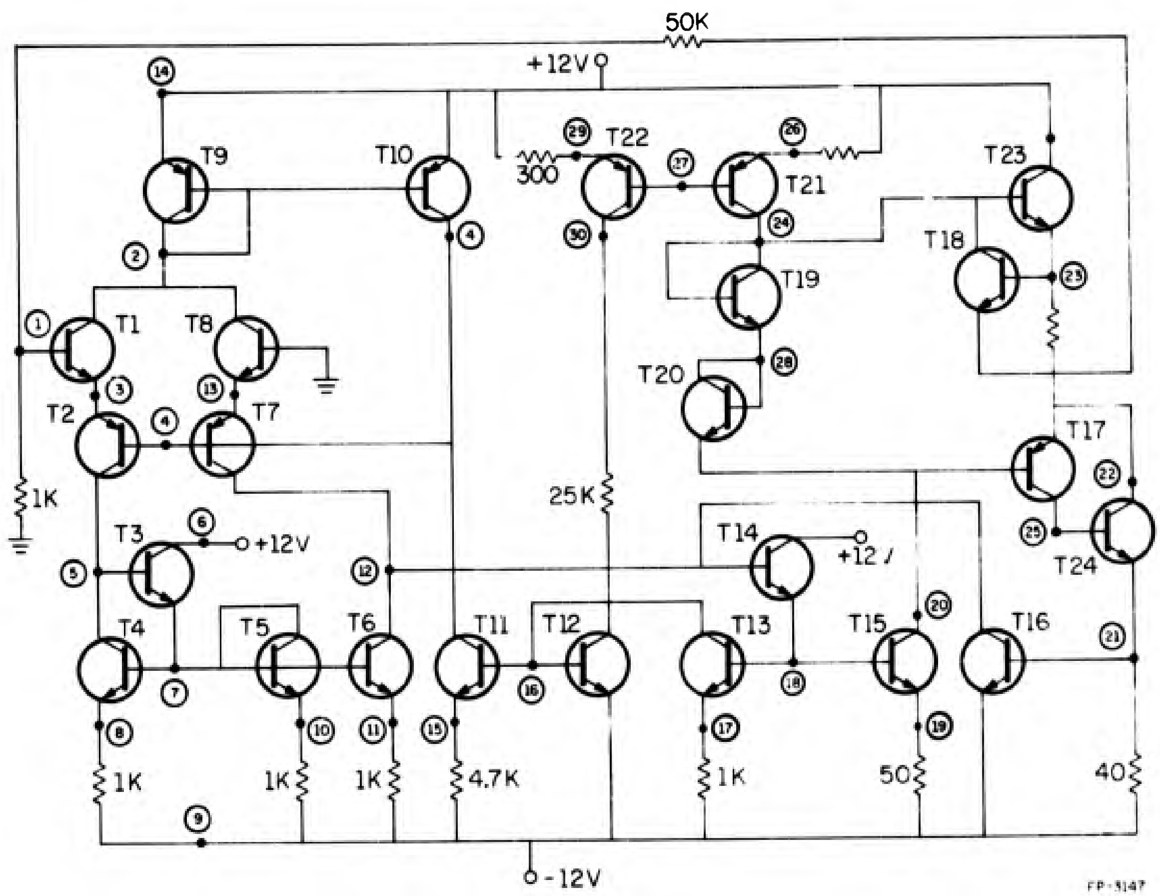


Figure 4.5. Operational amplifier.

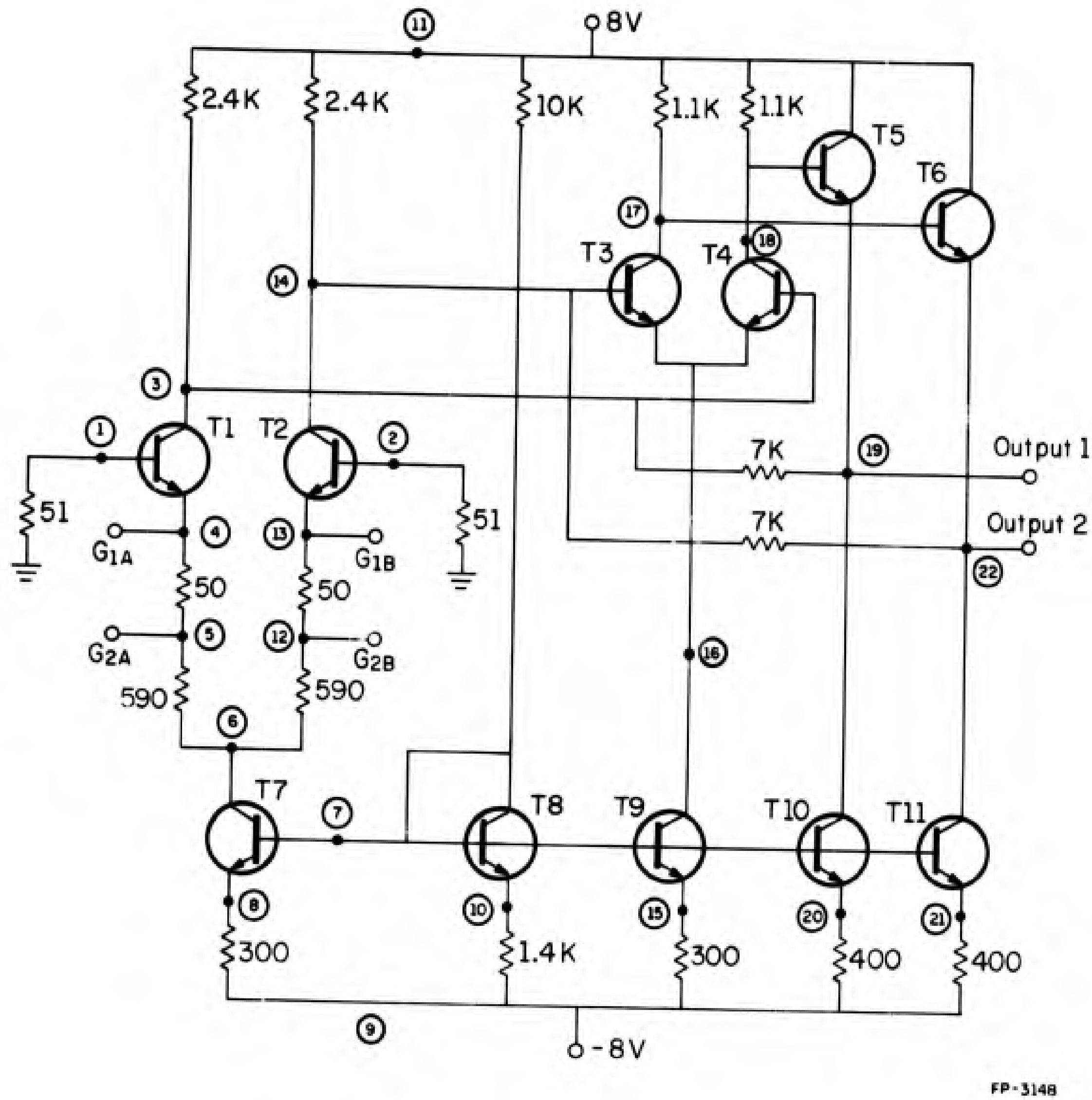


Figure 4.6. μA 733 differential video amplifier.

7. Collector Coupled Bistable Multivibrator

This circuit uses 2 equal (2N3642) transistors. As its name implies, this circuit has 2 stable states either of which remains until a stimulus is applied to make it change states. The two stable states in which the circuit will rest are:

1) with T1 on (saturated) and T2 off (nonconducting)

2) with the conditions of Q1 and Q2 reversed.

The transistors are connected essentially in cascade with a return connection to provide regeneration or positive feedback (see Figure 4.7).

The useful outputs of the bistable circuit are the voltages V_{c_1} and V_{c_2} appearing at the collectors of the two transistors. The collector of the conducting transistor will be very nearly at zero volts while the collector of the nonconducting transistor will be nearly 5 volts. The unstable state will occur when both transistors are carrying equal currents and both base voltages are identical. The conditions for such a situation found mathematically were approximately $v_{CE} = 0.8$ v and $v_{BE} = 0.3$ v. Any small disturbance such as thermal noise will cause the circuit to move rapidly to one of the stable states. The stable state the circuit achieves depends on the nature of the disturbance initiating the change since both stable states are equally probable at the unstable operating point.

8. Saturating Complementary Flip Flop (See Figure 4.8)

In this 4 transistor flip flop circuit, the collector return resistors of the lower N-P-N transistors are replaced by complementary

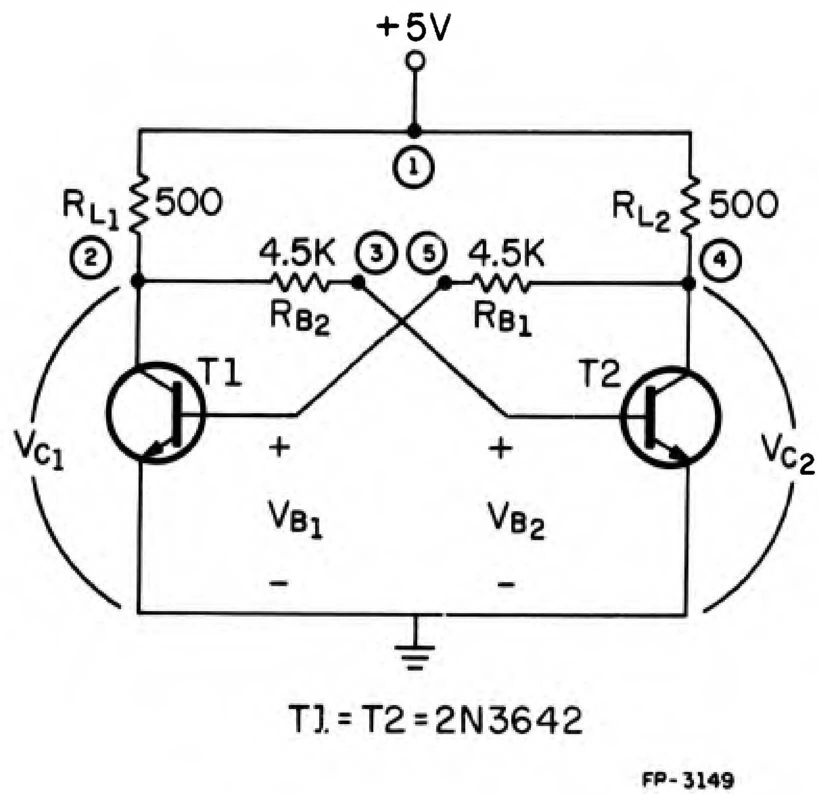


Figure 4.7. Collector coupled BISTABLE MULTIVIBRATOR.

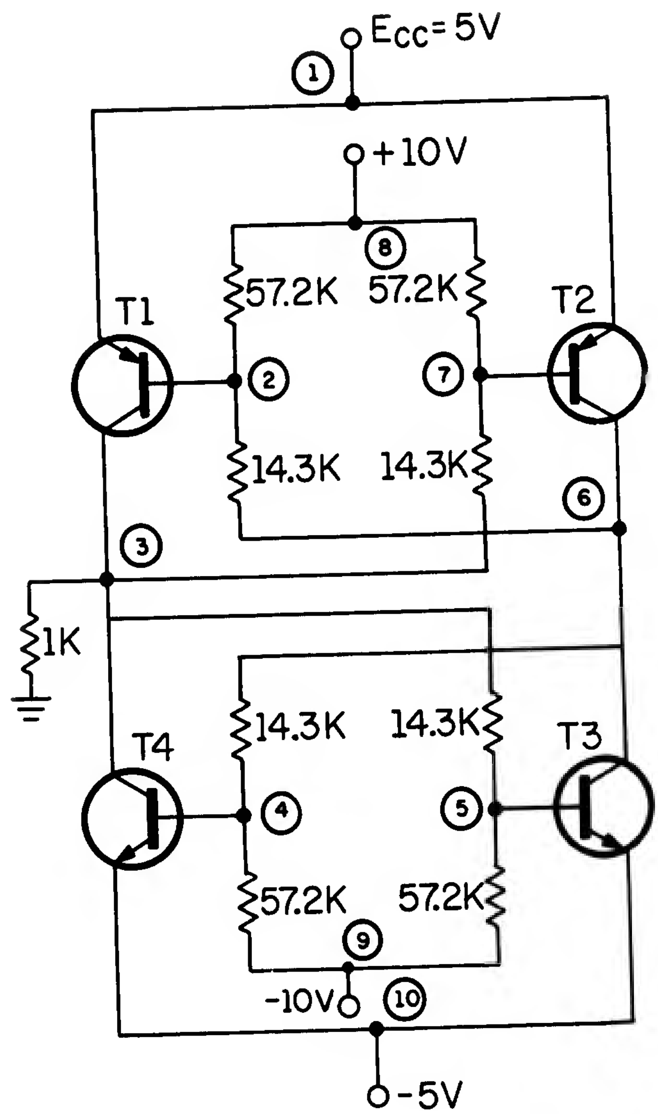


Figure 4.8. Saturating complementary flip-flop circuit.

P-N-P transistors. This arrangement of components yields a consistent output impedance to either load. At either load, looking back into the circuit, one ON and one OFF transistor are seen in parallel. Thus rise and fall times are equal, and response times are short. Also the circuit draws little stand-by power. The power drawn from the source is roughly proportional to the load requirements, and performance is relatively insensitive to component tolerances. Thus, the complementary flip flop constitutes a flexible building block circuit, adaptable to a wide variety of load requirements.

9. 741 Operational Amplifier (See Figure 4.9)

This is the familiar 741 operational amplifier. It has 19 transistors and 8 different transistor models.

10. Output Stage of Hearing Aid Amplifier

The circuit [18] is the output stage of a new class B integrated hearing aid amplifier. It has 9 transistors and 3 different transistor models. An interesting situation arises with this amplifier. If the charge storage elements are omitted for the transistors, i.e., if the default values $C_{j_x} = 0$ and $f_t = \infty$ for all transistors are used, the amplifier is unstable (see Figure 4.10).

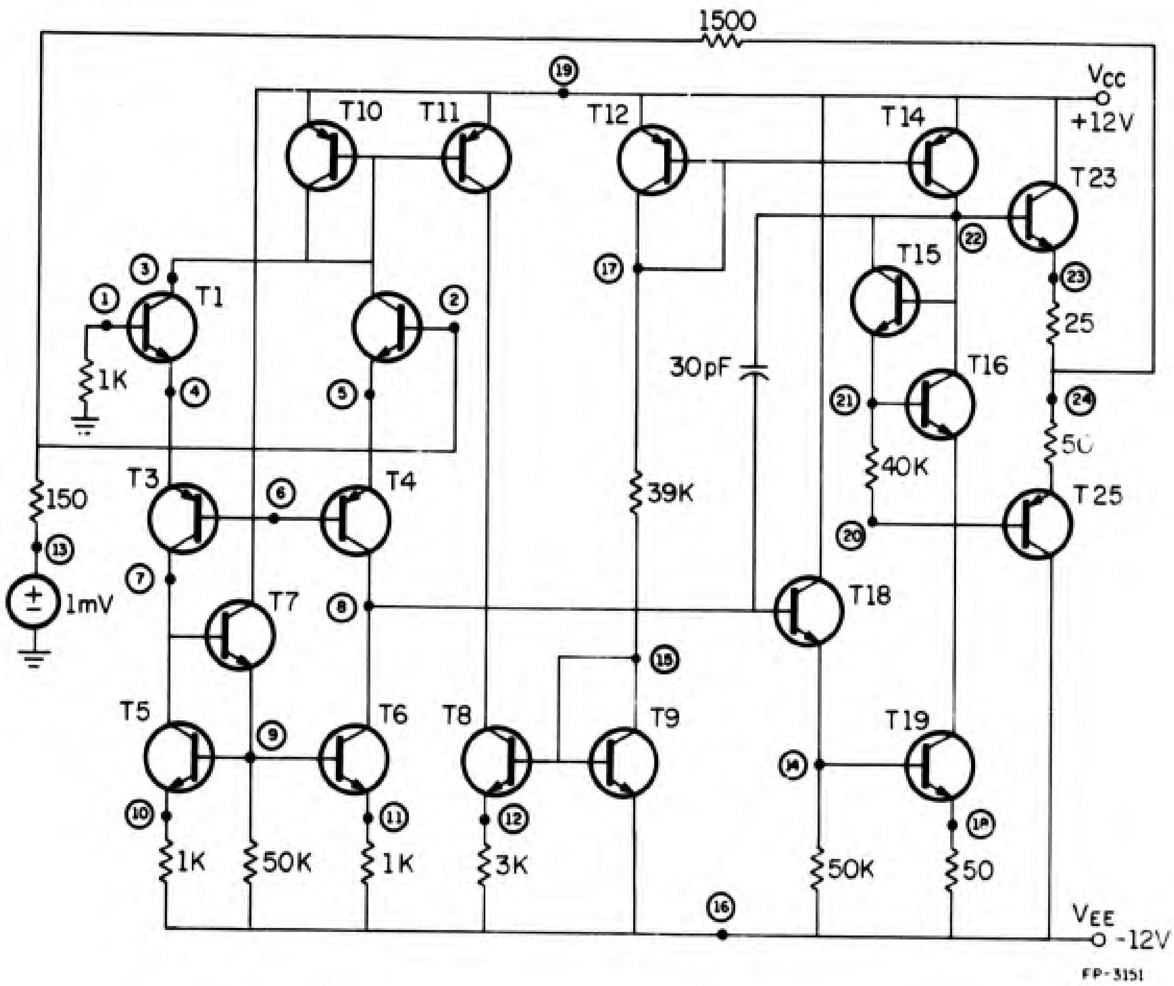


Figure 4.9. 741 OP AMP.

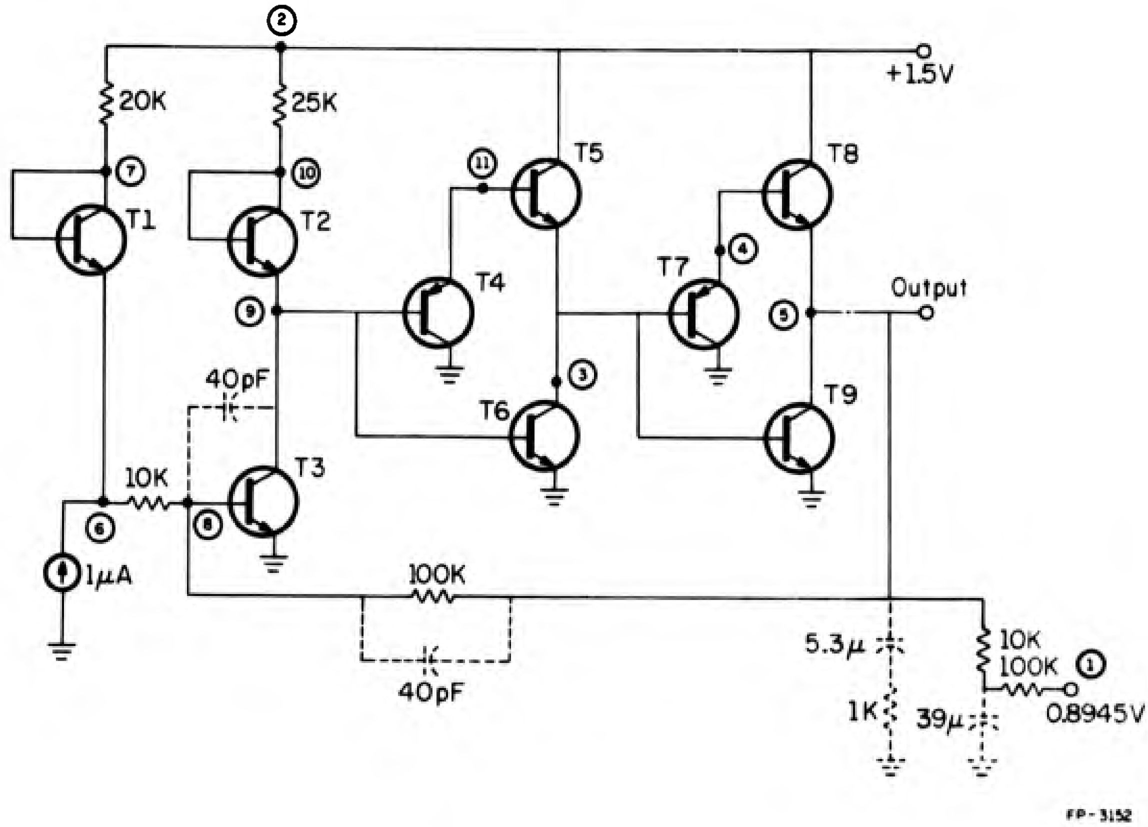


Figure 4.10. Output stage of integrated hearing aid amplifier.

V. COMPARISON OF RESULTS AND CONCLUSION

From the tabulated results in Table 5.1 note that ECAP II which is a norm reduction technique is the most reliable method. However, one pays a high price for this reliability in terms of computational cost. Particularly in large networks the computational cost was sometimes fifteen times greater than some of the other methods. Next we have the transformation of variable methods of COLON, BIAS 3, and CERMAK. These methods were definitely the fastest. The approach by COLON and BIAS 3 were nearly as reliable as ECAP II. The other method in this category by CERMAK required fewer iterations and less time than any other method for some of the smaller circuits. However, it seemed to have difficulty with large circuits.

The step size limitation approach in BROWN and CANCER also proved to be fast, but they were not quite as fast nor as reliable as BIAS 3 and COLON. Finally, the source stepping approach suggested by BROYDEN was very reliable except in some of the bistable circuits, however it required considerably more computational time.

In conclusion the transformation of variable methods (COLON, BIAS 3, and CERMAK) appear to be potentially the fastest methods for the dc solution of semiconductor circuits. The reliability of these methods could be improved by some type of source stepping, perhaps that suggested by CERMAK [4]. But source stepping should be applied only as a last resort to improve convergence as it can require excessive computational time. The method proposed by COLON has the simplest logic which means that it is the easiest to program.

	Constant Current Source without r_b, r_c		Constant Current Source with $r_b = 100\,\Omega$, $r_c = 10\,\Omega$		1 Kilohertz Oscillator	3 Cascaded Transistor Invertors with $r_b = 50\,\Omega$, $r_c = 10\,\Omega$	Operational Amplifier	
	IC1	IC2	IC1	IC2	IC1	IC2	IC1	IC2
COLON	1 sec 17 iter	1 sec 15 iter	2 sec 17 iter	2 sec 15 iter	1 sec 14 iter	< 1 sec 10 iter	13 sec 33 iter	7 sec 18 iter
BIAS 3	1 sec 16 iter	1 sec 15 iter	2 sec 16 iter	2 sec 15 iter	1 sec 10 iter	< 1 sec 13 iter	5 sec 13 iter	9 sec 23 iter
BROWN	2 sec 30 iter	2 sec 29 iter	5 sec 33 iter	5 sec 33 iter	2 sec 19 iter	2 sec 35 iter	25 sec 60 iter	26 sec 61 iter
CANCER	2 sec 32 iter	1 sec 17 iter	5 sec 32 iter	7 sec 44 iter	2 sec 20 iter	2 sec 36 iter	107 sec 248 iter	> 800 iter
ECAP II	7 sec 24 iter	4 sec 16 iter	11 sec 22 iter	9 sec 16 iter	8 sec 20 iter	3 sec 12 iter	39 sec 33 iter	138 sec 70 iter
BROYDEN	6 sec 68 iter	7 sec 83 iter	7800 iter	14 sec 85 iter	6 sec 56 iter	2 sec 35 iter	19 sec 47 iter	26 sec 63 iter
CERMAK	> 735 iter	1 sec 8 iter	> 705 iter	2 sec 9 iter	1 sec 6 iter	< 1 sec 6 iter	51 sec 66 iter	48 sec 62 iter

Table 5.1a

	μA 733 Differential Video Amplifier	Collector Coupled Bistable Multivibrator			Saturating Complementary Flip Flop			741 Operational Amplifier	Output of Hearing Aid Amplifier	
	IC1	Zero Initial conds.	T_1 on T_2 off	T_1 off T_2 on	Zero Initial Conds.	T_1 off T_2 on T_3 off T_4 on	T_1 on T_2 off T_3 on T_4 off	IC2	IC1	IC2
COLON	2 sec 12 iter	< 1 sec 6 iter	< 1 sec 5 iter	< 1 sec 5 iter	> 254 iter	< 1 sec 9 iter	< 1 sec 9 iter	6 sec 19 iter	1 sec 13 iter	1 sec 10 iter
BIAS 3	3 sec 14 iter	< 1 sec 6 iter	< 1 sec 16	< 1 sec 16	> 247 iter	< 1 sec 6 iter	< 1 sec 6 iter	16 sec 47 iter	1 sec 17 iter	1 sec 14 iter
BROWN	> 160 iter	< 1 sec 13 iter	< 1 sec 27 iter	< 1 sec 27 iter	> 555 iter	1 sec 22 iter	1 sec 22 iter			
CANCER	8 sec 32 iter	< 1 sec 9 iter	< 1 sec 16 iter	< 1 sec 16 iter	> 2000 iter	< 1 sec 15 iter	< 1 sec 15 iter			
ECAP II	30 sec 28 iter	< 1 sec 8 iter	1 sec 16 iter	1 sec 16 iter	1 sec 11 iter	3 sec 17 iter	3 sec 17 iter			
BROYDEN	14 sec 57 iter	< 1 sec 29 iter	69 sec 2471 iter	70 sec 2492 iter	> 500 iter	> 500 iter	> 500 iter			
CERMAK	8 sec 18 iter	< 1 sec 5 iter	< 1 sec 5 iter	< 1 sec 5 iter	> 260 iter	> 140 iter	> 260 iter			

Table 5.1b

REFERENCES

1. J. M. Ortega and W. R. Rheindboldt, Iterative Solution of Nonlinear Equations in Several Variables, Academic Press, Inc., New York, 1970.

2. D. A. Calahan, Computer-Aided Network Design, McGraw-Hill, Inc., 1972.

3. J. J. Ebers and J. L. Moll, "Large Signal Behavior of Junction Transistors," Proc. IRE, Vol. 42, December 1954, pp. 1761-1772.

4. I. A. Cermak and D. B. Kirby, "Nonlinear Circuits and Statistical Design," Bell Systems Technical J., Vol. 50, April 1971, pp. 1173-1195.

5. I. W. Sandberg, "Conditions for the Existence of a Global Inverse of Semiconductor-Device Nonlinear Network Operators," IEEE Trans. on Circuit Theory, CT-19, January 1972, pp. 34-36.

6. I. W. Sandberg, "Theorems on the Computation of the Transient Response of Nonlinear Networks Containing Transistors and Diodes," Bell System Technical Journal, Vol. 49, October 1970, pp. 1739-1776.

7. F. F. Kuo and W.G. Magnuson (editors), Computer Oriented Circuit Design, Prentice-Hall, Inc., 1969, Chapt. 4 by L. O. Chua.

8. D. F. Davidenko, "On a New Method of Numerical Solution of Systems of Nonlinear Equations," Dokl. Akad, Nauk SSSR, Vol. 88, 1953, pp. 601-602.

9. C. G. Broyden, "A Class of Methods for Solving Nonlinear Simultaneous Equations," Math. Comput., Vol. 19, October 1965, pp. 577-593.

10. R. D. Berry, "An Optimal Ordering of Electronic Circuit Equations for a Sparse Matrix Solution," IEEE Trans. Circuit Theory, Vol. CT-18, January 1971, pp. 40-50.

11. F. H. Branin, G. R. Hogsett, R. L. Lunde, and L. E. Kugel, "ECAP II - A New Electronic Circuit Analysis Program," IEEE Journal of Solid State Circuits, Vol. SC-6, August 1971, pp. 146-166.

12. C. G. Broyden, "A New Method of Solving Nonlinear Simultaneous Equations," Comput. J., Vol. 12, February 1969, pp. 94-99.

13. G. C. Brown, "DC Analysis of Nonlinear Networks," Electron. Lett., Vol. 5, August 1969, pp. 374-375.

14. L. Nagel and R. Rohrer, "Computer Analysis of Nonlinear Circuits, Excluding Radiation (CANCER)," IEEE Journal of Solid State Circuits, Vol. SC-6, August 1971, pp. 166-182.

15. L. D. Milliman, et al., "Circus, A Digital Computer Program for Transient Analysis of Electronic Circuits," Diamond Ordnance Fuze Lab., Washington, D. C., Rep. 346-2, January 1967.

16. W. J. Calla and W. G. Howard, "Bias-3, A Program for the Nonlinear dc Analysis of Bipolar Transistor Circuits," IEEE J. of Solid State Circuits, Vol. SC-6, February 1971, pp. 14-19.

17. Ivan A. Cermak, "DC Solution of Nonlinear State Space Equations in Circuit Analysis," IEEE Trans. on Circuit Theory, Vol. CT-18, March 1971, pp. 312-314.

18. T. E. Idleman, F. S. Jenkins, W. J. McCalla, and D. O. Pederson, "SLIC - A Simulator for Linear Integrated Circuits," IEEE J. of Solid State Circuits, Vol. SC-6, August 1971, pp. 188-203.

APPENDIX

For all the sample problems in Section IV the final solution in terms of the node voltages plus the following parameters are given:

BEF = FORWARD EMITTER SATURATION CURRENT
BCF = BACKWARD COLLECTOR SATURATION CURRENT
CB = CONVERGENCE CRITERION
AF = FORWARD α
AR = REVERSE α
θ = q/kT
IC = INITIAL CONDITIONS (IC1 or IC2)
N = NUMBER OF NODES.

Note: Both "e" and "E" do not represent exponential but instead are the FORTRAN representation for powers of ten.

1) Constant current source without r_b, r_c.

PARAMETERS - BEF = 0.1e - 14
BCF = 0.1e - 14
CB = 0.1e - 05
AF = 0.9802e - 00
AR = 0.6667e - 00
θ = 0.3890e +02
IC = IC1, IC2
N = 10

SOLUTION -

1	-.44974254E +01
2	-.27913966E +00
3	-.60000000E +01
4	-.65588142E +01
5	-.72185103E +01
6	-.64873731E +01
7	-.11994543E +02
8	-.58570615E +01
9	-.51179207E +01
10	-.32832145E +00

2) Constant current source with r_b = 100 Ω, r_c = 10 Ω. All parameters are the same as sample problem one except N = 22.

SOLUTION -

1	-.44731025E +01
2	-.44732224E +01
3	-.32833676E +00
4	-.35842688E +00
5	-.58568453E +01
6	-.64914450E +01
7	-.11994545E +02
8	-.65609331E +01
9	-.65606370E +01
10	-.60000001E +01
11	-.29954089E +00
12	-.32893273E +00
13	-.51115380E +01
14	-.51176157E +01
15	-.58567577E +01
16	-.64870174E +01
17	-.44735365E +01
18	-.44950220E +01
19	-.72224427E +01
20	-.30100952E +00
21	-.60000054E +01
22	-.29956996E +00

3) 1 Kilohertz Oscillator

PARAMETERS -

BEF = 0.1230e - 14
BCF = 0.7500e - 14
CB = 0.1e - 05
AF = 0.9836e + 00
AR = 0.1700e + 00
θ = 0.3890e + 02
IC = IC1
N = 13

SOLUTION -

1	.17938713E +01
2	.55989579E +01
3	.12286069E +01
4	.54190965E +00
5	.54190973E +00
6	.77590828E +00
7	.53948440E +00
8	.12207241E +01
9	.10481677E +01
10	.18031336E +01
11	.13172377E +01
12	.11638613E +01
13	.58916387E +00

4) 3 cascaded transistor invertors with $r_b = 50\ \Omega$, $r_c = 10\ \Omega$

PARAMETERS -
BEF = 0.1000e - 13
BCF = 0.1000e - 13
CB = 0.1e - 05
AF = 0.9901e + 00
AR = 0.6667e + 00
θ = 0.3890e + 02
IC = IC2
N = 14

SOLUTION -

1	.49979171E + 01
2	.83220012E + 00
3	.72805720E + 00
4	.49459233E + 01
5	.45031597E - 01
6	.16129944E + 00
7	.59746895E + 01
8	.16130869E + 00
9	.16130892E + 00
10	.49459232E + 01
11	.83086803E + 00
12	.72799165E + 00
13	.45325218E - 01
14	.16158726E + 00

5) Operational Amplifier

PARAMETERS -
BEF = 0.1000e - 14
BCF = 0.1000e - 14
CB = 0.1e - 05
AF = 0.9802e + 00
AR = 0.6667e + 00
θ = 0.3890e + 02
IC = IC1, IC2
N = 30

SOLUTION -

1	.36961553E - 01
2	.11556158E + 02
3	.85367929E + 00
4	.16703970E + 01
5	-.11057146E + 02
6	.12000000E + 02
7	-.11297849E + 02
8	-.11538459E + 02
9	-.11538459E + 02
10	-.11538459E + 02
11	-.11538387E + 02
12	-.11529369E + 02
13	.83519851E + 00
14	.11999961E + 02
15	-.11538459E + 02
16	-.11464180E + 02
17	-.11537627E + 02
18	-.11008622E + 02
19	.11538462E + 02
20	.16377361E + 01
21	-.11538409E + 02
22	.18844224E + 01
23	.18863324E + 01
24	.25127094E + 01
25	-.10999685E + 02
26	.11999805E + 02
27	.11473473E + 02
28	.20752228E + 01
29	.11999728E + 02
30	-.11444560E + 02

6) μA 733 differential video amplifier.

PARAMETERS -

BEF = 0.1000e - 13
BCF = 0.1000e - 13
CB = 0.1e - 05
AF = 0.9901e + 00
AR = 0.6667e + 00
θ = 0.3890e + 02
IC = IC1
N = 22

SOLUTION -	1	-.83280295E - 03
	2	-.13424069E - 02
	3	.22999484E + 01
	4	-.67709634E + 00
	5	-.81008170E + 00
	6	-.23793089E + 01
	7	-.56741067E + 01
	8	-.63684409E + 01
	9	-.79799833E + 01
	10	-.63294552E + 01
	11	.79800360E + 01
	12	-.81054450E + 00
	13	-.67759837E + 00
	14	.22999924E + 01
	15	-.63684409E + 01
	16	.16237107E + 01
	17	.50344484E + 01
	18	.50394011E + 01
	19	.43507881E + 01
	20	-.63611613E + 01
	21	-.63611613E + 01
	22	.43458397E + 01

7) Collector Coupled Bistable Multivibrator

PARAMETERS -

BEF = 0.5000e - 07
BCF = 0.5000e - 07
CB = 0.1e - 05
AF = 0.9868e + 00
AR = 0.5000e + 00
θ = 0.3890e + 02
N = 5
IC = 0.

SOLUTION -	1	.49832884E + 01
	2	.80537242E + 00
	3	.30916317E + 00
	4	.80538499E + 00
	5	.30916325E + 00

IC	(T_1 on, T_2 off)
1	0.0
2	0.6
3	0.0
4	0.0
5	0.6

SOLUTION -		
	1	.49891900E + 01
	2	.51513256E - 01
	3	.51626482E - 01
	4	.45218609E + 01
	5	.31757626E + 00

IC	(T_1 off, T_2 on)
1	0.0
2	0.0
3	0.6
4	0.6
5	0.0

SOLUTION -		
	1	.49891900E + 01
	2	.45218609E + 01
	3	.31757626E + 00
	4	.51513257E - 01
	5	.51626483E - 01

8) Saturating Complementary Flip Flop

PARAMETERS -

BEF = 0.1000e - 13
BCF = 0.1000e - 13
CB = 0.1e - 05
AF = 0.9100e + 00
AR = 0.5000e + 00
θ = 0.4000e + 02
N = 10
IC = 0.

<u>SOLUTION (UNSTABLE)</u> -

1	.49954511E +01
2	.43416967E +01
3	.23283064E - 07
4	-.43416967E +01
5	-.43416967E +01
6	-.22351742E - 07
7	.43416967E +01
8	.99998022E +01
9	-.99998022E +01
10	-.49954511E +01

IC	(T_1 on, T_2 off, T_3 on, T_3 off)
1	0.4
2	0.0
3	0.0
4	0.0
5	0.4
6	0.4
7	0.4
8	0.0
9	0.0
10	0.0

<u>SOLUTION (STABLE)</u> -

1	.49940563E +01
2	.43162651E +01
3	.48353529E +01
4	-.58681155E +01
5	-.43162651E +01
6	-.48353529E +01
7	.58681155E +01
8	.99998284E +01
9	-.99998284E +01
10	-.49940563E +01

IC	(T_1 off, T_2 on, T_3 off, T_4 on)
1	0.4
2	0.4
3	0.4
4	0.4
5	0.0
6	0.0
7	0.0
8	0.0
9	0.0
10	0.0

SOLUTION (STABLE) -

1	.49940563E + 01
2	.58681155E + 01
3	-.48353529E + 01
4	-.43162651E + 01
5	-.58681155E + 01
6	.48353529E + 01
7	.43162651E + 01
8	.99998284E + 01
9	-.99998284E + 01
10	-.49940563E + 01

9) 741 Operational Amplifier

PARAMETERS

CB = 0.1×10^{-5}
N = 25
IC = IC2

Model 1

θ = 0.3890e + 02
BEF = 0.1000e - 14
BCF = 0.5000e - 14
AFS = 0.9933e - 00
ARS = 0.9950e - 00

Model 2

θ = 0.3890e + 02
BEF = 0.1000e - 14
BCF = 0.7500e - 14
AFS = 0.9803e - 00
ARS = 0.9615e - 00

Model 3

θ = 0.3890e + 02
BEF = 0.1000e - 14
BCF = 0.7500e - 14
AFS = 0.9859e - 00
ARS = 0.9615e - 00

Model 4

θ = 0.3890e + 02
BEF = 0.1000e - 14
BCF = 0.7500e - 14
AFS = 0.9523e - 00
ARS = 0.9615e - 00

Model 5

θ = 0.3890e + 02
BEF = 0.1000e - 14
BCF = 0.5000e - 14
AF = 0.9941e - 00
AR = 0.9950e - 00

Model 6

θ = 0.3890e + 02
BEF = 0.1000e - 14
BCF = 0.5000e - 14
AF = 0.9955e - 00
AR = 0.9933e - 00

Model 7

θ = 0.3890e + 02
BEF = 0.1000e - 14
BCF = 0.7500e - 14
AF = 0.9967e - 00
AR = 0.5000e - 00

Model 8

θ = 0.3890e + 02
BEF = 0.1000e - 14
BCF = 0.3000e - 14
AF = 0.9900e - 00
AR = 0.9950e - 00

SOLUTION -

1	-.78495610E - 04
2	-.14753123E - 04
3	.11382089E + 02
4	-.59938232E + 00
5	-.59935045E + 00
6	-.11986861E + 01
7	-.10789276E + 02
8	-.10673008E + 02
9	-.11386759E + 02
10	-.11985622E + 02
11	-.11985622E + 02
12	-.11919367E + 02
13	.99327978E - 03
14	-.11278244E + 02
15	-.11302438E + 02
16	-.11998721E + 02
17	.11303635E + 02
18	-.11972227E + 02
19	.11998728E + 02
20	-.66327564E + 00
21	.29687878E - 01
22	.63893155E + 00
23	-.78639631E - 02
24	-.99771725E - 02
25	-.14535673E - 01

10) Output of Hearing Aid Amplifier

PARAMETERS

CB = 0.1×10^{-5}
N = 11
IC = IC1, IC2

Model 1

θ = 0.3890e + 02
BEF = 0.4000e - 13
BCF = 0.4000e - 13
AF = 0.9900e - 00
AR = 0.5000e - 00

Model 2

θ = 0.3890e + 02
BEF = 0.1000e - 14
BCF = 0.1000e - 14
AF = 0.7500e - 00
AR = 0.5000e - 00

Model 3

θ = 0.3890e + 02
BEF = 0.1500e - 13
BCF = 0.1500e - 13
AF = 0.9677e - 00
AR = 0.5000e - 00

SOLUTION -		
	1	.89450539E + 00
	2	.14949474E + 01
	3	.48783050E - 01
	4	.73101057E + 00
	5	.14875332E + 01
	6	.15975219E + 01
	7	.14949494E + 01
	8	.15875230E + 01
	9	.57330582E + 00
	10	.10832243E + 01
	11	.98141000E + 00