INVESTIGATION OF PHASE LOCKING OF MICROWAVE OSCILLATORS

Jackie Lee Clark

Naval Postgraduate School
Monterey, California

December 1972

NAVAL POSTGRADUATE SCHOOL
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THESIS

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OF MICROWAVE OSCILLATORS

by

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Thesis Advisor: D.B. Hoisington

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This paper is a report on experimental thesis work which investigated phase locking of a reflex klystron with a more stable microwave source. A discussion of the characteristics and components of a phase-locked loop and a qualitative overview of the theory of phase-locked loop operation is included. The specific circuit which accomplished phase locking at approximately 9.1 GHZ is described, with particular emphasis on the use of a crystal mixer tc provide the phase-sensitive feedback voltage for klystron frequency control. Capture and tracking ranges of this phase-locked loop are predicted and determined experimentally. The stabilization of the reflex klystron frequency by the phase-locked loop is demonstrated by spectrum photographs. A phase detector circuit which is expected tc provide a wide capture and tracking range with the VCO offset from the reference frequency is proposed and described. Progress toward realization of this detector and suggestions for its improvement are included in this report.

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Investigation of Phase Locking of Microwave Oscillators

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ABSTRACT

This paper is a report on experimental thesis work which investigated phase locking of a reflex klystron with a more stable microwave source. A discussion of the characteristics and components of a phase-locked loop and a qualitative overview of the theory of phase-locked loop operation is included. The specific circuit which accomplished phase locking at approximately 9.1 GHZ is described, with particular emphasis on the use of a crystal mixer to provide the phase-sensitive feedback voltage for klystron frequency control. Capture and tracking ranges of this phase-locked loop are predicted and determined experimentally. The stabilization of the reflex klystron frequency by the phase-locked loop is demonstrated by spectrum photographs. A phase detector circuit which is expected to provide a wide capture and tracking range with the VCO offset from the reference frequency is proposed and described. Progress toward realization of this detector and suggestions for its improvement are included in this report.

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I. INTRODUCTION

This thesis investigated the application of phase-locked loops in circuits operating at a microwave frequency. In particular, a reflex klystron operating at about 9.1 GHZ was phase-locked with a microwave sweep oscillator resulting in a markedly more stable spectrum for the klystron. This phase-locked loop proved the value of stabilizing a high-power microwave transmitter with a low-level but stable source.

The second part of this thesis investigated offset phase-locked loops for use at microwave frequency. A circuit for the accomplishment of offset locking is proposed and discussed. The components of this circuit were assembled but offset locking was not demonstrated because of difficulties in the realization of the phase detector. These difficulties, and suggestions for their resolution, are discussed later in this report. The theory of this proposed offset phase-locked loop is believed valid, and the circuits assembled by this researcher are suggested as a starting point for continued investigation of offset phase-locking of microwave sources.

II. THE PHASE-LOCKED LOOP

A. GENERAL

A phase-locked loop (PLL) is, essentially, an automatic frequency-control circuit which depends on the determination of phase difference between two signals to generate an error voltage. This voltage is applied in a feedback path to control the frequency of one of the signals. Since frequency is the time derivative of phase, the larger the instantaneous frequency difference between the two signals the larger the rate of change of the error voltage.

The concepts of phase-locking have been known since the early 1930's, but it was not until the advent of color television that PLL's were used widely [Ref. 1]. Many color television receivers use phase-locking in the chrominance signal processing section. Other applications include satellite-earth data links where the PLL enhances detection of a small signal in noise [Ref. 2]; and FM or AM demodulation, signal conditioning, and frequency multiplication, division and translation. An integrated circuit which is useful for frequencies in excess of 30 MHZ has been developed and is used in these latter applications [Ref. 3].

Phase-locked loops have already been used with reflex klystrons and at microwave frequencies [Refs. 4 and 5]. In 1968 Sage Laboratories offered as a new product a Sweeplock Synchronizer to offset phase-lock two microwave sweep oscillators 30 MHZ apart. With the expanding communications

requirements of the world and the already dense signal environment at lower frequencies, increased use of the microwave spectrum is anticipated. Thus, continued investigation of phase-locking at these frequencies was considered appropriate.

BLOCK DIAGRAM OF PHASE-LOCKED LOOP

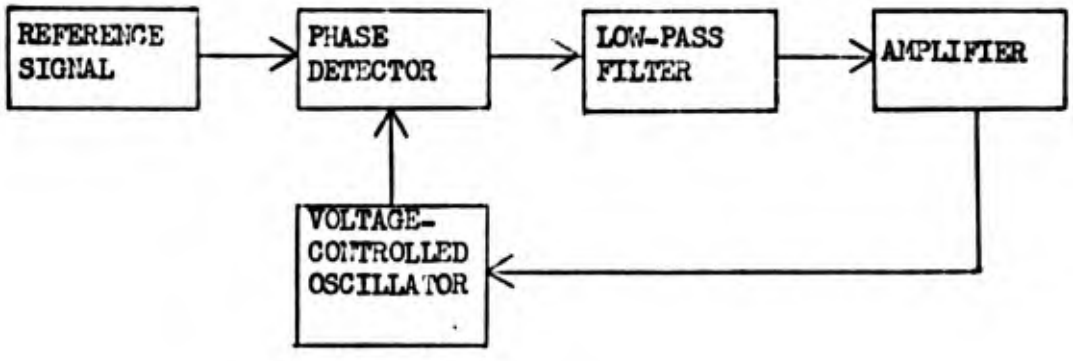


Figure 1

B. OPERATION OF A PHASE-LOCKED LOOP

A block diagram for a typical phase-locked loop is given in Fig. 1. The reference signal is the frequency to which the voltage-controlled oscillator (VCO) is locked by the functioning of the PLL. Depending on the application of the PLL, the reference signal might be the output of a highly-stable, low-level oscillator; the RF section of a receiver; or in experimental work, a stable, controllable-frequency, constant-amplitude signal source.

The phase detector (comparator, multiplier) compares the frequency and phase of the reference and VCO signals and furnishes a voltage related to the phase difference. Components of the phase detector output higher in frequency than the difference between the input signals are attenuated in the low-pass filter, whose cutoff determines the maximum frequency separation at which the PLL will function and, therefore, its capture range. Amplification provides the gain necessary for the low-pass filter output to control the VCO frequency, and the amplifier has flat response over the frequency range of the PLL (the capture range).

Frequency stability and FM demodulation characteristics of the PLL normally are determined by the VCO, thus this component is critical to the loop's performance. Desirable properties of the voltage-controlled oscillator are [Ref. 3]:

1. Linear voltage-to-frequency conversion.
2. Good frequency stability.
3. High conversion gain (sensitivity to small variations in control terminal voltage).
4. Wide tracking range (tunable over a wide band of frequencies by variation of control terminal voltage).

A detailed mathematical analysis of phase-locked loop operation is beyond the scope of this report. References 1 and 2 contain much of the detail of this analysis and include considerations of noise and other disturbances. A qualitative view of phase-locked loop functioning, drawn largely from Ref. 3, is offered here. When initial VCO and

reference signals (frequencies f_o and f_s respectively) are applied to the phase detector the output is a voltage related to the frequency difference. This voltage is filtered, amplified, and applied to the control input of the VCO causing it to change frequency so as to reduce this frequency difference. This process continues until the difference frequency is zero (average) and the two signals are synchronized, or in frequency lock.

In frequency lock the two signals are at the identical average frequency but differ by a phase angle necessary to generate the voltage which shifts the VCO to the reference frequency. Any variations in either the VCO or reference frequency will change the feedback voltage as necessary to shift the VCO to the reference frequency. Thus, the VCO is locked to the reference signal and will follow its variations. For example, if the reference signal is frequency modulated and the frequency control characteristic is linear, the voltage necessary to keep the VCO locked is an amplified replica of the modulating signal. Thus, the PLL can be used as an FM demodulator.

Frequency and phase errors in the loop are related as

$$2\pi\Delta f = d\theta_o/dt$$

where Δf is the difference frequency between the two signals and θ_o is the phase difference between the VCO frequency and the reference signal. Large frequency differences mean the phase difference is changing rapidly, and vice versa. At a

particular initial setting of f_o and f_s resulting in a difference frequency, Δf, the phase detector will furnish a sinusoidal voltage at the difference frequency. If this voltage is passed by the filter and amplified it will modulate the VCO frequency and Δf itself will become a function of time. The resultant phase detector output becomes asymmetrical, as is shown in Fig. 2 [Ref. 3]. Because of this asymmetry the phase detector output has a non-zero average value which shifts the VCO frequency toward synchronism with the reference signal.

PHASE DETECTOR OUTPUT

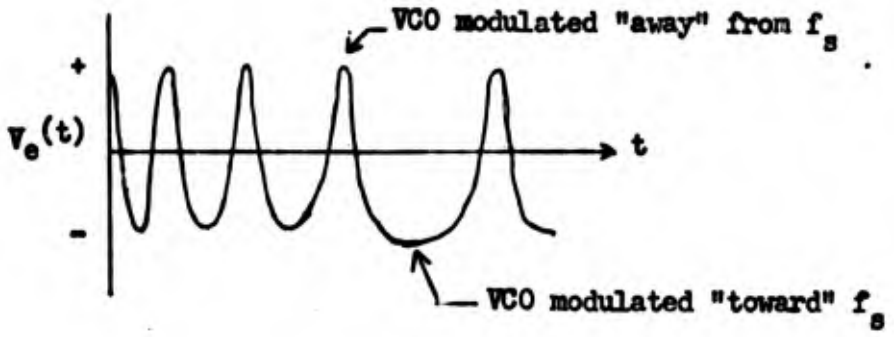


Figure 2

III. PHASE DETECTION

Phase detectors are identified as a multiplier [Refs. 1 and 2] or as a "synchronous type switch that is opened and closed by the reference input, and effectively 'chops' the signal input at the same repetition rate as the reference drive." [Ref. 3]. These phase detectors, and others, have in common an output which is a sinusoid whose argument includes the phase difference between the two inputs of the detector. Viterbi [Ref. 1] further desired this sinusoid to be a "sine" as opposed to a "cosine"; other wise the magnitude of the error signal will increase as the phase difference decreases and will not reflect the polarity of this difference since cosine $(-\theta)$ = cosine (θ). Thus, the phase detector output should be a sine function of the difference between the phases of the reference and VCO signals.

Phase detection can be accomplished by mixing the two signals, as the following derivation shows. A non-linear mixer has as output

$$V_p = k_1 V_i + k_2 V_i^2 + k_3 V_i^3 + \ldots\ldots\ldots\ldots$$

where V_i is the signal input to the mixer and the k's are constants which depend on the mixer's conversion loss. If the magnitude of the input is small, third and higher power terms will be very small in comparison to lower order terms and can be disregarded. The mixer output thus becomes

$$V_p = k_1 V_i + k_2 V_i^2$$

The mixer input is the sum of the VCO signal, V_o, and the reference signal, V_s. These signals are sinusoidal functions of time and are represented mathematically by the equations

$$V_s = A_s \sin[2\pi f_s t + \theta_s(t)]$$

$$V_o = A_o \cos[2\pi f_o t + \theta_o(t)]$$

where A_s and A_o are the signal amplitudes. Then the mixer input is

$$V_i = A_s \sin[2\pi f_s t + \theta_s(t)] + A_o \cos[2\pi f_o t + \theta_o(t)]$$

After performing the indicated squaring and multiplication the output of the mixer is

$$V_p = k_1 A_s \sin[2\pi f_s t + \theta_s(t)] + k_1 A_o \cos[2\pi f_o t + \theta_o(t)] +$$

$$k_2 A_s^2 \sin^2[2\pi f_s t + \theta_s(t)] + k_2 A_o^2 \cos^2[2\pi f_o t + \theta_o(t)] +$$

$$2k_2 A_s A_o \sin[2\pi f_s t + \theta_s(t)] \cos[2\pi f_o t + \theta_o(t)]$$

Using trigonometric identities for the square of the sine and of the cosine and for the product of the sine and the cosine, this becomes

$$V_p = \tfrac{1}{2}k_2A_s^2 + \tfrac{1}{2}k_2A_o^2 + k_2A_sA_o\sin[2\pi(f_s-f_o)t + \theta_s(t) - \theta_o(t)] +$$

$$k_1A_s\sin[2\pi f_s t + \theta_s(t)] + k_1A_o\cos[2\pi f_o t + \theta_o(t)] +$$

$$k_2A_sA_o\sin[2\pi(f_s+f_o)t + \theta_s(t) + \theta_o(t)] +$$

$$\tfrac{1}{2}k_2A_o^2\cos 2[2\pi f_o t + \theta_o(t)] - \tfrac{1}{2}k_2A_s^2\sin 2[2\pi f_s t + \theta_s(t)]$$

All component with frequency higher than f_s-f_o will be attenuated by the low pass filter leaving as the input to the amplifier

$$V_a = \tfrac{1}{2}k_2(A_s^2 + A_o^2) + k_2A_sA_o\sin[2\pi(f_s-f_o)t + \theta_s(t) - \theta_o(t)]$$

Before phase lock is achieved $f_s \neq f_o$ and the amplifier input is at the difference frequency. After phase lock is achieved, $f_s = f_o$ and instantaneous frequency differences are associated with $\theta_s(t) - \theta_o(t)$. Thus, the input to the amplifier after phase lock is achieved is

$$V_a = A + B\sin[\theta_s(t) - \theta_o(t)]$$

where $A = \tfrac{1}{2}k_2(A_s^2 + A_o^2)$ and $B = k_2A_sA_o$

The two components of V_a are a dc level, A, and an ac signal with amplitude B. Since A is derived from squared terms the dc level is always positive. However, the ac term will be positive or negative depending on the argument of the sine, $\theta_s(t) - \theta_o(t)$. If the two inputs to the mixer have equal amplitude ($A_s = A_o$), the dc level is equal to the peak ac magnitude and V_a can vary only between zero and

twice the dc level. Particularly significant, though, is the presence of the dc voltage, A, to provide VCO frequency shift even when the argument of the sine term is zero – when the phase difference between the VCO and reference signals is zero. Thus, it is possible to achieve phase lock without the phase difference specified by Gerbene [Ref. 3] to hold the VCO at the reference signal frequency.

This derivation shows that a non-linear mixer can provide the phase-sensitive output required of a phase detector. The mixer also furnishes a dc level which enables phase-locking with zero phase error. However, use of a mixer as the phase detector does limit the performance of a PLL in some ways. The dc level has the same polarity regardless of the direction of the frequency separation between the VCO and reference singals – whether f_s is greater or less than f_o. The mixer-derived error voltage will shift the VCO in only one direction from its center frequency. The magnitude of the dc level is a function only of the signal amplitudes, not of the frequency or phase separation (when lock has not occurred). Thus, the mixer-derived error voltage actually results in a new operating point for the VCO – a new center frequency, with the ac portion of the error voltage producing frequency changes around this new operating point. If this new operating point is near the limit of the VCO's tracking range the phase-related error voltage might drive the VCO out of oscillation before capture occurs. Conversely, if the loop

is activated with the two frequencies very close together the dc error voltage might drive the VCO through the lock frequency before capture is accomplished. Finally, this mixer-derived error voltage is amplitude sensitive. It is therefore highly desirable that the VCO and reference signals be at the same, unvarying level. This was accomplished manually with attenuators during this thesis work. However, clamping circuits in each signal path can be used as well.

IV. EXPERIMENTAL CURCUIT

CIRCUIT DIAGRAM

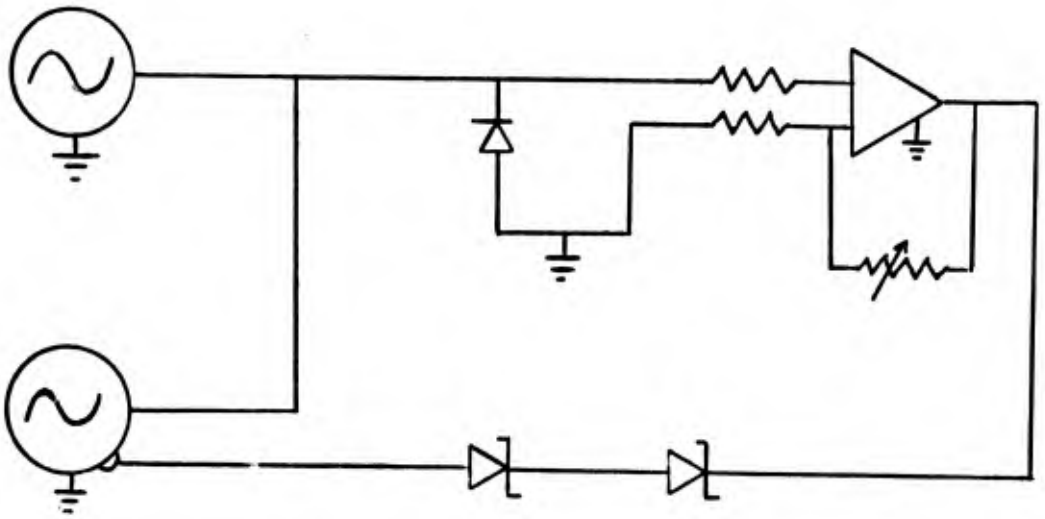


Figure 3

The experimental circuit used in this thesis work is diagrammed above. Various elements which permitted monitoring of the circuit or the establishment and control of initial conditions, but which did not affect the operation of the phase-locked loop, are not diagrammed. Circuit elements, including those not shown in Fig. 3, are discussed in the following paragraphs.

A Hewlett Packard 8690B microwave sweep oscillator was selected as the reference signal source. This source featured easy manual tuning, controllable-speed sweep, a constant level output regardless of frequency, and a

reasonably "clean" signal spectrum. Each signal path contained an isolator which prevented reflection of energy into the oscillator cavities. A variable attenuator in each signal path, used in conjunction with power meters connected through directional couplers, provided manual control of signal levels so that the ac and dc components of the error voltage were equal.

A cavity wavemeter in each signal path was used to determine the frequency of each of the signal sources. Although the dial of the sweep oscillator proved to be accurate, the wavemeter was the only method used to measure the klystron frequency directly – a spectrum analyzer was inaccurate for frequency measurement in the microwave region. The magic "T" summed the two microwave signals for input to the crystal mixer diode and also provided a connection point for the spectrum analyzer (difference port). A 1N23WE microwave diode mounted in a waveguide-to-coaxial adapter on the summing port of the magic "T" was used as the phase detecter. A CA 3029A integrated circuit operational amplifier provided both the gain and low-pass filtering necessary in the loop. The variable resistor in the amplifier feedback path enabled continuous gain control from zero to a voltage gain of 50 from dc to 2.5 MHZ, where rolloff began.

The Zener diodes shown in the schematic provided isolation between the low-level operational amplifier output and the high (negative) voltage on the reflector terminal of

the klystron. These diodes dictated some of the parameters of the PLL, such as reflector voltage operating point and tracking range. Attempts to use a high-voltage PNP transistor (2N6213) to provide this isolation were unsuccessful. This transistor would have permitted operation at any reflector voltage which did not break down the transistor; further, this transistor does not clamp the reflector at any voltage as did the Zener diodes.

A reflex klystron using a Varian 2K25 tube and a Hewlett Packard Model 715A power supply comprised the VCO in this phase-locked loop. The schematic diagram of a typical reflex klystron is shown in the figure below [Ref. 6]. Gross frequency control is accomplished by mechanically adjusting the resonator dimensions. Manual variation of beam and reflector voltage, using controls on the power supply, enabled frequency changes of several percent. However, the interest of this thesis was in automatic frequency control; thus the reflector voltage was modulated as indicated at the bottom of the schematic. The filtered and amplified mixer output was applied at this point, through the Zener diodes, to provide automatic frequency control of the reflex klystron.

Since the VCO is a critical element of the phase-locked loop the reflex klystron's properties were investigated to determine its utility as a VCO. Figure 5 verified the klystron's linear voltage-to-frequency conversion, conversion gain, and wide frequency tracking range. Tuning was easy

SCHEMATIC DIAGRAM OF A REFLEX KLYSTRON

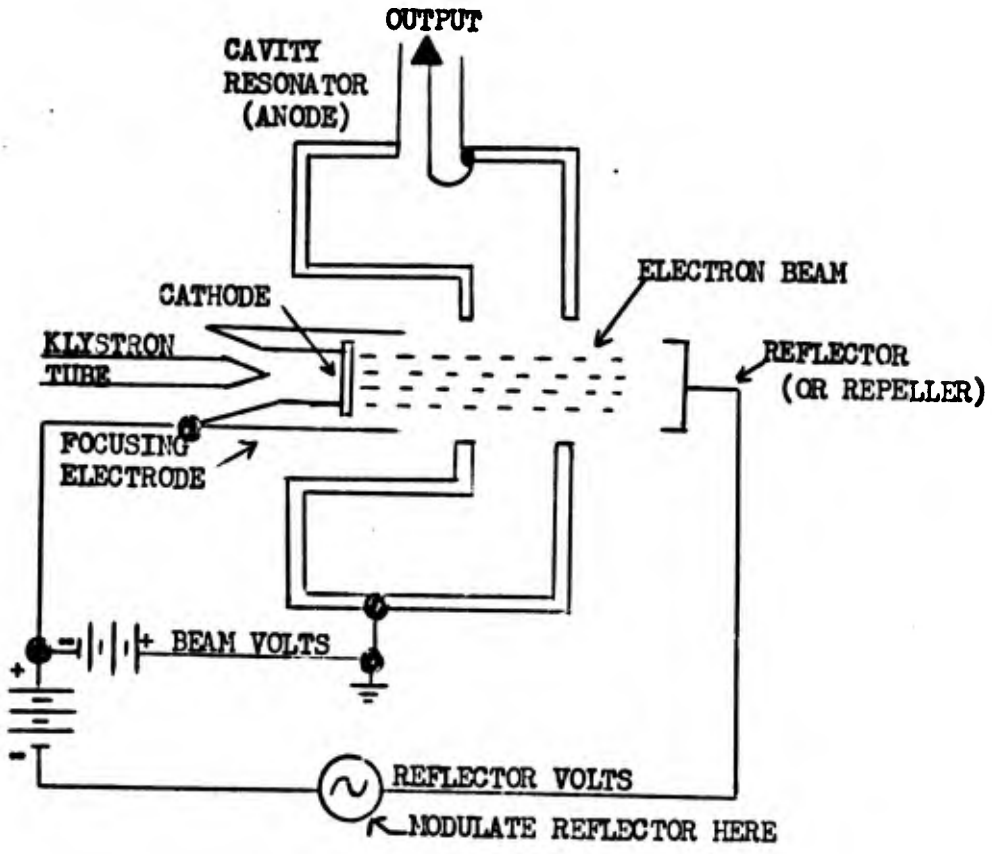


Figure 4

by the three ways listed in the preceding paragraph. And, since frequency stabilization was one of the goals of the experimental circuit, the dispersion and frequency drift of the klystron output were considered unimportant.

VOLTAGE-FREQUENCY PLOT

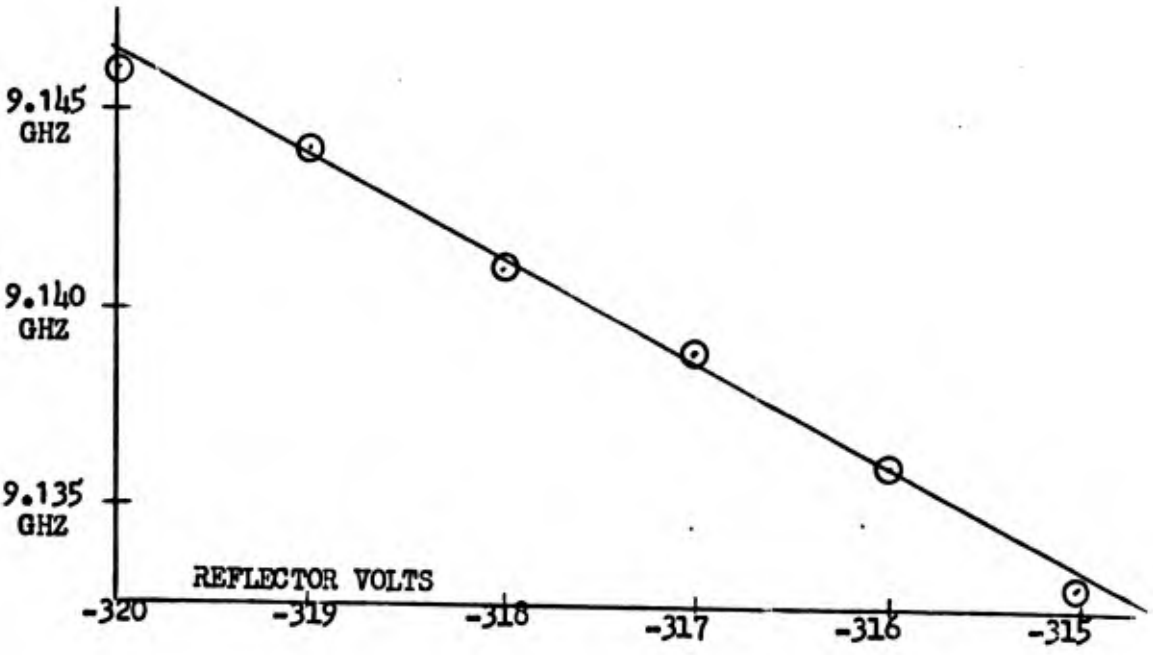


Figure 5

Waveguide (.4" x .9") was used for the signal paths from the sources to the magic "T". Since the signal paths were the same length, had the same number of connections, and had nominally identical elements it was assumed any random phase shifts between the sources and the mixer were cancelled at the mixer. The Zener diodes were assumed to be short-circuits to ac components of the error voltage and thus not sources of phase shifts. Thus it was necessary to determine the phase error due only to the mixer and amplifier. This was accomplished by splitting the klystron output and providing it in two equal-length paths to the mixer. One path included a variable phase shifter which controlled the

relative phase between the mixer inputs. Mixer and amplifier output voltages each twenty degrees of phase difference indicated a small phase error, which was considered insignificant. The crystal mixer-operational amplifier combination was evaluated satisfactory for this phase-locked loop experiment.

V. PREDICTED AND EXPERIMENTAL RESULTS

The Zener diodes provided a voltage drop of -317 volts with more than twenty microamperes current through them. This limited the tracking range indicated by Fig. 5 between -317 and -320 reflector volts corresponding to 7.875 MHZ, which was estimated to be the tracking range of this phase-locked loop.

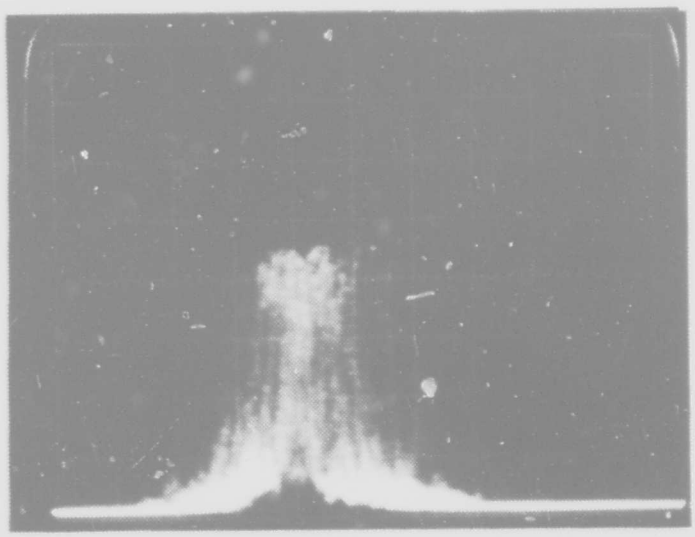
A dc level, A, was applied to the reflector terminal as soon as the loop was activated, even if the VCO and reference signals were widely separated in frequency. This resulted in a new operating point for the klystron with capture to be determined by the magnitude of the ac feedback voltage. Selection of attenuator-controlled signal levels and amplifier gain to provide a peak ac voltage of one volt yielded a predicted capture range of 2.625 MHZ - the slope of the frequency-voltage plot. in Fig. 5.

Capture and tracking ranges were determined by observation of a spectrum analyzer presentation of the two signals at the difference port of the magic "T". As the separation between the two frequencies was decreased (by either tuning the sweep oscillator down to the reflex klystron or by tuning the klystron up to the sweep oscillator) a critical point was reached. The frequency of the klystron became markedly less stable, as presented on the spectrum analyzer, when the difference frequency approached two MHZ. Further decrease

in the frequency separation resulted in capture. After numerous repetitions of this procedure, the capture range was established at two MHZ when the klystron frequency was below that of the reference signal. Capture range was established at approximately 500 KHZ when the klystron frequency was above that of the reference signal. This was attributed to the instability of the klystron and incidental FM rather than action of the phase-locked loop.

Tracking range was evaluated as seven MHZ with the reference frequency sweeping down toward that of the klystron; and as 2.5 MHZ when the reference frequency was sweeping upward. Tracking was bi-directional when the downward sweep of the reference frequency was stopped before track was lost - the klystron followed reference frequency variations in both directions from such a locked frequency.

Stabilization of the klystron frequency by phase-locking to the sweep oscillator was proven by the following three photographs. All were taken with the spectrum analyzer at the same gain and time-base setting and using the log scale. In addition to the wide dispersion of the klystron's frequency spectrum, it was subject to drift of as much as 500 KHZ even after a long warm-up time.



SPECTRUM OF
REFLEX KLYSTRON
AT APPROXIMATELY
9.1 GHZ
BEFORE PHASE LOCKING A

DISPERSION:
50 KHZ/DIVISION

LOG SCALE

Figure 6

SPECTRUM OF
HEWLETT PACKARD
8690B OSCILLATOR
AT APPROXIMATELY
9.1 GHZ

DISPERSION
100 KHZ/DIVISION

LOG SCALE

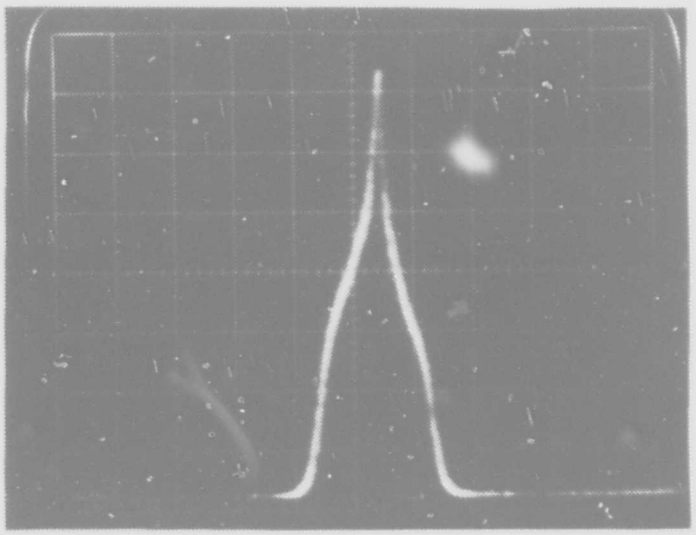


Figure 7

SPECTRUM OF
REFLEX KLYSTRON
AT APPROXIMATELY
9.1 GHZ
AFTER PHASE LOCKING

DISPERSION:
50 KHZ/DIVISION

LOG SCALE

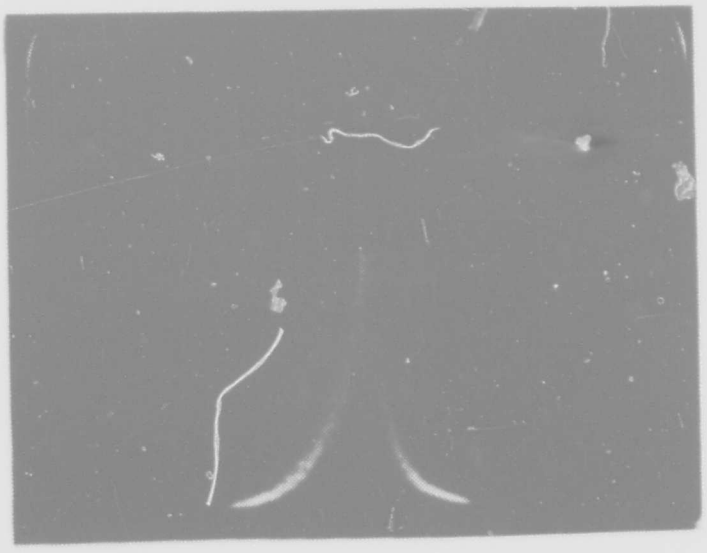


Figure 8

The magnitude of the error signal which produced phase-lock increased as the separation between the klystron and reference frequencies decreased. This indicated the ac component was a cosine rather than a sine function. Since this sinusoidal function was added to a dc voltage, the ac component served only to control the klystron frequency about the frequency established by the dc level. Both the sine and cosine functions vary between +B and -B, where B is the coefficient of the sinusoidal function. Therefore, addition of either a sine or cosine of the difference frequency caused the error voltage to vary between the same limits - zero and +2A, where A was the dc level at the

amplifier output when the difference frequency was not within the passband of the amplifier. Use of a variable phase shifter in one of the microwave signal paths to change the relative phase angle between the two signals applied to the mixer did not cause the klystron to be shifted out of lock except when the lock frequency was near the limit of the tracking range.

VI. AN OFFSET PHASE-LOCKED LOOP

The report thus far has been concerned with circuitry, procedure, and results related to the phase-locking of two microwave sources at exactly the same average frequency. Such a PLL does have many applications as the references indicate. An offset phase-locked loop, in which the VCO tracks the phase of the reference signal but at a fixed frequency difference, can be used in all these applications. The offset PLL is suited to FM demodulation, for heterodyne systems, and to additional applications in frequency synthesis.

BLOCK DIAGRAM OF OFFSET PHASE-LOCKED LOOP

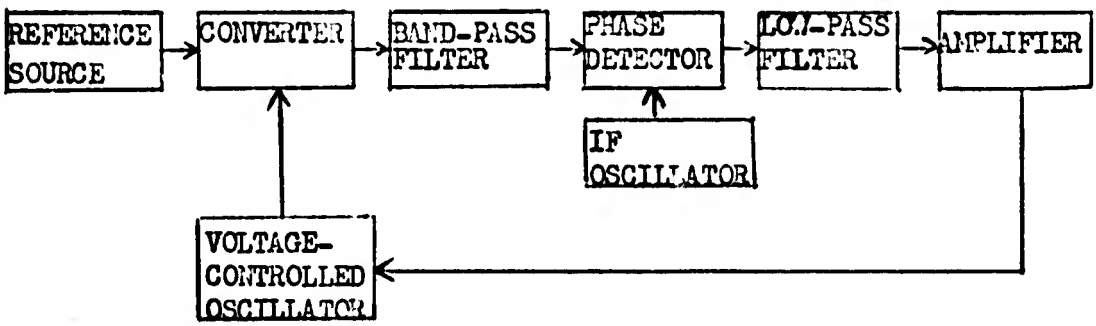


Figure 9

The offset phase-locked loop functions in the same way as the direct-frequency loop already discussed. A converter (usually a mixer) followed by a band-pass filter limits one input of the phase detector to frequencies in a small band

centered at the specified offset (intermediate) frequency. The second input is from a highly stable oscillator at the intermediate frequency. The phase detector compares the difference frequency between the reference and VCO signals to that of the IF oscillator and generates a phase-sensitive error voltage. Since the IF oscillator is essentially free of phase instability, this error voltage is related to the phase error between the VCO and reference signals. The error voltage is filtered, amplified, and used to control the VCO output, but at a frequency offset from that of the reference signal by the frequency of the IF oscillator.

It was desired that the offset phase-locked loop be capable of capture when the VCO frequency was displaced either above or below the lock frequency ($f_s \pm f_{IF}$). Thus, the error voltage had to be sensitive to both the direction of the frequency separation between the VCO signal and the lock frequency and to the phase difference between the VCO and reference signals. The sinusoidal component in the output of a non-linear mixer has this dual sensitivity, but it was considered that the outputs of both a discriminator and a non-linear mixer provided a wider tracking range than the mixer alone. The output of a discriminator is a dc voltage whose magnitude relates the amount of frequency separation between the input signal and the frequency to which the discriminator is tuned; and whose polarity reflects the direction of this frequency separation. Thus, the discriminator can hold the VCO at the same average frequency

as the reference signal, but no phase error voltage is provided. The discriminator facilitates capture since the VCO will receive a large driving voltage if the two signals are widely separated.

Use of a non-linear mixer in conjunction with the discriminator can provide the phase-sensitive error voltage. Direct summing of the mixer and discriminator outputs yields a voltage which is not symmetrical above and below the intermediate frequency since the mixer output always has a positive dc level. If this dc voltage is removed and the remaining sinusoidal voltage summed with the discriminator output, an error voltage suitable for use in controlling the VCO frequency is achieved. This combination of a discriminator and a non-linear mixer is proposed for the phase detector in an offset phase-locked loop.

PHASE DETECTOR SCHEMATIC

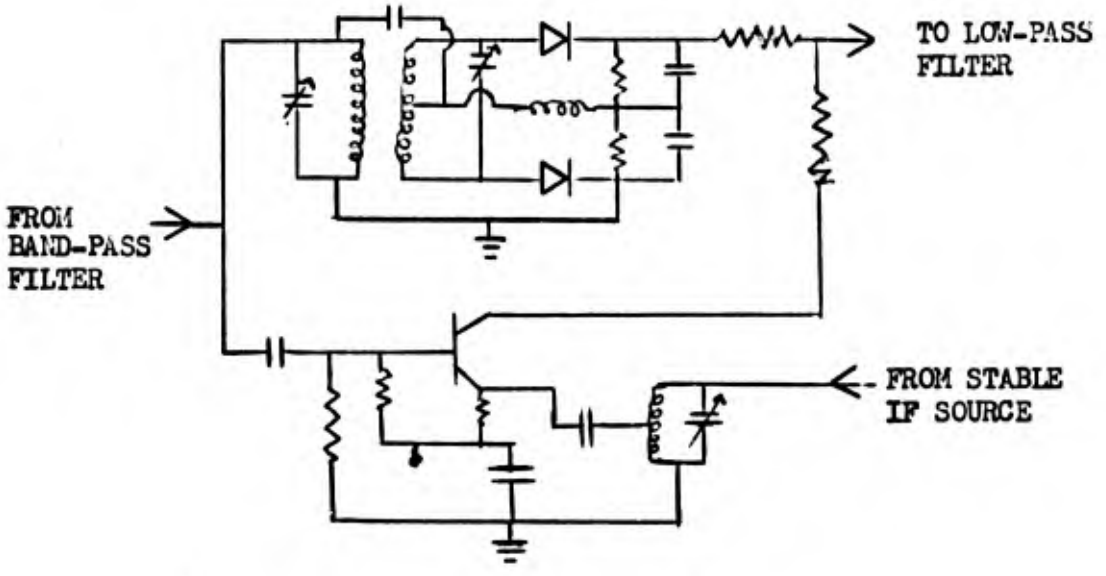


Figure 10

The upper section of Fig. 10 is a schematic of a Foster-Seeley discriminator. The output of this circuit is the "discriminator S-curve", a linearly increasing dc voltage when the input frequency is above the designed IF and a linearly decreasing dc voltage when the input frequency is below the designed IF [Ref. 7]. This circuit, or other discriminator such as a ratio detector, is used in various automatic frequency-control systems.

The lower portion of Fig. 10 is a circuit nominally designed to mix inputs at 30 and 35.5 MHZ and produce an output at the 5.5 MHZ difference frequency [Ref. 8]. This mixer was realized as shown in the reference except that a different transistor was used and the tuned circuit in the output was deleted since filtering was accomplished in the phase-locked loop. Preliminary evaluation of the mixer indicated satisfactory operation.

Use of this mixer circuit required the selection of 30 MHZ as the offset (intermediate) frequency. A vacuum-tube IF amplifier which provided band-pass filtering and sufficient gain to operate the diodes in the discriminator was available as a shelf item. However, difficulties experienced in the construction of the discriminator circuit prevented full evaluation of the proposed phase detector. These difficulties are attributed to stray capacitive and inductive effects characteristic at the 30 MHZ intermediate frequency and to problems in achieving a workable input transformer. Various attempts to construct this transformer

with tunable RF coils, with hand wound-coils on separate cores, and using a television IF-strip transformer resulted in insufficient tuning capability or narrow bandwidth due to low coupling and high Q of the coils. The final attempt used a hand-wound primary and center-tapped secondary on a single core, with the secondary winding between sections of the primary. The size 20 wire used in these windings resulted in a narrow bandwidth because of high Q, but parallel, resistive loading in the secondary compensated for this. This wire size and the choice of a one-half inch winding on a one-half inch core proved to be poor selections making the hand-winding task difficult and inaccurate. The transformer thus produced did permit realization of a discriminator, but alignment following the procedures in Ref. 7 did not result in equal positive and negative voltages as the signal applied to the discriminator was varied above and below the frequency to which the primary was tuned. More careful alignment of the discriminator and trial tuning might have resolved this lack of symmetry. Rewinding the transformer with a smaller wire (size 30) also should result in greater accuracy and easier discriminator alignment.

Stray RF energy was present in the discriminator despite the use of coaxial cable between the crystal mixer and the input transformer. The resulting unknown capacitive and inductive effects complicated discriminator alignment and might affect the summing network between this circuit and the second mixer. Closer element spacing, particularly in

the discriminator, and shorter interconnecting leads are suggested to resolve this problem.

Because of schedule requirements for thesis submission, experimental work was terminated before the suggestions for resolution of the problems experienced could be effected, and the proposed phase detector evaluated fully. Nothing in the experimental work completed caused doubt that the detector would perform as required in a phase-locked loop at a microwave frequency.

VII. SUMMARY AND CONCLUSIONS

The first part of this experimental work was related to the phase-locking of two microwave signals at the same frequency. Important insights into the components and operation of a phase-locked loop were gained from Refs. 1, 2, and 3, which are the principal information sources on which this work was based. From these sources it was determined that the error signal had to be a sinusoidal function of the phase difference between the reference and controlled signals.

A mathematical derivation proved that a non-linear mixer furnished the required sinusoidal function, but provided a dc component as well. A circuit which used a non-linear mixer (crystal diode) as the phase detector accomplished phase-locking of a reflex klystron with a microwave oscillator at a frequency of about 9.1 GHZ. Analysis of the operation of this circuit indicated that the dc component furnished by the mixer was superfluous since this voltage served only to change the center frequency of the reflex klystron oscillator. Since the signals applied to this mixer were controlled manually to approximately the same amplitude, the error voltage derived in this way had essentially equal ac and dc components. Thus, this error voltage was never negative and reflex klystron did not track through zero frequency difference and the resulting polarity shift.

The capture and tracking ranges achieved with this phase-locked loop, two and seven MHZ respectively; and the marked stabilization of the klystron frequency spectrum demonstrated an application of a phase-locked loop - that of control of a high-power signal source with a stable, low-level oscillator. Since the klystron frequency after phase-lock was accomplished was as pure, spectrally, as the signal to which the klystron was phase-locked, there was reason to believe that similar results would occur if the reference signal had a single-line spectrum.

The second part of this experimental work related to offset phase-locking, also at a microwave frequency. A block diagram of a circuit to achieve phase-locking of two microwave sources at an offset (intermediate) frequency has been discussed, with particular attention to components which were not included in the first part of this work. A two-element phase detector, consisting of a discriminator and a non-linear mixer, was proposed and its use analyzed briefly. The two elements were constructed and preliminary evaluations conducted. Suggestions for resolution of the problems experienced in realizing this phase detector are presented. Although this phase detector was not fully operational when experimental work was terminated, it is considered suitable for use in an offset phase-locked loop at a microwave frequency.

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