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VIDEO PROCESSING HARDWARE FOR USE WITH AN IMAGE DISSECTOR CAMERA

Tim C. Perry

Washington University

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An analog integrator and digital timing circuit which measure the output current from an image dissector tube and produce constant signal to noise ratios of 10, 32, or 100 (selectable) are presented. A digital circuit which produces a number proportional to the log of the dissector current is also presented.

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VIDEO PROCESSING HARDWARE FOR USE WITH AN IMAGE DISSECTOR CAMERA

1. INTRODUCTION

The problem dealt with in the following pages is the design of video processing hardware to best utilize an image dissector camera in an image processing environment. Although most of the work was done with the idea of using the results on a specific dissector camera, much of it is applicable to a wide range of photomultiplier devices.

An image dissector camera tube may be thought of as a photomultiplier tube whose output is proportional to the intensity of a small, preselected portion of the light sensitive surface. In a conventional photomultiplier tube a light sensitive surface, the photocathode, emits electrons toward a more positively charged target. The average number of electrons emitted per unit time is directly proportional to the intensity of light falling on the cathode.

In the photomultiplier tube all of the electrons leaving the photocathode are multiplied by an electron multiplier into an output signal current. In an image dissector, the electrons leaving the photocathode travel toward a positively charged plate (first anode) with a small hole or aperture in the center. Only those electrons which pass through the aperture enter the electron multiplier.

By applying a magnetic field perpendicular to the flow of electrons as they travel from the cathode to the first anode, the electron stream can be deflected allowing electrons emitted from a point somewhere other than directly in front of the aperture to pass through it. Any point on the surface of the cathode may be examined by choosing the correct magnitude and direction for the magnetic field. By examining small parts of the total image on the photocathode, the image may be "dissected" thus making the image dissector tube a useful tool in an image processing system.

The following chapters analyze the form of the output signal and propose a reasonable hardware solution to the problem of how best to get the video information from the camera into a digital computer for analysis.

Things to consider in the design of the hardware are: 1) signal to noise ratio on the video output; 2) time required to process one point; 3) ease of use by the processing system; and 4) video circuitry compatibility with the processing computer.

2. DISSECTOR OUTPUT ANALYSIS

2.1 Introduction

In this chapter we will analyze the signal and noise characteristics of the image dissector camera tube. Before mathematical relations are developed for the signal and noise, a brief discussion is presented to establish an intuitive feel for what is meant by signal and noise in this application.

Light consists of quantized packets of energy called photons. The intensity of the light is proportional to the number of photons per unit time striking the illuminated object. If the photon arrival rate were constant, the intensity of the light could be determined directly by measuring the time between two successive photon arrivals. Unfortunately things are not so simple. The photons striking the illuminated object arrive with an average rate directly proportional to the intensity, but individual arrival times are random and statistically independent.

The function of the photocathode is to convert the impinging photon into a photoelectron to be amplified by the electron multiplier into a current pulse at the output of the tube. Not only must the photons' behavior be characterized statistically, but the two conversion processes which follow (the photocathode and the electron multiplier), behave in a stochastic manner so they too must be characterized statistically.

Ideally each photon striking the photocathode would cause an electron to be emitted from the photocathode toward the electron multiplier. The photocathode does not do this consistently however, and has a conversion factor η relating the occurrence of an event at the input and the probability of the occurrence of an event at the output.

The electron multiplier is not as discriminating as the processes before it. For an input electron there will always be an associated current pulse at the output. The magnitude of this current pulse is not constant however, and it too must be characterized statistically. Since the electron multiplier does not change the relative time between pulses but only the relative size of these pulses, its effects on the overall statistics of the image dissector tube are different than those of the photon arrival distribution and the photocathode conversion process.

When all of these effects are combined, the resultant output consists of a series of current pulses of varying height whose average rate of occurrence is directly proportional to the light intensity of the photocathode. This average rate is the signal we wish to measure. The fluctuations around the average create the noise we wish to minimize. A quantitative model for the signal and noise will now be developed.

2.2 Photon Arrival Rate

Photons are emitted from a thermal source at random intervals and independently of any other photon emissions. The probability of n photons in a time interval of length τ is given by the Poisson equation (1) (2) (3)*,

*The numbers in parentheses in the text indicate references in the Bibliography.

$$P(n \mid \tau) = \frac{(\mu\tau)^n e^{-\mu\tau}}{n!} \qquad [2.1]$$

where μ is the average photon arrival rate.

The average value for n and its variance is:

$$\bar{n} = \mu\tau$$

$$\sigma^2 = \mu\tau = \bar{n}$$

Defining signal to noise ratio as:

$$S/N = \frac{\text{average}}{\text{standard deviation}} \qquad [2.2]$$

the signal to noise ratio for equation 1 becomes

$$S/N = \frac{\mu\tau}{\sqrt{\mu\tau}} = \sqrt{\mu\tau}. \qquad [2.3]$$

2.3 Photoelectron Emission

The probability that an electron will be emitted from the photocathode upon the arrival of a photon at its surface is characterized by the quantum efficiency factor η. η is a constant for incident light below a certain wavelength. This critical wavelength is dependent on the photocathode material but in the work presented here it is assumed that η is a constant within the range of the wavelengths of light being measured. (4)

Since the probability of an electron emission from the photocathode is independent of the past history of electron emissions, the photoelectrons follow the Poisson probability law just as the incoming photons do. The only difference is that the average rate has decreased by a factor of η. Therefore the probability of n events in time τ becomes:

$$p(n \mid \tau) = \frac{(\mu\eta\tau)^n e^{-\mu\eta\tau}}{n!}. \qquad [2.4]$$

The signal to noise ratio for equation 4 becomes:

$$S/N = \sqrt{\mu\eta\tau}. \qquad [2.5]$$

2.4 Electron Multiplier

For each electron entering the electron multiplier there are on average A electrons which leave it, where A is the gain of the multiplier. Reference (2) presents a summary of electron multiplier statistics. In the reference it is shown that, with good electron multiplier design, the multiplier will present relative noise free gain to the system. The paragraph summarizing the effects of an electron multiplier on the total signal to noise ratio of a photomultiplier concludes: "The

noise added to the input signal is very small. It is in this sense that the multiplication chain is said to provide noise free gain." For the remainder of this discussion we will assume that the variability in the multiplier gain introduces insignificant effects. We will examine the validity of this assumption when experimental results are presented.

2.5 Dissector Characteristics

The average pulse rate out of the dissector is equal to the product of the quantum efficiency factor for the photocathode and the average arrival rate of the photons striking the photocathode. In the following discussion we will find the range of incoming light intensities we wish to measure.

Table 1 presents the necessary image dissector specifications we will need in the following discussion.

TABLE 1

IMAGE DISSECTOR SPECIFICATIONS

Manufacturer: ITT Industrial Labs

Tube Model Number: F 4052

Photocathode Response: S11

Aperture: .0006 in. dia. round

Maximum useful photocathode diameter: 1.75 in. dia.

Average Electron Multiplier Gain: 2×10^6

Maximum Permissible Illumination: 25 foot candles

The energy of each photon striking the photocathode is given by the equation:

$$E = \frac{hc}{\lambda}$$

where:

$h = 6.63 \times 10^{-34}$ joule seconds
λ = wavelength in meters
$c = 3 \times 10^8$ m/sec.

Evaluating the equation above we get:

$$\text{Energy in one photon} = E = \frac{6.6 \times 10^{-34} \times 3 \times 10^{8}}{\lambda} ,$$

$$E = \frac{1.99 \times 10^{-25}}{\lambda} \text{ joules/photon} , \qquad [2.6]$$

$$1 \text{ lumen} = 1.5 \times 10^{-3} \text{ watts} ,$$

$$= 1.5 \times 10^{-3} \text{ joules/sec} .$$

Combining this with equation [2.6] we get the number of photons per second corresponding to a light flux of one lumen at a wavelength of 5600Å.

$$\frac{(1.5 \times 10^{-3})(5.6 \times 10^{-7})}{1.99 \times 10^{-25}} = 4.2 \times 10^{15} \frac{\text{photons}}{\text{sec. lumen}}$$

The manufacturer specifies the maximum light intensity which will not damage the tube to be 25 foot candles. The relation between foot candles and lumens is:

$$1 \text{ foot candle} = \frac{1 \text{ lumen}}{\text{ft.}^2} .$$

The average photon current density at 25 foot candles and 5600Å is therefore:

$$\frac{25 \text{ ft. cndl.}}{144 \text{ in.}^2} \times 4.2 \times 10^{15} \frac{\text{photons}}{\text{sec. lumen}} = 7.3 \times 10^{14} \frac{\text{photons}}{\text{sec. in.}^2} .$$

Reference (4) shows the quantum efficiency of an S11 photocathode is approximately 0.1 below a wavelength of approximately 6000Å. Therefore the average current density leaving the photocathode is:

$$(0.1)(7.3 \times 10^{14}) = 7.3 \times 10^{13} \text{ electrons/sec. in.}^2 .$$

These electrons pass through an accelerating mesh and then continue toward a positively charged plate with the aperture at its center. The dissector manufacturer (ITT) estimates the mesh transmission factor to be between 50% and 60%. The electrons which pass through the mesh and finally the aperture are then multiplied by the electron multiplier. Using the aperture diameter of 0.6 mils, a mesh transmission factor of 55%, and the electron current density given above, the number of electrons per second entering the electron multiplier is:

$$[(7.3 \times 10^{13})(\frac{6 \times 10^{-4}}{2})^2 \pi] \, 0.55 = 11.3 \times 10^{6} \text{ elec./sec.} \qquad [2.7]$$

The electron multiplier will change the charge associated with each of these pulses but it will not affect their time relationship. Therefore the maximum average pulse rate coming out of the dissector is the pulse rate given by equation [2.7]. Using the electron multiplier figure of 2×10^6, the maximum average output current becomes approximately 3.6 micro amps.

The upper limit has been imposed by the limitations of the dissector tube. The lower limit is not as well defined and is imposed for the most part by the circuitry used to measure the average current or pulse rate for very low light intensities.

3. PROCESSING TECHNIQUES AND REQUIREMENTS

3.1 Introduction

In chapter 2 we characterized the output current of the dissector. In this chapter different ways of detecting or processing the output will be investigated. Three major catagories are discussed:

1) Placing a low pass filter on the output of the tube and measuring the voltage from the filter;
2) Pulse counting; and
3) Integration.

After these methods are discussed one is chosen which best suits the needs of the environment in which the camera is to be used.

3.2 Processing Techniques

3.2.1 Low Pass Filter

In chapter 2 the current pulses from the output of the dissector were shown to be randomly distributed in time and statistically characterized by the Poisson equation. The average pulse rate per unit time interval is:

$$\text{average output pulse rate} = \mu\eta \ .$$

If a low pass filter were placed on the output of the dissector it would tend to filter out the high frequency components (noise) and leave a signal proportional only to the average pulse rate. The lower the cutoff frequency of the filter the closer the output would represent only the average pulse rate. The effectiveness of a low pass filter on the output may be evaluated analytically with the aid of Campbell's Theorem. (1) This theorem may be used to find the mean and variance of a filtered Poisson process. If w(t) is the impulse response of the filter and μ is the average of the Poisson process $x_1(t)$, then Campbell's Theorem states that the expected value and variance of the output $x_2(t)$ of the filter will be:

$$E\{X_2(t)\} = \mu \int_{-\infty}^{\infty} w(t)\, dt$$

$$Var\{X_2(t)\} = \mu \int_{-\infty}^{\infty} w^2(t)\, dt \ .$$

As an example of Campbell's Theorem applied to the image dissector, let the filter be a simple RC low pass network with a time constant τ. We will assume that the output pulse width of the dissector is small relative to τ. The impulse response of the RC filter is:

$$h(t) = \frac{1}{\tau} e^{-t/\tau} \qquad 0 \leq t \leq \infty \qquad [3.1]$$

We showed in Chapter 2 that the average pulse rate at the camera output was $\mu\eta$ where μ is the photon average arrival rate and η is the quantum efficiency of the photocathode. Using these facts with Campbell's Theorem we get:

$$E\left\{X_2(t)\right\} = \frac{\mu\eta}{\tau} \int_0^\infty e^{-t/\tau}\, dt = \mu\eta \qquad [3.2a]$$

$$Var\left\{X_2(t)\right\} = \frac{\mu\eta}{\tau^2} \int_0^\infty e^{-2t/\tau}\, dt = \frac{\mu\eta}{2\tau} . \qquad [3.2b]$$

Defining signal to noise ratio as in equation [2.2] we get the signal to noise ratio for this filtered Poisson process:

$$S/N = \frac{\mu\eta}{\sqrt{\frac{\mu\eta}{2\tau}}} = \sqrt{2\tau\mu\eta} . \qquad [3.3]$$

This technique of filtering the camera output and sampling the voltage from the filter is easy to implement in an image processing system. One drawback of this scheme which is not immediately obvious is a settling time proportional to τ which must be allowed when the dissector is directed at a point of new intensity.

3.2.2 Pulse Counting

Since the desired signal is directly proportional to the average pulse rate at the output, a theoretically simple way of determining this average is to count the number of pulses that occur in a given time period. Intuitively we see that for longer time periods we will count more pulses and our measured average will come closer to being the true average of the Poisson process.

Repeated trials of this technique will produce varying results since we can only approximate the average on each try. The fluctuations in the results represent the noise in the system and the magnitude of the fluctuations will be inversely proportional to the period over which the pulses are counted.

Equation [2.4] gives the distribution of the number of pulses which occur in a fixed time. The signal to noise ratio for this process is given by equation [3.4] .

$$S/N = \sqrt{\mu\eta\tau} \qquad [3.4]$$

τ in this case is the period over which the pulses are counted.

It is seen from equation [3.4] that the signal to noise ratio is dependent on the average pulse rate. Thus the signal to noise ratio will be greater for high light intensities. In many applications a non constant signal to noise ratio is inconvenient.

A constant signal to noise ratio may be obtained by measuring the length of time required for a fixed number of pulses to occur. The distribution of the time t required to count N pulses is given by the Erlangian distribution, (5)

$$p(t \mid N) = \frac{\mu\eta(\mu\eta t)^{N-1} e^{-\mu\eta t}}{(N-1)!} \qquad [3.5]$$

The mean and variance for this distribution are:

$$t = \frac{N}{\mu\eta} \qquad [3.6a]$$

$$\sigma^2 = \frac{N}{(\mu\eta)^2} \quad . \qquad [3.6b]$$

Using equations [3.6a] and [3.6b] the signal to noise ratio associated with equation [3.5] is given by equation [3.7].

$$S/N = \frac{\frac{N}{\mu\eta}}{\sqrt{\frac{N}{(\mu\eta)^2}}} = \sqrt{N} \qquad [3.7]$$

Equation [3.7] indicates that the signal to noise ratio is not a function of average pulse rate when we measure the length of time required to count N pulses.

3.2.3 Integration

If instead of counting the current pulses we integrate them with respect to time, the output voltage of the integrator would be directly proportional to the number of pulses which have occurred since the integration was begun.

The equations representing the process are the same as the ones for pulse counting. This is merely an alternative to actually counting individual pulses.

3.3 Processing Technique Selection

The signal to noise ratio equations given in this chapter for various processing techniques can be divided into two categories: 1) those yielding a non constant signal to noise ratio, and 2) those yielding a constant one. There are obvious advantages to a constant signal to noise ratio so only the second category will be given any further consideration. This leaves us with pulse counting a fixed number of pulses or ntegrating the dissector current to a fixed voltage.

From a practical point of view the pulse counting technique is preferable over the integration method for small average pulse rates. As the average pulse rate increases, the pulses

become closer together making it more difficult to resolve and count individual pulses. At the same time the average current rises, making it easier to integrate the current. Thus for high pulse rates and currents it is easier to integrate than count the pulses.

We found the maximum average pulse rate to be 11.3 x 10^6 pulses per second as shown in equation [2.7]. Using this figure we may get some idea of the required resolving time of a pulse counting circuit designed to count a series of pulses whose average rate is that given above. From equation [2.4] we can find the probability of no pulses occurring in time τ to be:

$$p(0 \mid \tau) = e^{-\mu\eta\tau} \qquad [3.8]$$

If we wish to know with a 99% likelihood that there will be no pulses in a time interval of length τ we can set equation [3.8] equal to 0.99 and solve for τ. Doing this yields a value for τ of approximately 900 pico seconds.

The design of a counter which could detect and distinguish between pulses separated by no greater than 900 pico seconds would be extremely difficult if not impossible with today's technology. For this reason the current integration scheme has been chosen as the technique best suited for the job. The detailed design of the integrator curcuit is presented in the next chapter.

4. METHODS OF ANALOG INTEGRATION

4.1 Introduction

As is the case for most engineering design problems, the solution to the problem at hand may be reached in a variety of ways and with various degrees of perfection. In this chapter we will investigate several methods of analog integration and breifly discuss pros and cons of each.

4.2 Ideal Integrator

Theoretically the simplest and the best current integrator is a capacitance, since the voltage across a capacitance is the time integral of the current into it. In this and the following sections an equation as a function of time will be given for a step of current at t = 0 with magnitude I_{in}. Figure 1 illustrates the ideal integrator and gives its output equation.

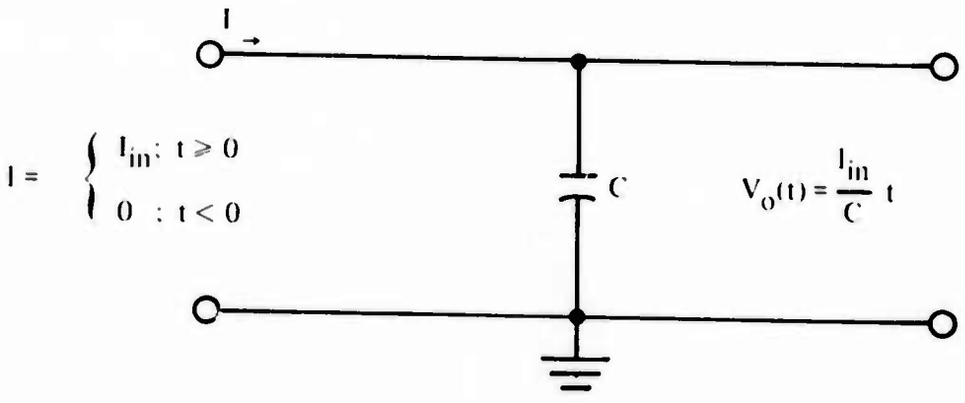


Figure 1: Perfect Integrator

It is not possible to measure V_o without imposing some finite impedance on the output. This impedance changes the current-voltage transfer characteristics and makes the circuit something less than an ideal integrator.

4.3 R-C Network As An Integrator

If we represent the input impedance of the circuit used to measure the voltage across the capacitor as a resistance and capacitance in parallel with the integrating capacitor, the equivalent circuit is an R-C network with R being the input resistance of the measuring device and C being the parallel combination of the integrating capacitor and the input capacitance of the measuring device.

Figure 2 shows the equivalent circuit and the step response for the R-C network.

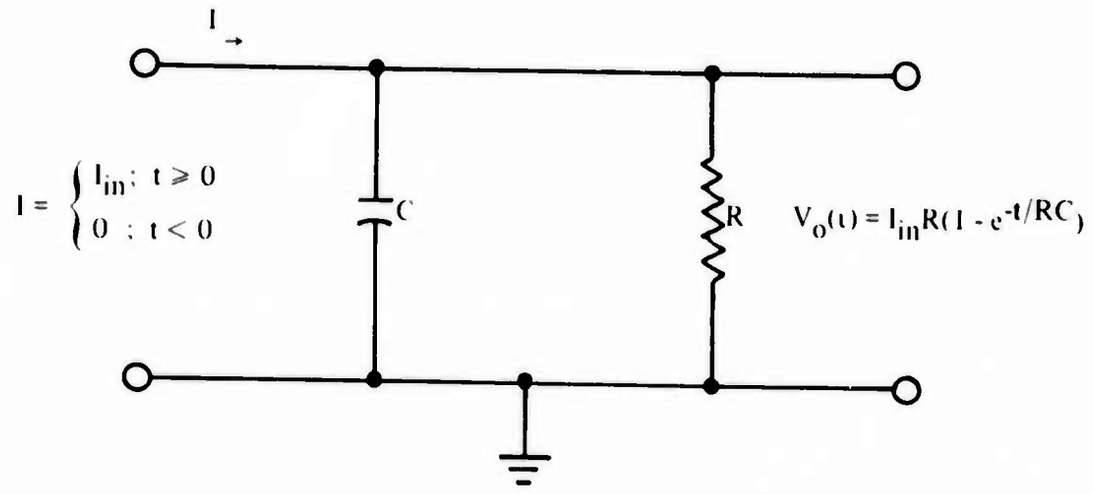


Figure 2: R-C Network as an Integrator

The voltage output equation given in figure 2 may be made to look like the one for the ideal integrator if the exponential term is written in a power series and a t/RC is factored out. When this is done equation [4.1] results.

$$V_o(t) = \frac{I_{in}}{C} t\left[1 - \frac{1}{2!}\left(\frac{t}{RC}\right) + \frac{1}{3!}\left(\frac{t}{RC}\right)^2 - \ldots\right]$$

$$= \frac{I_{in}}{C} t + \epsilon \qquad [4.1]$$

ϵ is an error term and goes to zero as R goes to infinity. Referring back to figure 1 equation [4.1] is the same as the step response for the ideal integrator except for the error term.

4.4 Integrator Using An Operational Amplifier

If we wish to amplify or buffer the voltage across the integrating capacitor, then all the nonideal characteristics of the amplifier used must be considered. There are two basic circuit configurations for current integration using operational amplifiers as shown in figure 3.

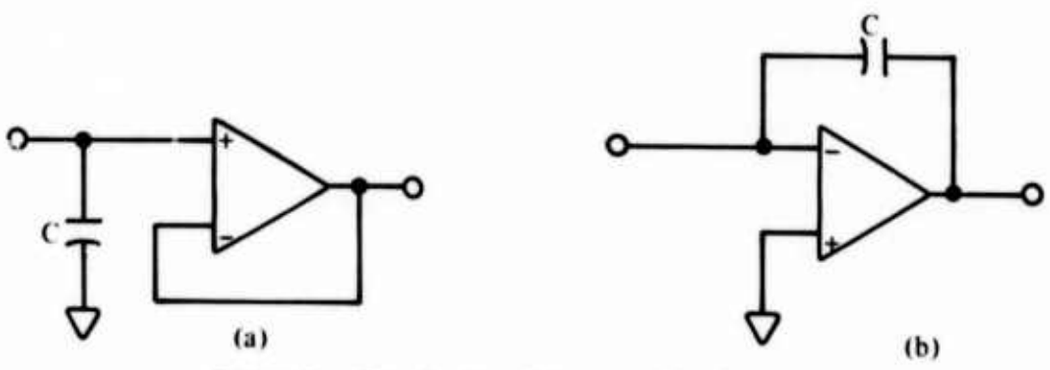


Figure 3: Two Op Amp Integrator Configurations

In the circuit of figure 3-b the input voltage to the operational amplifier is held at virtual ground. In figure 3-a the input voltage follows the voltage across the capacitor. If the input voltage is held at ground (as in figure 3-b) then no current will flow through any resistance which appears at the input. If the input voltage is allowed to deviate from zero (as in figure 3-a) some of the input current will be lost through the input resistance. For this reason the circuit shown in figure 3-b was chosen for further anlaysis.

If an ideal amplifier with infinite gain, zero offset current and zero offset voltage were used in the configuration of figure 3-b, the input voltage would always be held at zero and the input resistance of the circuit would have no effect. If an ideal amplifier with finite gain were used, then the equivalent circuit of the integrator would be the same as figure 2 with the exception that the effective resistance would be equal to the input resistance multiplied by the gain of the amplifier. Thus an ideal amplifier with finite gain would serve to decrease the effects of the input resistance and also buffer the output voltage.

In order to derive the transfer characteristics of an integrator using a nonideal operational amplifier, an equivalent circuit which includes all of its significant non idealities must be developed. Such an equivalent circuit is shown in figure 4.

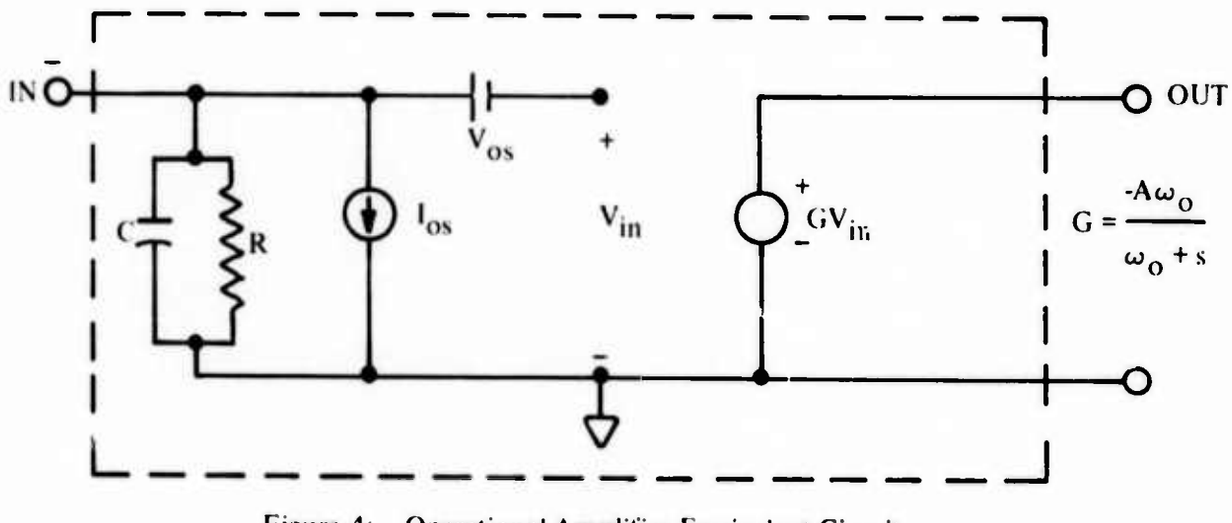


Figure 4: Operational Amplifier Equivalent Circuit

The equivalent circuit used includes. (1) parallel R-C input impedance, (2) offset current I_{os}; (3) offset voltage V_{os}; (4) finite DC gain A; and (5) single pole transfer characteristic with 3 db break point at ω_o.

The equivalent circuit of the signal source feeding the input may be represented by a current source in parallel with a capacitor and resistor.

In deriving the transfer characteristics of figure 3-b a number of simplifying assumptions and substitutions were made. These were: (1) total capacitance at the amplifier input to ground is equal to C_1 ,this is the parallel capacitance of the internal input capacitance of the amplifier and all the

external capacitances connected to the input); (2) C_2, the feedback capacitor has infinite DC resistance; (3) D is defined to be equal to $1 + C_1/C_2$; (4) total input resistance seen at the amplifier input to ground is equal to R_1; (5) ω_1 is defined to be equal to $1/R_1C_2$; (6) I_{eq} is defined to be the equivalent input current equal to the actual signal source output plus the offset current; and (7) the output impedance of the amplifier introduces negligible effects and may be ignored. The simplified model is summarized in figure 5.

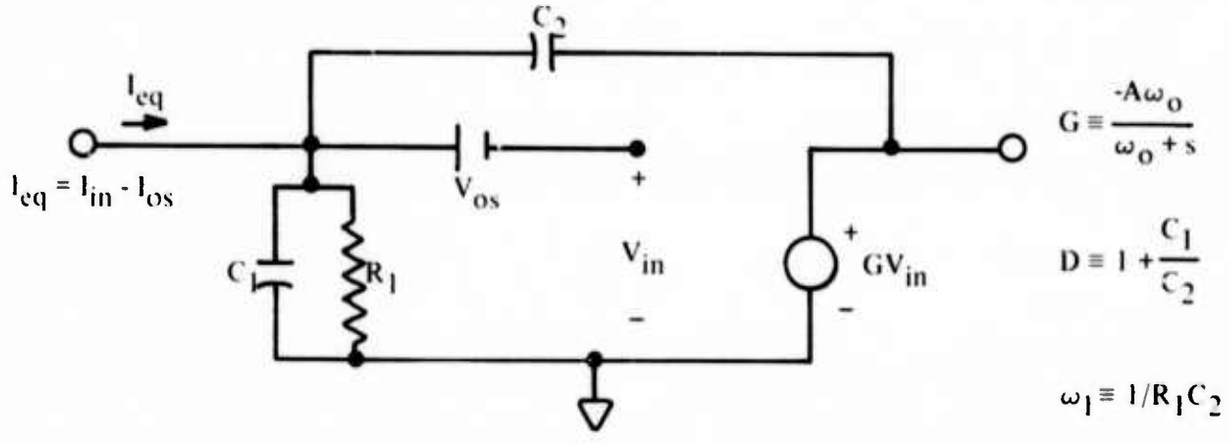


Figure 5: Equivalent Circuit of Op Amp Integrator

The results presented below were obtained through straightforward Laplace Transform techniques applied to the circuit of figure 5.

The signal current was assumed to be a step of current of magnitude I_{in} at $t = 0$. This assumption was made for two reasons. First, the presentation and understanding of the results is simplified by this assumption. Secondly, the shot noise process used to model the dissector output current has a power density spectrum with an impulse at zero frequency and a constant level for essentially all other frequencies up to the cutoff imposed by the dissector. (6) The magnitude of the impulse is the information we wish to obtain.

If no simplifying assumptions are applied to the circuit of figure 5 the resultant output equation is very cumbersome and hard to understand. If the assumption that the magnitude of the DC gain of the amplifier is much greater than two times D as defined in figure 5 such that $1 + A/2D$ may be approximated as $A/2D$ then a significant reduction in the complexity of the output equation can be made. C_1 of figure 5 serves no useful purpose and in any practical circuit would be the stray capacitances applied to the input of the amplifier. For this reason D will be small and the assumption is reasonable.

With the assumption stated above, the output voltage equation for the circuit of figure 5 with an input step of current of magnitude I_{in} applied at $t = 0$ is given by equation [4.2].

$$V_o(t) = \frac{A\omega_o}{(A\omega_o + \omega_1)} \left\{ \left(\frac{V_{os}}{R_1} - I_{eq} \right) \frac{t}{C_2} - D \left[\frac{(V_{os}/R_1 - I_{eq})}{C_2(A\omega_o + \omega_1)} - V_{os} \right] (1 - e^{-at}) \right\} \qquad [4.2]$$

$$a = \frac{1}{D}(A\omega_o + \omega_1)$$

In analyzing equation [4.2], it is helpful to consider an effective current I_{eff} as defined by equation [4.3].

$$I_{eff} \equiv \left(\frac{A\omega_o}{A\omega_o + \omega_1} \right) \left(\frac{V_{os}}{R_1} - I_{eq} \right) \qquad [4.3]$$

Equation [4.2] is valid within the constraints of the assumptions presented and provided the amplifier behaves in a linear manner. The amplifier will remain linear as long as the instantaneous value of I_{eff}/C_2 does not exceed the maximum slew rate of the amplifier. It should be remembered that the maximum dissector current of 3.6 micro amperes which was determined in chapter 3 is an average. This current consists of pulses whose amplitudes may be many times greater than the average.

If the amplitude of an individual pulse is greater than the product of the feedback capacitance and the amplifier's maximum slew rate then the output voltage of the amplifier will not be able to change fast enough to keep the differential voltage at zero. If the input current to the amplifier remains at zero when the voltage deviates from zero then none of the charge in the pulse will be lost through the amplifier. In this case the change in voltage across the feedback capacitor will be directly proportional to the amount of charge in the pulse but since the rate of change in the output voltage is limited by the slew rate, the input side of the capacitor will rise above zero until the output voltage has time to rise to the correct value and allow the input to return to zero.

The output pulse height of the image dissector is difficult to determine and the way in which an operational amplifier behaves when it is over driven is seldom given in specification sheets. If there were significant degradation in the output voltage when the amplifier was overdriven, it would show up when small values of feedback capacitance are used, since the value of I_{eff}/C_2 is greatest at that time. After an amplifier and feedback capacitor have been chosen, an experiment may be performed using the dissector to drive the integrator first with the chosen value of capacitance and then with one much larger. If the difference in output voltage is related only to the size of the feedback capacitors it may be assumed that no charge is lost due to non linearities of the amplifier for the values of capacitance chosen.

Up to this point the ability of a circuit to perform as an integrator has been examined by comparing its output equation with the equation for an ideal integrator given by the equation in figure 1. To facilitate such a comparison for the op amp integrator, equation [4.2] may be rewritten as shown by equation [4.4] taking advantage of the definition given in equation [4.3].

$$V_o(t) = \frac{I_{eff}}{C_2} t - V_{eff}(1 - e^{-at}) \qquad [4.4]$$

The left half of equation [4.4] is similar to the equation for an ideal integrator given in figure 1, the only difference being that the effective current integrated has been decreased (or increased depending on the signs of V_{os} and I_{os}) from the true current entering the integrator. The right half of equation [4.4] is an error term which exponentially approaches the magnitude of V_{eff}.

It is both interesting and significant to note the transfer characteristics of the integrator are improved in all cases by increasing the value of R_1, the input resistance of the integrator. It is therefore obviously important in a practical integrator circuit to keep the input resistance as high as possible.

In order to more closely examine the effects of the errors implied in equations [4.2] and [4.4], equation [4.2] may be rewritten to form equation [4.5].

$$V_o(t) = \frac{I_{eff}}{C_2}\left[t - \left(\frac{1}{a} - \frac{C_2 V_{os}}{I_{eff}}\right)(1 - e^{-at})\right] \qquad [4.5]$$

In this form it becomes more obvious that the effect of the exponential and the terms multiplying it is to delay the integrator ramp. After the exponential has died out, the remaining term of the error is no longer a function of time and this then becomes a fixed offset to the linear function of time.

Figure 6 is a graph of the left and right halves enclosed in the brackets of equation [4.5]. The left term is represented by long dashes, the right term by short dashes, and their sum by the solid line.

The delay time, τ_d, which is the difference between the solid line and the long dashed line for equal voltages after the exponential has died out is given by equation [4.6].

$$\tau_d = \frac{1}{a} - \frac{C_2 V_{os}}{I_{eff}} \qquad [4.6]$$

Digressing for a moment we recall from chapter 3 that we wish to use the integrator to integrate the output current from an image dissector tube and measure the time required for the output voltage to reach a reference level. If we were to use an integrator with a step response of the form of equation [4.5] and begin the time measurement as soon as the integration is begun, the time measured would be increased due to the delay in the beginning of the ramp.

If the integration was begun and the exponential allowed to die out before the time measurement was begun, the time measured for the output voltage to rise an additional amount equal to the reference voltage would be the true time we wished to measure. (Except for the fact that I_{eff} differs from the signal current as discussed before.)

Using this information chapter 5 will develop a useful integrator circuit.

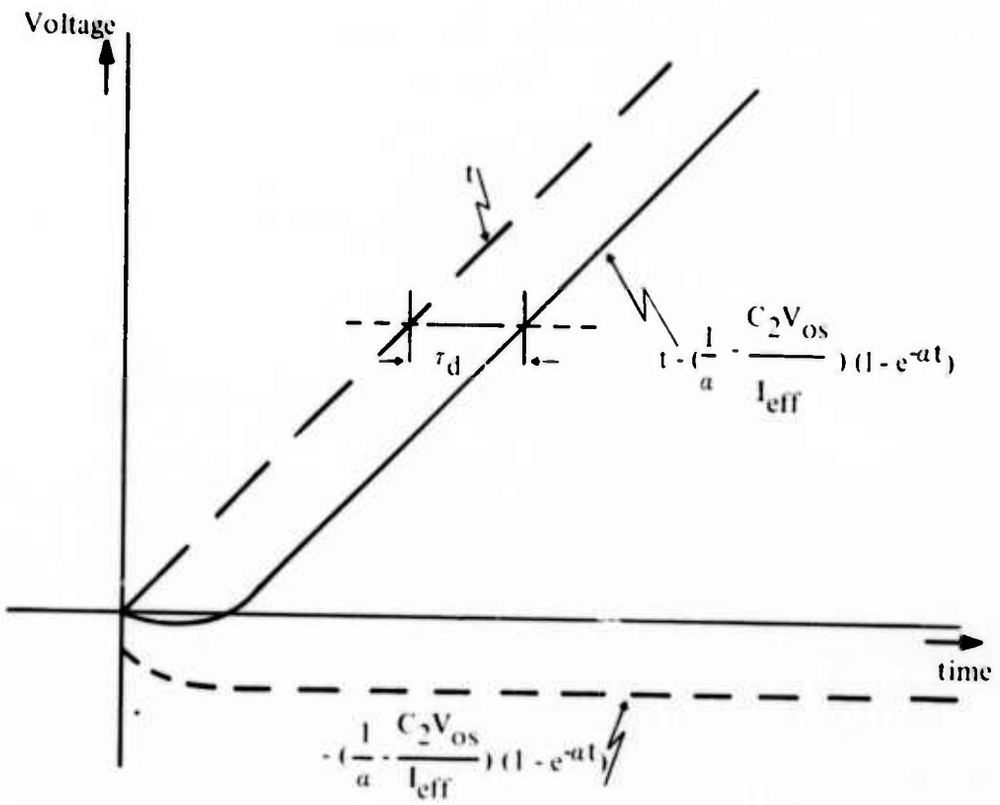


Figure 6: Graph of Equation [4.5]

5. CIRCUIT DETAILS FOR INTEGRATION SCHEME

5.1 Introduction

This chapter presents details of a circuit designed to implement the current integration scheme discussed in chapter 3. Figure 7 gives a black box representation of the circuit discussed in this chapter.

The basic function of the circuitry as a whole is to measure the length of time required to integrate the input current to a predetermined level. The time is measured by counting the output of a crystal oscillator during the period of integration. The number in the counter when the integration is completed is then inversely proportional to the average current into the integrator during the period of integration.

The implementation includes both analog and digital circuitry and details of each will be considered individually.

5.2 Analog Circuitry

The integration in the circuitry described here is achieved using the op amp integrator configuration presented and analyzed in Chapter 4. Other circuitry required is an analog comparator to determine when the integration is completed and some means to discharge the capacitor when completion occurs. A schematic of the circuit described here is given in figure 10 at the end of this section.

Before we may proceed further, the output signal to noise ratio we wish to achieve must be determined. Equation [3.7] indicates that the signal to noise ratio for this process is equal to the square root of the number of current pulses counted or integrated. A greater signal to noise ratio means more pulses, which in turn means a longer integration period.

There is an obvious tradeoff between speed and signal to noise ratio. Examining the conditions under which the dissector will be used indicates that a high signal to noise ratio is desirable for some purposes but a sacrifice in signal to noise ratio for the sake of speed seems desirable in others. It therefore seems reasonable to offer the user a choice. Signal to noise ratios of 10, 32, and 100 were selected as reasonable values for implementation with the circuit described.

5.2.1 Integrator

The integrator circuit analysis presented in chapter 4 will be used in this section to analyze the performance of a specific operational amplifier in the integrator configuration. Before this is done however we will determine values for the feedback capacitors and the reference voltage.

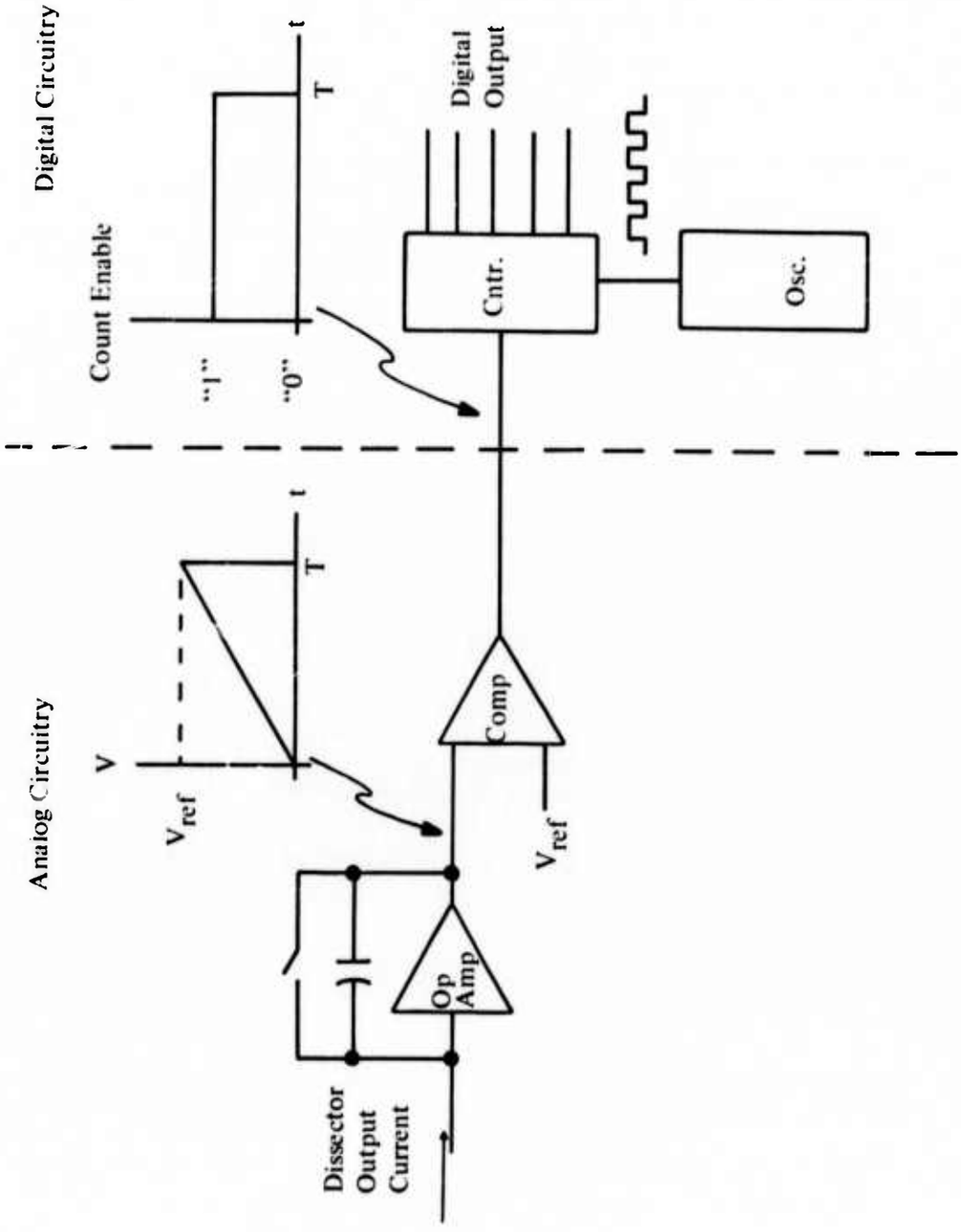


Figure 7: Current Integration Scheme

We have not yet said anything about the value of C_2 or the maximum V_o (the reference voltage V_{ref}). The amount of charge we want to integrate is dependent on the desired signal to noise ratio. From equation [3.7] we know that the necessary number of pulses we must integrate is equal to the square of the desired signal to noise ratio. We also know that each current pulse contains about 2×10^6 electrons since the pulse is the result of an electron entering the electron multiplier whose gain is 2×10^6.

The equation relating charge, voltage, and capacitance of a capacitor is

$$C = \frac{Q}{V} \quad \text{or} \quad Q = CV,$$

and in our case:

$$CV = Q = (S/N)^2 \times \frac{2 \times 10^6 \text{ elec/pulse}}{6.25 \times 10^{18} \text{ elec/coul}}$$

$$CV = (S/N)^2 \times 3.2 \times 10^{-13}. \qquad [5.1]$$

Thus the product of the capacitance and the reference voltage is fixed by the signal to noise ratio. Table 2 gives values of capacitance for various signal to noise ratios and reference voltages.

Switching from one signal to noise ratio to another could be achieved by either changing V_{ref} or C_2 or both. Implementation seems intuitively easier if one is changed and the other remains constant. Therefore, for a change in signal to noise ratio by a factor of 10 (10 to 100), either the capacitor or the reference voltage would have to vary by a factor of 100.

As shown in figure 7, the output voltage of the integrator is compared against V_{ref} to determine when V_o reaches its upper limit and to stop the integration. Any practical comparator will have some window of uncertainty when it can not determine which of the two is greater. The smaller the uncertainty relative to V_{ref} the greater the precision of the comparison. For this reason we wish to make V_{ref} large.

TABLE 2

CAPACITANCE AND REFERENCE VOLTAGE VALUES FOR VARIOUS SIGNAL TO NOISE RATIOS

S/N	V_{ref}	C_2
100	1.5	2100 pf
100	5.0	640 pf
32	1.5	210 pf
32	5.0	64 pf
10	1.5	21 pf
10	5.0	6.4 pf
10	1.0	32 pf

A practical upper limit for V_{ref} is 15 volts since this is the upper power supply voltage for most common operational amplifiers and a voltage higher than that would necessitate an additional voltage source. Also, 15 volts is in the range of the maximum differential input voltage specified for most practical comparators. If we were to vary V_{ref} to achieve the desired variations in signal to noise ratio, V_{ref} for a signal to noise ratio of 10 could then be no greater than 0.15 volts. At this level the window of uncertainty becomes a significant part of the comparison voltage. For this reason V_{ref} was fixed at a level as high as possible.

Once it is determined to fix V_{ref}, the only alternative left is to vary the feedback capacitance. Practically speaking, a lower limit on the capacitance is imposed by stray capacitances on the circuit board containing the integrator. It is therefore desirable to keep C_2 large enough that the stray capacitances do not dominate in order to have control of the total feedback capacitance.

As a compromise between large V_{ref} and large C_2, a value of 1.5 volts was chosen for V_{ref} and values of 21, 210, and 2100 pico farads were chosen for C_2 for signal to noise ratios of 10, 32, and 100 respectively. (These values are included in Table 2.)

At this point we may proceed to the selection of an operational amplifier. We will present an amplifier and examine its characteristics to show that it is suitable for the job.

The amplifier selected is an Analog Devices Incorporated 40K FET input operational amplifier. Figure 8 is a copy of an Analog Devices specification sheet for the 40K.

The single most important requirement for the amplifier is a very high input impedance and consequently a low leakage current. This requirement was discussed in chapter 4 and led to the selection of an FET op amp. The input resistance is specified to be of the order of 10^{11} ohms. 10^{11} ohms in parallel with the dissector output resistance of the same order of magnitude yields a total input resistance for the circuit of the order of 10^{10} ohms.

In equation [4.2], the term $(V_{os}/R_1 - I_{eq})$ appears twice. From the 40K specification sheet we see the initial offset voltage with a fixed 500 ohms trim resistor is ±2mV. Temperature variation adds little to this value. Using these values for R_1 and V_{os} the term V_{os}/R_1 is of the order of 10^{-13} amps. Therefore, for all practical purposes the term V_{os}/R_1 may be ignored relative to I_{eq}.

ω_1 only appears in equation [4.2] when it is summed with $A\omega_o$. $A\omega_o$ may be found from figure 8 labeled "small signal, unity gain". The value given is 4×10^6. ω_1 was defined to be $1/R_1C_2$. The smallest value of C_2 which would consequently yield the largest value of ω_1 is 21×10^{-12} farads. Using this value for C_2 and 10^{10} for R_1 gives a value of 4.8 for ω_1. Clearly ω_1 is negligible relative to $A\omega_o$ and the term $(A\omega_o + \omega_1)$ may be approximated as $A\omega_o$.

The term $(1 + C_1/C_2)$ which we called D in equation [4.2] has its greatest effect when it is large. We therefore would like to put an upper bound on it. C_2 will be the smallest when the value of 21 pico farads is used. C_1 is a function largely of the stray capacitances on the board plus the capacitance of the line between the dissector and the integrator. Using the value of 50 pico farads as a reasonable value for illustration, D becomes

$$D = (1 + C_1/C_2) = 1 + \frac{50}{21} \simeq 3.4.$$

MODEL 40J/K GENERAL PURPOSE LOW COST FET OP AMP

SPECIFICATIONS (typical @ 25°C and ±15VDC unless otherwise noted)*

MODEL	40J	40K
OPEN LOOP GAIN		
dc rated load, min	5×10^4	•
dc 10k load	2×10^5	•
RATED OUTPUT		
Voltage, min	±10V	•
Current, min	±5mA	•
Load capacitance range	0.005µF	•
FREQUENCY RESPONSE		
Unity gain, small signal	4MHz	•
Full power response, min	100kHz	•
Slewing rate, min	6V/µsec	•
Overload recovery	4µsec	•
INPUT OFFSET VOLTAGE		
External trim pot	1kΩ[1]	•
Initial offset, 25°C	±2mV(500Ωtrim)	•
Avg. vs. temp (+10° to +60°C) max	±50µV/°C[3]	±20µV/°C
vs. supply voltage	±50µV/%	•
vs. time	±250µV/month	•
INPUT BIAS CURRENT		
Input bias, 25°C, max	(0,-) 50pA	(0,-) 20pA
Avg. vs. temp	doubles every +10°C	•
vs. supply voltage	±1 pA/%	•
INPUT DIFFERENCE CURRENT		
Initial difference, 25°C	±25pA	±10pA
Avg. vs. temp	doubles every +10°C	•
INPUT IMPEDANCE		
Differential	$10^{11}\Omega \parallel 3.5$pF	•
Common mode	$10^{11}\Omega \parallel 3.5$pF	•
INPUT NOISE		
Voltage, 0.01 to 1Hz, p-p	6µV	•
5 to 50kHz, rms	3µV	•
Current, 0.01 to 1Hz, p-p	0.1pA	•
INPUT VOLTAGE RANGE		
Common mode voltage, min[2] (1% error)	+8, -10V	•
Common mode rejection[2] @ +8, -10V	80dB	•
Max. safe differential voltage	±15V	•
POWER SUPPLY		
Voltage, rated specification	±15V	•
Voltage, derated specification	±(12 to 18)V	•
Current, quiescent	5.5mA	•
TEMPERATURE RANGE		
Rated performance	0 to +70°C	•
Operating	-25° to +85°C	•
Storage	-55° to +125°C	•
MECHANICAL		
Case style - pin configuration	M-2	•
Mating socket	AC 1003	•
Weight	0.52 oz.	•
PRICE		
1-9	$12.00	$19.00
10-24	$11.80	$17.10

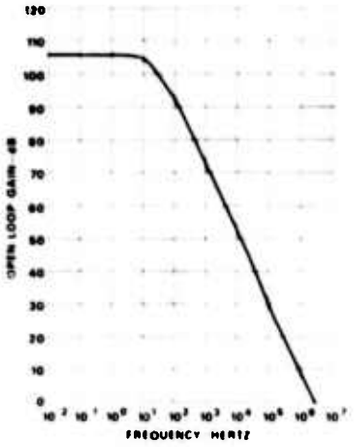
*Specifications same as for Model 40J

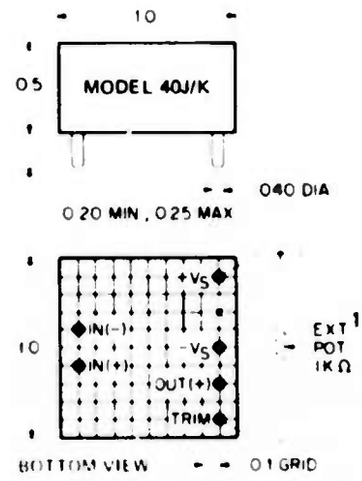
1 Analog Devices part no. 79PR 1K $3.00 (1-9)

2 CMRR of 74dB min @ ±10V, specify model 40JV, $3.00 additional (1-24)

3 Same specification available -25°C to +85°C. Consult factory or your nearest Analog representative about Model 40A.

Specifications subject to change without notice.





*Note Common supply connection not necessary within the amplifier

[1] External variable resistor is used to zero the amplifier. Fixed 500 ohm resistor gives nominal zero (±2 mV). If no resistor desired connect TRIM to +VS. If TRIM left open, unit operates, but with considerable offset.

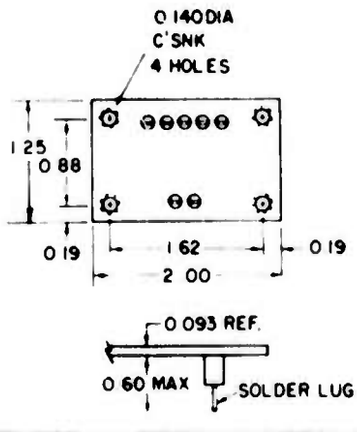


Figure 8: Analog Devices 40K Specification Sheet

Remembering that the output of an ideal integrator is characterized by the equation in figure 1 of chapter 4, we wish to substitute into equation [4.2] the nonideal characteristics of the amplifier as given by the specification sheet and compare the resulting equation to the ideal one.

Both I_{os} and V_{os} are functions of temperature. Using 55°C as a reasonable upper limit to the ambient temperature, I_{os} and V_{os} become 80 pico amps and 2.4 milli volts respectively. (This value of offset voltage is obtained when a fixed 500 ohm resistor is used as the offset voltage trim.) Using the Values of D, I_{os} and V_{os} as found here plus the value of 4×10^6 for $A\omega_o$ and ignoring the ω_1 and V_{os}/R_1 terms, we may write equation [5.2] from equation [4.2].

$$V_o(t) = -(I_{in} + 8 \times 10^{-11})\frac{t}{C_2} + [8.5 \times 10^{-7} \frac{(I_{in} + 8 \times 10^{-11})}{C_2} + 8.2 \times 10^{-3}](1 - e^{-1.2 \times 10^6 t}) \qquad [5.2]$$

The offset current is insignificant relative to any reasonable input current and can therefore be ignored. The part multiplying the exponential of equation [5.2] will have its greatest effect when it is large. With C_2 at its minimum value and I_{in} at its maximum, the offset voltage will be negligible relative to the term containing I_{in} and C_2. Equation [5.3] may be written from equation [5.2] neglecting both the offset current and offset voltage.

$$V_o(t) = -\frac{I_{in}}{C_2}[t - 8.5 \times 10^{-7}(1 - e^{-1.2 \times 10^6 t})] \qquad [5.3]$$

In chapter 4 it was proposed to delay the time measurement for some period of time after the integration had begun to allow the exponential to die out. If this were done, the resultant error would be approximately equal to the term multiplying the exponential in equation [5.3].

We will now move on to the feedback circuitry of the integrator.

We determined previously the values of feedback capacitance for the various signal to noise ratios to be 21, 210, and 2100 pico farads, but we have said nothing about how the capacitance values would be changed in the circuit. Figure 9 illustrates two ways this switching of capacitor values might be achieved.

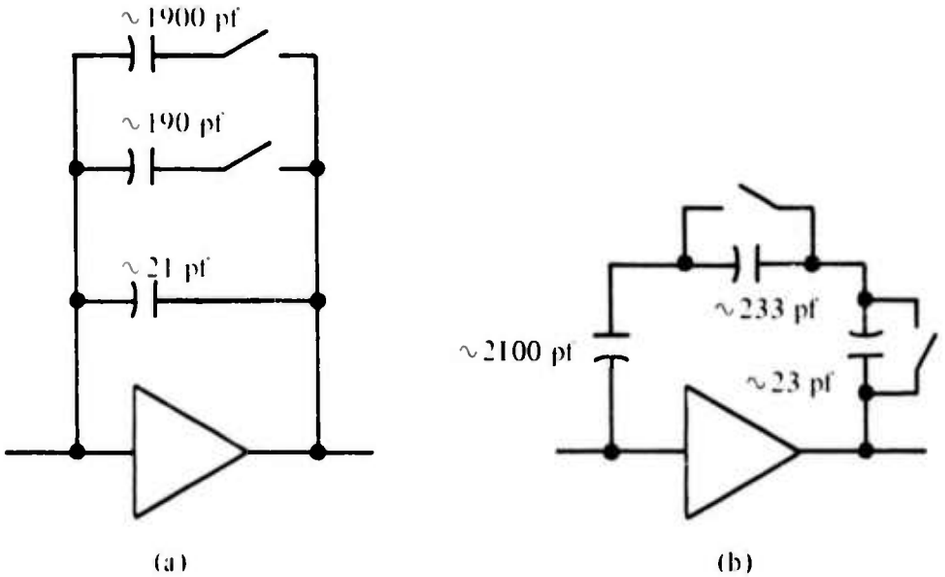


Figure 9: Two Methods of Changing Feedback Capacitor Value

In figure 9(a), the total feedback capacitance would be the effective parallel combination of the capacitors connected, and in figure 9(b), the total capacitance would be the effective series combination. The second alternative was chosen.

The advantage of the second configuration stems from a simplification in the adjustment procedure for the calibration of various signal to noise ratios. The signal to noise ratio is determined by the product of the reference voltage, V_{ref}, and the feedback capacitance, C_2. Three separate adjustments are needed to calibrate the three desired signal to noise ratios. The three adjustments may be chosen from four possibilities, these being the three capacitors and V_{ref}. Since a trimmer whose range is a significant part of 2100 pico farads is large physically, it was chosen to use a fixed value for the large capacitor, a trimmer for the smallest capacitor, a trimmer in parallel with an intermediate capacitor, and a potentiometer to vary the reference voltage.

With this choice of adjustments, the capacitor configuration of figure 9(a) yields an adjustment procedure where the adjustments are interactive. In this configuration there is no single adjustment for any signal to noise ratio. Each adjustment is dependent on another.

The adjustment procedure for the second case is straightforward and non interactive. The reference voltage is set with both switches closed to achieve the proper $C_2 V_{ref}$ product for a 100:1 signal to noise ratio. Next the switch in parallel with the intermediate sized capacitor is opened and the total capacitance is trimmed to achieve the correct product for a 32:1 signal to noise ratio. Finally, the second switch is opened and the trimmer for the smallest capacitor is adjusted.

The switches selected are mercury wetted relays. The contacts have an initial on resistance of no greater than 0.100 ohms. The off impedance is 10^{11} ohms in parallel with 3 pico farads. The capacitive part of the off impedance will sum with the capacitor it is shunting and the resisitive part is large enough that it may be ignored.

We have to this point presented an operational amplifier and a feedback network to achieve a useful integrator. We will now proceed to the design of the circuitry required to reset the integrator when the integration is completed.

5.2.2 Reset Circuitry

Once the output voltage of the integrator has reached its upper limit, the timer is stopped and the integrator must be reset in preparation for the next integration cycle. The integrator is reset by discharging the feedback capacitor. Conceptually this may be achieved by placing a switch in parallel with the capacitor. Ideally the switch would have infinite open impedance, zero closed impedance, and zero switching time.

A mechanical switch comes close to achieving the first two goals but does poorly on the third. Conversely, an electronic switch does poorly on the first two and better on the third. A second drawback for the mechanical switches is failure rate. The average number of contact closures for a practical mercury wetted relay is in the order of 10^7 to 10^8. (7) This number is much too small for any practical failure rate for the integrator circuit. For these reasons an electronic switch was chosen.

An FET offers the best characteristics for the function the switch is to perform. The most important characteristic is the source-drain leakage current in the off state. The lowest leakage current found for an FET commercially available (as of 6-1-72) was 0.1 nano amps at 25°C. This current sums with the input current and causes a corresponding error. The current is temperature sensitive and approximately doubles for every 10°C rise in temperature. A leakage current of this size is the dominant factor in imposing the lower current which can be measured.

The FET is used to short circuit the feedback capacitor C_2 and thus bring the output voltage of the integrator to zero. To limit the discharge current, a resistor of a few hundred ohms is placed between the drain of the FET and the input of the op amp.

Because of the gate to drain capacitance of the FET, it was necessary to capacitively couple to the drain a signal of opposite polarity to cancel out any charge induced into the input of the integrator during turn on and turn off of the switch. A trimmer capacitor was used so that its value could be adjusted to compensate the effects of the gate-drain capacitance.

The time required to reset the integrator is on the order of 4 to 5 micro seconds.

We will now proceed to the design of the comparator circuitry used to determine the gating of the timing circuit.

5.2.3 Comparator Circuitry

The requirements for the comparator circuitry have already been briefly discussed. It was determined that the timer should measure the time required for the integrator output voltage to rise 1.5 volts after the expiration of the required delay.

The proper gating for the timer may be achieved using two comparators whose comparison levels differ by 1.5 volts. The comparator at the lower level serves a dual purpose. First the desired delay is achieved by setting the lower level in such a way that the time required to integrate from zero to that level is at least as great as the delay time needed. Secondly, by detecting the lower level, the need for the integrator to be reset to an exact level is minimized. A drawback to this method is that the time required for the integrator to reach this lower level is dependent on the input current and may be considerably longer than necessary. It is therefore desirable to keep this level as low as possible. For the implementation described here the low level was chosen at 0.25 volts and the high level to be variable from approximately 1.5 to 2.0 volts.

The comparators used for gating the timer as described above should be able to compare the voltage with insignificant error relative to 1.5 volts and do the comparison in an insignificant amount of time relative to the minimum integration time. This minimum integration time occurs with the smallest feedback capacitor and the maximum input current which are 21 pico farads and 3.6 micro amps respectively. These figures give a time of approximately 8.7 micro seconds. The comparators chosen were National Semiconductor's LM311. Not only do they meet the requirements stated above but their power supply voltages are the same as the integrator's and their outputs are easily made compatible with the TTL circuitry used for the timer.

5.2.4 Summary of Analog Circuitry

We have to this point developed the necessary analog circuitry for the integrator shown in black box form in Figure 7. Figure 10 is a schematic showing this circuitry in detail. The intention of the preceding discussion was to point out some of the significant design problems and criteria and to illustrate how these problems affect the performance of the circuit. The circuit of Figure 10 was the first circuit built to test the basic ideas of the dissector current integration scheme. As will be shown in a later chapter, this circuit did verify the usefulness of such a scheme. Some thoughts on modifications and improvements to this circuit are given in the final chapter.

5.3 Digital Circuitry

The digital circuitry suggested by the right half of Figure 7 is sufficient to produce a number inversely proportional to the average current into the integrator. It is not, however, sufficient to implement other desirable functions for an image processing system. A discussion of the circuit requirements necessary to implement only the basic functions of Figure 7 will be presented here. Circuit details will be deferred to Chapters 6 and 7 where the implementation of this and other functions will be presented.

By the nature of the digital scheme outlined in Figure 7, the range of dissector output currents will be quantized into a range of digital numbers. The number of quantization levels governs the clock frequency and more importantly the resolution of the circuit as a whole. To simplify the following discussion, a specific number of quantization levels for a specific range of average dissector currents will be considered. It should be straightforward to see how a change in these numbers would affect the circuit.

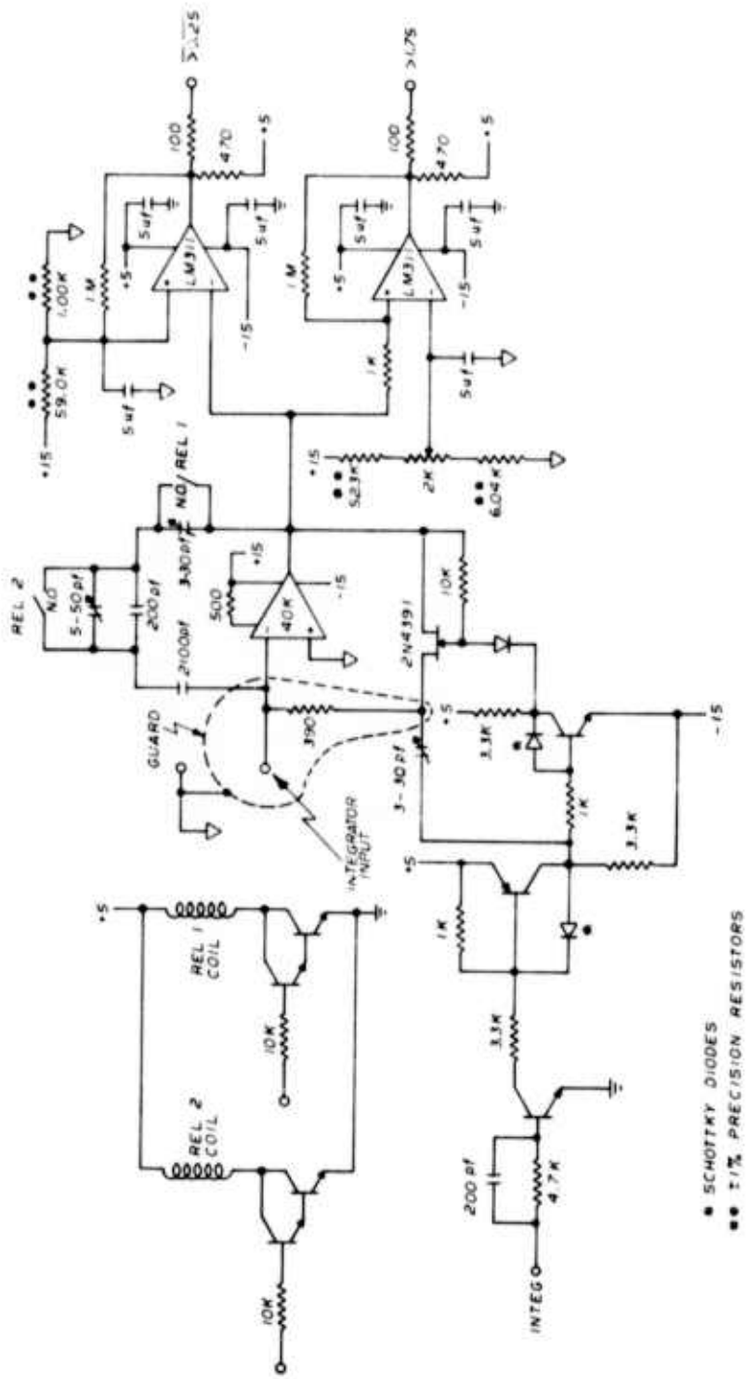


Figure 10: Integrator Schematic

The lower limit on the current which the circuit can measure without significant error is imposed largely by the leakage current of the FET used in the reset circuit. This current was given previously as 0.1 nano amps at 25°C and doubles for every 10°C rise in temperature. Allowing for a 20°C rise in temperature the maximum leakage current would be 0.4 nano amps. The maximum current from the dissector found previously was approximately 3.6 micro amps. An incident light intensity of 1% of the maximum would therefore produce a signal current into the integrator of 36 nano amps. The maximum error in measuring that current, due to the leakage current, would then be approximately 1.1% (0.4/36 * 100%). A signal current smaller than this would yield even a larger relative error and it is therefore unlikely that the measurement of a significantly smaller current would be attempted.

Counting a 78.125 kilo hertz reference (10 mega hertz ÷ 128) from 1 to 128 (200 base 8) covers a range of input currents of approximately 2.5 micro amps to 19 nano amps at a signal to noise ration of 10:1. A count of one would represent a current just below the maximum dissector current and a count of 128 would represent a current down in the range where significant errors begin to accumulate as previously shown for the 36 nano amp example.

If the output of a 78.125 kilo hertz clock were gated on and off to control the input to the counter, there would be an uncertainty of 12.8 micro seconds in the time of the first positive clock transition to the counter. This arises from the fact that the oscillator runs asynchronously relative to the gating signal which may occur any time within the 12.8 micro second period of the clock. If, on the other hand, a crystal clock were used with a frequency higher than necessary and the output of the oscillator were gated and then prescaled down to the proper frequency before being fed to the counter, the uncertainty would be one period of the higher frequency.

Starting with a 10 mega hertz clock and dividing that by 128 produces an output clock frequency of 78.125 kilo hertz and an uncertainty of 100 nano seconds between the gating signal and the first positive clock transition.

The integration times for signal to noise ratios of 32:1 and 100:1 are 10 and 100 times as great respectively as for a signal to noise ratio of 10:1. In order to produce the same digital number for a given average input current, independent of signal to noise ratio, the clock frequency may be divided down by an additional factor of 10 or 100 for the higher signal to noise ratio. The division for various signal to noise ratios may be achieved by using a three to one digital multiplexer with the inputs being 10 mega hertz, 1 mega hertz, and 100 kilo hertz and the output of the multiplexer going to the divide by 128 circuit.

Figure 11 indicates the circuitry necessary to implement the timing function just described. Chapter 6 presents a simple circuit for producing a number proportional to the log of the input current to the integrator.

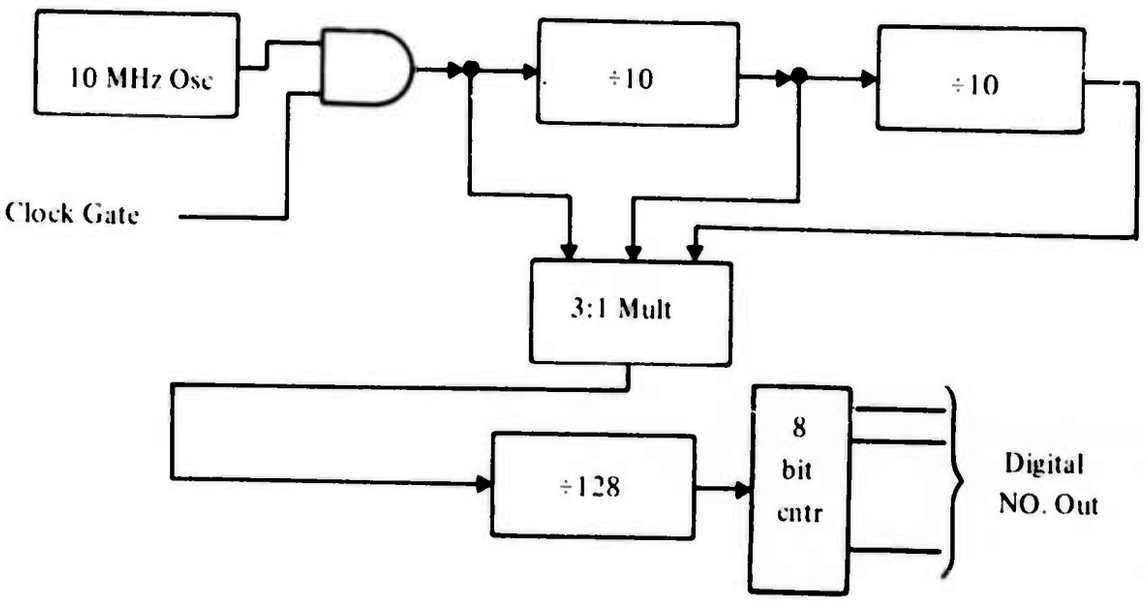


Figure 11: Timing Circuitry

6. LOG CIRCUIT

6.1 Introduction

The number derived from the circuit described in chapter five is inversely proportional to the light intensity. In many applications it is desirable to have a number proportional to the log of the intensity.

The scheme proposed here is a novel way of deriving the logarithm and when used in conjunction with the circuit described in the previous chapter will have the log of the number available as soon as the integration is complete. The scheme is entirely digital and its implementation is simple relative to the established methods of log taking.

6.2 Analog Representation of the Log Scheme

First an analog scheme will be proposed and an analytical model derived for it. Then it will be shown how the analog scheme may be approximated digitally.

Consider two ramps, one with a slope t and the other with a slope Bt where B is a constant greater than one. If every time the steeper ramp intersects the other it is reset, the graph of the two relative to each other would look as shown in Figure 12.

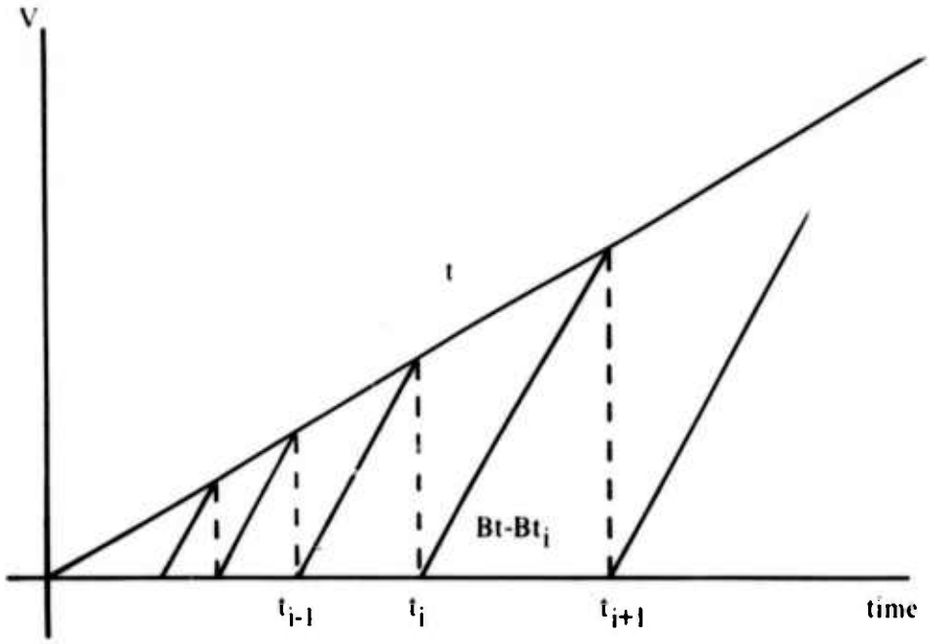


Figure 12: Graph of Ramps for Log Scheme

Setting the two functions equal at t_i (where t_i is the time of the i^{th} intersection) we obtain:

$$t_i = Bt_i - Bt_{i-1}$$

$$t_i(1-B) = -Bt_{i-1}$$

$$t_i = \frac{Bt_{i-1}}{B-1} = \left[\frac{B}{B-1}\right]\left[\frac{Bt_{i-2}}{B-1}\right]$$

$$= \left[\frac{B}{B-1}\right]\left[\frac{B}{B-1}\right]\left[\frac{Bt_{i-3}}{B-1}\right]$$

$$\vdots$$

$$t_i = \left[\frac{B}{B-1}\right]^i t_o$$

$$\ln t_i = i \ln\frac{B}{B-1} + \ln t_o$$

$$i = \frac{\ln t_i - \ln t_o}{\ln \frac{B}{B-1}} = \frac{\ln t_i}{K_1} - K_2 \qquad [6.1]$$

Where • $K_1 = \ln \frac{B}{B-1}$ and $K_2 = \frac{\ln t_o}{\ln \frac{B}{B-1}}$

Equation [6.1] indicates that the number of times the two ramps intersect is proportional to the log of the time. It is interesting to note that equation [6.1] is exact at the times the two ramps are equal. K_2 is a constant offset to i and K_1 is dependent on the ratio of the two ramp speeds and may be adjusted to achieve the desired base for the logarithm.

6.3 Digital Approximation

The two analog ramps of the preceding section may be approximated by the outputs of digital counters. When the number in the two counters are equal, the faster counter is reset and a third counter is incremented to form the log. The desired ratio of the counting speeds may be achieved in one of two ways. The faster counter may be incremented in larger steps than the slow counter and reset when its value is equal to or greater than the latter or, the faster counter may be incremented in unit steps at a greater rate than the slow counter and reset when their values are equal.

The first method requires an equal clock frequency for both counters; the second method requires a higher clock frequency for the fast counter than for the slow one. Generally, when taking the log of a number, it is desired to achieve the result in as little time as possible. Since the slow counter must count up to the number we wish the log of, it is then generally desirable to make the slow counter as fast as possible. If the faster counter must actually count at a higher rate than the slow counter, the maximum counting frequency is imposed on the fast counter and the slow counter's maximum counting frequency must then be some fraction of the maximum counting rate attainable. Thus, using the same type counters for both methods, the first method would yield the result sooner than the second. The disadvantage of the first method is that its increments are coarser than the second method and therefore it does not approximate a linear ramp as well.

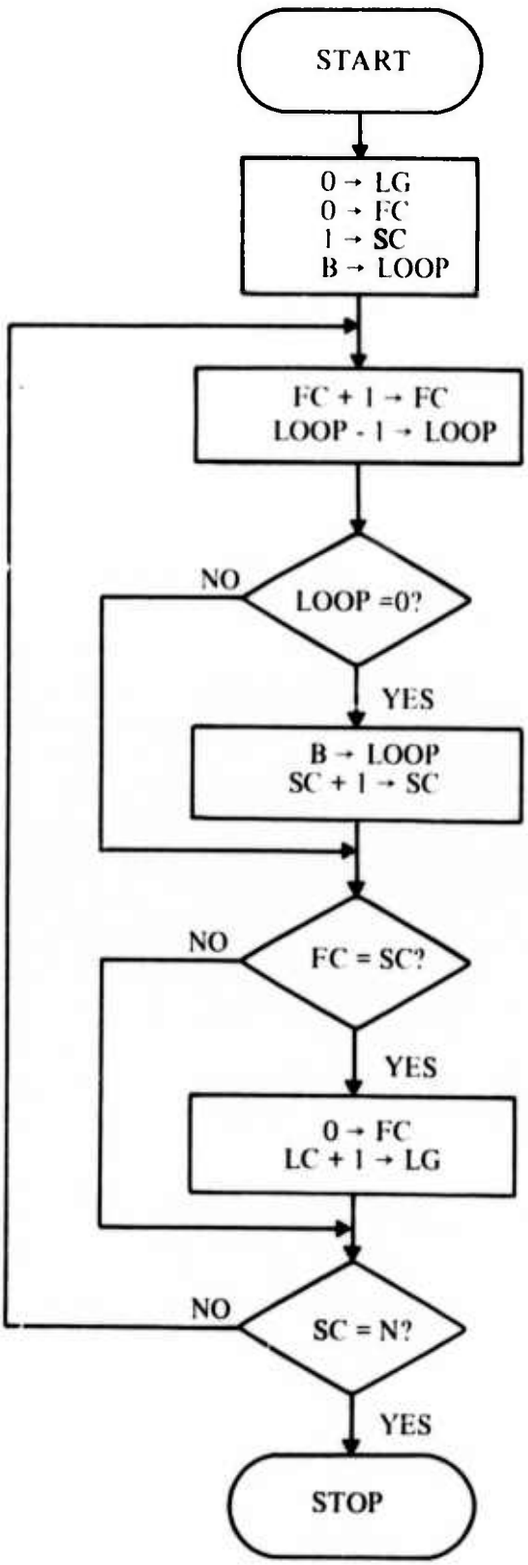
A digital computer program whose flowchart is shown in Figure 13 was written to test the effectiveness of the second alternative just described. The output of the program was a function of two numbers: 1) the argument of the log (N); and 2) the ratio of speeds for the two counters (B). Table 3 presents the results from this program for a number of combinations of N and B.

TABLE 3

DATA ATTAINED FROM ALGORITHM OF FIGURE 13

N \ B	2	4	8	16	32	64
1	1	1	1	1	1	1
2	1	3	7	15	31	63
4	2	6	13	28	57	116
8	3	9	19	40	81	164
16	4	11	24	51	104	210
32	5	14	30	62	126	255
64	6	16	35	73	148	300
128	7	19	40	84	170	344
256	8	21	45	95	192	388
512	9	23	51	105	214	432
1024	10	26	56	116	236	476
2048	11	28	61	127	258	520

The values for N given in Table 3 are integer powers of 2. The log of N should increase linearly as N increases exponentially. The columns of the table show a non linear increase in the log for small values of N but for large N the numbers increase at an approximately constant rate as desired.



Definition of Variable Names:

FC → Fast Counter
SC → Slow Counter
B → Ratio of Speeds
N → Argument of Log
LG → Log (N)

Figure 13: Log Scheme Algorithm

6.4 Application of the Log Scheme for Use with the Dissector

The circuit discussed in Chapter 5 developed a number inversely proportional to the current from the dissector camera. This number was obtained by counting the output of a crystal oscillator during the time the input current was integrated from zero up to a fixed reference voltage. The addition of the log circuit just described adds little complexity to the circuit as a whole.

The counter used in the circuit of Chapter 5 may be used as the slow counter for the log circuit and still function precisely as described previously. Therefore, in order to implement the log scheme three new functions must be added to the black box diagram of Figure 11 at the end of Chapter 5. These functions are : 1) a counter for counting at the faster rate; 2) a digital comparator to determine when the two counters are equal and to reset the fast counter; and 3) a counter to count the number of times the fast counter is reset.

It was previously pointed out that the analog log scheme could be approximated in two ways. The first approximation allowed a faster counting rate for the slow counter (and thereby produced the result in a shorter time) but was not as accurate as the second alternative. In the application of the log scheme to the dissector hardware, the speed of the slow counter is dependent on the integration time and the desired resolution. A clock frequency of 78.125KHz was chosen for the maximum counting rate for the counter. If we choose the better approximation for the log scheme the fast counter must then be capable of counting at a rate of at least B times 78.125KHz where B is the ratio of counter speeds.

Figure 14 is a modification of Figure 11 to include the necessary functions of the log circuit. Care must be taken in the implementation of the added functions shown. Since it is necessary for the digital comparator to compare the output of the slow counter with the output of the fast one between each increment of the fast counter, the sum of the propagation time from clock to output of the counter and propagation time through the comparator to the reset input of the fast counter must be less than one period of the fast counter. A ripple through counter would have been sufficient for use in the circuit implied by Figure 11 but because of the comparison requirements just stated, synchronous counters are required for the fast and slow counters of Figure 14.

Precaution should also be taken to ensure the validity of the comparator output. The output of the counters is unpredictable during the transition from one count to the next and may therefore produce an erroneous equality at the output of the comparator. This problem can be prevented in one of two ways. If the propagation delay discussed above is less than half the clock period, the positive transition of the clock may be used to increment the counter and the negative (or low) half of the cycle may be used to gate the comparator output to the reset input of the fast counter. The second alternative is to use synchronous counters which can be set to zero on a positive clock transition. Using the synchronous counters, clock pulse p would produce an equality and the output of the comparator could then be fed to the "clear" input of the counter to perform the clear operation on clock pulse p + 1.

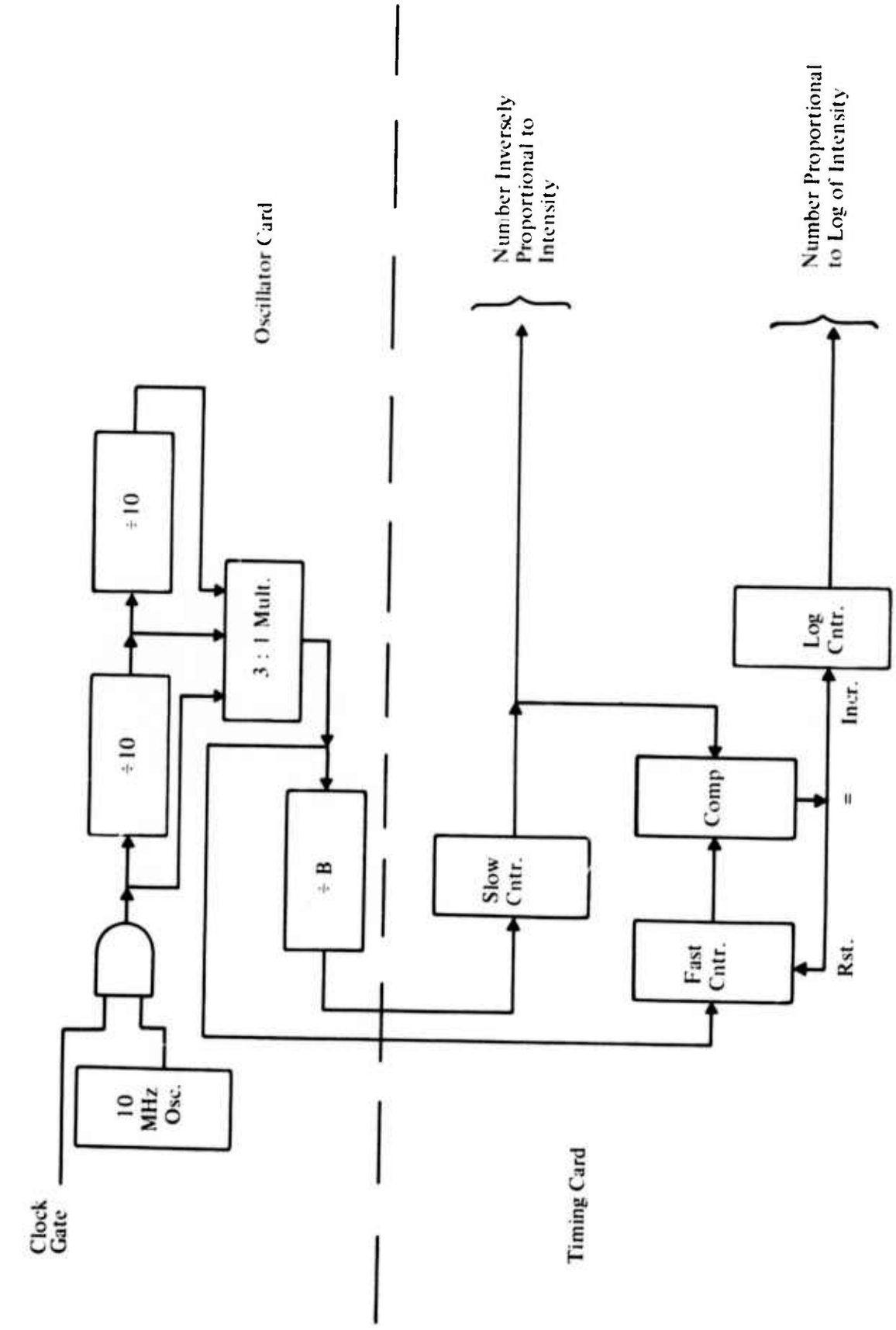


Figure 14: Addition of Log Function to Timing Circuit

Not only must the fast counter be reset when an equality occurs, but the log counter must be incremented as well. The possibility for erroneous counting is the same here as was the possibility for erroneous clearing of the fast counter above. The circuit in Figure 15 produces a negative pulse during the negative half of clock cycle p + 1 if the input "EQUAL" was high at the end of clock cycle p. This output pulse may be used to correctly increment the log counter.

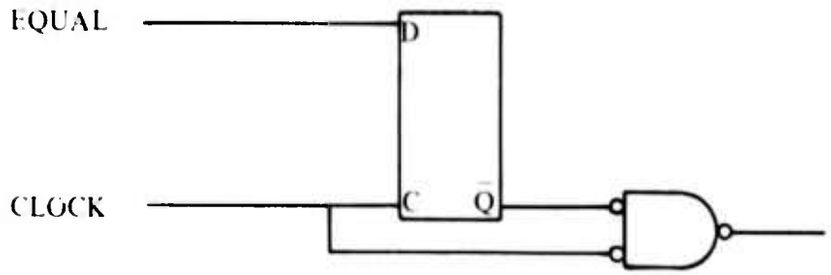


Figure 15: Increment Circuit for Log Counter

The next chapter will present details of the digital circuitry designed to implement the ideas of this chapter and the previous one. Numerical results from the application of the video processing hardware as a whole will also be given.

7. HARDWARE IMPLEMENTATION AND EVALUATION

7.1 Introduction

In this chapter details of the digital circuitry discussed in Chapter 6 will be presented. Also discussed will be details of interfacing techniques implemented to interface the video processing hardware as a whole to a PDP-12 digital computer. Finally, data taken by the computer from the processing hardware operating in an image processing environment will be presented and evaluated.

7.2 Digital Timing and Log Circuit Realization

Figure 16 is a slight modification of Figure 14 to include three new function blocks. The circuit implied by Figure 16 was the circuit constructed. The desire for the limit register and limit comparator arose from the frequently occurring image processing requirement of determining if the intensity of a point lies above or below a fixed threshold (or limit). With these added functions, an upper limit for the slow counter may be placed in the limit register. If an integration cycle has not completed before the slow counter reaches the value contained in the limit register, an equality output signal from the limit comparator will end the cycle. When a cycle is completed in this way, a bit may be set to indicate that the intensity of the examined point is at least as dim as the intensity represented by the number in the limit register.

Not only does the technique just described provide a simple way to determine if the intensity of the examined point lies above or below the threshold, it also limits the maximum time for an integration cycle. Time will not be wasted on determining the exact intensity of a point which is dimmer than the threshold.

The third functional block is a 2 to 1 data multiplexer used to gate either the number inversely proportional to the intensity or the log of it onto the data out lines.

Figure 17 is a schematic diagram showing in detail the circuit realization of everything below the dotted line in Figure 16. The circuit was constructed on a Digital Equipment Corporation wire wrap card model number W941. Figure 18 indicates parts locations, Figure 19 gives a parts list and indicates pins which are tied off to either ground, plus 5 volts, or to a 1K ohm resister to plus 5 volts. Figure 20 gives signal names for each of the card edge connector pins shown in Figure 17.

Certain aspects of the circuit deserve special note. The integrated circuits used for the fast and slow counter are SN74161 TTL synchronous 4 bit counters with synchronous load and asynchronous clear. The asynchronous clear is important so the counters may be preset to zero before the clock starts. The synchronous load is used to load all zeros into the fast counter on the next positive clock transition after an equality from the comparators.

At this point a word about the comparators seems in order. Two comparator functions are shown in Figure 17. One is needed to determine when the fast and slow counters are equal and the other to determine when the slow counter equals the contents of the limit register. The

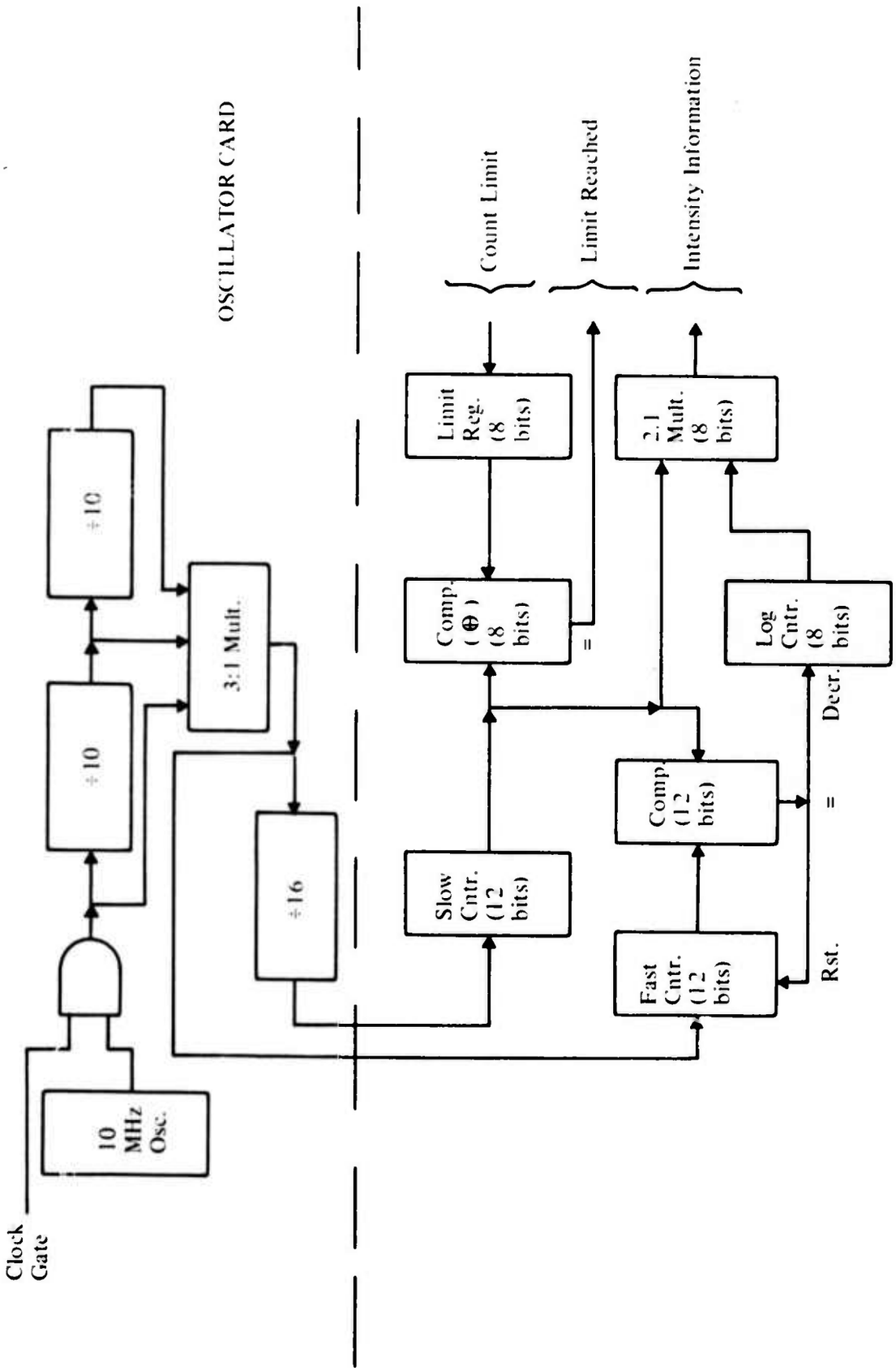


Figure 16: Complete Timing Circuit

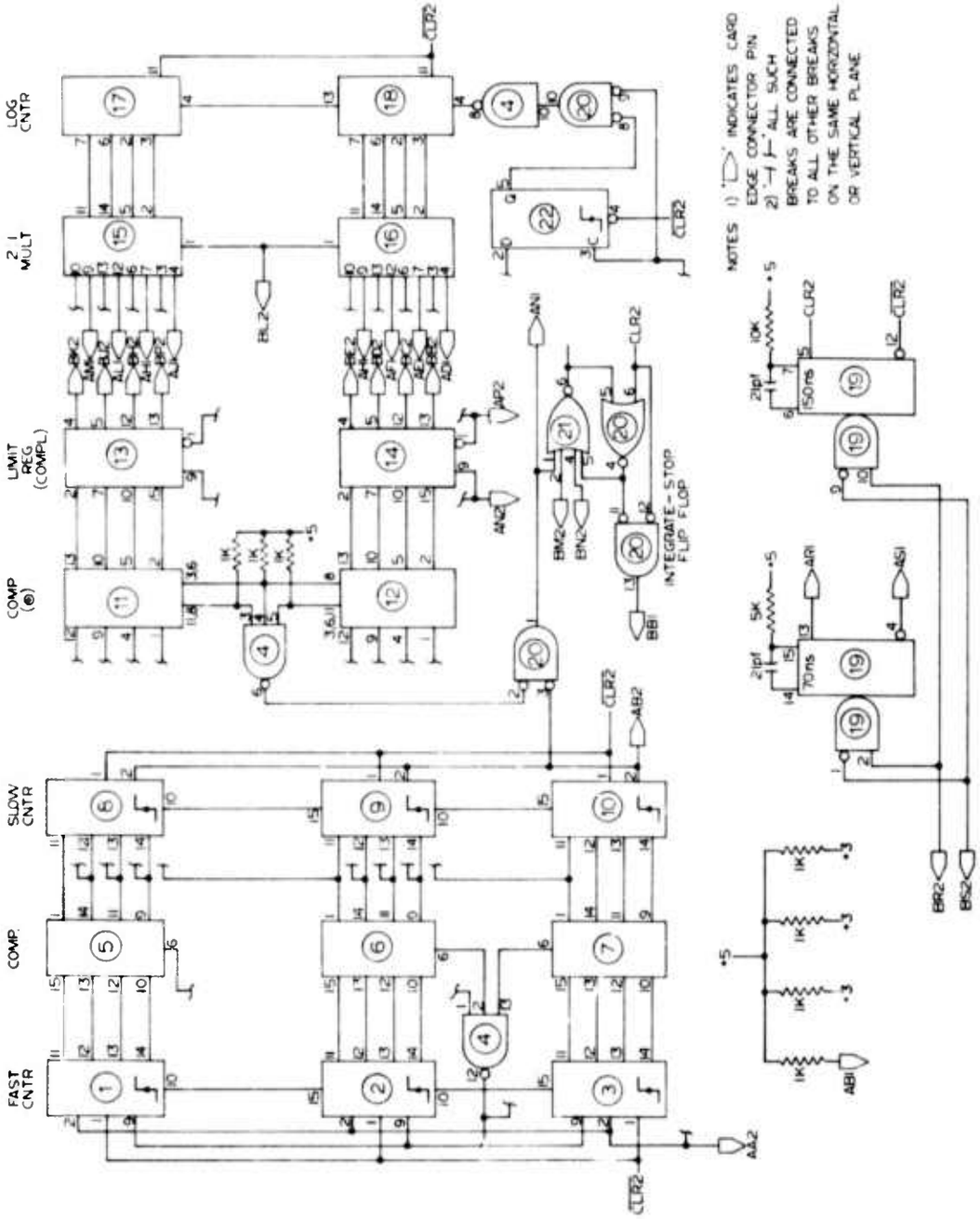


Figure 17: Timing Circuit Schematic

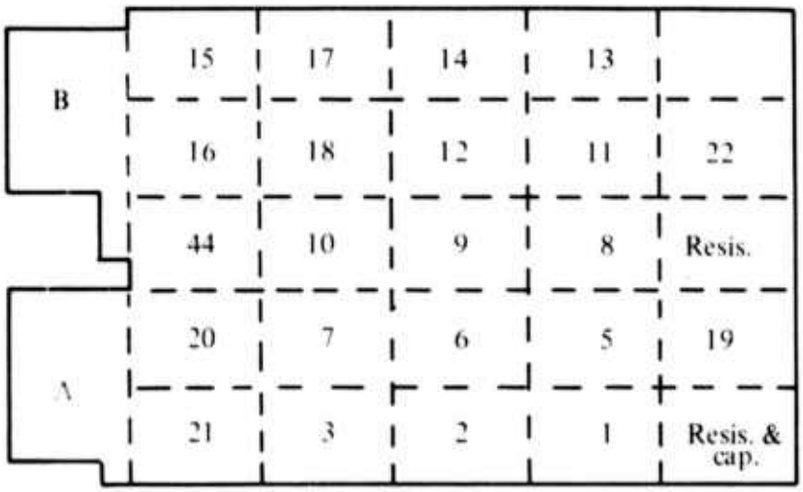


Figure 18: Timing Board Component Locations

IC Packages

No.	Type
1	SN74161
2	SN74161
3	SN74161
4	SN74H10
5	SN7485
6	SN7485
7	SN7485
8	SN74161
9	SN74161
10	SN74161
11	SN74136
12	SN74136
13	SN74175
14	SN74175
15	SN74175
16	SN74175
17	SN74193
18	SN74193
19	SN74123
20	SN7402
21	SN7425
22	SN7474

Ground

Packages	Pins
1, 2, 3	3, 4, 5, 6
15, 16	15
17, 18	10, 11, 14, 15
18	9
1 - 3, 5 - 10, 13 - 19	8
4, 11, 12, 20 - 22	7

+ 3 (1KΩ to + 5)

Packages	Pins
19	3, 1
8, 9, 10	3, 4, 5, 6, 7, 9
3, 10	7, 10
4	9, 11
1, 2, 3	7
5, 6, 7	2, 3, 4
17, 18	5
17	9
22	1, 10, 11, 13
21	3, 9, 10, 11, 12

+5

Packages	Pins
1 - 3, 5 - 10, 13 - 19	16
4, 11, 12, 20 - 22	14

Figure 19: Parts List and Pins to be Tied Off

Pin No.	Side 1 (OUT)	Side 2 (IN)
AA	GND	FSTCLK
B	+3 (Source)	SLWCLK
C		
D	DATA 0 (LSB)	
E	DATA 1 (LSB)	
F	DATA 2	
H	DATA 3	
J	DATA 4	
K	DATA 5	
L	DATA 6	
M	DATA 7 (MSB)	
N	LIMRCH	LIMSET
O		MAXSET
R	CLR	
S	CLR	
T	+5	
U		
AV	GND	
BA	GND	
B	INTEG	LIM 0 (LSB)
C		LIM 1
D		LIM 2
E		LIM 3
F		LIM 4
H		LIM 5
J		LIM 6
K		LIM 7 (MSB)
L		LOG
M		PRESET
N		>1.5
P		
R		START
S		START
T	+5	
U		
BV	GND	

Figure 20: Signal Names on Card Edge Connector for Figure 17

requirements of the former are more stringent than those for the latter since the first must make its decision in a fraction of one period of the high frequency and the second need only make its decision in a fraction of one period of the lesser frequency.

Before we procede, note that both the fast and slow counters are shown as 12 bit counters in Figure 16. This was done to minimize the error in the result of the log. Referring back to Chapter 6 it was pointed out that there was a noticeable error in the log of N for small values of N. The effects of this error have been reduced by using 12 bit counters and taking the result from the most significant 9 bits. In this way, N has been scaled down by 8 and the errors associated with taking the log of N equal 1 to 7 only impose an additive constant to the result (log (N)).

For the faster comparator, SN7485's were used. These are 4 bit cascadable digital comparators which produce greater than, less than, and equality outputs. If the individual comparators were cascaded to produce a 12 bit comparator, the propagation delay time would be too great. Since only the equality outputs were needed, each of the three outputs from the individual comparators are ANDed together to produce a low output when the two counters are equal. This output is fed to the "load" input of the fast counter and the "D" input of the flip-flop for the log counter.

The other comparison was accomplished using collector ORing of open collector exclusive OR gates. The limit register is loaded with the complement of the desired limit and the output of this register is fed to one side of the exclusive OR's. When all bits match, the output of the NAND gate, which combines the various exclusive OR outputs, will go low and during the negative half cycle of the clock this "equal" signal will reset the "integrate-stop" flip-flop. By ANDing the "equal" signal with the negative half of the clock cycle, the output of the comparator has time to settle during the positive half cycle.

The "integrate-stop" flip-flop in Figure 17 is a minor variation of the simple set-reset flip-flop. An integration cycle is begun by providing a start pulse to the one shot which produces clear or initialize pulses to all counters and sets the "integrate-stop" flip-flop. The output of the flip-flop which enables the integrator is inhibited until the one shot returns to its normal or stable state. The flip-flop is reset by one of three signals: (1) preset; (2) signal indicating integrator has reached its upper limit; or (3) signal indicating slow counter has reached the limit held in the limit register. It is significant to note that no counter is reset until the beginning of a new cycle. In this way, the counters serve as output registers for the data generated.

Another point worth mentioning is the counter circuit used to keep track of the number of times the fast counter is reset and thus form the log. First of all, note the type D flip-flop serving the function discussed in Chapter 6 and illustrated in Figure 15. To insure that this circuit functions correctly, the sum of a number of delay times must be less than one period of the highest frequency to the fast counter. This period is 100 nano seconds. The delay time is the sum of: (1) clock to output of the fast counter (same as clock to output of slow counter so it may be ignored); (2) input to equality output of the SN7485 comparator; (3) input to output of SN74H10 NAND gate; and (4) set up time for the D input to the flip-flop. The maximum specified times for each of the above are: (1) 23 nano seconds; (2) 30 nano seconds; (3) 10 nano seconds; and (4) 20 nano seconds. Thus the maximum delay time from positive edge of clock pulse p to correct setup of the D input to the

flip-flop is 83 nano seconds which is sufficient time in preparation for the data to be clocked in on the positive edge of clock pulse p + 1.

The second significant point about the log counter is that it is used as a down counter. Since taking the log of a number inversely proportional to the intensity produces minus the log of the intensity, counting down from a preloaded value in the log counter will produce a number proportional to plus the log of intensity. The log counter is preset to 200 octal during initialization just prior to an integration cycle.

7.3 Interface to the Computer

The communications between computer and video processing hardware will be discussed in this section. The method by which this communication is established would of necessity vary somewhat from one type of computer to another. However, the information passed between computer and the hardware should essentially stay the same.

The communications about to be described were achieved with the use of minor additional circuitry to that already discussed. This circuitry was designed for the specific purpose of interfacing the video processing hardware to a DEC PDP-12. The circuitry includes nothing more than some data complementers, decoders for decoding bus information from the computer, a set-reset flip-flop for interrupt enable and disable, and a few registers for storing mode bits (such as signal to noise ratio).

Before we procede to describe what the circuit interfaced to the computer does do, it is significant to mention one thing it does not do. In a working system, of which this hardware is a part, the dissector's deflection coils must be deflected to the desired point and be given time to settle before the integration cycle is begun. The hardware described here assumes that when it receives a start signal the deflection circuits have already settled to their final value. Suggestions for some interaction between deflection circuitry and video processing hardware are made in Chapter 8.

The correct operating procedure for this processing hardware interfaced to the PDP-12 will now be given.

Data is passed to and from the computer via the accumulator. Figure 21 indicates the function of the accumulator bits for transfers into and out of the computer.

After the accumulator has been loaded with the appropriate information, an I/O instruction is executed to load the accumulator bits into the proper interface registers. The sign bit of the accumulator-out determines whether the limit register on the timing card is loaded with the contents of the least significant eight bits of the accumulator or set to its maximum value of 377_8.

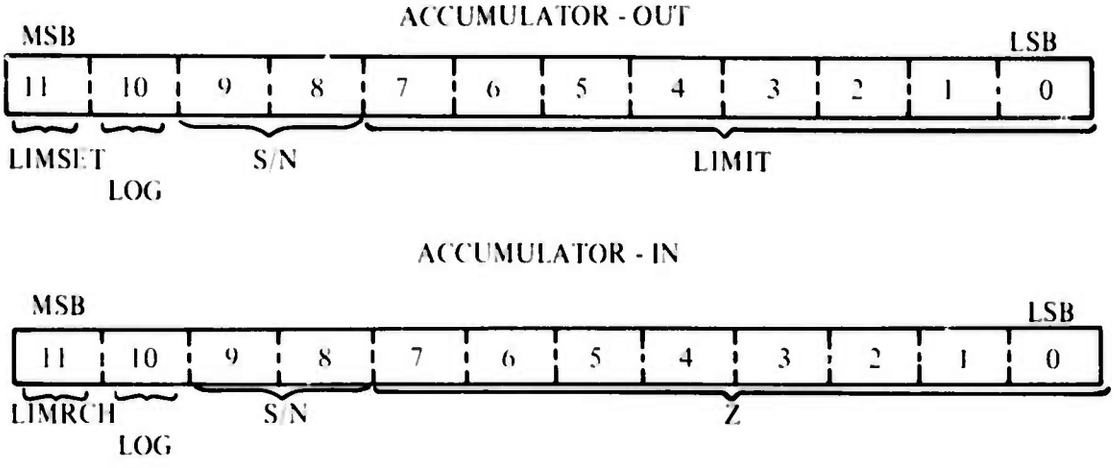


Figure 21: Use of Accumulator for Information Transfer

The two bits labelled "S/N" select the desired signal to noise ratio as defined below. A code of "10" is undefined.

S/N	CODE
10	00
32	01
100	11

The "LOG" bit determines whether the number returned to the computer is inversely proportional to intensity or proportional to the log of it.

An I/O test instruction may be executed to test for the completion of an integration cycle. This is a skip type instruction and both senses are available (skip if ready or skip if not ready).

After it has been determined that an integration cycle has completed, an instruction may be executed to retrieve the data. The intensity information is loaded into the least significant 8 bits of the accumulator. The present status of the "LOG" and "S/N" registers within the processing hardware are placed in the bits so marked in Figure 21. The sign bit of the accumulator-in indicates whether or not the cycle was stopped by the limit register. If the bit is returned low, the least significant 8 bits will be a true representation of the intensity of the examined point. By placing this information in the sign bit it is easily tested.

The efficiency of the system as a whole may be improved considerably by operating in the interrupt mode. After the interrupt has been enabled, the video processing hardware will interrupt the computer at the end of the integration cycle. In this mode of operation the computer is free for other functions at all times other than when it is handling the interrupt. During the interrupt it must take the new intensity information, select a new point to be examined, and start the new integration cycle.

Now that the system operation has been presented, we move on to presentation and discussion of results obtained from the circuitry while performing in an actual image processing environment.

7.4 Presentation and Discussion of Results

In this section we will treat two parts of the processing hardware separately. First we examine the performance of the log circuit. Secondly, we will evaluate the performance of the processing hardware as a whole and discuss its effectiveness as a useful image processing tool.

7.4.1 Data From the Log Circuit

In order to evaluate the ability of the log circuit to take the log of a number given it, a program was written to implement the algorithm indicated in the flow chart of Figure 22. Since the value of the log is truncated to an integer, there will be several values of N for which log (N) will be the same. The program is therefore written to print out the first value of N which produces a new value of log (N). At the same time N is printed, its associated value for the log is also printed.

Table 4 contains some selected values of N and their associated log and Figure 23 presents a semi-log graph of that data. The values of N given in Table 4 were selected on the basis of which values would make approximately linear increments in the value of the log. The other data produced by the program described above was omitted from the graph only for the sake of clarity.

Due to the fact that the value produced by the log circuit is truncated, the true value of the log could be as much as one more than calculated. Because of this, the graph of Figure 23 indicates an uncertainty of one in the value of LOG(N).

The graph indicates an error for small values of N, but for all values of N greater than 3 on the graph, the line intersects all experimental values as shown. The third column of Table 4 was obtained by evaluating equation [7.1] below for each value of N given. (Calculations were done on a Hewlett Packard model HP-35 calculator.)

$$LOG(N) = 94.2 - 15.47 \ln(N). \qquad [7.1]$$

Note that for all values of N greater than or equal to 7 the value obtained by truncating the third column of Table 4 is the same as the corresponding value in the second column. The log circuit, when used to take the log of a number, as the number is accumulating in a counter, has obvious advantages over other log calculating schemes. These advantages include: (1) small amount of hardware required to implement the algorithm; (2) stability and repeatability inherent to digital circuitry; and (3) log is developed simultaneously with the number accumulating in the base counter.

7.4.2 Adjustment of the Integrator

Before any useful data may be taken from the video processing hardware, the integrator should be properly adjusted. As discussed in Chapter 5 there are 4 necessary adjustments. These adjustments include: (1) a trimmer capacitor to compensate for gate-drain capacitance of the reset

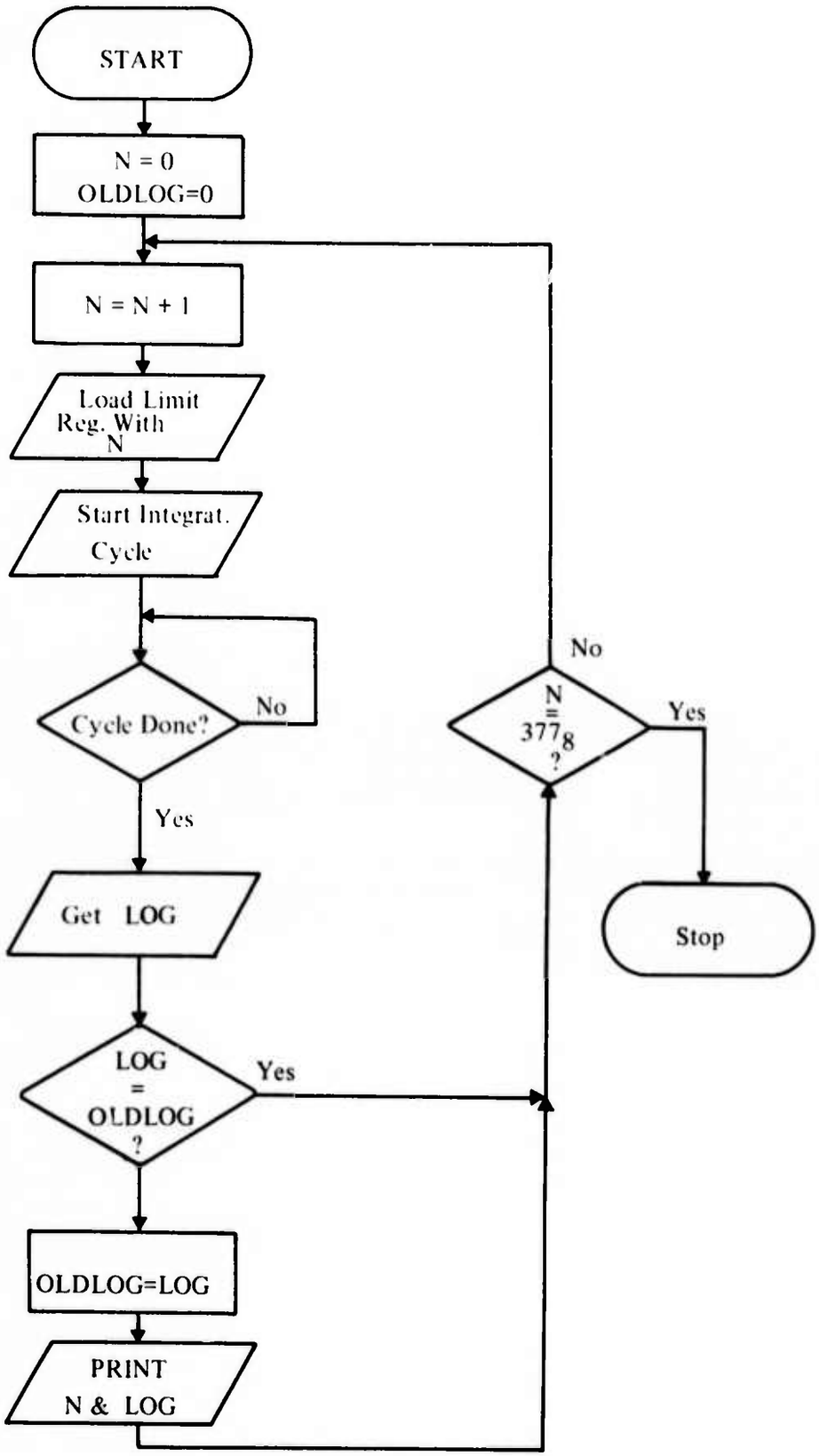


Figure 22: Flow Chart for Log Data Acquisition

TABLE 4

DATA OBTAINED WITH ALGORITHM OF FIGURE 22

N	EXPERIMENTAL LOG (N)	CALCULATED* LOG (N)
1	92	94.2
2	82	83.5
3	76	77.2
4	72	72.8
5	69	69.3
6	66	67.2
7	64	64.1
8	62	62.0
9	60	60.2
10	58	58.6
13	54	54.5
15	52	52.3
18	49	49.5
20	47	47.9
25	44	44.4
30	41	41.6
36	38	38.8
44	35	35.7
50	33	33 7
60	30	30.9
73	27	27.8
83	25	25.8
95	23	23.8
115	20	20.8
139	17	17.9
180	13	13.9
205	11	11.9
249	8	3.8

* LOG (N) = 94.2 - 15.47 ln(N)

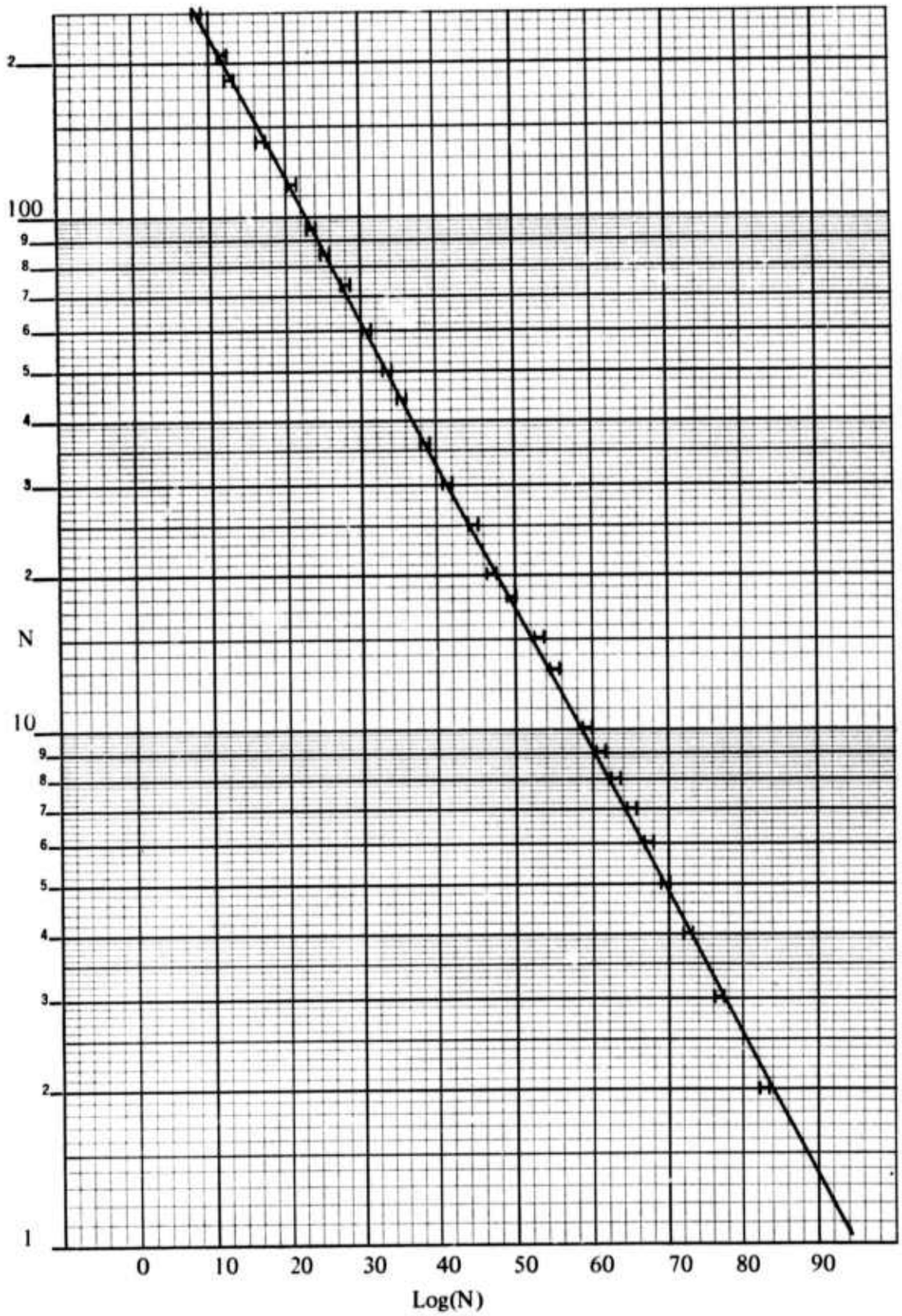


Figure 23: Graph of Data from Figure 4

transistor; (2) a variable resistor for adjusting the reference voltage; (3) a trimmer capacitor for adjusting the feedback capacitance for a signal to noise ratio of 32; and (4) a trimmer capacitance for adjusting the feedback capacitance for a signal to noise ratio of 10. The order of adjustments is the same as the order of presentation here.

With no input current to the integrator, the FET trimmer should be adjusted so there is no apparent discontinuity to the integrator output voltage when the FET is turned off at the beginning of the integrator cycle. The signal to noise ratio adjustments may be made using a known input current to the integrator and adjusting the appropriate component for the correct number out of the timing circuit for the given input current.

The clock period for the slow counter may be found from equation 2.

$$\tau_{clk} = 0.128 \times (S/N)^2 \ \mu s. \qquad [7.2]$$

Equation [5.1] indicates that the charge integrated is a constant for any given signal to noise ratio. Since charge is equal to the product of current and time, the integration time becomes:

$$\tau_{int} = \frac{(S/N)^2 \times 3.2 \times 10^{-12}}{I_{in}} . \qquad [7.3]$$

The number produced by the counter then becomes:

$$N = \frac{\tau_{int}}{\tau_{clk}} = \frac{3.2 \times 10^{-13}}{0.128 \times 10^{-6}} \frac{1}{I_{in}} = \frac{2.5 \times 10^{-6}}{I_{in}} . \qquad [7.4]$$

With equation [7.4] and remembering the N is truncated to an integer value, a value of I_{in} and a corresponding value of N may be chosen for the adjustment procedure. If a value of I_{in} is chosen such that when properly adjusted, the counter output will oscillate between n and n + 1, the adjustment procedure becomes very simple. As an example of such a combination of I_{in} and n, I_{in} could be chosen at 125 nano amps and the integrator should be adjusted such that the number produced by successive integration cycles would oscillate between 19 and 20 (23 and 24 octal).

With a current standard supplying 125 nano amps to the integrator input, the adjustment procedure becomes: (1) continuously cycle the integrator in the 100 to 1 signal to noise ratio mode and display the number produced at the end of each cycle; (2) adjust the trim pot until the number displayed oscillates between 23 and 24 octal; (3) switch to signal to noise ratio of 32 to 1 and adjust appropriate trimmer capacitor until the number again oscillates between 23 and 24 octal; and (4) repeat step 3 for signal to noise ratio of 10. This completes the adjustments.

7.4.3 Data From Integrator and Timing Circuit

The first set of data to be presented was obtained by supplying a number of different known input currents to the integrator and recording the corresponding numbers produced by the timing circuit. The data obtained from this procedure is presented in Table 5.

TABLE 5

DATA FROM INTEGRATOR AND TIMING CIRCUIT
WITH CURRENT SOURCE SUPPLYING INPUT CURRENT

I_{in}(nA)	N_8
2000	1
1000	2
500	5
250	12
125	24
62.5	46
31.3	111
15.6	202

Each succeeding value for I_{in} in the left column of the table is one half of the preceeding value. Since the count produced by the timing circuit is inversely proportional to I_{in}, we would expect that N would therefore double in each succeeding row (within the bounds of the truncation error).

Below an input current of 125 nano amps, an error begins to appear in the right column of table 5. For an input current of 15.6 nano amps we would expect a value for N of 240_8. The fact that the numbers generated by the timing circuit are smaller than expected would indicate that there is a leakage current into the integrator with the same polarity as the signal current. The signal current required to produce an output count of 240_8 was determined to be approximately 11.1 nano amps. The difference between the predicted value of I_{in} and the measured one required to produce the output count of 240_8 indicates that the leakage current is approximately 4.5 nano amps.

A leakage current of 4.5 nano amps corresponds to an error of 0.1 percent of the maximum input current 3.6 micro amps found in Chapter 2). Although this may be a significant error for some purposes, it should be pointed out that the integration and timing scheme used produces high resolution for low input currents and in many image processing applications the resolution is more significant than the absolute accuracy. The needs of the individual image processing system should determine if it is desirable or necessary to invest the time and effort to improve the circuit and decrease this error term.

The second set of data to be presented was obtained by repeated integration of the dissector output while it was directed at a fixed point of constant intensity. By taking repeated samples, a histogram of the number generated by the processing hardware versus the number of times that number occurred was produced. After such a histogram was generated for each of the three signal to noise ratios, a statistical evaluation program, written in FORTRAN, was executed on the data and produced the numbers in the right three columns of Table 6.

TABLE 6

DATA FROM STATISTICAL EVALUATION PROGRAM

THEORETICAL S/N	MEASURED S/N	$\bar{t}$ (In milli sec.)	NUMBERS OF SAMPLES TAKEN
10	11.35	1.01	109,656
32	33.84	10.24	68,183
100	89.42	103.70	4,987
100	90.61	103.73	12,366
100	90.66	103.69	21,427
100	87.25	103.61	33,454

The first column of Table 6 is the desired signal to noise ratio selected by the S/N mode bits to the hardware. The second column is the signal to noise ratio calculated by the FORTRAN program by taking the ratio of the mean of the data to its standard deviation as suggested by equation [2.2]. The third column is the calculated average integration time in milli seconds. (Using equation [7.3], the average current can be shown to be approximately 31 nano amps which corresponds to approximately 0.9% of maximum.) The fourth column of the table is the total number of samples used for the statistics.

One objective in compiling the data presented in Table 6 was to determine the ability of the processing hardware to measure the intensity of a point within a certainty dictated by the selected signal to noise ratio. For theoretical signal to noise ratios of 10 and 32, the observed signal to noise ratio was slightly higher but for a theoretical signal to noise ratio of 100 the observed signal to noise ratio was less.

There are four rows of data given for a signal to noise ratio of 100 with each successive row being the results of an additional accumulation of samples from the previous one. This data was obtained by recording the progress of the histogram on four occasions during execution of an experiment.

It is significant to note that the first three rows of data for the 100:1 signal to noise ratio indicate a move toward a reasonable value of measured signal to noise ratio but the fourth row indicates a downward movement away from the theoretical value. The cause of this unexpected observation has been attributed to variations in the high voltage power supply due to ambient temperature changes.

As is shown in Appendix 9.1, the dissector's output current is hightly dependent on the voltage supplied to it. If the ambient temperature of the high voltage power supply changed significantly during the middle of an experiment such that there was a measurable change in the average dissector output current, the width of the histogram (the variance of the data) would increase and subsequently cause the observed signal to noise ratio to decrease. Such variations in the output current were observed and directly correlated to the air conditioning cycles within the room where the experiments were performed.

The variations in the dissector's output current due to ambient temperature changes did not significantly affect the data in Table 6 for signal to noise ratios of 10 and 32. This may be explained by considering two factors. First, the time required to accumulate the data for the lower signal to noise ratios is significantly less. Each sample for a signal to noise ratio of 10 takes 10 and 100 times less than the average sample times for 32:1 and 100:1 signal to noise ratios respectively. Because the data may be accumulated in a shorter period of time, the probability of a significant ambient temperature change during the time of the experiment is less.

The second factor accounting for the apparent poorer performance for the higher signal to noise ratios is that a small shift in the average output current will cause a higher percentage change in the variance of the data for high signal to noise ratios as opposed to lower ones.

7.5 Chapter Conclusions

For its simplicity in both conception and implementation, and because of the favorable performance indicated by the data presented in this chapter, the new log scheme seems to be well suited for this application. The data presented in Table 5 indicates favorably the ability of the integrator and timing circuit to measure input currents in the range of interest. Table 6 however, suggests some problems exist in the performance of the image processing system as a whole. Chapter 8 will discuss these problems and suggest how they may be corrected. Also presented in Chapter 8 are suggestions for additions to the processing hardware to make the system perform in a more useful and efficient manner.

8. RECOMMENDATIONS FOR FUTURE WORK

8.1 Improvement of High Voltage Power Supply

It was suggested in Chapter 7 that the cause for the observed temperature instability of the dissector current was poor regulation of the high voltage power supply. Appendix 9.1 shows the dependency of the dissector on the voltage supplied to it. The findings of Appendix 9.1 will be summarized here.

Equation [8.1] represents the absolute voltage change which would produce a factor of K change in the output current of the dissector (e.g. K = 1.01 for a 1% change).

$$\Delta V = 170.85 \ln K. \qquad [8.1]$$

The dependency of focusing on high voltage is also discussed in Appendix 9.1 and it is suggested there that a 0.006% change in the high voltage supplied to the dissector will produce a noticeable degradation in the resolution of a properly focused camera.

The requirements for power supply stability are imposed largely by the focus dependency on high voltage. For the resolution of the camera to be limited only by the physical size of the aperture, the variability of the output voltage with respect to line variations and temperature (load constant) must be less than 0.006% over the entire range of environments the dissector will be subjected to.

The temperature coefficient of the high voltage power supply used for the experiments of Chapter 7 was at best 0.02%/ C which indicates that, independent of line variations, a 2°C change in ambient temperature would decrease the resolution by a factor greater than two and the average output current would change by approximately 0.5%. For an image processing system whose performance is limited by the limitations of the dissector tube, a significantly better power supply is mandatory.

It should be noted that in later dissector cameras manufactured by ITT, a voltage regulator is used to regulate the first anode potential relative to the photocathode and thus decrease focusing instability.

8.2 Improvements to the Integrator

8.2.1 Use of Faster Operational Amplifier

The output voltage equation as a function of input current and nonidealities of the amplifier for an operational amplifier integrator is approximated by equation [4.5] and may be represented by the equation of an ideal integrator delayed by a time τ_d. The equation for that delay time is given by equation [4.6] and rewritten as equation [8.2] for convenience.

$$\tau_d = \frac{1}{a} - \frac{C_2 V_{os}}{I_{eff}} \qquad [8.2]$$

$$a = \frac{A\omega_o + \omega_1}{D}$$

This delay was the primary reason for the additional comparator at the lower level. If the time τ_d could be made negligible relative to the integration period the lower comparator would not be necessary.

$A\omega_o$ and V_{os} of equation [8.2] are the small signal unity gain and the offset voltage respectively for the operational amplifier used. For many high performance amplifiers, the offset voltage is adjustable to zero. If the null adjustment of the offset voltage became part of the adjustment procedure, the effective delay τ_d would be dependent only on a. By choosing an amplifier whose small signal unity gain would yield a τ_d insignificant relative to the smallest integration time, the lower comparator would then be unnecessary.

Remembering that the minimum clock period for the slow counter is 12.8 micro seconds, it is sufficient for τ_d to be negligible relative to that time. The meaning of "negligible" is dependent on the specific system user's requirements. We may choose a τ_d of 100 nano seconds (less than 1% of minimum clock period) as an example to provide some feeling for the necessary $A\omega_o$. Using values of 3.4 and 4.8 for representative values of D and ω_1 respectively (these values were determined in Chapter 5) the value of $A\omega_o$ to produce a τ_d of 100 nano seconds is approximately 3.4×10^7.

An obvious reason for using a better operational amplifier and consequently doing away with the lower level comparator is a reduction in circuit complexity. There are two other reason not as obvious but at least as significant as the first.

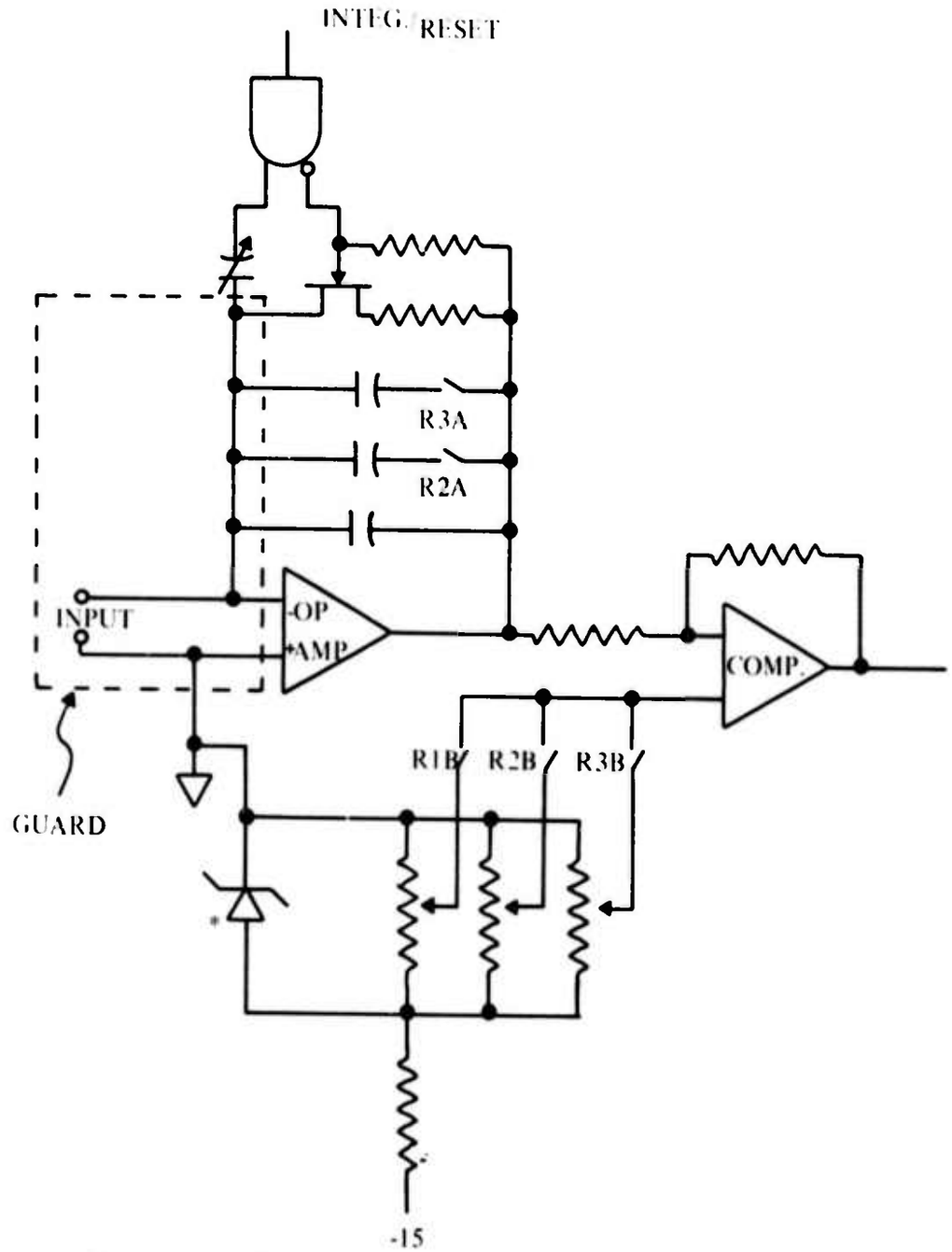
Completion of an integration cycle is established by either the integrator reaching its upper limit or by the slow counter reaching the value contained in the limit register.

Consider what would happen if there were little or no input current to the integrator (dissector directed at a very dark point). If the output voltage of the integrator never reached the level of the lower comparator, the counter would never be gated on and the cycle would never be terminated. If the counter is enabled at the beginning of the cycle, as it would be if there were no lower level comparator, a termination of one kind or the other is assured.

The third advantage to the exclusion of the comparator is a savings in time. Without this comparator, no time is wasted integrating up to the lower level.

8.2.2 Rearrangement of Feedback Capacitors

Figure 9 of Chapter 5 suggests two alternatives for the method of switching feedback capacitor values. The method shown in figure 9-b was chosen for the circuit built. It was suggested



*Temperature Compensated Zener

Figure 24: Abbreviated Schematic of Improved Integrator

in Chapter 5 it was undesirable to switch both the feedback capacitor and the reference voltage to achieve different signal to noise ratios. Since only one was to be switched, the method of switching capacitors suggested by figure 9-b was chosen because it allowed for a noninteractive adjustment procedure. We now wish to present an alternative method which has several advantages to the circuit described in Chapter 5.

Consider a capacitor feedback arrangement where the capacitors are in parallel as in Figure 9a. If the relays used to switch in and out the capacitors had DPST contacts then one contact could be used for the capacitors and the other half could be used to switch a new reference voltage to the comparator for each value of total feedback capacitance. A simplified schematic of the modified integrator is presented in Figure 24.

The primary advantage to this circuit is the mechanical layout of the circuit board required. With the new circuit the input ends of all capacitors may be tied together and electrically isolated from the board. This is important because it reduces the possibilities for leakage paths which could impede the proper operation of the integrator with very low input currents.

If the value for the three feedback capacitors are properly chosen, the relative shift from one reference voltage to another will be small. Figure 24 shows the addition of a temperature compensated zener to establish a stable voltage which is used to provide the various reference levels.

8.2.3 Conclusions

By using a better operational amplifier and the circuit configuration of Figure 24, reduction in the complexity of both analog and digital circuitry may be achieved with an overall improvement in circuit performance.

8.3 Circuit Additions

8.3.1 Buffering of Input and Output Data

A latency period between the completion of one integration cycle and the beginning of the next exists in the operation of the video processing hardware described in previous chapters. This latency period is the time required for the computer to take the data generated from the previous cycle, deliver new X and Y coordinates to the deflection circuitry, and start the integrator.

The computer service time may be done in parallel with the integration if the data to and from the video processing hardware is buffered. After the initiation of the n^{th} integration, the computer may load the deflection buffers with the coordinates for the $(n+1)^{th}$ point to be examined and then procede to other operations. At the end of the n^{th} integration cycle the processing hardware would store the Z information in the output register, indicate to the computer that the cycle had completed, and then begin on the $(n+1)^{th}$ operation without any intervention from the computer.

8.3.2 Asynchronous Deflection Circuitry

For speed optimization, the use of the video processing hardware developed in previous chapters should be asynchronous relative to the computer driving it. Given that the overall use of

the circuitry is already asynchronous, a potentially time saving addition is to make the deflection circuitry asynchronous as well by varying the settling time in relation with the distance the camera is deflected. By allowing for small settling times for small deflection increments the system will operate faster than if a maximum deflection settling time were allowed after the selection of each new point.

9. APPENDIX

9.1 Dissector Instability with Voltage and Temperature

The purpose of this appendix is to investigate potential variations in the dissector's performance with changes in ambient temperature and high voltage.

Figure 9.1.1 is a graph taken from reference (2) indicating the anode sensitivity in amperes per lumen and the typical amplification characteristics of a photomultiplier as a function of applied voltage. It was pointed out in Chapter 1 that an image dissector may be represented as a photomultiplier tube with the ability to examine only small portions of its photosensitive surface.

Using Figure 9.1.1 we wish to obtain some feeling for the dissector sensitivity to variations in the high voltage power supply. To do this it is sufficient to find the slope of the lines presented. The equation characterizing the lines in Figure 9.1.1 are of the form indicated by equation [9.1],

$$\ln A = mV + b \ . \qquad [9.1]$$

where A is the gain or sensitivity and V is the applied voltage.

The slope may be found by taking two points from one of the lines (slopes of all lines are equal within the necessary precision for this discussion) and applying them to equation [9.2].

$$m = \frac{\ln(A_1/A_2)}{V_1 - V_2} \ . \qquad [9.2]$$

where m is the slope, A_1 and A_2 are the gains, or sensitivities from the two points and V_1 and V_2 are the corresponding values for the voltage for those two points (equation [9.2] was derived by solving the two simultaneous equations $\ln A_1 = mV_1 + b$ and $\ln A_2 = mV_2 + b$ for m).

Using the line labeled "MAXIMUM SENSITIVITY" in Figure 9.1.1 the following values were taken for use with equation [9.1].

$$A_1 = 2 \times 10^7 \qquad V_1 = 1.16 \times 10^3$$

$$A_2 = 4.2 \times 10^5 \qquad V_2 = 5 \times 10^2.$$

These values for A and V yield a value of 5.853×10^{-3} for m.

Exponentiating both sides of equation [9.1], equation [9.3] results

$$A = e^{(mV + b)} = e^b e^{mV} = C_1 e^{mV}. \qquad [9.3]$$

Solving equation [9.3] for V in terms of C_1, A, and m yields equation [9.4].

$$V = \frac{1}{M} \ln \frac{A}{C_1} \ . \qquad [9.4]$$

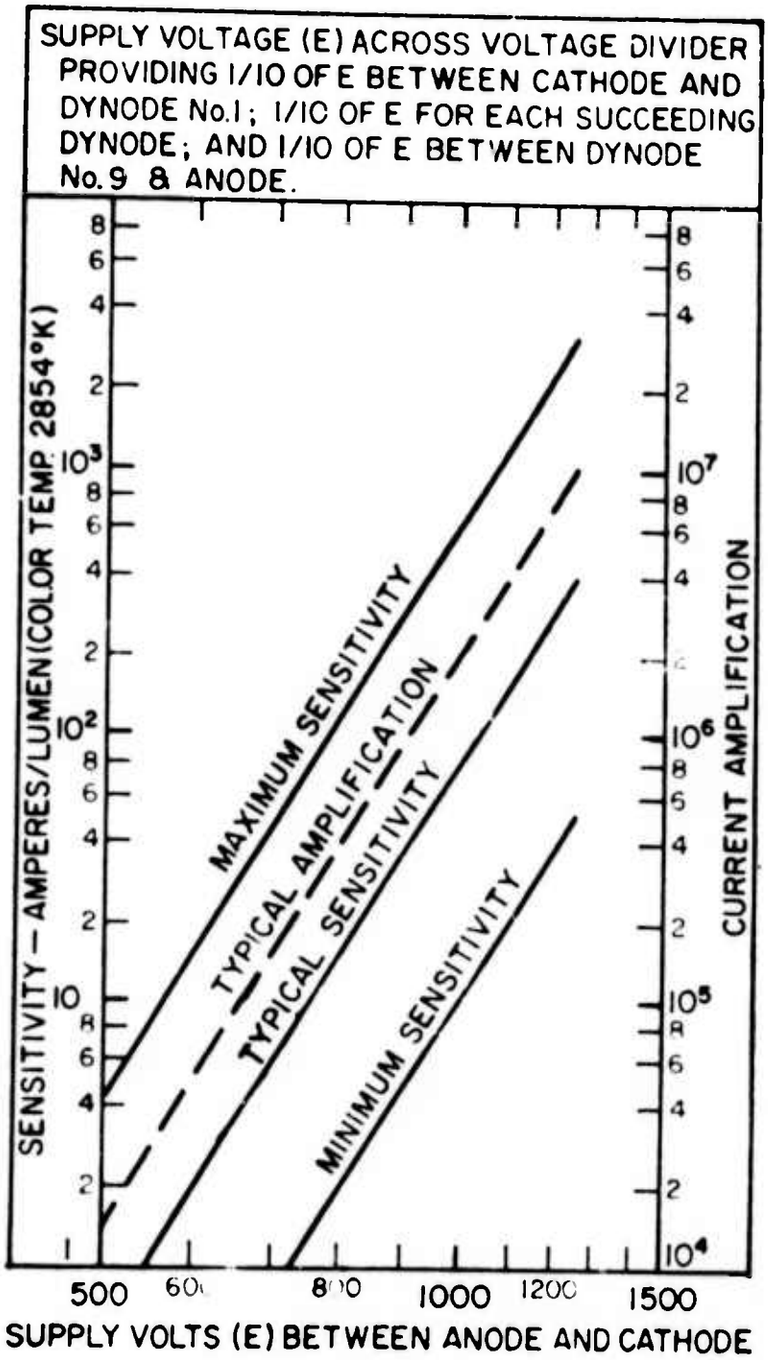


Figure 9.1.1: Voltage Sensitivity of Photomultiplier Time

Using equation [9.4] it is now desired to find the change in V for a factor of K change in A. This is shown in equation [9.5].

$$\Delta V = \frac{1}{M}\left[\ln \frac{KA}{C_1} - \ln \frac{A}{C_1}\right]$$

$$\Delta V = \frac{1}{M} \ln \left(\frac{KA}{C_1} \cdot \frac{C_1}{A}\right)$$

$$= \frac{1}{M} \ln K. \qquad [9.5]$$

Knowing the maximum allowable change in the output current due to power supply instability, equation [9.5] may be used to calculate the maximum allowable power supply variations. As an example, assume that a variation in output current of no greater than one percent due to the power supply is desired. One percent change implies K = 1.01 and yields a ΔV of 1.7 volts which is 0.08% of the nominal 2100 volts supplied by the high voltage power supply to the dissector. Table 9.1.1 presents similar data for various values of K.

TABLE 9.1.1

DISSECTOR DEPENDANCY ON HIGH VOLTAGE POWER SUPPLY

K	ΔV	% of 2100 VOLTS
1.005	0.85	0.04
1.010	1.70	0.08
1.015	2.54	0.12
1.020	3.38	0.16
1.030	5.05	0.24
1.050	8.34	0.40

Table 9.1.1 suggests that a well regulated power supply is essential if a predictable output current versus photocathode illumination is desired from the dissector.

For the dissector camera used for the experiments of Chapter 7 voltage instability may be even more significant in its effects on resolution than it is on average current.

The model of the dissector tube deviates from the model of a photomultiplier when the aperture of the dissector is considered. As discussed in previous chapters, the signal current from the dissector is established by deflecting electrons from a selected point of the photocathode in such a way that these electrons will pass through the aperture and the electron multiplier and appear as a signal current at the output of the tube.

The resolving power or resolution of the tube is determined by the relative size of the photocathode compared to the effective aperture size. The word "effective" is used here because the true physical size of the aperture will be equal to the effective aperture size only if there is perfect electron focusing between the photocathode and the aperture.

As the electrons travel toward the aperture they are subjected to a magnetic focusing field. The effects of this field on the motion of the electrons is dependent on the electron's velocity which is in turn dependent on the accelerating voltage between the photocathode and the first anode which contains the aperture at its center. In the dissector camera used for the experiments of Chapter 7 the acceleration voltage is 600 volts which is developed using a resistor divider across the 2100 volt high voltage power supply. The manufacturer (ITT Aerospace/Optical Division) was consulted to determine the dependence of focusing on acceleration voltage and the following is a quotation from the manufacturer in a written reply dated March 15, 1973. "In practice it is found that a change in image section volts of about 40mV causes a barely detectable change in effective aperture size - hence resolution. A change of 0.2 volts nearly doubles the effective size of a small (e.g., .001") aperture".

0.2 volts change out of 600 is 0.03 percent which relates directly to the percentage change in the high voltage required to double the effective aperture size or cut the resolution in half.

After having observed experimentally temperature instability in the output current of the dissector and realizing the importance of a well regulated power supply, the high voltage power supply was removed from the camera and its output versus temperature curve was plotted. (The power supply was loaded with an equivalent resistance of the resistor divider chain for the dissector.) The measured temperature coefficient was 0.04%/°C. This would suggest that if the ambient temperature for the room in which the dissector camera is used were to change by 1°C the average output current would change by approximately 0.5% and the resulution would decrease to less than half the original value!

In order to confirm or disprove the above evaluation of the high voltage power supply, ITT was consulted on the specified temperature coefficient for the power supply provided by them with the camera. An ITT representative informed the author verbally that they had no such information (this was four and a half years after initial delivery of the camera) but if it was felt that this information was significant he would arrange for a representative sample of the power supply to be tested.

In a written reply from ITT the high voltage power supply temperature coefficient was specified to be approximately 0.02%/°C. This meant that the ambient temperature of the power supply could change by 2°C instead of 1°C, as predicted by the author, to experience a halving of the resolution.

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