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TRAPATT AMPLIFIER FOR PHASED ARRAYS

M. I. Grace, et al

Sperry Research Center

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February 1974

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This report describes the design and development of a wideband TRAPATT amplifier in a microstrip configuration, and is also concerned with the progress being made on the development of CW devices in a ring geometry. Particular emphasis is placed on describing surface degradation effects observed in large periphery devices and the approaches used toward solving these difficulties.
An amplifier broadbanding technique based on a lumped element technique is described and preliminary experimental results are presented. A section

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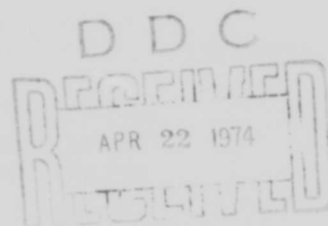
TRAPATT AMPLIFIER FOR PHASED ARRAYS

M. I. GRACE
C. N. POTTER
H. KROGER
H. J. PRATT

SPERRY RESEARCH ~~CORPORATION~~ Center



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FOREWORD

This final report was prepared by Sperry Research ~~Corporation~~ Center, under Contract F30602-72-C-0202, Job Order No. 55730536. Mr. R. Hunter Chilton (OCTE) was the RADC Project Engineer.

The report has been reviewed by the Office of Information, RADC, and approved for release to the National Technical Information Service (NTIS).

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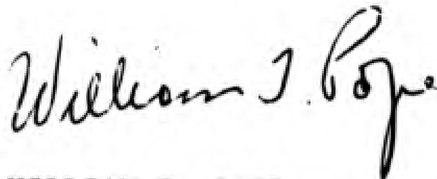
R. H. CHILTON
Project Engineer

APPROVED: 

WILLIAM T. POPE
Assistant Chief
Surveillance and Control Division

FOR THE COMMANDER:

CARLO P. CROCETTI
Chief, Plans Office

ABSTRACT

This report describes the design and development of a wideband TRAPATT amplifier in a microstrip configuration, and is also concerned with the progress being made on the development of cw devices in a ring geometry. Particular emphasis is placed on describing surface degradation effects observed in large periphery devices and the approaches used toward solving these difficulties.

An amplifier broadbanding technique based on a lumped element technique is described and preliminary experimental results are presented. A section describing the use of small area diodes as a means of lowering input power thresholds for a TRAPATT amplifier is included. Improvements in amplifier efficiency through the use of a new bias network which permits second harmonic tuning is also described. Finally, a summary of a generalized TRAPATT amplifier design technique developed at SCRC is presented.

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EVALUATION

Project: 5573
Contract No: F30602-72-C-0202
Effort Title: TRAPATT Amplifier for Phased Array
Contractor: Sperry Research Center, Sudbury, Mass.

1. Phased Array systems having solid state microwave generators as the source of rf power have not achieved their potential due to a large degree to the lack of sources. It is to this objective that this effort has been directed, as outlined in the RADC Technology Plan - TPO - 18.

2. Details of the work covered by this report on TRAPATT amplifiers are a significant step toward achieving the objectives and information contained should be of value to researchers pursuing similar programs. For example, surface degradation in large area devices is identified as a major problem and various approaches to overcome this problem are presented. Also, a new bias network was developed toward the end of the effort that yielded higher overall efficiencies. Both of these are significant and warrant further investigation.

R. H. CHILTON
Project Engineer

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SECTION 1

INTRODUCTION

The objective of the program is the further development of a wideband TRAPATT amplifier, originally evolved at the Sperry Research Center with RADC's support under Contracts No. F30602-70-C-0110 and F30602-71-C-0294. Present work has largely been concerned with surface degradation effects observed in the large periphery ring devices and improved circuit techniques for increasing the amplifier bandwidth, lowering input power thresholds, and improving amplifier efficiency.

The basic diode structure used the broadband amplifier and is discussed in Sec. 2. Section 3 describes the fabrication techniques used in producing the single mesa ring diode. CW oscillator results at 1.8 to 2.0 GHz are presented. Degradation in the operation of ring diodes has been observed, and has been attributed to surface effects. Section 4 is concerned with a description of the observed surface degradation and a summary of the approaches used to attempt to solve this problem.

Section 5 is concerned with circuit techniques. A method using lumped circuit elements as a means of increasing amplifier bandwidth and flattening amplifier response is described. The use of diodes of smaller area than we have previously used is considered as a method of reducing amplifier input power threshold. A new bias circuit which permits second harmonic tuning is described as a method of improving amplifier efficiency and increasing amplifier gain. A summary of the report is given in Section 6. An appendix is also included which gives a summary of a generalized method developed at SCRC for the design of wideband TRAPATT amplifiers.

SECTION 2

BROADBAND AMPLIFIER DIODES

The broadband amplifier diodes used in the 3.4 GHz amplifiers were punch-through p^+ -n-n^+ silicon devices with breakdown voltages typically in the range of 75-85 V with active areas equal to about 10^{-4} cm^2. The diodes were fabricated either by diffusion of boron into n/n^+ silicon wafers or by diffusion of phosphorus into p/p^+ silicon wafers. Although the widest bandwidth ever observed was with an n-p-p^+ structure (17%), in general, superior performance with regard to efficiency and reproducible bandwidth was achieved with p-n-n^+ devices. A particularly unattractive feature of the behavior of the n-p-p^+ devices was the high input power density of at least 6×10^5 W/cm^2 required to excite the broadband TRAPATT amplifier mode. The p-n-n^+ diodes, shown in profile in Fig. 1, had field widths of about 3.0 ± 0.2 μ at breakdown as determined by measurements of differential capacitance and area. The acceptor concentration curve of Fig. 1 represents the combined effects of boron diffusion to a depth of about 2 μ followed by an etch back of the surface by about 1 μ in order to reduce the thermal impedance by limiting the amount of silicon between chip surface and the active, high electric field, portion of the device. The field width at breakdown appears to be the most critical parameter associated with the doping profile of the broadband amplifier diode.

The doping density of the n-type epitaxial layer was not critical, with excellent structures fabricated from n layers doped as lightly as 1.2×10^{15} cm^{-3} and as heavily doped as 5×10^{15} cm^{-3}. It is interesting to note that TRAPATT diodes with field widths as great as 3 μ would not produce particularly efficient self-excited oscillators at 3.4 GHz, but, rather, would have their peak efficiency at about 2.0 - 2.2 GHz.

The amplifier diodes, when biased with current densities of about 100 A/cm^2 all showed a small-signal negative resistance over the frequency range from about 6 to 8 GHz. While this latter observation may not necessarily

be directly related to the operation of the broadband TRAPATT amplifier mode, it does underscore the fact that these devices have a remarkably wide field width for operation at 3.4 GHz. The best oscillator, as distinguished from amplifier performance, at 3-4 GHz was obtained from devices whose field width was so narrow that no small-signal negative resistance could be observed at 6-8 GHz under dc bias conditions.

When operated in the broadband TRAPATT amplifier mode, the devices were biased with current densities in the range of 2.5×10^3 to 10^4 A/cm^2. Under such conditions, it is possible that a small-signal negative resistance exists at the second harmonic of the fundamental frequency[1] due to excitation of Relaxing Avalanche Mode.[2] This observation may have direct bearing on the operation of the broadband TRAPATT amplifier mode, since a device is imbedded in a circuit which provides a parallel resonance at the second harmonic of the amplifier output frequency.

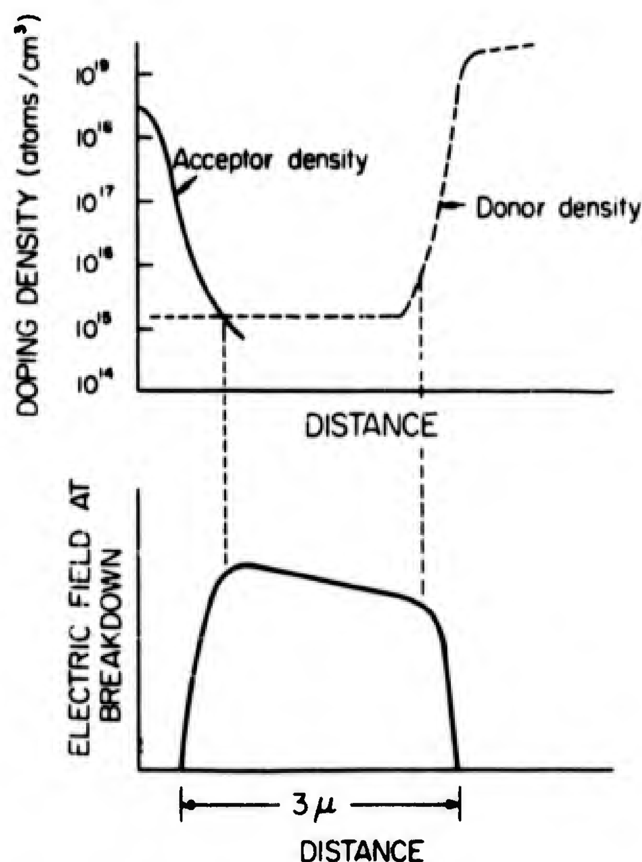


FIG. 1 Doping density and electric field distribution vs distance for S-band broadband TRAPATT diode.

SECTION 3

BASIC RING DIODE STRUCTURE

3.1 FABRICATION

The type of ring structure studied in this program is a single mesa structure. A completed device, together with mounting details, is illustrated in Fig. 2. This configuration is not only simple in concept, but also simple to fabricate; only a single photoresist step is needed. Initially, this approach was viewed as a high risk effort, largely because of the apparent complexity of the final fabrication step; however, this did not turn out to be the case.

The steps in fabricating this structure are outlined in Fig. 3. The starting silicon slices are only one to two mils thick and are uniform in thickness to ±10%. This excellent control on thickness has been achieved through recent improvements in the cupric-ion displacement process. Gold layers 2000 Å thick are evaporated on both sides of the wafer. The gold layer on the back side of the wafer is plated up to ~ 6 μ (Fig. 3(a)). Photoresist application (Fig. 3(b)), mesa delineation (Fig. 3(c)), and mesa etching (Fig. 3(d)) proceed in the normal manner. The photoresist and the top contact metalization are then stripped (Fig. 3(e)).

A prolonged gold etch is used to separate the chips (Fig. 3(f)). The separated chips are then metallized on the top surface (junction side) by evaporation to form the electrical contact (2000 Å of gold is applied). This evaporation deposits some metal on the sides of the mesa, but this is removed later in the process. The diodes are then TC bonded to diamonds that are metalized to a thickness of 2 μ. The bonding permanently protects the freshly applied contacts and the less than 2000 Å of gold covering the sides of the mesa can be quickly etched away without impairing the 2 μ thick gold metalization on the diamond or the 6 μ thick back contact. Simultaneous with bonding the device to the diamond, the gold preform contact and the strap (~ 1 mil thick) are bonded to the back of the chip. The device is then etched to the required area.

A completed structure mounted in an experimental configuration is

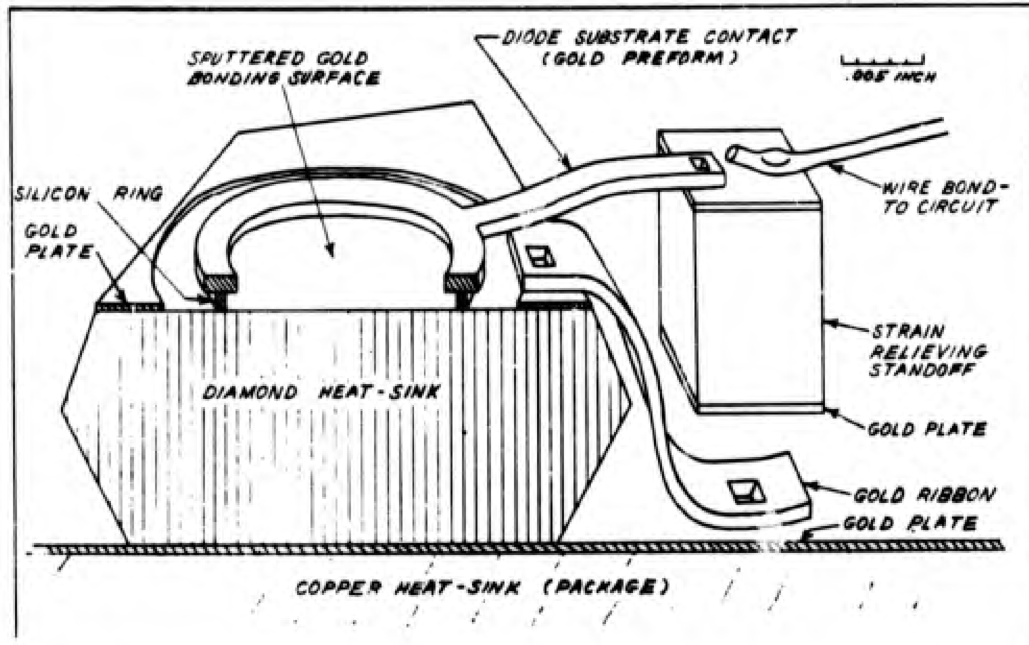


FIG. 2 Cut away diagram of mounting of single mesa ring diode.

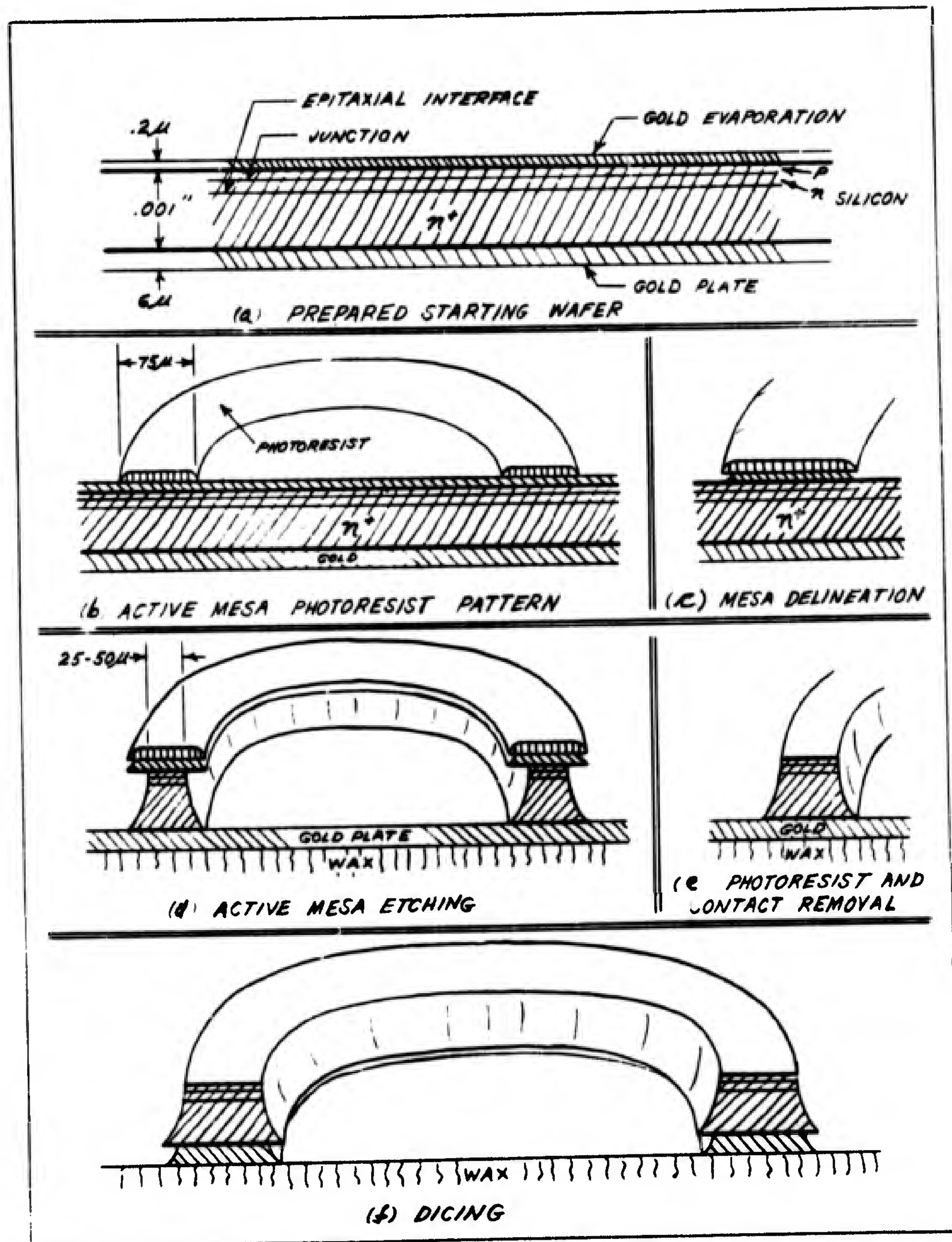


FIG. 3 Cut-away view of sequential steps in fabrication of single mesa ring diode:

(a) Starting wafer;

(b) Photoresist application;

(c) Mesa delineation;

(d) Mesa etching;

(e) Removal of photoresist and junction side contact;

(f) Chip separation by prolonged gold etch to backing metallization.

shown in Fig. 2. The "strain-relieving standoff" need not be used. Its purpose is to ensure that if the wire bond to the circuit needs to be changed (to tune the parasitic reactances of the mounting - an important part of the whole TRAPATT circuit), it can easily be done since the final width of the silicon (8 μ) is too thin to conveniently serve as a bonding surface. Likewise, the gold ribbon from the top of the diamond to the copper heat sink is usually not needed, in that the plating on the sides of the diamond is usually sufficient. It should be noted that the lateral dimension of the diamond shown in Fig. 3 is not to scale. The diamonds nominally have a linear dimension of ~ 40 mils, while the diameter of the ring is approximately 15 mils. A photomicrograph of a single mesa ring diode is shown in Fig. 4.

3.2 PERFORMANCE

Several runs of ring diodes have been operated as cw oscillators. These devices were fabricated with breakdown voltages of approximately 80 V and field widths at breakdown of 3 μ. These characteristics were chosen to optimize wideband amplifier performance at 3.4 GHz; however, diodes with these parameters operate quite efficiently as self-triggered oscillators between 1.9 and 2.2 GHz. When operated as cw oscillators, typical efficiencies of 20-23% with output powers ranging from 4.5 to 5.5 W were achieved. In these experiments, the far side of the copper heat sink to which the diamond was bonded was held at about 10°C.

Several interesting and important observations have been made in these experiments. As the dc voltage is gradually increased in a pretuned circuit, a "precursor" mode to true TRAPATT operation is usually observed; significant power outputs of 2 to 3 W are measured over a relatively wide frequency band near the normal operating frequency of the TRAPATT oscillator. The spectrum of this "precursor" mode is noisy and energy output is often fairly uniformly distributed over a 100 MHz bandwidth. As the input power is increased further, a slight narrowing of the noise output is first noted and then the growth of a single signal frequency output is observed. Finally, after still further increases in input power, an abrupt change takes place. Instead of the energy content being spread over a relatively wide bandwidth, more than 99% of the output suddenly appears at a single frequency. This abrupt change need not be accompanied (unless still further increases in input

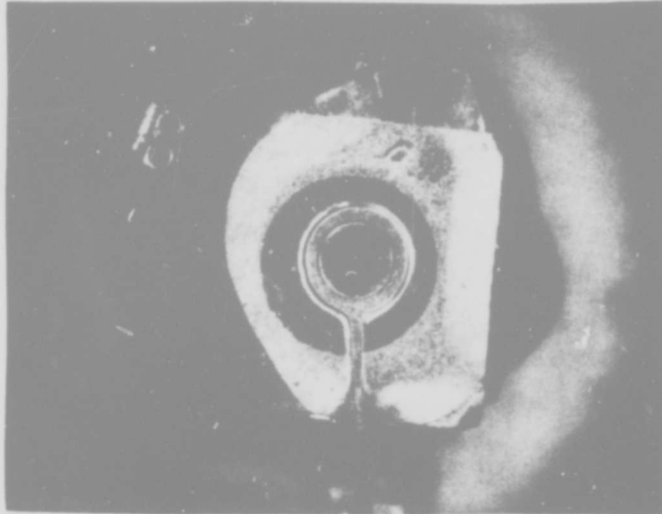


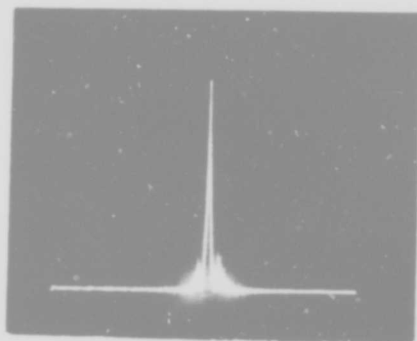
FIG. 4 Photomicrograph of ring diode mounted on diamond. Diode is actually bonded under ring tab gold preform. Circular area of sputtered gold surrounds diode. Outer portion of diamond has a gold preform bonded to it before diode is bonded to sputtered gold layer.

power are applied) by any significant output power of the device.

When the "clean signal" TRAPATT output appears, the input power density is about the same as that which would mark the onset of the TRAPATT mode under pulsed operation. Photographs of spectrum analyzer displays of the output signal of one cw TRAPATT diode are shown in Fig. 5. In Fig. 5(c), in which the spectrum analyzer dispersion is 300 kHz/div, some incidental FM on the output was observed and was found to be traceable to the power supply regulation. The spectral output of the cw TRAPATT was as clean as that of a silicon IMPATT displayed on the same spectrum analyzer.

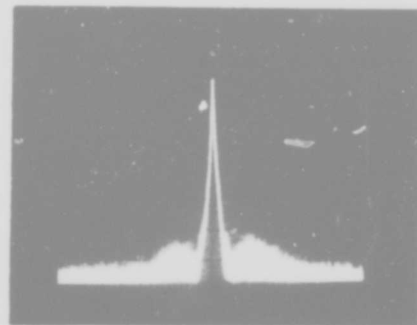
If the same devices were operated as pulsed oscillators, their efficiencies were somewhat lower than under cw conditions. This observation probably has no fundamental long range significance; however the origin of this difference is traceable to the geometry of these ring devices: the large surface area (~ 100 mil total perimeter) of the devices makes their TRAPATT performance especially sensitive to any charge residing on their surfaces. As will be discussed in detail in the following section of this report, cw operation can be useful in "improving" the devices by causing a gradual removal of undesired charge from the surface. This is almost certainly the reason why the cw efficiencies observed were higher than the pulsed efficiencies.

Conventional solid area mesas of the same material (identical diffusion, metalization, etc.) and the same active area as the cw ring diodes would oscillate (pulsed) with efficiencies in excess of 30%, a significant increase above the 20-23% observed for the ring structure. It is believed that this difference is related to the smaller surface area of the conventional mesas which makes them much less sensitive to surface effects. Further improvement in cw operation (higher output power, efficiency, wide band amplifier performance) most certainly is dependent upon reduction of the surface sensitivity of the ring structure. An extended description of this surface phenomenon is presented in the following section of this report.



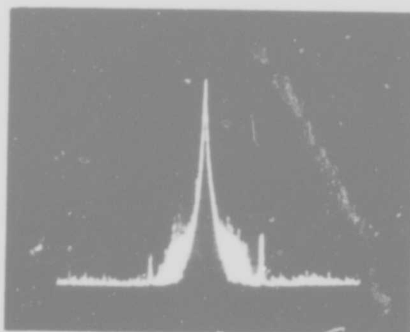
(a)

vert. = log 10 dB/cm
hor. = 10 MHz/cm



(b)

vert. = log 10 dB/cm
hor. = 3 MHz/cm



(c)

vert. = log 10 dB/cm
hor = 300 kHz/cm

FIG. 5 CW TRAPATT oscillator spectra.

f_o = 2.2 gHz
P_{out} = 5.5 W
eff = 22%
V_{BD} = 70 V
I = 350 mA

3.3 DIAMOND METALLIZATION

The metallization used to contact the diamonds was almost exclusively chromium-gold or chromium-silver; although molybdenum-gold, and tantalum-gold were also investigated. The desirable properties of a metallization layer are strong adherence, low thermal resistance and smooth structure. These properties were more readily achieved at our laboratory with chromium-gold or chromium-silver than any of the other combinations of metals, although certain precautions must be observed if the application is to be successful.

A precleaning of the diamond surface with hot sulfuric acid followed by an ultra-pure H_2O rinse proved satisfactory, and was standardly used although this step does not appear to be critical. Similarly, if the metallization is to be applied by sputtering, a sputter etching of the diamond surface prior to deposition did not appear to affect the final results.

The critical steps involved the actual deposition of about 200 Å of chromium followed by 2000 Å of silver or gold. If vapor evaporation is used then quite satisfactory results can be achieved but, unfortunately, not with complete consistency. Varying degrees of poor adhesion result fairly often. However, if good adhesion is achieved then excellent thermal impedances result when devices are bonded to the diamond.

A more reliable method of applying the metallization is to use sputtering. Excellent adhesion is attained essentially 100% of the time, but careful preparation of the chromium target is necessary for low thermal impedance layers. If the chromium target is not pre-cleaned by sputtering for a period of time at least 20 minutes immediately before the deposition, then high thermal impedances are observed (the measured thermal impedances may be as much as 20% greater than expected). The responsible agent for the higher thermal impedances is very likely a layer of chromium oxide which forms adjacent to the diamond. This layer is observed when the diamonds are reclaimed for an additional processing. A thin (~20-50 Å) grey colored layer appears on the diamond surface after the metallic chromium layer is removed by etching. This layer is essentially impervious to chemical treatment and even sputter etching and is only slightly attacked by chromium oxide etches. It is readily apparent to the naked eye and a diamond surface will lose its brilliance and white color. The only certain method of removal is by

polishing the diamond with diamond paste. The high thermal impedance produced by certain sputtered metallizations is associated with the presence of this layer. Excellent thermal impedances can be achieved with sputtered chromium layers, however, if the chromium target is precleaned properly before deposition. This lengthy precleaning requires, in practice, a well-cooled chromium target which was not available to us when sputtered layers were first applied in our laboratory.

SECTION 4

SURFACE EFFECTS

4.1 BASIC OBSERVATION OF SURFACE EFFECT

Throughout the published literature on TRAPATT devices there are no explicit references to the importance of surface effects on the TRAPATT behavior of mesa diodes. Nevertheless, a simple and fundamental relationship has been found between device performance and surface properties which indicates the surface of the diode to be of prime importance. It is a necessary condition for achieving high efficiency and low threshold that the surface of the device does not degrade under the high current state required by the TRAPATT diode.

The effects of surface degradation can be observed experimentally in the arrangement diagrammed in Fig. 6, which permits simultaneous application to the diode of a 120-cycle saw-tooth current from a curve tracer and a periodically applied pulse of much greater current amplitude which is sufficient to excite and sustain TRAPATT operation. It will be initially assumed in this experiment that the 120-cycle current is applied at levels of 50 mA peak or less, even if the device is capable of cw operation. If too large a dc current is applied, the effect to be discussed is prone to change, sometimes rapidly, with time.

The basic observation of the experiment on a nonideal diode is shown in the photograph of the curve tracer oscilloscope presentation shown in Fig. 7. In this experiment, the high current ($\sim$ 400 mA) pulse width was 1 μs at a repetition rate of 1 kHz. The resulting faint trace produced on the oscilloscope by the small duty cycle of the applied pulse was apparent to the naked eye but was not visible in the photograph because of the small dynamic range of the Polaroid film used. It is important to note that the I-V characteristics of the TRAPATT diode are quite "hard" while no high current pulses are applied: leakage currents at avalanche breakdown are often less

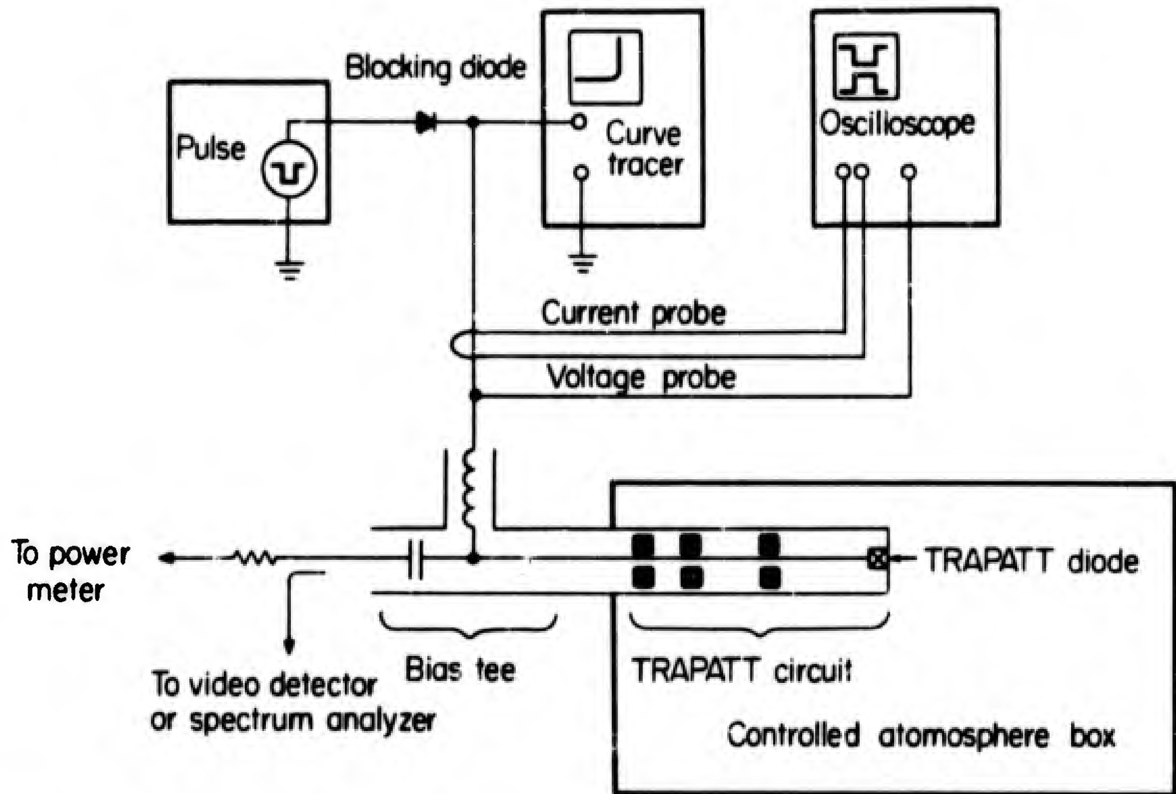


FIG. 6 Diagram of equipment used to study I-V degradation.

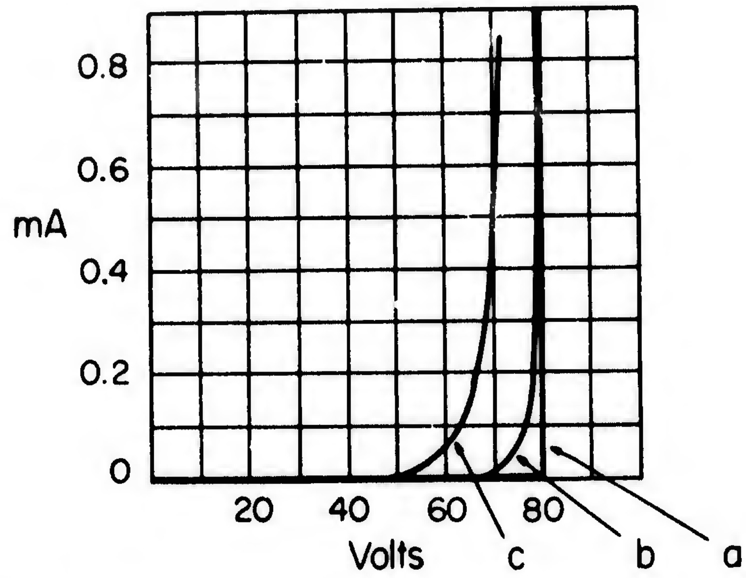


FIG. 7 I-V characteristics showing surface degradation: (a) no pulse; (b) with pulse - not in mode; (c) with pulse in mode.

than 50 nA, even for ring diodes of total perimeter equal to about 0.25 cm. Upon application of current pulses of 400 mA peak amplitude, when the device is not tuned into the TRAPATT mode, the degradation of the I-V characteristic is so significant that "rounding" of the breakdown characteristic occurs. If the pulse current through the device is left unchanged and the microwave circuit is tuned into the TRAPATT mode, a greater degradation of the I-V characteristic of the diode is produced, as shown in Fig. 7.

Any diode which shows significant I-V degradation at currents of $\leq 100\ \mu A$, which are at a level below which true bulk breakdown current begins to flow, will both be inefficient and have a high input power threshold requirement. Conversely, all diodes which have extraordinarily low thresholds or high efficiencies evidence little or no I-V degradation. These statements admit no known exceptions and are based on the analysis of data taken from devices fabricated over a three-year period. These diodes operated with fundamental TRAPATT frequencies between 1 and 10 GHz.

4.2 EVIDENCE FOR IMPORTANCE OF THE MESA SURFACE

The above description of the I-V degradation and its correlation with TRAPATT performance is not necessarily related, by any argument heretofore advanced, to the surface of the device. There are, however, several related observations which substantiate the conclusion that the surface is the critical region of the device directly related to the observed I-V degradation.

1. The final wet chemical treatment of the mesa surface is the most important single means of partially controlling the extent of the I-V degradation. For example, rinsing the device in an H_2SO_4-H_2O_2 solution immediately following mesa etching always reduces the degree of degradation. Also, all mesas etched at one time show almost identical amounts of I-V degradation, while mesas etched from the same wafer (same metallization, diffusion, etc.) at a different date or in different apparatus will often show different I-V degradations.

2. The atmosphere (relative amounts of N_2 and O_2) in which non-passivated diodes are placed will often change the I-V degradation and, hence, TRAPATT performance. High relative humidity

(> 50%) is almost always effective in increasing the I-V degradation and reducing TRAPATT efficiency.

3. A device may be repeatedly cycled through varying amounts of I-V degradation by repeated etchings followed by alternate strong oxidizing washes (H_2SO_4-H_2O_2) and HF treatments. During these successive etches, only a small fraction of a micron of the silicon surface need by removed, as was determined by capacitance bridge measurements.

4. Generally, those processes designed to affect primarily the surfaces of mesa diodes, affect the extent of the I-V degradation. For example, the application of resins commonly used to seal the surfaces of mesa diodes increases the amount of I-V degradation.

In addition, there are other observations which, though they do not prove that the surface of the mesa is directly involved, are at least consistent with the present hypothesis:

1. Removal of the high pulse voltage generally permits return of the I-V characteristic to "hard" diode conditions. The time constant for the return to hard breakdown is from tens of milliseconds to several minutes. Such time constants are 3 to 7 orders of magnitude greater than the thermal time constant of the devices. Such a long time constant is consistent with a model of trap filling. Although both bulk and surface traps could certainly be conceived as a mechanism for realizing these long-time constants, surface states can certainly be considered to be the prime candidates for such behavior.

2. Almost all devices (≥ 95%) can be improved by "training." Long periods (several hours) of pulsing or relatively short times (~ 5 minutes) of dc TRAPATT operation, can greatly increase efficiency and lower the threshold with a corresponding simultaneous reduction of I-V degradation. Often it is observed that TRAPATT operation is initially impossible at a given level of dc or pulse current; however, with continued

operation (no adjustment of either the circuit or the current level), the device will gradually go into the TRAPATT mode. This phenomenon suggests that a limited amount of surface impurities can be removed by high current operation of the device. Figure 8 illustrates the change in efficiency that resulted from continued operation along with the change in current-voltage characteristics. Improvement in efficiency by as much as a factor of 3 to 5 is not uncommon for ring diodes "trained" under dc conditioning.

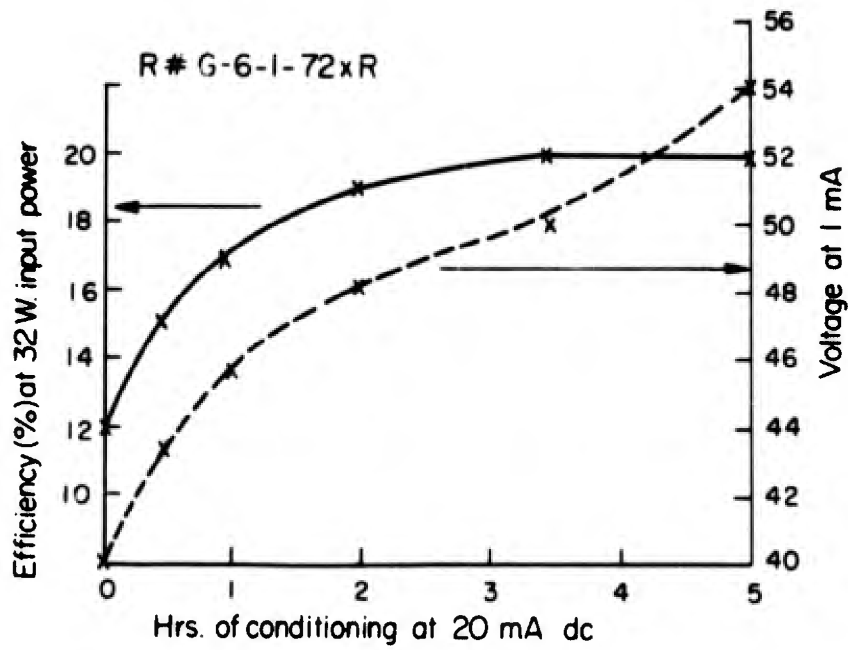
3. A given amount of I-V degradation will have a much greater effect in reducing the efficiency of a ring mesa diode than a conventional mesa diode of the same cross-sectional area. It may be reasonably supposed that the perimeter of the ring mesa, which is eight times that of the conventional mesa, is the likely reason for this effect. A much larger fraction of the total volume of the device is "near the surface" in the case of the ring diode.

4.3 METHODS OF REDUCING SURFACE SENSITIVITY

Numerous methods of reducing surface sensitivity have been examined or are currently being investigated. The major experiments are shown in Table 1.

The treatment most likely to be useful is one that can remove ions from the surface rather than just binding them in place. This is because the degradation clearly involves ionic motion since only ionic motion explains the "training" phenomenon. Since we expect that all likely applications of the device will involve local temperatures in excess of 100°C, simple covering of the device with an oxide is not sufficient since ionic conductivity in SiO_2 can become high at such temperatures.

It also has been observed that the <u>order</u> in which surface treatments are applied can affect the resulting behavior. This is illustrated in Fig. 9. Most combinations of the treatments listed separately in Table 1 were evaluated and in no case was there a net cumulative effect greater than the best result of an individual treatment.



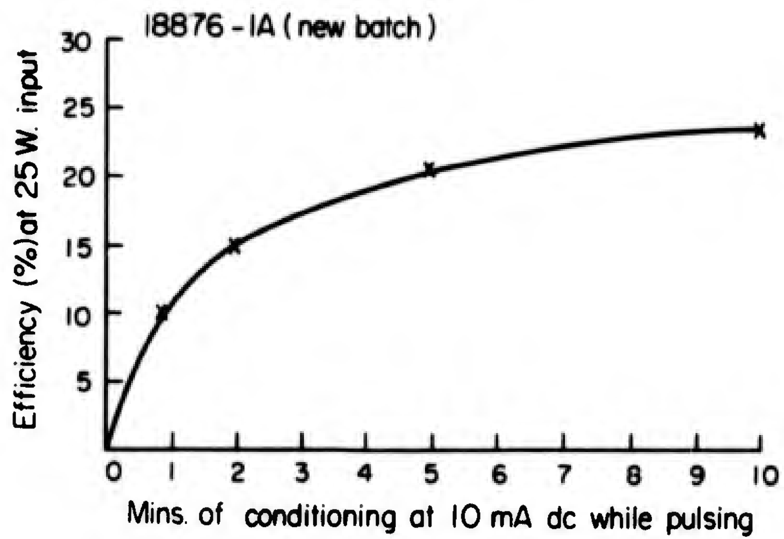


FIG. 8 Effects of dc conditioning on a ring diode.

TABLE 1

SURFACE SENSITIVITY EXPERIMENTS

TREATMENTS	RESULTS	COMMENTS
1. Training by dc current	Usually improves performance	Never (or rarely ever) completely successful
2. Electrolytically etched mesas	No change	Those were attempts to shape mesa to reduce surface fields
3. Changes in wet chemical treatments		
a. Prolonged ultra-pure wash after etching	Usually slight improvement	
b. Use of proprietary sequestering agents	No change	
c. $H_2O+H_2O_2+NH_4OH$ and $H_2O+H_2O_2+HCl$ rinses etching	slight improvement (c and d)	These are standard finishing wet treatments used in certain LSI processing
d. Drying devices after H_2O solution with alcohols	slight improvement (c and d)	
e. Wash in hot $H_2O+H_2SO_4+H_2O_2$ solution	Always improves device	Never (or rarely ever) leaves device perfect; best treatment found
f. Change constituents of etches	No effect	
4. Use of resins, elastomers and coatings commonly used to seal mesa surface	Usually degradation increases	
5. Partial test of phosphorus doped glasses to getter devices	No effect	Supposed to getter metallic ions at 400°C; have only been tested to 350°C until metallization scheme is changed.
6. Gettering of impurities from surface with HCl gas during growth of oxide on side of mesas	Partially completed evaluation	This method of gettering standard for many MOS devices. Process described in detail in next section.

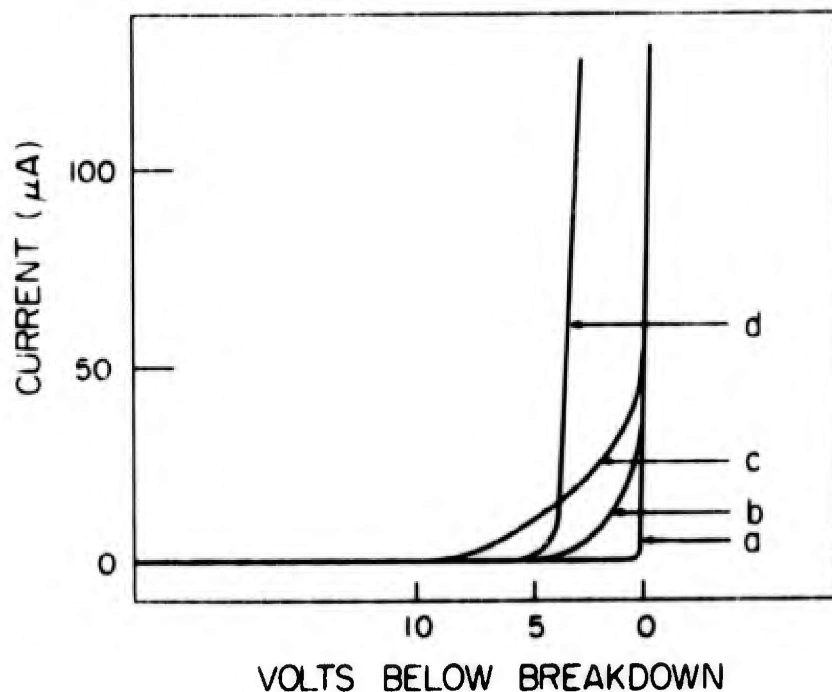


FIG. 9 Typical I-V degradation produced by different surface treatments.

a) All devices - no pulse applied.

b) Devices washed in H_2O_2-H_2SO_4 - pulse applied.

c) Devices washed in H_2O_2-HCl followed by H_2O_2-NH_4OH_4 wash - pulse applied.

d) Devices washed in H_2O_2-NH_4OH followed by H_2O_2-HCl wash - pulse applied.

4.4 HCl GETTERING AND OXIDE GROWTH ON THE MESA SIDES

One method used in MOS technology to produce stable gates with zero offset voltages is to grow the gate insulator in an HCl atmosphere. This procedure is effective either through binding metallic ions in stable compounds or by removal of the unwanted impurity by formation of volatile compounds, while forming an SiO_2 passivating layer.

Such a procedure seems to be a very attractive solution to the surface sensitivity problem of TRAPATT devices if it can be carried out. One possible configuration for such a finished device with the SiO_2 layer covering the sides of the mesa is shown in Fig. 10.

The method of producing such a mesa structure is shown in Fig. 11. Since the mesa must be first etched before the oxide can be grown, one must have some means to protect the top of the mesa from oxidization during the HCl-oxide growth on the mesa sides. No photoresist process will be useful in removing an oxide grown on the mesa top, since the mesa shape is not perfectly circular from device to device. Thus, one would either leave some oxide on the top or remove some from the side. Either situation is disastrous: the former because of the low thermal conductivity of SiO_2 (10^{-6} cm of SiO_2 would have the same thermal impedance as 10^{-2} cm of Si), and the latter because the SiO_2 layer might be removed at the junction where it is most needed.

Experimentally it has been established that the protective layer which masks against oxide growth cannot be any combination of metals. However, the use of a Si_3N_4 layer has been found to be acceptable. The Si_3N_4 can be preferentially etched by phosphoric acid, which will not significantly attack the SiO_2. The steps illustrated in the process shown in Fig. 11 have been successfully completed (application of Si_3N_4, metal masking, mesa etching, oxide growth, and Si_3N_4 removal). The final removal of the metal from the mesa sides is performed after bonding of the device. Silver is chosen for the final metal layer because it can be removed more completely than gold without risking an attack of the surrounding gold metalization on the diamond and the device contacts.

Two test runs of devices have been completed and both have stable surfaces. The first run was made of a material know to have relatively poor

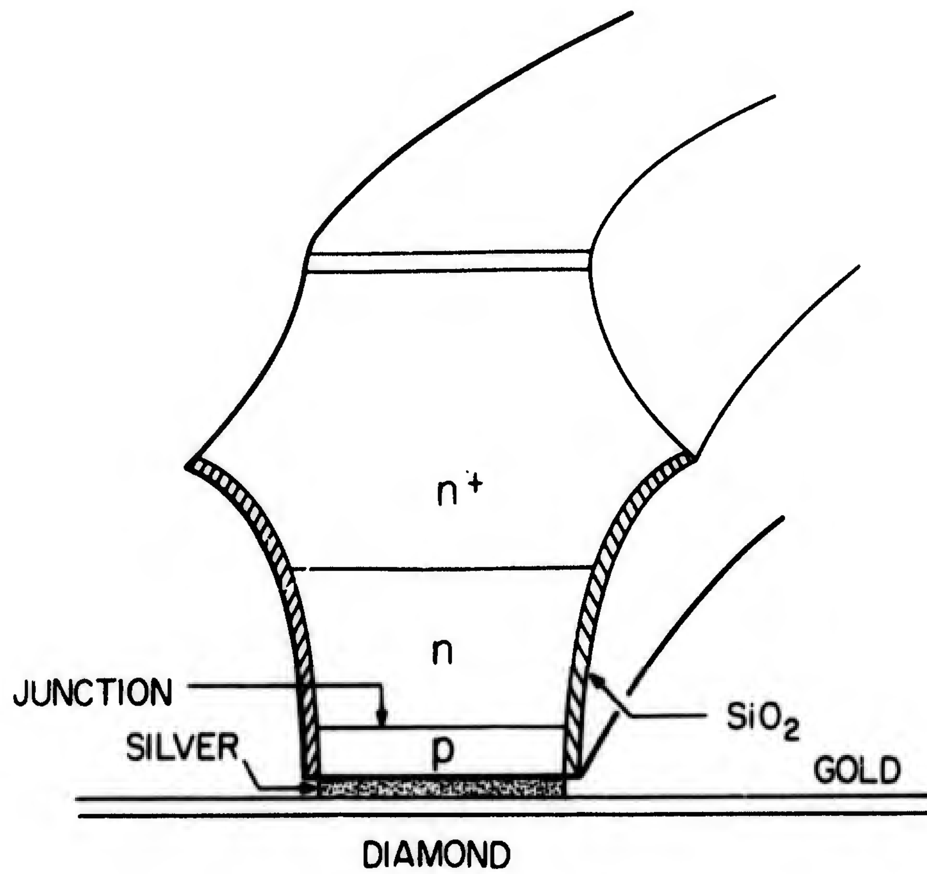


FIG. 10 Cross section of SiO_2-passivated ring diode.

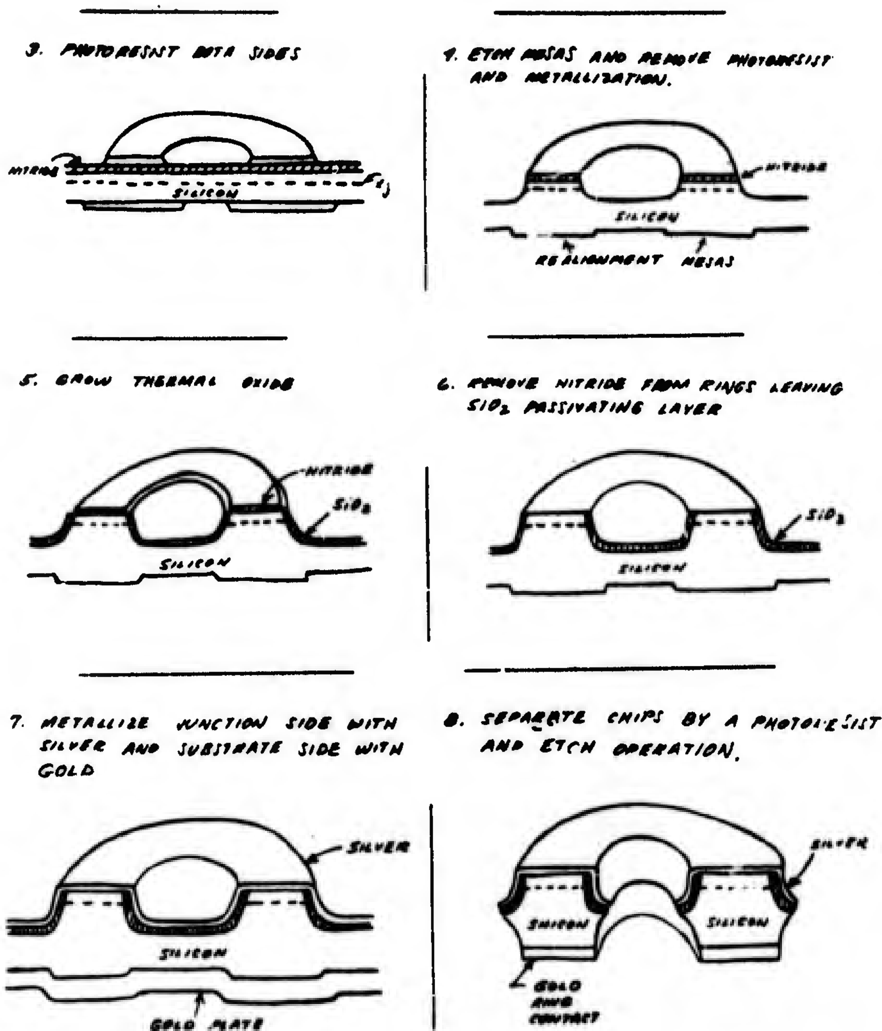


FIG. 11 Processing steps for fabricating SiO_2 passivated ring diode.

TRAPATT performance. The devices had the same breakdown voltage and similar (poor) TRAPATT performance whether or not the oxide layer was in place or had been removed by etching in buffered HF. The second attempt, on better quality silicon epitaxial layers, resulted in breakdown voltages of 14 V when the oxide was in place and 85 V when the oxide was removed. It is clear that unwanted charge was introduced into the oxide, perhaps by improper annealing. Further study of this problem is continuing.

SECTION 5

MICROWAVE CIRCUIT INVESTIGATIONS

The major efforts in circuit investigations have been in broadbanding techniques, the design of amplifiers using diodes of smaller area than those used previously, and improved biasing methods. The section dealing with broadbanding describes the progress being made on a microstrip amplifier configuration using a three-resonator, impedance-matching bandpass filter located as close to the diode as is practical. The reason for examining the use of smaller area diodes for amplifiers is basically one of lower threshold and, hence, a better opportunity for cw amplifier operation. Results achieved on a pulsed basis on diodes as small as 0.35 pF at voltage breakdown are described. The improved biasing methods are concerned with improvements in oscillator and amplifier efficiencies. The description of the circuit and the results achieved are described.

5.1 WIDEBAND AMPLIFIER

The bandwidth of the prototype wideband amplifier can be improved by replacing the lowpass filter with an impedance-matching bandpass filter located as close to the diode as is practical. The filter is designed to give a prescribed midband gain and bandpass ripple. Design procedure and experimental results are described in the following section. In the Appendix a generalized design procedure for TRAPATT amplifiers is presented.

5.1.1 Design Procedure

The design procedure assumes the TRAPATT amplifier can be represented by an equivalent circuit comprised of a negative resistance and a lossless reactive interconnecting network. The circuit elements which represent the active semiconductor elements are the negative resistance, the depletion layer capacitance, and an electronic reactance. The design of

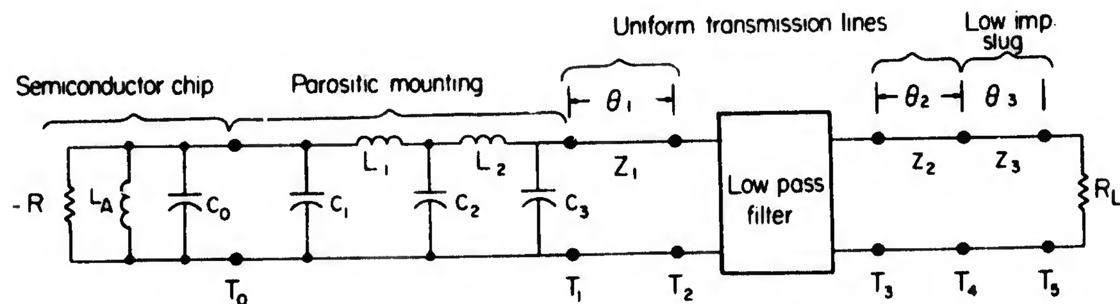
multiple device mountings can be included within this design procedure by introducing the interconnection parasitics between adjacent devices.

The large-signal equivalent circuit for the prototype TRAPATT amplifier, as determined from impedance measurements on the experimental amplifier, is shown in Fig. 12. The negative resistance -R, the electronic inductance L_a, and the capacitance C_0 are the large-signal equivalent parameters of the active semiconductor chip. The capacitance C_0 represents the equivalent depletion layer capacitance of the chip, and the inductance L_a represents the electronic reactance due to the impact ionization process. The magnitude of the negative resistor -R is calculated from measurements of amplifier gain and load impedance at the terminals of the semiconductor chip. The circuit elements C_1, C_2, C_3, L_1, and L_2 represent the parasitic reactances introduced in mounting the diode. These parasitic elements form the major portion of the TRAPATT amplifier circuit. The short section of the uniform transmission line and the lowpass filter provide a small amount of time delay triggering (TDT) enhancement necessary for TRAPATT amplification. The slug Z_3 of length θ_3 is positioned a length θ_2 from the lowpass filter so as to resonate the diode at the fundamental output frequency ω_0.

The gain and bandwidth of the experimental amplifier are determined by the Q of the network and the value of the load resistance. For the prototype broadband amplifier, the circuit Q at the output terminals T_5 was calculated to be -37.50. The 3 dB bandwidth was 275 MHz and the 1 dB bandwidth was 102 MHz. If it is possible to realize a TRAPATT amplifier having T_2 as the accessible terminals, the negative Q would be reduced to 22.5 and the corresponding 3 dB and 1 dB bandwidths would increase to 424 and 170 MHz respectively. The computer calculated passband response of the amplifier is shown in Fig. 13.

The 1 dB bandwidth of the amplifier can be further increased by the use of broadbanding techniques developed by Getsinger[3] for reflection-type negative resistance amplifiers. This technique involves the use of prototype impedance-matching filters to shape the bandpass characteristics of the amplifier.

A bandpass impedance-matching filter is chosen rather than a lowpass filter. The terminals T_2 are chosen as a reference plane rather than the terminals T_5 in order to obtain the lowest possible negative Q (Fig. 12).



$-R = 8\ \Omega$
$L_A = 0.5$ nHy
$C_j = .4$ pF
$C_1 = .09$ pF
$L_1 = 2.5$ nHy
$C_2 = .55$ pF
$C_3 = .045$ pF
$\theta_i = 1.0'$
$Z_1 = 61.1\Omega$
$Z_2 = 61.1\Omega$
$Z_3 = 17\ \Omega$
$\theta_3 = 0.6''$
$R_2 = 50\ \Omega$

Gain = 5 dB

at terminal T_5 $Q_5 = -37.4$
Bandwidth 3 dB = 275 MHz
1 dB = 102 MHz

at terminal T_2 $Q_2 = -22.5$
Bandwidth 3 dB = 424 MHz
1 dB = 170 MHz

FIG. 12 Large-signal equivalent circuit for prototype wideband TRAPATT amplifier.

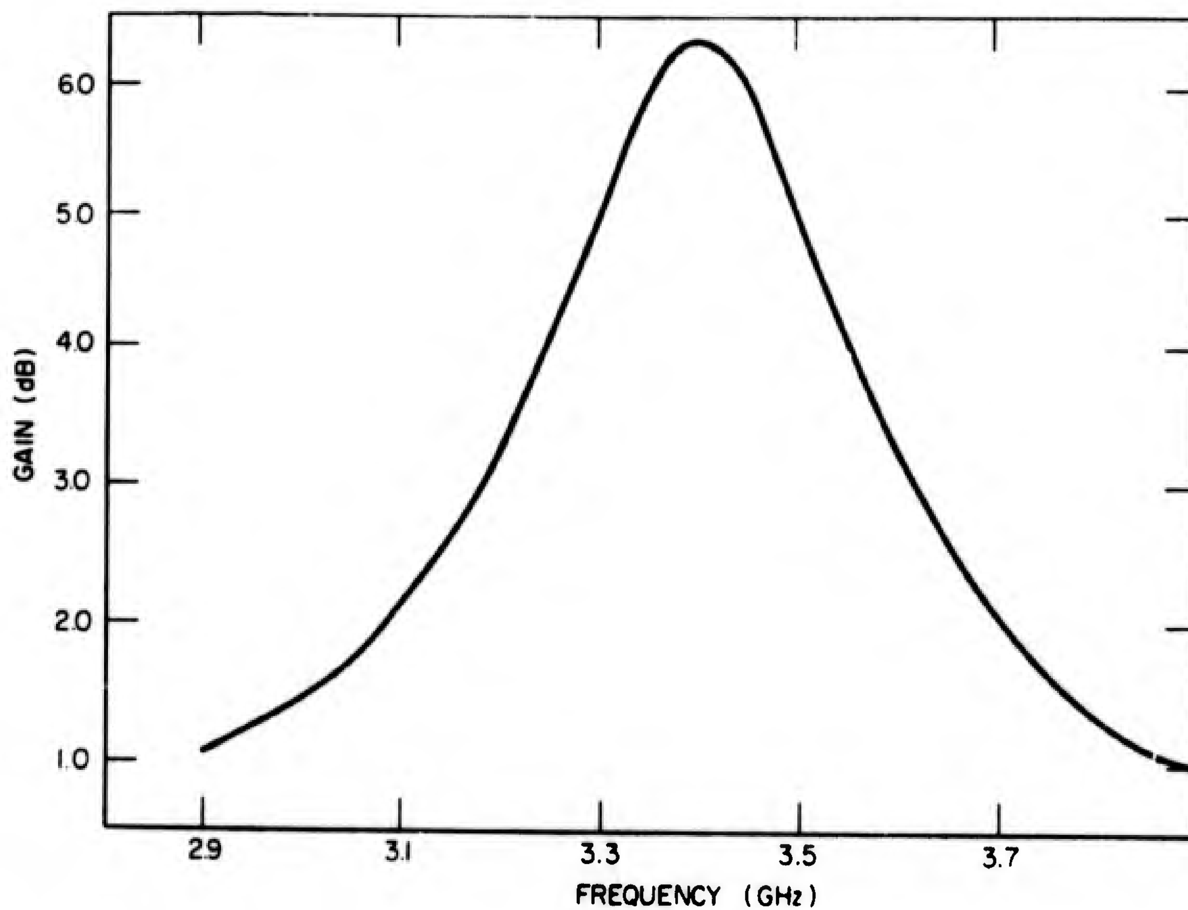
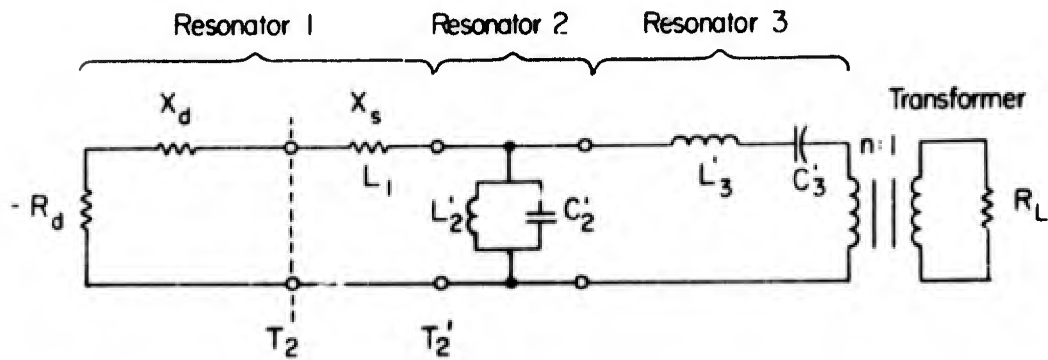


FIG. 13 Computer-calculated passband response of TRAPATT amplifier referenced at terminal T_2.

The equivalent circuit of the amplifier, including matching transformer, is shown in Fig. 14. The negative resistor R_d and the reactance X_d are the equivalent circuit resistance and reactance measured at terminals T_2. An external series reactance X_s is added to resonate the amplifier at the required operating frequency. Figure 15 shows the absolute value of both the real and imaginary parts of the impedance seen to the left of terminals T_2 (Fig. 12 For this particular S-band prototype amplifier, the external series reactance X_s was an inductor of 0.48 nH. The real part of the impedance is relatively constant over the band of interest and lumped element equivalent circuit techniques can be used.

The lowpass filter of the prototype amplifier is replaced by a two- or three-resonator bandpass filter whose values are chosen to give a specific bandpass amplifier response. The circuit elements of the bandpass filter are shown schematically as lumped element inductors and capacitors. However, these elements may not be realizable in this form. If so, impedance and admittance inverters[4] may be used. The transformer T is used to present the proper load resistance for the required gain. The improvement in amplifier performance is illustrated by the computer-generated passband response shown in Fig. 16. For this case, a 5 dB gain, 0.5 dB ripple, three-resonator circuit design was used. The 1 dB bandwidth is in excess of 500 MHz. The slight response asymmetry is due to differences in the values of the negative resistance presented to the matching filter at the band edges. It is difficult to realize the circuit elements required for a given bandpass amplifier response. These elements must be frequency invariant up to and including at least the third harmonic in order that the triggering waveforms will be maintained. For the wideband amplifier design shown in Fig. 16, resonator 2 is a 0.179 nH inductor in shunt with a 12.234 pF capacitor. This requires the use of a short length of wire in parallel with a lumped element capacitor. Because of the small values of inductance and, hence, the short section of small-diameter wire, MOS capacitors have to be used. A schematic of a microstrip version of amplifier is shown in Fig. 17. The ring diode is mounted upon a diamond heat sink. A short wire whose length and diameter is chosen to yield the required inductance L_1 and distributed capacitance C_1 is connected from the diode to the lumped capacitor C_3. A second short section of wire, whose size is chosen to correspond to L_3 and C_3, is connected between the



L_1 = 0.48 nHy

L'_2 = 0.179 nHy

L'_3 = 3.379 nHy

C'_2 = 12.234 pF

C'_3 = 0.647 pF

R_L = 50 Ω

n ≅ 2

Gain 5 dB ripple 0.5 dB

FIG. 14 Equivalent circuit for wideband TRAPATT amplifier referenced at terminal T_2.

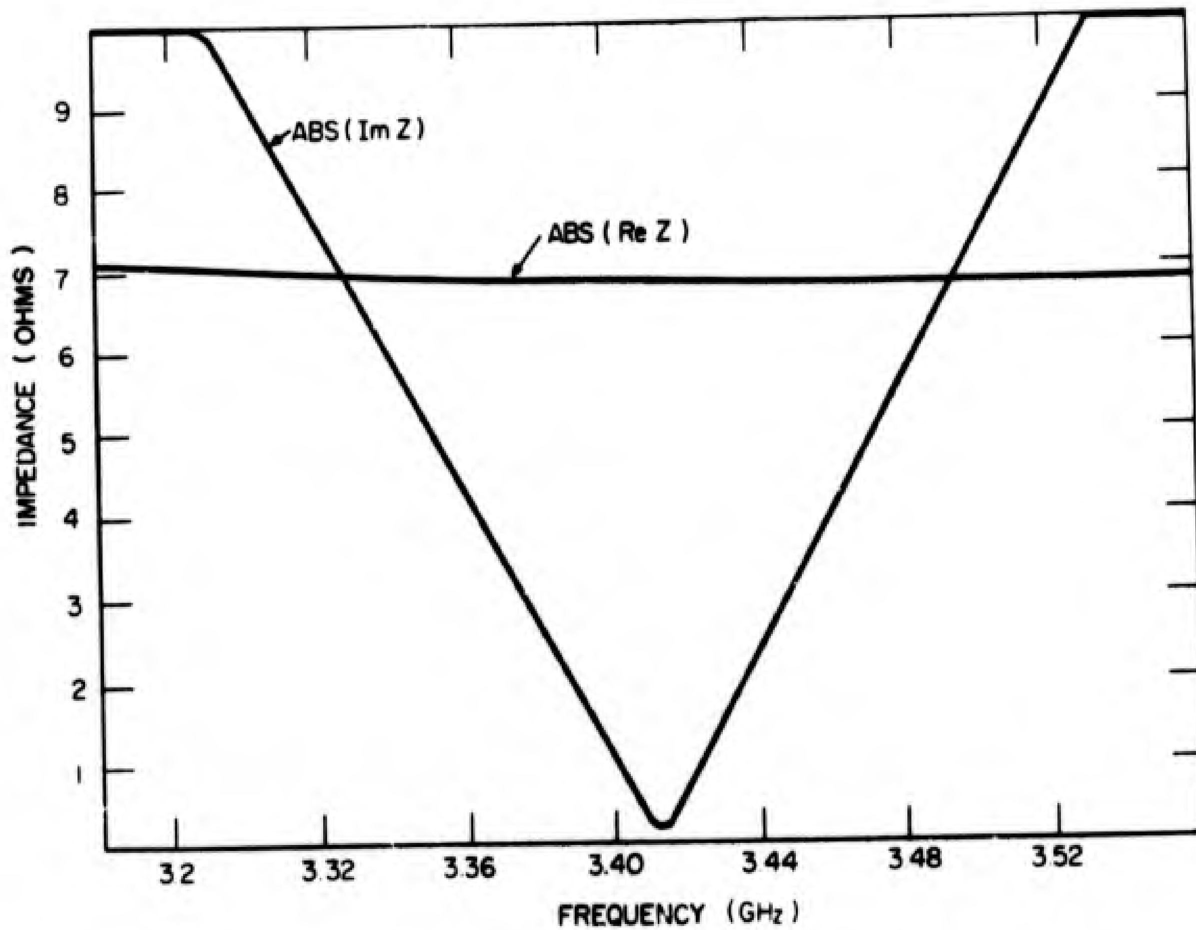


FIG. 15 Absolute value of the diode resistance and reactance referenced to terminal T_2 including the added inductance L_1.

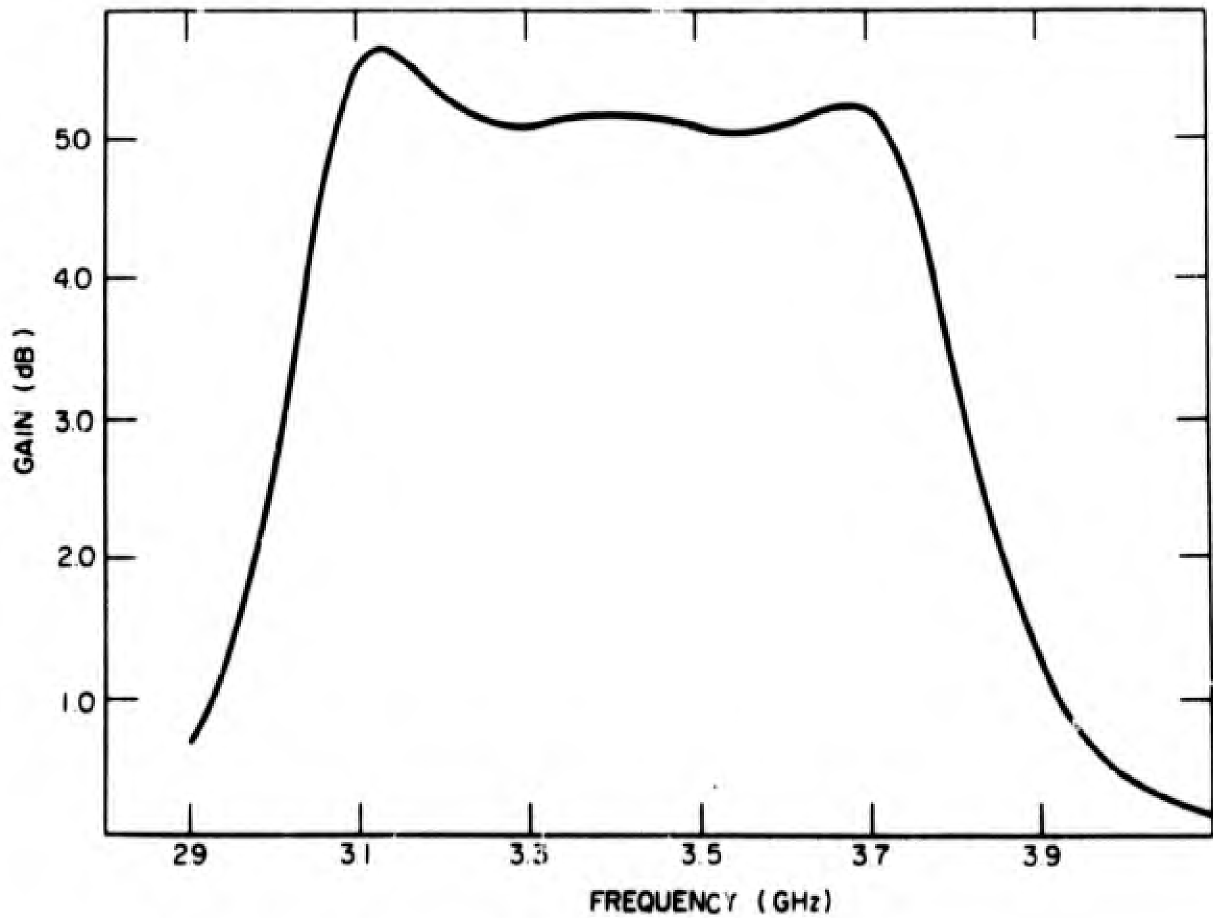
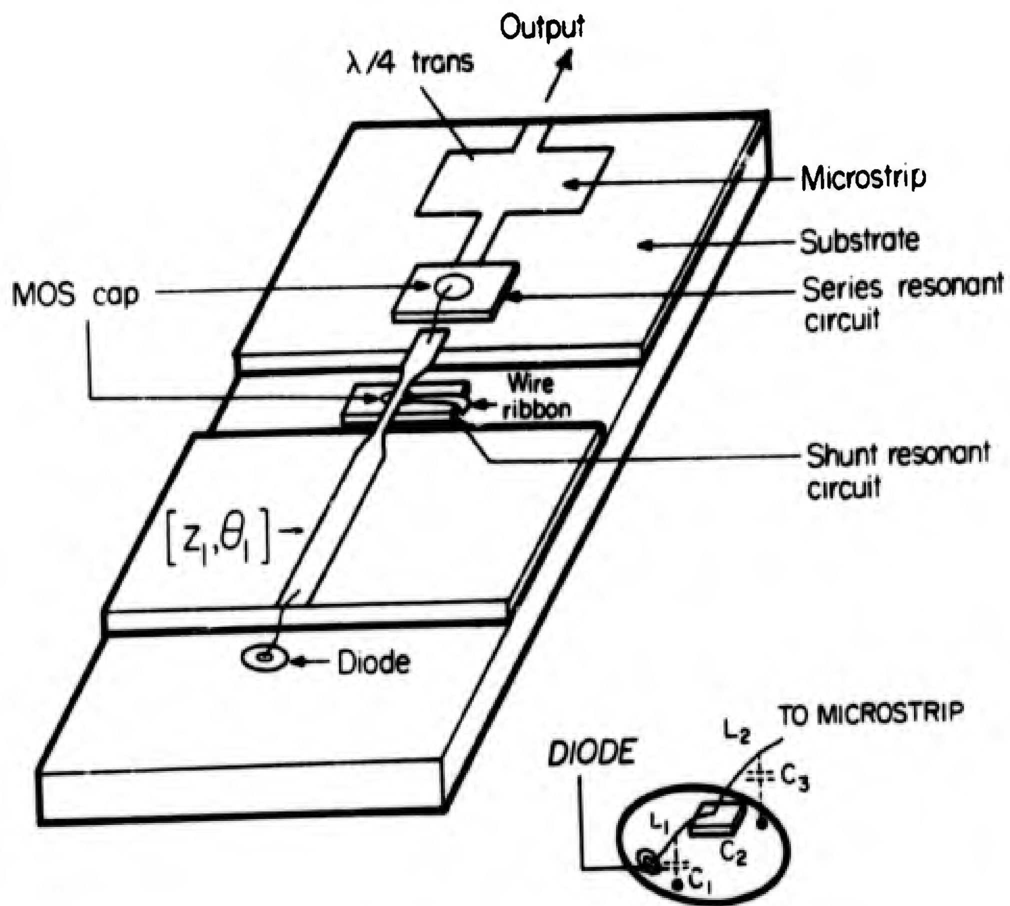
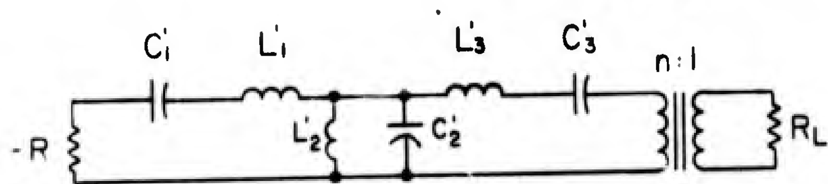


FIG. 16 Computer-calculated bandpass response of wideband TRAPATT using a 3-resonator impedance matching filter designed for 5 dB midband gain and 0.5 dB ripple





$-R \sim 6\ \Omega$ n:2 $R_2 = 50\ \Omega$

$C'_1 = 0.332$ pF $L'_1 = 6.576$ nHy   Gain ~ 5 dB

$C'_2 = 12.234$ pF $L'_2 = 0.179$ nHy   1 dB bandwidth 620 MHz

$C'_3 = 0.647$ pF $L'_3 = 3.379$ nHy

FIG. 17 Schematic of improved bandwidth microstrip amplifier circuit.

capacitor and the short section of microstrip transmission line (Z_1, θ_1). The shunt resonator 2 is comprised of an MOS capacitor and a wire ribbon inductor. The second series resonator 3 is also formed by using MOS capacitors and a short section of wire. The quarterwave transformer T transforms the load resistor to the proper value for the required gain. The use of the bandpass filter will not affect the triggering waveform because, at the harmonic frequencies, resonator 2 of the bandpass filter presents a very low impedance to the diode in a manner similar to that of the lowpass filter (above its cutoff frequency) used in the prototype amplifier. This is illustrated in Fig. 18, which shows the computer-generator triggering waveform as a function of frequency. This does not include any effect due to an externally applied signal. The waveforms are similar to those obtained using the lowpass filter. The gain value chosen for the proposed amplifier was 5 dB, to maximize the bandwidth; however, higher gain designs have been generated using the computer-aided broadband design techniques.

A computer calculation of the gain and phase response for the proposed improved bandwidth amplifier is shown in Figs. 19 and 20. The gain response is for an 8 dB midband gain amplifier having a 0.05 dB passband ripple. The gain variation over the required frequency band is due to the frequency sensitivity of the negative resistance, as referenced to the input terminals of the impedance-matching bandpass filter. The total gain variation is ±0.5 dB and can be reduced by changing the resonant frequency of the shunt-tuned resonator.

The computed phase response for the amplifier is shown in Fig. 20. The phase deviation from linear is due to use of the three-resonator impedance-matching network. An improved phase response having a much smaller deviation from linear can be obtained by using a greater number of resonators.

The broadbanding technique described here has been used successfully with many types of negative resistance amplifiers, and, provided the triggering waveforms are unchanged over the frequency band of interest, it will be successful with TRAPATT amplifiers. It should be stressed that the improvement in the 1 dB bandwidth is accomplished by multiple tuning at the fundamental frequency. This technique does not affect the harmonic impedances which control the triggering waveform. Further improvement can only be accomplished by broadbanding the harmonic impedances.

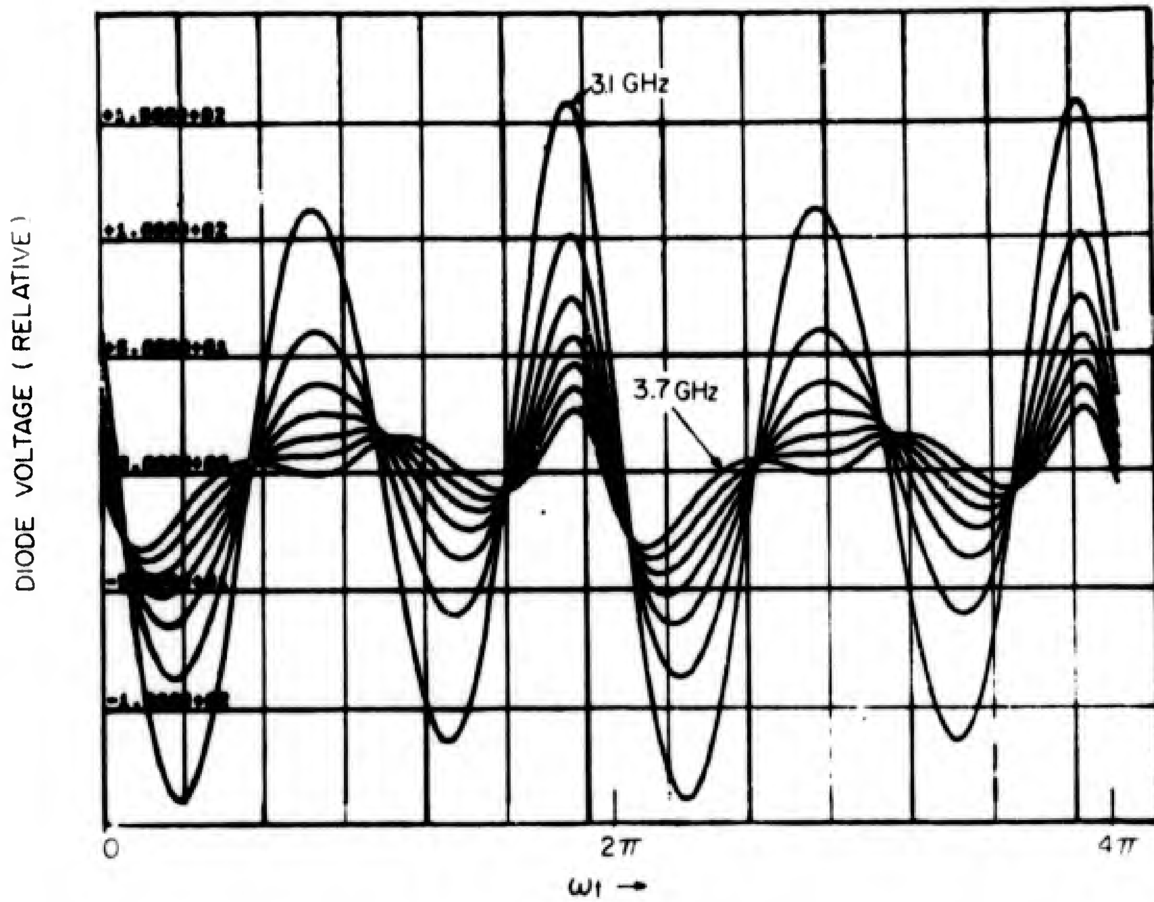


FIG. 18 Computer-generated triggering waveform for improved bandwidth amplifier.

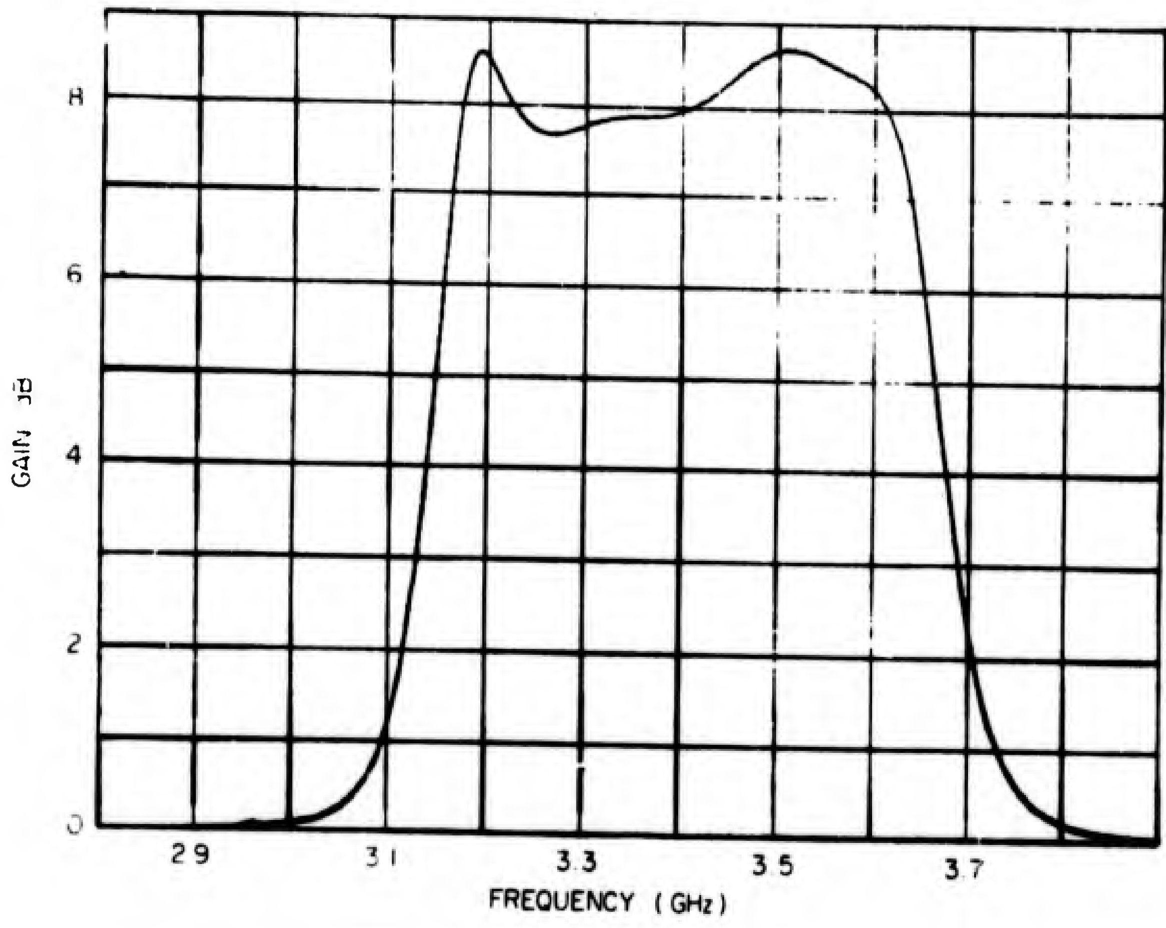


FIG. 19 Computer calculation of the passband of an 8 dB gain, 0.05 dB ripple amplifier stage.

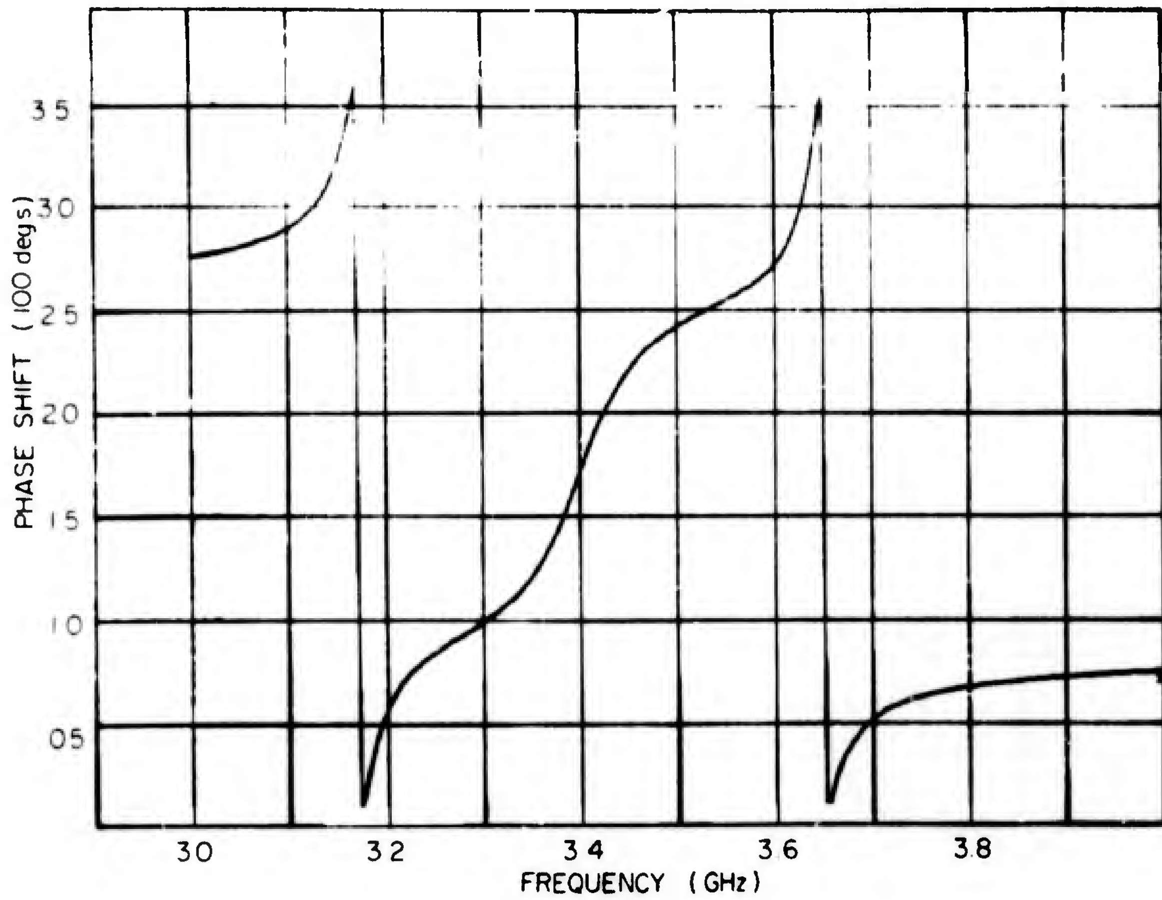


FIG. 20 Computer-calculated passband phase response for a 3-resonator impedance matching filter.

5.1.2 Experimental Wideband Amplifier

An experimental wideband amplifier was constructed in microstrip using the design criteria described in Sec. 5.1.1. The amplifier design was based upon the use of two tuned resonators for broadbanding. The equivalent circuit for the amplifier is shown in Fig. 21. The computer calculations required that the shunt resonator have a slope reactance that corresponds to a capacitance of 10 pF and an inductance of 0.46 nHy. Attempts to realize a high Q shunt resonance using 10 pF MOS capacitors obtained from Frequency Sources Corporation of Chelmsford, Massachusetts were unsuccessful. It is believed that the Q of the capacitors when used in a shunt resonant circuit is much lower than the advertised value. A sufficiently high Q resonant circuit was achieved using 1 pF MOS capacitors. Even though this value of capacitance will not theoretically yield a wideband amplifier response, a prototype amplifier was fabricated to determine if the wideband amplifier circuit configuration would indeed work. A photo of the prototype amplifier is shown in Fig. 22. TRAPATT amplification was obtained at a frequency of 2.5 GHz. A photograph of the bandpass of the amplifier is shown in Fig. 23. The centerband gain was 5 dB and the 3 dB bandwidth 90 MHz. The efficiency was 17%. The frequency of operation was lower than the design frequency of 3.0 GHz, and is due to the addition of the parasitic reactances introduced in the mounting of the MOS capacitor and the shunt inductor. The bias was applied to the diode via the rf bypass capacitor located at the diode mount.

It is believed that, with higher Q MOS capacitors, the theoretical bandwidth for wideband amplifiers can be realized.

5.2 SMALL-AREA DIODE AMPLIFIERS

In the prototype (14 mm coax) amplifier, the diodes used have a nominal depletion layer capacitance at voltage breakdown of 0.5 pF. Recent experiments on oscillators and narrowband TDT amplifiers have given results showing lower input power thresholds for smaller area devices. This feature is important in achieving cw broadband amplification in that the high-efficiency mode can be initiated at a lower diode thermal dissipation level. From the viewpoint of practicality of fabrication, the smallest diodes that can be made using our 3.5 GHz amplifier material have a $C_j \sim 0.35$ pF at voltage breakdown. These diodes, operated as oscillators in the 2 GHz region,

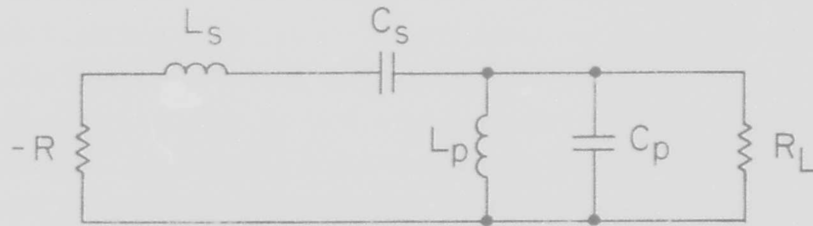


FIG. 21 Equivalent circuit of two resonator wideband amplifier.

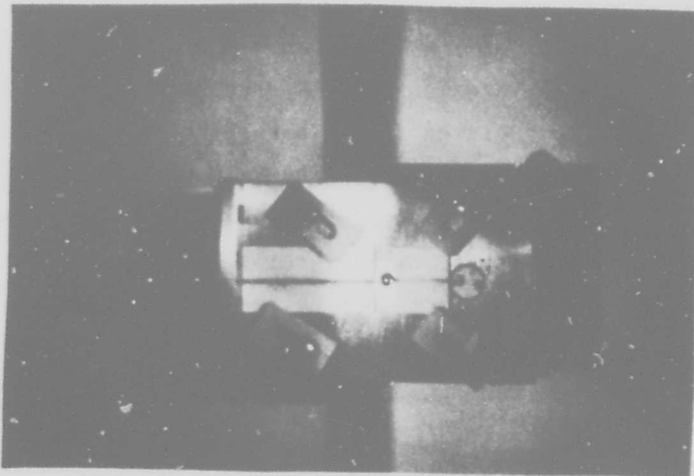


FIG. 22 Photograph of two resonator wideband amplifier.

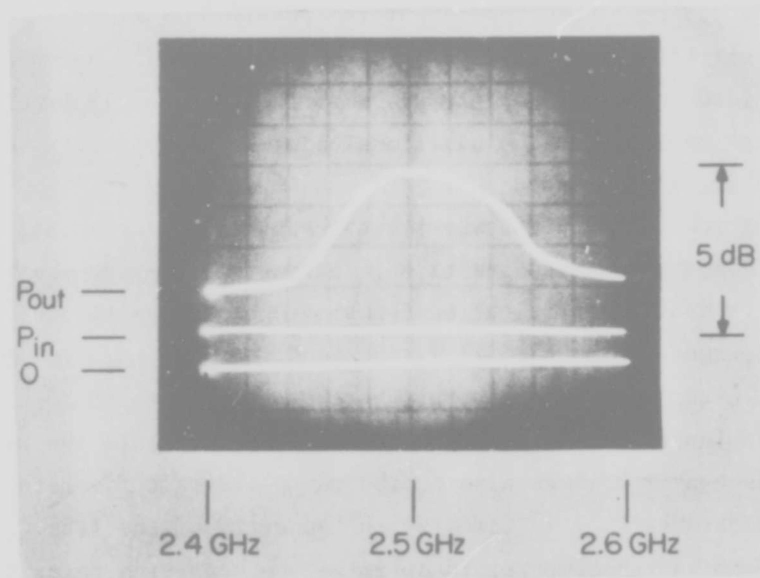


FIG. 23 Bandpass response of two resonator wideband amplifier.

exhibited reduced threshold levels; hence, an amplifier design was started using a diode with a $C_j = 0.35$ pF and the package parasitics normally used with a $C_{j(VBD)} = 0.5$ pF diode. Using our computer program, which calculates the triggering waveforms and the network characteristics, it was found that this combination would result in a triggered oscillator at approximately 3.2 GHz. This result was verified experimentally. In constructing coaxial amplifiers, we had been concerned about the possibility of higher order moding in the 14 mm circuit, particularly at the second and third harmonics. It was therefore decided to perform all future work in this area in precision 7 mm coax. This choice also has the additional advantage of yielding more accurate network analyzer measurements.

A series of computer experiments was then performed, attempting to optimize the diode parasitics and circuit parameters. Since the most critical constraint on wideband amplification appears to be the existence of an open circuit at the second harmonic, it was decided that the parallel resonance of the parasitic circuit (Fig. 24) should be the same for the 0.35 pF junction as for the 0.5 pF junction. In addition, as a starting point, the parasitic series resonance near $3f_0$ was also chosen to be the same for both area diodes. The corner inductance (L_C) is fixed by the geometry of the line. An attempt was then made using the computer to optimize the remaining parasitics, the lead inductance (L_C), and the package capacitance (C_P). The results of this analysis are:

	C_J(pF)	C_P(pF)	L_R(nH)	L_S(nH)
Large-area junction	0.5	0.59	0.53+	1.9
Small-area junction	0.35	0.7	0.42*	2.2

\+ - 14 mm coaxial line

* - 7 mm coaxial line

A second series of computer runs was then performed varying five of the amplifier circuit parameters (Fig. 25): (1) the characteristic impedance (Z_ℓ) of the line between the diode and the lowpass filter; (2) the electrical length (θ_ℓ) of the same line; (3) the characteristic impedance of the tuning

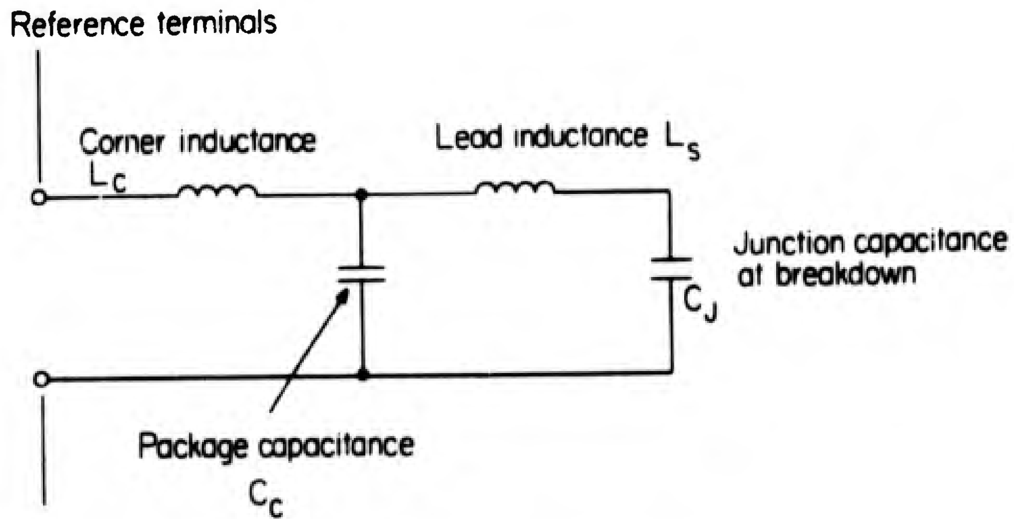


FIG. 24 Diode parasitic circuit model.

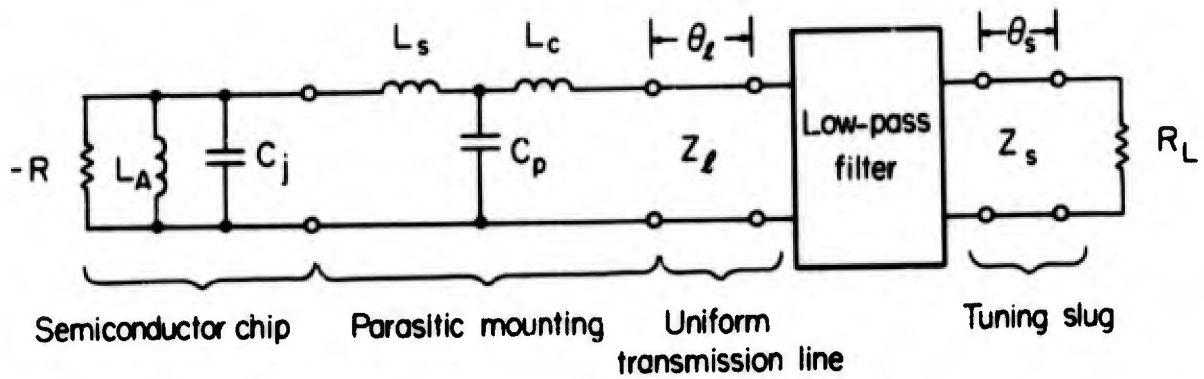


FIG. 25 Large-signal equivalent circuit model for small-area diode wideband TRAPATT amplifier.

slug (Z_S); (4) the electrical length (θ_S) of the tuning slug; (5) the position of the tuning slug. The criteria for optimization used for the computer analysis were: (1) bandwidth of triggering waveforms; (2) circuit response; (3) flatness of the real part of the impedance seen by the diode; (4) linearity of the phase response of the network; and (5) efficiency. In keeping with results achieved on the prototype amplifier, a centerband gain of 6 dB was chosen.

It was found that by increasing the impedance of the line between the diode and the lowpass filter from 62 to 70 Ω and by slightly shortening the line length from 1.040 to 0.960 inches, only small tuning slug changes were necessary. This resulted, at least analytically, in a small-area diode amplifier having essentially the same gain-bandwidth product as the prototype 14 mm coaxial amplifier.

Rather than attempt to use any fixed diode package, the diode was thermocompression bonded to a gold-plated copper puck, and the parasitic circuit was fabricated from lengths of 1 mil diameter gold wire as inductors, and a thin Al_2O_3 ceramic metalized on opposite broad sides as the "package" capacitor.

When the experimental amplifier was assembled and tested, the results were encouraging but not exactly as anticipated. The gain, efficiency, and centerband frequency agreed quite well with the computer predictions. However, the measured bandwidth of the amplifier was only 50 mHz while the calculated bandwidth was in excess of 200 mHz. In addition, the circuit tuning was very critical.

A careful examination of the various experimental measurements made on the diode showed discrepancies in the diode small-signal equivalent circuit measurements. These variations were traced to reference terminal problems, thus making network analyzer measurements inaccurate. The problem has been corrected and the entire small-area broadband amplifier design is being reiterated.

5.3 IMPROVED BIAS NETWORK

This section describes an improved bias circuit for TRAPATT amplifiers and oscillators. In general, TRAPATT amplifiers and oscillators are biased using networks which are dc coupled to the semiconductor device and do

not affect the impedance as seen by the semiconductor device at the operating and harmonic frequencies. The bias circuit described in this section, however, allows one to control the impedance at the even harmonics in such a manner as to improve the dc to rf conversion efficiency of oscillators and amplifiers and/or to decrease the dc input power necessary for TRAPATT operation.

Most TRAPATT oscillators and amplifiers are operated using bias circuits of the type shown in Figs. 26a and b. In Fig. 26b, the bias to the semiconductor device is applied through an inductive input low pass filter. The operating frequency of the device is chosen to lie within the stop band of the filter. The input impedance of the filter at the operating frequency and its harmonics does not contribute to the required load impedance for TRAPATT operation; e.g., the input impedance at the bias network is an open circuit at all frequencies of interest. The bias arrangement shown in Fig. 26b uses a capacitor input low pass filter whose impedance is small in comparison to the load impedance at all important frequencies and therefore can be neglected.

The improved bias circuit is shown in Fig. 27a. The short circuit behind the diode is replaced by half wavelength folded choke. The equivalent circuit is shown in Fig. 27b. The sections of transmission line Z_1 and Z_2 are both electrically $\lambda/4$ long at the operating frequency f_0. The characteristic impedances of lines Z_1 and Z_2 are a function of the choke dimensions and are less than the characteristic impedance (50 Ω) of the main transmission line. The transmission line Z_2 is a $\lambda/4$ long, shorted section in series with line Z_1. At the frequency f_0 and at all odd harmonics $(2n-1)f_0$, the short at terminal plane $T_2{}^1$ is transformed to an open circuit at reference plane $T_1{}^1$-T_2. This open circuit impedance is in series with the impedance at terminals T_2. The net impedance at $T_1{}^1$ is therefore an open circuit and is transformed to a short circuit at plane T_1 by the $\lambda/4$ section of transmission line. Thus the input impedance at terminals T_1 is a short circuit at f_0 and all odd harmonics, independent of the impedance at terminals T_2.

At the even harmonics (nf_0), the short circuit at terminals $T_2{}^1$ is transformed to a short circuit between terminals $T_1{}^1$ and T_2. Thus the impedance at terminals $T_1{}^1$ is the same as the impedance at terminals T_2. The input impedance for the even harmonics at terminals T_1 is the same as that at terminals T_2. Therefore, one can independently control the second harmonic impedance to improve TRAPATT performance.

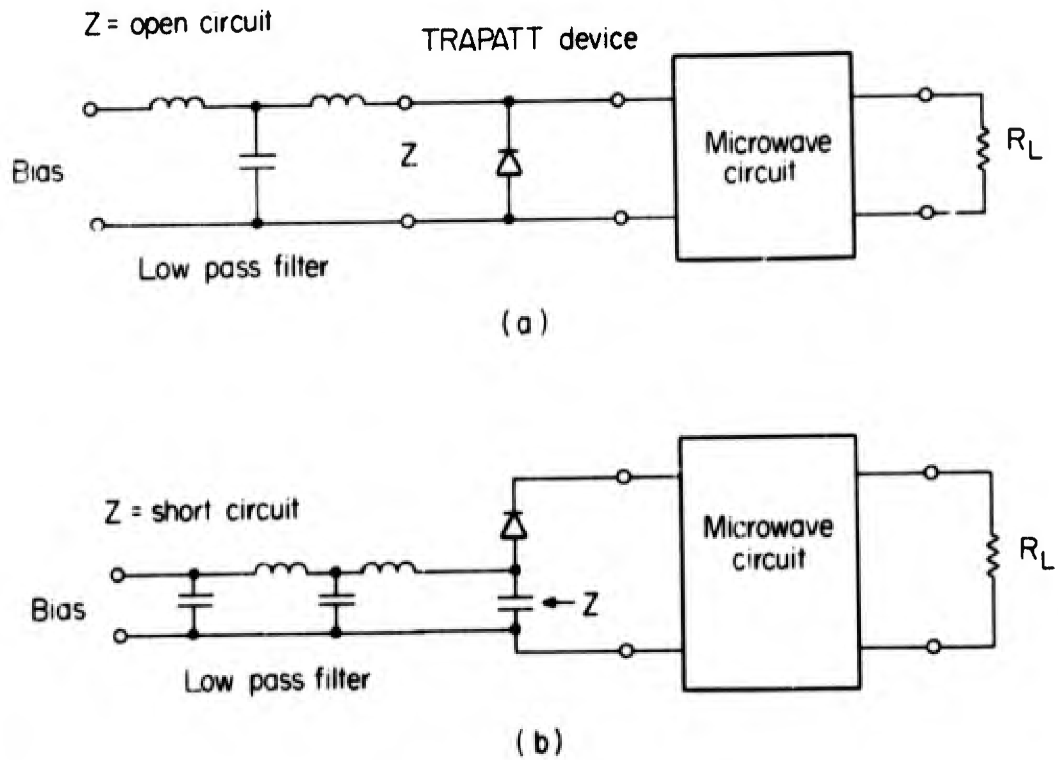
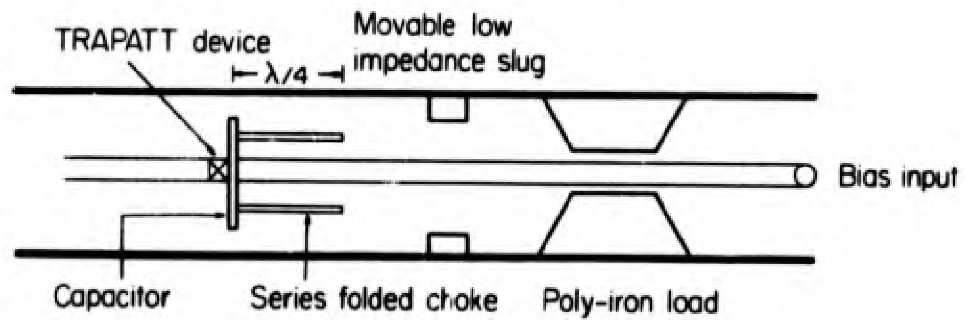
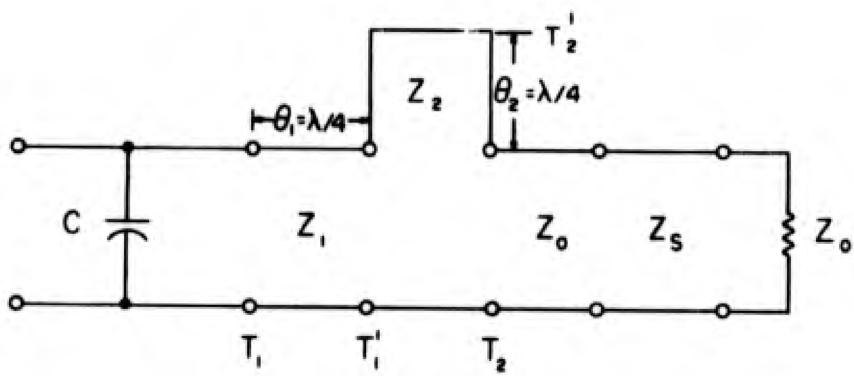


FIG. 26 Conventional bias circuits
(a) Inductive input low pass filter
(b) Capacitive input low pass filter



(a)



(b)

FIG. 27 Folded choke bias circuit
(a) cross sectional drawing
(b) equivalent circuit

The capacitive disc at the input to the folded choke guarantees that the device is terminated by a low impedance for all harmonics greater than the fourth harmonic. It may also serve as a source of charge necessary for the excitation of the avalanche shock front required for TRAPATT operation.

The equivalent circuit for the TRAPATT oscillator at the operating frequency f_0 and the harmonic frequencies 2 f_0 and 3 f_0 is shown in Fig. 28. At the frequencies f_0 and 3 f_0, the impedance Z is a short circuit, and the terminal impedance ($Z_T = Z_L$) presented to the TRAPATT device is the load impedance Z_L, the same as in the conventional TRAPATT circuit. At the second harmonic, 2 f_0, the terminal impedance presented to device is the sum of the load impedance Z_L and the impedance Z (2 f_0) due to the folded choke circuit. It is possible to adjust the impedance Z (2 f_0) to be any value by varying the length and the impedance of the slug Z_c (Fig. 29). The effect of varying the position of the slug Z_c is shown in Fig. 27. This shows the second harmonic impedance of Z (2 f_0) as a function of slug position for a given slug length and impedance.

The equivalent circuit of the folded choke bias circuit at frequencies between dc and the operating frequency f_0 is shown in Fig. 30. The capacitance C_f and the inductance L_f represent the low frequency equivalent circuit for the $\lambda/2$ folded choke. The distributed resistance R_m and distributed capacitance C_m represent the equivalent circuit for the polyiron load. At all frequencies of interest (f_0 and its harmonics), the polyiron load behaves as a matched lossy transmission line. At the bias frequencies, the polyiron load is transparent and there is no dc power dissipated in the polyiron. The use of the improved bias circuit in the wideband amplifier has resulted in typical increases of efficiency from 17% to 23%. Increased gain (from 6 to 9 dB) has also been observed; however, no improvements in the gain-bandwidth product were achieved.

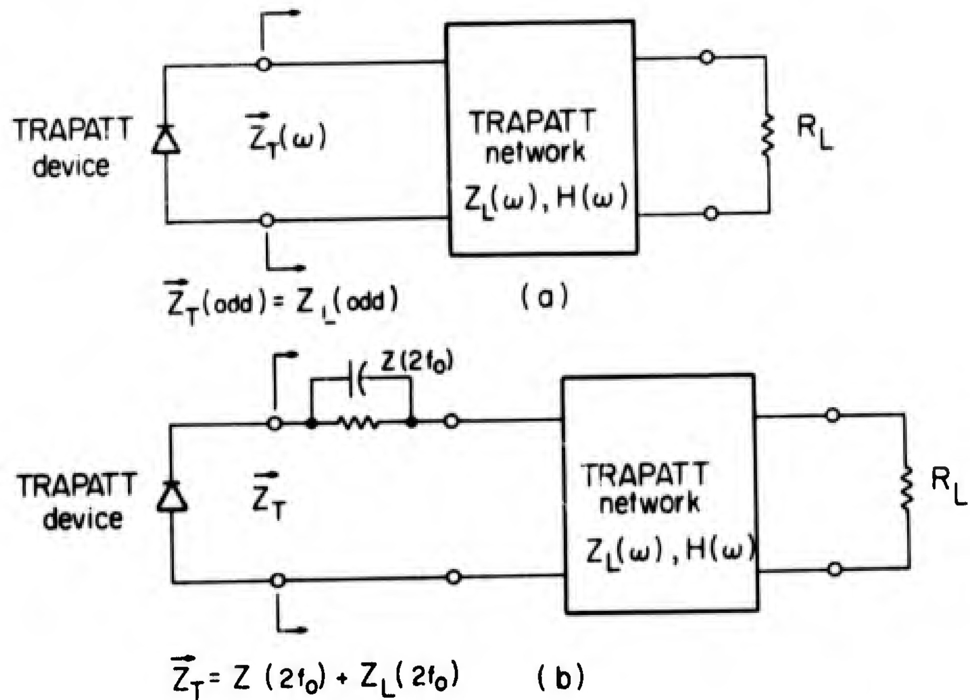


FIG. 28 Equivalent circuits of TRAPATT networks utilizing folded choke bias circuit
(a) fundamental and third harmonic
(b) second harmonic

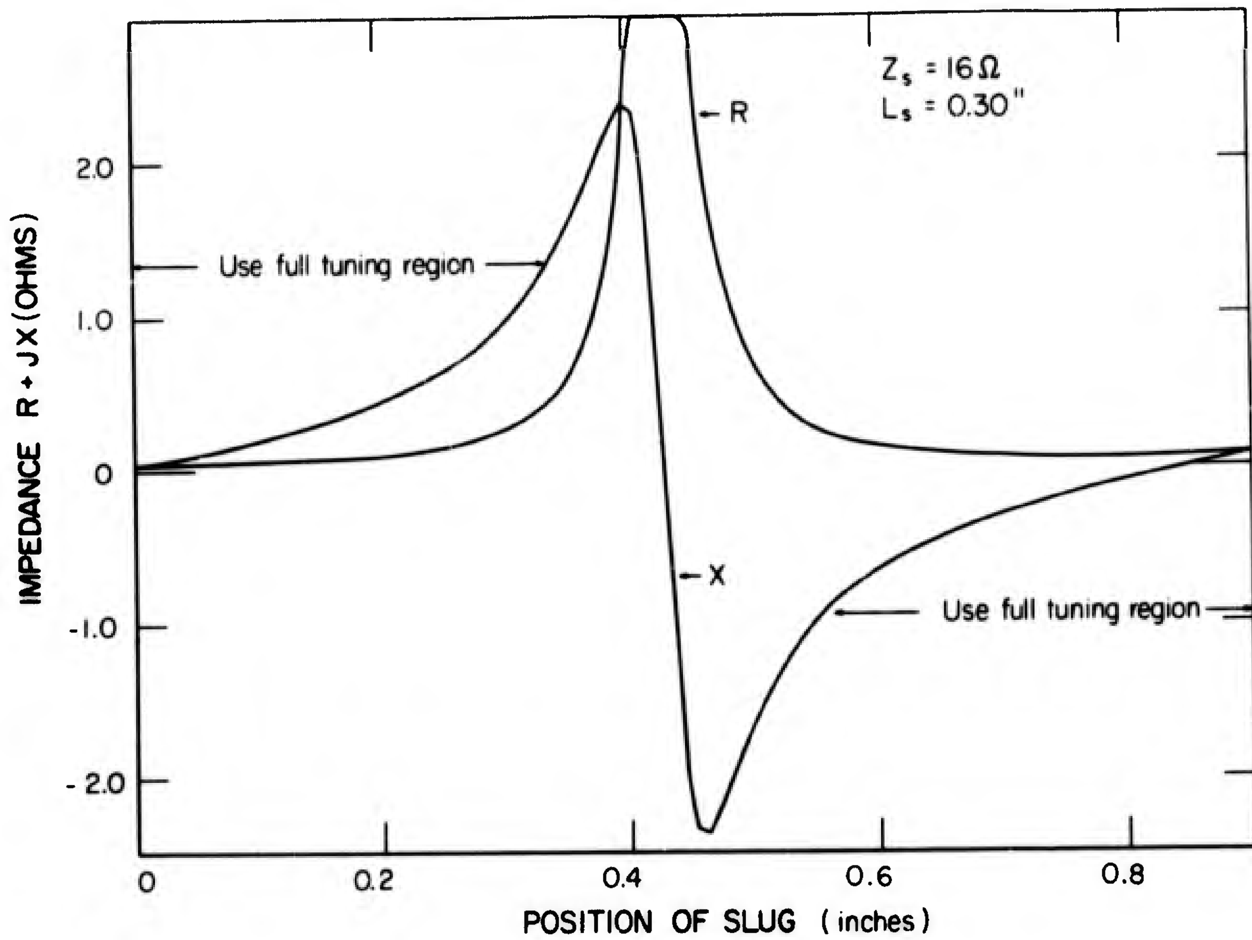


FIG. 29 Second harmonic tuning response of folded choke bias circuit.

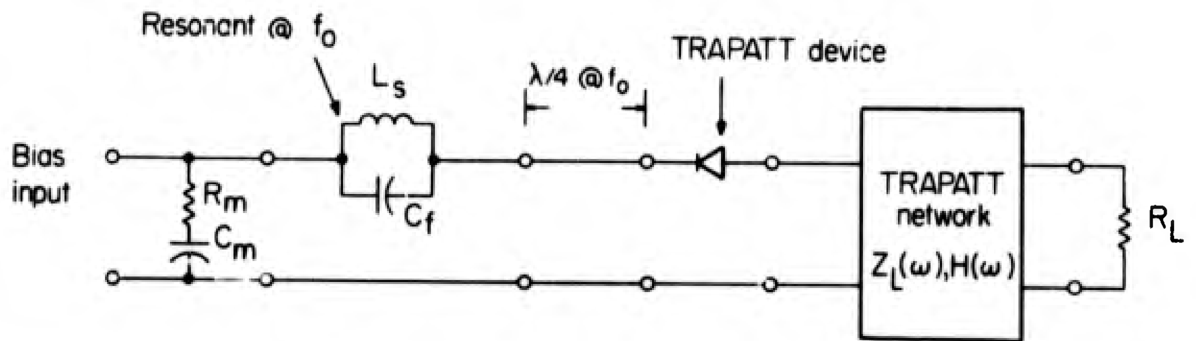


FIG. 30 Equivalent circuit of folded choke bias network.

SECTION 6

SUMMARY

A technique for fabricating single mesa ring diodes has been successfully developed. Diodes designed for 3.5 GHz amplifier application have been operated as cw oscillators at 2.0 GHz. Power outputs of 4.5 to 5.5 W at 20% to 23% efficiencies were achieved. The input power threshold for a 3.5 GHz amplifier is in excess of the thermal dissipation capability of the devices and therefore they were operated in the amplifier mode only on a pulsed basis.

It was observed that the large periphery devices (rings) and, to a lesser extent, the solid mesas degrade while operating in the TRAPATT mode. A study of the degradation characteristics led to the conclusion that the problem was related to surface contamination. A complete description of the surface instability and its effect on TRAPATT operation are presented. A summary of a variety of techniques explored as methods of minimizing surface effects is presented and the present status of the problem is reviewed.

A new circuit design for increasing the bandwidth of the prototype TRAPATT amplifier is presented. The low pass filter is replaced by a multi-resonator, impedance-matching bandpass filter placed as close to the diode as is practical. The feasibility of the approach was verified experimentally at 2.5 GHz using a circuit constructed of non-ideal elements.

It was determined experimentally that the lowest thresholds for TRAPATT operation were observed on small area diodes. An amplifier design was therefore initiated as a method of lowering the input power threshold of an amplifier to a point where cw operation would be feasible. Preliminary results are presented.

In an effort to improve the efficiency of TRAPATT amplifiers, an investigation of various circuit techniques was performed. The best results were achieved using a new bias circuit based on a folded choke. By proper choice of the choke design, tuning at the second harmonic became practical. A typical result is that the 17% efficiency measured in the prototype coaxial circuit was increased to 23% by only a change in the bias network.

SECTION 7

REFERENCES

1. Private communication with C. A. Lee, Cornell University.

2. G. C. Dalman, F. C. Zappert, and C. A. Lee, "Relaxing Avalanche Mode Reflection Amplifier", Electronics Letters 8, p. 243-244 (1972).

3. W. J. Getsinger, "Prototypes for Use in Broadbanding Reflection Amplifiers," IEEE Trans. MTT 1 (November 1963).

4. G. L. Matthaei, L. Young, and E. M. T. Jones, Microwave Filters, Impedance-Matching Networks, and Coupling Structures (McGraw-Hill Publishing Co., N. Y., 1964).

APPENDIX

DESIGN PROCEDURE FOR WIDEBAND TRAPATT AMPLIFIERS

INTRODUCTION

As a result of several years' effort at SCRC, an analytical theory and a design procedure have been developed for wideband TRAPATT amplifier circuits. General amplifier design criteria such as series resonances at the fundamental and odd harmonic frequencies and parallel resonances at the even harmonic frequencies are considered first. Then, combining semiconductor parameters with the design criteria, an equivalent network of the amplifier is arrived at through computer analysis. Particular attention is paid to checking that the network model is consistent with avalanche shock front triggering requirements.

Additional computer analysis is then applied to determine the required network elements. Filter networks are designed using modern network techniques. Applying an impulsive current to the resulting network, the resulting wave shapes are checked to see that they are consistent with TRAPATT operation. Finally, assuming that all of the preceding steps have been successfully completed, the network elements are then checked for their practicality.

TRAPATT AMPLIFIER THEORY

Previous work[1, 2] has established a number of criteria for broadband TRAPATT amplifier behavior. These will not be described in detail here, but are only briefly listed. Fuller discussions of these points are presented in RADC-TR-71-40, the final report for Contract No. F30602-70-C-0110; and RADC-TR-72-101, the final report for Contract No. F30602-71-C-0294. The important requirements are:

(a) The circuit should be series-resonant at or near the first (f_0) and third ($3\ f_0$) harmonics. The low impedance presented to the diode at the first harmonic permits large current flow at this frequency.

(b) The circuit should be parallel-resonant in the vicinity of the second harmonic of $2f_0$. The high impedance presented to the circuit at this frequency demands that a high second harmonic voltage be developed if any current flows at either frequency. Such currents will, of course, be present, since the active diode itself is a very nonlinear element and will develop second harmonic current from the input (signal) frequency. High voltages at the second harmonic could greatly aid the development of the large voltage swings which are required to trigger the ASF, especially if the time-delayed triggering mechanism is not present.

(c) Time-delayed triggering (TDT) must be suppressed as an oscillation-sustaining mechanism. This mechanism, originally described by Evans, is an extremely effective means of increasing the instantaneous voltage of the TRAPATT diode to such a high value that launching of avalanche shock fronts (ASF) is readily accomplished. If TDT is not suppressed as an oscillation-sustaining mechanism, then severe intermodulation distortion in the passband will be observed - if attempts are made to operate the device as an amplifier.

(d) Empirically, it was found that all devices which would operate in a broadband amplifier circuit exhibited a small-signal negative resistance at the second harmonic frequency. This small-signal negative resistance at $2f_0$ could enhance the ability of the diode to generate a signal at $2f_0$, which is presumably necessary for triggering.

The small-signal negative resistance, as well as the parallel resonance of the diode, are shown in Fig. 1, which presents the small signal impedance of a packaged TRAPATT diode successfully operated as a wideband amplifier. Figure 2, on the other hand, presents similar experimental data for a packaged diode which did not operate in the wideband amplifier mode. This diode had a parallel resonance near the second harmonic but no small-signal negative resistance.

The circuit used to achieve wideband amplification free from intermodulation distortion is shown in its equivalent circuit form in Fig. 3, The most critical part of the circuit is the diode mounting and its lumped element reactances which form the circuits at the fundamental and second and third harmonics.

FIG. 1 Small-signal impedance of packaged Trapatt diode succes operated as wideband amplifier at 3.3 GHz.

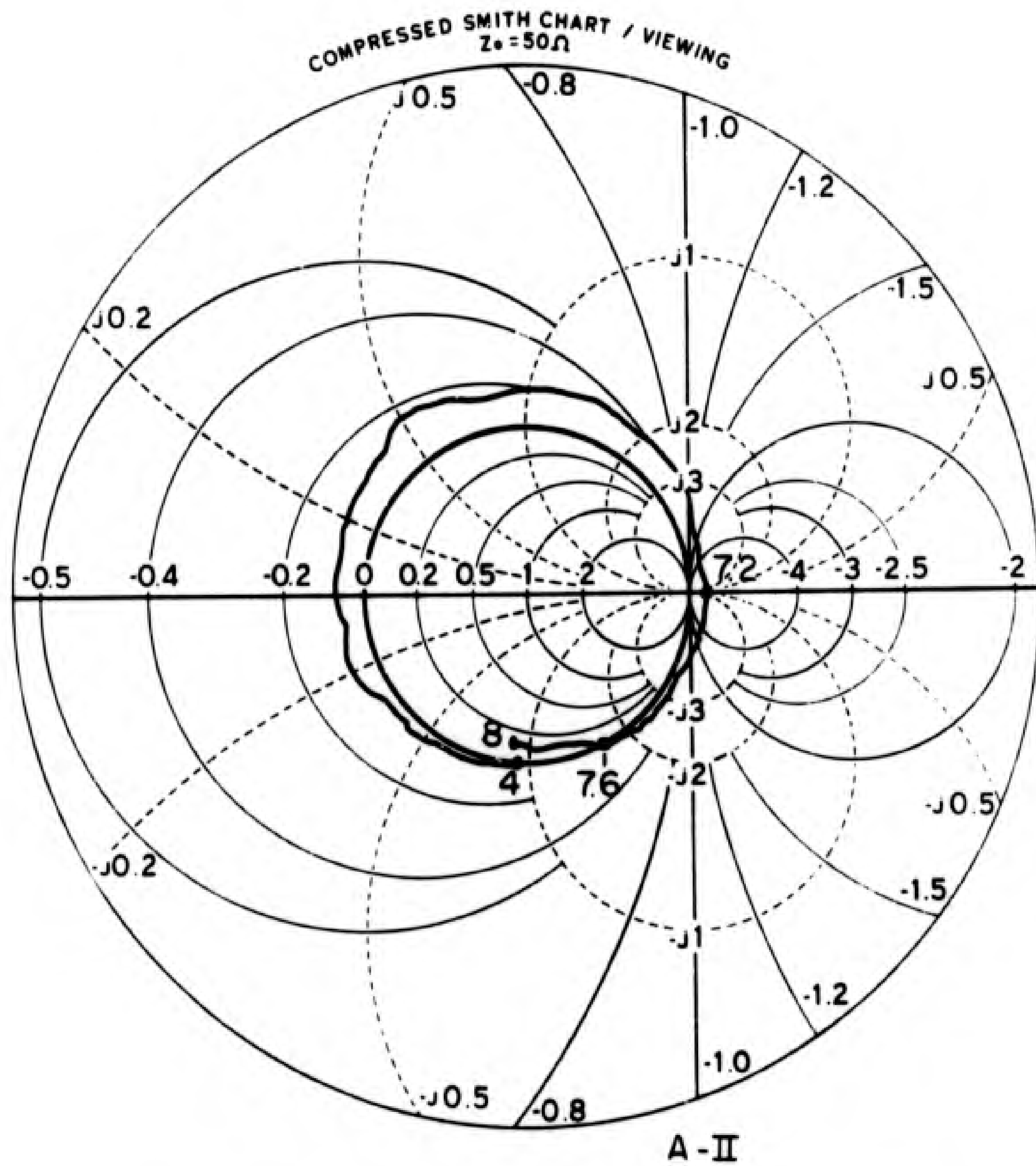


FIG. 2 Small-signal impedance of packaged TRAPATT diode which could not be operated as wideband amplifier.

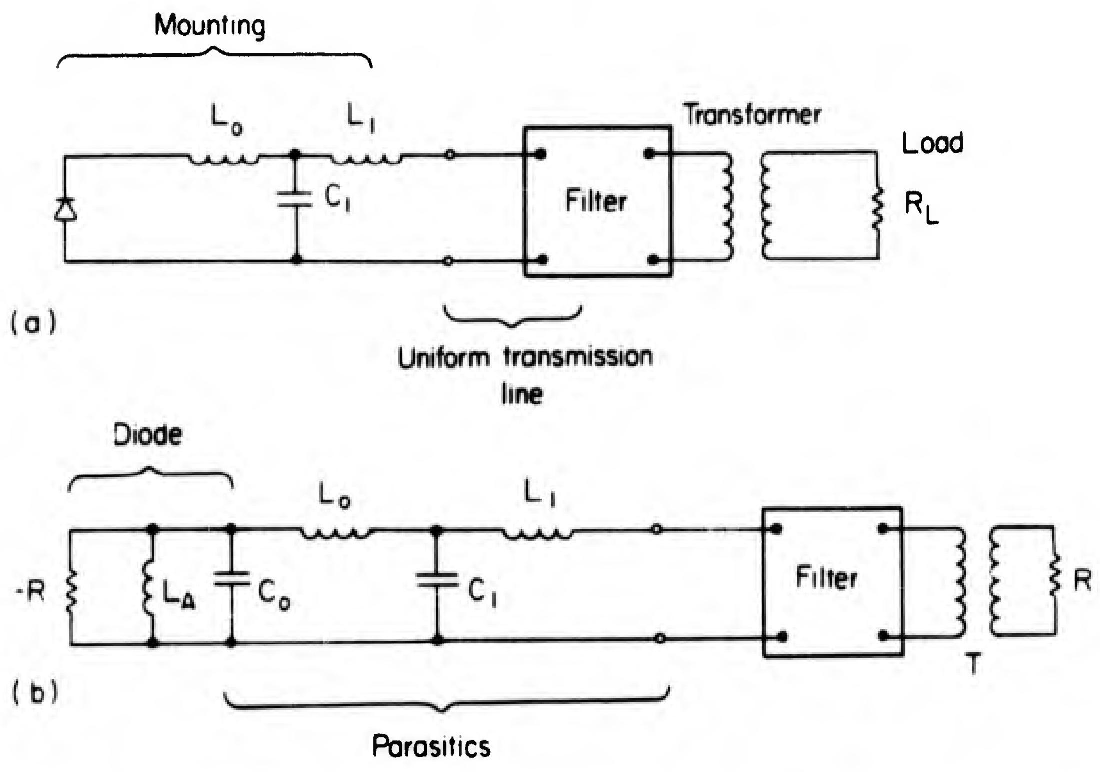


FIG. 3 Equivalent circuit of wideband TRAPATT amplifier.

(a) Diode with its mounting impedance, uniform transmission line, low-pass filter and transformer to load.

(b) Same as above diagram, but with diode represented by its equivalent frequency domain active (electronic) impedance: a negative resistance shunted by an "avalanche" inductance. The magnitudes of these active elements were determined empirically.

The main features of this circuit theory of the wideband TRAPATT amplifier are undoubtedly correct, since application of this theory has guided the successful development of both an X-band amplifier and the translation of the original coaxial form of the S-band amplifier to a microstrip form. However, the theory outlined above is clearly incomplete in the following respects:

(1) No complete analytic theory has been presented for the amplifier;

(2) No complete treatment of the mechanism for triggering avalanche shock fronts in the amplifier circuit has been presented.

The purpose of this section is to present a preliminary analytic theory for the amplifier. This theory is based upon the extremely important insight, first advanced by Carroll,[3] that the interaction between a TRAPATT diode and the oscillator circuit in which it is imbedded can be approximated by a simple model, and that, when the voltage across the diode and its time rate of change exceed certain critical values, then the device acts as an impulsive current generator. A second important contribution by Carroll[4] was to apply to this model the powerful techniques of pseudo-transient analysis in order to determine the response of the circuit to the periodic current impulses. The theory of the TRAPATT amplifier is an extension of Carroll's work and brings out, in a natural way, the requirements for triggering of the avalanche shock fronts (ASF).

In a recent paper by J. E. Carroll,[5] a technique for the analysis of TRAPATT circuits based upon the use of pseudo-transients was presented. This technique allows one to describe the mechanism by which an avalanche diode is triggered into the TRAPATT mode, and to distinguish the "TRAPATT oscillator" (where TDT is the oscillation sustaining mechanism) from the "TRAPATT amplifier" (where TRAPATT operation is externally triggered). The analysis presented here is an extension of Carroll's work for the specific circuit developed for the wideband TRAPATT amplifier.

The basic model of the TRAPATT circuit and diode is shown in Fig. 4. The diode is represented by a particle current generator in shunt with the depletion layer capacitance C_0. The quantities L_a, L_0, C_1, and L_1 represent

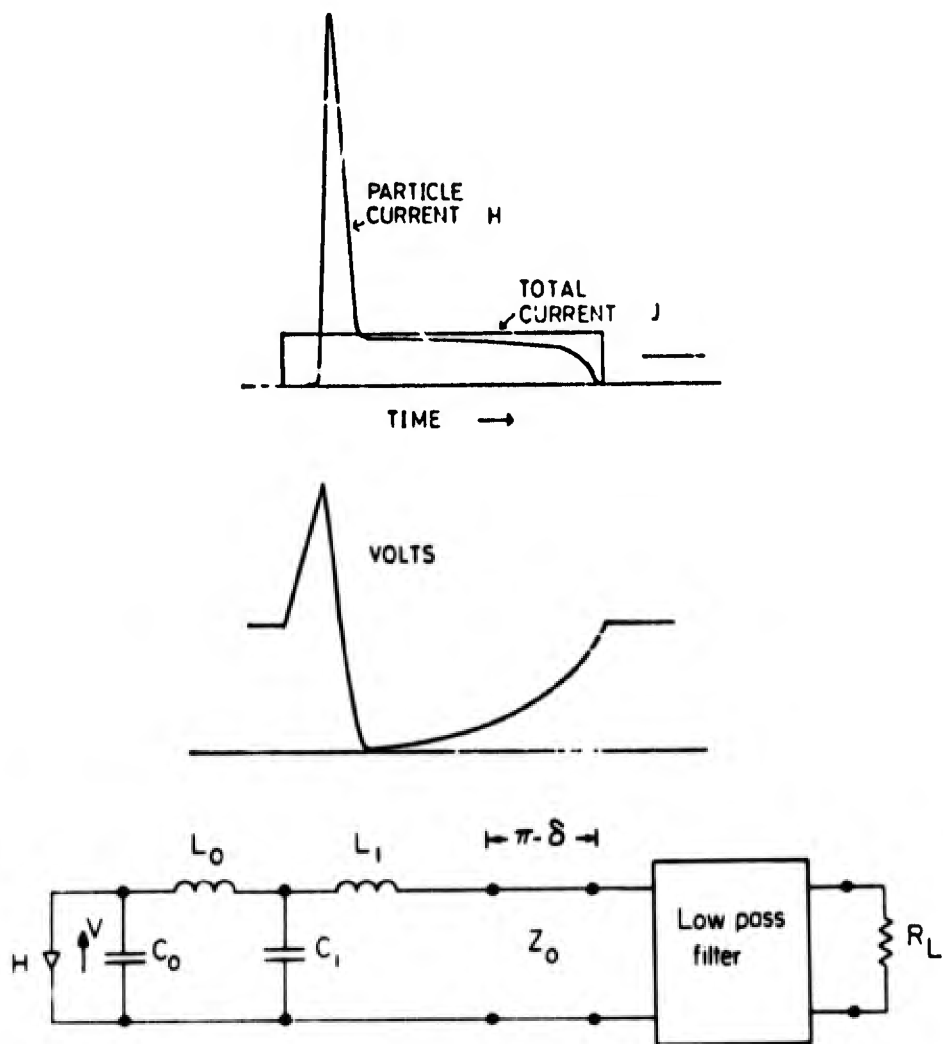


FIG. 4 Basic voltage current properties for TRAPATT mode: (top) particle and total current; (middle) diode voltage; and (bottom) circuit model.

the electronic reactance, parasitic lead inductance, case capacitance, and equivalent corner inductance of the diode packages. An ideal low-pass filter is located at a distance ℓ away from the diode package. It is assumed that the low pass filter passes the fundamental operating frequency unattenuated and is a short circuit to all harmonics of the fundamental frequency.

The current generator H injects an impulsive current density that is induced by the charge carriers generated by the avalanche multiplication. This is a particularly useful model, because the device physics of the avalanche shock front indicate that the induced current has a large impulsive component which controls the voltage response of the circuit. The shape of the particle current H is assumed to be that of a short pulse, as shown in Fig. 4, whereas the total current through the diode J is assumed to have a rectangular form that is consistent with Clorfeine's device theory.[6] These assumptions regarding J and H also determine the time-varying part of the voltage V, since

$$J = H + C_o \frac{dV}{dt} + \frac{1}{L_a'} \int V \, dt \ .$$

It can be seen from Fig. 4 that the voltage across the diode is self-consistent with the TRAPATT mode theory (e.g., there is a large overvoltage that can trigger an avalanche shock front [ASF],causing the diode voltage to drop to zero and then recover).

It will be shown that the circuit used for the TRAPATT amplifier is much different from that of the TRAPATT oscillator in that the steady-state response of the amplifier circuit will exhibit a voltage waveform that does not have a sufficient "over-voltage" to trigger an ASF unless an external voltage at the operating frequency is applied.

We assume that the diode particle current H can be represented by a recurrent delta function with repetition period T given by

$$H(t) = Q \ \mathrm{Rep}_T \delta(t) \qquad 0 \le t \le \infty \quad .$$

The steady-state voltage across the diode can then be determined by using Laplace transform techniques. To analyze the circuit, we will initially replace the low-pass filter by a short circuit at all frequencies. When considering the more realistic case of power extraction, the filter will be chosen to pass power only at the fundamental frequency.

The impedance presented to the particle current generator, with a short circuit replacing the low pass filter, is given by

$$N = S^3 L_0 L_1 C_1 + S(L_0 + L_1) + (1 + S^2 L_0 C_1) \tanh S(\pi - \delta)$$

$$D = S^4 L_0 L_1 C_0 C_1 + S^2 [(L_0 + L_1)C_0 + L_1 C_1] + S[C_0 + C_1 + S^2 L_0 C_1 C_0] \tanh S(\pi-\delta)+1$$

$$\frac{Z}{Z_0} = \frac{S L_a N}{S L_a D + N}$$

where $S = j\,\omega/\omega_0$, $L_0 = \omega_0 L_S/Z_0$, $L_1 = \omega_0 L_R/Z_0$, $C_0 = C_j \omega_0 Z_0$, $C_1 = C_c \omega_0 Z_0$,

$L_a = \omega_0 L_a/Z_0$, ω_0 = fundamental radian frequency, $\theta = \omega_0 t$.

The distance ℓ from the diode to the filter is given by the phase angle $(\pi-\delta)$, where δ represents the effect of placing the filter less than a half wavelength away from the diode.

The steady-state reactive voltage across the diode can be determined by decomposing the particle current H into the Fourier components given by

$$H(\theta) = \sum_{n=1}^{\infty} H_n e^{S\theta} .$$

The steady-state voltage across the diode is therefore given by

$$V_{ss} = \sum_{n=1}^{\infty} H_n Z_n e^{S\theta}$$

where Z_n is the complex impedance at the nth harmonic, given by $Z(jn)$. Because we are only concerned with harmonics of the fundamental (integer values of ω/ω_0), the impedance function Z/Z_0 can be replaced by a pseudo-impedance function which differs from the original impedance function only by the substitution of $-\tanh S\delta$ for $\tanh S(\pi-\delta)$ wherever it occurs in the expression for Z/Z_0. This pseudo-impedance function gives the same impedance at all harmonics, but now has a set of pseudo transients $e^{p\theta}$, where p are the roots of

$$S\, L_a\, D + N = 0$$

It has been shown[5] that for every root $S = +p$ there is a root $S = -p$. The exponential parts of roots together with the residues of these roots for the pseudo-impedance function can be used to determine the steady-state voltage response. The steady-state behavior of the circuit may be usefully described to be the approximate pseudo-impedance function

$$\frac{Z(S)}{Z_o} = \sum_{i=1}^{n} R_i\left(\frac{1}{S-p_i} + \frac{1}{S+p_i}\right) + \sum_{\ell=1}^{m} R_\ell \left\{\frac{S+\sigma_\ell}{(S+\sigma_\ell)^2 + \nu_\ell^2} + \frac{S-\sigma_\ell}{(S-\sigma_\ell)^2 + \nu_\ell^2}\right\}$$

where R_i is the residue at real pole p_i, R_ℓ is the residue at complex pole $p_\ell = \pm\sigma_\ell \pm j\nu_\ell$, n is the number of real poles, m is the number of complex poles.

This complex impedance function can be used to find a steady-state voltage response to periodically applied impulsive current[7] $H(S) = \dfrac{Q}{1-e^{-2\pi S}}$

$$V(\theta) = \sum_{i=1}^{n} - \frac{R_i QZ_0 \text{ Sinh } p_i(\theta - \pi)}{\text{Sinh } p\,\pi} + \sum_{\ell=1}^{m} QR_\ell Z_0 \left\{ \frac{\sinh \sigma_\ell(\theta-\pi) \sinh \sigma_\ell \pi \cos \nu_\ell \theta}{\sinh^2 \sigma_\ell \pi + \sin^2 \nu_\ell \pi} \right\} .$$

For a good oscillator circuit ($\delta << 1$) there is only one set of real roots, and the imaginary roots have very small real parts($\sigma << 1$) and the complex frequency $\nu > 3$. The residue associated with the complex root is, in general, one order of magnitude less than that of the real root. Thus, for the oscillator case the periodic voltage across the diode is given by*

$$V(\theta) \approx V_0 + RQZ_0 \frac{\sinh p(\theta - \pi)}{\sinh p\pi} \quad 0 < \theta < \pi$$

and

$$V(\theta + 2\pi) = V(\theta) .$$

The elements of TRAPATT operation can be seen by examining the voltage waveform shown in Fig. 5. As the diode fires (ASF excited) an impulse of particle current collapses the voltage, which then grows exponentially as a sinh function. The reactive termination at the harmonic serves the function of pretriggering the TRAPATT mode, while the resistive impedance that is added across the diode through the low pass filter at the fundamental extracts the power with a minimum alteration of the triggering process. In order to trigger the avalanche shock front, one requires that the voltage rise fast enough so that $C_0\, \partial V/\partial t$ exceeds the critical current at breakdown. On this basis, if p is too small, the rate of rise of voltage will fail to initiate an avalanche shock front. It should be noted that the charge Q must be sufficient to make the circuit voltage fall to zero if the low impedance plasma state of the diode is to be matched.

The power extraction is accomplished by adding an additional voltage which is in anti-phase with the current pulse. This implies readjusting $Z(\omega_0)$ so as to add a series impedance Z_r to the original fundamental

* Note the pseudo-transient can have exponential functions, since the growth is limited to one period only and the value of the function at $V(2\pi) = V(0)$.

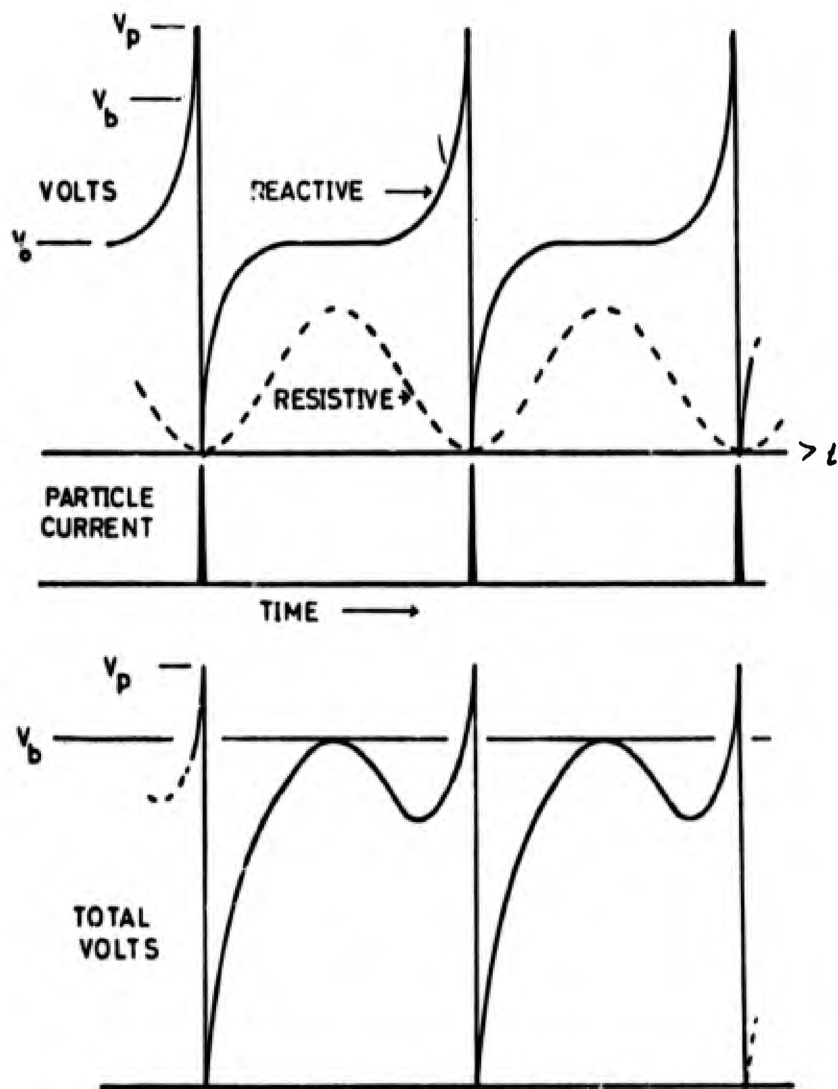


FIG. 5 TRAPATT circuit voltage waveforms.

impedance Z(S). Power extraction is shown schematically in Fig. 5. The maximum fundamental voltage swing is determined by the condition that there should not be premature avalanche.

As one would expect, the triggering waveform is greatly dependent upon the parasitic reactances of the diode package and δ. The ideal case would be one where the radial mode corner inductance L_1 and the parasitic lead inductance L_0 would be zero. However, in practice, only the radial mode inductance can be reduced to an insignificant value (by using a very small diameter coaxial line). The lead inductance usually can be reduced to some small value. The effect of varying the lead inductance is illustrated in Fig. 6, which shows the reactive or triggering voltage as a function of inductance L_0 and for a particular value of capacitances. If the inductance is too small (L_0 = 0.125 nH), a high frequency ringing appears; if too large an inductance is used (L_0 = 3.5 nH), a transient which has exponential functions between 0 and 2π is excited (the real pole becomes complex). In fact, by increasing the inductance, we can suppress TDT as the oscillation-sustaining mechanism for the TRAPATT mode.

The amplifier circuit differs from the oscillator circuit in that the inductances L_0 and L_1 are too large for good oscillation waveforms, and the value of δ is also too big. It has been shown by Carroll[4] that increasing δ decreases the amplitude of p, therefore reducing the rate of rise of voltage necessary to excite the avalanche shock front. This observation provides an analytic and quantitative explanation for the experimental result that the distance between device and the closest filter element must be well under a half wavelength, as described in RADC-TR-71-40 (Final Report for Contract F30602-70-C-0110). This circuit was originally designed, of course, largely on intuitive grounds.

The wideband amplifier circuit differs significantly from the oscillator circuit in that the low pass filter is located much closer to the diode, and the inductance L_S is much larger than that used in an oscillator added to the circuit at the diode terminals. The effect of the added inductance and the reduction in the distance from the low pass filter to the diodes is to suppress TDT as an oscillation-sustaining mechanism. This is illustrated in Figs. 7 and 8, which show the effect of variation

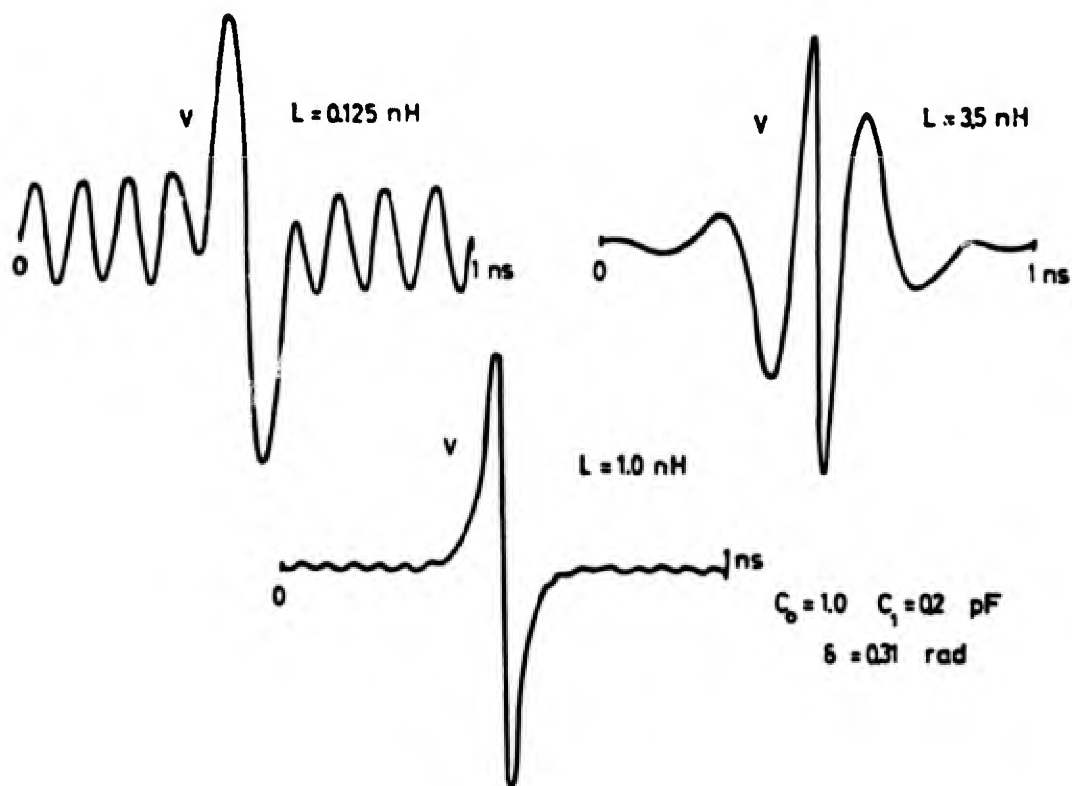


FIG. 6 Variations of diode voltage response for changes in inductance L_0.

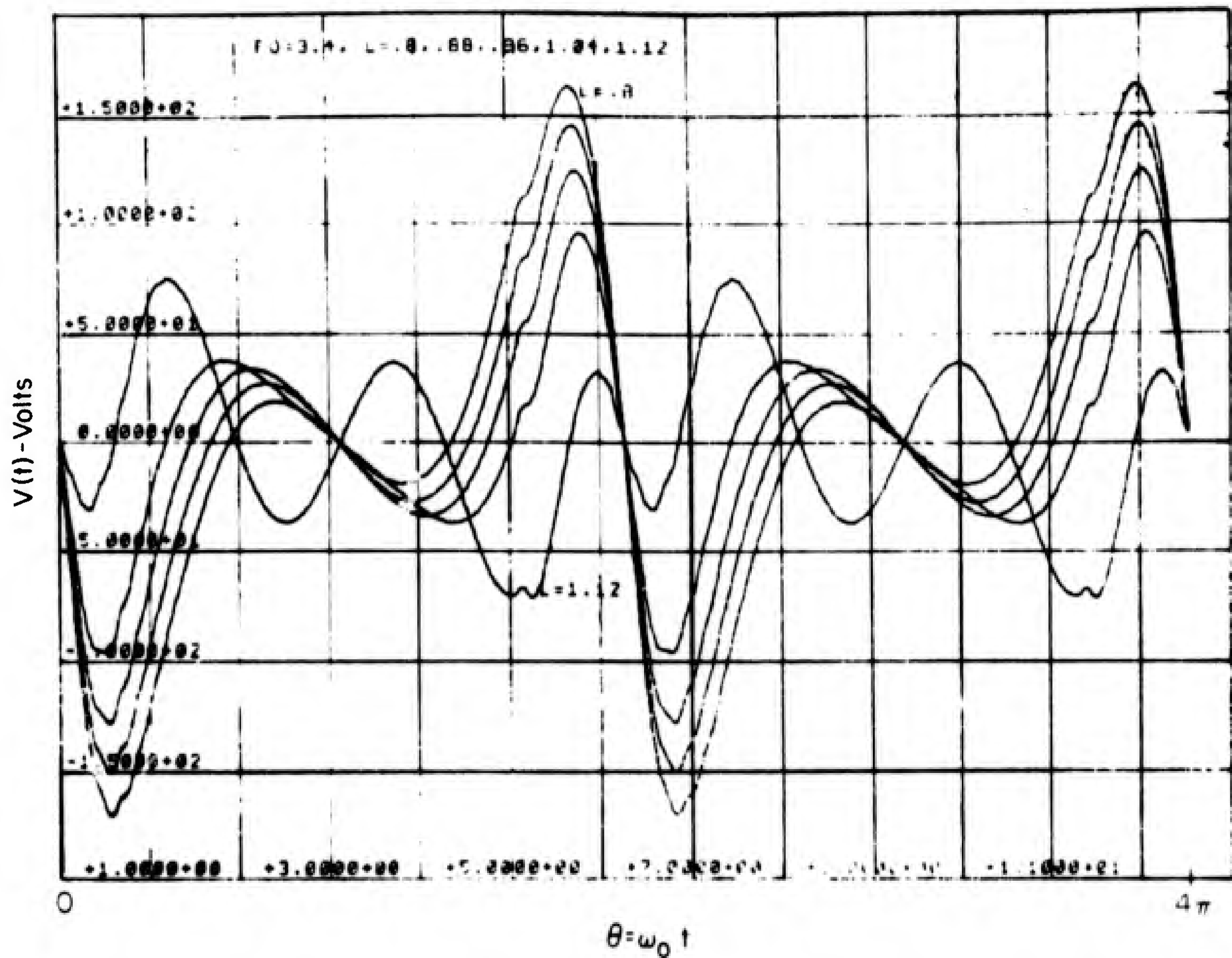


FIG. 7 Steady-state voltage response to a periodic current $H = A[(1+\cos\theta)/2]^n$ at semiconductor chip as a function of parasitic lead inductance L_S. Center frequency 3.3 GHz, $I_{dc} = 0.5$ A, $n = 18$, $C_j = 0.6$ pF, $C_c = 0.5$ pF, $L_R = 0.5$ nH, $\ell = 1.0$". Inductance increment 0.5 nH plotted for $L_S = 1.0 - 4.0$ nH.

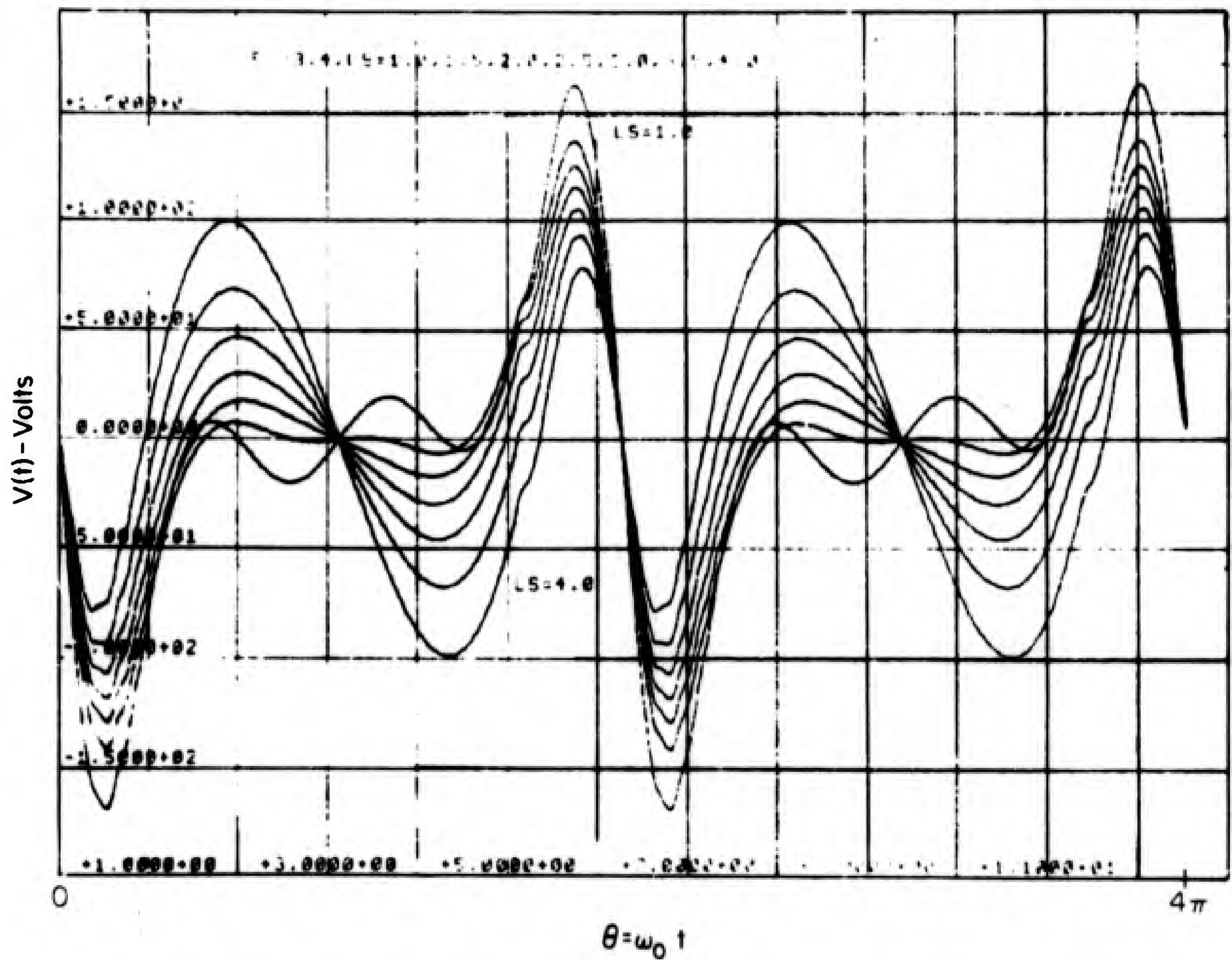


FIG. 8 Steady-state voltage response to a periodic current $H = A[(1+\cos\theta)/2]^n$ at the semiconductor chip as a function of the distance ℓ between the diode package and the low-pass filter. Center frequency 3.3 GHz, $I_{dc} = 0.5$ A, $n = 18$, $C_j = 0.6$ pF, $C_c = 0.5$ pF, $L_S = 2.7$ nH, $L_R = 0.5$ nH.

of the inductance L_S and the distance δ. The curves of these figures were produced from the computer programs and are the graphical plottings of the expressions for $V_{(\theta)}$, with values of the circuit elements chosen to be good approximations of actual amplifier circuits. The current waveform was chosen to be of the form $H(\theta) = A_n[\frac{1}{2}(1 + \cos\theta)]^n$, where A_n was normalized to yield an average current of 700 mA in order to be in agreement with actual operating conditions of a particular experimental amplifier. The value of $n = 18$ was chosen so that the impulsive current half-width was 15 psec, which is probably a fairly good approximation to actual TRAPATT waveforms.

For $L_S = 1.0$ nH there is a large overvoltage with sufficient dV/dt so that TDT is an oscillation sustaining mechanism. As L_S is increased, the peak-to-peak voltage decreases from 340 V for $L_S = 1.0$ nH to less than 150 V for $L_S = 4.0$ nH . It is interesting to note that increasing L_S seems to cause a large second harmonic voltage across the diode. This is consistent with the experimental evidence of the necessity of having a large second harmonic voltage in order to enhance the ability of the circuit to trigger ASF within the diode, as described. For the case where L_S is large enough ($L_S > 2.0$ nH), there would have to be an external signal at ω_0 applied to the diode in order to trigger the TRAPATT mode, as observed in the experimental amplifier. For inductance less than 1.0 nH, the computer predicts that the triggering waveforms are grossly distorted and no ASF can be triggered. This again has been observed experimentally.

The steady-state voltage at the diode terminals as a function of the parameter δ is shown in Fig. 8. The amplitude of the reflected voltage decreases with increasing δ. This decrease in the overvoltage is similar to that observed for increasing lead inductance L_S. It is interesting to note that the amplitude of the overvoltage is a much stronger function of δ than is the time delay between the incident and reflected voltages of the TDT waveforms.

The computer-generated voltage waveform at the diode terminals as a function of frequency is shown in Fig. 9. These curves were generated using the actual parameters of a wideband amplifier circuit and diode.

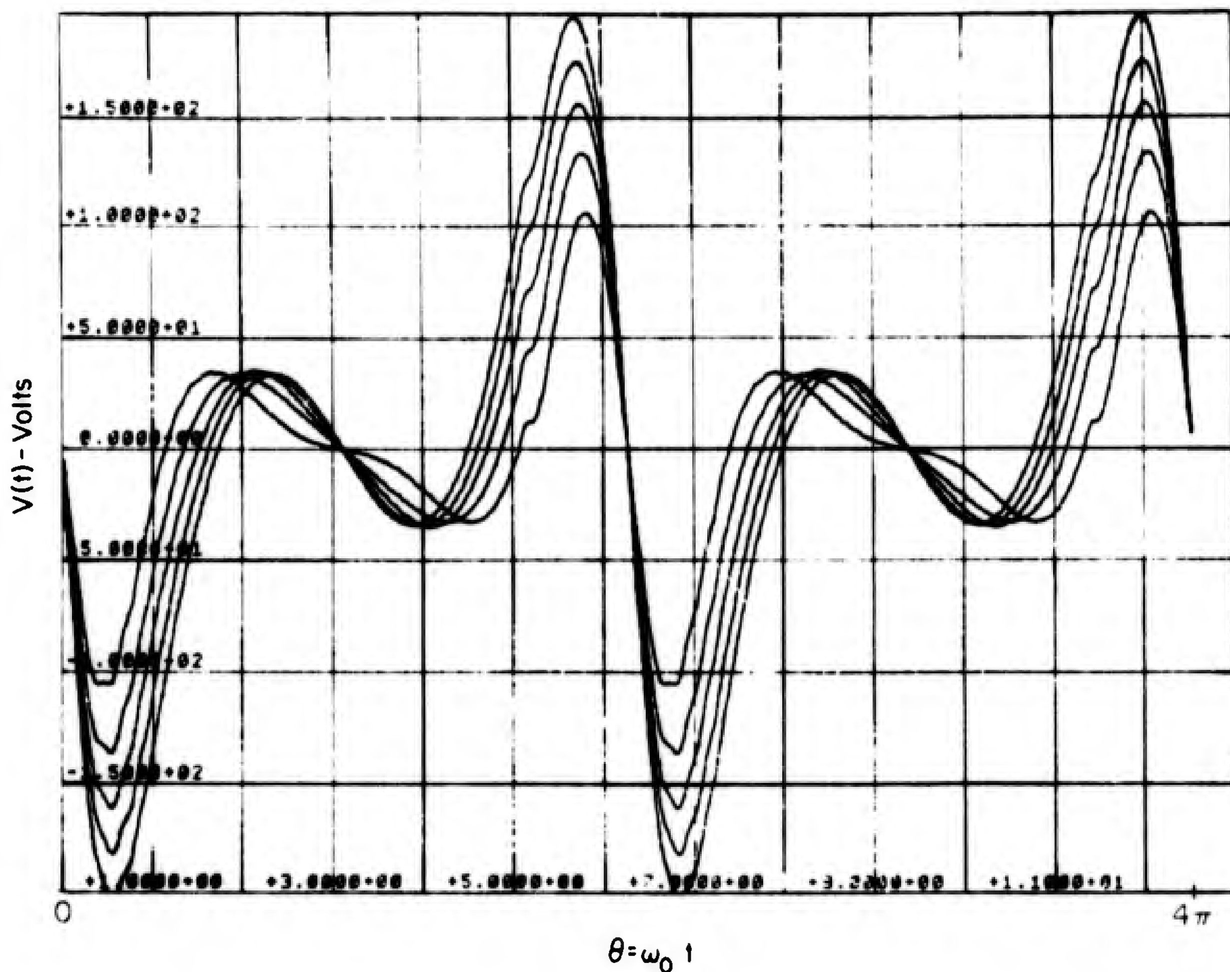


FIG. 9 Steady-state voltage response to a periodic current $H = A[(1+\cos\theta)/2]^n$ at the semiconductor chip as a function of frequency. $I_{dc} = 0.7$ A, $n = 18$, $C_j = 0.6$ pF, $C_c = 0.5$ pF, $L_s = 2.7$ nH, $L_R = 0.5$ nH, $\ell = 1.0"$. Frequency variation 3.0 GHz to 3.8 GHz in 0.2 GHz steps.

The amplitude of the overvoltage decreases with increasing frequency. This would indicate that the bandwidth of the ideal amplifier is limited at the high end by the 3 dB half-power point and at the low end by TDT oscillations. This type of operation has been experimentally observed. However, by adjusting the parameters of the low pass filter, the low end of the passband response can be made to exhibit a half-power band limitation. This type of analysis does, however, predict that a wide 1 dB bandwidth should be possible, with the low frequency limitation TDT oscillation and the high frequency limitation being determined by the fall-off in amplitude of the overvoltage.

Further computer analysis using the actual impedance of a practical amplifier circuit will give the true limitations of wide TRAPATT amplifier circuits.

A most important conclusion from this method of analysis is that the location of the low pass filter from the diode plays a secondary role in preventing TDT from being an oscillation-sustaining mechanism, and that, for the wideband amplifier circuit developed at SCRC, it is the series inductance L_0 together with the parameter δ which is mainly responsible for suppressing TDT oscillations. This effect is further demonstrated in Fig. 8, which shows the effect the inductance has on the voltage waveform at the terminals of the TRAPATT diode in an actual amplifier circuit. A short pulse ($\approx$ 60 ps) time-domain reflectometer was used. The pulse was applied at the terminals of the semiconductor chip. The voltage at these terminals was measured as a function of the parasitic lead inductance L_1. Figure 10(a) shows the voltage waveform for L_0 = 2.7 nH; the reflection from the low pass filter is almost totally obscured by the differentiation due to the large inductance. In Fig. 10(g) the inductance has been reduced to about 0.4 nH . This has the effect of allowing the reflected pulse to exist at the terminals, delayed in time by an amount equal to the round-trip propagation from the diode to the filter and back again.

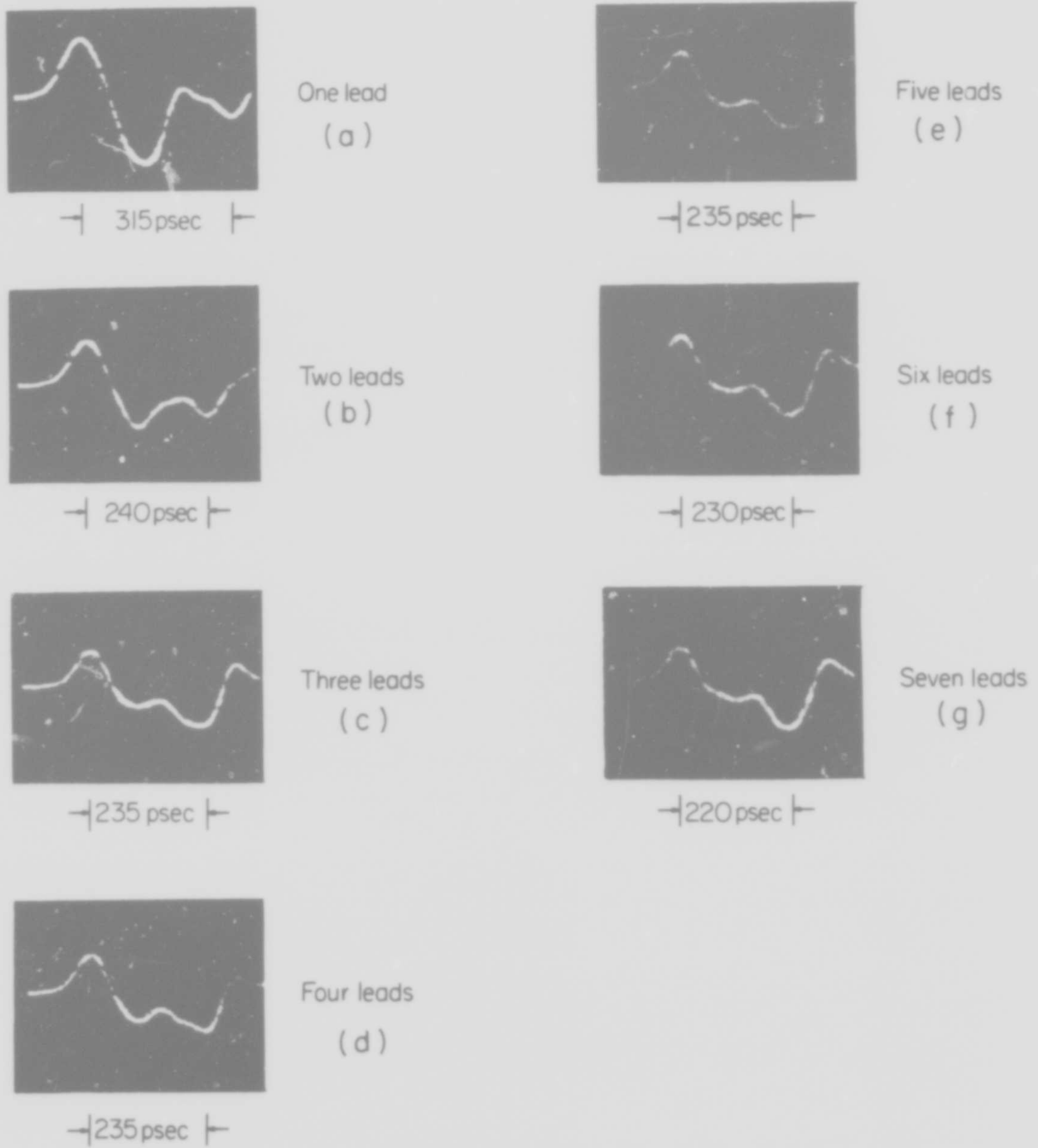


FIG. 10 Time-domain reflectometer presentation of impulse voltage response at diode terminal as a function of parasitic lead inductance.

REFERENCES

1. M. I. Grace, H. Kroger, C. N. Potter, H. J. Pratt, Jr., and J. Telio, Final Technical Report for Contract No. F30602-71-C-0294.

2. M. I. Grace, "Broadband High-Efficiency-Mode Amplifiers at S-Band," Proc. 1971 European Microwave Conference, Vol. 1, pp. A-8/1:1-A 8/1:4.

3. J. E. Carroll, "An Analytic Theory for the Evans' Circuit for Avalanche Diodes," Trans. Microwave Theory and Techniques MTT-18 (November 1970).

4. J. E. Carooll, "The Use of Pseudo-Transients in the Solution of Evans' TRAPATT Circuit," Paper presented at 8th International Conf. on Microwave and Optical Generation and Amplification, Amsterdam, 1970.

5. J. E. Carroll and R. H. Crede, "A Computer Simulation of TRAPATT Circuit," International J. of Electronics Vol. 32, No. 3, (1972).

6. A. S. Clorfeine, R. J. Ikola, and L. S. Napoli, "A Theory for the High-Efficiency-Mode at Oscillation in Avalanche Diodes, R.C.A. Rev. 30, 397-422 (September 1969).

7. S. Seshu and N. Balabanian, Linear Network Analysis (J. Wiley & Sons, Inc., 1959) pp. 168-186.

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