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INVESTIGATION OF TECHNICAL PROBLEMS
IN GALLIUM ARSENIDE

Fred E. Eisen, et al

Rockwell International Corporation

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13. ABSTRACT A broad area of technological problems of GaAs is covered in this progress report. The goal is to make contributions that will improve the current technology of micro-wave devices. The devices considered here are the Schottky barrier FET (MESFET) and the IMPATT diode. The work reported here covers problems of growth and characterization of very thin high-conductivity epitaxial films and high-resistivity epitaxial films; some aspects of processing of MESFET devices; study of the RF performance of IMPATT diodes and its relationship with the material parameters; problems of growth and characterization of semi-insulating GaAs; use of proton bombardment to convert conductive layers into high-resistivity layers, and, finally, study of n-type doping of GaAs by ion implantation with particular emphasis on the annealing problems. These activities and their role in the device technology are in separate sections along with their goals, the progress made in the first six months of this contract and the future plans. This work is being carried out in cooperation with the California Institute of Technology, Cornell University, Stanford University, and the University of Southern California.			
KEY WORDS: Ion implantation, Semi-Insulating GaAs, Epitaxy, MESFET, IMPATT.			
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TABLE OF CONTENTS

	Page
1.0 INTRODUCTION	1
2.0 PROGRAM GOALS AND TECHNICAL APPROACH	5
2.1 Epitaxial Materials Growth and Characterization	5
2.1.1 Ultra-Thin, High-Conductivity Layers	5
2.1.2 High-Resistivity GaAs Thin Films	8
2.1.3 Processing and Device Measurements	8
2.1.3.1 MESFET	8
2.1.3.2 IMPATT	15
2.2 Semi-Insulating Materials	19
2.2.1 Crystal Growth	22
2.2.2 Measurement Techniques	22
2.2.2.1 Analytical Measurements	23
2.2.2.2 Quantitative Measurements of Impurity Concentrations	24
2.2.2.3 Complementary Measurements	25
2.2.2.4 Measurements on Devices	25
2.2.3 Proton Bombardment and Oxygen Implantation	26
2.3 n-Type Doping of GaAs by Ion Implantation	27
2.3.1 Annealing Cap	28
2.3.2 Characteristics of Implanted Layers and Junctions	29
2.3.3 Device Processing, Fabrication, and Evaluation	29
3.0 RESULTS	30
3.1 Epitaxial Material Growth and Characteristics	30
3.1.1 Ultra-Thin, High-Conductivity Layers	30
3.1.2 High-Resistivity GaAs Thin Films	32
3.1.2.1 Summary of Results	35
3.1.3 Processing and Device Measurements	39
3.1.3.1 MESFET	39
3.1.3.2 IMPATT	45

Table of Contents (Cont'd)

	<u>Page</u>
3.2 Semi-Insulating Materials	52
3.2.1 Crystal Growth	52
3.2.2 Measurement Techniques	54
3.2.2.1 Analytical Measurements	54
3.2.2.2 Quantitative Measurements of Impurity Concentrations	56
3.2.2.3 Complementary Measurements	64
3.2.2.4 Summary	70
3.2.3 Proton Bombardment	72
3.3 n-Type Doping of GaAs by Ion Implantation	78
3.3.1 Annealing Cap	79
3.3.2 Characteristics of Implanted Layers and Junctions	82
3.3.3 Device Processing, Fabrication, and Evaluation	90
3.4 Interface Measurements	94
4.0 FUTURE PLANS	99
4.1 Epitaxial Material Growth and Characterization	99
4.1.1 Ultra-Thin, High-Conductivity Layer	99
4.1.2 High-Resistivity GaAs Thin Films	100
4.1.3 Processing and Device Measurements	100
4.1.3.1 MESFET	100
4.1.3.2 IMPATT	101
4.2 Semi-Insulating Materials	101
4.2.1 Crystal Growth	101
4.2.2 Measurements	101
4.2.3 Proton Bombardment and Oxygen Implantation	102
4.3 n-Type Doping of GaAs by Ion Implantation	102
4.3.1 Annealing Cap	102
4.3.2 Characteristics of Implanted Layers and Junctions	103
4.3.3 Device Processing, Fabrication, and Evaluation	103
5.0 REFERENCES	104

TABLE OF ILLUSTRATIONS

<u>Figure</u>	<u>Page</u>
1.0-1 A frequency divider-by-two using transferred electron logic	3
2.1-1 Approximate growth rate-time elapsed nature of epitaxial lay deposition	6
2.1-2 A cross section of an FET active region showing the dependence of circuit parameters on N_D and dimensions	9
2.1-3 Some important relations governing the FET device performance	10
2.1-4 The lines of constant $N_D x d$ product that show constant unilateral gain contours	12
2.1-5 A simple single-gate FET	16
2.1-6 Electric field and carrier concentration levels for a 10 GHz IMPATT device with transit angle of drift region ψ of 180°	18
3.1-1 Thickness variation of a layer grown in liquid phase epitaxial growth system	31
3.1-2 A growth cell for liquid phase growth of epitaxial GaAs	33
3.1-3 A system for the liquid phase growth of epitaxial GaAs	34
3.1-4 Photoluminescence spectra on undoped (a) and chromium-doped GaAs grown from Ga	37

Table of Illustrations (Cont'd)

<u>Figure</u>	<u>Page</u>
3.1-5 Configuration of an ideal FET where the ohmic contacts are deep into the active layer and the device is dated by means other than mesa etching	40
3.1-6 SEM X-ray energy dispersive analysis on the contact area obtained by the alloying of eutectic gold-germanium at 450°C for 2 minutes	42
3.1-7 SEM photomicrograph showing a metallization break in the gate at the point where it climbs the edge of the mesa	44
3.1-8 Equivalent circuit of cavity and series circuit for diode	46
3.1-9 Small signal gain at 3 to 4 GHz of cavity-mounted GaAs device as a function of reverse current	47
3.1-10 Small signal gain at 6 to 7 GHz of cavity-mounted GaAs device as a function of reverse bias current	51
3.1-11 Large signal gain characteristic of cavity-mounted GaAs device as a function of input power at frequencies between 6.25 and 7.00 GHz	53
3.2-1 Absorption coefficient of semi-insulating GaAs at room temperature	57
3.2-2 Schematic of the n-i-m structure	59
3.2-3 Ideal I-V characteristics for an insulator under single injection	61
3.2-4 I-V characteristics at an n-i-m structure under electron injection, and a p-i-m structure under hole injection	63

Table of Illustrations (Cont'd)

<u>Figure</u>	<u>Page</u>
3.2-5 Thermally-stimulated current measurements on semi-insulating GaAs with AuGe contacts	65
3.2-6 Thermally-stimulated current measurement on semi-insulating GaAs in an n-i-m structure after illumination and after electron injection	67
3.2-7 Photoconductivity spectrum of semi-insulating GaAs in an n-i-m structure at 4.2°K	69
3.2-8 Photovoltaic effect in a p-i-m structure at 4.2°K	71
3.2-9 (a) Schematic of a proton-bombarded sample (b) Depth of the semi-insulated layer vs proton beam energy	73
3.2-10 Breakdown voltage vs depth of semi-insulating layers made by proton bombardment	75
3.2-11 Thermally-stimulated current spectrum of proton-bombarded GaAs	76
3.2-12 Flat band voltage of capacitance-voltage measurements on a reverse-biased n-i-m structure	77
3.3-1 Energy spectrum of 2 MeV He ions backscattered from a sputtered AlN film on carbon	80
3.3-2 Capacitance-voltage characteristics of two ion-implanted diodes	83
3.3-3 Electron concentration and mobility profiles for a tellurium-implanted sample processed with a Si ₃ N ₄ cap during anneal	84

Table of Illustrations (Cont'd)

<u>Figure</u>	<u>Page</u>
3.3-4 Electron concentration and mobility profiles for a tellurium-implanted sample processed with an AlN cap during anneal	85
3.3-5 Electron concentration vs depth profile obtained from Schottky barrier capacitance-voltage data for a sample implanted with 220 keV tellurium and annealed with an AlN cap	87
3.3-6 Electron concentration vs depth profile obtained from Schottky barrier capacitance-voltage data for the sulfur-implanted layer used for FET fabrication	91
3.3-7 Current-voltage characteristics of an FET fabricated in an n-type layer produced by sulfur ion implantation	93
3.4-1 C-V measurements on an epi-on-epi interface	98

LIST OF TABLES

	<u>Page</u>
3.1-1 Epitaxial GaAs Growth Conditions and Properties	36
3.2-1 Impurities in Cr-Doped GaAs	55
3.3-1 Comparison of Doping in Tellurium-Implanted GaAs Annealed with a Si_3N_4 Cap or an AlN Cap	89
3.4-1 Determination of Ga and As on GaAs Surfaces After Treatment as Measured by ESCA	97

INVESTIGATION OF TECHNICAL PROBLEMS IN GaAs
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1.0 INTRODUCTION

There is little doubt that device feasibility and, in some cases, device production, has been demonstrated using GaAs. However, to bridge the gap separating feasibility from a viable production capability where matters such as yield, cost, and reliability must be emphasized requires solutions to important technological problems ranging from material growth to device processing and fabrication.

There are many examples in areas of high technology where the transition from demonstration to production was prematurely attempted with technically and financially unfortunate results. The above points will be illustrated, and, at the same time, some of the problems that we have initially identified for this research program will be discussed by taking as an example the state-of-the-art of a typical microwave device whose problems are representative of a whole class of components.

The Schottky barrier GaAs FET (MESFET) has aroused considerable interest as an r.f. low-noise preamplification device. It has shown the way to obtain distinctly better performance in the X and Ku band for communication. However, the device is not easy to produce in production quantities due largely to the immature state of GaAs technology in areas of materials and processing. Problems of immediate concern are the following:

1. Lack of high-quality substrate material having low background impurity and defect density
2. Lack of high-quality epi-layers having a high degree of thickness and dopant uniformity
3. Defects at the interfaces between substrates and epitaxial layers
4. Complex device processing steps including contact problems resulting in low yield
5. The necessity to etch mesas thus forfeiting the benefits of a truly planar technology

These same problems would plague any attempt to fabricate circuits which use the Transferred Electron Logic Devices. The transferred electron effect gives rise to the negative differential resistivity which, in turn, causes dipoles of charge to traverse two terminal samples of GaAs when the electric field between terminals is raised above a threshold level E_T . The TEL element consists of a two-terminal device fabricated (much as a MESFET) on a thin conductive layer supported by a semi-insulating substrate (as shown in Fig. 1.0-1). The thin conductive layer is capable of supporting a high field domain and since the distance between the contacts is $20\mu\text{m}$, the transit time of a dipole once formed at the source region is 2×10^{-10} sec (5 GHz). When the electric field everywhere is below E_T , no domains will be formed, but if one applies a negative pulse to a gate in the immediate vicinity of the source, then a domain forms at the source and will traverse the device length. While the domain is in transit, further negative pulses at the source gate do not

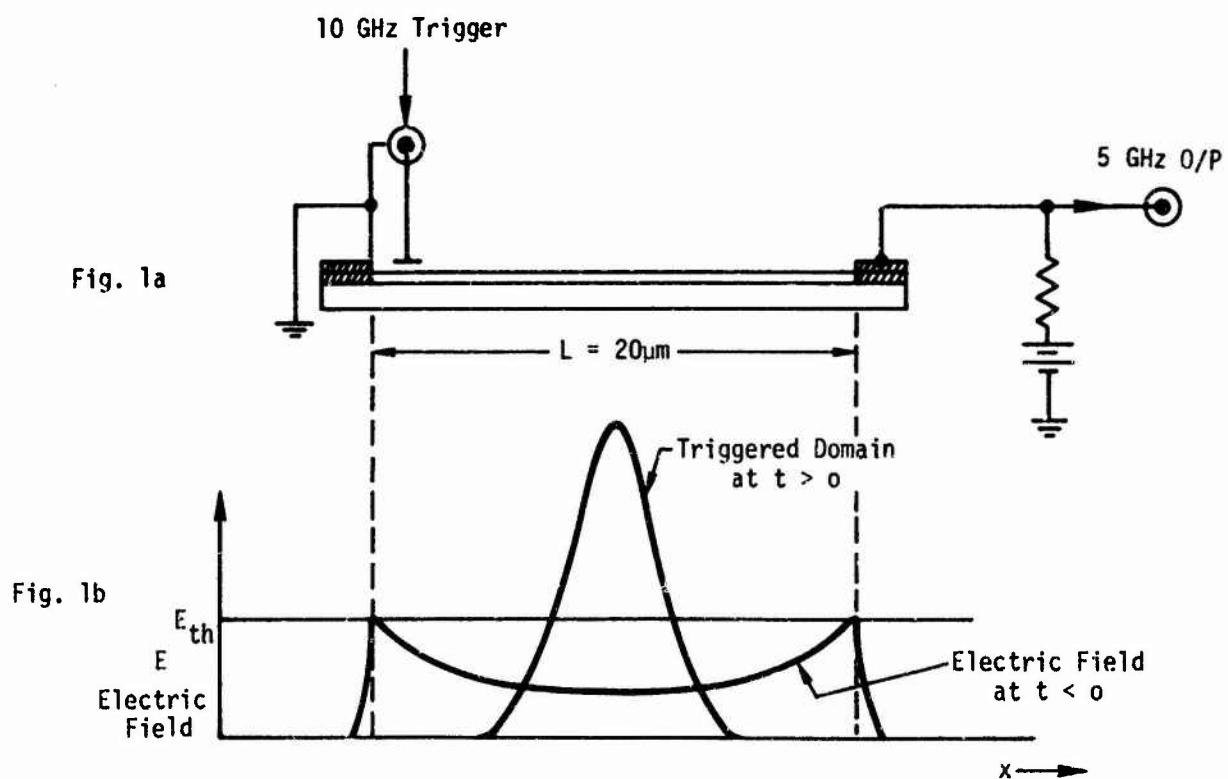


Fig. 1.0-1 A frequency divider-by-two using transferred electron logic.

generate new domains. Only after the domain has exited the drain and the field is restored to the "quasi-uniform" state will any effect be obtained from negative pulses on the source gate. Thus, we have the capability of frequency-dividing by choice of the drift length of the device. This is a very useful application and Figs. 1.0-1a and b show that 10 GHz can be divided by 2 if the length is 20 μ m. There are many applications for this type of device in delay lines, triggers, etc., and the list of possible usages is growing.

The TEL and the MESFET share a common geometry, and in monolithic combinations the common set of problems mentioned previously.

Our approach in the initial stages of this contract is to perform detailed studies in the following areas:

1. Growth and characterization of epi-layers by LPE and processing and fabrication of devices for the purpose of elucidating properties of the film, the interface, and the substrate. (In cooperation with Professor C. A. Lee at Cornell University and Professor G. L. Pearson at Stanford University.)
2. The growth and characterization of high-quality semi-insulating bulk material. (In cooperation with Professor J. M. Whelan at the University of Southern California.) Study of implantation techniques to make semi-insulating layers.
3. Implantation of n-type dopants into high-resistivity substrates (bulk or epitaxial) to obtain thin conducting layers and the technological problems involved in this. (In cooperation with Professor J. Mayer at the California Institute of Technology.)

2.0 PROGRAM GOALS AND TECHNICAL APPROACH

2.1 Epitaxial Materials Growth and Characterization

The activities discussed in this section include materials growth through device measurements. The goal is to investigate in practical devices the effects of material problems on device performance including gain, noise, yield, and lifetime. These problems may be related to epitaxial film properties such as thickness and free carrier level or substrate properties such as dislocation density, chromium density, and surface damage. The emphasis on the contract is LPE growth; however, we have established by company funds a chemical vapor deposition capability. We plan to perform comparative studies and, hopefully, arrive at a basic understanding of advantages and disadvantages of both growth techniques.

2.1.1 Ultra-Thin, High-Conductivity Layers

Measurements have indicated that the initial growth in normal liquid gallium growth systems takes place very rapidly. Figure 2.1-1 illustrates this problem best showing the thickness of a grown layer in an "unmodified" system as a function of time. It is observed that for a given saturation temperature initial growth is taking place very fast especially when there is a temperature gradient imposed at the liquid-solid interface as is the case in most orthodox LPE systems. The temperature gradient is introduced to avoid problems of constitutional supercooling and to ensure good surface morphology. The very rapid growth presents a problem to the grower of ultra-thin layers resulting in very short growth times and an uncontrolled process.

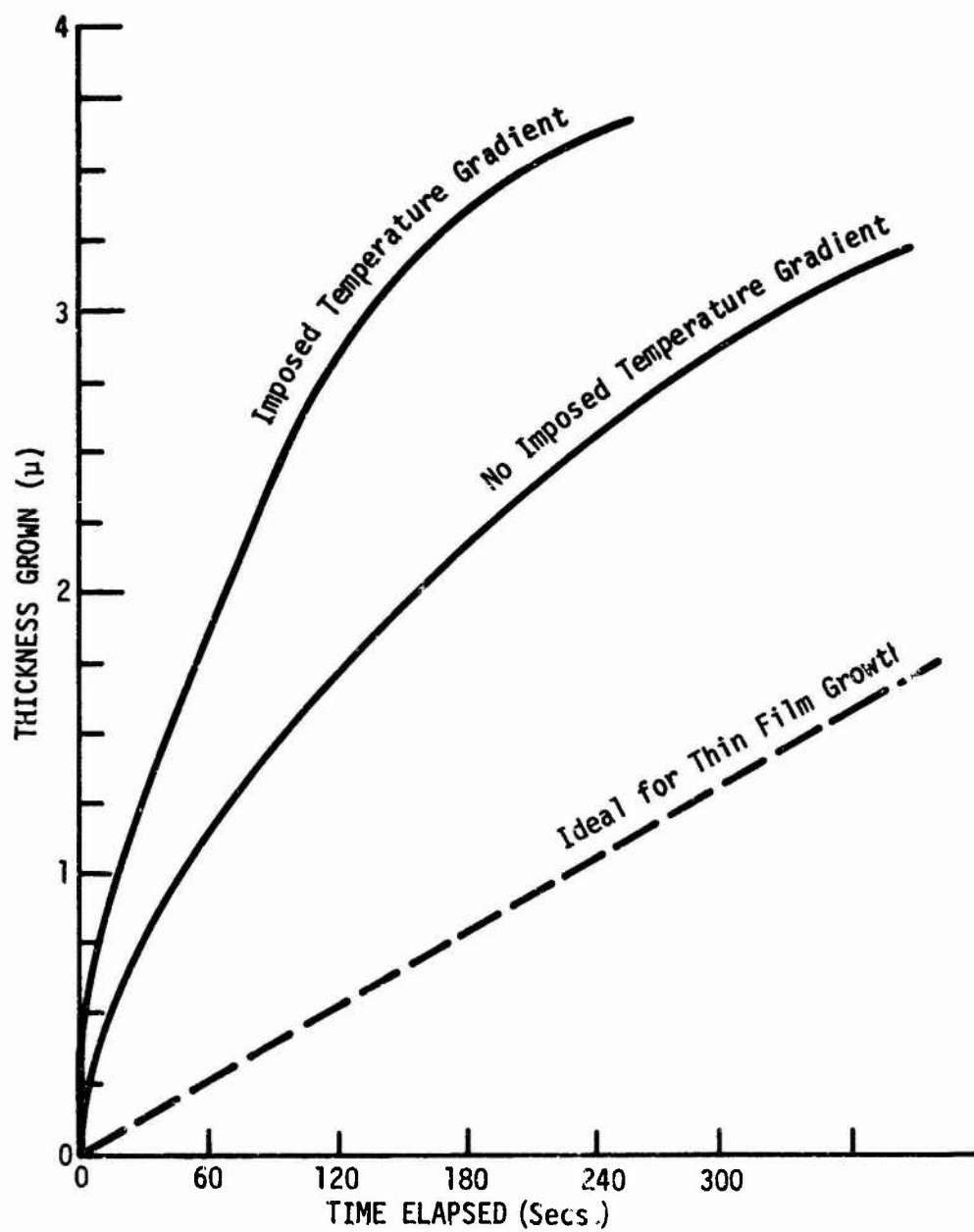


Fig. 2.1-1 Approximate growth rate-time elapsed nature of epitaxial lay deposition.

A new system for growth has been designed and built with company funds to accomplish the first step necessary to slow down initial growth rate. This step is to lower the temperature gradient at the liquid-solid interface without suffering the consequences due to constitutional supercooling. Growth experiments are being performed to calibrate the controls and see if the growth-rate-time-elapsed curve is more nearly ideal as in Fig. 2.1-1.

The attainment of a growth-time relationship near the ideal would greatly ease the problem of obtaining material for GaAs MESFET devices. As discussed in this report (Section 2.1.3), the thickness requirements on MESFET material are quite difficult to satisfy by ordinary growth techniques. The requirements for the low-power, low-noise FET's are:

Thickness in the range ($0.2\mu\text{m}$ to $0.3\mu\text{m}$)

Free carrier level in the range (6×10^{16} to 1×10^{17})

The characterization of the grown materials will include measurements of (a) free carrier level and its uniformity over a grown film, both in the plane of the film and through the film, (b) thickness and thickness variation across the film, and (c) mobility, possibly as a function of layer thickness.

2.1.2 High-Resistivity GaAs Thin Films

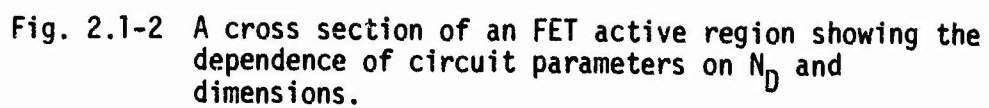
The research on this is being pursued at Stanford University. The objective of this work is to investigate chromium doping in liquid phase epitaxy to determine if at moderate temperatures chromium takes up the deep acceptor role resulting in semi-insulating material. If high-resistivity material results from this study of chromium doping at LPE temperatures, then it will be examined for application to the buffer layer problem in MESFET devices.

2.1.3 Processing and Device Measurements

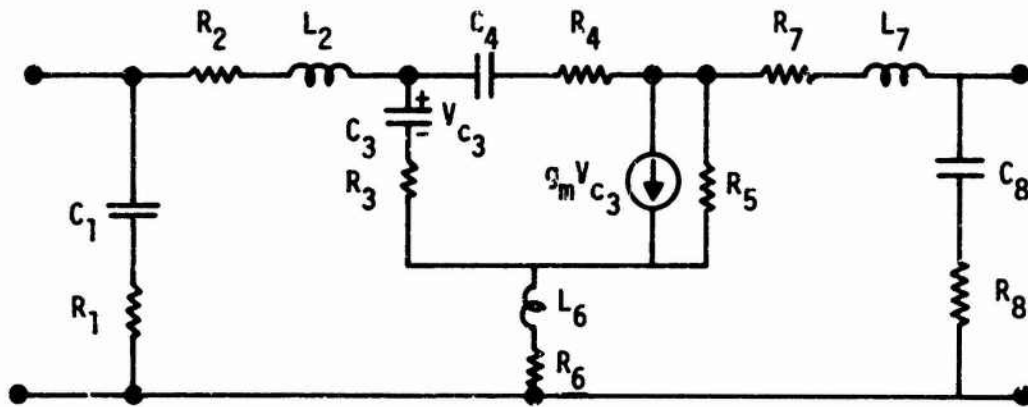
The central issue of our contract activity is what effects do known materials problems have upon the functioning of devices. To provide a starting point for such a discussion, it is advantageous to derive the optimum material configuration for the devices in question. This being done, materials problems are then treated as perturbations of these ideal conditions and the effects on the device are the more easily understood.

The devices considered are the MESFET and the IMPATT. Both of these devices are treated in a simple analysis to establish optimum materials requirements and then the program of measurements to be carried out is outlined.

2.1.3.1 MESFET. The basic picture of Field Effect Transistor action is depicted by Fig. 2.1-2. This is translated into the simple equivalent circuit of Fig. 2.1-3 where the parameters



STANDARD CASE EQUIVALENT CIRCUIT



$$g_{mo} = V_s C'_3 W$$

where W = gate width, V_s = saturation velocity, and C'_3 = capacitance per unit area under the gate

$$g_m(\omega) = g_{mo} \frac{e^{-j\omega\tau_1}}{1+j\omega\tau_2}$$

where τ_1, τ_2 (are functions of R_2, R_3 and C_3) and are $< 5 \times 10^{-12}$ sec

$$\omega_0 = g_{mo}/C_3 \quad \omega_0 = \text{frequency where current gain} = 1$$

$$\omega_{\max} = \frac{g_m}{C_3} \left[\frac{1}{2\sqrt{\frac{R_3+R_6}{R_5}}} \right] \quad \omega_{\max} = \text{frequency where power gain} = 1$$

$$U = \frac{g_m^2}{4\omega^2 C_3^2 \left(\frac{R_3+R_6}{R_5} \right)} \quad U = \text{Unilateral gain}$$

F_{opt} = Optimum noise figure

$$F_{\text{opt}} = 1 + 2\omega \sqrt{\frac{C_3^2 (R_3+R_6)}{g_m}}$$

Fig. 2.1-3 Some important relations governing the FET device performance.

are related to figures of merit of the device. There are certain simplifying assumptions made in arriving at the relations shown in Fig. 2.1-3. Firstly, the value for g_{mo} is derived on the assumption of a saturated carrier velocity. Secondly, to arrive at the simple expression for unilateral gain, the value of R_6 was added to R_3 and the "common" circuit branch δ was removed. These simplifications are done with the purpose of obtaining a first-order measure of the effects of the material parameters that determine the component values.

One observes from the expression in Fig. 2.1-3 that there is (1) an increase in transconductance, (2) a decrease in the values of R_3 , R_6 , and R_7 , and (3) an increase in the magnitude of unilateral gain U when there is an increase in the free carrier level N_D . The upper limit of the product of free carrier level N_D and thickness d of the epitaxial layer that may be used is imposed by the fact that we may, for a Schottky barrier, consider that breakdown occurs when the field beneath the metal reaches a value of 4×10^5 V/cm. Calculations based on this enable us to precisely specify a "breakdown" thickness (d_{br}) as a function of N_D . This is shown in the upper line of Fig. 2.1-4. In making an FET the "maximum tolerable" thickness must be some safety margin below the breakdown thickness. Let us sensibly maintain that the "pinch-off"

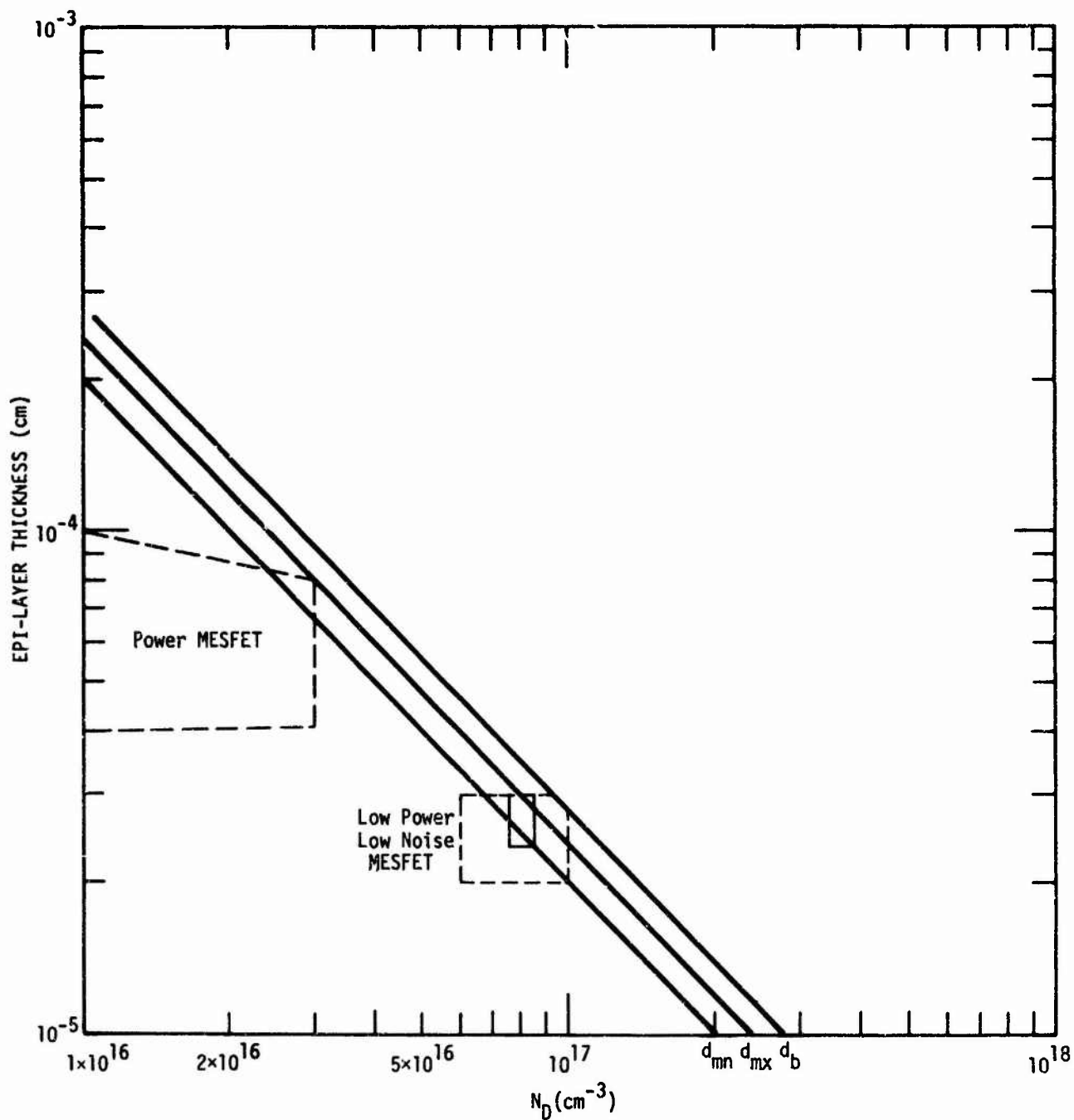


Fig. 2.1-4 The lines of constant $N_D d$ product that show constant unilateral gain contours. d_b represents the breakdown limit. d_{mx} represents the maximum allowable $N_D d$ product. d_{mn} represents a desirable lower limit on $N_D d$.

voltage shall not be more than 75% of the breakdown voltage.

The maximum thickness d_{mx} shall then be not more than 86% of the breakdown thickness. The lower limit thickness d_{mn} , set by consideration of performance, shall be that at which the unilateral gain in a simple equivalent circuit as in Fig. 2.1-3 shall be only 1 db below that available at the maximum thickness. Each of these three lines in Fig. 2.1-4 represents constant unilateral gain and a constant $N_D x d$ product.

So, Fig. 2.1-4 provides a guide as to the desirable thickness and carrier level for low-power, low-noise MESFET's. Higher power devices are made from material to the left in this diagram, and the thickness limitations are only tentative for this device as more conservative ratios of pinch-off voltage to breakdown voltage are needed in power transistors. This figure serves as a guide to relate desirable materials to the materials technology in that it gives the tolerable limits of thickness which may be compared with the attainable limits as of today. The attainable control of thickness is presently $0.25\mu\text{m} \pm 0.1\mu\text{m}$ with a uniformity of thickness on each layer of $\pm 20\%$.

From the figures that represent the present degree of control of thickness in growth, it would appear from the lines of constant $N_D x d$ product that N_D should be about $8 \times 10^{16} \text{ cm}^{-3}$. For a thickness of $0.25\mu\text{m}$, this means a pinch-off voltage of approximately 5 volts. Pinch-off voltage should not be allowed to go

lower than 5 volts in transistors for two reasons: (1) normal biasing for reasons of satisfactory output impedance levels and for moderately low power levels require at least 5 volts, and (2) transistor lifetime is greatly diminished if the breakdown voltage (which is only 30% higher than the pinch-off voltage) is allowed to be only 5 volts. For this reason the maximum N_D tolerable is 1×10^{17} .

The "tight" specification for thin films for use in GaAs MESFET's is as follows:

Free carrier level: 7.6 to $8.4 \times 10^{16}/\text{cm}^3$

Thickness between $.24\mu\text{m}$ to $.30\mu\text{m}$

This should be the long-term goal of the effort to grow epitaxial layers. Short-term specifications to be met are:

Free carrier level: 6 to $10 \times 10^{16}/\text{cm}^3$

Thickness: $.2$ to $.3\mu\text{m}$

This is shown by the broken-line-defined area to the right in Fig. 2.1-4. We have seen for Fig. 2.1-4 that lines of constant $N_D d$ are lines of constant unilateral gain in the simple equivalent network. It would be extremely useful to develop this kind of diagrammatic approach to show upon a similar diagram contours of maximum available gain and noise-figure or noise-measure optima. This shall be the goal of further study.

Measurements of the material effects in practice shall proceed using a sample transistor with gates designed to be $4\mu\text{m}$ long. Figure 2.1-5 shows the configuration of such a transistor. The mounting of these transistors shall be accomplished on headers and without the use of beam lead technology. Measurements of gain, noise, and power level will be correlated to materials parameters where possible.

2.1.3.2 IMPATT. The materials requirements for IMPATT devices depend, of course, on the frequency at which this device is designed to work. We, in our effort (mainly conducted at Cornell University by C. A. Lee), will concern ourselves exclusively with the Read diode structure. Devices will be fabricated from material grown either at the Science Center or at Cornell, and measurements will be made on these devices to derive information about the GaAs material using the theory of IMPATT reflection amplifiers derived at Cornell by Professor C. A. Lee. This theory will be briefly repeated in its essentials in the section on results.

The materials requirements may be briefly explained here by designing a diode to work with a minimum electronic reactance at 10 GHz. This design will be based on the present knowledge of GaAs properties such as avalanche ionization coefficients and

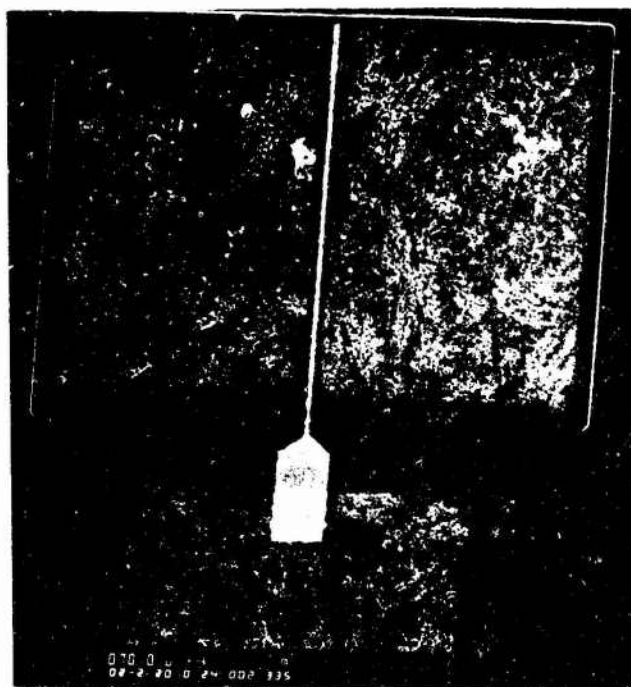


Fig. 2.1-5 A simple single-gate FET. Gate width, 4 μ m. This device is produced for experiments and general investigative work on GaAs thin epitaxial layers.

saturation velocity. Figure 2.1-6 shows the electric field form required of a Read structure. The peak electric field under the barrier at avalanche should be approximately 4×10^5 v/cm for GaAs. At this value of electric field, the holes in the reverse saturation current cause an avalanche multiplication by band-to-band ionization. The object of the Read structure is to have avalanche occur in as narrow a space as possible. This means reducing the electric field by a factor of 2 at least in as little as $3000\text{\AA}$. The avalanche region is followed by a drift region for the generated carriers. The drift region must have an electric field that is above saturation (3 KV/cm) everywhere. The drift region must be such that for a saturation velocity of 10^7 cm/sec, the time taken for charge to traverse the drift region is one-half a period at 10 GHz.

From the above specification, one can derive the profile of doping of the active regions of the IMPATT device.

First, the drift region must be $5\mu\text{m}$ long for a saturated drift velocity of 10^7 cm/sec, and we assume that the electric field at the "tail" or n^+ boundary on the positive contact is above 6 KV/cm and that the electric field at the avalanching region-drift region boundary is not more than 160 KV/cm, by Poisson's law we arrive at the conclusion that doping level in the drift region should not exceed $2 \times 10^{15}/\text{cm}^3$ --a level possible to achieve with

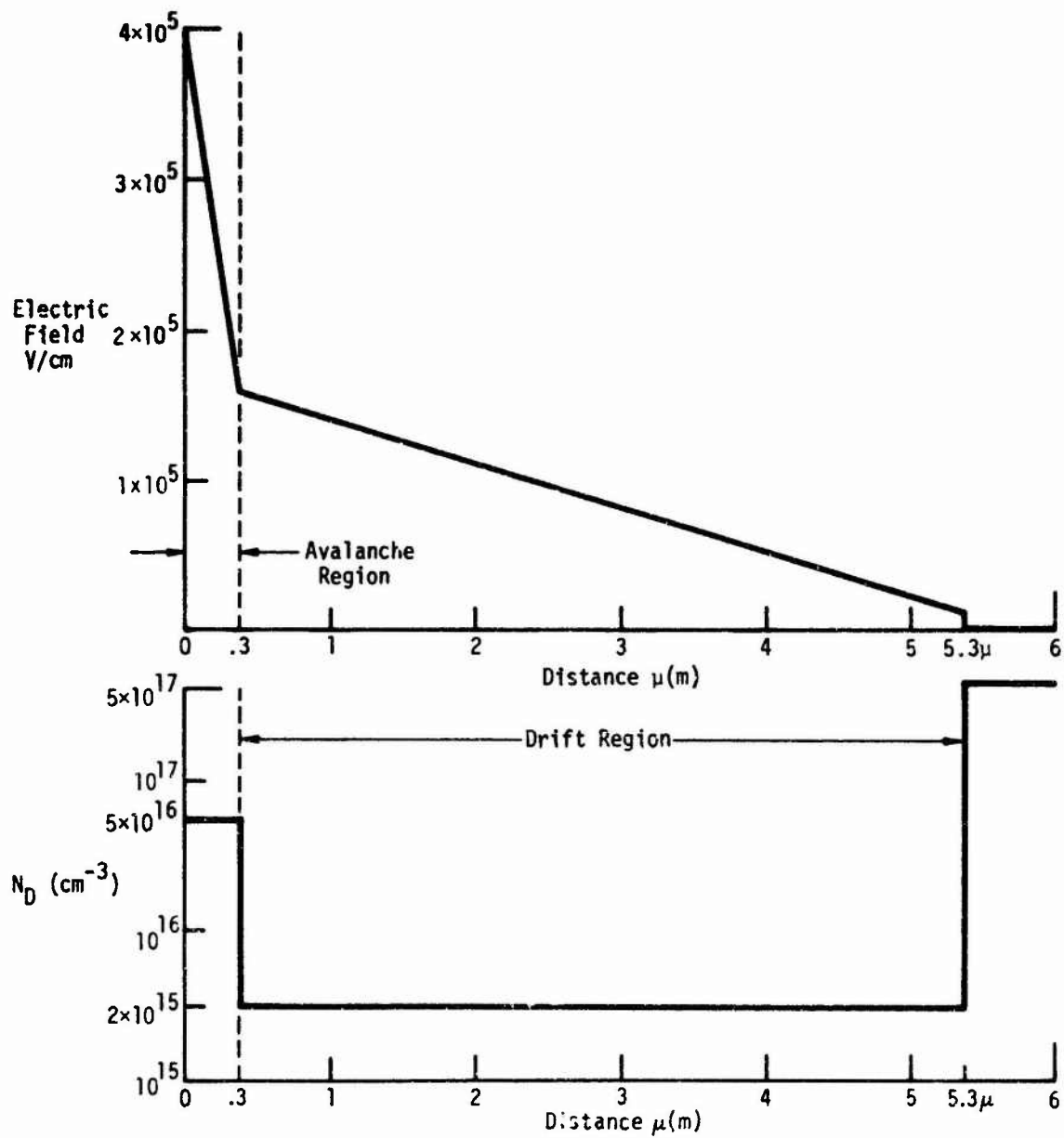


Fig. 2.1-6 Electric field and carrier concentration levels for a 10 GHz IMPATT device with transit angle of drift region ψ of 180° .

liquid phase epitaxy. The carrier level in the avalanche region should be such as to raise the electric field to 4×10^5 KV/cm in $.3\mu$. This calls for a $5 \times 10^{16}/\text{cm}^3$ doping level. These material parameters requirements are based on our present knowledge of GaAs. Mesa diode devices will be fabricated from such material, and measurements of gain versus frequency will be made on these devices with the aim of determining (a) whether the saturation velocity is 10^7 cm/sec or less, (b) the ionization rates of holes and electrons, and (c) material inhomogeneity. The reasoning that makes these deductions possible has its basis in the r.f. circuit and device analyses which are summarized in the section on results.

As a final note, indications are that the saturated velocity may be as low as 6×10^6 cm/sec (see the section on results). In this case the optimum drift region length is $3\mu\text{m}$. In this case the doping levels in both regions may remain the same, the changes will be in the avalanche voltage of the device and in the dielectric capacitance of the device.

2.2 Semi-Insulating Materials

The semi-insulating substrate is obtained by growth from the melt when chromium is used as a dopant. Important physical parameters that must be controlled are: (a) the excess of chromium sites active as deep acceptors over the background impurity; (b) the background impurity density, and (c) the density of native defects in the crystal.

The excess of chromium over background impurity level must be controlled in growth as closely as possible, for if this excess is large and exceeds the doping concentration of the thin n-type layer grown on the substrate, then the depletion layer of the p-n junction at the interface protrudes into the active layer. This has the added effect of placing a high electric field at this interface thus augmenting a noise problem due to defects at that interface. Furthermore, any change of the voltage applied to the interface; i.e., when a bias voltage is changed, has the effect of changing the penetration depth of the depletion layer into the active layer. This changes the characteristic of the device. Ideally, the solution is to keep the excess of Cr one order of magnitude below the doping concentration of the active layer so that the penetration of the depletion region into the active layer is negligible. However, this is a stringent requirement on the substrate material because the ideal carrier concentrations for a MESFET epi-layer is as low as $6 \text{ to } 10 \times 10^{16} \text{ cm}^{-3}$ (see Sections 2.1.1 and 2.1.3), and excess Cr is likely to be of the same order in commercially-available semi-insulating GaAs, as indicated by mass spectroscopy analysis (see Section 3.2.2). On the other hand, if the excess of deep acceptors over background donors is too low, then isolation between adjacent elements at different potential levels is easily lost because the threshold for transition to space-charge-limited current flow between these elements is seriously lowered.

The background impurity level of such chromium-doped material is a donor and it would be extremely advantageous to lower this from two points of view. A lower background level means that the chromium level may be made lower with-

out sacrificing isolation and, secondly, the material would be better fitted for use in such applications as implantation and epitaxial growth thereon.

The native defect density of melt-grown crystals of GaAs, measured by counting etch pits, is between 10^3 and $10^4/\text{cm}^2$. Growth of epitaxial layers generally attenuates point defect density but line defects and stacking faults in the substrate can and do propagate into the epitaxial layer. In so doing they diminish the electrical figures of merit of those films, particularly when they are thin as are most of the films with which this technology is concerned.

Other means for producing semi-insulating GaAs must be considered. It is known that proton bombardment and ion implantation can serve such a purpose. At the present time, the main usefulness of ion beam generation of thin layers of semi-insulating GaAs is in avoiding etching mesas to make devices. In addition, it opens possibilities for new device structures. However, before these techniques can be effectively used in device production, correlations must be established between ion beam dosage and annealing process on one side, and physical parameters of the semi-insulating films on the other--the phrase "physical parameters" being used in the same sense as in the preceding discussion of the bulk semi-insulating substrate. It is necessary to reach the point where ion beam dosage and annealing parameters can be prescribed as part of the design of a device--ideally from a table where physical parameters are listed as functions of the ion beam processing parameters.

2.2.1 Crystal Growth

This aspect of the program was conceived as the fundamental step in a feedback loop consisting of growth of semi-insulating substrates, physical measurements on the substrates, epitaxial film growth, measurements of film properties, device fabrication, and device measurements. All the feedback information would be used for improvement of the quality of the substrates.

Until USC, the supplier of substrate material, starts producing good-quality semi-insulating GaAs, the program will depend on commercial suppliers. The above sequence of operations will be performed in an "open-loop" manner. The goal will be to establish correlations between physical properties of the substrate and device performance, and to evaluate available materials against the requirements. From here, some specifications will be drawn for USC and other institutions interested in growth of semi-insulating GaAs.

2.2.2 Measurement Techniques

Given the small amount of information published on semi-insulating GaAs, there is a wide choice of measurement techniques which can yield valuable information on the material. In the first period of this contract the choice of techniques was broad in order to explore in a practical way the advantages and difficulties of different types of measurements. In the following phase it becomes important to be very selective in order to avoid spreading the efforts. In spite of the scientific

March 5, 1974

interest aroused by some of the initial measurements, it is necessary to select only those that can yield the most relevant information from the standpoint of this contract.

As discussed at the beginning of Section 2.2, the most relevant bulk parameters are the depth of the Cr impurities (acceptably well known), the depth of the background impurities, the chromium density, and the background impurity density. It is important to monitor the variation of these parameters between different manufacturers and to monitor uniformity in a boule. It is equally important to correlate these parameters with the device performance. The actual identification of impurities takes a second place until there is interaction with crystal growth. Some consideration must also be given to breakdown effects in the substrate because these effects are important for device design. On the other hand, from measurements on the surface, the most relevant parameters to be obtained are density and uniformity of native defects. Here nondestructive measurements are very desirable.

Four types of bulk measurements are programmed:

2.2.2.1 Analytical Measurements. These are routine analyses of impurity content. In view of the tests done in the first period of this contract (see Section 3.2.2), mass spectroscopy will be used almost exclusively.

2.2.2.2 Quantitative Measurements of Impurity Concentrations.

In standard semiconductor technology, the fastest technique to determine concentrations and activation energies of impurities is measurement of resistivity and Hall constant as functions of temperature. However, in semiconductors overcompensated by deep acceptors, only the activation energy of the acceptors (which is already known) and the donor-acceptor density ratio can be obtained.¹ At the same time, the measurement technique becomes more difficult than in low-resistivity semiconductors. An additional difficulty is to make reliable ohmic contacts. On the other hand, capacity measurements are proving very effective.² Transient high-frequency capacity measurements at Schottky barriers and p-n junctions are emerging as powerful techniques for the measurement of concentrations of both shallow and deep impurities, plus activation energies of deep impurities.³ This technique is very appealing because the instrumental requirements are not complex and the sample preparation is easy. In our case, Schottky barriers are easy to make by metal evaporation, and n-semi-insulator junctions are made when n-type layers are grown on the semi-insulating substrate for the construction of devices. However, the transient capacity technique has been applied almost exclusively to n- or p-type materials with some deep traps. The method is now under evaluation in order to determine its prospect for semi-insulating GaAs where the density of deep traps is dominant.

2.2.2.3 Complementary Measurements. Photoconductivity and thermally-stimulated current measurements will continue in order to complement the information on total impurity concentrations and average activation energies from the measurements described above with more fine information on the position of the impurities in the gap. These measurements will be made on the same type of n-i-m and p-i-m structures that have already been used (see Section 3.2.2). In addition, low voltage breakdown effects which occur below the predicted trap-filled voltage will be studied. However, consistent with the discussion at the beginning of this section, this set of measurements will play a secondary role.

2.2.2.4 Measurements on Devices. Some of the measurements enumerated under 2.2.2.2 and 2.2.2.3 will be made on actual MESFET devices. This is possible to do with capacity measurements and measurements of breakdown voltages. The devices may be modified in some cases; i.e., thinning the substrate or removing the gate. The purpose here is to establish correlations between parameters of the substrate and the low-frequency characteristics of the devices.

With regard to surface measurements, it was shown that X-ray topographs can be used in several semiconductors, GaAs included, to reveal dislocations.⁴ The appeal of X-ray topography is in that it is a nondestructive technique. Mapping of dislocations on the substrate can be done before growing the epitaxial layer, and the properties of the film can be related back to the dislocation map. Unfortunately, no work has been done on semi-insulated GaAs by X-ray topography, but the technique should be applicable. The question is whether it is sensitive enough. The sensitivity will be tested by comparing with dislocation etches. If the sensitivity will be insufficient, it will still be possible to do dislocation etches and repolish the substrate surface before the film is grown.

2.2.3 Proton Bombardment and Oxygen Implantation

As discussed in Section 2.2, the goal is to convert thin epitaxial layers of n-type GaAs into semi-insulating material mainly in order to eliminate mesa-etching in device fabrication. Both proton bombardment and oxygen implantation have successfully produced semi-insulating material. However, fundamental questions still remain. Proton bombardment generates high-resistivity material by introducing damage.⁵ Such damage could, in principle, be removed by annealing. The main question is whether the operating temperature of a device is sufficient to degrade the resistivity of the material by annealing effects over a long period of time. Such a question is vital for device applications. On the other hand, oxygen implantation is more likely to achieve high resistivity by impurity com-

pensation. There are indications⁶ that it is possible to achieve a high resistivity material stable after annealing at high temperature. This suggests oxygen implantation as a more reliable technique. However, it is possible to penetrate deeper into the material with proton bombardment than with oxygen implantation. This is an advantage of proton bombardment when thick semi-insulating layers are required.

From the above discussion, it is clear that it is not possible to make a clear-cut choice between the two techniques. Some initial work has been done by proton bombardment in the initial phase of this contract. This work will be continued and similar work will be done by oxygen implantation. The evaluation of the films will be made by the same techniques proposed for semi-insulating substrates (see Section 2.2.2).

In this work some attention will be in gathering practical information on dosage, energies, exposure times, and annealing parameters for direct use in device fabrication.

2.3 n-Type Doping of GaAs by Ion Implantation

Our past experience with tellurium implantation in GaAs has shown that the use of a cap material during annealing, which is a diffusion mask for gallium as well as for arsenic, is essential in obtaining good electrical activity from the implanted tellurium.^{7,8} Difficulties have been encountered, however, in obtaining reproducible films to use as an annealing cap. These difficulties must be overcome in order to obtain consistent doping results by implantation. Some information on the characteristics of n-type layers pro-

duced by tellurium implantation for different implant and anneal temperatures and varying doses, has been obtained. Considerable further information is required in order to effectively apply implantation to device fabrication. As this information is obtained, it is important to begin using implantation for device fabrication and to evaluate the characteristics of the device produced in this way. The details of our program in these areas are given below.

2.3.1 Annealing Cap

The deposition of AlN films (see Section 3.3.1) by reactive sputtering will be investigated to determine the parameters necessary to obtain films of reproducible composition and density which give consistently good protection of the surface of GaAs during high temperature annealing. Composition of the films will be determined using helium ion backscattering. Ellipsometry measurements will be performed in order to determine the film thickness and index of refraction. The density of the films can also be obtained from the backscattering data using the thickness determined by ellipsometry. The effectiveness of films as an annealing cap will be studied by determining the change in the electron concentration near the surface of n-type epi-layers covered with the film and annealed to temperatures in the range between 750° and 900°C. Our previous work indicates temperatures in this range are required to obtain good electrical activity in tellurium-implanted GaAs.^{7,8} Some work is in progress with company funds to attempt to understand why these rather high annealing temperatures are required.

2.3.2 Characteristics of Implanted Layers and Junctions

The objective is to obtain an understanding of the effects of implantation temperature, anneal temperature, and dose on the maximum electron concentration and the electron concentration and mobility profiles obtained by ion implantation. Initially the work will concentrate on the implantation of tellurium. Chromium-doped semi-insulating GaAs, p-type GaAs, and n-type epitaxial GaAs will be used as substrates for the implantation. This will facilitate the detection of possible effects of the substrate on the implantation results, and permit the determination of the properties of implanted p-n junctions in the case of p-type substrates. The implanted layers will be investigated using capacitance-voltage measurements, Hall effect, and resistivity measurements and stripping and sequential Hall and resistivity measurements. Goals are the production of n-type layers suitable for FET fabrication and the attainment of high doping concentration for application to contacts.

2.3.3 Device Processing, Fabrication, and Evaluation

FET's will be fabricated in thin n-type layers produced by ion implantation. Initially, this work will involve making devices with a $4\mu\text{m}$ gate so as to avoid the critical fabrication problems connected with the use of the very short gate required for state-of-the-art high-frequency devices. Mesa etching and Au-Ge contacts will also be used. The properties of the implanted devices will be compared with those

fabricated with the same geometry in epitaxial films. After this work is underway, improvement of contacts may be attempted using implantation. Consideration will be given to the development of fabrication techniques permitting the most advantageous use of implantation, such as a planar process for FET fabrication.

3.0 RESULTS

3.1 Epitaxial Material Growth and Characteristics

3.1.1 Ultra-Thin, High-Conductivity Layers

In the past quarter we have acquired a profile plotter to provide a considerable assist in the measurement and characterization of the thin layers grown here. This instrument automatically converts C-V data being measured into a plot of carrier concentration level versus distance below the surface. This plot is obtained directly on-line in hard copy. From these plots topographic maps are drawn and an example of such a map is in Fig. 3.1-1. On this, areas of the same "altitude" are separated by lines. It is noticeable that there is a "mound" in the center as noticed in early growths, but in this, representative of the later growths, the mound is considerably less than before. The tendency to grow thicker at the corners is more noticeable now also. Nevertheless, the crystal depicted is uniform, and if the carrier level were correct, would produce many fine MESFET's. As discussed in Section 2.1.3, thickness of the epitaxial layer is a prime determinant of current levels, transconductance, and gain and should be controlled to within $\pm 20\%$ at least for a uniformity of gain of ± 1 db.

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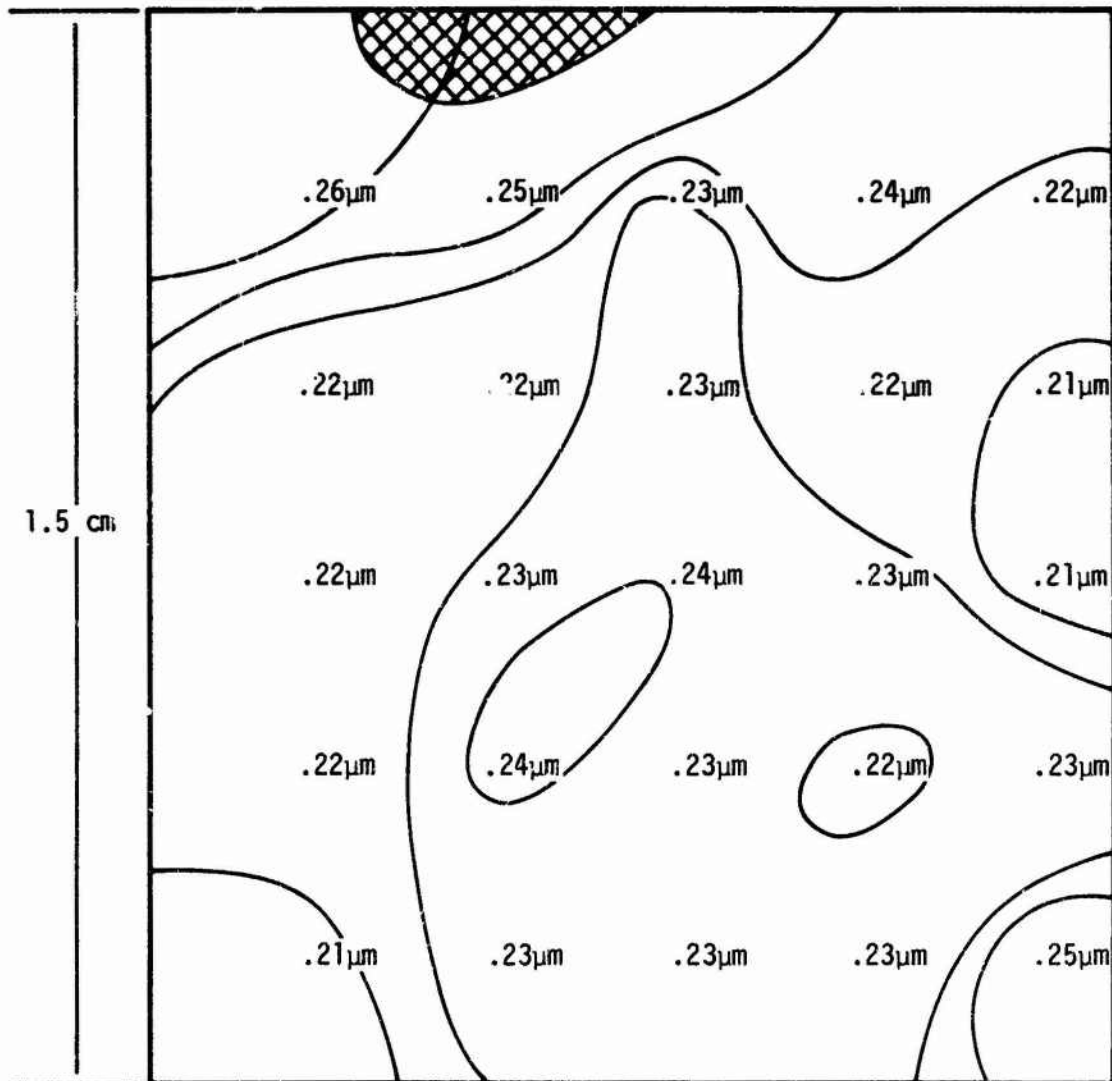


Fig. 3.1-1 Thickness variation of a layer grown in liquid phase epitaxial growth system. Thickness is $0.23 \pm .02 \mu\text{m}$.

3.1.2 High-Resistivity GaAs Thin Films

A horizontal tilt system with a temperature gradient cell⁹ was assembled and used for growth of LPE GaAs. The cell, as shown in Fig. 3.1-2, consists of a high-purity graphite growth cell floating on a liquid Ga reservoir contained in a graphite cradle together with a quartz heat transfer tube which is immersed in the Ga reservoir. H_2 flows through a system as a cooling gas. The horizontal tilt system is shown in Fig. 3.1-3.

The starting materials are 6 9's GaAs from Alsuisse Company, an undoped polycrystalline GaAs source (Asarco), and Cr-doped semi-insulating GaAs single crystal substrates (Laser Diode Laboratories). All substrates are oriented to the (100) crystallographic plane within $\pm 0.5^\circ$. They had an etch pit density of 8700 cm^{-2} , and a resistivity of $5.2 \times 10^7 \text{ ohm-cm}$.

The transient method was employed for the growth with a saturation temperature from 600 to 700°C and cooling rates from 600 to 700°C/hr. The procedure for growing an epitaxial layer consists of the following steps: (1) substrate preparation and cleaning¹⁰; (2) after loading the substrate, the reactor tube is purged with H_2 for 2 hours; (3) the saturation temperature is stabilized for 30 minutes to insure uniform As saturation of the Ga solution; (4) during saturation, the cooling gas is forced through the heat transfer tube to induce a temperature gradient of

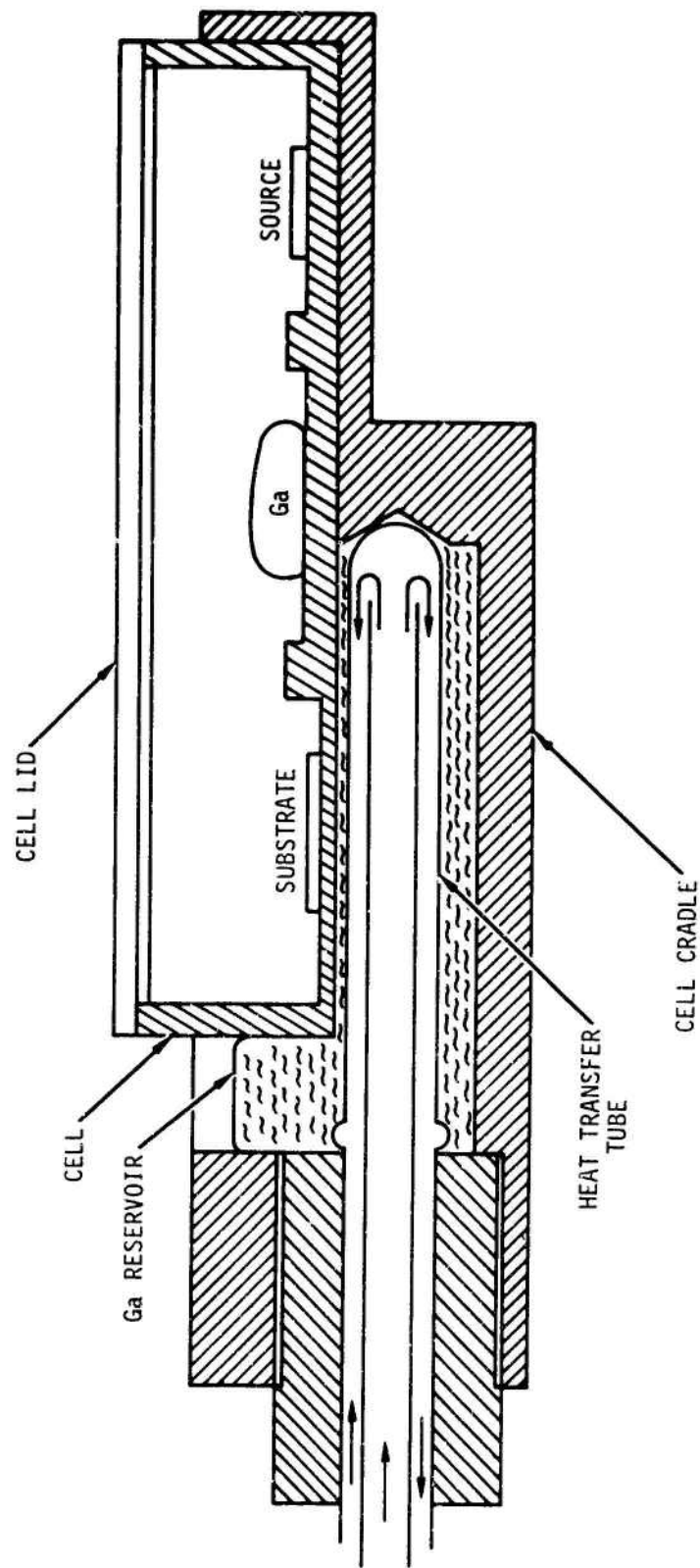


Fig. 3.1-2 A growth cell for liquid phase growth of epitaxial GaAs. The cell is specially designed to impose a uniform temperature gradient at the substrate-liquid interface.

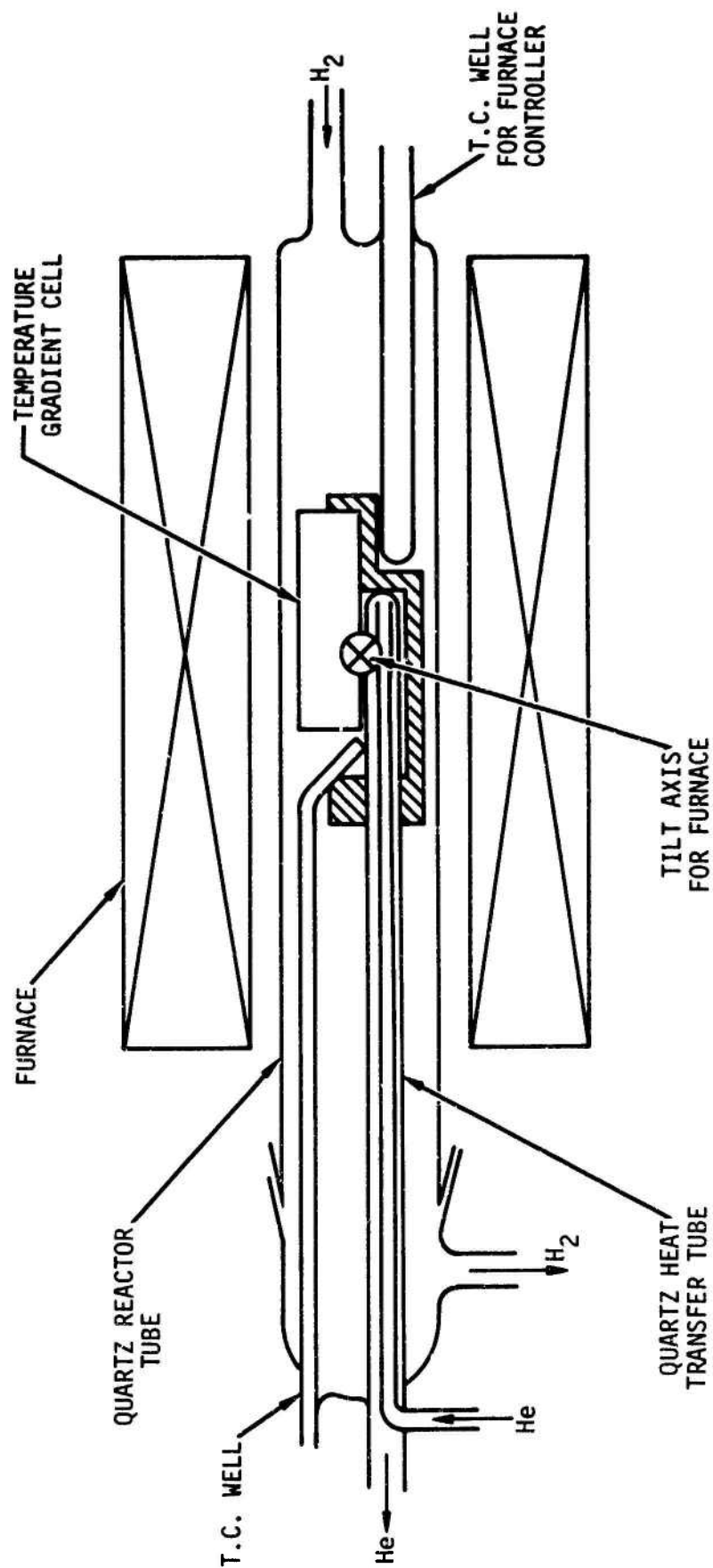


Fig. 3.1-3 A system for the liquid phase growth of epitaxial GaAs.

approximately $5^{\circ}\text{C}/\text{cm}$ to $10^{\circ}\text{C}/\text{cm}^2$; (4) the furnace is tilted to roll the As-saturated Ga onto the substrate, and (6) the furnace is then cooled at an initial rate of 600 to $720^{\circ}\text{C}/\text{hr}$ in order to epitaxially grow GaAs on the substrate from the As-saturated gallium solution.

The carrier density and mobility of the epitaxial GaAs layer were evaluated by the Van der Pauw technique at 300 and 77°K . Ohmic contacts were made using 10-mil-diameter spheres and alloying them at 400°C for 4 minutes under vacuum. Schottky barrier diode C-V measurements were also made on sample Nos. 206 and 207 to determine the carrier density profile. The carrier densities from Schottky barrier measurements are about 2 to 3 times larger than that obtained from Van der Pauw measurements. The epitaxial GaAs growth conditions and properties are summarized in Table 3.1-1.

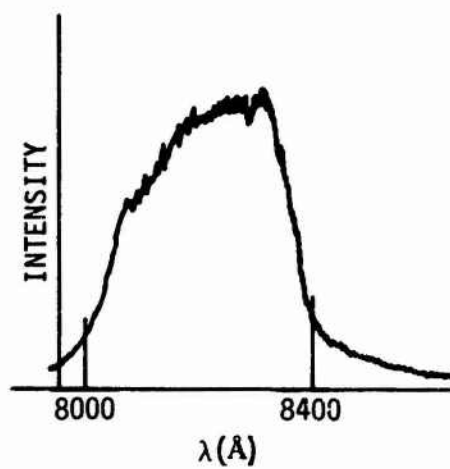
Sample Nos. 207 and 208 were grown after adding 1.7 mg of Cr into 5 gm of As-saturated Ga solution. Photoluminescence measurements, using an Ar-laser ($4800\text{\AA}$) as an excitation source, were used to examine the difference of the photoemission spectra between samples before and after adding Cr into the melt. The spectra near the band-to-band emission region are shown in Fig. 3.1-4.

3.1.2.1 Summary of Results

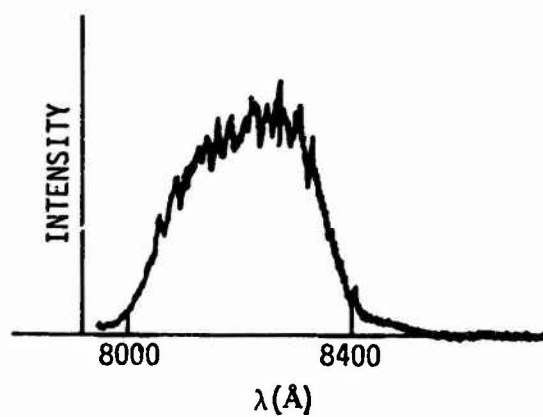
1. From Table 3.1-1, we see that the electrical properties improved after a few successive growths at fixed bakeout and saturation temperatures.

Table 3.1-1
Epitaxial GaAs Growth Conditions and Properties
(H₂ Flow Rate, 0.6 l/min)

Growth No.	Substrate Orientation	Bakeout		Saturation Temp. (°C)	Cooling Rate (°C/hr)	Mobility 300/77°K (cm ² /V-s)	Carrier Density 300/77°K (cm ⁻³)	Thickness (μm)
		Temp. °C	Period (Hrs.)					
101	(100)	650	38	700	600	3430/10,947	2.64×10 ¹⁶ /1.67×10 ¹⁶	19.2
102	(100)	650	15	700	75	6017/16,383	2.96×10 ¹⁶ /2.04×10 ¹⁶	18.2
103	(100)	650	20	700	75	4372/16,207	1.43×10 ¹⁶ /9.1×10 ¹⁵	19.6
104	(100)	650	28	650	720	4547/35,580	2.55×10 ¹⁵ /1.77×10 ¹⁵	11.2
105	(100)	650	28	650	600	4074/26,341	7.8×10 ¹⁵ /4.7×10 ¹⁵	9.6
106	(100)	650	24	650	660	4700/32,600	1.4×10 ¹⁶ /9.3×10 ¹⁵	8.9
107	(100)	650	20	600	600	3553/19,368	5.15×10 ¹⁵ /3.7×10 ¹⁵	5.8
108	(100)	650	26	600	600	5184/35,927	5.17×10 ¹⁵ /3.46×10 ¹⁵	5.6
New Ga and GaAs Sources								
201	(100)	580	79	600	600	Discontinuous Hillocks		
202	(100)	579	24	598	600			
203	(100)	667	25	706	720	4913/24,037	3.27×10 ¹⁵ /2.48×10 ¹⁵	24.9
204	(100)	680	18	697	720	6287/32,507	2.98×10 ¹⁵ /2.3×10 ¹⁵	18.2
205	(100)	589	21	590	600			
206	(100)	680	22	711	700	6515/44,062	1.65×10 ¹⁵ /1.4×10 ¹⁵	16.7
Added 5-9s Cr to Melt								
207	(100)	680	24	704	720	5260/18,876	4.65×10 ¹⁵ /3.39×10 ¹⁵	12.0



(a)



(b)

Fig. 3.1-4 Photoluminescence spectra on undoped (a) and chromium-doped GaAs grown from Ga. The excitation for these measurements was provided by an argon laser beam.

2. The thickness of the epi-layer is determined by the amount of As dissolved in the Ga at the saturation temperature, since no means is provided to wipe the melt off the substrate during growth.
3. At 600°C saturation temperature, discontinuous hillocks appeared on the substrate. This may be due to supercooling that occurs with high cooling rates and/or an oxide on the surface that was not reduced.
4. The background carrier density, before adding Cr, is in the low 10^{15} cm^{-3} range, with 300/77°C mobilities around 6,500/40,000 $\text{cm}^2/\text{v-sec}$. The thickness ranged from 5 to 20 μm for initial growth temperatures between 600 and 700°C.
5. From preliminary studies, after Cr is added, the carrier densities increased. From the photoluminescence spectra, no Cr peaks appeared either in the mid-band region or band-to-band emission regions but additional shallow levels appeared after adding Cr (Fig. 3.1-4). The possible reasons for this behavior are: (1) due to the very small segregation coefficient of Cr ($\sim 10^{-5}$),¹¹ the amount of Cr getting into the solid is not large enough to compensate the residual shallow level impurities;

(2) for growth temperatures below 850°C, Cr in the GaAs may act as an n-type impurity, and (3) the impurities contained in the 5-9's Cr may predominate.

3.1.3 Processing and Device Measurements

3.1.3.1 MESFET. The ohmic contacts which form the drain and source areas of an FET device in GaAs are a very critical factor in determining the performance of the device. It is desirable that the contacts be "deep" in the sense that the very high conductivity region penetrate far into the epitaxial layer. This is shown in Fig. 3.1-5 where the configuration of an ideal FET is shown. This deep contact avoids the spreading resistance associated with a contact where the very high conductivity region of which was confined to the surface. Simple calculations of this spreading resistance for a surface-confined contact on an epitaxial layer such as one might use for an FET (0.25 μ thick and $7 \times 10^{16}/\text{cm}^3$ carrier level) reveals that the spreading resistance may be as high as 20 ohm for a contact 500 μm by 50 μm in dimension.

One of the ways to obtain a deep contact has been to use the eutectic alloy of gold-germanium to form the contacts by dissolving and regrowing the GaAs in the ohmic contact area. This has been unsatisfactory because of the uncontrollable regrowth characteristics. The alloy dissolves the GaAs deeply, but upon cooling the

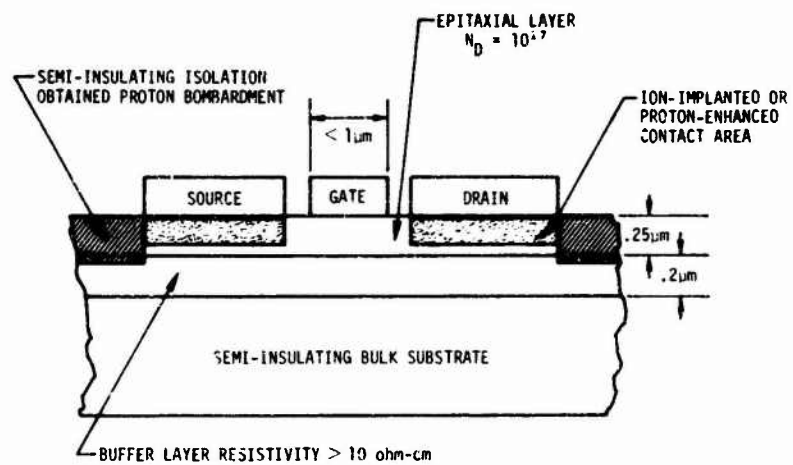


Fig. 3.1-5 Configuration of an ideal FET where the ohmic contacts are deep into the active layer and the device is dated by means other than mesa etching

gold and GaAs segregate in a manner illustrated by Fig. 3.1-6. This honeycomb-like interspersing of GaAs and gold solid phases raises the contact specific resistance. The dark areas in the figure appear to X-ray analysis as GaAs with a small content of gold and germanium. The bright areas are gold almost entirely with a small content of gallium and arsenic. The specific resistivity of such a contact is much higher than it would be if a uniform metallization had resulted from the alloying. This solid phase segregation proved to be a persistent problem in the use of the eutectic and for this reason the eutectic alloy was abandoned in favor of separate deposition of germanium and gold.

The experiments conducted so far seem to indicate that the deposition of 100Å to 200Å of germanium followed by 3000Å to 4000Å of gold and a subsequent alloy at 500°C produces a very satisfactory deep contact. The deep nature of this contact is judged from measurement of specific resistance of dot contacts on a thin epitaxial film. When the dots are small and the distance between pairs of dots known, the specific resistance of the dot contact may be derived.

The contact resistance is a function of the alloy temperature and has an optimum temperature at between 500°C and 550°C. At temperatures above 550°C, marked deterioration occurs in the uniformity or smoothness of the metal leading to an increase in

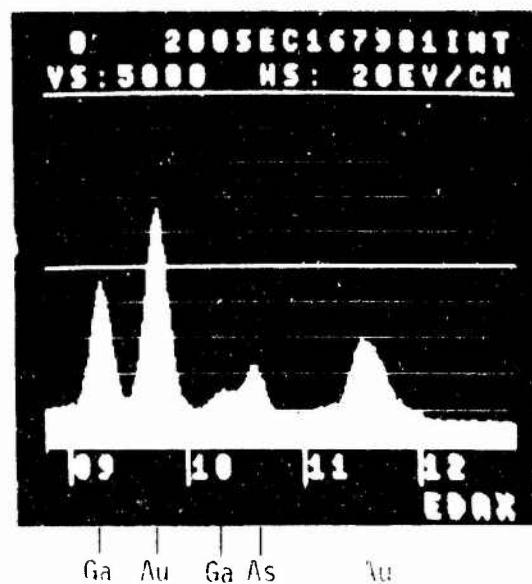
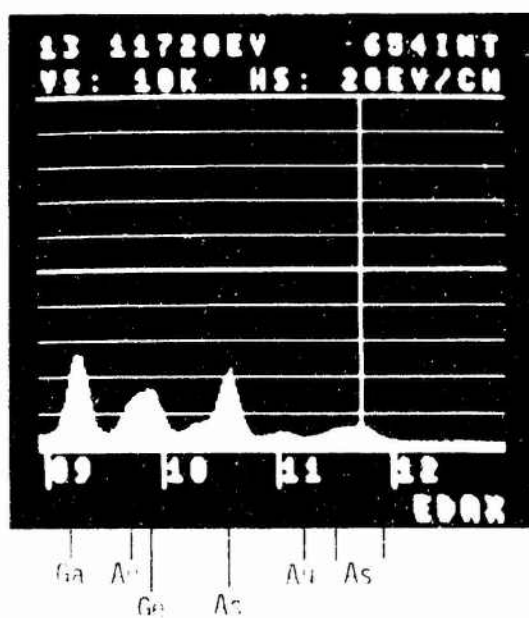
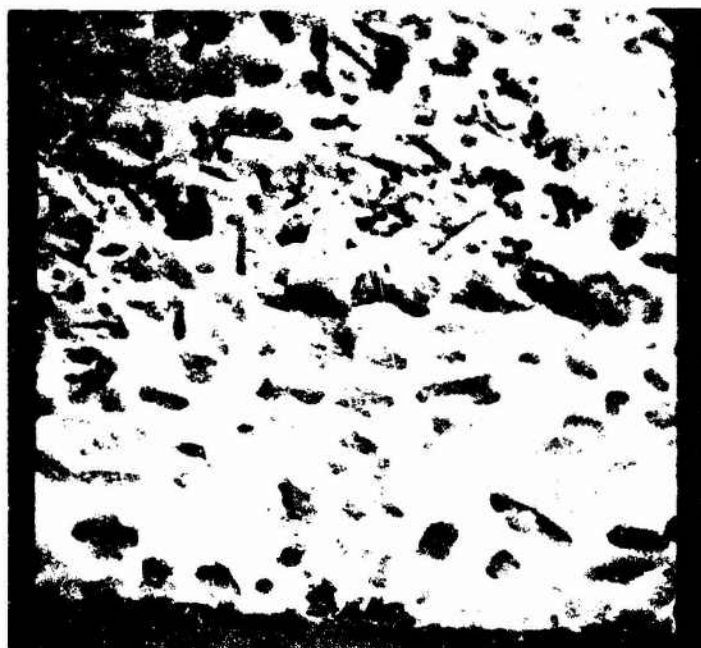


Fig. 3.1-6 SEM X-ray energy dispersive analysis on the contact area obtained by the alloying of eutectic gold-germanium at 450°C for 2 minutes. The analysis reveals a segregation of the GaAs-Au into two separate solid phases

resistance of the contact. The specific resistance measured for these contacts was 5×10^{-4} ohm-cm² when alloyed at 500°C.

There is room for improvement here and current work is experiments with multiple layer metallization to improve lifting and alloying quality.

The SEM is being used to evaluate the depth of contacts using secondary electron images. Future work will use Auger electron analysis.

Figure 3.1-7 is of a gate metallization over a mesa edge. There is a microcrack evident in the metal right at the mesa edge. This problem of the difficulty of ensuring, successfully, metallization up the sides of such mesas provides the motivation for investigating proton bombardment as a means of converting the surrounding epitaxy around an FET structure into semi-insulating.

Figure 2.1-5 is a picture of a 4μm gate FET. This simple device shall provide the means to do the measurements that are called for in the evaluation of improvements in materials and processing. Processed without the aid of electron beam lithography, it is a much cheaper device than state-of-the-art devices and can be used quite effectively in our program.

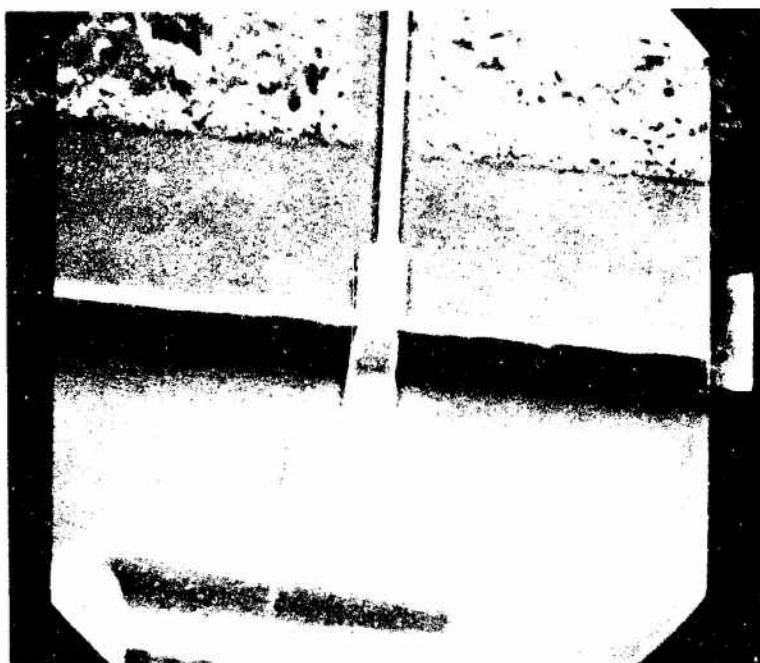


Fig. 3.1-7 SEM photomicrograph showing a metallization break in the gate at the point where it climbs the edge of the mesa

3.1.3.2 IMPATT. The IMPATT activities are aimed at relating material and device properties to the performance of amplifier ensembles. This relation being established then provides a means of checking on device or material properties. To achieve this, analytical work has been performed on both the device physics and the circuit problems, and the common link in both analyses is a factor called the electronic reactance factor Q_p which is a measure of the electronic reactance of the device divided by the electronic negative resistance. This factor Q_p may be derived from the measurements made of gain in a reflection amplifier and then expressed in terms of device quantities.

The microwave setup is a simple cavity-mounted diode reflection amplifier upon which measurements are made of (1) small signal gain vs frequency at different set values of device d.c. current, and (2) power output vs frequency at different levels of input power and fixed device current.

Figure 3.1-8 illustrates an equivalent circuit for the total ensemble of cavity components, device components, and load.

Figure 3.1-9 are the results from measurements of small signal gain on such a cavity as a function of different levels of device current. It is evident that there is a shift in the gain peak frequency and an increase in gain peak value for each increase in current. From the theory of the microwave reflection amplifier, the small signal peak gain is given by the expression

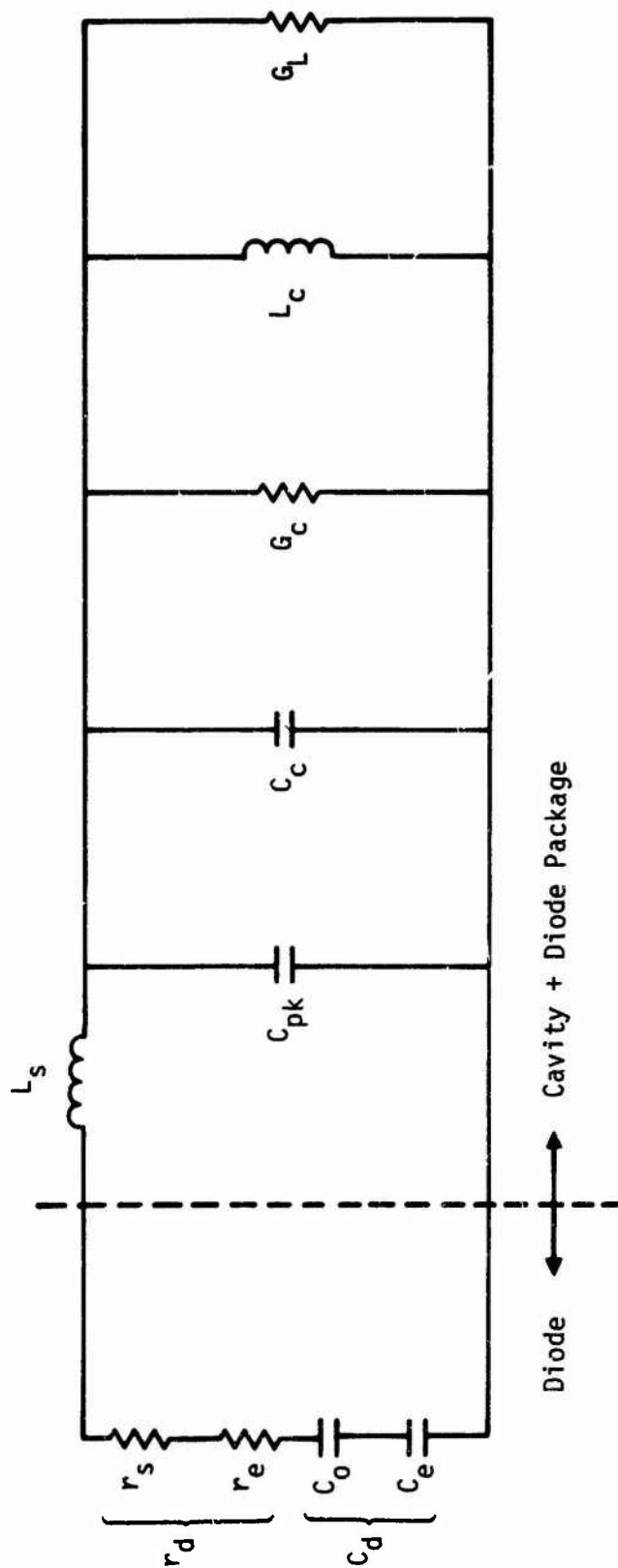


Fig. 3.1-8 Equivalent circuit of cavity and series circuit for diode

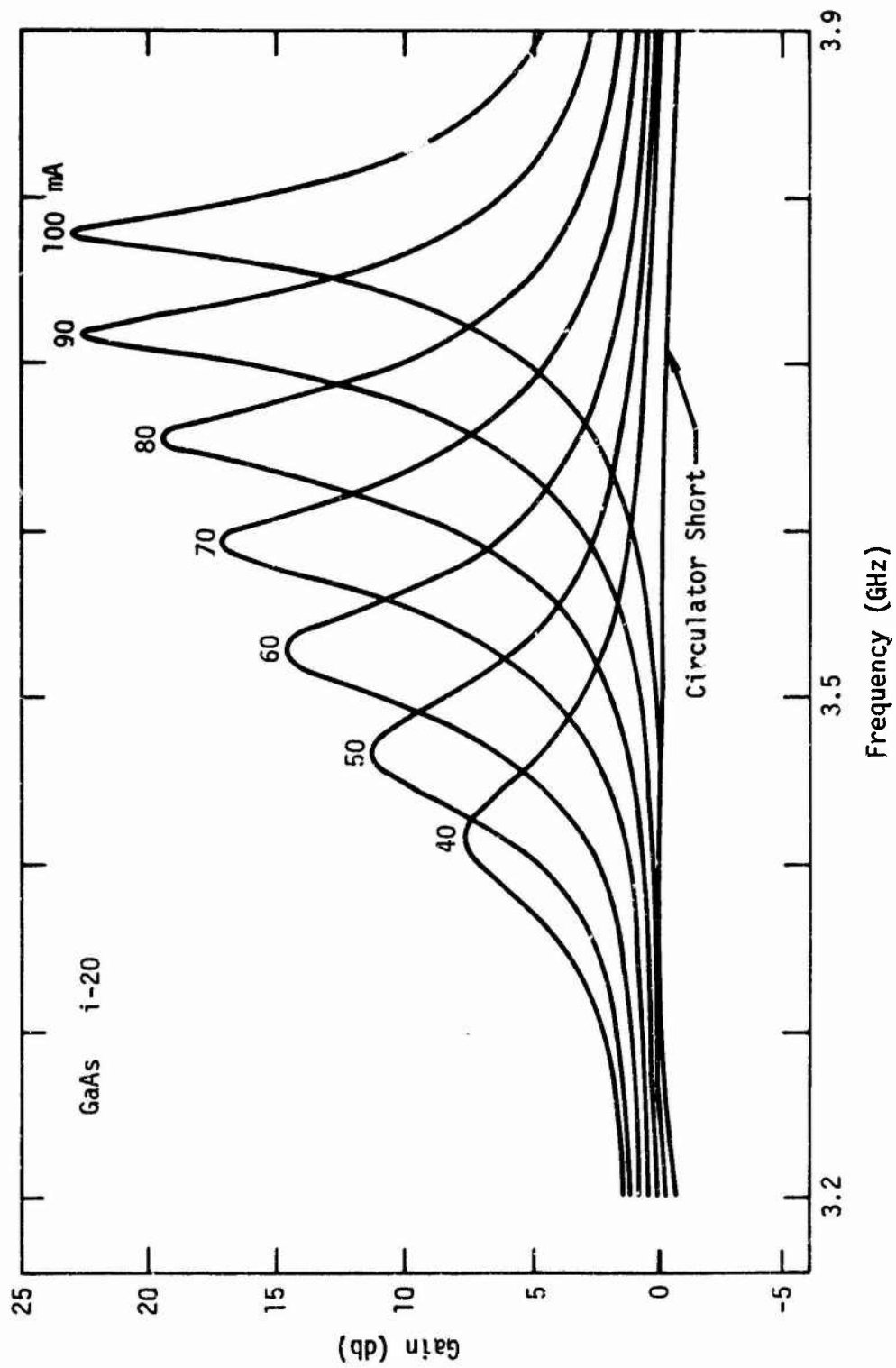


Fig. 3.1-9 Small signal gain at 3 to 4 GHz of cavity-mounted GaAs device as a function of reverse current

$$G_1 = \frac{1 - (Q_x/Q_A)^2}{1 + (Q_x/Q_A)^2}$$

where

$$\omega_0^{-2} = C_{\text{Total}} L_C$$

$$Q_x = (\omega_0 C_{\text{Total}}) \div (G_L)$$

$$Q_A = (\omega_0 C_{\text{Total}}) \div (G_{\text{Device}})$$

$$C_{\text{Total}} = C_o + C_{pk} + C_c + (-L_s G_L^2)$$

G_{Device} = Negative resistance parallel equivalent, a function of r_e the negative electronic resistance, r_s the series resistance and the electronic plus dielectric capacitances

Peak gain is then a measure of the G_{Device} . The frequency shift δ in peak gain is expressed by the theory developed as

$$\delta = \frac{\omega_{pk}}{\omega_o} - \frac{\omega_o}{\omega_{pk}} = -\frac{1}{2} \frac{Q_p}{Q_A}$$

where

$$Q_p = \omega_o C'_e / G_{\text{Device}} \quad \text{"Electronic Reactance Factor"}$$

The shift in frequency provides a means of making a measure of the ratio Q_p and of measuring whether Q_p is positive or negative.

Thus Q_p is directly derived from the measurements described above. For the ideal device this should, by theory, be less than 1.0. In practice, as is observable in many devices, this Q_p factor may be greater than 1.0. In devices where Q_p is much greater than 1.0, the shift in the frequency of peak gain with a change in device current is very marked as in Fig. 3.1-9.

This is an undesirable feature in such amplifiers leading to distortion of signals.

Q_p is related to such device physics aspects as the transit angle of the drift region and the relative width of the avalanche region. The analytical theory relating Q_p to device physical parameters has been derived and given by Lee, et al.,¹²⁻¹⁵ using the "quasi-static" approximation to describe the time-dependent behavior of avalanche. From this theory one can derive the following approximate expression for Q_p

$$Q_p \approx \frac{\sin\psi + x_1(W - x_1)^{-1}\psi}{1 - \cos\psi}$$

where

$$\psi = \omega \frac{W - x_1}{V_{sat}}$$

V_{sat} = Saturation velocity

W = Total space charge width

x_1 = Length of the avalanching region

Now Q_p may be negative as seen from the above expression if x_1 is very small as is desirable for maximum efficiency. If one obtains a measure of Q_p from the cavity reflection measurements one can make deductions with respect to the value of ψ and from that upon the value of V_{sat} and/or x_1 . The effects of Q_p are small when Q_p is less than 1.0, but upon an increase of Q_p above 1.0, phase distortion, amplitude modulation to phase modulation distortion, and power hysteresis effects can occur.

Measurements have been made on GaAs avalanche devices (supplied by Raytheon). The measurements at small signal levels have been performed at two frequencies as shown in Figs. 3.1-9 and 3.1-10. The higher frequency measurements indicated a Q_p that is quite small in magnitude and negative as the frequency pushing is positive. This device, which was not a "Read" structure, was esti-

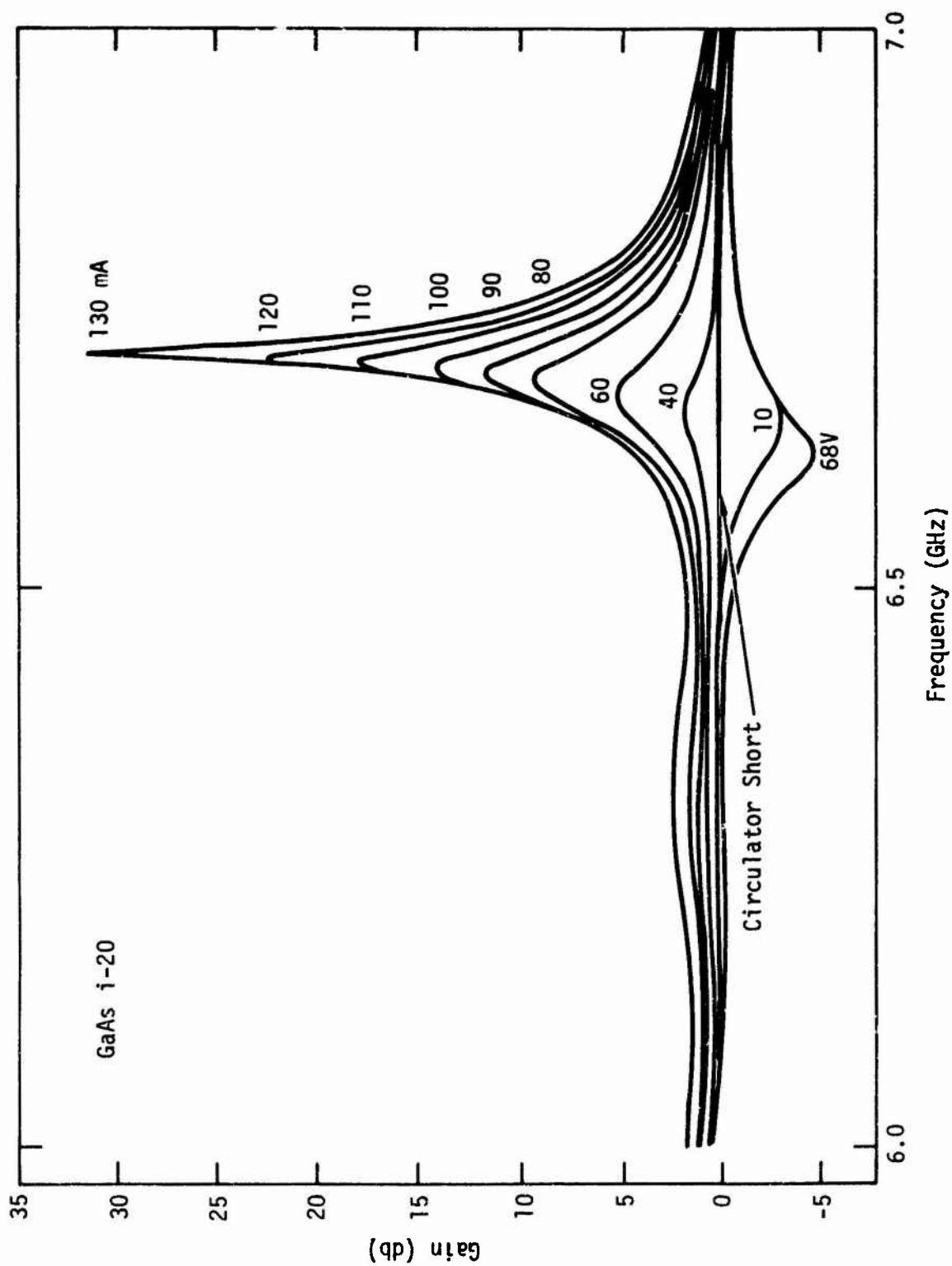


Fig. 3.1-10 Small signal gain at 6 to 7 GHz of cavity-mounted GaAs device as a function of reverse bias current

mated to have a Q_p value very small and negative at approximately 7 GHz (i.e., $\psi \simeq \pi$) and a drift region of approximately $3.5\mu\text{m}$. These figures imply a saturation velocity for the carriers of 5 to 6×10^6 cm/sec.

From measurements of the power saturation characteristics of these GaAs devices come curves such as the one in Fig. 3.1-11. Here the derived Q_p (which is the ratio of the rate of change of frequency over the rate of change of gain with increase in input power) is again less than one and negative.

So the results on GaAs devices seem to imply a lower saturation velocity than 10^7 cm/sec. In addition, from the small values of Q_p , there is evidence that the avalanching region x_1 is less than 10% of the total width W and that the ionization coefficients of holes in GaAs are much higher than electrons.

3.2 Semi-Insulating Materials

3.2.1 Crystal Growth

At this stage, the progress at USC has been in preparing the facilities for growth. Therefore, the work reported here has all been done on commercial materials.*

* Supplied by Laser Diode Laboratory and Texas Instruments, Materials Laboratory.

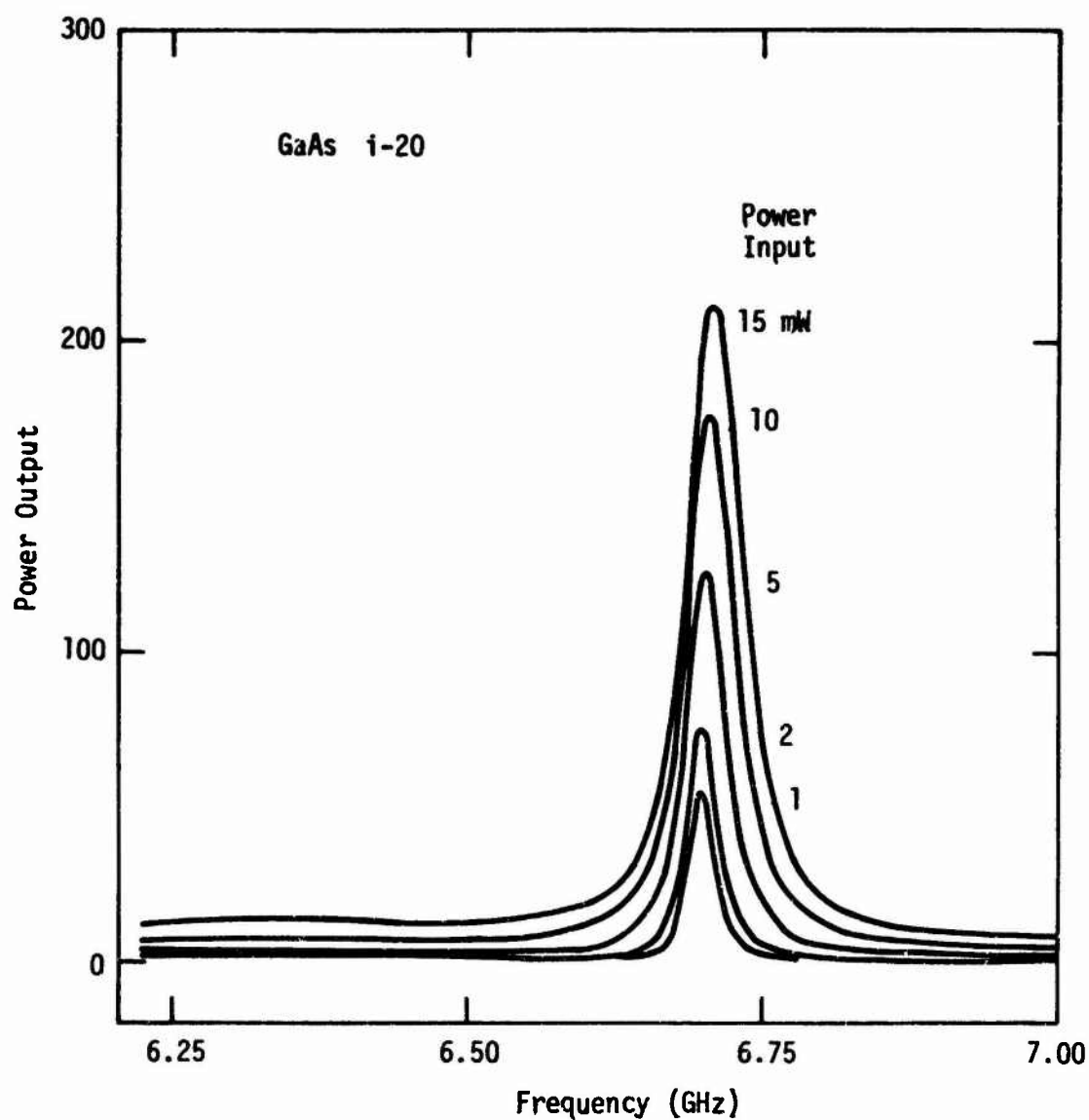


Fig. 3.1-11 Large signal gain characteristic of cavity-mounted GaAs device as a function of input power at frequencies between 6.25 and 7.00 GHz.

3.2.2 Measurement Techniques

In this initial phase, the emphasis was on setting up and evaluating some of the experimental techniques rather than in the actual evaluation of semi-insulating GaAs. Therefore, the approach presented in Section 2.2 reflects the experience accumulated in this period.

3.2.2.1 Analytical Measurements. A quick evaluation of analytical techniques for the measurement of impurity concentrations was made. This evaluation was done in a practical way by comparing results obtained by different techniques from the same wafer. Some results from a Laser Diode wafer are shown in Table 3.2-1. Mass spectroscopy measurements done by sparking two pieces of the same samples against each other indicate the presence of considerable amounts of C, O, Fe, and Cu. This means that Fe and Cu may play an important role in the compensation mechanism. C and O could also play the same role. The measurement of Cr by atomic absorption is in excellent agreement with mass spectroscopy. The emission spectroscopy results are inconsistent since they show a high concentration of Te which would certainly lower the resistivity of the material if it were actually present. It is not clear whether this is a limitation of the technique or just the effect of contamination in a careless measurement. Neutron

Table 3.2-1
Impurities in Cr-Doped GaAs (in cm^{-3})

	Cr	Fe	Cu	Te	C	O	Si	Al
Mass Spectroscopy (Electronic Materials Corporation; formerly Bell & Howell)	4.3×10^{16}	1.4×10^{16}	1.0×10^{16}	N.D.	5.8×10^{16}	8.5×10^{16}	1.3×10^{16}	1.4×10^{16}
Atomic Absorption (Science Center)	5.1×10^{16}							
Emission Spectroscopy (Materials-Charac. Lab-Texas Instruments)	1.9×10^{16}	$0.6 \text{ to } 6 \times 10^{16}$	$0.5 \text{ to } 5 \times 10^{16}$	$7-70 \times 10^{16}$			$1.1 \text{ to } 11 \times 10^{16}$	$1.2 \text{ to } 12 \times 10^{16}$

activation was not considered because Ga and As are excited along with Cr in the activation process unless the material is grown using a radioactive isotope of Cr--a cumbersome procedure even if growth facilities were available.

A practical conclusion of this survey is the choice of mass spectroscopy as the technique for routine analysis of substrates.

3.2.2.2 Quantitative Measurements of Impurity Concentrations. In view of the results reported by Jones and Hilton¹⁶ on correlations between content of Cr and optical absorption coefficient below the gap, transmissivity measurements at room temperature were done on a 0.3-mm-thick wafer of semi-insulating GaAs. The absorption coefficient is plotted against photon energy in Fig. 3.2-1. The tail of impurity absorption below the gap is clearly distinguishable, but the absorption coefficient is lower than that reported by Jones and Hilton¹⁶ for concentrations of Cr similar to those indicated for our sample by mass spectroscopy (Table 3.2-1). However, when optical or electrical measurements are compared with analytical measurements, it is important to bear in mind that only a certain fraction of the impurities is optically and electrically active.

The transmissivity method is clearly not reliable for quantitative measurements of impurity content because it is not absolute. However, it is easy to use for tests of uniformity. An area of 1 cm² of the same sample on which optical absorption was

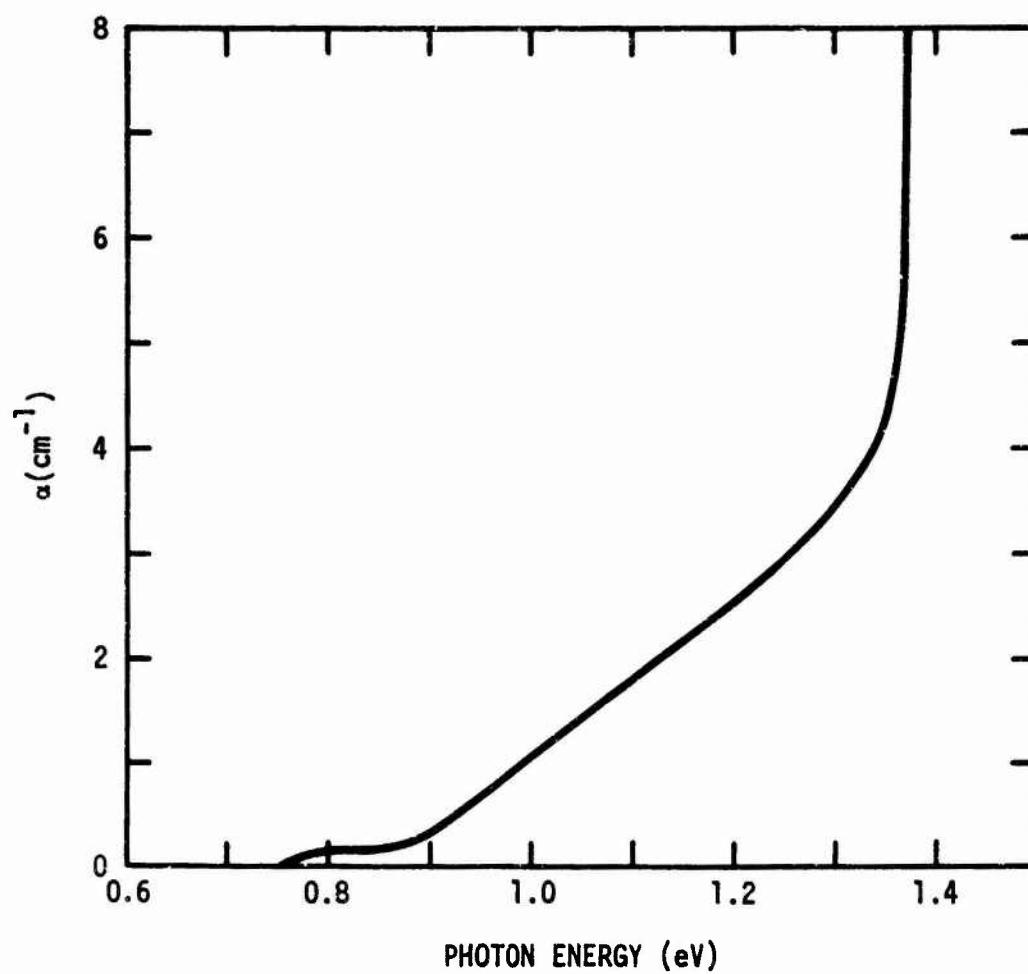


Fig. 3.2-1 Absorption coefficient of semi-insulating GaAs at room temperature.

measured was tested for variations of transmissivity with an automatic laser scanner operating at 1.06μ . Variations of the absorption coefficient below the gap are proportional to the impurity density. The tested area was found uniform. However, this test only rules out large changes of concentrations because it could only resolve changes larger than 26% due to the low absorption. The spot diameter was 0.18 mm average, determined by field depth limitations. A technique like photoconductivity, with better S/N ratio, would be more convenient than trying to improve the S/N ratio of absorption measurements. A more sensitive technique would also allow for better spatial resolution by using thin samples. The diffraction limit is typically 3μ .

The main thrust for quantitative measurements of impurity densities is on electrical measurements. All the measurements that require electrical contacts were done on the n-i-m sample configuration shown in Fig. 3.2-2. The same n-type epitaxial layer of the MESFET device is grown on a semi-insulating substrate. The epitaxial layer is attached to a plate with an ohmic contact. The semi-insulating substrate is polished or etched to reduce the thickness to typically 10μ , and an Al contact is evaporated. In the context of this project, this structure offers some advantages over ohmic contacts. It contains several of the elements of the FET device, in particular the very important n-i junction.

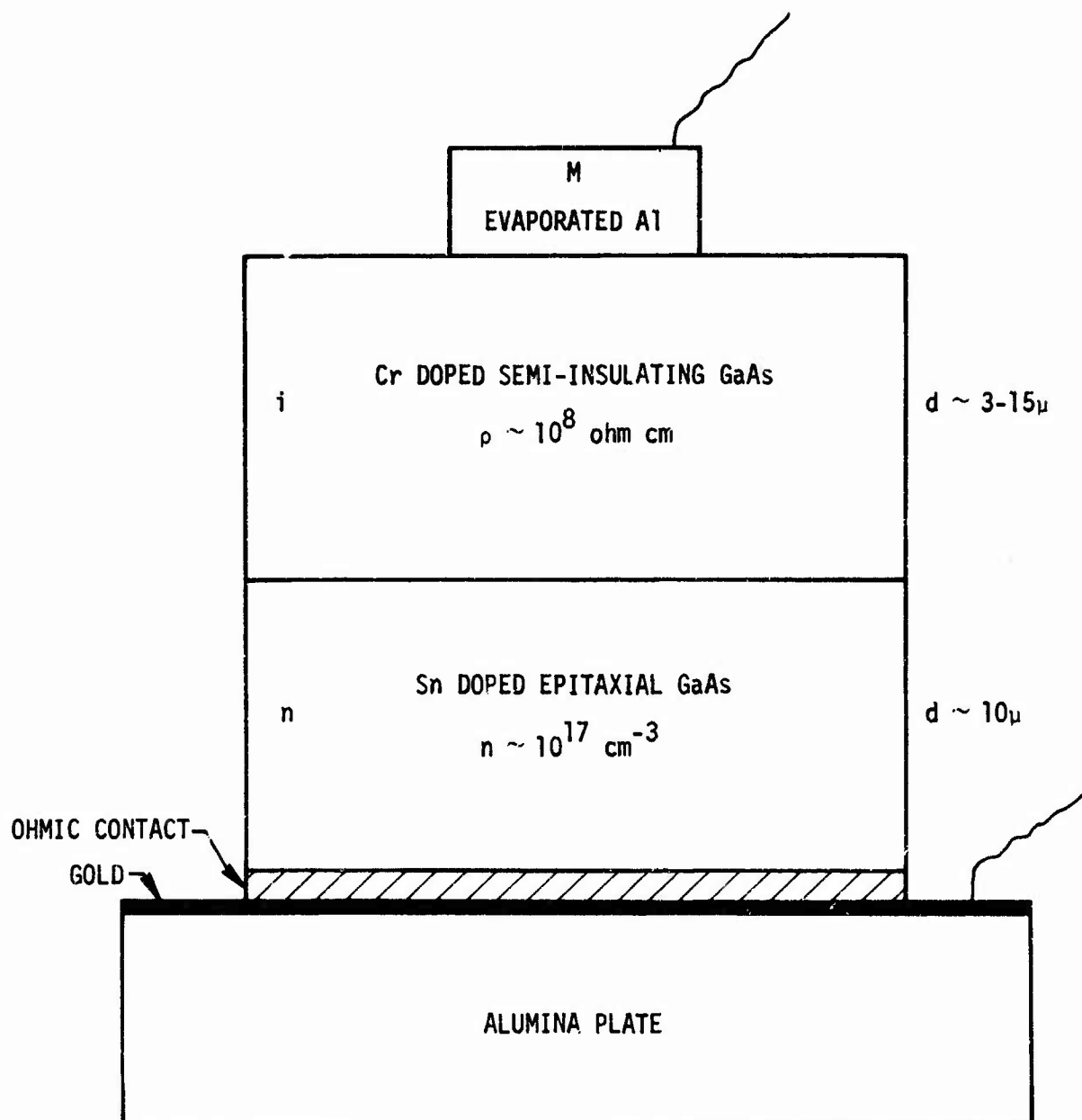


Fig. 3.2-2 Schematic of the n-i-m structure.

Furthermore, it is an asymmetric structure with preferential electron injection from the n-type layer. As a complement to help in understanding some of the effects in the n-i-m structure, similar p-i-m structures are built.

The type of I-V characteristic expected for the n-i-m structure under electron injection is shown in Fig. 3.2-3.¹⁷ At low voltage the free carriers in the insulator sustain ohmic conductivity. When electrons start being injected from the n-type layer, they start filling the Cr acceptor traps so that they become ionized. This trapped space charge keeps the current low and determines a V^2 dependence. All the traps are filled when the voltage reaches the value V_{TFL} given by

$$V_{TFL} = \frac{qN_A L^2}{2\epsilon} \quad (1)$$

where q is the electronic charge, N_A the density of neutral acceptors, L the thickness of the semi-insulating material, and ϵ the static dielectric constant. At V_{TFL} there is a sharp increase at current until it reaches a free carrier space-charge-limited regime. For practical purposes, the sharp rise of current at V_{TFL} is breakdown.

In principle, measurements of I-V characteristics of the n-i-m structure under electron injection should yield the density of

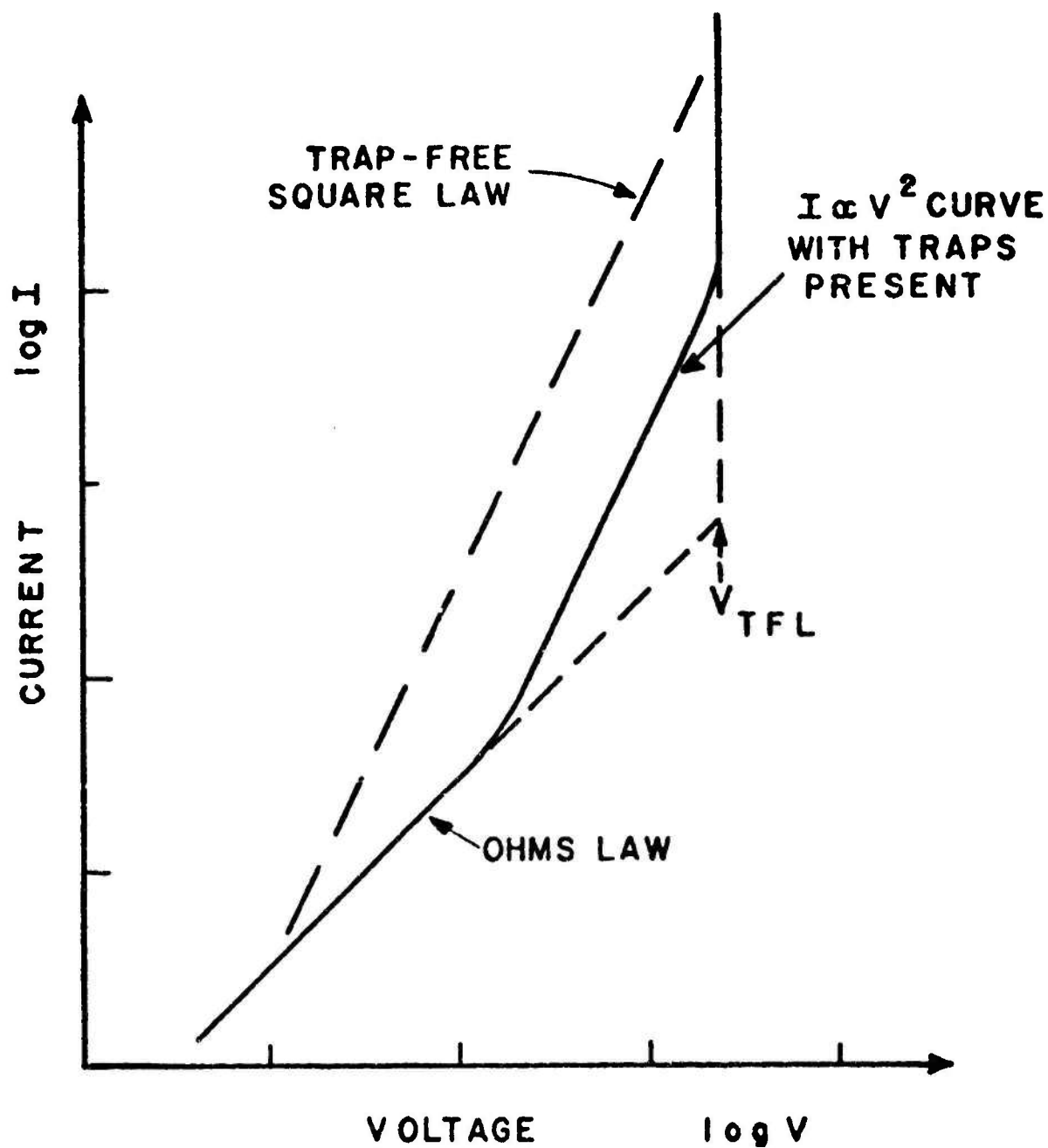


Fig. 3.2-3 Ideal I-V characteristics for an insulator under single injection.

neutral acceptors from the breakdown voltage (Eq. (1)). Similarly, it should be possible to obtain the density of neutral donors from the breakdown voltages of the p-i-m structures under hole injection.

Figure 3.2-4 shows typical I-V characteristics of the n-i-m and p-i-m structures under electron and hole injection, respectively. The shape of the curves agrees in general with the ideal characteristic (Fig. 3.2-3), but the breakdown voltages are extremely low. For example, from the breakdown voltage of the n-i-m structure in Fig. 3.2-4, Eq. (1) would predict a density of neutral acceptors $N_A \sim 2 \times 10^{13} \text{ cm}^{-3}$. Although such density is unknown, it is expected to be comparable to the Cr density; therefore, the figure is probably a couple of orders of magnitude too low indicating that the model is not applicable. This pattern of low breakdown voltages repeats consistently for different thicknesses of the semi-insulating layer.

It is unlikely that avalanche effects play some role because the electric fields are low. It is possible that the trapping cross section is low in this material, or that the trapping cross section decreases sharply with the electric field. This would explain the low trap density estimated from Eq. (1). Another possibility is that double injection takes place, with injection of carriers from the metal. Such double injection would lead to a behavior similar to that of the p-i-n structure with a negative characteristic at breakdown.¹⁷ Indeed, hysteresis effects are

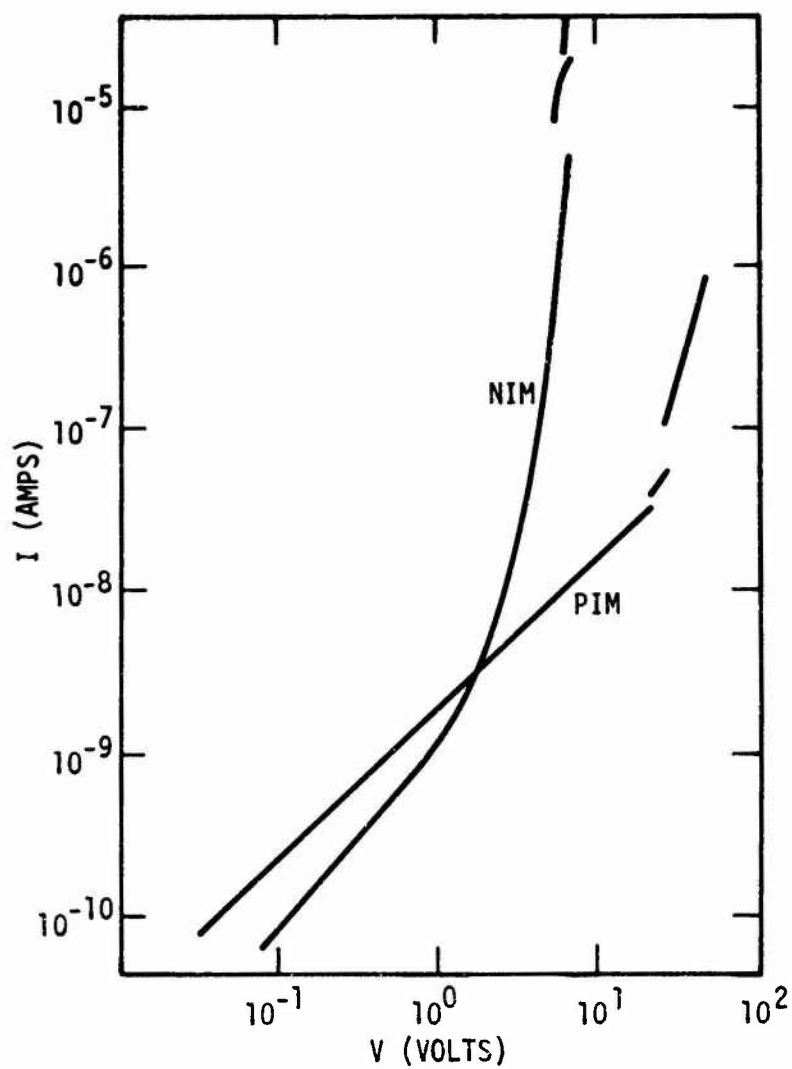


Fig. 3.2-4 I-V characteristics at an n-i-m structure under electron injection, and a p-i-m structure under hole injection. The thickness of the semi-insulating layer is 20μ .

seen at breakdown (Fig. 3.2-4) indicating a negative characteristic, but more experiments need to be done. It is clear at this point that measurement of breakdown voltages cannot be used as a tool for direct measurement of trap densities, as it was planned when the experiment was designed. However, these measurements expose a problem of low breakdown voltages that is relevant for the devices in order to avoid breakdown effects between electrodes. As a means to obtain trap densities, other techniques must be used. As discussed in Section 2.2.2, transient capacity measurements is the most promising technique.

3.2.2.3 Complementary Measurements. Measurements of thermally-stimulated currents are in progress. An example of the type of results obtained is shown in Fig. 3.2.5. The principle is to fill the traps in the semi-insulating material at a low temperature (77°K), then remove the excitation and slowly warm up the sample while measuring the current. The temperature, as it increases, begins to empty the trap levels slowly. If the levels are sufficiently discrete and the rate of warming sufficiently slow, distinct peaks of current are discerned leading to identification of the trap levels. When the trap levels are not sufficiently separated in energy, there may be difficulty in discerning the presence of two levels rather than one due to the simultaneous emptying of the traps. It is good practice in this measurement

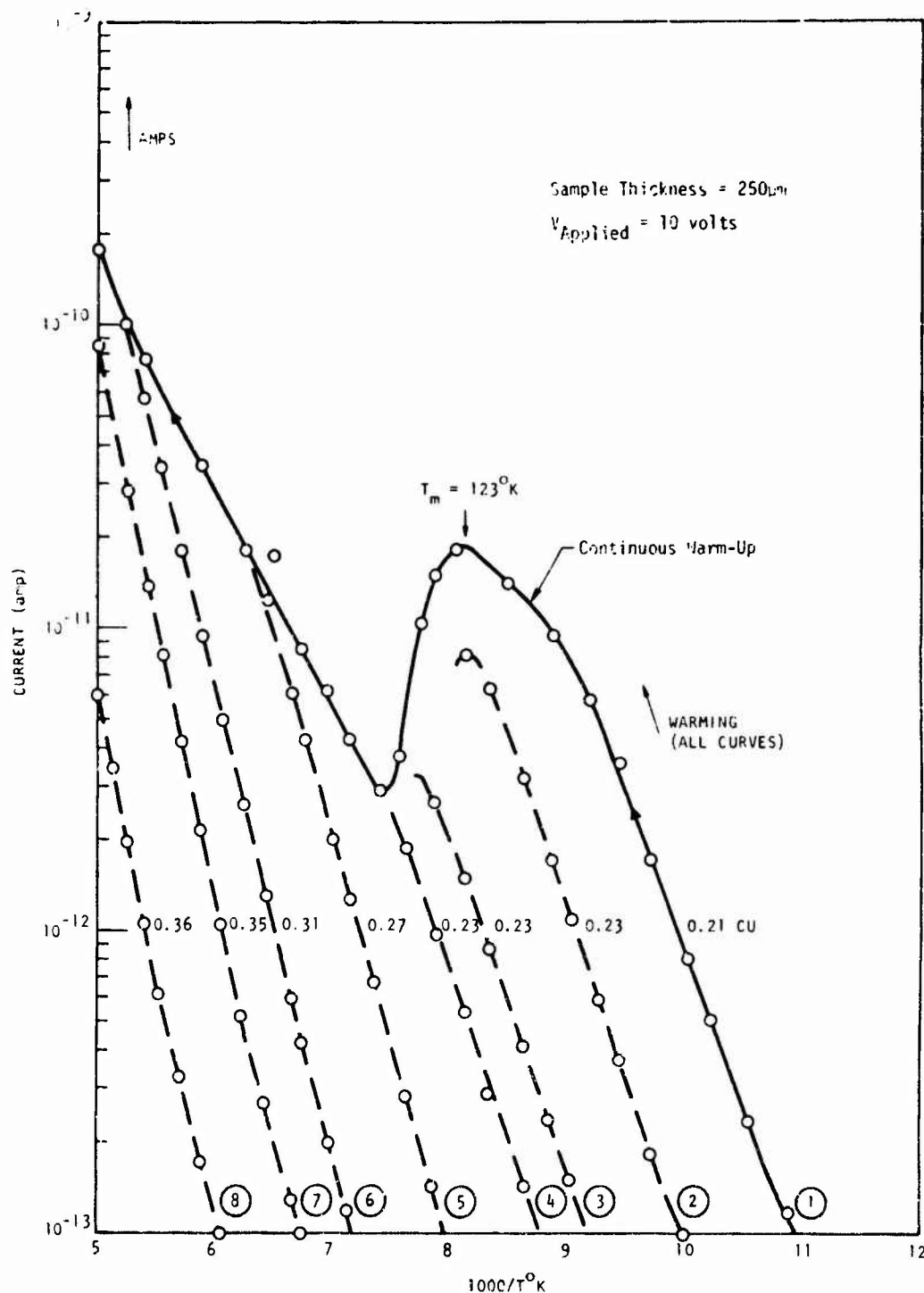


Fig. 3.2-5 Thermally-stimulated current measurements on semi-insulating GaAs with AuGe contacts. The dotted lines represent repeated cycles of warming up to progressively higher temperatures. The full line represents an uninterrupted warm-up measurement.

to do what is referred to as "successive warming" measurements.¹⁸ This means slowly warming the sample up to a temperature at which the shallower of the two traps in question is nearly exhausted of its trapped carriers. Then the sample is recooled to a very low temperature and slowly warmed up again. On the second warming cycle the diminished presence of trapped carriers in the shallower trap can no longer effectively mask the characteristic release rate of the second deeper trap. An example of such measurements is shown in Fig. 3.2-5.

The spectrum presented in Fig. 3.2-5 was obtained from a chromium-doped sample with metal contacts at a very low voltage. Current was, therefore, in the bulk, ohmic current and the trap levels were filled by a period of intense illumination with bandgap radiation. The trap nature is, therefore, not fully defined but a qualitative picture is presented of the traps present in the bandgap. It is seen that there are levels at 0.21-0.23 eV and 0.36 eV. Information about trap levels deeper than 0.5 eV is not easily obtained this way because it requires raising the temperature much above room temperature.

The same thermally-stimulated current measurements can be done on the n-i-m or p-i-m structures discussed above. A spectrum of the n-i-m structure is shown in Fig. 3-2-6. Here the "successive warming" technique was not applied. Instead, the effect of filling

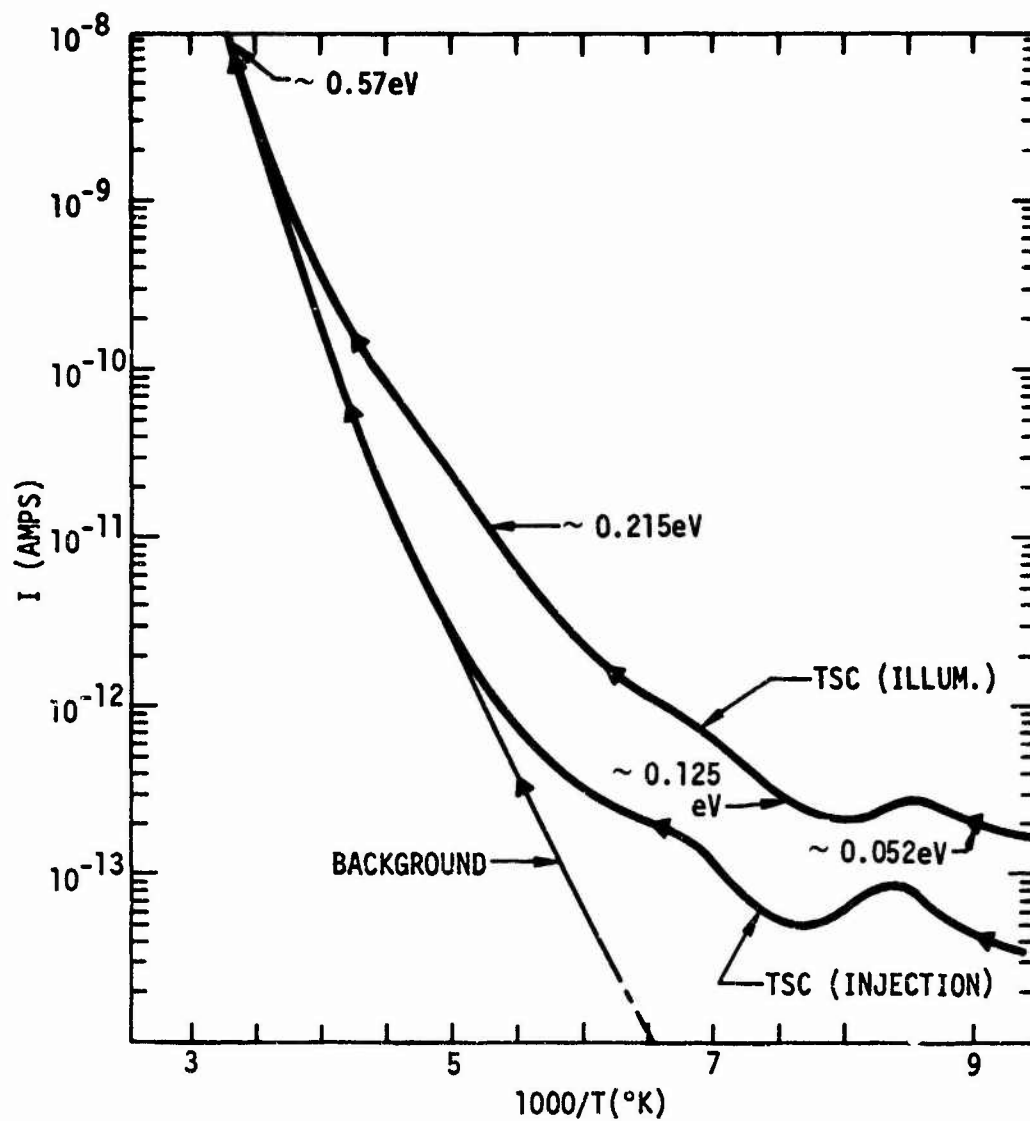


Fig. 3.2-6 Thermally-stimulated current measurement on semi-insulating GaAs in an n-i-m structure after illumination and after electron injection.

the traps with light illumination or current injection is compared. The lower intensity in the case of current injection is probably due to the limited volume of the sample in which the traps are filled. In the case of light illumination the whole sample is exposed. In the future, once the I-V characteristics are better understood and it becomes possible to determine and control when single injection takes place, thermally-stimulated current measurements could be done on samples with either the electron or the hole traps filled only. Therefore, it would be possible to distinguish between the two types of traps.

Photoconductivity measurements were done on semi-insulating GaAs in the n-i-m and p-i-m configuration. Photocarriers are created by a monochromatic light beam. A DC bias is applied to the sample and the photocurrent is measured as a function of the incident photon energy. A spectrum from the n-i-m structure at liquid He temperature is shown in Fig. 3.2-7. The bandgap appears only as a small kink to the right of the sharp peak at 1.5 eV. This peak corresponds to shallow impurities. The left portion is all due to extrinsic photoconductivity--the threshold at 0.8 eV being at the depth of the Cr levels from the conduction band.¹⁹ Even without further analysis of the photoconductivity peaks, the power of this technique for the detection of impurities is evident.

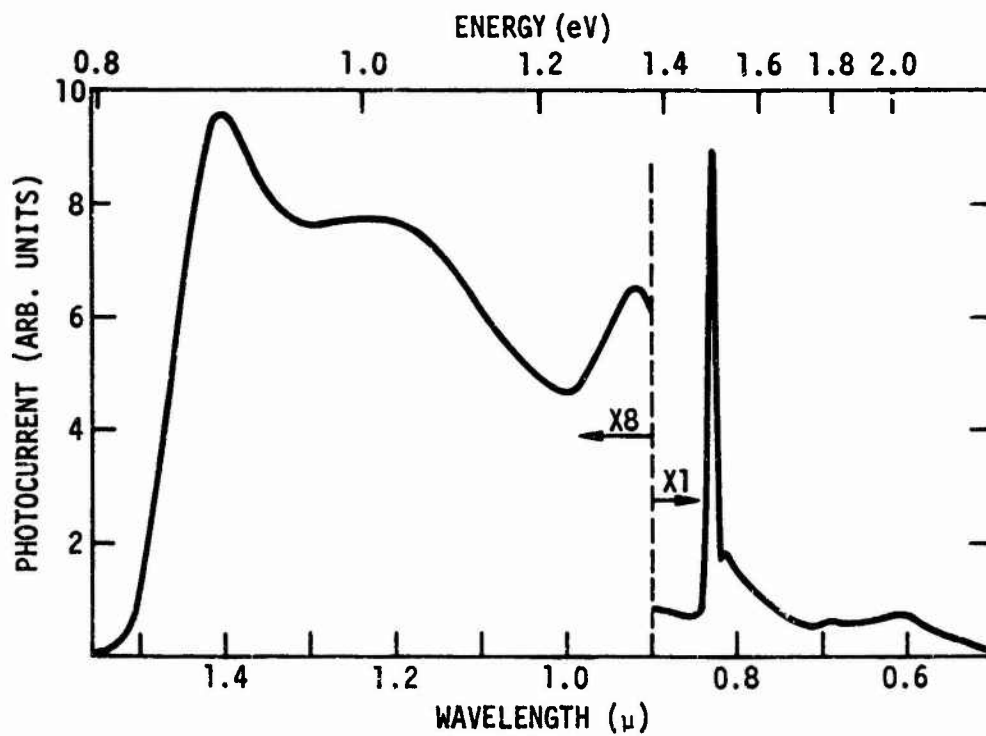


Fig. 3.2-7 Photoconductivity spectrum of semi-insulating GaAs in an n-i-m structure at 4.2°K. (Uncorrected for spectral variation of intensity of the lamp.)

In addition, photovoltaic effects are detected in the n-i-m and p-i-m structure. Such effects yield information on the junctions between semi-insulating GaAs and n-type GaAs, p-type GaAs, and metals. In particular, the n-i junction is a critical part of the MESFET and TEL device as discussed in Section 1.1. The spectrum of the photovoltaic effect in the n-i-m structure with light penetrating from the metal side (Fig. 3.2-2), is similar to that of the photoconductivity, shown in Fig. 3.2-7. On the other hand, in the p-i-m structure the spectrum of the photovoltaic effect shows a change of sign at the energy gap (Fig. 3.2-8). The change of sign is an indication of band bending in opposite directions at the p-i and i-m junction.

3.2.2.4 Summary. Different analytical techniques to measure total contents of impurities were compared. Mass spectroscopy offers the best balance of convenience and reliability. However, these measurements are only an indication of the presence of impurities regardless of whether they are electrically active or not. For quantitative measurements of trap densities, the breakdown voltages of single-injection n-i-m and p-i-m structures under forward bias were measured. Since breakdown should occur when all traps are filled, the trap density would be obtained from the straightforward relationship between trap density and breakdown voltage. However, breakdown takes place at too low

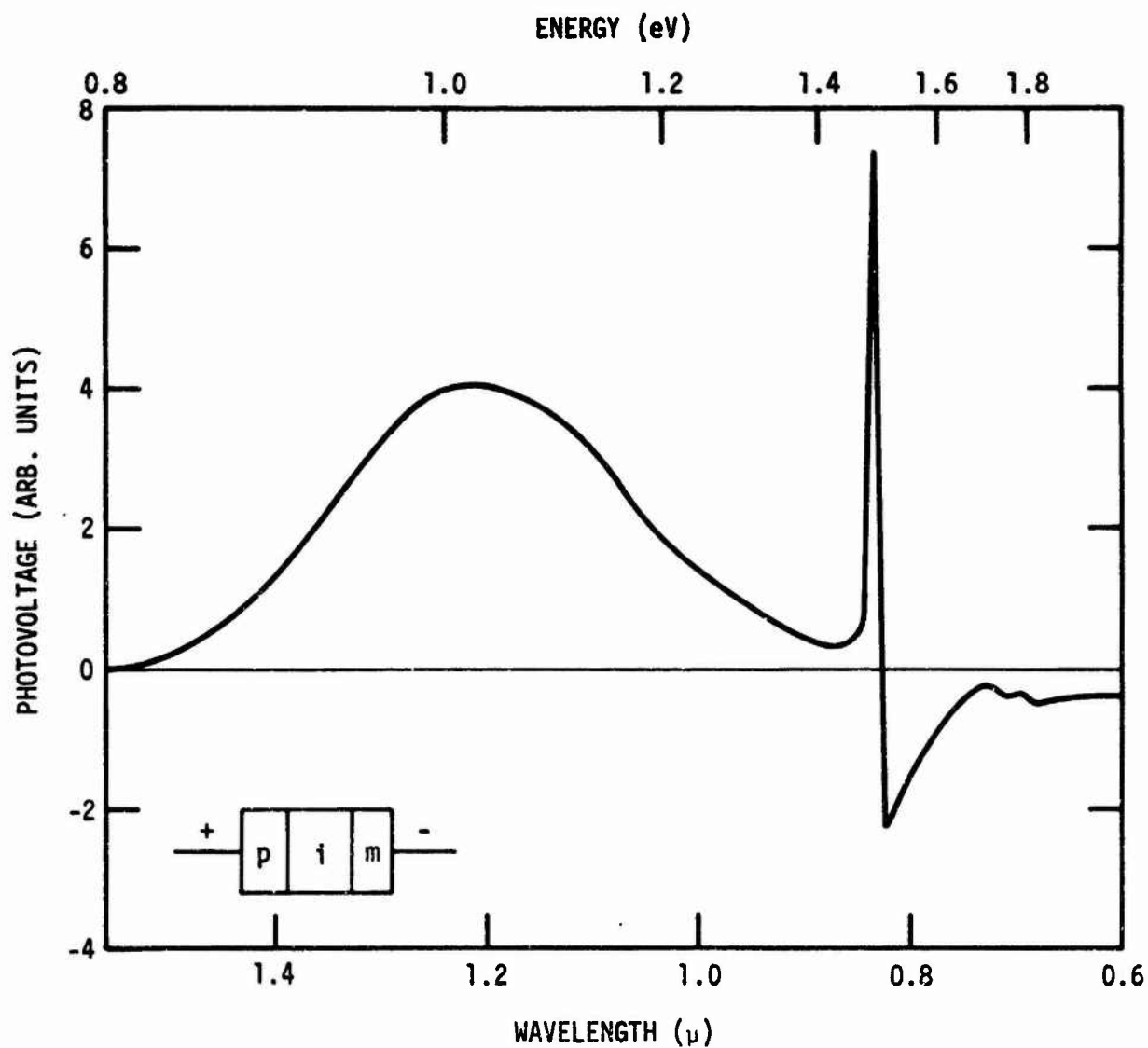


Fig. 3.2-8 Photovoltaic effect in a p-i-m structure at 4.2°K. (Uncorrected for spectral variation of the lamp intensity.) The light beam is incident on the metal side.

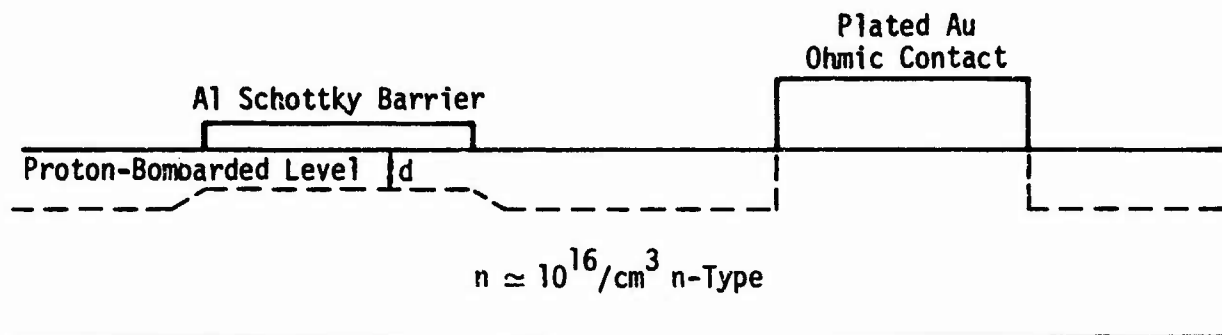
voltages, which yield unrealistically low trap densities. This method was abandoned as a tool for measurement of trap densities, but the problem is under investigation because low breakdown effects in the substrate affect the design of devices. Transient capacity is being considered as an alternative method for measurement of trap densities. Thermally-stimulated currents and photoconductivity were measured in the n-i-m and p-i-m structures. Photovoltaic effects were observed both at the n-i (or p-i) and i-m junctions. These effects appear as possible tools for spectroscopy of the junctions.

3.2.3 Proton Bombardment

An experiment was done to see the effects of a constant-dosage and increasing energies. The samples used were as shown in Fig. 3.2-9a, and they are similar to the n-i-m structures of the chromium-doped investigation. Under forward bias (when negative voltage is applied to the n-type epitaxial layer) electrons are injected into the bombarded region. In reverse bias the metal-insulator junction is blocking and C-V become the most revealing measurements available. So the measurements conducted on samples were principally breakdown in the "forward" direction and C-V in the reverse direction.

In these experiments the depth of the insulator layer is seen to be a linear function of energy as depicted in Fig. 3.2-9b. This depth is derived from the zero voltage capacitance. The breakdown voltage in

(a)



(b)

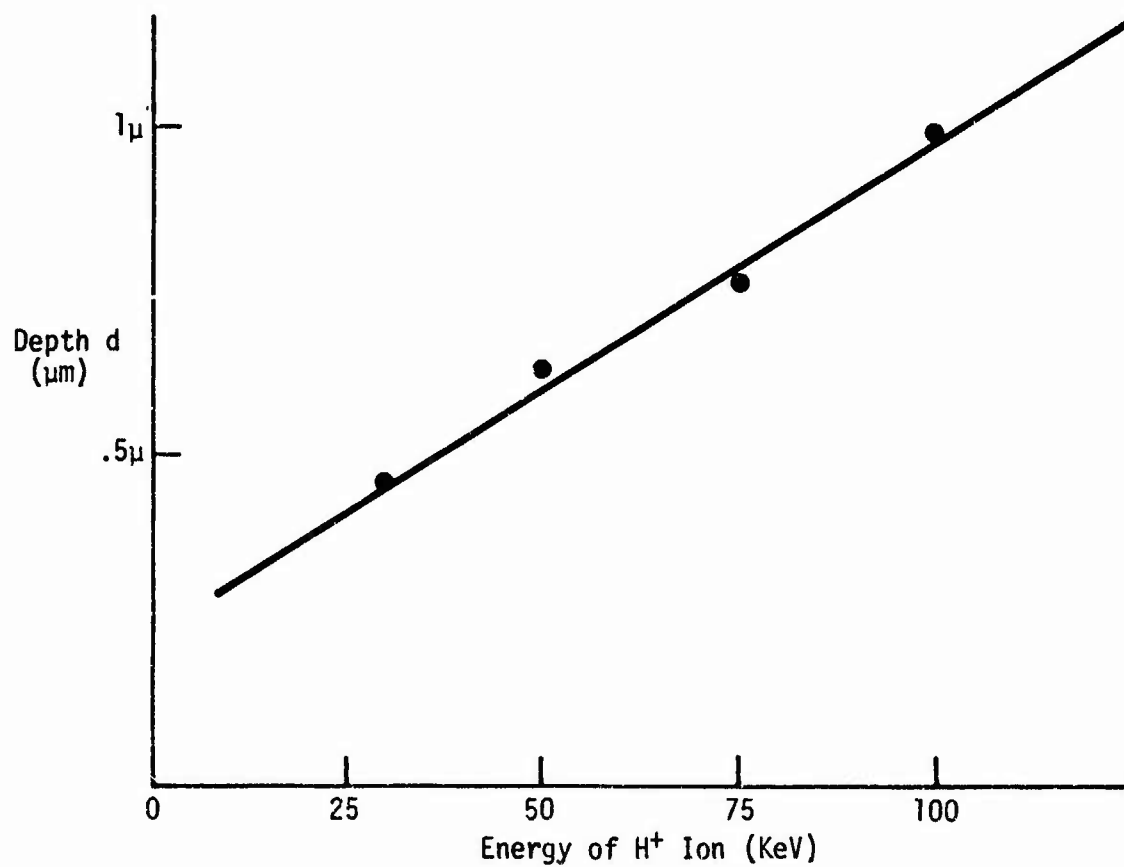


Fig. 3.2-9 (a) Schematic of a proton-bombarded sample. (b) Depth of the semi-insulated layer vs proton beam energy.

the forward direction for this n-i-m structure seems to be proportional to the square of the depth of the insulator layer as shown in Fig. 3.2-10. This suggests a "transition to SCLC-type of breakdown." It may be remarked that the material withstands higher voltages than much thicker portions of melt-grown, chromium-doped, semi-insulating materials do in similar tests. Our measurements were done only up to 100 KeV. Further work must be done in this area.

Thermally-stimulated current measurements of this type of structure are shown in Fig. 3.2-11. The current due to injection excitation is much greater than that due to optical absorption by above-bandgap light. This is an opposite effect from that obtained with the chromium-doped material, possibly indicating a greater density of active trap sites for electrons. The initial TSC measurements suggest a deep level at 0.31 eV. Further measurements at higher temperatures must be awaited before more definitive statements can be made.

A second experiment was to look at the effects of increasing the dosage rate at a constant energy level. Quite marked effects appear in the C-V measurements. In fact, the flat band voltage increases in proportion to the dosage. The increase in flat band voltage is depicted in Fig. 3.2-12. The implied level of net positive fixed charge in the insulator region is only about 1% of the proton dose. Further effects are noticeable from the increased dosage experiment. The generation-

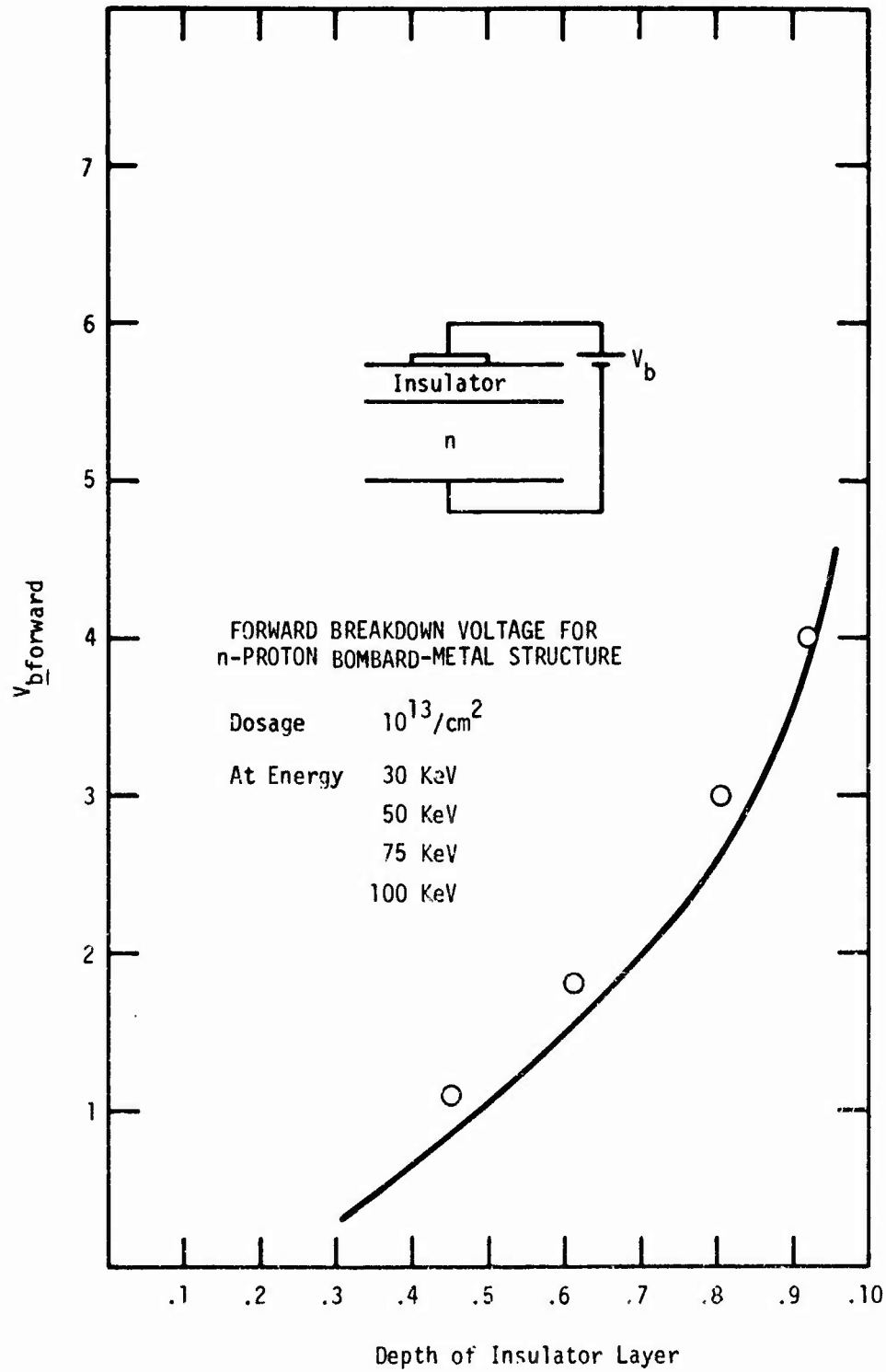


Fig. 3.2-10 Breakdown voltage vs depth of semi-insulating layers made by proton bombardment.

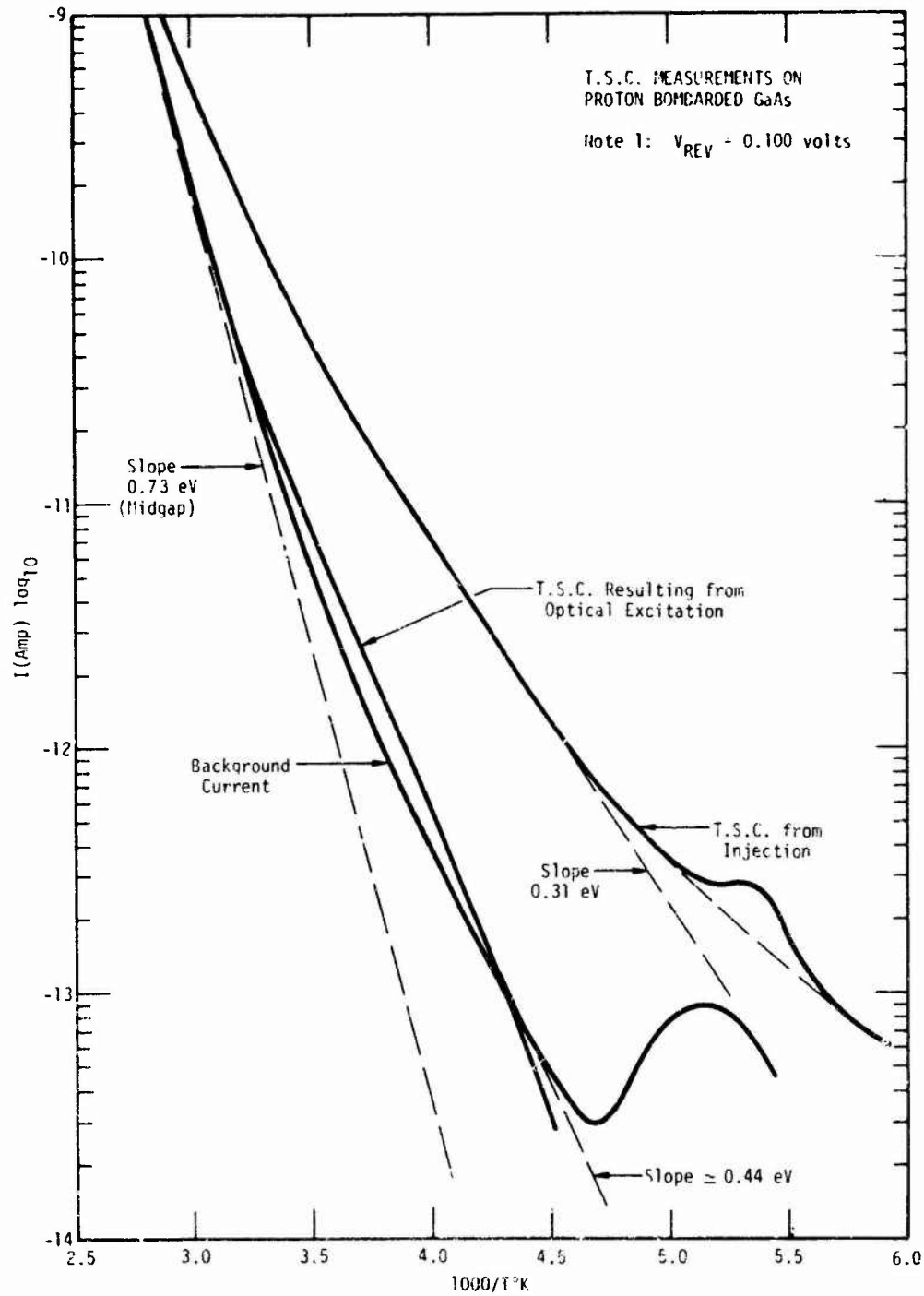


Fig. 3.2-11 Thermally-stimulated current spectrum
of proton-bombarded GaAs

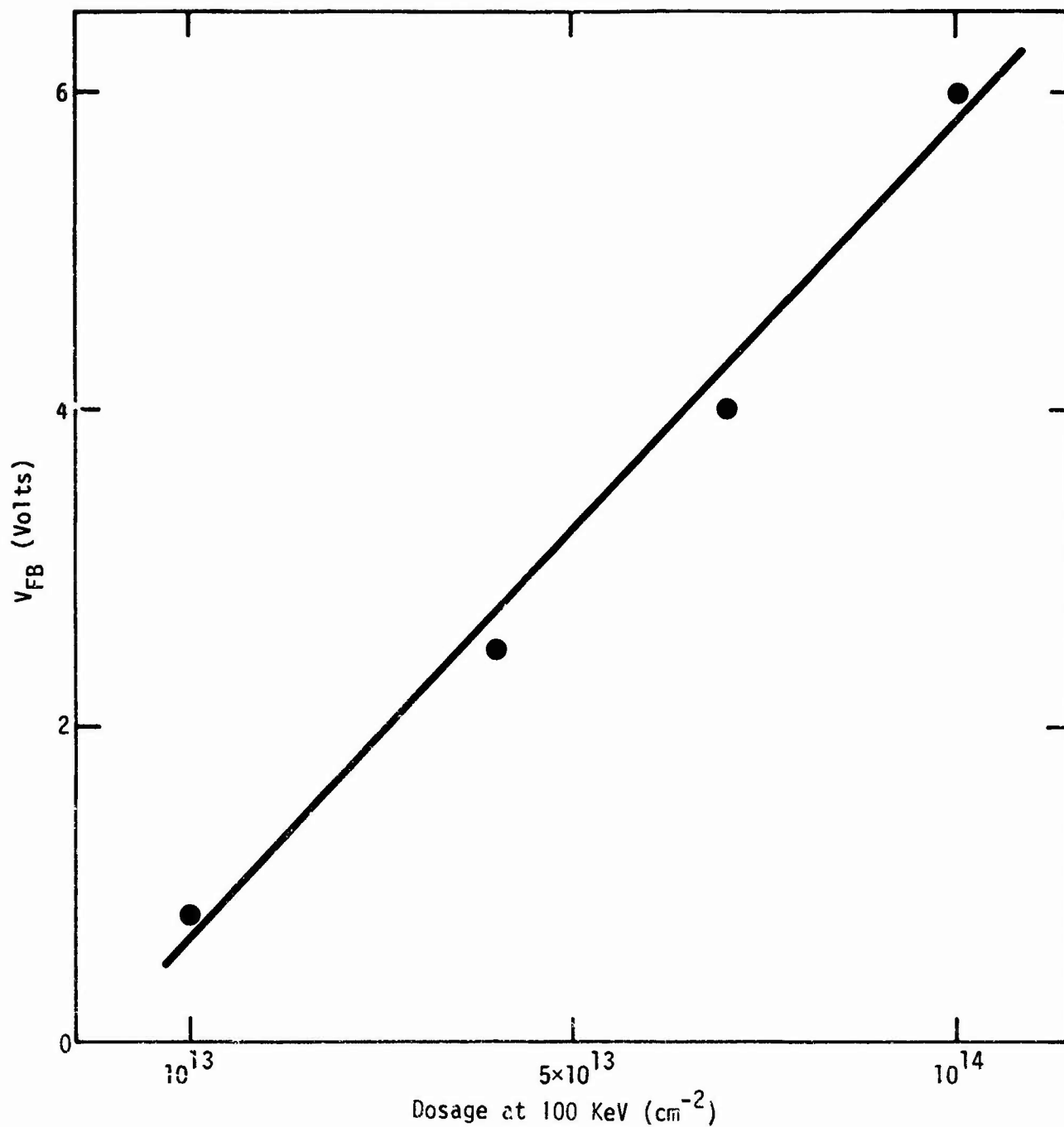


Fig. 3.2-12 Flat band voltage of capacitance-voltage measurements on a reverse-biased n-i-m structure. The semi-insulating layer was produced by proton bombardment at a constant energy with increasing dosages.

recombination leakage current increases considerably. There is an optimum dosage level that may be fixed by initial conductivity level and possible annealing conditions.

3.3 n-Type Doping of GaAs by Ion Implantation

The implantation energy in our past work with Te has been limited to 220 KeV because the field in the analyzing magnet was not sufficient to deflect higher energy Te ions into the beam leg connecting to the sample chamber. Recently, a new beam leg has been completed which will permit the implantation of any heavy ion at energies up to the limit of the Van de Graaf accelerator (400 to 500 KeV). This should facilitate the attainment of deeper doping profiles and also make it easier to carry out implantation experiments at very high temperatures through dielectric layers on the surface of the GaAs. A neutral trap has been incorporated in this beam line. This should result in the implanted dose being more uniformly distributed over the whole sample than has been possible in the past since the beam line that has been in use did not have such a neutral trap, and it was known that there was a significant increase in the Te concentration near the center of the implanted area. This greater uniformity will be of use not only in Te implantations but in the implantation of other dopant ions in GaAs also. This capability will make it possible to more exactly evaluate the electrical activity achieved by ion implantation and will facilitate the application of implantation to the production of microwave devices.

3.3.1 Annealing Cap

Previous work on doping GaAs by tellurium implantation, under our IR&D program, has shown that the nature of the cap used to protect the surface of the implanted GaAs during annealing has a strong effect on the implantation results. The use of silicon nitride as a cap material has resulted in much higher electrical activity of the implanted tellurium than the more commonly used silicon dioxide.⁷ This is thought to be due to the fact that gallium diffuses much more rapidly in the oxide than in the nitride at the annealing temperatures employed, so that there is a possibility of diffusion of gallium into the oxide and the formation of gallium vacancies in the GaAs. Support for this hypothesis has been obtained from photoluminescence measurements which indicate a much higher concentration of gallium-vacancy-associated defects in implanted samples annealed with silicon dioxide as compared with samples annealed with a silicon nitride cap.

Some difficulty has been encountered with the use of silicon nitride as a cap during annealing. In some cases the nitride layer has been observed to bubble and lift from the GaAs surface during annealing.⁸ Aluminum nitride has a thermal expansion coefficient much closer to that of GaAs than does silicon nitride. For these reasons experiments on the use of aluminum nitride as a cap material were undertaken.

The results of electrical measurements on GaAs samples which were implanted with tellurium and annealed with an AlN cap are presented in

Section 3.3.2. The composition of these AlN films was evaluated using helium ion backscattering. The backscattering measurements were carried out on samples of the nitride layer deposited on carbon blanks at the same time as the deposition on an implanted sample. An example of the results is shown in Fig. 3.3-1. The scattering edges for aluminum, oxygen, and nitrogen are shown in the figure. From the relative height of the oxygen and nitrogen scattering yields, it may be concluded that there were approximately equal amounts of oxygen and nitrogen in this sputtered film. This was true of all other films examined as well.

Backscattering measurements made on a GaAs sample, covered with AlN, before and after annealing indicate that there was no diffusion of gallium or arsenic into the AlN during the annealing. The sensitivity of these measurements is not great, and other techniques, such as that suggested in 2.3.1, will be required to fully evaluate the effectiveness of AlN as an annealing cap.

The doping results obtained so far on Te-implanted GaAs samples annealed with an AlN cap are very encouraging (see 3.3.2). The electrical activities seem to be greater than those obtained with a Si_3N_4 cap and exhibit less scatter than with Si_3N_4 . It is of special interest that these results have been obtained with AlN films having an appreciable oxygen concentration. This suggests that the presence of oxygen in the AlN film is not deleterious. In order to fully evaluate the effect of

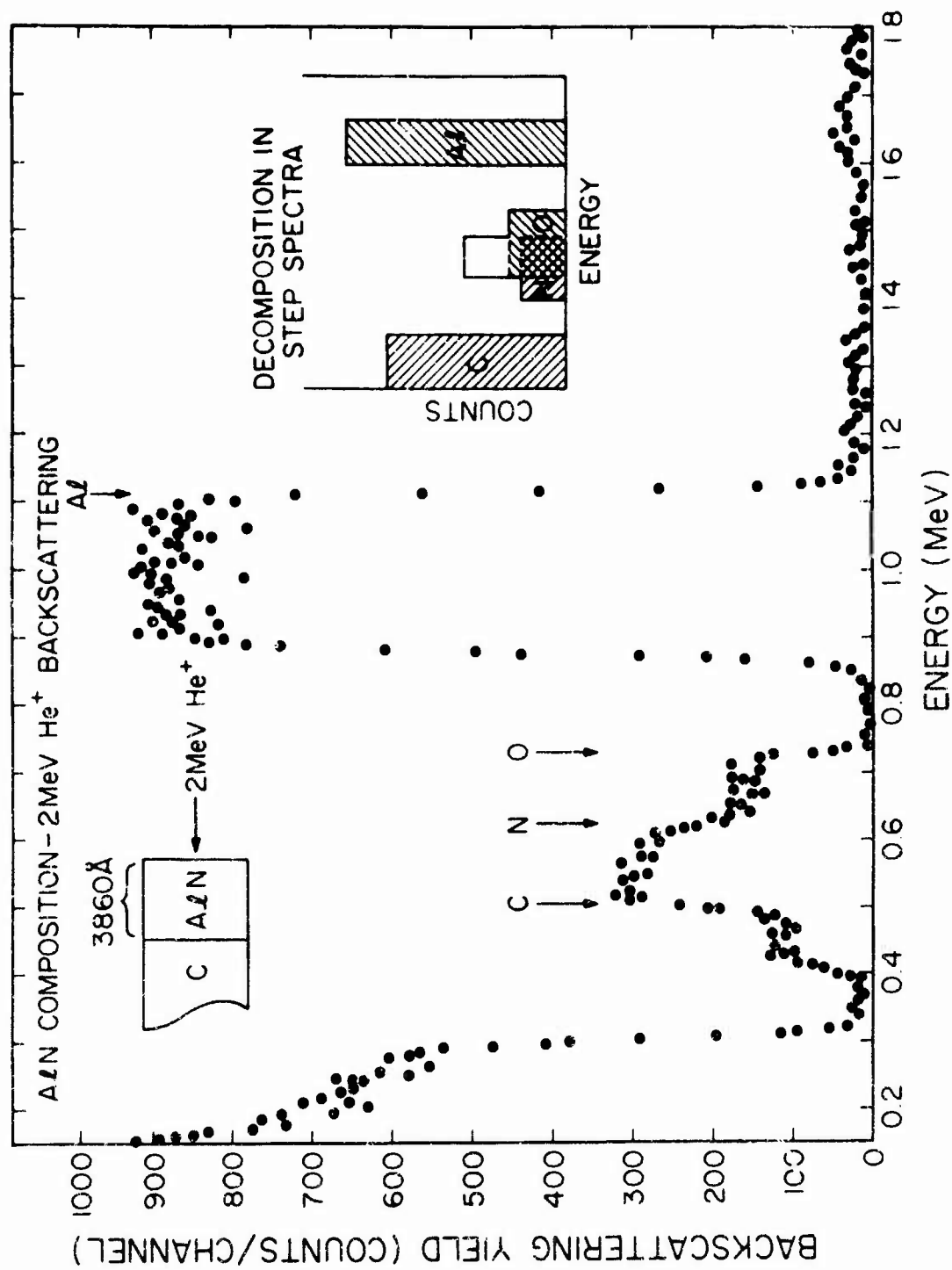


Fig. 3.3-1 Energy spectrum of 2 MeV He ions backscattered from a sputtered AlN film on carbon

oxygen contamination of the AlN, it will be necessary to produce AlN films with very low oxygen concentrations. We have recently obtained a new sputtering system which will be dedicated solely to the production of films for annealing caps for implanted GaAs. It is felt that by the use of this dedicated system some of the contamination problems resulting from our previous use of a general-purpose sputtering system will be avoided. This system is now in use. The composition of some of the initial films has been evaluated by He-ion backscattering measurements. The problem of oxygen contamination has not been completely eliminated, but the oxygen concentration in the first films is appreciably below that in the films which were produced in the general-purpose sputtering system that had been used up to now.

3.3.2 Characteristics of Implanted Layers and Junctions

Capacitance voltage data for two diodes obtained by implanting Te into p-type substrate materials are shown in Fig. 3.3-2. Si_3N_4 was used as the annealing cap for one of the samples and AlN for the other sample. In both cases the reciprocal of the cube of the capacitance varies approximately linearly with voltage. This indicates that the donor concentration is a linear function of distance in the region of the junction. Chemical etching and sequential Hall coefficient and resistivity measurements have been used to determine the electron concentration profile to a depth of about $1500\text{\AA}$ for two samples. The results of these measurements are shown in Figs. 3.3-3 and 3.3-4. For the sample shown in Fig. 3.3-3, the junction

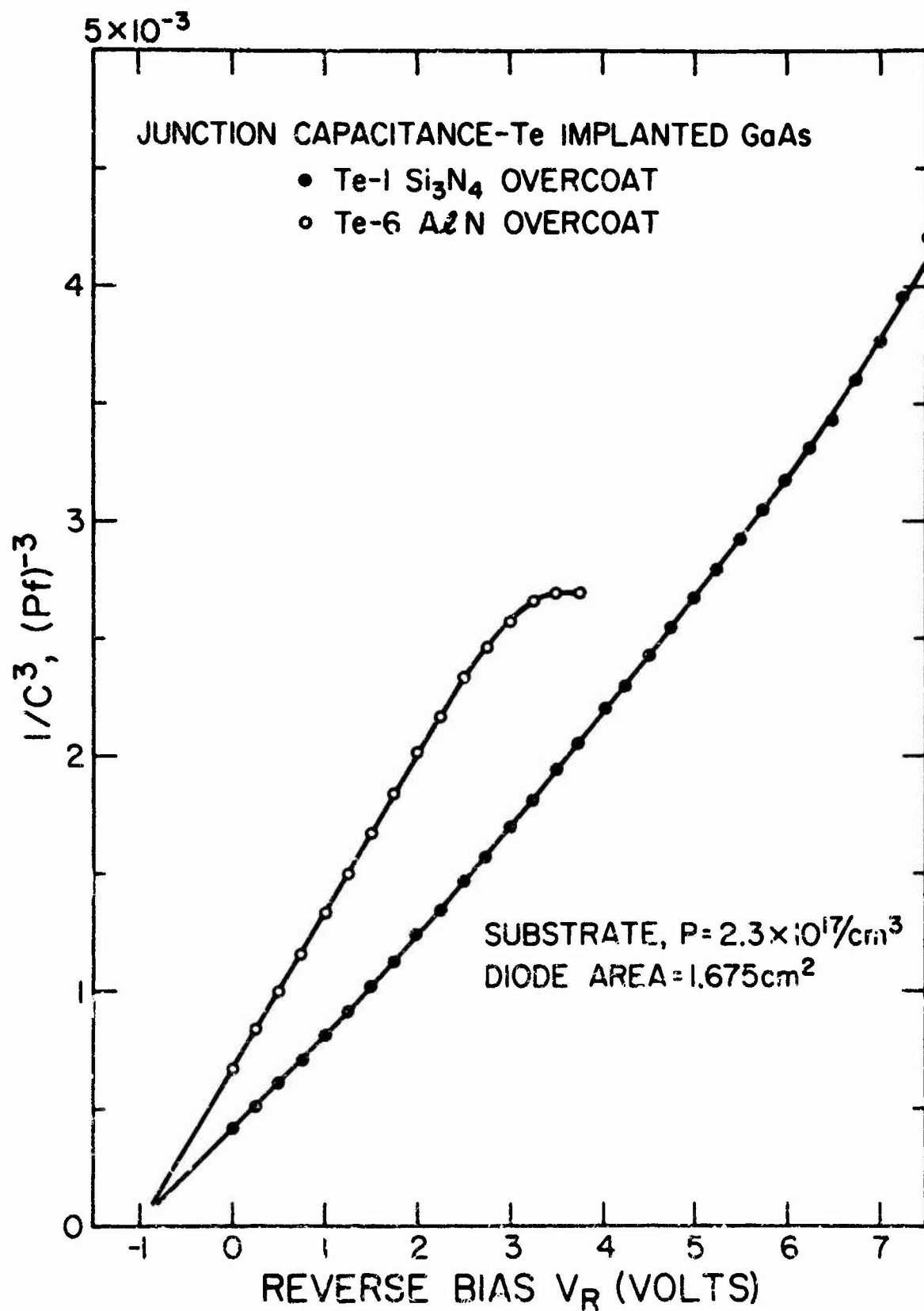


Fig. 3.3-2 Capacitance-voltage characteristics of two ion-implanted diodes

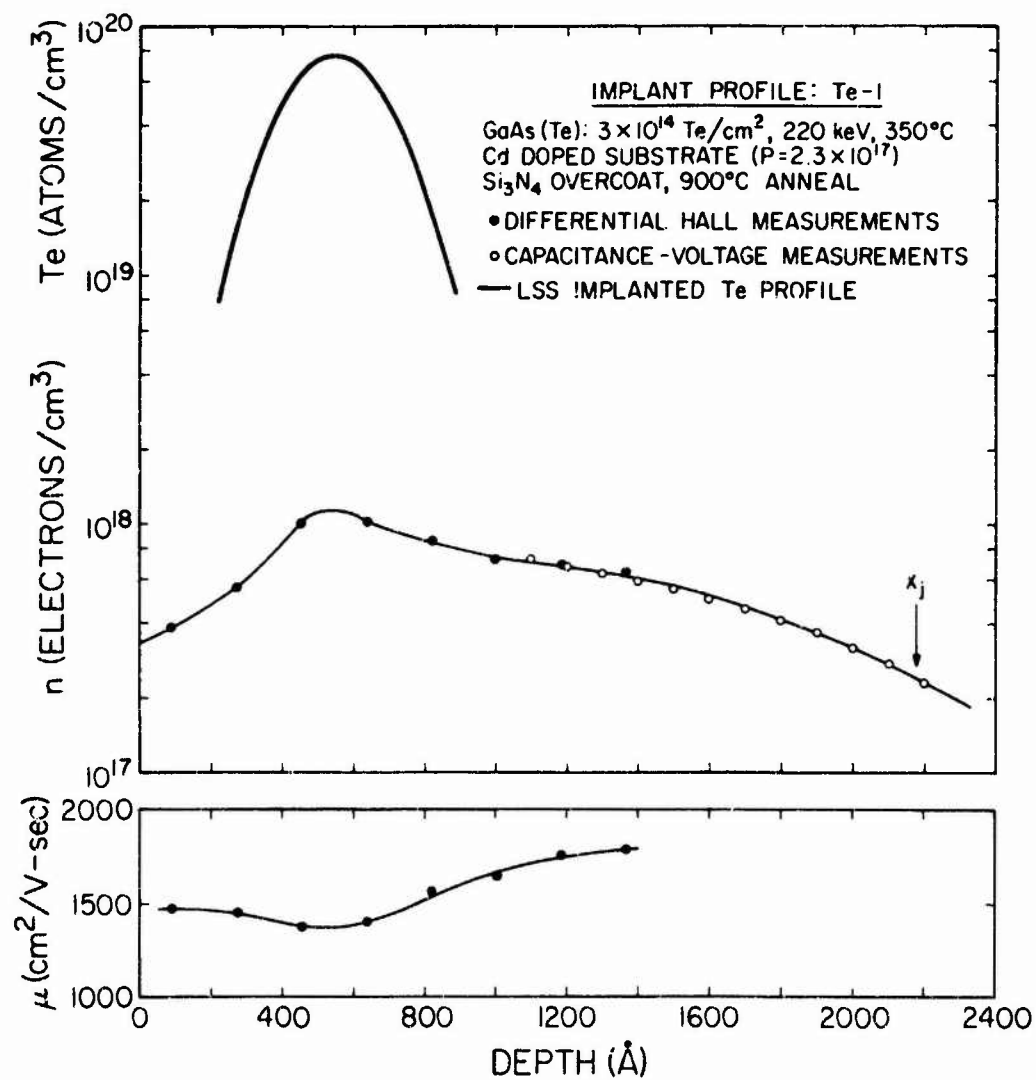


Fig. 3.3-3 Electron concentration and mobility profiles for a tellurium-implanted sample processed with a Si₃N₄ cap during anneal

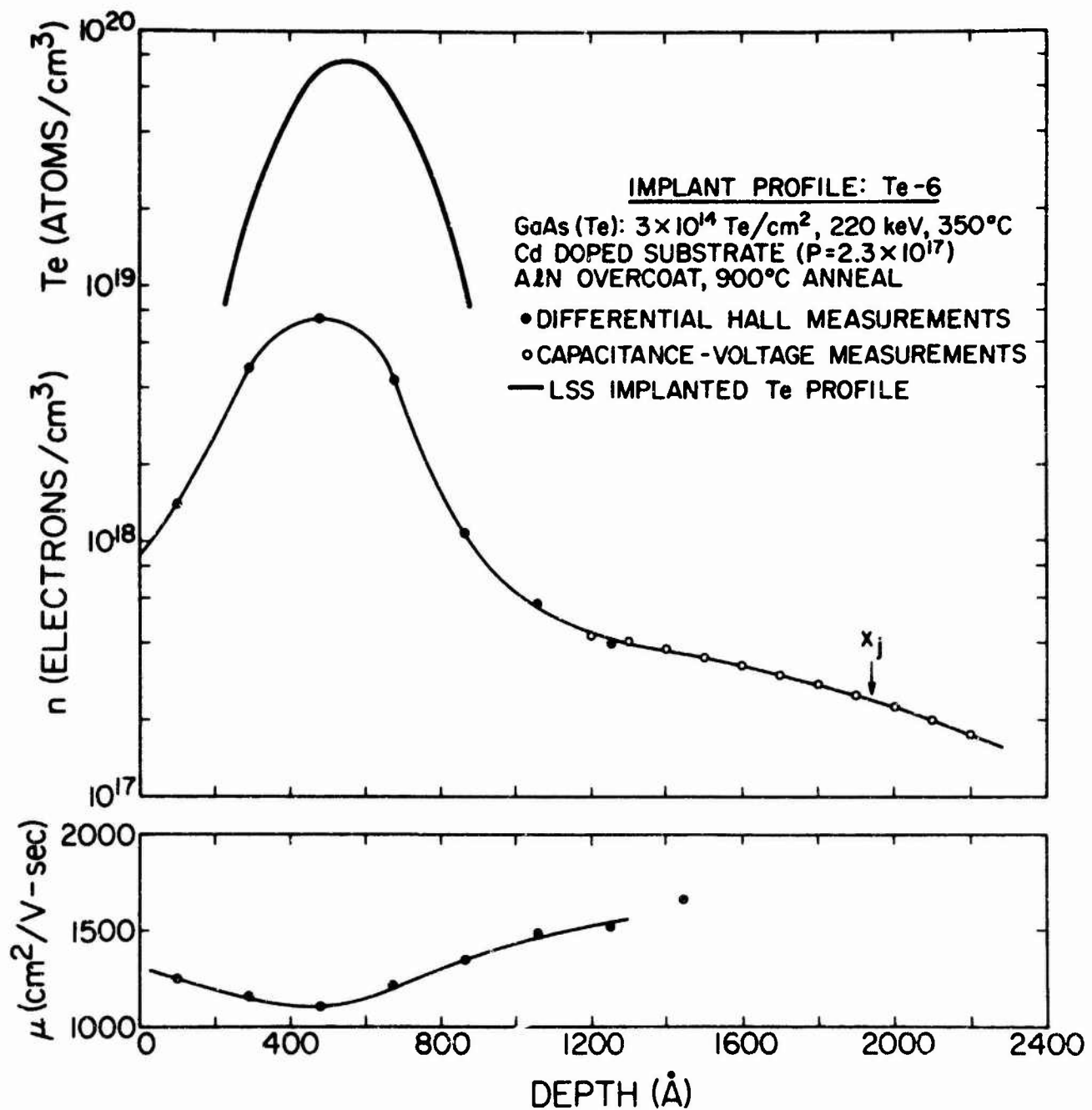


Fig. 3.3-4 Electron concentration and mobility profiles for a tellurium-implanted sample processed with an AlN cap during anneal

depth was determined by a measurement in the scanning electron microscope. From a knowledge of the initial hole concentration in the p-type substrate and this junction depth, it is possible to match the C-V data on the diode to the profile obtained from the stripping. Agreement between the two methods of measurement in the region where they overlap is quite good. In the case of the data shown in Fig. 3.3-5, no direct junction depth determination was made, and the superposition of the stripping data and C-V data was carried out by matching the slope of the two different curves. There is a considerable difference in the peak electron concentrations obtained for these two different samples. The sample shown in Fig. 3.3-4, which was annealed with an AlN cap, exhibits a maximum electron concentration of about 7×10^{18} which is approximately equal to the maximum electron concentration which has been obtained by doping GaAs with Te during growth. A profile for the sample which was annealed with Si_3N_4 on the surface shown in Fig. 3.3-3 has a peak carrier concentration which is only slightly above 1×10^{18} . In both the cases the peak depths agree well with that calculated for the Te distribution from the LSS²⁰ range theory. Both electron distributions show a tail region in which the electron concentration is much greater than would be predicted from the LSS theory.

A summary of the surface carrier concentration measured and the percent of electrical activity achieved in several p-type GaAs samples implanted with Te and annealed with either Si_3N_4 or AlN on the surface

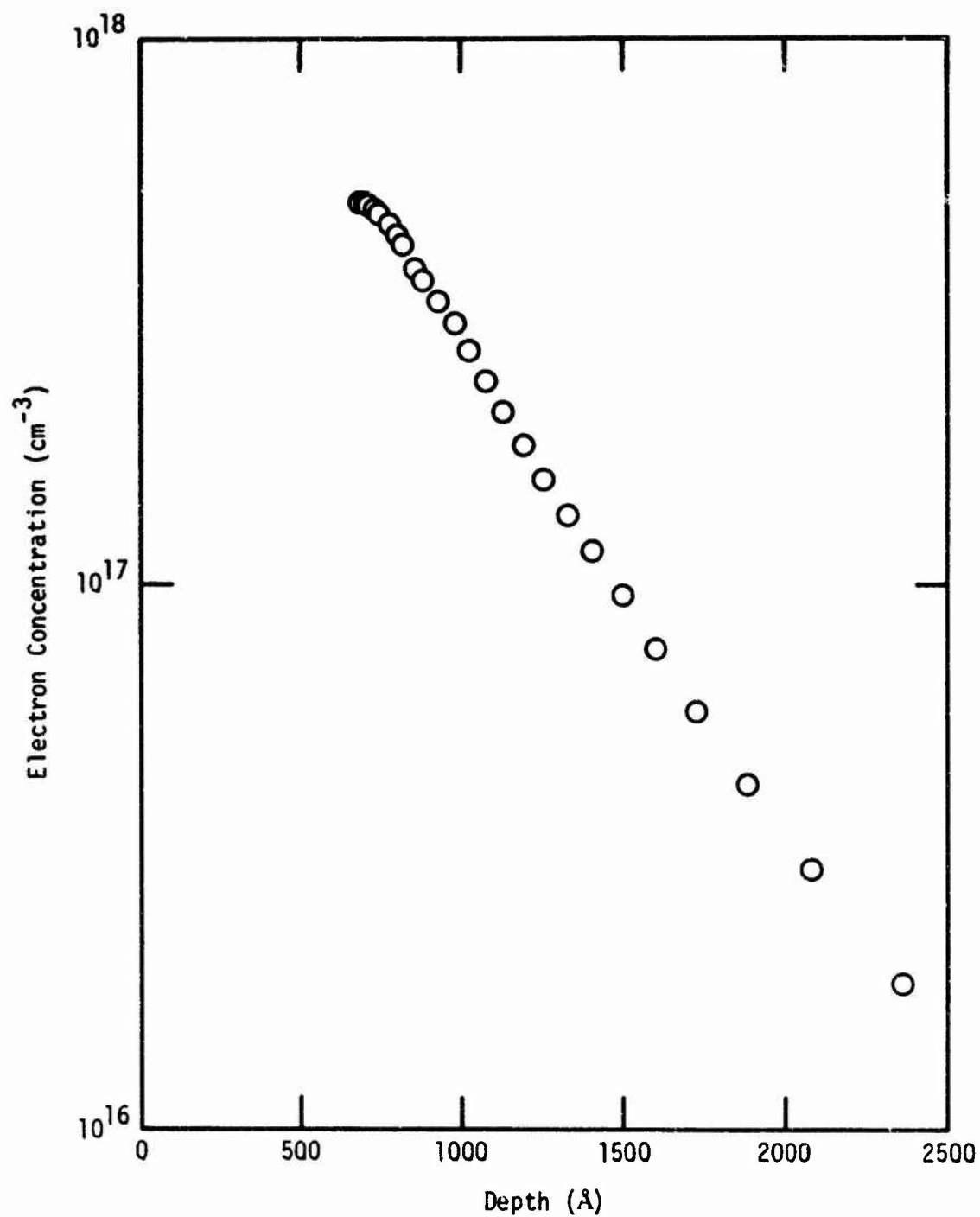


Fig. 3.3-5 Electron concentration vs depth profile obtained from Schottky barrier capacitance-voltage data for a sample implanted with 220 keV tellurium and annealed with an AlN cap

is shown in Table 3.3-1. For the highest doses shown, the efficiency is probably low because of the limitation on the electrical activity due to solubility effects. It can be seen that for the samples annealed with an AlN cap the efficiencies are higher and not as scattered as for the samples annealed with the Si_3N_4 cap. For the 1×10^{14} doses, for example, the results for an AlN cap are 20 and 23% electrical activity, whereas for Si_3N_4 the values obtained for electrical activity were 5%, 13%, and 20%.

Lower dose implants into Cr-doped semi-insulating GaAs have also been annealed with AlN on the surface. For implantation doses, of 3 to $4 \times 10^{12}/\text{cm}^2$, the electrical activity obtained has been found to be approximately 100%. The electron concentration profile for one such implanted sample obtained from Schottky barrier capacitance voltage measurements is shown in Fig. 3.3-5. As in the case of higher-dose implants into p-type substrates discussed above, this profile shows significant electron concentrations at depths well beyond those expected from the LSS range distribution.

The deeply penetrating tail on the electron distribution in both p-type and chromium-doped substrates may be due to diffusion of tellurium during annealing or some channeling of the tellurium during implantation. Further experiments are required in order to determine the relative contribution of these two mechanisms. Because of the deeply penetrating tail on the electron distributions resulting from tellurium implantation, it

Table 3.3-1
Comparison of Doping in Tellurium-Implanted GaAs
Annealed with a Si_3N_4 Cap or an AlN Cap

Sample No.	Implant Dose (cm^{-2})	Anneal Overcoat	Surface Carrier Concentration (cm^{-2})	% Electrically Active
Te-4	3×10^{13} (a)	Si_3N_4	6.6×10^{12}	17
Te-2	1×10^{14} (a)	Si_3N_4	7.2×10^{12}	5
G-74	1×10^{14}	Si_3N_4	2.0×10^{13}	20
G-80	1×10^{14}	Si_3N_4	1.3×10^{13}	13
Te-1	3×10^{14}	Si_3N_4	1.2×10^{13}	4
Te-3	3×10^{13} (a)	AlN	1.8×10^{13}	45
Te-5	1×10^{14} (a)	AlN	3.1×10^{13}	23
Te-19	1×10^{14} (a)	AlN	2.6×10^{13}	20
Te-6	3×10^{14}	AlN	4.0×10^{13}	13

(a) For these samples, an additional implant was made at 60 keV with a dose one-third of the 220 keV dose given.

will be necessary to determine implantation profiles for various implantation doses. In order to accomplish this, it is desirable to have a more accurate layer-removal technique than is provided by chemical etching. Previous work with Si-implanted layers suggests the use of anodic oxidation for layer removal. Several anodization studies of GaAs are reported in the literature. Recent attempts at Cal Tech to utilize these methods were not satisfactory. However, it has been found that N-methylacetimide (without KNO_3) gives uniform films with low leakage currents. Back-scattering and channeling measurements indicated that oxide films between 200 and 500Å thick could be grown. Further work is required to determine layer-removal rates and the various anodization parameters.

3.3.3 Device Processing, Fabrication, and Evaluation

One of the potential applications of ion implantation to GaAs is the production of thin n-type regions suitable for device fabrication. To demonstrate the feasibility of this application of ion implantation, GaAs Schottky barrier field effect transistors have been fabricated in an n-type film produced by sulfur implantation in a chromium-doped, semi-insulating GaAs substrate. The implantation of 1×10^{13} 100 KeV sulfur ions was carried out at a temperature of 350°C, and the implanted sample was annealed at 900°C covered with a 2000Å layer of Si_3N_4 . The measured sheet carrier concentration of the layer was $1.3 \times 10^{12}/\text{cm}^2$, and the mobility was 4900 $\text{cm}^2/\text{v-sec}$. Figure 3.3-6 shows the carrier concentration vs depth profile obtained from Schottky barrier capacitance voltage measurements. The measured profile shows a peak of at least 7×10^{16} electrons/ cm^3 at 1200Å,

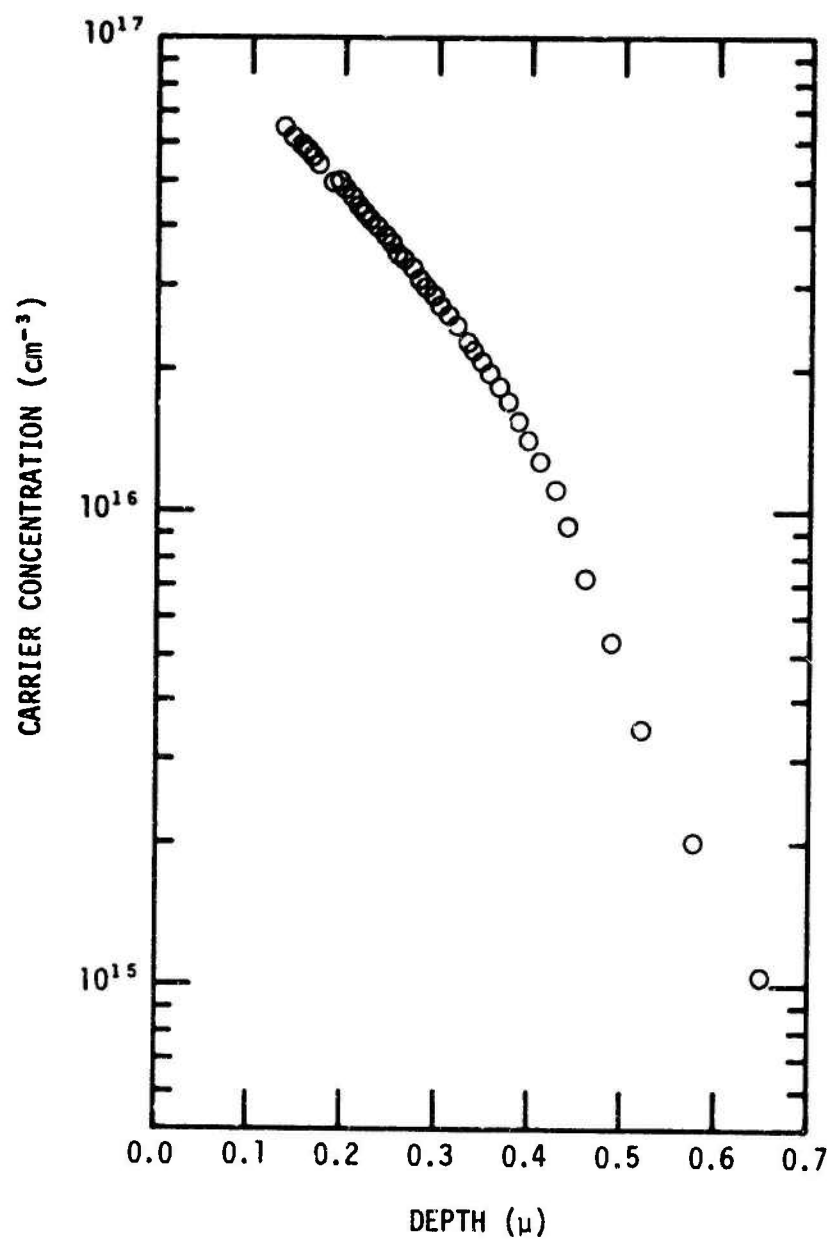


Fig. 3.3-6 Electron concentration vs depth profile obtained from Schottky barrier capacitance-voltage data for the sulfur-implanted layer used for FET fabrication

and a sharp drop to about 10^{15} electrons/cm³ at a depth of 6000Å. The profile is significantly deeper than the LSS theory would predict. This effect has been seen by other workers and attributed to a damage-enhanced diffusion occurring during the annealing cycle. Based on the carrier concentration and mobility results, this was a reasonable n-type layer for an FET device.

The gate length of 4μm and channel width of 12μm were chosen to simplify device fabrication rather than yield state-of-the-art devices. Standard techniques were used in applying the Au-Ge contacts and etching mesas to isolate the source and drain contacts from the gate pad. A 2000Å Al layer was evaporated and photoresist lifting techniques were used to produce a 4μm gate.

Current voltage characteristics for a typical FET device taken with the gate and substrate connected together are shown in Fig. 3.3-7. The device displays good FET action pinching off at about 2 volts reverse bias on the gate and has a high output impedance as indicated by the flat saturation curve. The gate Schottky barriers exhibited forward conduction at a bias of 0.6-0.7 volts and showed a reverse breakdown voltage of 10-12 volts. The maximum transconductance of the device shown in Fig. 3.3-7 was 3.75 mA/V, which is somewhat less than one would predict from a simple estimate based on the concentration vs depth profile. The substrate materials on which these devices were fabricated had a less than ideal semi-insulating quality which probably significantly affects the

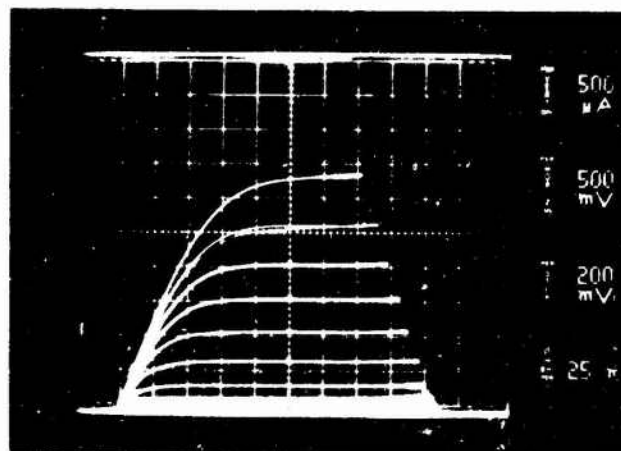


Fig. 3.3-7 Current-voltage characteristics of an FET fabricated in an n-type layer produced by sulfur ion implantation

electrical characteristics of the devices. The devices exhibited a slightly lower transconductance when tested with the substrate grounded to the source. When they were illuminated with light of bandgap energy or greater, a significant increase in the transconductance and saturation current level was observed. This effect presumably involved carrier trapping in the GaAs but is not understood in detail at present.

This work shows that thin film n-type devices such as FET's can be produced from ion-implanted GaAs. One of the most important observations is that the yield of working devices was about 70%. The majority of the device failures occurred because of gate metallization problems which are unrelated to the use of an implanted layer. This high yield of working devices demonstrates the control of doping uniformity which can be expected from implantation. It is our intention to produce more implanted FET's and to make high-frequency microwave measurements in order to fully evaluate the potential of implantation. A major problem associated with this application of implantation is lack of high-quality semi-insulating substrates or semi-insulating epitaxial films with which to work.

3.4 Interface Measurements

Interface defects in epi-layer growth may have their origin in the heat treatment of the surface of a substrate prior to growth or in the slight lattice mismatch due to very small changes in the lattice constant arising from impurity contents.

Two experiments have been performed, and the results from these experiments indicate that at the low temperatures used for the epitaxial growth of MESFET-type layers of GaAs, no damage is induced on a substrate surface and that the interface between two epitaxial layers of moderate carrier level is free of any noticeable defects.

The first experiment performed this quarter was a series of ESCA measurements on surfaces of GaAs. Several pieces of a crystal of GaAs were subjected to different surface preparations and then measured for surface chemical analysis with particular emphasis on the measurements of stoichiometry. The relevant preparations were the chemical etching normally used in substrate preparation and the heat treatment of the surface as performed prior to epitaxial growth. The latter treatment means the annealing in hydrogen gas at 700°C and at 800°C for at least one hour. Also, other treatments including proton bombardment and ion implantation were used.

ESCA measurements are a form of Auger electron spectroscopy. Intense electromagnetic (X-ray) radiation excites core electrons of surface atoms to a very high energy state. The X-ray radiation is monochromatic and is the K_{α} line of aluminum, therefore, having an energy of 1486.6 eV. An energy-dispersive electron spectrometer counts the electrons emitted from the material with a resolution of .75 eV. In the spectrum of emitted electron energies are the peak electron counts at energies characteristic of the core electrons of all the atoms at the surface. Different elements present may be sorted out as their characteristic energies are easily discernible. In the case of GaAs the energies corresponding to the core, 3d electrons were used in our experi-

ment on the stoichiometry measurement. Relative data only can be obtained, but by careful signal averaging techniques and subtraction of the background one may come to a measurement of within 1% of the Ga-to-As ratio. Also, one may obtain relative data on the quantity of oxide of Ga and As present as separate peaks are detected for these atoms in their oxide phases.

This type of measurement was performed on the surfaces of four crystals. All were chemically etched in the normal manner in an acid etch with the make-up $3\text{H}_2\text{SO}_4:1\text{H}_2\text{O}$. One piece was then ion-implanted with tellurium at an energy of 100 KeV and dosage of $10^{14}/\text{cm}^2$. Then two were separately annealed in hydrogen at 675°C and 790°C . The results of the ESCA measurement are shown in Table 3.4-1. The notable point with respect to the annealed samples is their almost perfect stoichiometry in comparison with the other two samples and also the reduction in the oxide quantity detected.

Upon probing the annealed samples and depositing Schottky barrier capacitors thereon, no detectable n-layer was seen upon the surface of these semi-insulating substrates.

As an experiment to detect the presence of trap states or extra defect sites at the interface between two epitaxial growths, we grew by liquid phase epitaxy a thin $10^{17}/\text{cm}^3$ n-type layer on top of another epitaxial layer of electron level $10^{16}/\text{cm}^3$. The C-V curve taken on this structure, shown in Fig. 3.4-1, indicated a flat profile for the top layer with a straight line curve for $(1/c^2)$ as a function of V . At the interface, no flattening of the C-V curve was noticeable nor any marked drop to indicate extra traps or compensa-

Table 3.4-1
Determination of Ga and As on GaAs Surfaces
After Treatment as Measured by ESCA

Date	Run No.	Sample No.	Treatment	Normalized Ga Area	Normalized As Area	Ga:As	Remarks
11-1-73	11	(11)	Chemical Etch	79888	113623	0.70	Both Ga & As ~ 1/3 oxide
11-1-73	16	(14)	H ₂ Heat Treat 791°C	33345	33814	0.99	Ga 1/5 oxide As 1/10 oxide
11-3-73	18	(12)	Te Implant	76271	57463	1.33	Ga 1/1.2 oxide As 1/10 oxide
11-1-73	19	(15)	H ₂ Heat Treat 675°C 1/2 hr	33176	34844	0.95	Ga ~ 1/4 oxide As almost no oxide

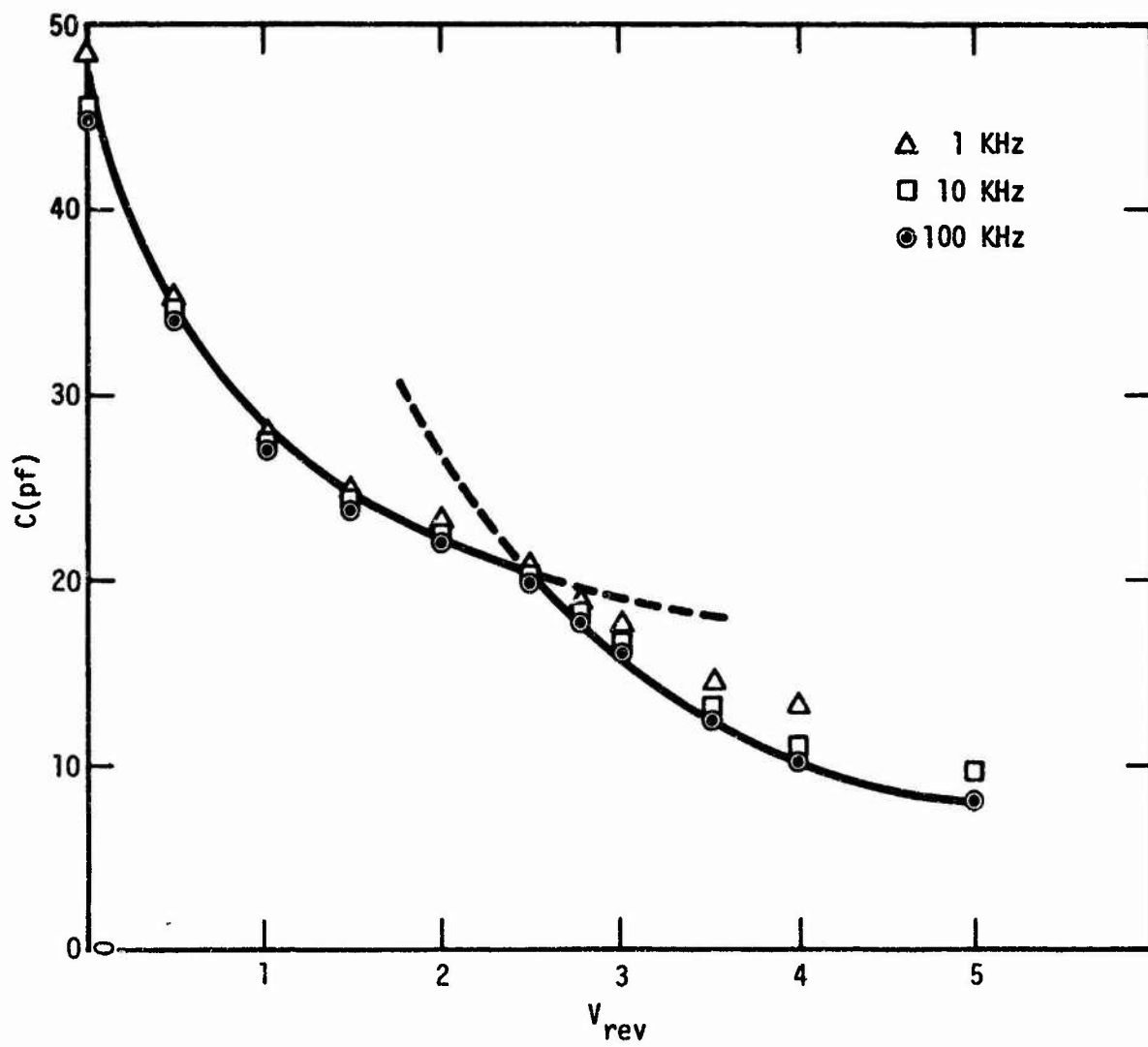


Fig. 3.4-1 C-V measurements on an epi-on-epi interface.

tion at this point. Therefore, the first interpretation of this curve is of a homojunction where there is a minimum of defects. There is one thing that is out of order and this is the slow rate of descent of the free carrier level to the expected 10^{16} level. The rate of descent might be expected to be in accord with a Debye length of $500\text{\AA}$ but seems rather to be descending at a rate more in accordance with a Debye length of $1000\text{\AA}$. This is related perhaps to diffusion of dopant into substrate.

4.0 FUTURE PLANS

4.1 Epitaxial Material Growth and Characterization

4.1.1 Ultra-Thin, High-Conductivity Layer

The redesigned growth system is presently undergoing a period where minor faults are being corrected. In the next three months the basic properties of the redesigned growth system will be tested. The main expected result will be the much greater control over the growth of extremely thin layers. Layers of $2000\text{\AA}$ should be grown in seconds or more rather than the present extremely fast rates. Meanwhile, on the contract, growth will be continued using the conventional apparatus and technique so that devices can be processed and evaluated. There will be an attempt using the conventional apparatus to operate at lower saturation temperatures.

Material evaluation will continue to put emphasis on measuring thickness uniformity. Stripping measurements of Hall voltage are to be done on thin layers to provide information on mobility near the interface.

4.1.2 High-Resistivity GaAs Thin Films

1. Improve the technique for the growth of LPE GaAs at temperatures below 600°C by using slower cooling rates and by finding a method to reduce the oxide on the substrate surface.
2. Reduce the impurity concentration in the undoped GaAs epi-layer to achieve higher mobility and lower background carrier densities.
3. For Cr-doped LPE GaAs growth:
 - a. Use faster cooling rates to increase the effective segregation coefficient and add larger amounts of Cr to the growth to make the Cr concentration in the epi-layer exceed the background impurity concentration and thus bring the total carrier concentration down to the semi-insulating region.
 - b. Use higher temperatures to study the amphoteric behavior of the Cr in the GaAs epi-layer.

4.1.3 Processing and Device Measurements

4.1.3.1 MESFET. The improvements on the ohmic contact area will be continued. Present work is aimed at increasing the thickness of contact metal that can be defined and lifted.

Using the 4 μ m gate transistor, preliminary experiments will be conducted to:

1. Measure the effects of substrate quality

2. Measure the effects of improved material uniformity of thickness
3. Measure the effects of improved ohmic contact processing
4. Measure and evaluate the effectiveness of proton bombardment for isolation

The measurements referred to will be those of r.f. power, gain, and noise figure.

4.1.3.2 IMPATT. The application of the device and circuit theory to measurement of GaAs avalanche devices will continue with an emphasis on deriving a better measure of saturation velocity of electrons and the ionization rates of electrons and holes in GaAs.

4.2 Semi-Insulating Materials

4.2.1 Crystal Growth

It is planned that USC will provide the Science Center with semi-insulating material for evaluation shortly.

4.2.2 Measurements

Routine mass spectroscopy analysis will be done on samples of all materials purchased or received from USC.

The transient capacity technique will be evaluated and tested as a substitute of trap-filled-limit breakdown for quantitative measurements of trap densities. Reflection X-ray topography will be tested and compared with other techniques for monitoring dislocation densities.

The above measurements will have first priority because of their role in a loop that starts with material characterization and ends with device evaluation. Complementary measurements of photoconductivity and thermally-stimulated currents will be continued. Work will be continued on the problem of low breakdown effects in the substrate material.

Efforts will be made to perform some of the characterization measurements, mainly capacity, on actual MESFET device structures in order to establish some direct correlation between substrate trap densities and low-frequency characteristics of the device.

4.2.3 Proton Bombardment and Oxygen Implantation

Proton bombardment work be continued and oxygen implantation will be started.

In the proton bombardment work, the goal is to observe how low-temperature annealing degrades the high-resistivity in order to predict the effect of heating of a device in operation. In oxygen implantation the goal is to verify that compensation by oxygen is the dominant mechanism to produce high resistivity. A second goal for both techniques is to establish practical recipes in terms of dosage and exposure.

4.3 n-Type Doping of GaAs by Ion Implantation

4.3.1 Annealing Cap

The effort to reduce the oxygen content of AlN films will continue. The effects of varying the temperature at which the substrate is held

during sputtering, and other parameters, will be investigated. Composition and density of films will be correlated with their effectiveness as an annealing cap.

4.3.2 Characteristics of Implanted Layers and Junctions

Development of the anodization technique will continue and it will be applied to the stripping of implanted samples. Profiles will be measured for different implant and anneal conditions, using the anodization technique. The use of multiple energy tellurium implants to obtain an n-type layer suitable for FET fabrication will be explored.

4.3.3 Device Processing, Fabrication, and Evaluation

Progress here will depend somewhat on the success of the efforts under 4.3.2. It is hoped that some n-type layers will be produced which can be used for device fabrication. When such layers are available, FET's will be fabricated and evaluated.

Rockwell International Corporation's Science Center has taken the following steps to save energy: heat has been turned off in conference rooms and unoccupied offices and reduced in all other areas, light levels in halls and offices have been reduced and all exterior decorative lights have been turned off; air-conditioning has been reduced along with the exhaust system operation; and employees have been encouraged to form car pools as well as informed on various means of conserving energy both at the office and at home. Additional efforts are being planned to make better use of energy and fuels.

5.0 REFERENCES

1. T. Inoue and M. Ohyama, Sol. State Comm. 8, 1309 (1970).
2. See, for example, T. Ikona and B. Jeppsson, Gallium Arsenide and Related Compounds, Proc. of Fourth Inter. Symp. at Boulder, Colorado, September, 1972; published by the Institute of Physics, London, p. 75.
3. C. I. Huang and S. S. Li, Sol. State Electronics 16, 1481 (1973).
4. See, for example, M. Halliwell, J. B. Childs, and S. O'Hara, Gallium Arsenide and Related Compounds, Proc. of Fourth Inter. Symp. at Boulder, Colorado, September, 1972; published by the Institute of Physics, London, p. 98.
5. A. G. Foyt, W. T. Lindley, C. M. Wolfe, and J. P. Donnelly, Sol. State. Electronics 12, 209 (1969).
6. P. N. Favenec, G. P. Pelous, M. Binet, and P. Bauded, Ion Implantation in Semiconductors and Other Materials, B. L. Crowder, ed., Plenum Press, New York (1973), p. 621.
7. J. S. Harris, F. H. Eisen, B. Welch, J. D. Haskell, R. D. Pashley, and J. W. Mayer, Appl. Phys. Lett. 21, 601 (1972).
8. F. H. Eisen, J. S. Harris, B. Welch, R. D. Pashley, D. Sigurd, and J. W. Mayer, Ion Implantation in Semiconductors and Other Materials, B. L. Crowder, ed., Plenum Press, New York (1973).
9. B. L. Mattes and R. K. Route, J. of Crystal Growth 16, 219 (1972).
10. Final Report, "Synthesis of Compound Semiconducting Materials and Device Application," ARPA Contract No. DAHC15-70-C-6, Stanford University, July 1, 1972-June 30, 1973.

11. E. Andre and J. N. LeDuc, *Mat. Res. Bull.* 4, 149 (1969).
12. C. A. Lee, R. L. Batdorf, W. Wiegmann, and G. Kaminsky, "Time Dependence of Avalanche Processes in Silicon," *J. Appl. Phys.* 38 (7), 2787 (1967).
13. C. A. Lee, R. L. Bardorf, W. Wiegmann, and G. Kaminsky, "Analysis of the Q Factor, Efficiency, Stability and the Design of Read Structures in the Nonlinear Range," *J. Appl. Phys.* 38 (7), 2797 (1967).
14. R. Kuvas and C. A. Lee, "Quasistatic Approximation for Semiconductor Avalanches," *J. Appl. Phys.* 41 (4), 1743 (1970).
15. R. Kuvas and C. A. Lee, "Carrier Diffusion in Semiconductor Avalanches," *J. Appl. Phys.* 41 (7), 3108 (1970).
16. C. E. Jones and A. R. Hilton, *J. Electrochem. Soc.* 113, 504 (1966).
17. See, for example, A. G. Milnes, Deep Impurities in Semiconductors, Wiley, New York (1973), Ch. 11.
18. R. H. Bube, G. A. Dussel, C. T. Ho, and L. D. Miller, *J. Appl. Phys.* 37, 21 (1966); W. C. Mallard and J. H. Crawford, *J. Appl. Phys.* 43, 2060 (1972).
19. G. A. Allen, *J. Phys.* D1, 593 (1968).
20. J. Lindhard, M. Scharff, and H. E. Schiøtt, *Mat. Fys. Medd. Dan. Vid. Selsk.* 33, no. 14 (1963).