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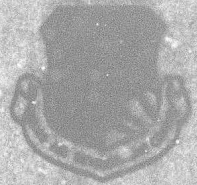
AUTHORITY

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ASFIR THIRD SITE MODIFICATIONS

John Dodson

RCA Missile and Surface Radar Division

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FOREWORD

This final report was prepared by the Missile and Surface Radar Division of the Radio Corporation of America, Borton Landing Road, Moorestown, New Jersey 08057, under Contract AF30(602)-3743, Project 6512, Task 651209. The author was John Dodson. The following RCA engineers contributed significantly to this report: R. Houck, G. Stevens, and R. Rippey.

RADC Project Engineer was Earle H. Filer, EMASE.

This document is not releasable to CFSTI because it contains information embargoed from release to Sino-Soviet Bloc Countries by AFR 400-10, "Strategic Trade Control Program."

This technical report has been reviewed and is approved.

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Ch, Surveillance and
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FOR THE COMMANDER:
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ABSTRACT

Changes and additions were made to the two-site Active Swept Frequency Interferometer Radar (ASFIR) to provide three-site capability. Addition of the second base line (3rd Site) required a new angle tracker, timing and logic modifications, new mode selection logic and revised data formatting. Distribution and generation of new RF signals were also required. New capability designed into the modification program included extended unambiguous range tracking to 3600 nmi, reduction of system timing jitter, frequency multiplexing of the range rate and angle rate signal processing, and target simulation. The total modification kit included six new racks of equipment plus considerable changes to the existing 14 racks of equipment, including relocation for optimum packaging. Verification of the changes, using the target simulator (which proved to be an effective tool for system test, alignment and evaluation) and by tracking Echo II, showed a considerable improvement in track loop performance and a 3:1 reduction in system timing jitter. Data formatting and logic compatibility were shown by producing a test data tape for data reduction. Detailed recommendations include noise reduction techniques, short term phase stability improvements, improved modulation methods, and system changes to eliminate system timing jitter and to provide AGC.

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LIST OF ILLUSTRATIONS

EVALUATION

The modifications described in this report are a part of the changes incorporated in the ASFIR system to provide for a two baseline operation.

Incorporated in these changes are improvements that give better and more flexible operation of the ASFIR system.

ASFIR is an Air Force Program to obtain high angular accuracies on orbital bodies conducted under project 6512.

EARLE H. FILER
Project Engineer
EMASE

SECTION I

INTRODUCTION

The contract on the ASFIR Third Site Wide Band Exciter/Data Take Off (WBE/DTO) Modification was awarded to RCA in July 1965. The effort to be accomplished included the revision of existing equipments supplied previously by RCA to RADC under contracts AF 30(602)-2804 and AF 30(602)-3125.*

The modifications accomplished on this contract were necessitated by the addition of a second base line to the existing ASFIR system. Included in the contract were the changes of logic, timing and hardware implementation necessary to be compatible with the additional slave site. In addition, significant system capabilities were added, including increased unambiguous range capability, reduction of system jitter, doppler fine line correction and target simulation equipment.

The basic concept of the WBE and its relationship with ASFIR is described in RADC Technical Report TDR-63-114 and supplemented in RADC-TDR-63-353 and RADC TR-65-18. These reports offer a rather comprehensive treatment of the concept, development and final configuration of the WBE/DTO complex. These fundamentals were not altered but were merely expanded by the subject contract.

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*Effort on these contracts ended in July 1964.

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SECTION II

ORIGINAL SYSTEM CONFIGURATION

Before proceeding with the discussion of the modification and additions
to the existing equipment, a brief description of the original wideband
exciter - data take off (WBE/DTO) equipment will be given. For more design
detail the reports mentioned in Section I should be consulted.

The main feature of the original WBE was the technique employed to
generate the linear frequency ramp (FR) for transmission and the delayed
replica for correlation (DCFR). The technique was the same for FR and DCFR
except that the DCFR was compensated for target doppler. The linear wave-
form was developed by generating a staircase frequency waveform by means of
a digital oscillator (DO), and the staircase is filled in with a linear saw-
tooth frequency waveform. The DO generates frequency jumps of F, 2F, 4F
... 64F, while the fill-in ramp frequency deviation is only F. The nF
signals are derived by digital division of the system master clock frequency
and imposed upon convenient carriers for mixing and frequency translation.
The derived waveform with duration of 2400 μs (4.8 MHz) is then converted to
3.0 GHz for transmission. Five transmission waveforms are available: pulsed,
CW, 4.8 MHz (increasing or decreasing frequency) and 48 MHz (increasing or
decreasing frequency). The 48 MHz bandwidth is obtained by multiplying the
4.8 MHz ramp by 10. The DCFR is generated at the appropriate point in range
to supply the cross correlation reference for pulse decoding. After cross
correlation, the resultant narrow-bandwidth signal is spectrum analyzed by
coherent memory filters. These integrators supply time analogs of frequency
which are tracked by the WBE/DTO servo loops. For single pulse coherent
memory filter (SPCMF) operation, split gate (EG/LG) discrimination is used.
The targets are tracked in range, range rate, angle and angle rate. Error

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signals proportional to the energy in the EG/LG discriminator are used to control the various VCO's used in the range, range rate, angle and angle rate trackers.

In the multiple pulse coherent memory filter (MPCMF) mode of operation, the fine line spectrum is analyzed by a center-of-gravity tapped delay line range technique to derive errors for the range and range rate track loops. The rate information is obtained by sampling the position of the center fine line with respect to the system reference center frequency.

The WBE also generates all of the system timing, such as pulse repetition rates, pulse widths, pre-trigger and range gates. The DTO establishes mode control and selection, displays, operator controls and all data recording. Data is recorded on digital tape in IBM format.

The DTO has the angle and angle rate servo loop including the voltage controlled oscillators.

The general relationship of the WBE/DTO with the ASFIR system is shown in Figure 1. The diagram has been coded to indicate changes and new equipment.
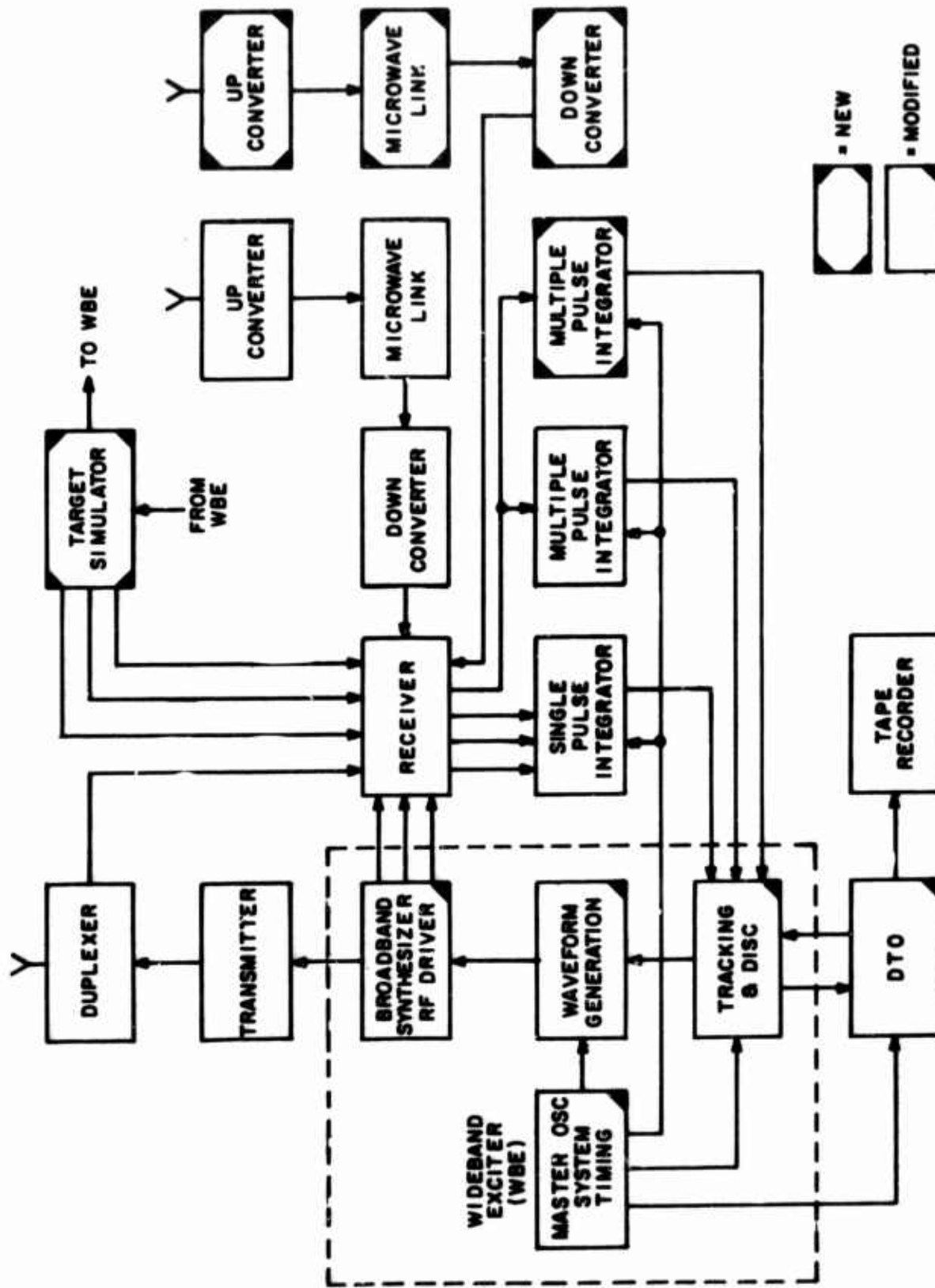
Fig 1 - Relationship of the Wide Band Exciter to the ASFIR System

SYSTEM CHANGES

Changes in the system are described in the following paragraphs.

1. ANGLE AND ANGLE RATE TRACKER AND VOLTAGE CONTROLLED OSCILLATOR

Addition of the second baseline required one new angle tracker. This tracking loop is essentially the same as the one in the present equipment for the first base line. There are two major differences: (1) the Θ_2 and $\dot{\Theta}_2$ VCO's have a frequency deviation of 2.2 times the Θ_1 and $\dot{\Theta}_1$ VCO's, and (2) a single pulse integrator is included in the servo loop for single pulse mode only. Figure 2 shows the general block diagram of this portion.

2. DELAYED COHERENT FREQUENCY RAMP (DCFR) AND CW LOCAL OSCILLATOR

To provide for the decorrelation of the second slave site target echo return, a receiver local oscillator signal at 3072 MHz was generated. This signal is referred to as the Angle 2 DCFR and has the appropriate modulation, either CW or FM (.1 or full deviation) to decode the carrier and provide a CW IF pulse at 72 MHz.

In addition, several existing CW signals were needed for new functions. In every case the distribution was made by feeding the existing signal into an amplifier capable of driving up to five loads with an interchannel isolation of better than 40 dB. This was done to minimize any interaction between new and existing equipment. Figure 3 shows the block diagram of this implementation.

3. VARIABLE PHASE SHIFTER

Alignment of the digital oscillator (DO) had been done by changing lengths of cable at 21 points within the DO and observing the effects upon
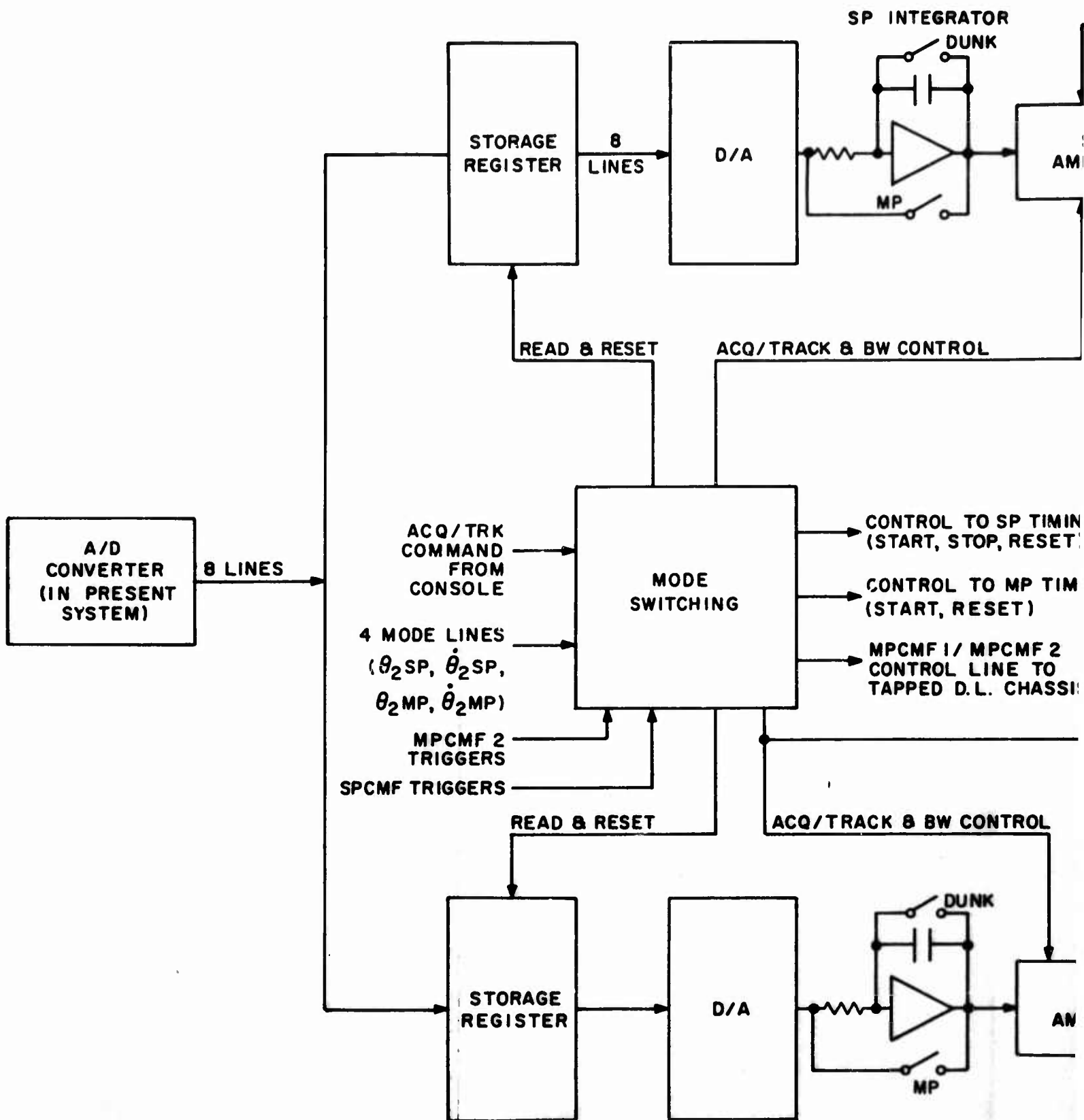
Fig 2 - Angle 2 and Angle Rate

ATOR
UNK

SERVO
AMPLIFIER

SLEW VOLTAGE IN

ANGLE ANALOG TO
DESIGNATION CIRCUITRY

θ_2 VCO
69 MHz ± 4 MHz

64 MHz
CW

5 MHz ± 4 MHz
θ_2 OUT TO
FREQUENCY CTR.

OL

TO SP TIMING
(TOP, RESET)

TO MP TIMING
(RESET)

MPCMF 2
LINE TO
O.L. CHASSIS

FEED
FORWARD
NETWORK

θ_2 MODE

69 MHz ± Δf
TO ANGLE 2
DCFR

$\dot{\theta}_2$ MODE

CONTROL

SLEW VOLTAGE IN

ANGLE RATE ANALOG
TO DESIGNATION
CIRCUITRY

UNK

SERVO
AMPLIFIER

$\dot{\theta}_2$ VCO

$\dot{\theta}_2$ MIXER

69 MHz ± 12 KHz

66 MHz

$\dot{\theta}_2$ OUT TO
FREQUENCY CTR.
3 MHz ± 12 KHz

Angle Rate 2 Track Electronics

2

Fig 3 - Frequency Synthesi

ALL DIST. AMPL. ARE W

TO TARGET SIMULATOR

66 MHz
FROM J17 — CE — EF
5 MHz FREQ. SYNTH

EF

TO ASFIR SYSTEM

EF

CONVERTER

EF

TO TARGET SIMULATOR

ITH

EF

ONVERTER)

69 MHz
FROM J14 — CE — EF — TO ASFIR SYSTEM
10 MHz FREQ. SYNTH

EF

TH

TO SP FREQ. OFFSET PROC

EF
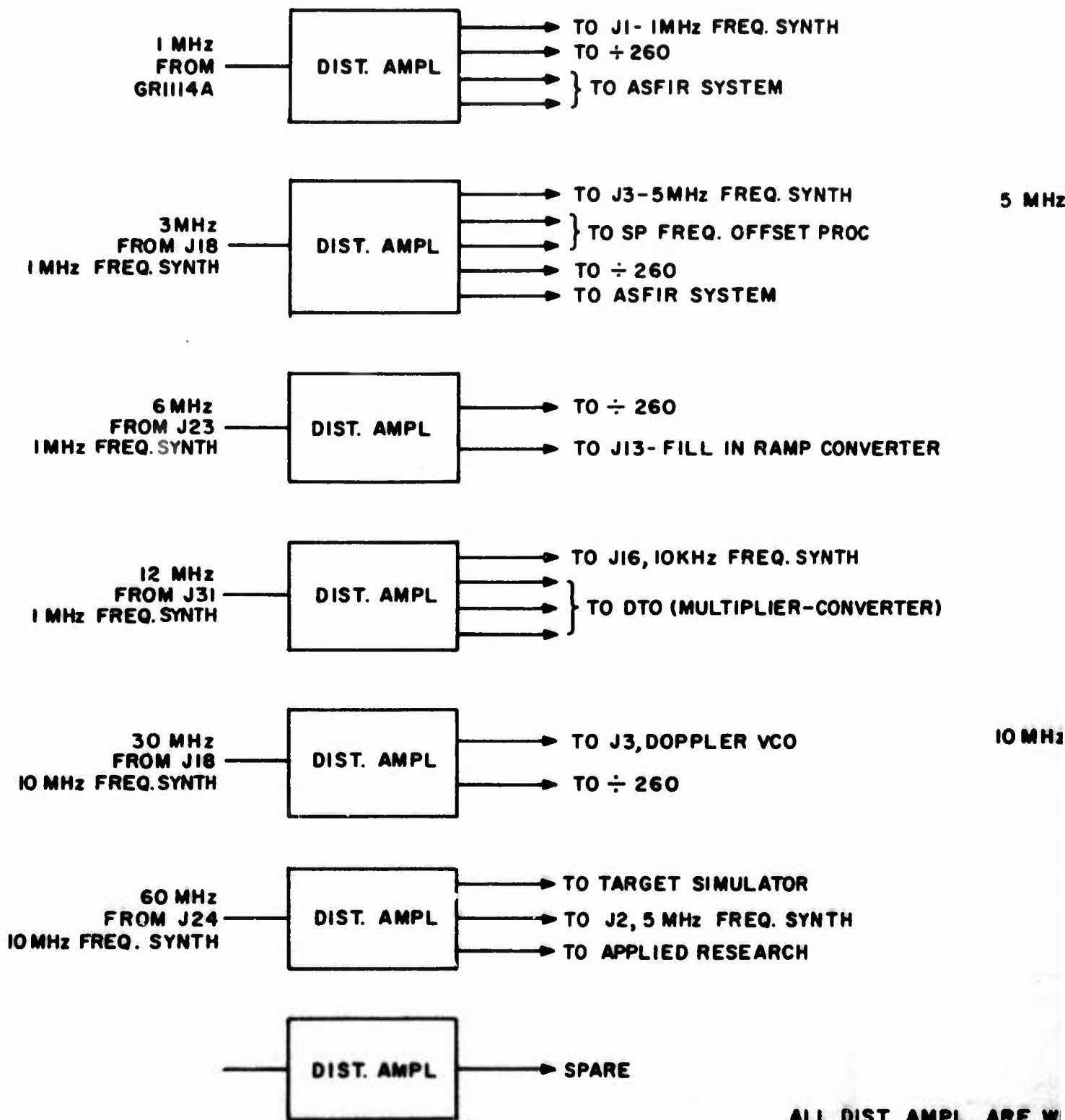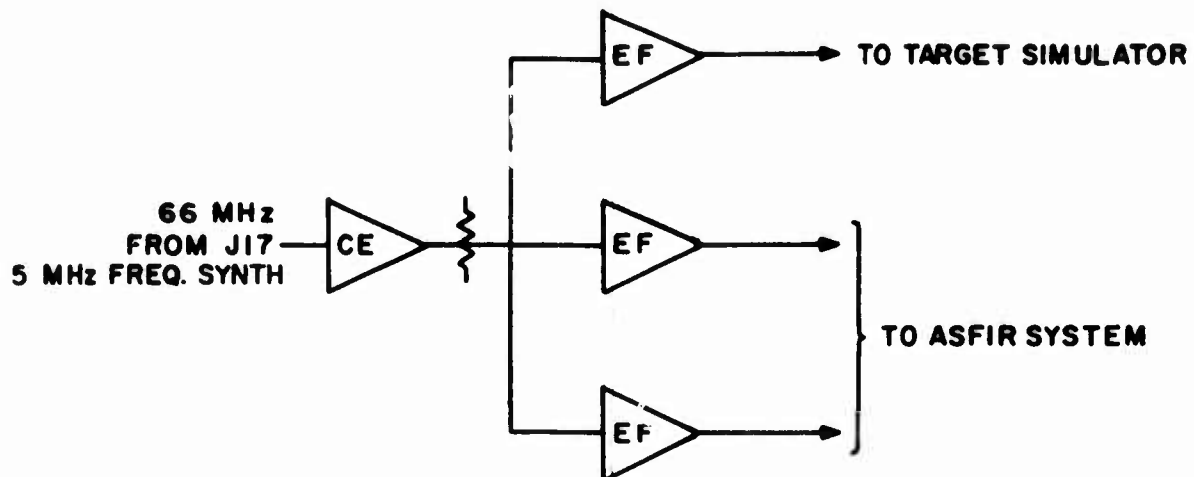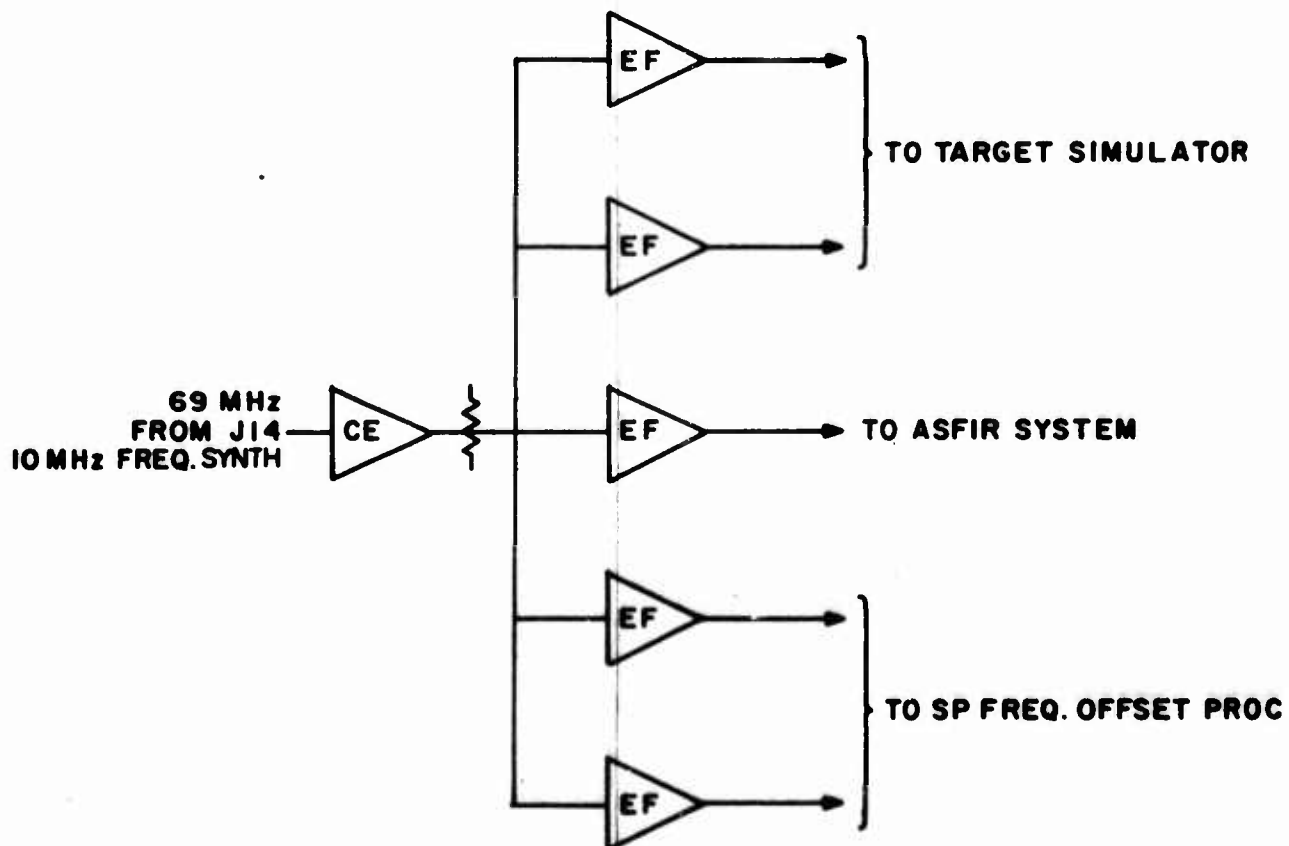
DIST. AMPL. ARE WBE 8632871

- Frequency Synthesizer/Buffer

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2

the correlated spectrum using the Single Pulse Coherent Memory Filter (SPCMF).

For the modification kit, wide band phase shift modules were used to replace these cables. Phase adjustment is now accomplished by tuning the capacitance of an R/C phase shifter. The shielded plug-in module not only provides phase adjustment but provisions have been added for amplitude control as well.

4. CONTROL CONSOLE

The control console was modified to permit selection of the two new modes (Θ_2 and $\dot{\Theta}_2$) for acquisition, display, joy stick, meter control, and printer readout.

The switches to permit the alternative transmission of 0.1 deviation and full deviation frequency ramps, and doppler fine line correction were added.

The zone and PRF in use is shown by a lamp display with automatic and manual selection of zone and PRF available.

5. TIMING AND DATA FORMATTING

The timing and data formatting were modified and 22 new digital signals generated. The IBM format was modified for optimum packing of the new data words. Additional data storage for the Θ_2 and $\dot{\Theta}_2$ data was also provided.

6. FREQUENCY COUNTER

In the present system a single counter was shared for the counting of the $\dot{R}$ and $\dot{\Theta}_1$ VCO frequency. The modification provides for two new counters to alleviate the necessity of sharing. These new counters are used for $\dot{\Theta}_1$ and $\dot{\Theta}_2$ with the old counter being used for $\dot{R}$.

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SECTION IV

SYSTEM ADDITIONS

In addition to the above mentioned changes a significant part of the contract was devoted to the design of techniques to provide considerably improved performance and capability. These increases in capability are discussed in the following paragraphs.

1. UNAMBIGUOUS RANGE

The original system had a single PRF of 100 pps with transmitted pulse widths of 2.4 and 1.2 milliseconds. These parameters limited the usable range to 98.5 nmi (minimum) to 782 nmi (maximum). To provide for a wider usable range and to permit a more abundant source of satellite targets, two significant changes were made. The pulse widths were made selectable. Three choices were provided (2.4, .976 and .578 milliseconds). In addition three PRF's were used (100, 80.6, and 65.8 pps).

The block diagram for the 3-PRF Wide Band Exciter System is shown in Figure 4. It should be noted that the primary zone and PRF control is located in the Data Take Off (DTO) System. The PRF and zone control shown in the WBE (Wide Band Exciter) block diagram are logic functions making use of the primary controls from the DTO.

The FR (frequency ramp) and DCFR PRF Counters have been modified to accommodate the three PRF's. This was accomplished by controlling the feedback for each PRF. An extra stage was also added to each counter. Depending on the PRF, the PRF counters are reset to a number (1024-N PRF). The PRF then counts the state of all "zeroes" in the counter. The counter is reset at this time to the number (1024-N PRF) and the cycle is then repeated. This technique makes it possible to gate out all pre-triggers with the same gating for all PRF's.

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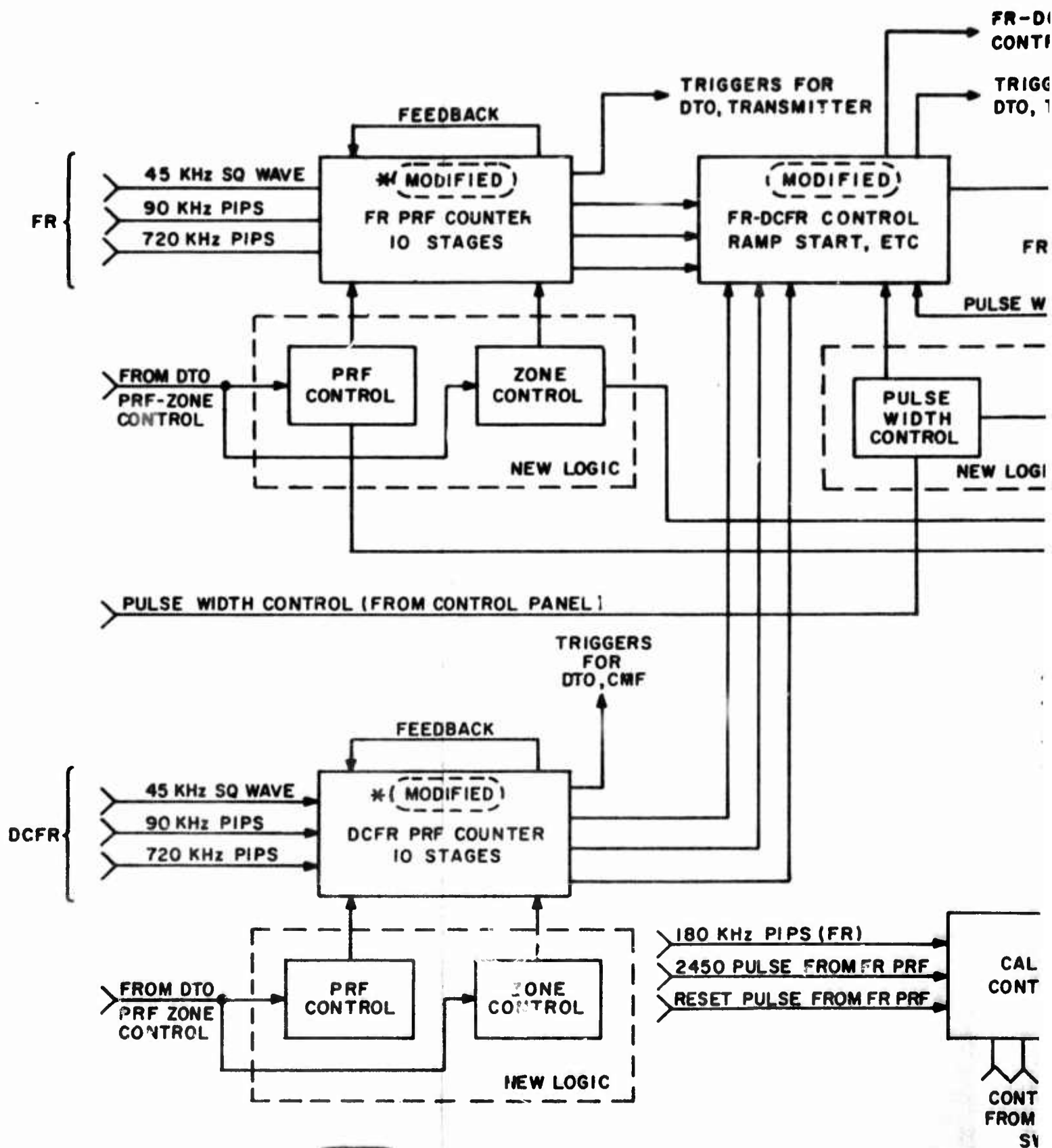
Fig 4 - Wide Band Exciter Block Diagram Showin[g]
Logic for 3 PRF System

FR-DCFR CONTROLS

TRIGGERS FOR DTO, TRANSMITTER

D.O. RF SWITCH CONTROL LINES

(MODIFIED)
DIGITAL OSCILLATOR CONTROL

STEP PULSES FROM FIRG NEST

PULSE WIDTH CONTROL PULSE

PULSE WIDTH CONTROL

NEW LOGIC

NEW LOGIC

PRF-ZONE RESET CONTROL

ZERO TIME TRIG
11.52 MHz CLOCK
ZERO RANGE TRIG

*(MODIFIED)
RANGE COUNTER 20 BITS

COARSE RANGE WORD 20 BITS (TO DTO)

CALIBRATION CONTROL LOGIC

STOP DCFR
START DCFR

R PRF
FR PRF

CONTROL LINES FROM CALIBRATE SWITCHES

NOTE

SECTIONS OF EXISTING LOGIC WHICH HAVE BEEN MODIFIED ARE MARKED (MODIFIED)

AN ASTERISK DENOTES MAJOR MODIFICATION.

:k Diagram Showing Control and Timing

2

When changing the PRF in the second and third zone, the FR PRF must be changed before the DCFR PRF is changed. This is necessary to avoid loss of video returns and to synchronize the range gate with the shifted video returns in the new PRF.

The basic triggers supplied to other subsystems are not changed by the additional stage in the PRF counter or by the PRF controlled feedback in each counter.

The FR-DCFR control logic and the digital oscillator control have been modified to incorporate the three pulse widths. In the FR-DCFR control logic, a transmitter stop pulse must be generated for each of the three pulse widths. Additional gating was needed for the third pulse width. The digital oscillator control logic also terminates the FR at different times for the three pulse widths. New logic, pulse width control, is used to gate out these new pulses.

Two other new signals are also provided in this modification. They are the external radar sync pulse and the voltage waveform generator pre-trigger.

The final modification to be discussed is the range counter. The entire word is counted in the WBE and read in parallel to the DTO. The range counter is pre-set to a number depending on the PRF and zone. At zero time and upon a read request from the DTO, the 11.52 MHz pips are counted to the zero range trigger which represents the ambiguous range. The total number in the range counter then represents the true range.

For zone 1, the range counter is set to zero for all PRF's and the count is to the ambiguous range which is also the true range.

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For zone 2, the following numbers (each of which represents one PRF interval) are pre-set to the range counter.

PRF	No.
100	115,200
80.6	142,828
65.8	175,104

At zero time the ambiguous range is counted to give true range on the PRF following a Read Request, the pre-set number is read in, and the ambiguous range is counted. Therefore, true range is available on the PRF following the request.

For zone 3, the following numbers (each of which represents two PRF intervals) are pre-set into the range counter.

PRF	No.
100	230,400
80.6	385,656
65.8	350,208

The pre-set condition is determined by the PRF ZONE reset control logic. This new logic pre-sets the range counter on a PRF to PRF basis.

Storage of the range word is provided in the WBE and transformed to the DTO upon the read request signal. Line drivers are provided for angle tracker inputs and data timing will be similar to the present DTO.

The use of multiple PRF's required a change to the existing tapped delay line chassis.

Figure 5 is a block diagram of the proposed delay line configuration. As is shown a total of 23 taps are necessary to perform the functions for all
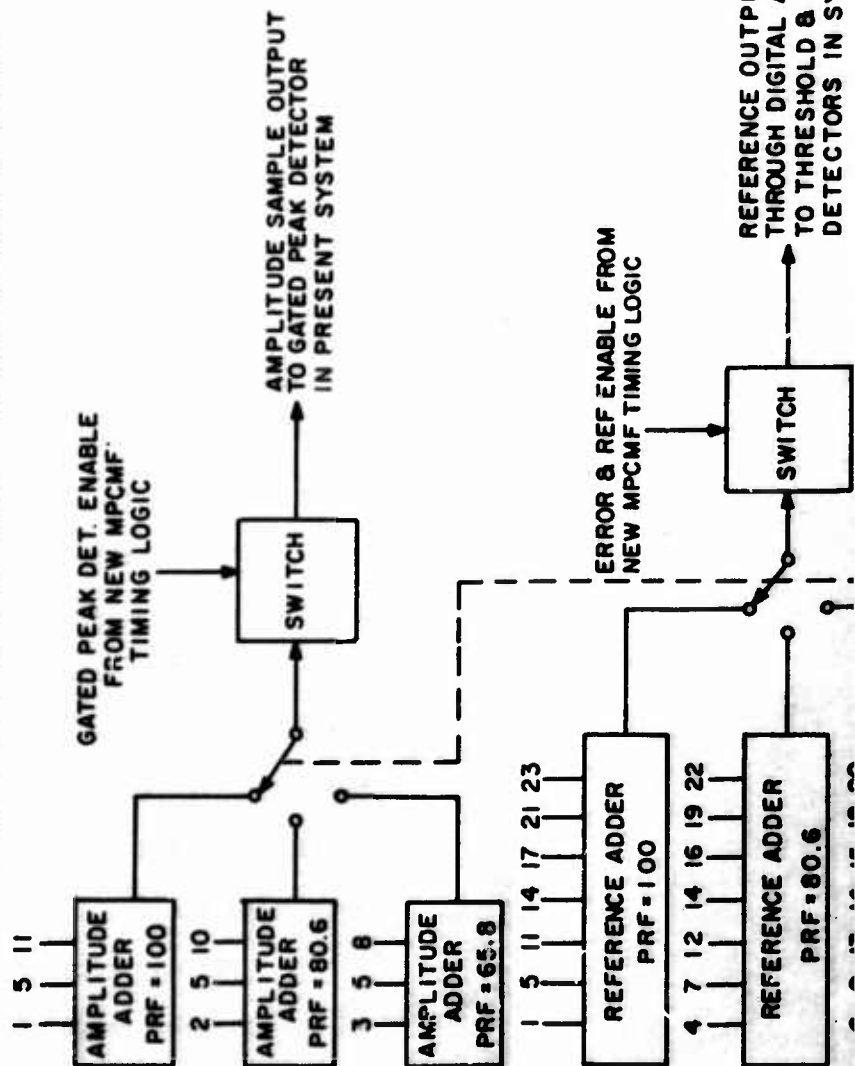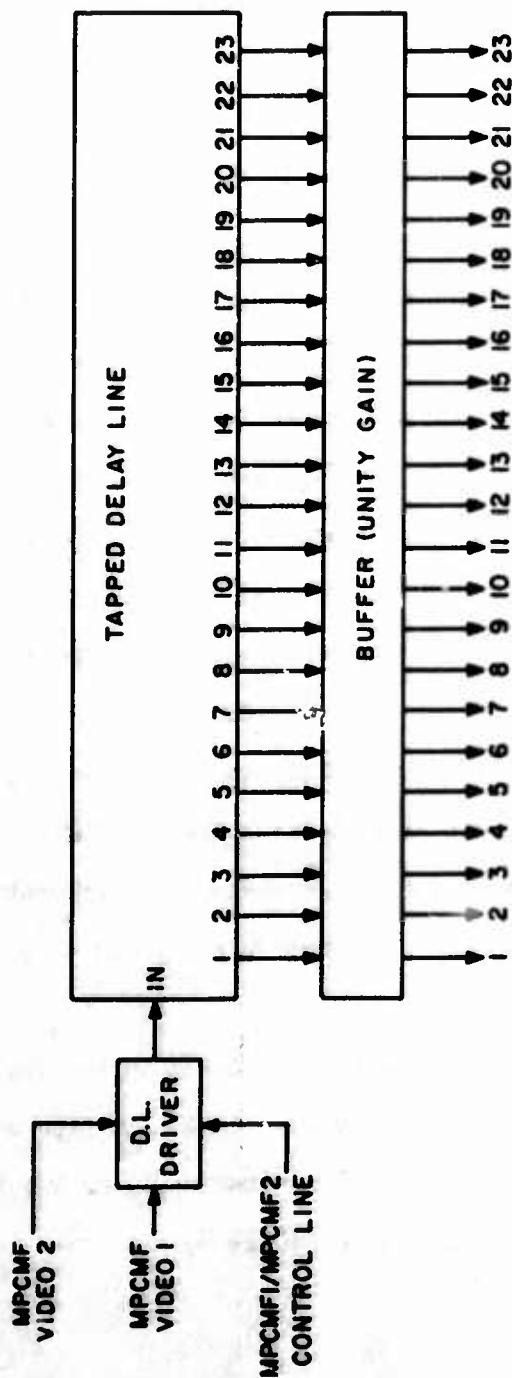
DELAY LINE TIMING	
TAP NO.	DELAY FROM INPUT
1	0
2	4.65
3	8.20
4	14.0
5	24.0
6	24.6
7	33.3
8	39.8
9	40.4
10	43.35
11	48.0
12	52.65
13	56.2
14	72.0
15	87.8
16	91.35
17	96.0
18	103.6
19	166.7
20	175.4
21	176.0
22	186.0
23	200.0
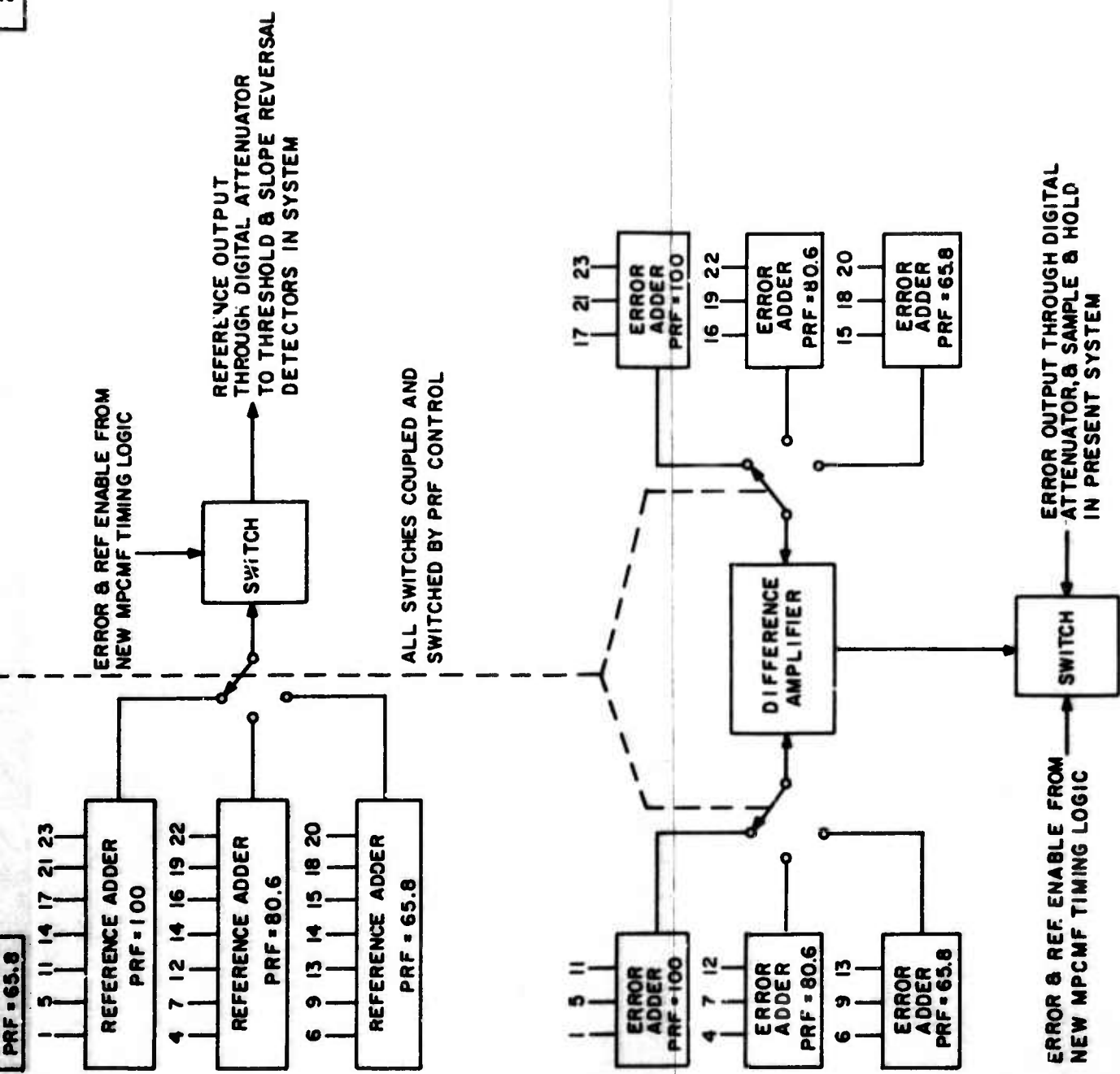
Fig 5 - New Tapped Delay Line Chassis

three PRF's. The three outputs from this chassis are identical in gain and dynamic range to the existing chassis.

The necessary gain and balance controls to assure proper gain and error balance in all three PRF's are provided to ensure proper track. loop performance and proper interface with existing equipment. Input switching of the MPCMF-1 and MPCMF-2 inputs is also provided. The selected video will be sent to the DTO for display.

The section of the chassis associated with SPCMF operations remains identical to that on the present chassis.

Minor modifications to the MPCMF timing logic were necessary in order to accommodate the multiple PRF's. These modifications consisted of changing the widths and positions of the gated peak detector enable and the multiple-pulse error and reference enable to the widths appropriate for each of the three individual PRF's. The appropriate width is chosen automatically by the PRF control lines so that in each PRF the gates will enable a frequency interval equal to the PRF and centered around the zero error position of the delay line output information. The delay line taps provided on the new tapped delay line chassis assure that the zero error position of the reference output occurs at the same position for all PRF's. As a result, the gated rundown, which is sampled to generate rate information, is utilized for all PRF's with the same rundown start and stop times as in the present system.

The PRF and zone selection and control logic is required as a result of the extended range of operation. The selection is made either by an operator using the console controls or automatically as the target range approaches an interference region (see Figure 6).

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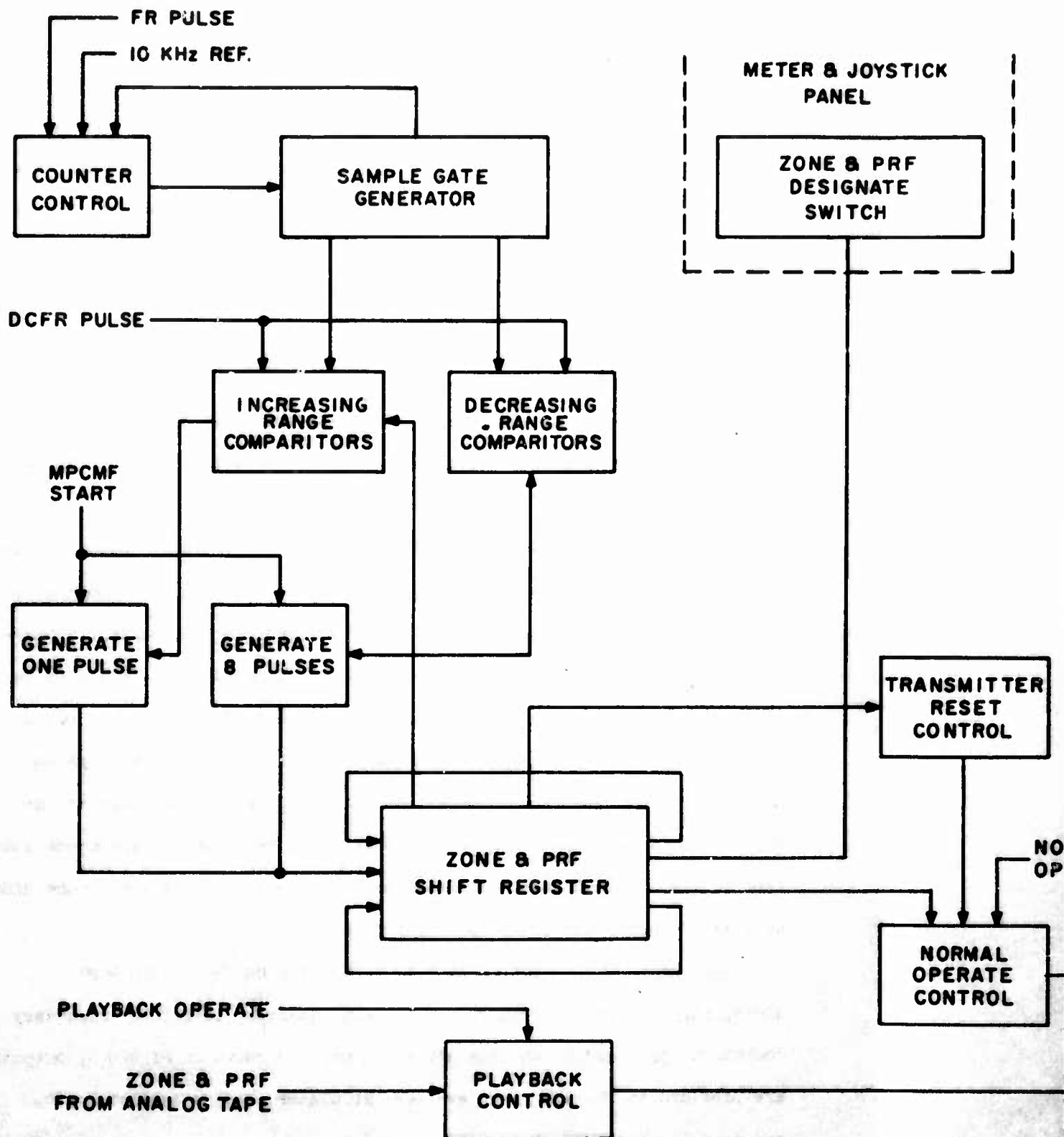
Fig 6 - Zone and PRF Selection and Control (All

OYSTICK

PRF
IATE
CH

ENCODE TO
6 LINES → LAMP
DRIVERS → TO
DISPLAY

ENCODE
TO
4 BITS → TO TIME WORD
STORAGE
REGISTER

TRANSMITTER
RESET
CONTROL

LINE
DRIVERS → TO WBE

→ TO MODE
SELECT LOGIC

NORMAL
OPERATE

NORMAL
OPERATE
CONTROL → NORMAL
OR
PLAYBACK → DESIGNATE
WBE → LINE
DRIVERS → TO
SIMULATOR

WBE
REQUEST

and Control (All New Equipment)

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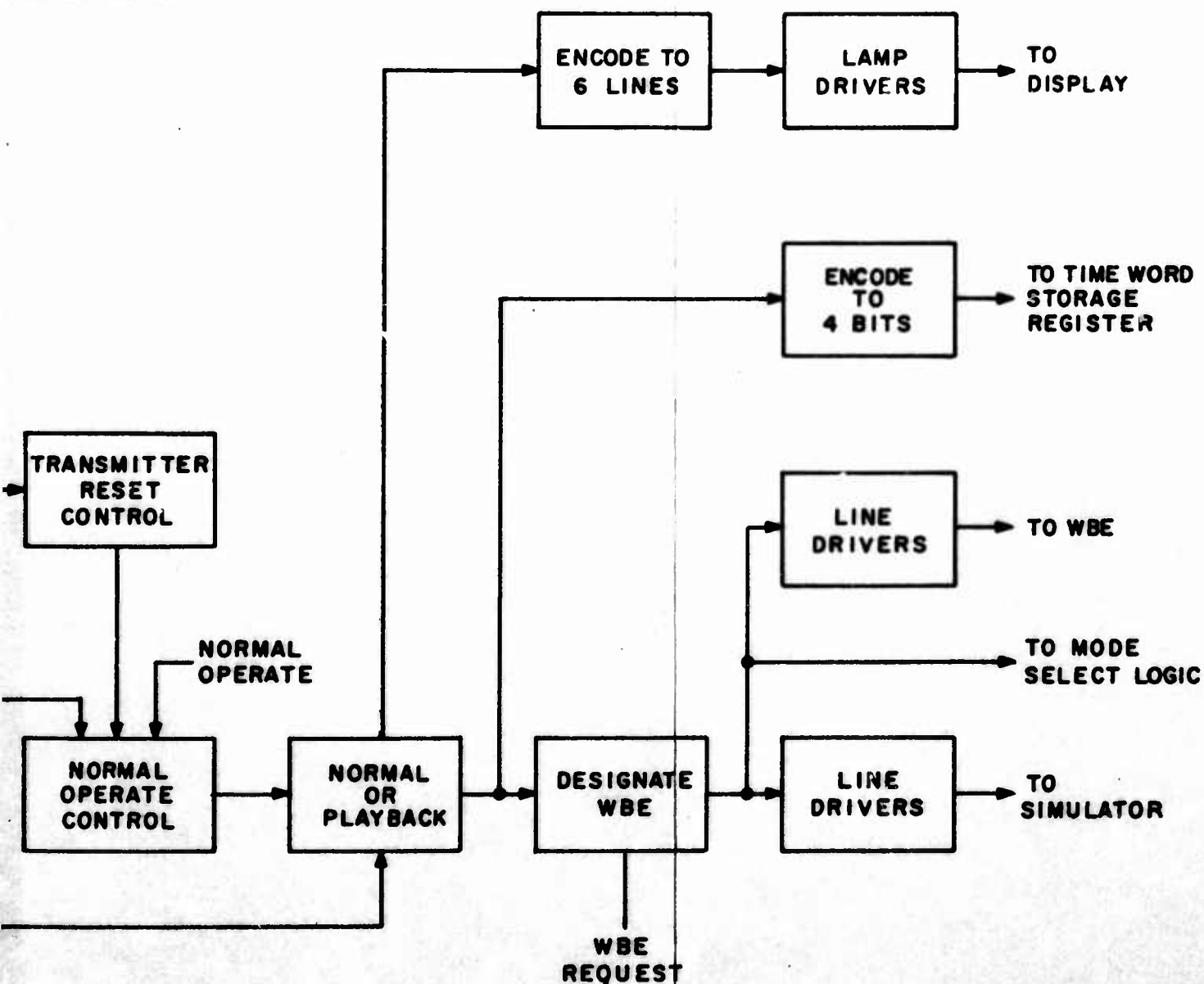
The initial selection of zone and PRF is made by the console operator by selection of the desired zone and PRF with the rotary selection switch on the meter and joystick panel. The operator selection is then set into the system at the end of an integration period. The zone and PRF information is held in a shift register and is gated out upon request from the time gate generator. Outputs are provided for console display. The purpose of storing the information in a shift register is to enable automatic switching of PRF's and zones while tracking a target to provide an optimum data rate. The sample gate generator is started by the FR pulse and continues counting 10 kHz timing pulses and generating interference detection gates until a DCFR pulse has been received. At this time a comparison is made to determine if an interference zone in a PRF has been detected. Two sets of comparators are used, one for increasing range and one for decreasing range; therefore, if a comparator output indicates increasing range and an approaching interference region, a pulse will be generated to step the zone and PRF shift register one position to the right. At the end of an integration period, the shift register output is sampled and the new zone and PRF information is indicated to the system. Likewise, if a comparison is made that indicates decreasing range and an approaching interference region, the shift register count is moved one position to the left. This is accomplished by connecting the PRF and zone counter as a ring counter and inserting eight pulses.

Zone and PRF information is also accepted from the analog tape during playback rather than from the shift register; therefore necessary control was provided to utilize either input. As shown in Figure 5, outputs are provided to the wide band exciter, simulator, mode selection logic, and console display.

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The PRF and zone information sent to the wide band exciter is used to reset the range counter to the minimum range setting in any indicated zone, thus permitting the readout of actual range and eliminating the need of converting the range word after it has heen sent to the DTO.

2. FINE LINE CORRECTION

One of the difficulties encountered in the original ASFIR system was the acquisition and lock-on to the center line of the fine line spectrum. With a spectrum spacing of 100 pps (or 24 microseconds in the time domain) and a gross amplitude envelope due to the 2.4-millisecond pulse, the presence of noise and a moving target made the selection of the center fine line difficult. An automatic means of determining this error and making the appropriate correction was developed. The technique utilizes the existing multiple pulse (MP) fine line range discriminator. This discriminator is a tapped delay line in which the tap spacing is determined by the PRF. Three taps on either side of the center fine line are algebraically summed to develop an error signal for range tracking. This discriminator is normally used for the range measurement (FM transmission); however, it can be used to generate an error detection signal for the CW mode (doppler). If the center fine line has been acquired in the CW mode, the gross spectrum will be symmetrical and the output of the discriminator will be zero. The discriminator will have an output (the actual output will be a staircase jumping in voltage according to the PRF in use) that can be used to enable the fine line correction signal. The logic has been established such that if five error indications out of the first eight integration periods occur, the correction is enabled. A correction is also enabled if there are 32 error indications out of 100 integration periods.

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The block diagram in Figure 7 shows the fine line correction system for range rate. Corrections for $\dot{\Theta}_1$ and $\dot{\Theta}_2$ are accomplished by duplication of the equipment in the dashed lines. The MP error signal from the range (or angle) discriminator is applied to two comparators. One comparator has a positive threshold word applied and the other has a negative threshold word applied. The threshold words are generated by threshold control logic which automatically switches thresholds according to the PRF in use. If the MP error signal exceeds either of the threshold settings, a pulse is applied through an "and" gate to the appropriate bit counter. The "and" gates are also conditioned by an inhibit signal from the DTO which can disable the system and by a mode signal which allows only threshold crossings which occur in the appropriate MP rate modes to be applied to the bit counters. The bit counters then accumulate bits until reset by the interval counter. The interval counter is arranged to generate a reset once each 100 occurrences of the appropriate rate mode. If 32 or more bits are accumulated in either bit counter between resets, the appropriate correction control unit is activated. The pulse former then applies a pulse to the correction control units. The appropriate correction control unit then generates a voltage step which will automatically step the appropriate rate VCO by an amount equal to the PRF in use. In the case of range rate, the range rate VCO step will cause an error in range (in hertz) equal to the PRF and the range loop will then pull in to the correct range value.

3. SINGLE PULSE (SP) INPUT TIMING SYNCHRONIZATION

The lack of synchronization between SPCMF output triggers and the 11.52 MHz clock in the SP timing logic causes a jitter of better than 86 ns (70 Hz) in the gates generated in the WBE and the video used in the tracking

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CORRECTION FOR $\dot{\theta}_{IMP}$ ACCOMPLISHED BY ADD THE UNITS ENCLOSED BY DASHED LINES.
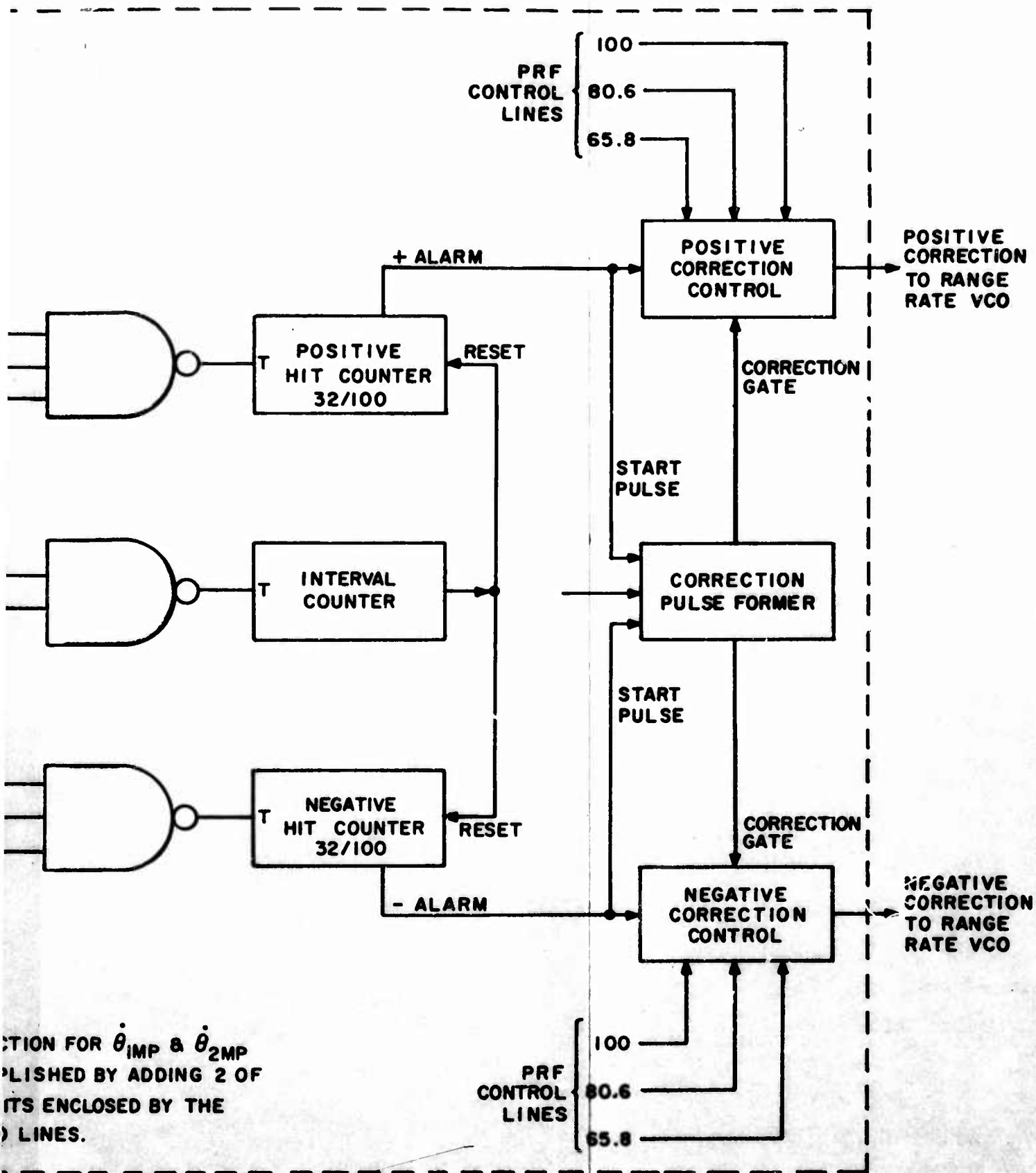
Fig 7 - Fine Line Correction

discriminator. This jitter causes difficulty in SP tracker alignment and errors in the SP tracker output. Figure 8 shows a synchronization unit that greatly reduced this jitter.

The 11.52 MHz clock used in the SP timing logic is applied to a tapped delay line. The delay line taps are then fed to a coincidence gate. The other inputs of the coincidence gates are fed by the SP counter start pulse (trigger 9) through a pulse shaper and an input gate. Upon the arrival of the SP start pulse, coincidence is observed between the start pulse and the delayed 11.52 MHz pips at one of the coincidence gate inputs. This gate output will set the appropriate flip-flop, and this flip-flop output is fed back to inhibit the input gate and prohibit further coincidence. The other side of the flip flop sends an enable through a delay slightly greater than the 11.52 MHz pulse width (approximately 20 ns) to the associated output gate. The enabled gate then sends the properly delayed 11.52 MHz pulse train to the SP timing logic with greatly reduced time jitter. Each output gate has, in addition to an enable input and a delayed pulse train input, an inhibit input from the adjacent flip flop. This inhibit prevents enabling of two adjacent gates on the same start pulse.

4. INCREASED FREQUENCY RESOLUTION

The rate (range, angle 1, angle 2) VCO outputs are available for counting for a period of 100 milliseconds. To increase the frequency resolution without increasing the counting period, each of these signals $(\dot{R}+\Delta f,$ $\dot{\theta}_1+\Delta f$ and $\dot{\theta}_2+\Delta f)$ were multiplied by five and then down converted by mixing with $4\dot{R}$ $(4\dot{\theta}_1$ or $4\dot{\theta}_2)$ to produce the signals $\dot{R}+5\Delta f,$ $\dot{\theta}_1+5\Delta f,$ and $\dot{\theta}_2+5\Delta f$ for counting.

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Fig 8 - Single Pulse Input

TAPPED DELAY LINE

30 40 50 60 70 80 ns

COINCIDENCE GATES

S

R S R S R S R S R S

FF FF FF FF FF FF

0 1

e f g h k

DL DL DL DL DL DL

OR GATE

11.52 MHz
TO SP
TIMING
COUNTER
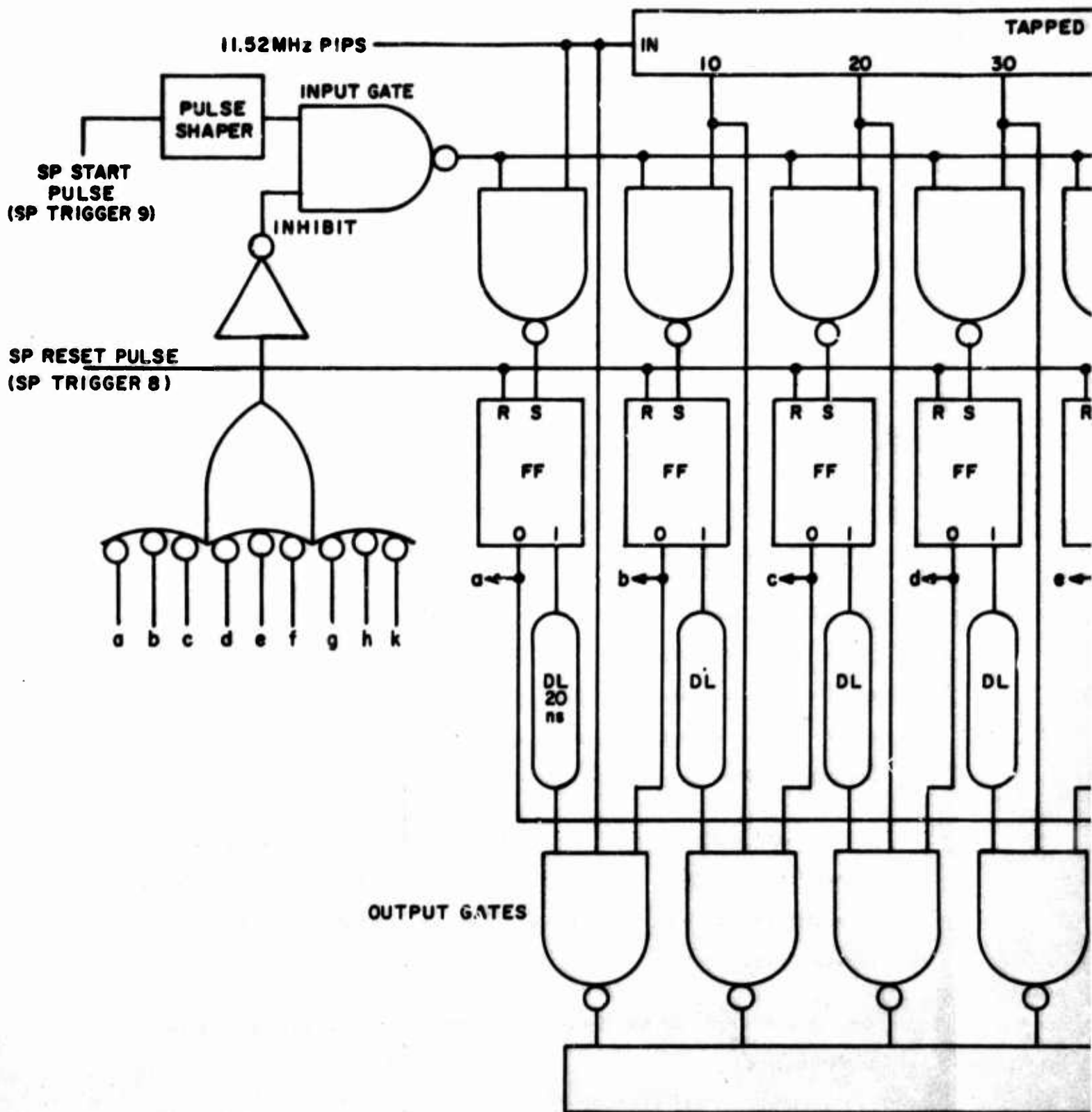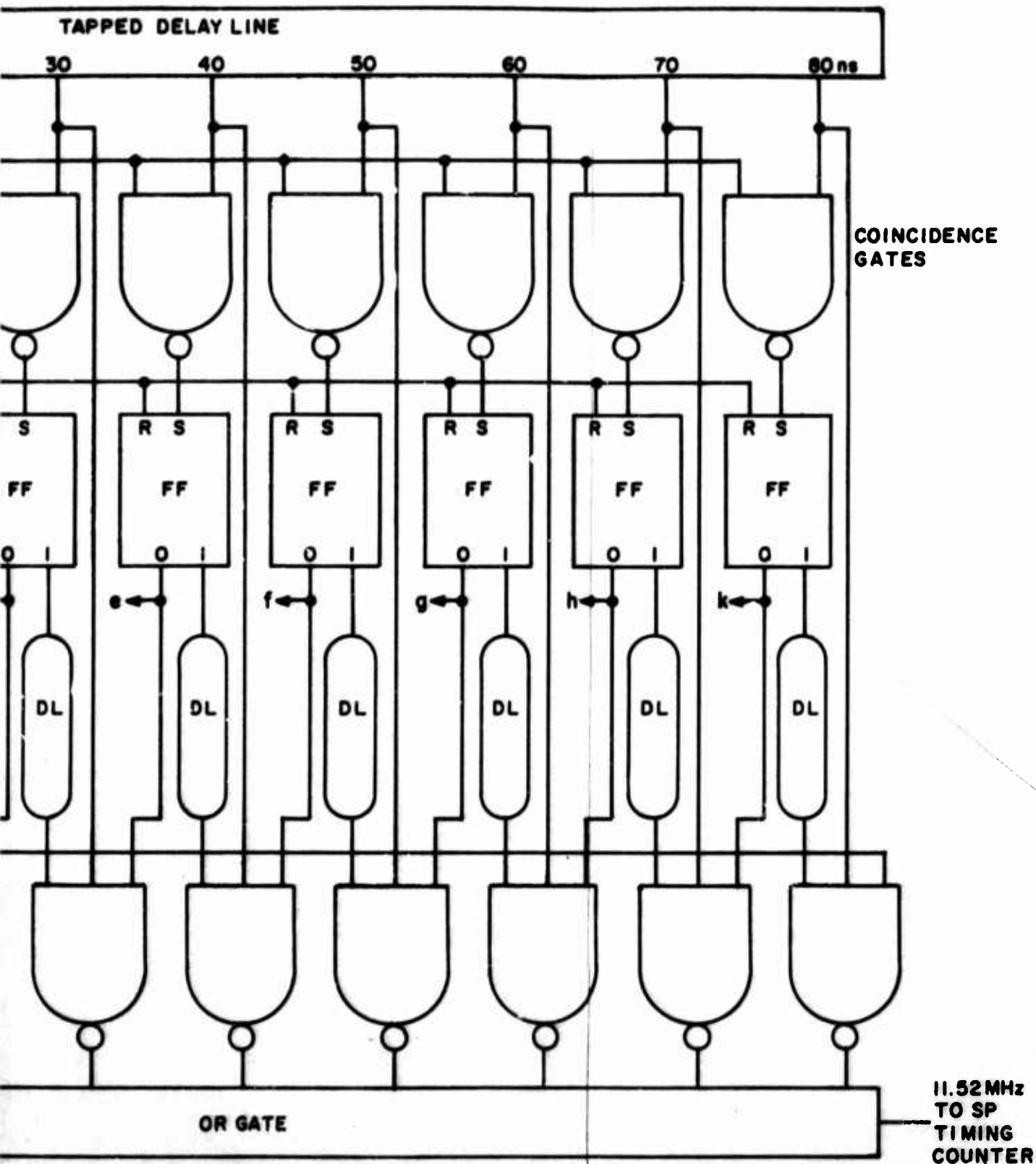
ie Pulse Input Timing Synchronization

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5. LOGIC REVISION

Much logic was modified but there are only a few areas that warrant any particular delineation and discussion.

In the original equipment two separate counters were used for the MP and SP tracking modes. This has been combined into a single function and a logic preference designed for the MP mode.

The mode control logic was also modified to permit the CW transmission waveform to be up-converted by mixing rather than by multiplying.

The track loop digital attenuator reset logic has been revised to minimize noise and transient effects prior to processing the target video.

6. TARGET SIMULATOR

The same technique employed in the DCFR counter to compensate for target doppler has been used to generate a simulated moving target. For 11.52 MHz, a stationary target is generated. For frequencies about 11.52 MHz, targets are generated at slightly different PRF's.

Three S-band outputs are provided with the appropriate frequency waveform imposed upon the S-band carrier. Three types of orbits have been approximated by analog voltage control of VCO's. These orbits are 100, 500 and 1000 nautical miles.

The basic assumptions and design of the analog forming voltage are shown in Appendix II.

For the monostatic mode, the target simulator's R VCO is imposed on the S-band output and the doppler frequency (f_d) is divided by 260 for use in the target generation counter (FR counter in WBE). In the bi-static mode, Θ_1 or $\dot{\Theta}_1$ will be exercised by the analog function generator driving the Θ_1 VCO while the Θ_2 VCO will be at a fixed frequency. To exercise Θ_2 and $\dot{\Theta}_2$, the analog function generator is switched to the Θ_2 mode.

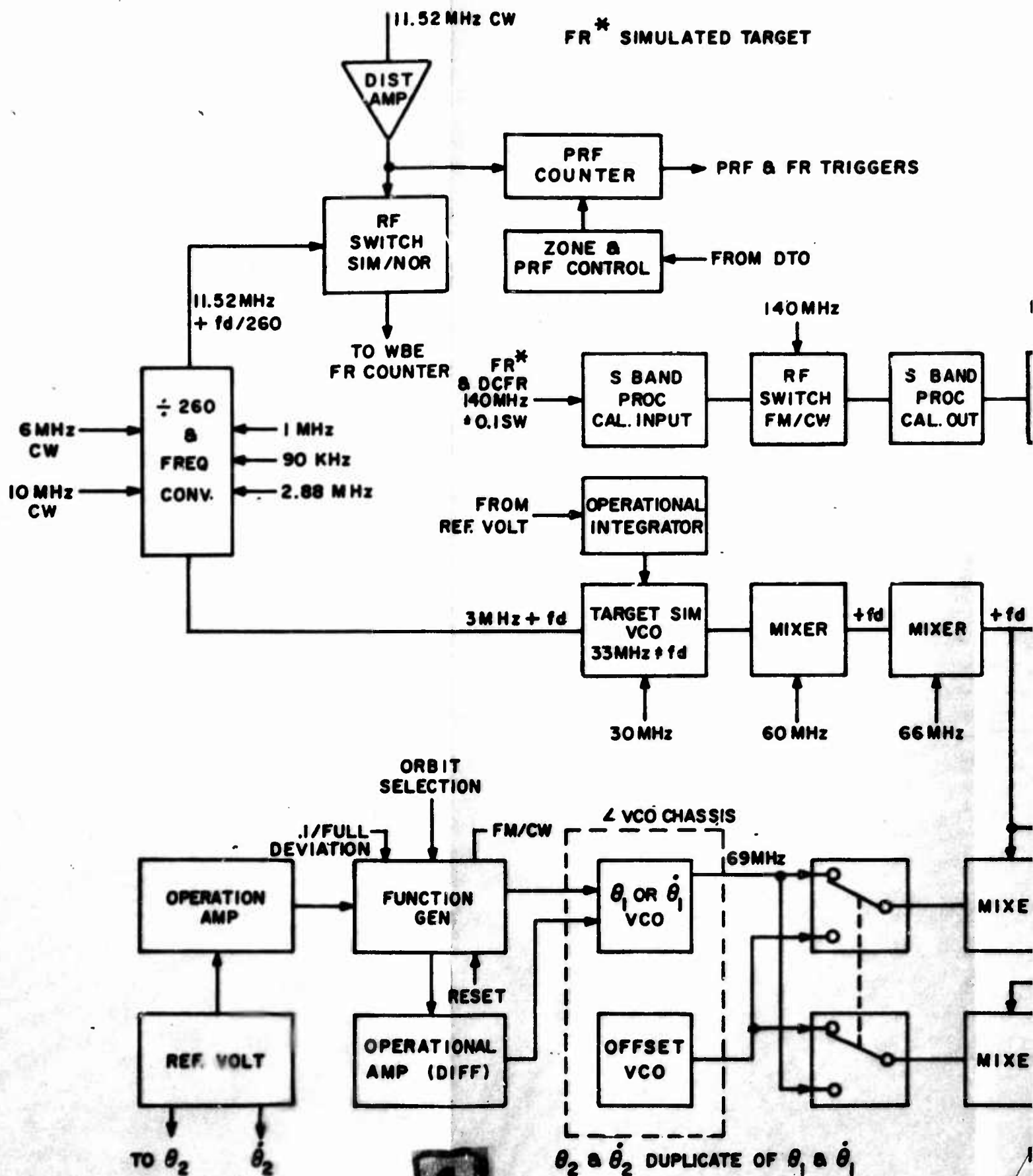The basic 140 MHz $\pm$.1 sweep is obtained by operating on a synthesized 11.52 MHz in place of the master oscillator derived 11.52 MHz. An RF switch is provided to select the normal/simulated modes. In the simulator mode, a PRF counter is provided to generate standard FR triggers. This counter is controlled for zone and PRF by the DTO. The 11.52 MHz for target simulation is derived by counting the converted 3 MHz $\pm$ f_d from the Target Simulator VCO and mixing this to 11.52 MHz. System operation for the target simulator is the same as in the normal WBE for FR generation, except that the target can move with respect to zero time. The 140 MHz $\pm$.1 sweep is gated for CW/FM operation and to eliminate the DCFR from the simulator output. The simulated target is delayed by 2450 μsec and converted back to 140 MHz. The processing from this point to the 3 GHz output is similar to the present S-band conversion equipment. A times-ten path and a times-one path are provided for wide band/narrow band operation. However, no provision was made for negative slope operation (Figure 9).

The control voltages for the VCO's are obtained by operational amplifier and simple diode voltage forming networks. The VCO's are similar to existing system VCO's.

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11.52 MHz CW

DIST AMP

PRF COUNTER → PRF & FR TRIGGERS

RF SWITCH SIM/NOR

ZONE & PRF CONTROL ← FROM DTO

11.52 MHz + fd/260

TO WBE FR COUNTER

FR* & DCFR 140 MHz + 0.1SW

140 MHz

S BAND PROC CAL. INPUT

RF SWITCH FM/CW

S BAND PROC CAL. OUT

6 MHz CW

10 MHz CW

÷ 260 & FREQ CONV.

1 MHz

90 KHz

2.88 MHz

FROM REF. VOLT

OPERATIONAL INTEGRATOR

3 MHz + fd

TARGET SIM VCO 33 MHz + fd

MIXER +fd MIXER +fd

30 MHz   60 MHz   66 MHz

ORBIT SELECTION

.1/FULL DEVIATION

FM/CW

∠ VCO CHASSIS

69 MHz

OPERATION AMP

FUNCTION GEN

θ₁ OR θ̇₁ VCO

MIXE

REF. VOLT

RESET

OPERATIONAL AMP (DIFF)

OFFSET VCO

MIXE

TO θ₂ θ̇₂

θ₂ & θ̇₂ DUPLICATE OF θ₁ & θ̇₁

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Fig 9 - Target Simulator Block Diagram

The target simulator provides an effective means of evaluating and calibrating the WBE and ASFIR system. All subsystems excluding the high power transmitter can be checked by use of this simulator.

7. ACQUISITION STUDY

As a corollary of the subject contract, a study of acquisition techniques were made. This study considered the acquisition process and the known problems to develop means for improving the system process.

Acquisition in $\dot{R}$ is relatively easy using the SPCMF; however, the transfer to the MPCMF was difficult because of the SPCMF/WBE jitter problem and the difficulty in selecting the desired center fine line. Several ideas were advanced and implemented into the modification kit. Two of these items have been discussed previously. They are the SP input logic synchronization and fine line correct. In addition, intensity modulation of the console display was implemented to aid the operator during lock on.

Single pulse operation was optimized by inserting a single pulse integrator to average all 16 target returns instead of one as in the original equipment. This area is treated in detail in Appendix I.

Joystick control speeds were adjusted using the target simulator for the desired granularity and response time.

8. SINGLE PULSE OFFSET PROCESSING

The capability to process, track, and display the rate parameters was aided by frequency multiplexing the return through the SPCMF. This was accomplished by developing two new frequencies: 66 MHz $\pm$ 150 kHz. These signals were used to offset the $\dot{\theta}_1$ and $\dot{\theta}_2$ frequency duration. This permitted the tracking of $\dot{\theta}_1$ at +150 kHz and $\dot{\theta}_2$ at -150 kHz while $\dot{R}$ was tracked at the SPCMF center frequency. Figure 10 shows this implementation.
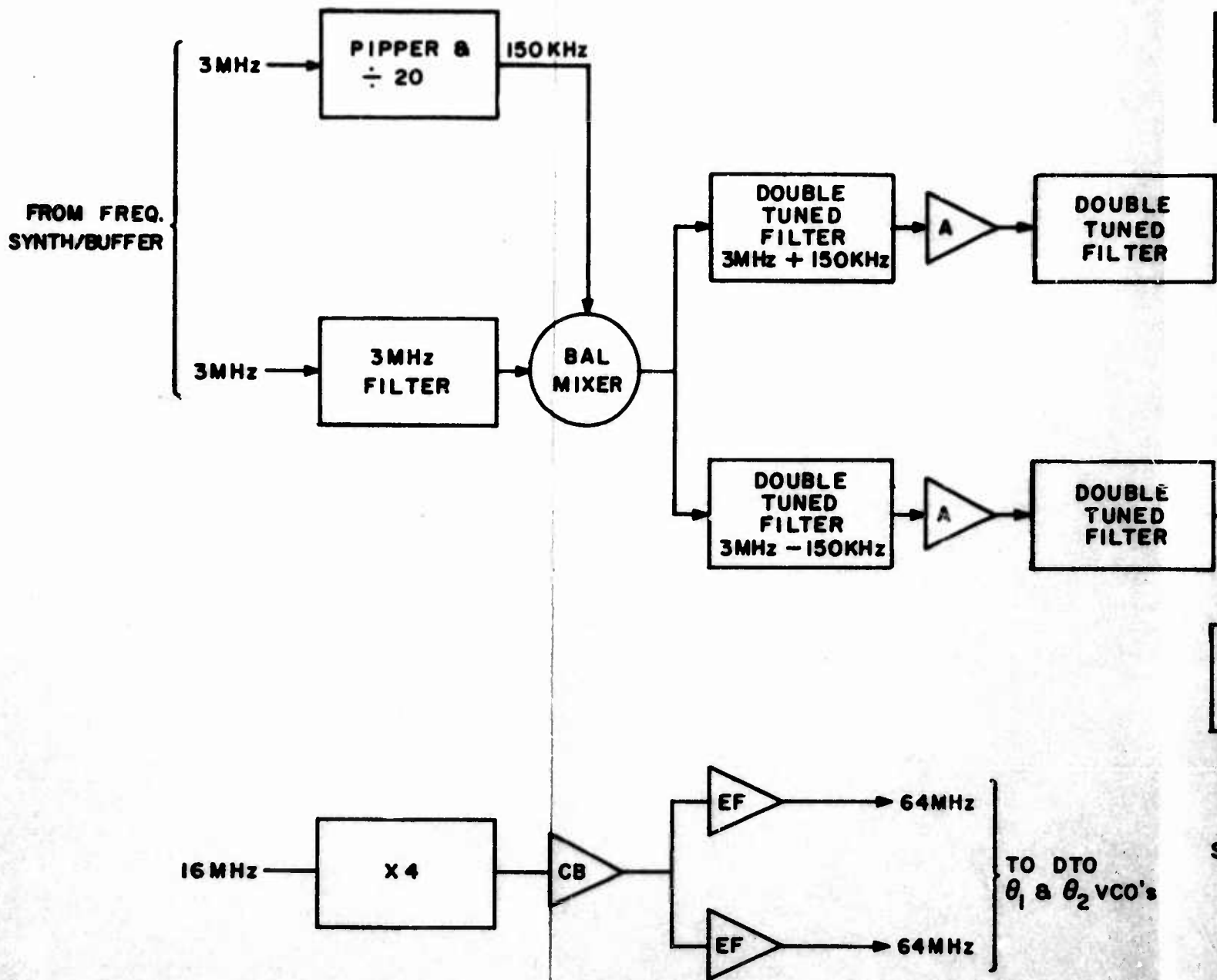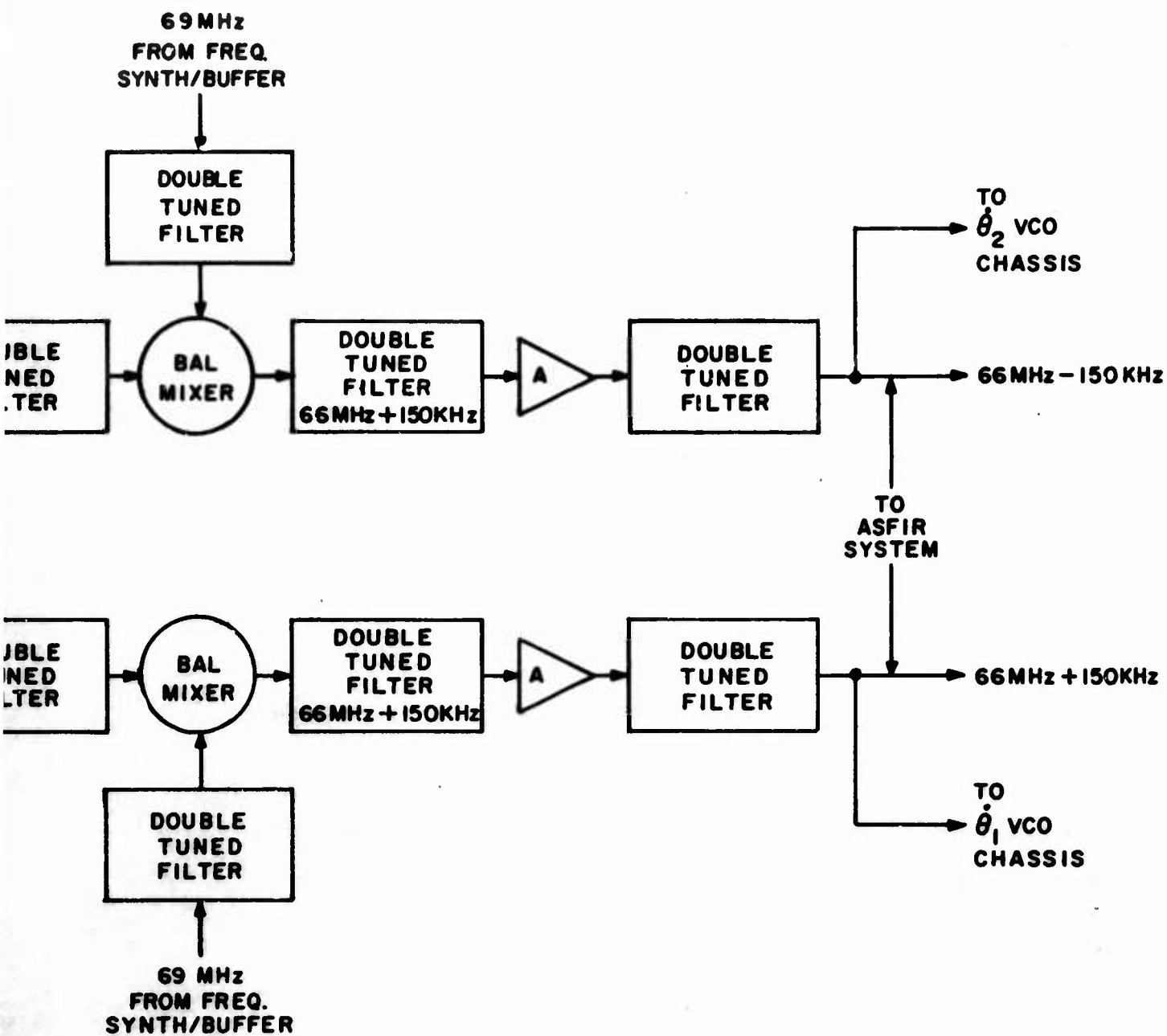
Fig 10 - SP Frequency Offset Processing

SECTION V

RESULTS

The nature of the effort performed on this contract precluded the gathering of detailed data and test results. Many of the modifications and additions were limited or restricted in their outward effect upon system performance. Other modifications were adjusted empirically by using the test target simulator. These changes were "documented" by observing performance and adjusting for the most desirable mode of operation. An example of this was the variation of the control console track loop VCO slew voltage controls.

In general, a large number of the changes were handled this way. However there are other areas where performance of an individual area could be monitored and data regarding that area gathered and recorded. All of the data and results obtained were a byproduct of running the Acceptance Test Plan and represented a mutual effort involving RADC and RCA personnel. It was found that the new target simulator represented a powerful tool in the interrogation of system problems and optimization of system performance parameters.

For consistency the results will be reported in the same order as the various changes were described in Section III, System Changes, and Section IV, System Additions.

1. RESULTS OF SYSTEM CHANGES

a. Angle and Angle Rate Trackers and Voltage Controlled Oscillator

Two tracking loops were added for θ_2 and $\dot{\theta}_2$. The tracking loop gain and $\dot{\theta}_2$ feed forward were adjusted for best performance. Four new VCOs were

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supplied. The Θ_2 VCO is centered at 69 MHz with a deviation of $\pm$ 4 MHz. The $\dot{\Theta}_2$ VCO is centered at 3 MHz and converted to 69 MHz with a deviation of $\pm$ 12 kHz. In addition, the Θ_1 and $\dot{\Theta}_1$ VCO's were replaced with units similar to the Θ_2 and $\dot{\Theta}_2$ VCO's. The center frequencies are identical but the deviations have been set to $\pm$ 2 MHz and $\pm$ 5 kHz for Θ_1 and $\dot{\Theta}_1$, respectively. Simulated targets in angle have been acquired and tracked by both tracking loops.

b. Delayed Coherent Frequency Ramp (DCFR) and CW Local Oscillator

The new 3072 DCFR channel was installed and interfaced with the existing RF subsystem. The overall system bandwidth of 100 MHz was achieved with a power output of 10 mW. Spurious signals, after a design modification, were better than 40 dB down.

The new system CW signals were provided at the desired 5 mW level.

c. Variable Phase Shifter

The new phase shift buffer units were integrated into the waveform generation equipment and used to perform the DO phase alignment.

d. Control Console

The modified control console was used during tracks of simulated and live targets.

e. Timing and Data Formatting

Evaluation of this area was confirmed by using the modified system to produce a sample data tape for examination by RADC.

f. Frequency Counter

This aspect of operation was verified using the target simulator.

2. RESULTS OF SYSTEM ADDITIONS

a. Unambiguous Range

This area was evaluated by the use of the target simulator and the data paper printer. The target was tracked through all zones and PRF's while the range data was observed to provide an unambiguous range read out.

b. Fine Line Correction

For this test, an open loop doppler tracking error was simulated and the frequency of the subject VCO monitored to ensure a proper frequency change.

c. Single Pulse Input Timing Synchronization

The measured jitter was found to be 25 ns or less for all PRF's. This represents an improvement of better than 3:1 in the reduction of system jitter.

d. Increased Frequency Resolution

The performance in this area was verified by signal substitution and the data paper printer.

e. Logic Revision

All logic, both modified and unmodified, were evaluated by performance on live and simulated targets.

f. Target Simulation

The 3000 MHz outputs were measured for power, bandwidth and spurious slope over the target simulator VCO frequency deviations.

The 3000 MHz outputs yielded power of from 25 to 8 mW with each having 40 dB (nominal) of available attenuation.

System bandwidth of 100 MHz with less than 0.5 dB ripple were achieved. The spurious output, after modification, was 38-40 dB down.

The VCO's were calibrated to provide the proper frequency deviation for each test mode: R, θ_1, θ_2, $\dot{\theta}_1$, and $\dot{\theta}_2$. Range was evaluated by observing that a smoothly moving test target was generated.

g. Acquisition Study

Results of this study are included in Subsection 8 of Section IV.

h. Single Pulse Offset Processing

The performance of this modification was evaluated using the target simulator and live targets.

SECTION VI

RECOMMENDATIONS

As would be anticipated from an experimental program undergoing test and evaluation, several design changes would improve the performance of the WBE/DTO. The recommendations can be considered as those particular to the WBE/DTO, and those primarily concerned with the ASFIR system. However, since the WBE/DTO is so uniquely related to the complete system, any change in system design will most likely result in some modifications to the WBE/DTO complex.

1. WBE/DTO

These recommendations are of a specific nature, usually concerning a single unit or chassis.

a. Range VCO

The Range VCO is presently mounted on a module. It is recommended that this unit be placed on a chassis and have an oven added to improve the long term stability.

b. Track Loop Noise Reduction

Presently the servo amplifiers and track loop functional operations are modularized and located in module nests. It is suggested that all six track loops be placed on chassis with their respective VCO. This would eliminate the nest wiring problems and should result in better operation.

c. Removal of Phase Locked Oscillator (PLO)

The DO uses active filters (PLO's) to eliminate undesired harmonics in the DO mixing for staircase generation. As a means of improving the short

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term phase stability the removal of the 16 presently used PLO's and the use of 16 crystal filters is recommended. This would improve the maintainability of the WBE and reduce the short term stability to passive rather than active elements.

d. Improved Broadband Mixers

Since the WBE was first built, the technology has advanced in the development of diodes and balanced transformers for use in the double balanced diode bridge modulators. There are several areas in the frequency region of 95 to 140 MHz where the new hot carrier diodes would provide improved performance. As an example, Hewlett Packard now has a balanced mixer module available that has extraordinary characteristics over this frequency region.

e. Calibration Mode Changes

There are three changes to the calibration subsystem that would improve performance. First, the gating function for the target simulation should be performed by a balanced diode switch (Sanders DS 11) instead of the existing (Sanders DS 201) single balanced switch to remove the gating pedestal. Second, the new target simulator should be modified to include a VCO for $\dot{\theta}$. This would increase the long term stability of the simulator $\dot{\theta}$ signal. This is important because of the use of rate feed forward in the tracking loops. Finally, a 3-MHz VCO capable of deviating at least ± 1500 Hz should be added. This oscillator would be used to calibrate the SPCMF and the WBE single pulse discriminator.

f.   Angle VCO Decreased Deviation

The specified angle VCO deviation for the second base line site was ±4 MHz with a center frequency of 69 MHz. However in actual use, only half this deviation is ever used unless the frequency slope of the transmitted waveform is changed from positive to negative. Since the system primarily operates in the positive mode, the deviation could be recentered to 71 MHz ± 2 MHz. This would yield at least a 2:1 increase in stability of the angle VCO.

2.   ASFIR SYSTEM

a.   SPCMF/WBE Timing Jitter

As mentioned previously, a significant reduction of system jitter was accomplished by the addition to the SP input logic. However, it was ascertained during system testing that perfect coherence could be obtained by using a clock derived from the SPCMF. Basically, this signal should be a multiple of 1/BW of the SPCMF and should be as close to the present WBE 11.52 MHz clock as possible to minimize logic changes. If this change were implemented, all SP/WBE jitter would be removed and this would facilitate SP acquisition and lock-on.

b.   Active Compensation of Phase and Amplitude Distortion

The present waveform generation equipment is capable of compensating for doppler and of being aligned in phase to accomplish an optimized correlated spectrum. Based upon receiving this idealized rectangular CW pulse, cosine squared exponential weighting is applied in the coherent memory filters to reduce the time side lobes. However, the effectiveness of this weighting is proportional to the system time bandwidth product and to any

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amplitude and/or phase perturbations experienced by the pulse before correlation.

For the ASFIR case, the time-bandwidth product is high enough for the first assumption to be true; however, no compensation has been considered for the amplitude and phase distortion experienced at wideband prior to correlation. The DCFR generation provides a possible method to introduce this phase compensation, but there apparently is no convenient place to insert the amplitude modulation except in the receiving channel. Further study would be required in this area prior to implementation to achieve the best overall result.

c. Receiver Automatic Gain Control (AGC)

To normalize changes in target amplitude due to target size and range variation, a slow AGC should be added to the receiver. The present WBE amplitude word could be used with a digital comparator to derive the AGC servo signal. The gain controlled unit could then either be the 69 MHz IF amplifier or a voltage variable attenuator in series with the IF amplifier. This would be most beneficial in the angle channels, where an additional amplitude variation is encountered because of slave site pointing errors. Timing of the amplitude samples and gain settings would be made synchronous with the present mode logic (integration period basis) to prevent gain changes during any given mode.

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APPENDIX I

TRACKING LOOP DESIGN FOR ASFIR THIRD SITE

The following assumptions were used in the design of the ASFIR tracking loops:

1. Doppler and angle rate measurements will always be made on the CW pulses.

2. Range and angle will be measured on the FM pulses.

3. At least three out of six CW pulses will be equally spaced.

4. Range will not be measured in 1/10 ramp while angles are measured in full ramp.

5. Range must operate in full ramp while angles are in 1/10 ramp.

6. At least two out of six pulses will be reasonably spaced for range measurements.

Based on the foregoing assumptions, the number of data measurements for each parameter for the various conditions will be as shown below:

Parameter	Range in 1/10 ramp	Range in full ramp
Range	3	2 or 3
Doppler	3	3
Angle #1	3	1 or 3
Angle #2	3	1 or 3
Angle rate #1	3	3
Angle rate #2	3	3

Based on the foregoing tabulation, the design PRF for each parameter will be as shown below:

Parameter	Design PRF
Range	3 in 1/10 ramp, 2+ in full ramp
Doppler	3
Angle	1 or 3 switchable in full ramp, 3 in 1/10 ramp
Angle rate	3

It is necessary to have a second order tracking loop to.keep the target dynamic errors to a minimum. It is assumed that dynamic errors are larger than thermal noise errors so that the track loop bandwidths should be as wide as possible consistent with good stability.

1. MULTIPLE PULSE COHERENT MEMORY FILTER (MPCMF) OPERATION.

In the MPCMF mode, the parameter errors are measured at the above PRF rates and then sampled and held until the next error measurement. A sample and hold circuit is a zero order hold circuit and it has a transfer function of:

$$G_H(S) = \frac{1 - e^{-S/PRF}}{S} = \left| \frac{\sin \frac{\omega}{2 \; PRF}}{\frac{\omega}{2 \; PRF}} \right| \; \angle -\frac{\omega}{2 \; PRF}$$

If the PRF varies, even only slightly, its average value should be used in the transfer function. $G_H(S)$ for a PRF of 1, 2 and 3 are shown in Figure 11. A second order track loop will have an open loop transfer function, $G_T(S)$, given by (exclusive of the hold circuit):
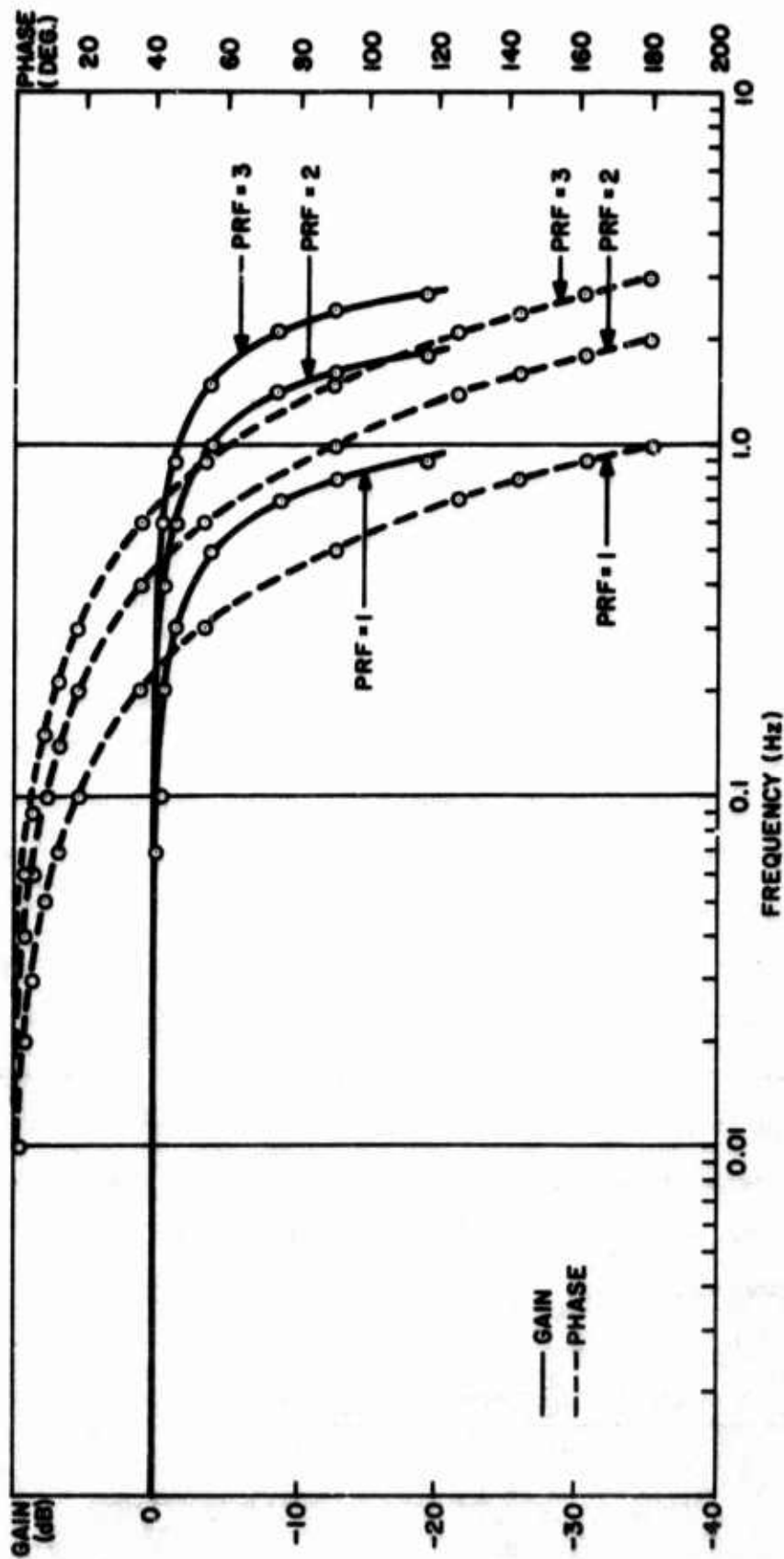
$$G_T(S) = \frac{K_a \; (S/\omega_a + 1)}{S^2}$$

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Fig 11 - Gain and Phase Characteristics of a Zero Order Hold Circuit for Various PRF Values

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For good stability, a rule of thumb value of ω_a should be:

$$\omega_a \approx \frac{\omega_{co}}{\sqrt{10}}$$

and

$$K_a = \frac{\omega_{co}^2}{\sqrt{10}}$$

Where ω_{co} is the open loop gain crossover (gain = 0 dB) frequency of the tracking loop.

Therefore:

$$G_T(s) = \frac{\omega_{co}^2}{\sqrt{10}} \quad \frac{\left(\frac{s \sqrt{10}}{\omega_{co}} + 1\right)}{s^2}$$

$G_T(s)$ is plotted in normalized form in Figure 12. For good closed loop response, a servo should have a phase margin (amount the open loop phase is above -180° when gain = 0 dB) of 30° or above and a gain margin (amount the gain is below 0 dB when the open loop phase is -180°) of 6 dB or above. From Figures 12 and 13. the maximum value of f_{co} that can be realized and still meet the gain and phase margin criteria is about 0.2 PRF. For this value of f_{co}, the gain margin is 11 dB and the phase margin is 40°, both of which are close enough to the desired values. Figure 12 shows the open loop and closed loop characteristics for a servo loop with an open loop crossover of 0.2 PRF. Therefore, the various servo loops should be implemented to the following transfer function:

$$G_T(s) = \frac{0.525(PRF)^2 \quad \frac{2.56}{PRF(s+1)} \quad (1 - e^{-s/PRF})}{s^3}$$
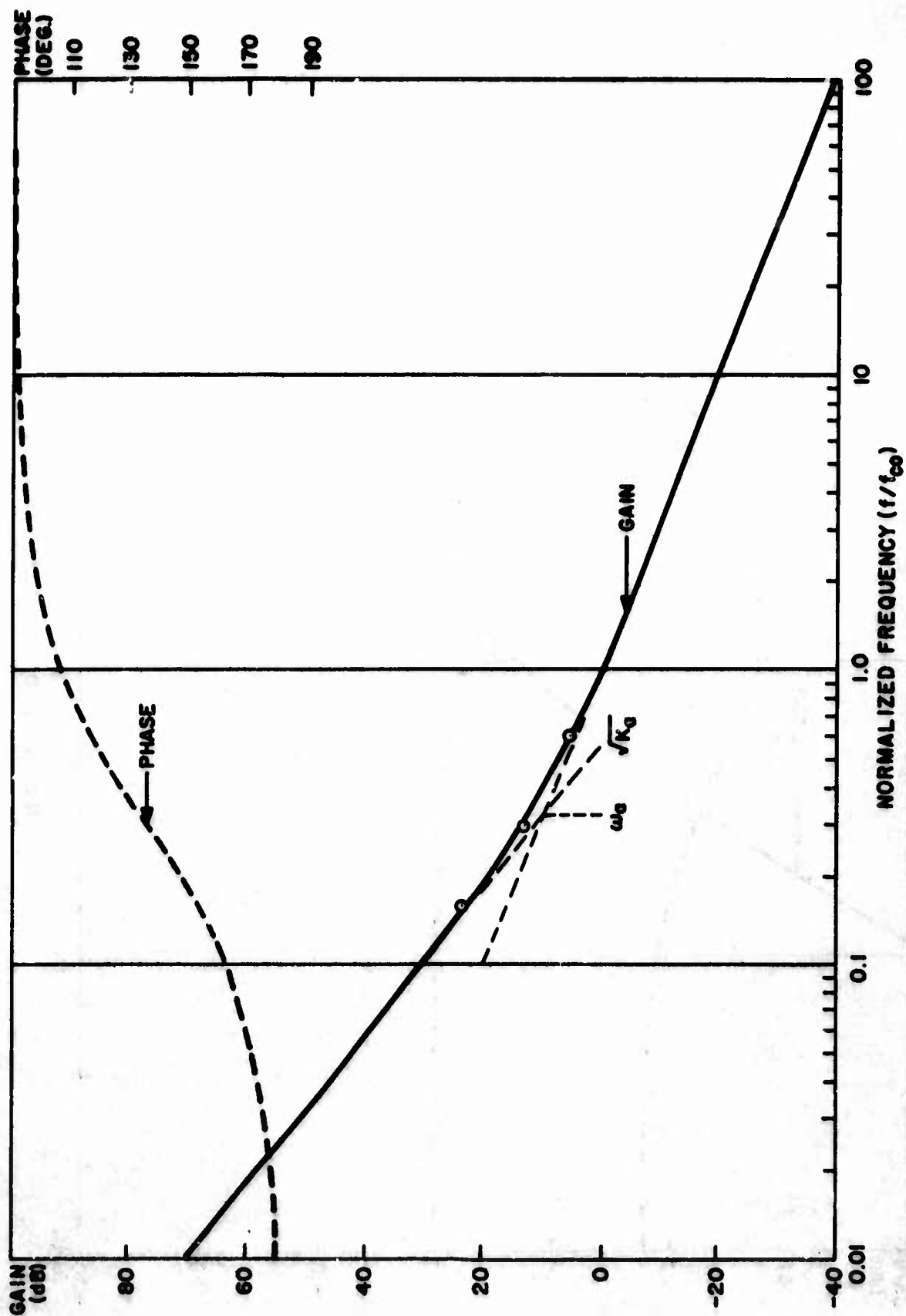
38

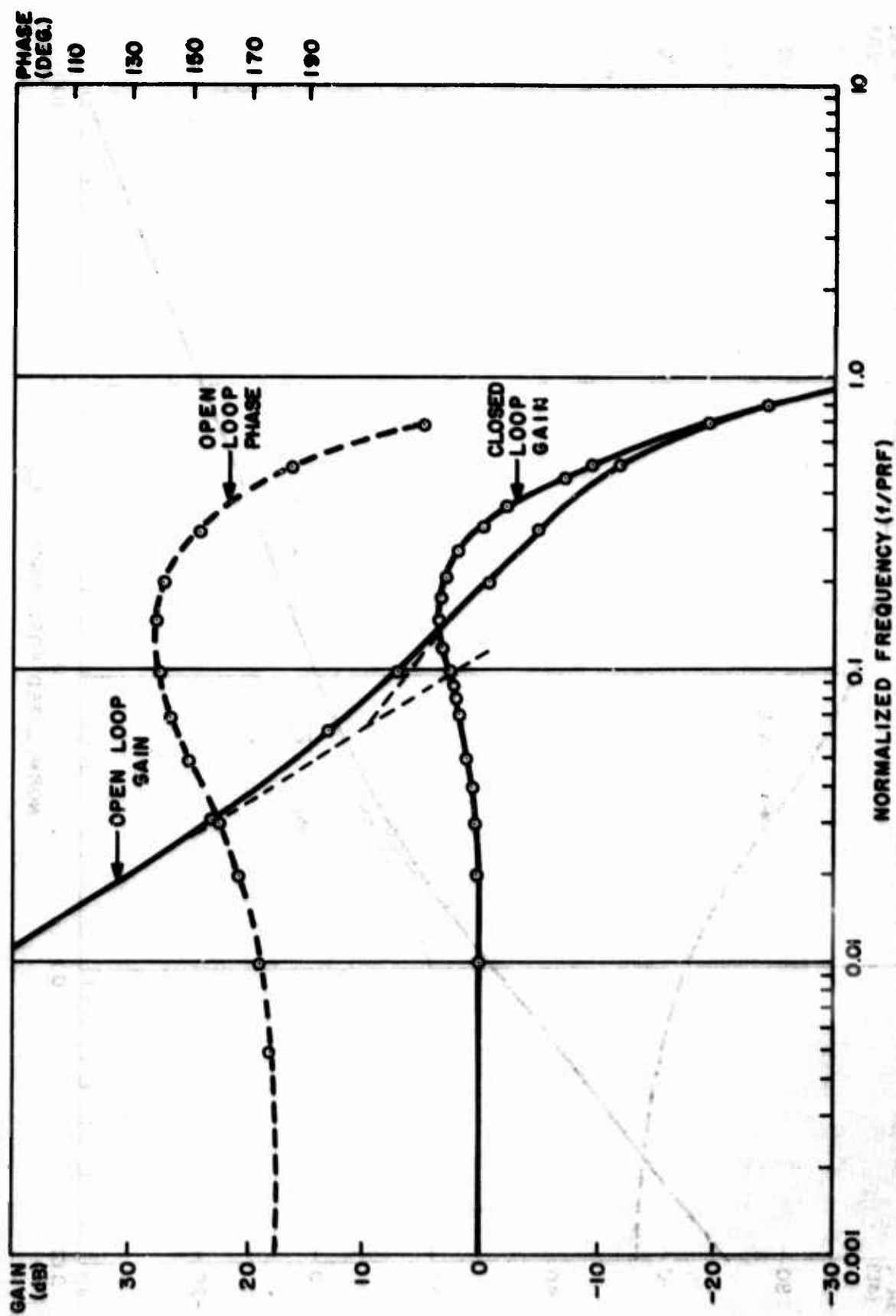Fig 12 - Second Order Track Loop Transfer Function

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Fig 13 – Characteristics of a Second Order, Sampled Data Servo with
Open Loop Crossover Equal to 0.2 Sampling Frequency

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Exclusive of the sample and hold circuit, the transfer function should be:

$$G'_T(S) = \frac{0.525(PRF)^2 \left[\frac{2.56(S+1)}{PRF}\right]}{S^2}$$

PRF = 1:

$$G'_T(S) = \frac{0.525\left(\frac{S}{0.391} + 1\right)}{S^2}$$

PRF = 2:

$$G'_T(S) = \frac{2.10\left(\frac{S}{0.782} + 1\right)}{S^2}$$

PRF = 3:

$$G'_T(S) = \frac{4.725\left(\frac{S}{1.17} + 1\right)}{S^2}$$

2. SINGLE PULSE COHERENT MEMORY FILTER (SPCMF) OPERATION

In the SPCMF mode, a burst of pulses is transmitted for measurement of the corresponding coordinate and a single-return error estimate is made on each return. The number of pulse bursts is the same as for the MPCMF mode. It is desired to use the average error over the burst for tracking purposes. There are three methods that could be used to implement this averaging process:

1. Smooth the output of the single hit error estimator, convert this average error to digital at the end of the burst, and hold this digital number in the corresponding D/A converter of the servo.

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2. In each servo, feed the single hit errors out of the D/A converter into an integrating amplifier, reset the D/A at the end of the pulse burst, and use the integrator output as the servo amplifier input between pulse bursts.

3. Widen the servo bandwidth during the pulse burst, allow the servo to settle to a new velocity, and switch to coast between pulse bursts.

The third technique reduces the servo to essentially a first order track loop and increases the influence of the pulses near the end of the burst. Another disadvantage of the third technique is the difficulty in analyzing the track loop set-up required for this type of operation.

The first and second techniques give about the same servo performance. The second technique requires correction for the error buildup during the integration period. The first technique could be implemented with three averaging circuits while the second approach requires six circuits. From an overall system point of view, the first approach would be the best but it will be the hardest to implement. The configuration in Figure 14 is suggested for the SPCMF operation.

The EG/LG inputs to the SPCMF error detector are reversed to compensate for the integrator inversion of the averaging circuit. The integrator output increases linearly during the pulse burst and an appropriate gain increase must be made in the loop gain. This gain increase varies from 12/11 (PRF = 1) to 4/3 (PRF = 3). It is suggested that the gain be set at 1.2 for all PRF values as this matches the required gain values within $\pm$ 1 dB. The integrator must be dunked at the beginning of the pulse burst. This dunk pulse should be
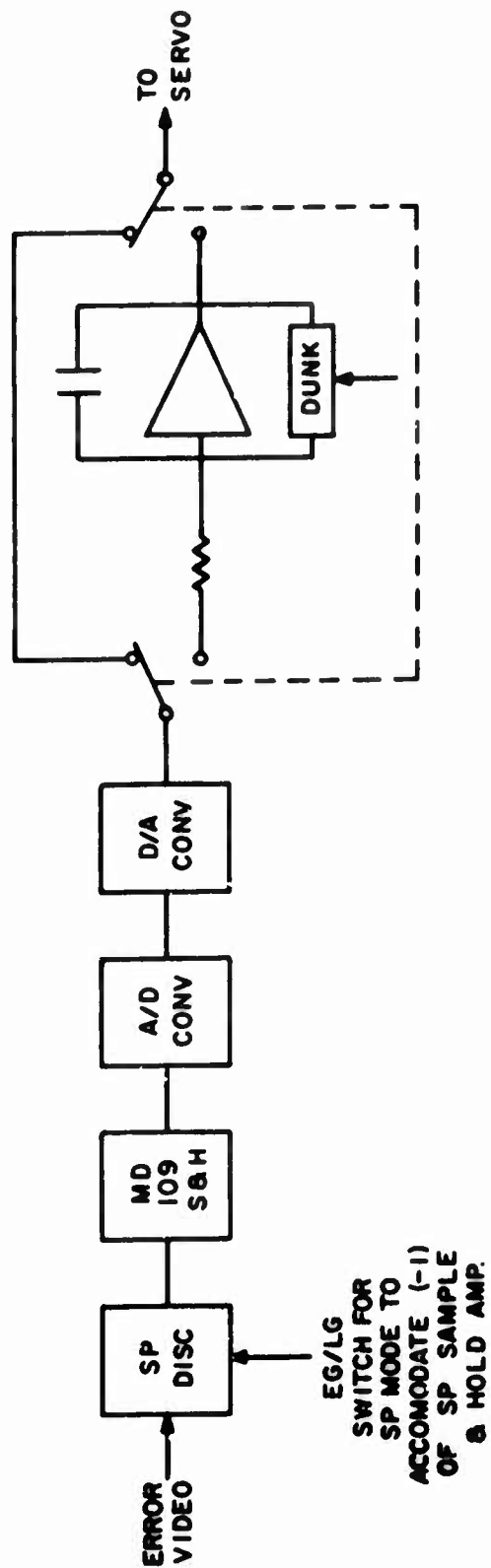
42

Fig 14 - Suggested Configuration for SPCMF Operation

less than 5 ms in duration. At the end of the pulse burst, the integrator input must be switched to the designated position or the D/A converter must be reset to zero output. Taking into account the 1.2 to 1 gain increase, the RC time constant of the integrator should be 0.14 seconds. Assuming a 1K dunk impedance, the value of C must be less than $1 \mu F$. Therefore R should be either 133K or 147K with C = $1 \mu F$; 133K is used for all parameters except angle and 147K is used for angle. The rest of the servo amplifier will remain unchanged.

APPENDIX II

TARGET SIMULATOR ORBITAL CALCULATIONS

The following simple model was used to develop the orbital trajectories used in the target simulator. The results were used to design analog waveforms that were used to deviate voltage controlled oscillators.

The three-site configuration is shown in Figure 15 with an orbital path halfway between Slave Site 2 and the Master Site ($R_1 = R_2$ for all points on the proposed orbital path).

The function R_1 (range from target to the Master Site) can be approximated by the following equation:

$$R_1 = R_o - R_a \cos \omega t$$

then

$$\dot{R}_1 = R_a \omega \sin \omega t \text{ which yields the target doppler } f_d$$

$$f_d = \frac{2f_T}{C} (R_a \omega \sin \omega t)$$

where

f_T = Transmitter frequency: 3×10^9 Hz

C = Speed of light: 3×10^8 m/s

The method of implementation for the target simulator (Figure 16) introduces the simulated range rate movement at 11.52 MHz. The $\dot{R}$ VCO is centered at 33 MHz with a total deviation of 150 kHz which represents the maximum doppler for 200-nmi circular orbit satellites for a transmitted frequency of 3 GHz. This means that the deviation at 11.52 MHz must be

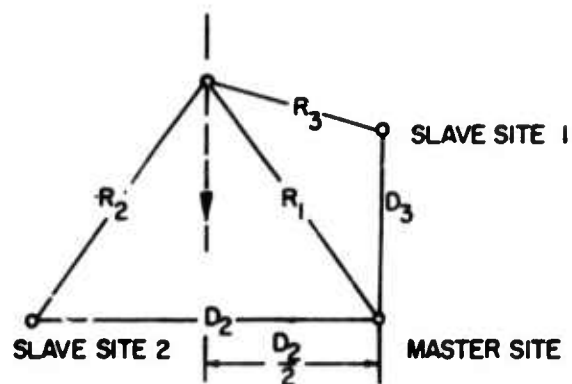$$\frac{11.52 \times 10^6}{3 \times 10^9} \times 150 \text{ kHz}$$
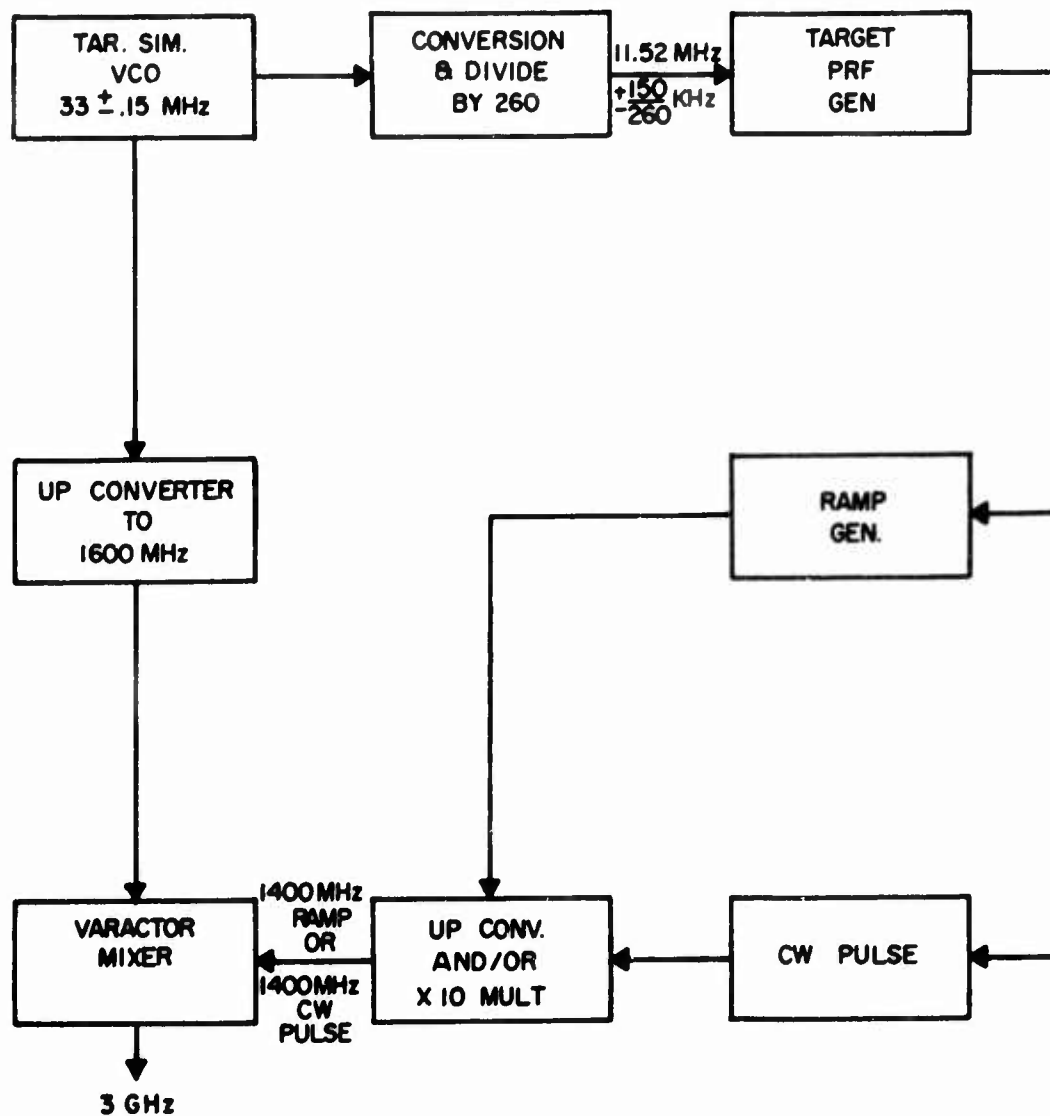
45

Fig 15 - Three Site Configuration

Fig 16 - Target Simulation Block Diagram

This deviation has been approximated to an acceptable degree of accuracy by dividing 150 kHz by 260.

The target PRF generator is a high speed counter that yields a train of constant frequency pulses for an input of 11.52 MHz and yields pulse trains of varying frequency for input frequencies about 11.52 MHz.

Graphs of range versus time (Figure 17) and range rate versus time (Figure 18) have been made for circular orbits with altitudes of 100, 500, and 1000 nautical miles. Figure 18 also shows the sine wave approximation used in the analog function generator for the Target Simulator $\dot{R}$ VCO.

Since the system has two slave sites the appropriate frequency modulations must be developed for the other two simulator outputs.

For the path selected, that is perpendicular to a line D_2 between the Master Site (MS) and the Slave Site 2 (SS2) and half way between the MS and SS2, the range difference between the MS and SS2 is given by

$$T_{\theta_{12}} = \frac{1}{C} (R_2 + D_2 - R_1)$$

and the frequency

$$f_{\theta_{12}} = T_{\theta_{12}} \alpha \quad \text{where } \alpha = \text{ramp slope in Hz/s}$$

for this path $R_2 = R_1$

$$f_{\theta_{12}} = \frac{D_2 \alpha}{C}$$

For the other orbital path supplied by the target simulator halfway between the MS and SS1, the same deviation holds and the expression for $f_{\theta_{1n}}$ becomes

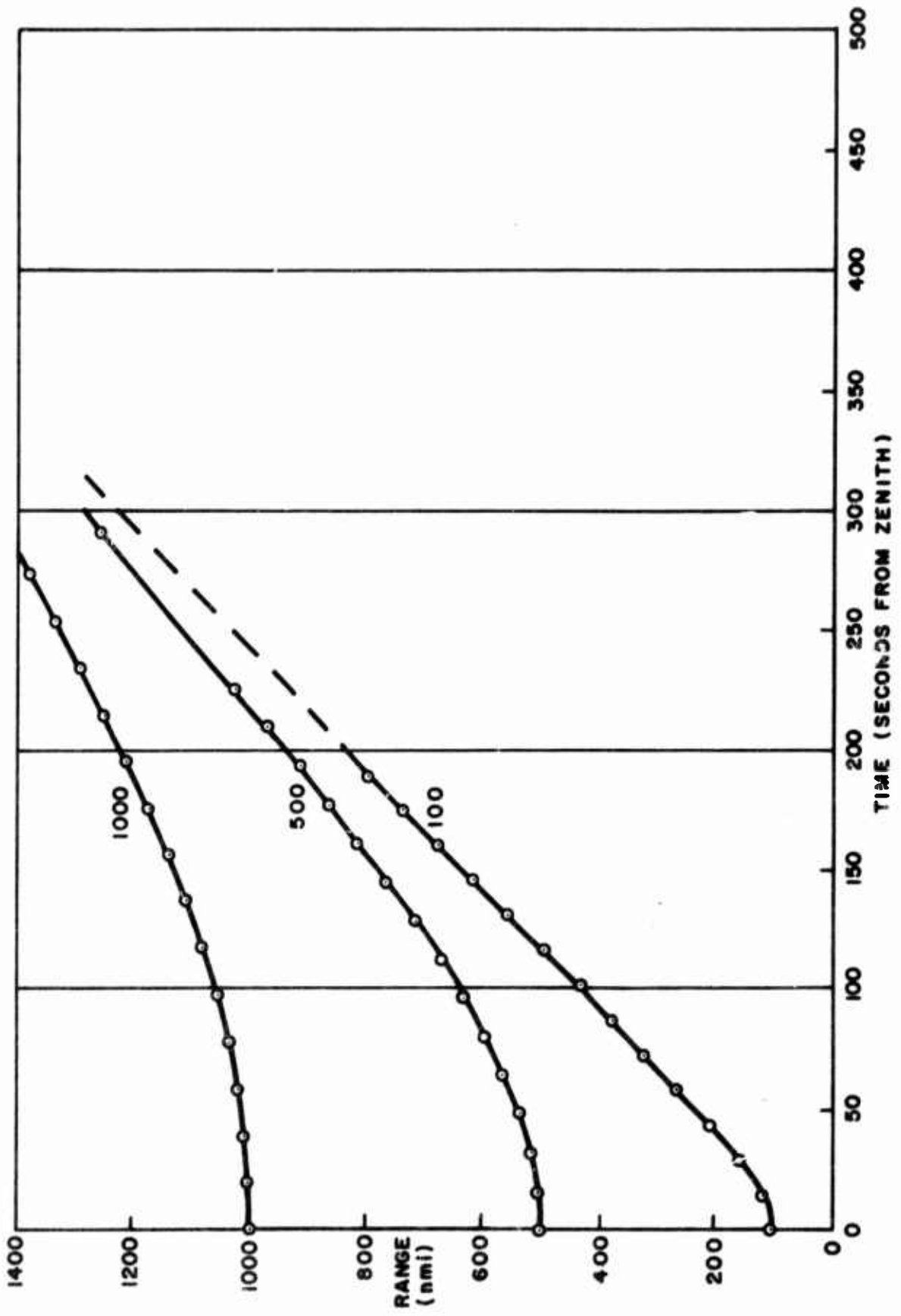$$f_{\theta_{1n}} = \frac{D_n \alpha}{C}$$

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Fig 17 - Range vs Time for Overhead Passes of Circular Orbits
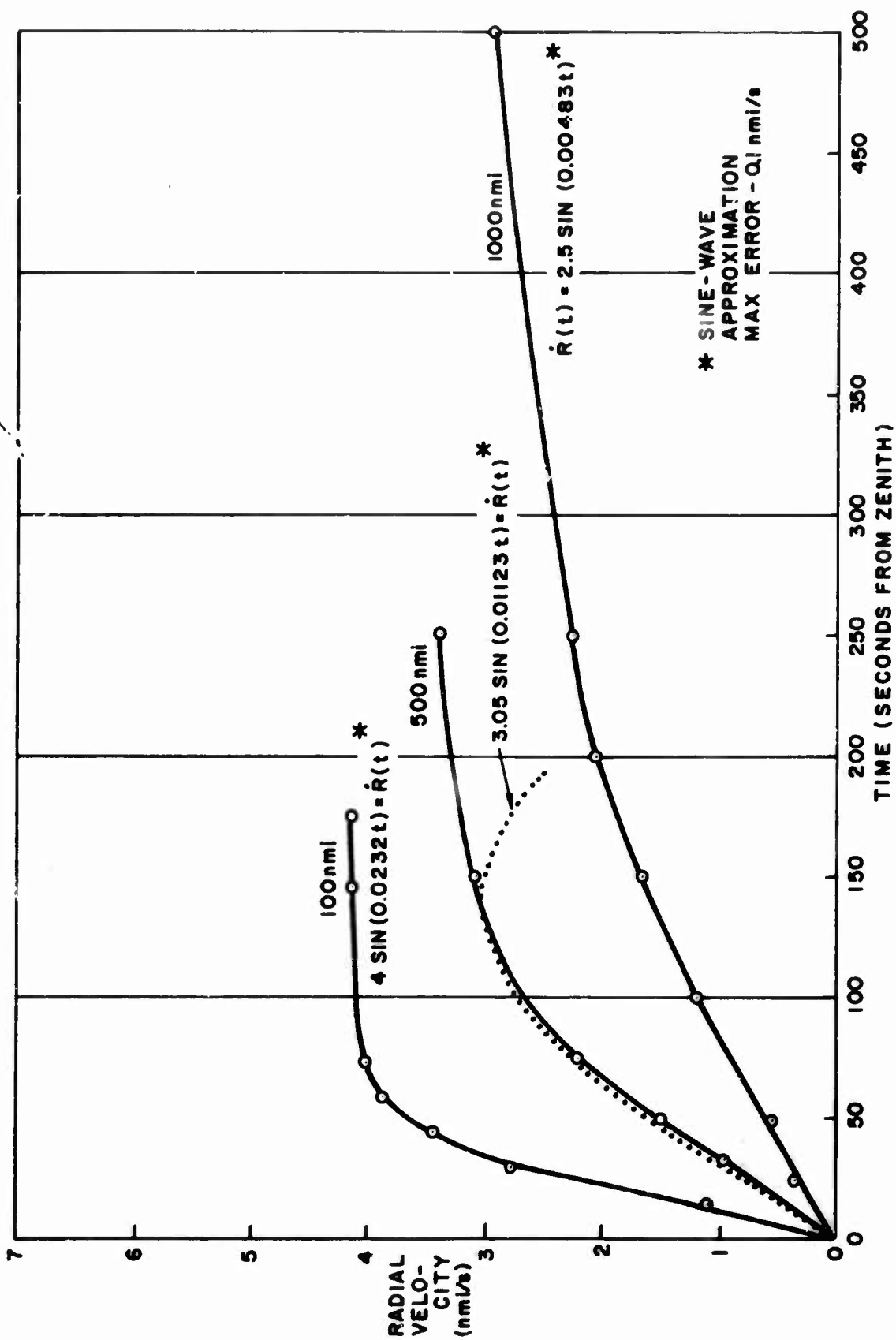at Altitudes of 100, 500 and 1000 Nautical Miles

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Fig 18 - Range Rate vs Time for Overhead Passes of Circular
Orbits at Altitudes of 100, 500 and 1000 nmi

For this system $D_n = 6.25$ nmi and 13.5 nmi

$$\alpha = 2 \times 10^4 \text{ Hz/s} \quad \text{or} \quad 2 \times 10^5 \text{ Hz/s}$$

This has been implemented by using a switchable voltage divider to supply the appropriate control voltage to a VCO. This VCO has been designated as the offset VCO and is centered at 69 MHz. The configuration for the two angle outputs is shown in Figure 19.

The angle rate variation is

$$\dot{\Theta}_{12} = \frac{2 f_T}{C} (\dot{R}_2 - \dot{R}_1) = 0$$

For the first orbital path assumed, the relationship involving the MS and SS1 can be derived by considering that the target occurring at the MS is the same as at the SS except that it is delayed by an amount of time equal to the time that the satellite takes to go the base line distance D_3. Let τ_x be this time delay, then

$$R_3 = R_0 - R_a \cos \omega(t - \tau_x)$$

and

$$\dot{R}_3 = R\omega \sin \omega(t - \tau_x)$$

$$\tau_{\Theta_{13}} = \frac{1}{C}(R_3 + D_3 - R_1)$$

$$= \frac{1}{C}\left[D_3 + R_0 \cdot R_a \cos \omega(t - \tau_x) - R_0 \alpha R_a \cos \omega t\right]$$

$$= \frac{1}{C}\left[D_3 - 2R_a \sin \frac{\omega \tau_x}{2} \sin (\omega t - \frac{\omega \tau_x}{2})\right]$$

$$= \frac{\alpha}{C}\left[D_3 - 2R_a \sin \frac{\omega \tau_x}{2} \sin (\omega t - \frac{\omega \tau_x}{2})\right]$$
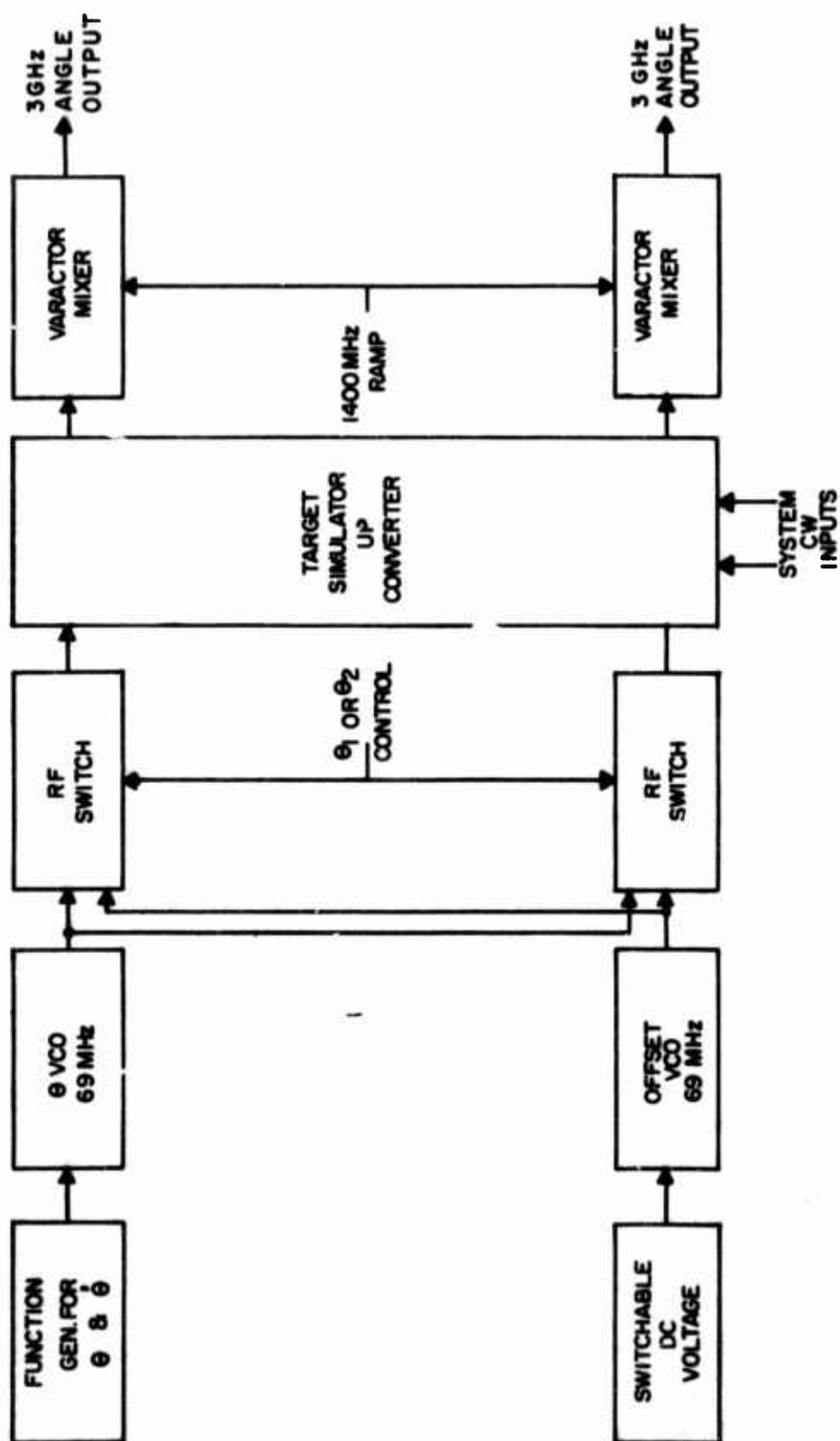
51

Fig 19 - Switch Configuration for Target Simulator

which can be generalized to

$$f_{\Theta_{1n}} = \frac{\alpha}{C} D_n - 2R_a \sin \frac{\omega\tau_x}{2} \sin \left(\omega t - \frac{\omega\tau_x}{2}\right)$$

$f_{\Theta_{13}}$ can also be obtained as above and is

$$f_{\Theta_{13}} = \frac{4f_T}{C} R_a \omega \left(\sin \frac{\omega\tau_x}{2}\right) \cos \left(\omega t - \frac{\tau\alpha\omega}{2}\right)$$

Since $\frac{\omega\tau_x}{2}$ is very small $f_{\Theta_{1n}}$ and $\dot{f}_{\Theta_{1n}}$ can be approximated by

$$f_{\Theta_{1n}} = \frac{\alpha D_n}{C} \left(1 - \frac{R_a \omega \tau_x}{D_3} \sin \omega t\right)$$

$$\tau_x = \frac{D_n}{v_n} \quad \text{where} \quad v_n = \text{satellite velocity}$$

$$f_{\Theta_{1n}} = \frac{\alpha D_n}{C} \left(1 - \frac{R_a \omega}{v_n} \sin \omega t\right)$$

and $\dot{f}_{\Theta_{1n}}$ is

$$\dot{f}_{\Theta_{1n}} = 2\omega^2 \frac{f_T R_a}{C} \tau_x \cos \omega t$$

$$= \frac{2\omega^2 f_T R_a D_n}{C v_n} \cos \omega t$$

DOCUMENT CONTROL DATA - R&D

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13. ABSTRACT

Changes and additions were made to the two-site Active Swept Frequency Interferometer Radar (ASFIR) to provide three-site capability. Addition of the second base line (3rd Site) required a new angle tracker, timing and logic modifications, new mode selection logic and revised data formatting. Distribution and generation of new RF signals were also required. New capability designed into the modification program included extended unambiguous range tracking to 3600 nmi, reduction of system timing jitter, frequency multiplexing of the range rate and angle rate signal processing, and target simulation. The total modification kit included six new racks of equipment plus considerable changes to the existing 14 racks of equipment, including relocation for optimum packaging. Verification of the changes, using the target simulator (which proved to be an effective tool for system test, alignment and evaluation) and by tracking Echo II, showed a considerable improvement in track loop performance and a 3:1 reduction in system timing jitter. Data formatting and logic compatibility were shown by producing a test data tape for data reduction. Detailed recommendations include noise reduction techniques, short term phase stability improvements, improved modulation methods, and system changes to eliminate system timing jitter and to provide AGC.

DD FORM 1473

14. KEY WORDS	LINK A		LINK B		LINK C	
	ROLE	WT	ROLE	WT	ROLE	WT
Interferometer						
Linear FM						
Radar						

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