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Final Report

INVESTIGATION OF RELIABILITY TESTING AND PREDICTION TECHNIQUES FOR INTEGRATED CIRCUITS

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Texas Instruments, Incorporated

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FOREWORD

This final report was prepared by Texas Instruments, Incorporated, P. O. Box 5012, Dallas, Texas, under Contract AF30(602)-3723, Project 5519, Task 551902, System 760E, Contractor Report Number 03-66-131. The period of time covered was from 19 April 1965 through 19 October 1966. Authors were D. R. Fewer, W. L. Gill, S. F. Musket and W. L. Workman.

RADC Project Engineer was Mr. Regis Hilow (EMERR). Technical Advisors were Mr. John Carroll (EMERP) and Mr. Edward O'Connell (EMERM).

The information contained in this report pertains to the reliability, performance and evaluation of state-of-the-art components.

This technical report has been reviewed by the Foreign Disclosure Policy Office (EMLI). Release of subject report to the general public is prohibited by the Strategic Trade Control Program, Mutual Defense Assistance Control List (revised 6 Jan 65) published by the Department of State.

This technical report has been reviewed and is approved.

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ABSTRACT

This report is the last in a series of three reports relating to the work performed by Texas Instruments under this contract. The work is divided into four parts: (1) Data analysis and preliminary tests to determine failure mechanisms for early direction in the study; (2) a physics of failure program consisting of fundamental oxide studies, metal contact and interconnection evaluations, and circuit analysis; (3) a test program including data and failure analysis and consisting of two major segments; and (4) the development of a reliability screening procedure for integrated circuits. Three computer programs, SERF, LINDA 1 and LINDA 2 were written to assist in the analysis of data.

The physics of failure program consisted of fundamental surface studies to produce stable metal-oxide-silicon (MOS) systems, circuit analysis of the SN5420 integrated circuit, and a study of the molybdenum-gold expanded contact system.

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TABLE OF CONTENTS

TABLE OF CONTENTS (Continued)

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS (Continued)

LIST OF TABLES

LIST OF TABLES (Continued)

EVALUATION

1. The objectives of this effort were to comprehensively define, through physics-of-failure studies and a test program, all of the pertinent factors that affect silicon microcircuit reliability. The end items sought in this effort were a nondestructive reliability screening procedure for failure rate improvement and acceleration factors for rapid reliability prediction for a given class of silicon monolithic microcircuits.

2. The physics-of-failure studies were concerned with oxide stability, contact and interconnect studies, and circuit analysis. The main test vehicles used in the oxide studies were MOS capacitors and MOS transistors, whereas the SN5420 was utilized in the circuit and metalization studies. Concurrent with these studies, a detailed test program was conducted to determine the operating failure modes of the SN5420 and their dependence on various electrical and environmental stresses.

3. The significant achievements resulting from this effort are specified as follows:

a. A complete nondestructive screening procedure including real cost of each screen was developed. Included in this procedure are detailed visual criteria for accepting or rejecting precapped microcircuits.

b. The bond study clearly demonstrated that bond strength varies from lot-to-lot. A shear bond test was developed to measure this variance and is presently employed by Texas Instruments as a quality control procedure.

c. Substantial proof is provided to show that the development of universal acceleration factors for monolithic microcircuits is virtually impossible.

d. A detailed circuit analysis of the SN5420 resulted in two non-conventional (not called for in manufacturer's electrical specifications) a-c tests and proved to be more sensitive preindicators of device degradation than the standard on-off d-c tests.

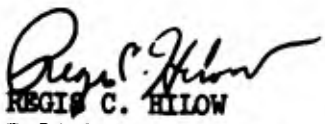
e. Demonstrated that a silicon monolithic microcircuit can be more reliable than the discrete transistors that make up the circuit.

f. Developed two computer programs to aid in developing screening tests for any electronic part.

g. Definition of work elements that need further investigation.

Although the results of this effort were obtained from the study and testing of the SN5420, TTL dual nand gate, the major portion of the resulting techniques and definitions is applicable to any silicon microcircuit.

4. Two follow-on efforts are presently underway to optimize the screening procedure mentioned in 3.a with respect to cost and efficiency and to generalize the circuit techniques. The techniques developed in this report have been utilized in the preparation of RADC Exhibit 2867A, "Quality and Reliability Assurance Procedures for Monolithic Microcircuits," and are being utilized in preparation of the Joint DOD/NASA Standards for silicon monolithic microcircuits.



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SECTION I

INTRODUCTION

1. SUMMARY OF REPORTS

This report is published in two volumes and is the last in a series of three reports on United States Air Force Contract No. AF30(602)-3723, prepared for Air Force Systems Command Research and Technology Division, Rome Air Development Center, Griffiss Air Force Base, New York.

One volume titled "Surface Studies" (RADC-TR-66-776)[1] reports results of the fundamental oxide studies performed as a part of the physics of failure program. This volume contains results of other physics of failure studies, test programs, failure and data analysis and the integration of these studies to determine reliability screening and prediction methods for integrated circuits.

This report covers progress made during the calendar period 20 April 1966 through 19 October 1966. The work discussed in two previously published interim reports[2, 3] is summarized in Section II.

2. PROGRAM SUMMARY

The contract was an eighteen-month program consisting of four major interrelated work elements.

Data Analysis and Preliminary Tests

Physics of Failure Program

Accelerated Reliability Tests

Nondestructive Reliability Screening

a. Data Analysis and Preliminary Tests

A study was conducted to analyze the reliability of the SN5420 to determine failure mechanisms for early direction in the study.[2] The analysis was supplemented by a series of short-term high-stress tests to provide additional information on failure mechanisms and gross time stress relationships. Data acquired from these studies provided information for the design of the test program.

b. Physics of Failure Program

The physics of failure program consisted of surface studies, contact and interconnection studies, and circuit analysis.

Surface Studies. Surface studies, reported in a separate volume,[1] were primarily concerned with sodium contamination of thermal oxide on silicon. The work was concerned with linking the instability of the oxide in the metal-oxide-silicon configuration to chemical contamination levels. The final report details how the techniques of neutron activation analysis and precision profiling were applied to measurement of sodium levels in phosphorous diffused oxide as well as conventional and clean oxides. In this connection, the kinetics of thermal diffusion of phosphorous oxide in planar oxide were also detailed. Two techniques for the formation of clean oxides were discussed. Sufficient description was made to allow other investigators to repeat the work; hence some techniques for clean oxide formation have been extended to the industry at large. It was demonstrated that once a clean oxide has been produced, the problem of contamination caused by application of contacts still remains. The work describes how simple chemi-sorbed impurities may be efficiently removed with aqueous HF solution and de-ionized water washing. Further the importance of the method of metal contact application was detailed.

Circuit Analysis. A d-c analysis of the SN5420 under one set of operating conditions showed that the power dissipation was concentrated in diagonally opposite corners of the chip. From a power distribution standpoint, it appears that the circuit topology could be improved. However, such a change would probably result in increased lead resistance, shunt capacitance and possibly in crossovers. Furthermore, the actual operating stresses in a typical system probably depend more on transient effects than on steady state power dissipation. The point at which parasitic capacitance has the greatest effect on the output waveform, was identified. Any significant change in this capacitance, as a function of stress, would introduce a reliability problem. Fortunately, doping levels and applied voltages are such that this kind of change is not likely. From a power dissipation standpoint, it was found that d-c stress conditions were not particularly good approximations of use conditions wherein a device is rapidly switched between its two output states. A ring counter test with appropriate load capacitors recommended as more representative of actual use conditions was evaluated during the program. Results of this evaluation are reported in Appendix A.

Electrical measurements, voltage gain and output impedance which characterize the NAND gate as a linear device were developed as a part of the circuit studies. These measurements are referred to as non-functional since they are not specified on the standard data sheet of the device. Complete results of these circuit analysis studies were reported in a previous interim report[3]. These measurements were used in addition to standard functional measurements to characterize devices subjected to the test program.

Contact Studies. A study of the molybdenum-gold contact system was conducted. Results are contained in Section V of this report. Test samples were selected from the same manufacturing lots represented by devices used in the reliability test program. A study conducted to investigate bond strength and metallization adherance revealed that no significant degradation occurred as a result of high thermal and mechanical stress. However, bond strength and metallization adherence was found to be highly lot dependent. A correlation between measured bond strength, the modes by which the bonds separated, and the incidence of failure due to peeling metallization which occurred on the test program, was determined. A new technique to measure shear bond strength was used during the evaluation. This technique is included as a part of the reliability screening procedure outlined in Table I.

Additional studies were performed to evaluate voids, thin spots, scratches and metallization resistance by high thermal and electrical stresses. The emitter base junctions of transistor components were characterized during high thermal and electrical stress to detect any evidence of resistive contact formation. None was found.

c. Test Program

Accelerated reliability tests were conducted during the program to determine the principle failure mechanisms of the SN5420 and the relationships between fixed and step stresses. The first approach to data analysis was the use of computer techniques to determine discriminant reliability screening and prediction methods suitable for incorporation into reliability specifications. It became evident early in the study that few failures could be obtained from stresses conducted as long as 1000 hours; functional electrical parameters (data sheet parameters) or combinations thereof, could be used to predict less than 10 percent of these failures. On the basis of the results, a fundamental change in the program was made. Electrical stresses were extended to 2000 hours and the levels of stress increased to the limits of device materials and test equipment capabilities. Die photographs taken prior to capsulation of the device were used to determine what visual information existed on the dice which would predict failure. While the extended stresses caused few additional failures, the study served to identify specific failure mechanisms associated with longer term stress. Photographic analysis revealed that one-third of the stress failures caused by die faults were related to visual information which existed on the dice prior to stress. This work was essential in developing the reliability screening procedure discussed in the following paragraph.

d. Nondestructive Reliability Screening

A reliability screening procedure developed during the contract for the SN5420 is shown in Table I. The effectiveness of two techniques developed from the physics of failure studies, namely shear bond strength and the nonfunctional electrical measurements, were demonstrated during the test program. In addition,

Table 1. Reliability Screening Procedure for SN5420

Procedures			Effectiveness of Screens to Eliminate Failures**				
			Die Integrity			Package Integrity	
Screening Levels	Techniques	Detail Ref.	Oxide	Metal	Bulk	Wire Dress	Die Mounting
I. Precap lot acceptance	Shear Bond Strength	Fig. 27		80%			
II. Precap 100% screen	20X Package Screen	Fig. 10				50%	
	70 X Die Screen	Table 4	50%		50%		
III. Postcap 100% screen	Hermetic Seal*	Sec. IV.					
	Electrical Measurements	Table A-2					
	Centrifuge - X, Z planes	Sec. IV.				40%	
	Followed by X-ray	Fig. 10					
	Centrifuge - Y_1 plane			20%		10%	100%
	Electrical Measurements	Table A-2					
	300°C Storage-168 Hr.				50%		
	Electrical Measurements	Table A-2					
	Electrical Burn-in 160°C - 168 Hours	Figs. A-3,4	50%				
	Electrical Measurements	Table A-2					
	Hermetic Seal*	Sec. IV					

* No Failures were caused by poor hermetic seals. Refer to Section IV for discussion.

** Effectiveness (%) = No. Failures detected by technique divided by total No. Failures X100.

precapsulation photographs of the devices subjected to stress were used to relate failure mechanisms to information which existed on the dies prior to capsulation. The screening procedure was developed by identifying the failure mechanisms resulting from the test program and relating these to information which existed at the earliest point in the manufacturing cycle following the die mount and lead mount operations. The percentages shown in Table I demonstrate the effectiveness of the screens to identify failures which occurred during the stress program. The term "effectiveness" is used to describe the proportion of failures removed by the screening technique. This term should not be identified with the term "screening efficiency" used in this report to measure the ability of computer programs such as SERF and LINDA to discriminantly identify potential failures from a population of devices. A comprehensive discussion of the screening procedure, techniques, and cost of screening is presented in Section IV.

e. Computer Programs

The computer program SERF developed for this contract was demonstrated to be of value in isolating the preindicators of failure. It is based on the assumption that devices which are less reliable have at least one parameter whose value is higher or lower than the rest of the devices. The term "parameter" may refer to absolute values or to the change observed in the value of a parameter as a function of stress. The computer program examines the parameters of each device in the sample and selects the parameters and parameter values for the sample which optimize the screening efficiency, a term used to denote a quantitative measure of the effictiveness of the screening procedure to eliminate failures. Screening efficiency was calculated in two ways:

$$e = \frac{\% \text{ Failures Removed}}{\% \text{ Population Removed}}$$

or

$$e^* = 0.5 + 0.5\,(F_f - F_g)$$

where

F_f = Fraction of total failures removed

F_g = Fraction of total good devices removed

Two other computer programs, LINDA 1 and LINDA 2 which are based on linear discriminant analysis [4] were written and adapted for use in the program. This method requires that a linear discriminant function be determined prior to screening the devices. The function is a weighted sum of the measurements to be used in screening; it is determined from measurements made on a group of devices, some of which are known to be stress failures, others known to have survived stress. It is assumed that the device to be evaluated is from the same general population as the devices used

to generate the linear discriminant function. The parameter measurements of a device in the population to be screened are converted to a value of the discriminant function. This procedure ultimately results in the division of the population into two groups, either good or bad, defined by a critical value of the discriminant function. The use of models to relate fixed and step stress and computer screening techniques to this program was severely limited for two reasons. First, few failures (5 to 10%) occurred from stresses conducted at levels far beyond the maximum ratings of the device. It was also determined that functional (or data sheet) parameters or combinations of these could be used to predict only certain types of failures, representing less than 10% of the devices which failed. However, the SERF Program was used to isolate parameters which preindicate failure for a few devices which failed high temperature storage stress. This work is discussed in Sections III and IV.

f. Publications

The following is a list of the papers published as a result of the work performed on this contract.

H. G. Carlson, C. R. Fuller, and D. E. Meyer, "Effects of Phosphorus on Sodium Distributions in Oxides, "Las Vegas, Nevada (1965). Silicon Interface Specialist's Conference (SISC)

H. G. Carlson, C. R. Fuller, and J. F. Osborne, "Effects of Phosphorus Diffusion on Sodium Concentration Profiles in Thermally Grown Silicon-dioxide Films," Buffalo, New York, (October, 1965). Electro-chemical Society (ECS)

H. G. Carlson, G. A. Brown, C. R. Fuller, and J. F. Osborne, "Effects of Phosphorus Diffusion in Thermal Oxides on the Elevated Temperature Stability of MOS Structures," 1965 Physics of Failure in Electronics Symposium (November, 1965). Published in Volume 4 of Physics of Failure in Electronics, Defense Documentation Center, Cameron Station, Alexandria, Virginia. AD No. 637 529

H. G. Carlson, C. R. Fuller, J. F. Osborne and G. A. Brown, "Stability of Etched Oxides," The Electrochemical Society Meeting, Philadelphia, Pa. (October 1966).

H. G. Carlson, V. Harrap, and J. F. Osborne, "Sodium Free Oxides," Electrochemical Society Meeting, Philadelphia, Pa. (October 1966).

H. G. Carlson, D. E. Meyer, C. R. Fuller, V. Harrap, J. F. Osborne and G. A. Brown, "Clean MOS Systems," Fifth Annual Physics of Failure in Electronics Symposium, (November, 1966). To be published in Volume 5 of Physics of Failure in Electronics, Defense Documentation Center, Cameron Station, Alexandria, Va.

Walter L. Gill and Wilton Workman, "Reliability Screening Procedures for Integrated Circuits," Fifth Annual Physics of Failure in Electronics Symposium, (November, 1966). To be published in Volume 5 of Physics of Failure in Electronics, Defense Documentation Center, Cameron Station, Alexandria, Va.

D. F. Meyer, "Retention of HF on Surfaces Common to Silicon Devices — II," Cleveland, Ohio (May, 1966). Electro-chemical Society (ECS)

SECTION II

PROGRAM REVIEW

1. INTRODUCTION

This section highlights results of the work discussed in two interim reports relative to this contract. These are identified by the following report numbers:

RADC-TR-65-463 — Technical Documentary Report I [2]

RADC-TR-66-345 — Technical Documentary Report II [3]

2. TEST VEHICLE [2]

The SN5420 dual four input NAND gate was studied throughout the program. The logic equation of the circuit is $E = \overline{ABCD}$. The device is fabricated on a single chip using the diffused isolation. The molybdenum-gold expanded contact system was used with the device, which is packaged in a fourteen-pin metal flat pack.

3. CIRCUIT ANALYSIS [3]

a. Objective

The objective of the circuit studies program were to determine the design factors which affect reliability of integrated circuits and to develop electrical measurements which are more sensitive to degradation and more useful for reliability prediction than standard functional tests. These studies were divided into three main parts; dc analysis, small signal analysis and a transient analysis.

b. DC Analysis

The dc analysis was performed under conditions representing a compromise between the on and off state encountered in an actual system. The ECAP computer program was utilized in this study. The power dissipated in each of the elements of the circuit was calculated and it was determined that the layout of the silicon chip was such that most of the power was dissipated in two diagonally opposite corners.

c. **Small Signal Analysis**

The operating level used in the dc analysis was used in conjunction with the small signal analysis to develop nonfunctional parameters which might be significant degradation indicators. Two useful parameters, circuit gain and output impedance, were determined from this study. The term "nonfunctional" is used to identify these parameters separately from the standard parameters which are used to specify electrical performance of the device. The measurements are affected by changes in current gain of three transistors and in the values of three resistors in the circuit. They were implemented into the main test program and used to study degradation phenomena in devices subjected to stress. Refer to Section III for discussions of this work.

d. Transient Analysis

The main purpose of this study was to determine the effects of the various parasitic elements within the circuit. Both theoretical and measured output wave forms were obtained. Parasitic capacities were evaluated and it was determined that the frequency of a square-wave input is increased, the instantaneous power dissipated during switching may become significant. The instantaneous power dissipation in each component was calculated and it was determined that significant power pulses are present in the output and phase splitting transistors. The results indicated that for a square-wave drive at 50 MHz the average power dissipated by the circuit is about three times the low frequency power. It was further determined that from a power dissipation standpoint it appeared that dc stress conditions are not particularly good approximations of use conditions wherein a device is rapidly switched between two output states. A ring counter test with appropriate load capacitors is more representative of actual use conditions. A stress test was performed to evaluate the effect of added power due to load capacitance on reliability. Results of the test are presented in Appendix A.

4. FAILURE DEFINITION AND STRESS CIRCUIT ANALYSIS[2]

A study of functional parameters was conducted to determine parameter failure limits on the basis of device physics. These limits were used throughout the test program.

An analysis of the ring counter, forward bias, and reverse bias stress circuits used in the test program was also performed. Nominal values of voltage and power dissipation for each component in the circuit were specified.

5. DATA ANALYSIS AND PRELIMINARY TESTS[2]

At the beginning of the program a study was conducted to analyze reliability data of integrated circuits from other sources such as the Component Quality Assurance Program.[5] This study was conducted to determine failure mechanisms for early

direction in the study. The analysis was supplemented by a preliminary investigation consisting of short term high stress tests to provide a preliminary identification of failure mechanisms and gross time-stress relationships directly applicable to the SN5420. Data acquired from the study provided information for design of the test program. The preliminary investigation indicated that it was not possible to predict device failure at high stress levels from lower stress data. Results further indicated that design of the test program should include an increase in both stress levels and duration.

6. TEST PROGRAM

As a result of the preliminary investigation, the test program was designed utilizing high level fixed and stress step tests.

a. Step Stress Series [3]

The first replicate of the test program consisted entirely of step stress tests. Temperatures for operating tests ranged between 140°C and 200°C. Storage step stress was performed between 300°C and 500°C. Constant acceleration step stress was also performed. Devices which did not fail catastrophically were marked by extreme stability of their electrical parameters. Short-term electrical stress did not produce a significant number of failures even though stress temperatures greater than 200°C were employed. Analysis of very limited data indicated that devices specially processed to contain oxidative oxide did not differ appreciably from the standard production units and their response to stress. It was further demonstrated that few failures were being generated with tests other than storage and constant acceleration. A typical electrical stress test involving 15 devices produced two failures. Stress equipment limitations prohibited the increase of stress temperature, and secondly, since a study of device failure criteria indicated that few if any additional failures could be obtained by tightening the failure criteria, an additional test was performed to extend the time for which stress was applied to the devices. The devices were placed under the same stress which had been applied before but the temperature was maintained at 200°C for 264 hours. Special tests indicated that none of the devices exceeded any of the parameter failure criteria. In fact, the change in the parameter value was so small that any meaningful redefinition of the failure criteria would still not indicate any failures. The additional 264 hours on a special test gave a maximum total stress time of 744 hours on the device. As a result a second test, the Fixed and Step Stress Series was designed using 2000 hours as a maximum time for stress. [2]

b. Fixed and Step Stress Series [3]

The design and performance of this program followed completion of the Step Stress Series. [2] To aid in the development of the reliability screening procedure for integrated circuits, devices were subjected to a photographic analysis

just prior to capsulation. Anomalies observed from the photographs were categorized into 15 groupings. Results of studies performed to relate stress failures to information obtained from the photographic analysis are contained in Appendices A and D of this report. A visual die inspection procedure discussed in Section IV was developed from this work.

7. COMPUTER PROGRAMS[3/]

Three computer programs have been written for the analysis of the data generated on this program. SERF (Screening Efficiency Reliability Factors) determines from the input data the relative screening efficiencies of up to 40 measured parameter values as well as delta and percent change of these values, a total of 120 parameters on up to 100 components. Parameters predicting failure are isolated and the screening levels for these parameters are determined. LINDA I (Linear Discriminant Analysis) determines the weighting factors λ in the linear discriminant function

$$U = \sum_{i=1}^{m} \lambda_i P_i$$

(P_i are parameter values) as well as that value of U which gives maximum discrimination between the good and bad devices of a population. It is assumed in using LINDA 1 that the covariance matrices of the good and bad devices are identical. However, a more sophisticated program, LINDA 2, does not make this assumption. A complete description of SERF and LINDA are contained in Appendix C of this report.

SECTION III

TEST RESULTS AND ANALYSIS

1. INTRODUCTION

In this section, data is presented to demonstrate the results of screening using the SERF Computer Program, behavior of nonfunctional parameter measurements as a function of stress, and the highlights of the test program and related failure analysis activities. The reader is referred to Section II for a review which summarizes the results of work reported in two previous interim reports. [2] [3] The items listed below are frequently referred to in the discussions which follow and serve as guides to more detailed information concerning the individual topics.

a) Test Program - Preliminary Investigation [2] (Section II); Step Stress Series [3] (Section II); Fixed and Step Stress Series (Appendix A); and Component Evaluation (Appendix B).

b) Failure Analysis (Appendix D)

c) Functional Parameters and Failure Limits [2] (Appendix A)

d) Nonfunctional parameters [3] (Section II)

e) Theory Relating Fixed and Step Stress (Appendix E)

f) Computer Programs (Appendix C)

2. MEASUREMENT ERROR DETECTION AND CONTROL

To detect and/or minimize errors in parameter measurements equipment malfunctions and faulty mechanical contacts, procedures to determine the variations in data due to these causes were followed for all of the tests conducted during the program. The procedures may be separated into two categories, error detection and error control.

Error detection consists of conducting measurements on unstressed control samples while simultaneously measuring stressed samples. Variations attributable to measure error can be detected by analyzing the repeated measurements taken on the "control" samples. This procedure is followed when the measurement technique

is limited primarily to the laboratory or where a predetermining measurement failure criteria for the stressed samples is not specified. Examples of the types of evaluations in this program in which this approach was utilized are contact studies (Section V) and nonfunctional gain and output impedance parameters (this section).

The error control contains all the elements of error detection, but also incorporates additional procedures to control the accuracy of the measurements. This approach to error minimization was used in the test program where failure limits were assigned to parameters of the SN5420. Prior to conducting the test program, repeated measurements on the control samples were accumulated over a period of several days. The average ($\bar{X}$) and range (R) of each of the parameters was calculated. This data from the control sample served two purposes. First it was used to demonstrate that limits used to define failure were not significantly affected by measurement error. Secondly, it was used throughout the test programs to verify that measurements taken on test samples were accurate, within the previously defined range of measurement error. When deviations in the control data occurred, corrections were made to the equipment to bring the control measurements back within the required range.

3. SERF SCREENING RESULTS

Application of the SERF program to results of high temperature storage data has revealed that short circuit output current (Ios) is an effective screening parameter. Previously reported analyses of the preliminary investigation indicated that a screening level of 33.9 mA could be used to eliminate 50% of the failures which occurred during storage step stress. Analysis of data from the Fixed and Step Stress Series revealed that six devices degraded on Ios during high temperature storage. Failure analysis traced the cause of degradation to an increase in R_2 and R_3 resistor values (Refer to Appendix B for circuit diagram). The degradation was more greatly pronounced in the measurement of the nonfunctional output impedance and was evident at much earlier steps of applied stress. However, similar changes in the nonfunctional measurements of good devices were also observed and are discussed later in this section. Five of these six failures were predicted by the SERF computer programs discussed in the following paragraphs.

The six failures were located in five of the high temperature storage stress cells defined in Table A-1 of Appendix A. The criterion used to define failure was ± 20% change in the Ios parameter. To evaluate SERF, the Ios failure criteria was changed to ±15% and applied to all of the cells to determine whether more failures could be generated. Twenty-one new failures were defined in this manner all of which occurred in the high temperature storage cells. In all cases, the measurements taken prior to stress were used for prediction. The results of analysis to determine the preindicators of failure for those devices is summarized in Table 2.

Table 2. SERF Screening Results

Test	Screening Conditions	Sample Size	No. of Failures In Sample	No. of Failures Removed By Screening	No. of Good Devices Removed By Screening
Storage Step Stress					
108 Hours/Step	$T_{ON} \geq 9.9$ ns	20	2	2	1
156 Hours/Step	$T_{ON} \geq 8.6$ ns	20	4	4	1
216 Hours/Step*	(a) $V_{OFF} \leq 2.7$ V or (b) $I_{OS} \geq 39.3$ mA	20	6	6	2
264 Hours/Step	$T_{ON} \geq 8.6$ ns	20	11	9	2
Storage Life					
375°C *	(a) $I_{IN} < 1.16$ mA or (b) $I_{IL} > 11.1\ \mu A$	30	9	7	3

* Device is eliminated by screening if at least one of the two conditions are satisfied.

For example, the table reveals that all of the failures on the 216 hours/step test were removed together with two good devices by screening on V_{off} only. Nine of the eleven failures on the 264 hours/step test were removed together with two good devices by screening on the T_{on} switching parameter. The prediction results can be considered very good when considering that screening was done on initial data while most of the failures occurred after 500 hours of stress. It must be emphasized that the screening criteria are based on small samples and only two manufacturing lots (represented by the Preliminary Investigation and Fixed and Step Stress Series). Additional experimentation and analysis is necessary before definite screening criteria can be established.

4. ANALYSIS OF NONFUNCTIONAL MEASUREMENTS

The nonfunctional voltage gain and output impedance parameters discussed in Section II have revealed some interesting information about the stability of circuit components (transistors, resistors, etc.) during stress. Previously reported analyses of functional [2] and nonfunctional [3] measurements indicated that functional parameters are relatively insensitive to certain types of changes in component parameter values such as transistor h_{fe} degradation, when compared to the nonfunctional measurements. In the following discussions the results of analyses of the nonfunctional measurements taken during the Fixed and Step Stress Series are presented. The reader is referred to Appendix A for the description of the test circuits.

In the discussions which follow the term stress cell, ring counter and forward bias are used frequently. Stress cell refers to a particular stress to which a small sample (20 to 30 device) were subjected during the Fixed and Step Stress Series discussed in Appendix A. Ring counter and forward bias refer to two modes of electrical stress used throughout the test program. An analysis of these stress circuits was presented in a previous report, [2] while circuit diagrams may be found in Appendix A.

a. Voltage Gain

The study of voltage gain was conducted by assigning to the measurement an arbitrary failure criteria of percent change relative to initial values. A device was defined as a failure in the following ways (there are two gates per device).

1) ± 10% and ± 20% change Gate 1

2) ± 10% and ± 20% change Gate 2

3) ± 10% and ± 20% change Either Gate

Failures were observed in every stress cell of the Fixed and Step Stress Series. The approach to the analyses was to find the distributions of failures as a function of time and temperature and to calculate activation energy. A theoretical discussion of

activation energy and the relationships between fixed and step stress is contained in Appendix E.

Distributions of failures which are lognormal in time were noted in some cases while discontinuities were observed in others. Degr dation, which can be both circuit and design dependent [2] is believed to have confounded the results. Curves representing the forward bias life tests, forward bias step stress tests and ring counter life tests are reproduced in this report.

In Figure 1, the four cumulative percent failure curves are drawn for forward bias life test; the actual points are shown with each curve. These curves are summarized into one graph shown in Figure 2. Figures 3 and 4 show the cumulative percent failure curves for ring counter life and step stress, respectively. Finally, in Figure 5, the acceleration curves for ring counter life and step stress are given. The acceleration curves were used to determine a possible pattern to the ac gain failures, and whether a relationship between fixed and step stress existed. An activation energy which is disucssed in the following paragraph was calculated to obtain information about the mechanism causing change in the parameter values. It should be noted that the majority of devices represented by the data did not fail any functional parameters during stress.

The step stress data points in Figure 5 for the cumulative 10 and 20 percent failure yield a reasonably good fit to a linear acceleration curve. However, the correlation between the step stress and fixed stress data is not good. The lines connecting the 200°C and 180°C life test points for 10 and 20 percent cumulative failure are entirely different from the step stress lines. The dashed line shown in Figure 3 connects the data points observed through 500 hours for 200°C life test failures. The slope of this line is obviously quite different from the line connecting the 500 to 2000 hour data. Using the former curve (dashed line) to obtain 10 and 20 percent failure points, a reasonably good fit to the step stress data of Figure 3 is obtained as illustrated by ◇'s on Figure 5. Using the step stress data, an activation energy of approximately 0.23 eV for the ± 20 percent gain failures is obtained from the forward bias life test data. Approximately the same value is obtained from the forward bias life test data (Figure 2). The gain measurement is known to be sensitive to changes in resistor values and transistor h_{FE}'s of the circuit components.[3] Tests conducted on circuit components, discussed in Appendix B, revealed that transistor h_{FE} degradation occurred during electrical stressing; efforts to characterize the degradation and to determine a possible failure mechanism are discussed. However, during the test program, no failures defined by functional parameters were caused by transistor h_{FE} degradation, nor was the nonfunctional gain parameter found to preindicate functional failures in the devices.

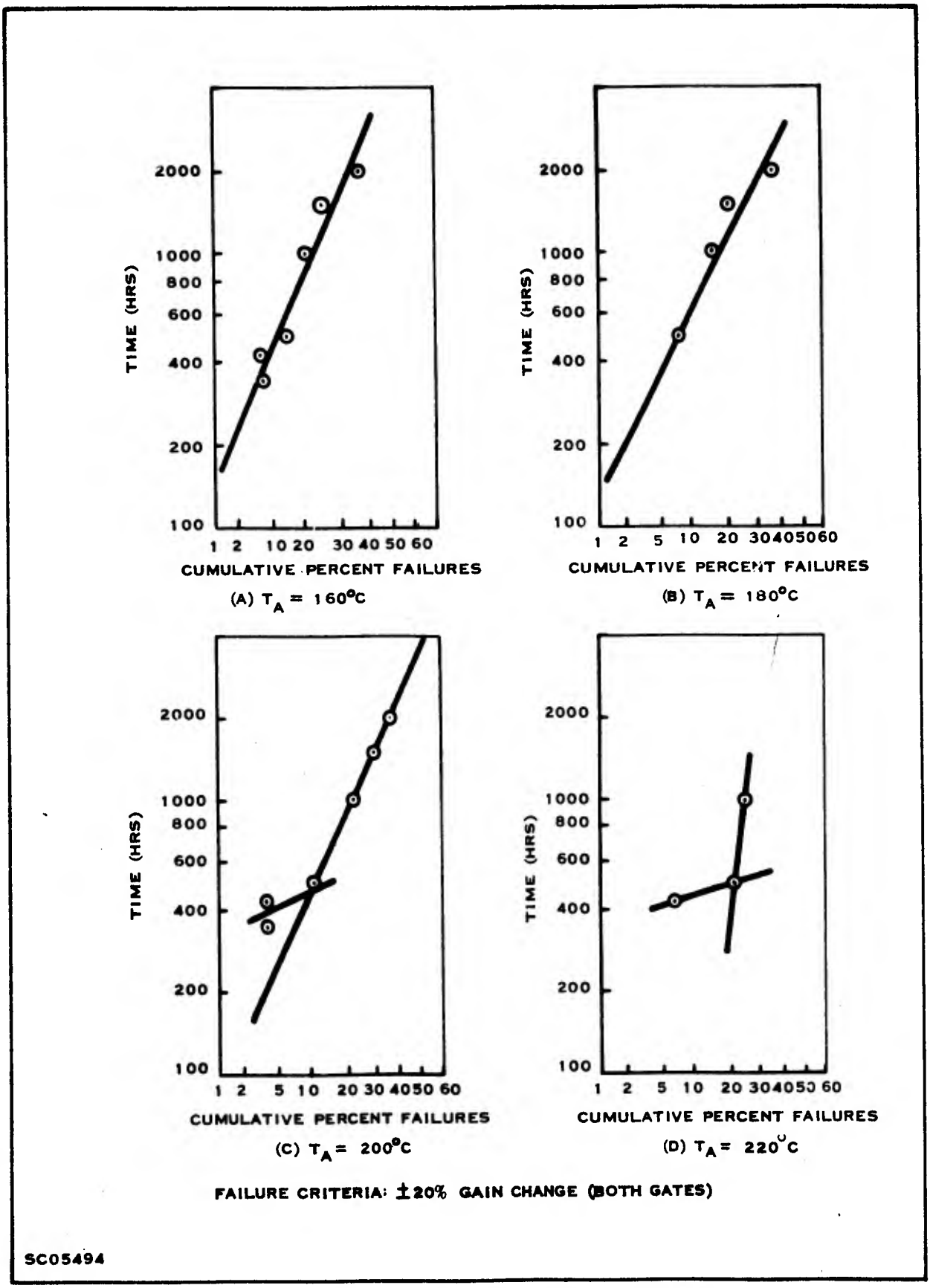


Figure 1. Cumulative Percent Failures vs Logarithm Of Time for Forward Bias Life

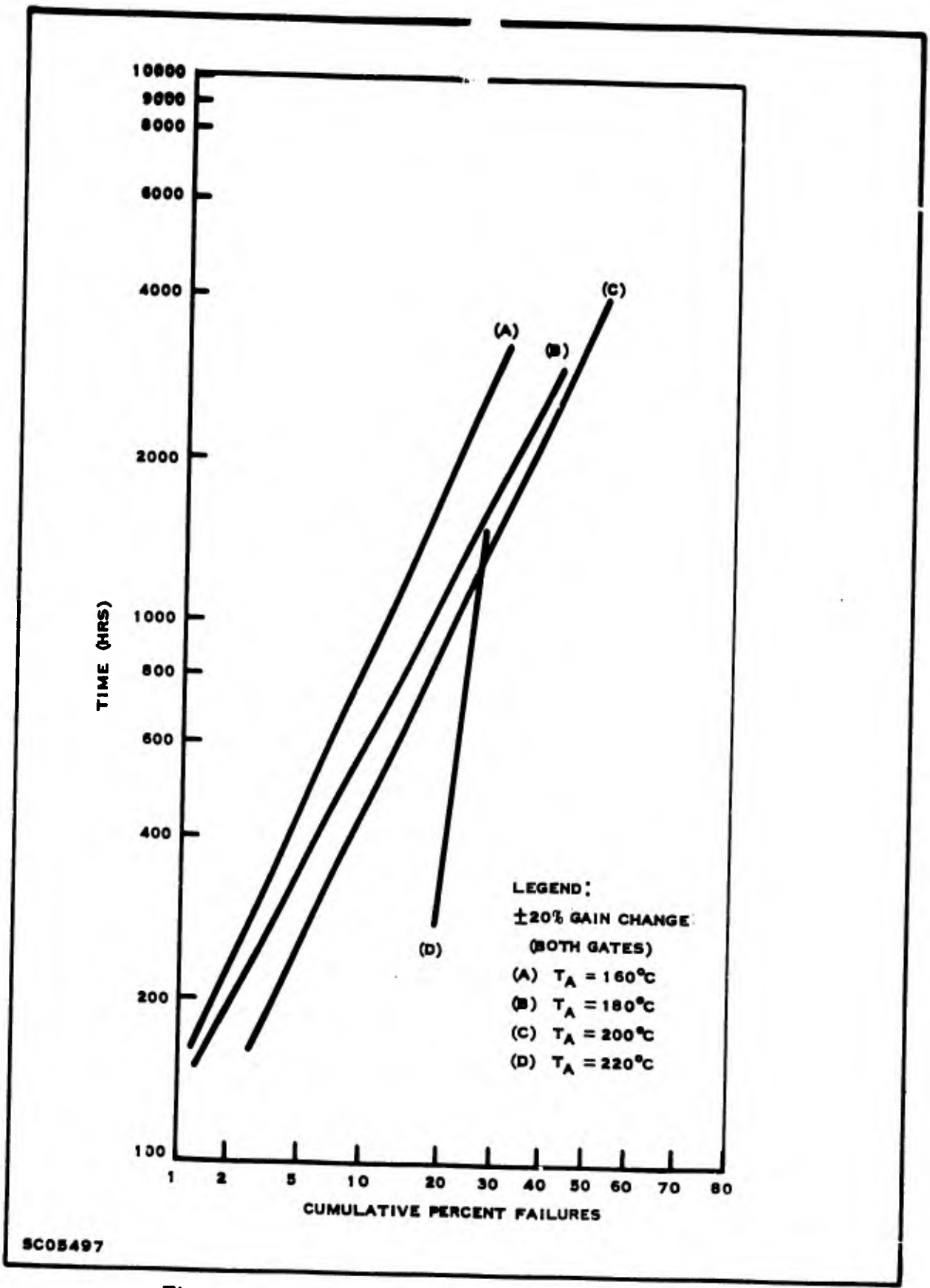


Figure 2. Cumulative Percent Failure vs Logarithm of Time for Forward Bias Life (Summary of Figure 1)

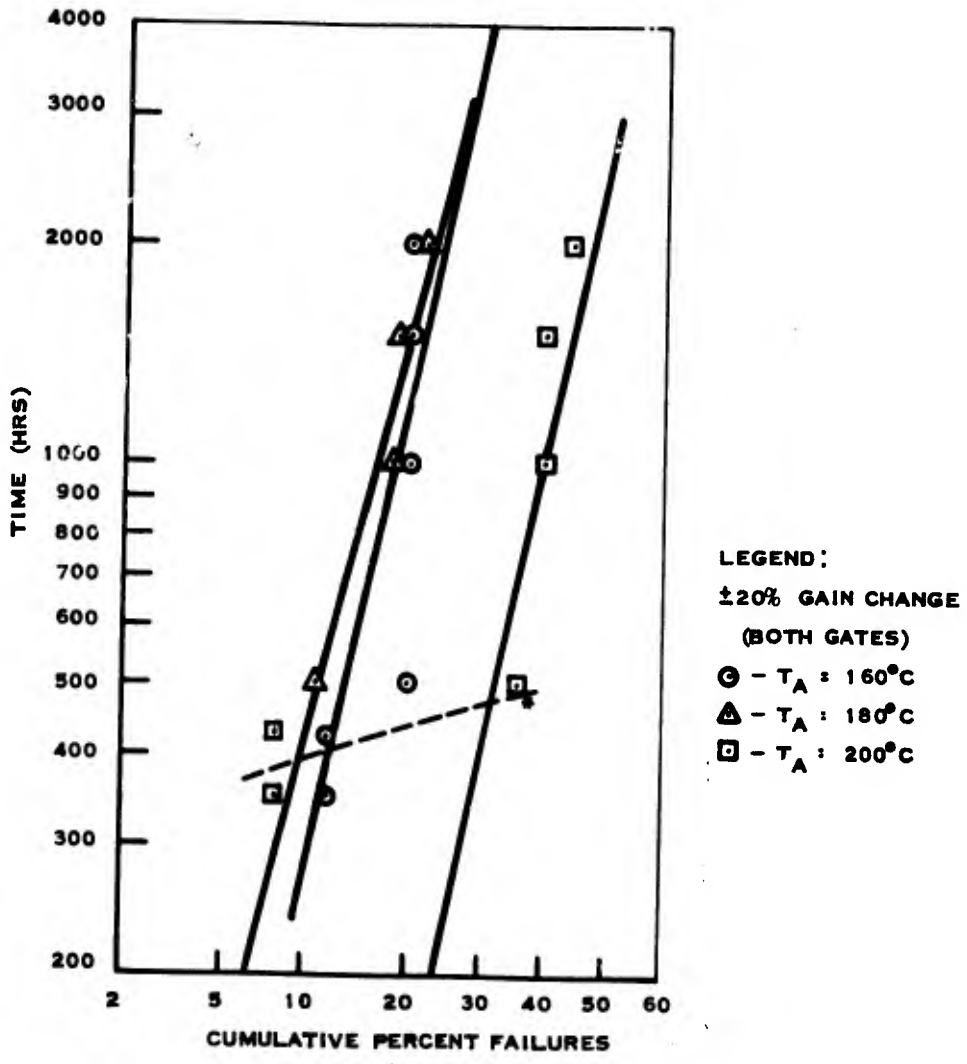


Figure 3. Cumulative Percent Failures vs Logarithm of Time for Ring Counter Life

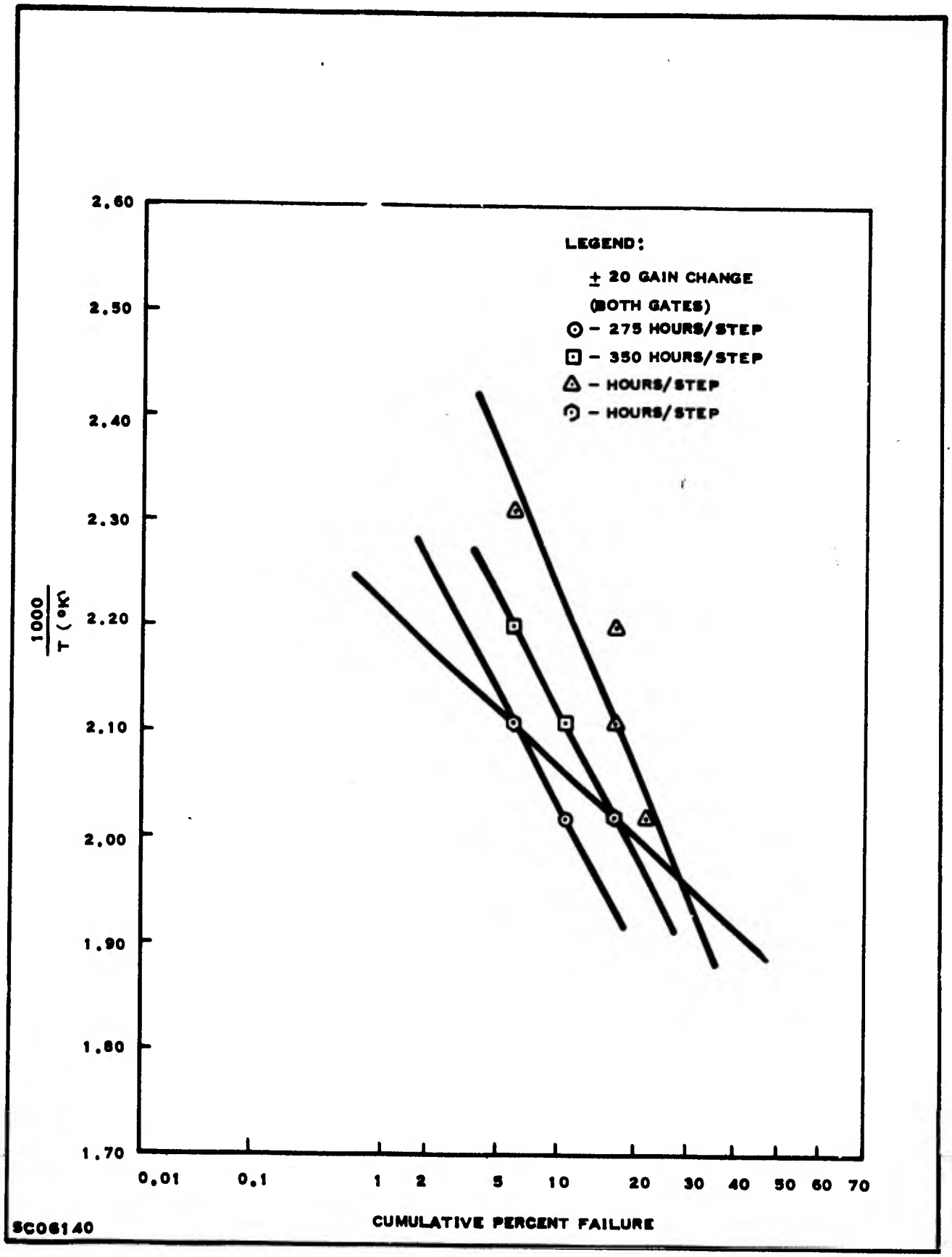


Figure 4. Cumulative Percent Failure vs 1000/T(°K) for Ring Counter Step Stress

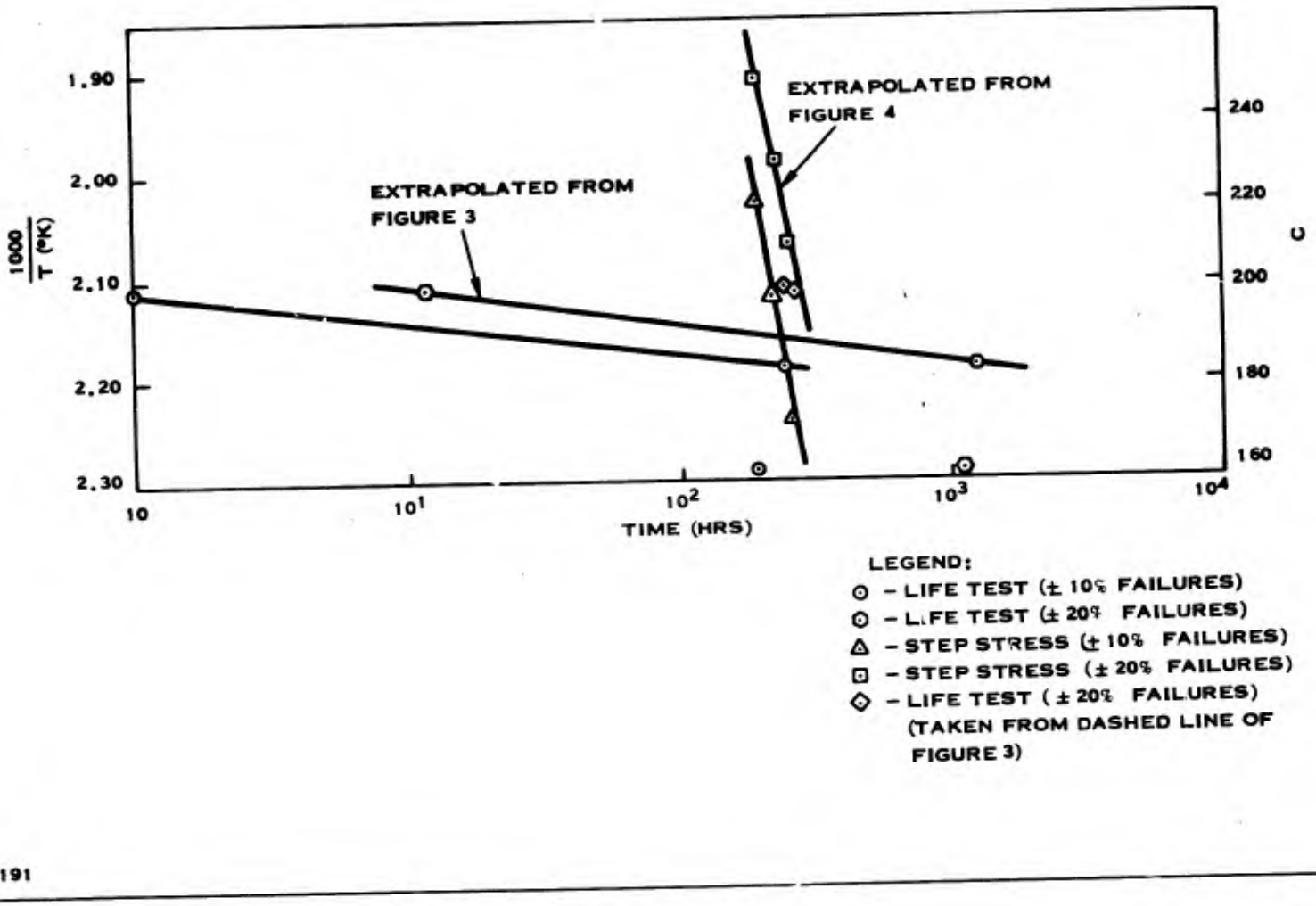


Figure 5. Ring-counter Acceleration Curve

b. Output Impedance

An analysis of the behavior of output impedance was performed to determine the effectiveness of the parameter to preindicate failure in functional devices. Curves showing the variation of output impedance with time were made for many devices subjected to stress. A few of these are presented in Figure 6 through Figure 9 to illustrate the results. Figure 6, shows curves for five devices which did not fail 2000-hour life test; these demonstrate good stability of the particular devices represented. However, Figure 7 demonstrates how considerable variation in the measurements of good devices can occur. Figure 8 illustrates how the measurements of devices which fail late in stress life can be well behaved prior to failure; all of these devices were found to be functional failures at 2000 hours (final stress interval), but there was no apparent preindication of failure. Figure 9 illustrates how output impedance can preindicate failure; all of these devices failed storage life test at either 500 or 1000 hours. A significant increase in output impedance was observed, however, after only 100 hours of stress. While the output impedance measurements were not found to discriminantly predict failure, their sensitivity to component parameter changes, not detectable by functional measurements, has been demonstrated.

5. ANALYSIS OF STRESS FAILURES

The significant results of failure analysis are listed in Table 3, according to the type of stress causing failure. Few failures occurred from storage and electrical stress even though the minimum stress levels used were above the maximum ratings of the devices. The dominant mechanisms observed in failures from the Preliminary Investigation, Step Stress and Fixed and Step Stress Series differed considerably as shown in Appendix D (Table D-1).

Sixty percent of the Preliminary Investigation failures were caused by photolithographic faults and die delamination. A production change to improve die mounting eliminated recurrence of this mechanism.

Seventy-five percent of the Step Stress Series failures were caused by ball bond separation and die and wire dress problems. Analysis of X-rays revealed the dice were oriented improperly in the package, decreasing the minimum separation between bond wires. Constant acceleration caused the wires to touch, which resulted in failure.

Sixty percent of the Fixed and Step Stress Series failures were caused by bond wire dress, peeling, metallization, and die cracks. Wire dress failures were caused primarily from excess slack in wires connecting the die to the package. The slack permitted the wires to move during constant acceleration stress causing the wire to weaken and break at the stitch bond. The incidence of wire breakage was increased if the stitch bond was not centered properly on the bonding pad. Die crack failures

Table 3. Test and Failure Analysis Results

Stress*	Failure Mechanism (Ref Appendix D)	Quantity Failed	Comments	Reliability Screens	
				Screening** Levels	Estimated*** Effectiveness (%)
High Temperature Storage (300-500°C) (325 Devices Tested)	Photolithographic faults	3	Mask misalignment; abnormally large emitter window	III	100
	Metal scratch	1	Scratch exposed molybdenum	II	100
	Die crack	1	Crack occurred during stress	III	100
	Peeling metal	5	Gold peels from molybdenum - occurred with equal probability throughout all stress intervals	I	100
	Resistor degradation	6	Resistors R_2, R_3 increased. Significant changes in non-functional Z(out) parameter observed.	III	80
Electrical Stress (160°-200°C) (880 Devices Tested)	Surface contamination	1	Particulate matter bridged two metal leads on die	II	100
	Oxide defects	7	Pinholes under metal; scratches under metal; spurious diffusion; particulate contamination	II, III	100
	Peeling metal	4	(Remarks for storage failures apply)	I	100
	Die cracks	9	Cracks under bonding pads - existed prior to stress - failures occurred with equal probability throughout all stress intervals	II	100

Table 3. Test and Failure Analysis Results (Continued)

Stress*	Failure Mechanism (Ref Appendix D)	Quantity Failed	Comments	Reliability Screens	
				Screening** Levels	Estimated *** Effectiveness (%)
Constant Acceleration (90 Devices Tested)	Die delamination	10	Die mount material separated from Au plated Kovar. Production corrective action eliminated problem	III	100
	Die and wire dress	29	Die improperly oriented in package; slack wires; non-centered stitch bonds	II, III	100
	Ball bond separation	5	Inadequate bonding pressure or temperature; gold peeling from molybdenum	I, III	100

* Includes preliminary investigation, Step Stress Series I and Fixed and Step Stress Series

** Refer to Table 1.

*** $\% \text{ Effectiveness} = \frac{\text{Failures Removed By Screening}}{\text{All Failures}} \times 100$

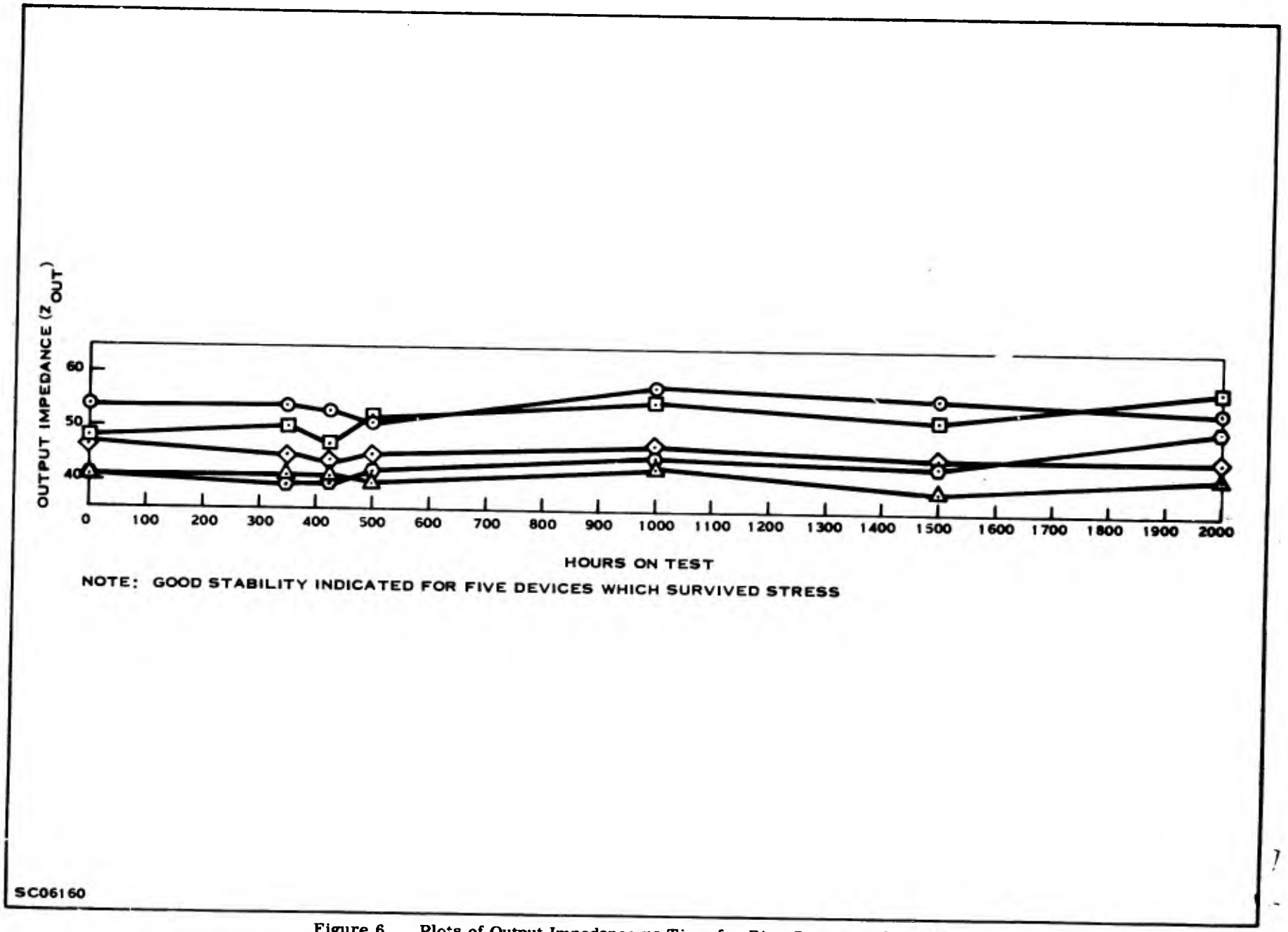


Figure 6. Plots of Output Impedance vs Time for Ring Counter Life Test

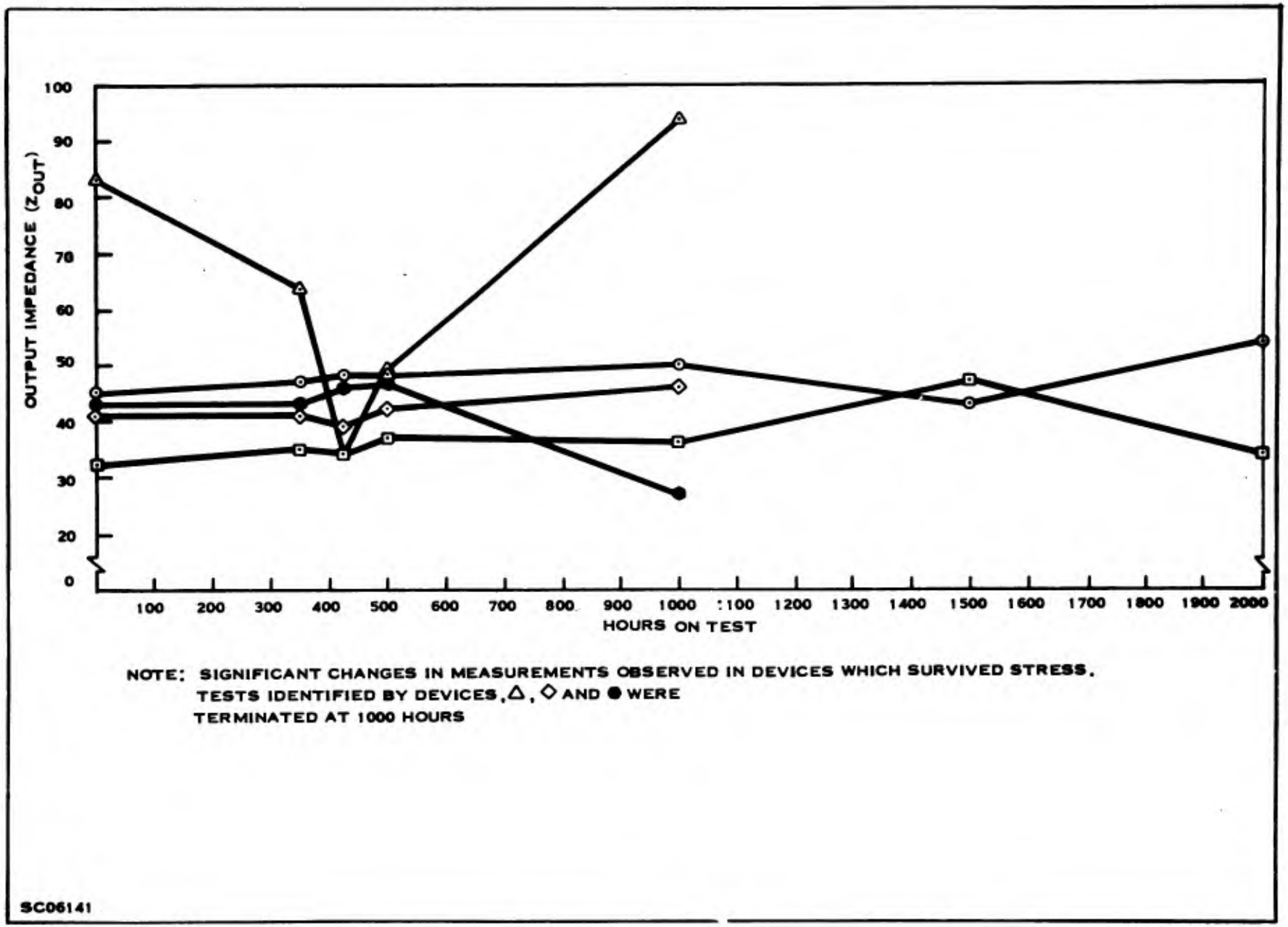


Figure 7. Plots of Output Impedance vs Time for Ring Counter Life Test

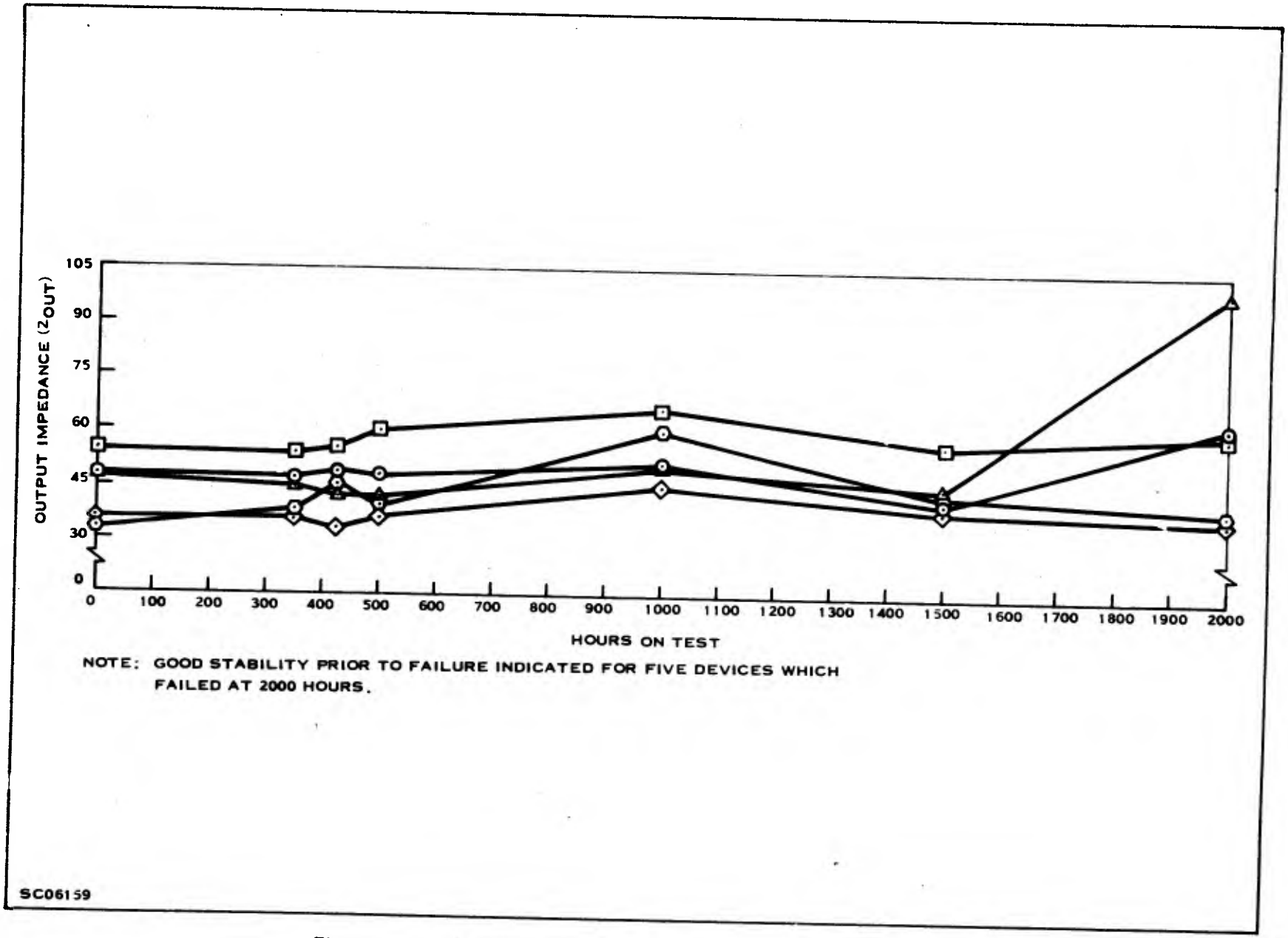


Figure 8. Plots of Output Impedance vs Time for Ring Counter Life Test

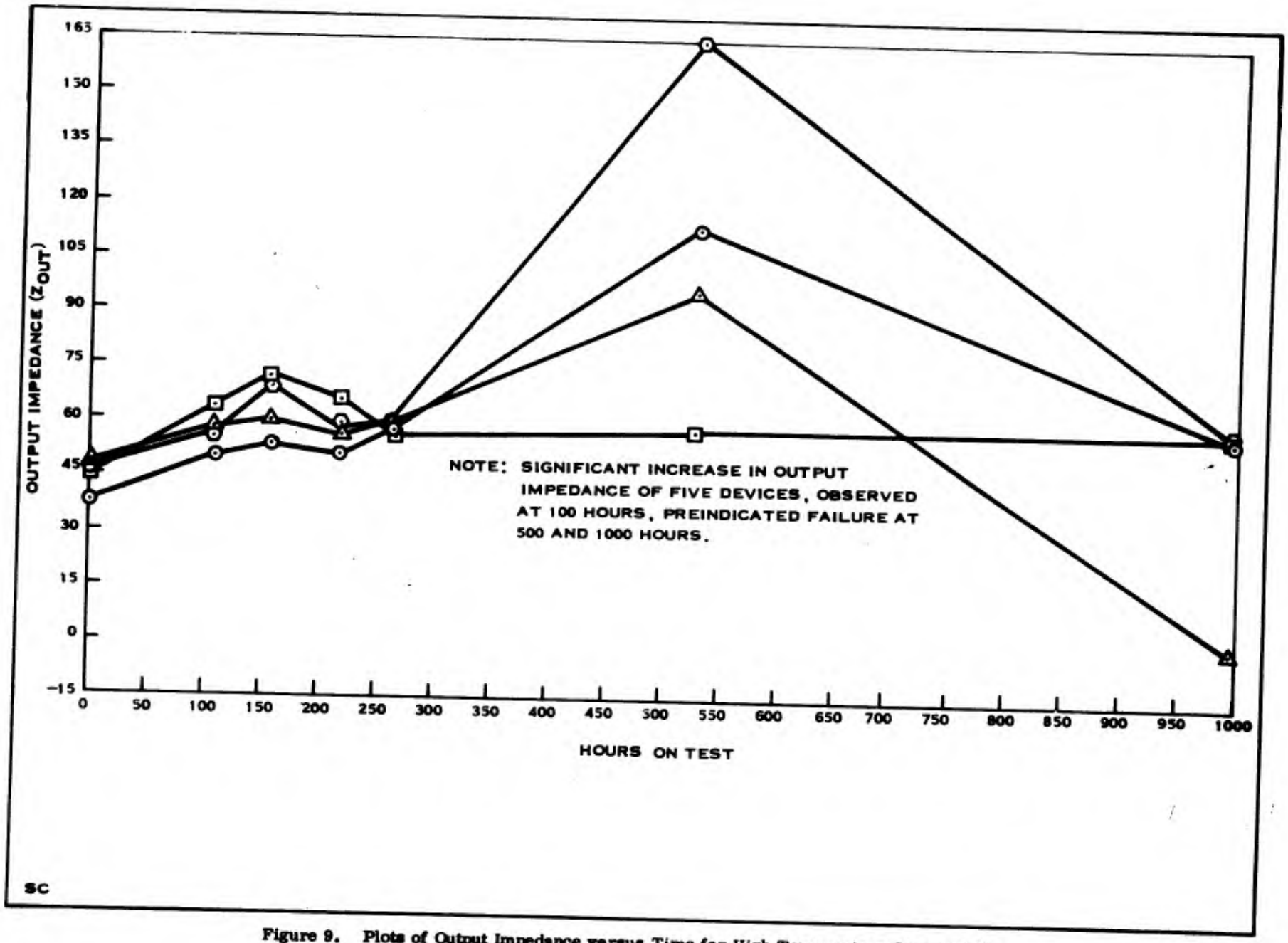


Figure 9. Plots of Output Impedance versus Time for High Temperature Storage Life

were caused primarily from cracks beneath bonding pads and were known to exist prior to conducting the stress tests. Peeling metallization, caused by lack of adherence of gold to molybdenum was encountered on both high temperature storage, ring counter and forward bias operating tests.

6. COMPONENT EVALUATION

A step stress test program was conducted on transistor, diode, and resistor components of the SN5420. Results of the study are reported in Appendix B. The most significant parameter change was seen in transistor h_{FE} caused by reverse bias stress (both junctions reverse biased). The suspected mechanism of this change is emitter-base diode channeling, caused by the inversion of P type material.

Other less significant parameter changes were observed in components subjected to power dissipation and storage stress. The component parameters, transistor V_{BE} and resistor values, which dominate the equations describing a functional device parameter, were found to be relatively stable during stress.

SECTION IV

RELIABILITY SCREENING

1. INTRODUCTION

A reliability screening procedure for the SN5420 digital NAND gate has been developed as a result of studies conducted during this contract. Three major work elements from which the screening procedure was developed are described below:

1) Circuit analysis was conducted to determine; design factors affecting reliability; the stresses which more nearly approximate circuit applications; define functional parameter failure criteria; and to develop non functional measurement techniques which are more sensitive to degradation than functional measurements. The results of these studies are contained in a previous report [2] and are summarized in Section II.

2) A study of the molybdenum-gold expanded contact system was conducted to define failure modes, their cause and the techniques to predict their occurrence. Refer to Section V for amplification.

3) A high stress test program coupled with failure analysis was conducted. The effectiveness of the techniques derived from circuit analysis and contact studies were demonstrated during the test program. Precapsulation photographs of the devices subjected to stress were used to relate failure mechanisms to visible anomalies which existed on the dies prior to capsulation. Refer to Section III and Appendix D for test and failure analysis results.

The reliability screening procedure is shown in Table 1. It was developed by identifying the failure mechanisms resulting from high stress tests and relating these to information which existed at the earliest point in the manufacturing cycle following the die mounting and lead bonding operations. Two types of failures are not included in the screening procedure, namely emitter flashover and stress errors. These are discussed in Appendix D. These were determined not to be related to use-conditions. The discussion which follows is organized according to the techniques used in the screening procedure shown in Table 1.

2. PRECAPSULATION LOT ACCEPTANCE FOR METAL ADHERENCE

Failures caused by peeling metallization were found to occur with equal probability throughout all intervals of the stress program. Since these failures could not be

discriminantly predicted by visual inspection or electrical measurements, a destructive shear bond strength test performed on a sampling basis is specified. The reject criteria is specified in terms of $\bar{x}$ (average) and R (range) of bond strength distributions. A discussion of the technique and its effectiveness to predict failures is contained in Section V of this report.

3. DIE AND WIRE DRESS

Die and wire dress problems were revealed from constant acceleration stress. Both pre and post capsulation screens are recommended to remove potential failures caused by:

- Wire breakage which occurs above the stitch bond terminal.
- Wires shorting together, to the case or die.

A comprehensive discussion of this problem is contained in Appendix D. Three steps in the screening procedure to remove potential failures are:

- 20 X visual inspection with diffused lighting prior to capsulation. Refer to Figure 10 for a criteria for inspection.
- Constant acceleration in the X Z planes after capsulation followed by topological X-ray. The visual inspection criteria of Figure 10 can be used in conjunction with the X-ray photographs. The following sequence for constant acceleration is recommended: X_1, X_2, Z_1, Z_2. Refer to Appendix Figure D-12 for illustration.
- Constant acceleration in the Y_1 plane.

Analysis of constant acceleration failures, coupled with prestress X-rays indicates 20 percent of potential failures caused by die or wire dress can be detected by 20X visual inspection prior to capsulation. However, figures presented in Appendix D demonstrate how slack wires can be seen by a topological X-ray following constant acceleration in the X and Z planes. The lateral centrifugal force causes wires with high arcs not previously visible from a vertical view to "fold over," revealing an extensive amount of bow in some wires. Thus, constant acceleration in the XZ planes followed by topological X-ray is a very effective tool for removing escapes from the precap inspection.

Constant acceleration in the Y_1 plane is utilized to eliminate devices with stitch bonds formed with too little or too much pressure. The centrifugal force is exerted upward and snaps the narrow neck shown in the figures of Appendix D, or breaks a weak bond between the wire and bond pad. This screen also eliminates potential failures caused by weakly formed ball bonds.

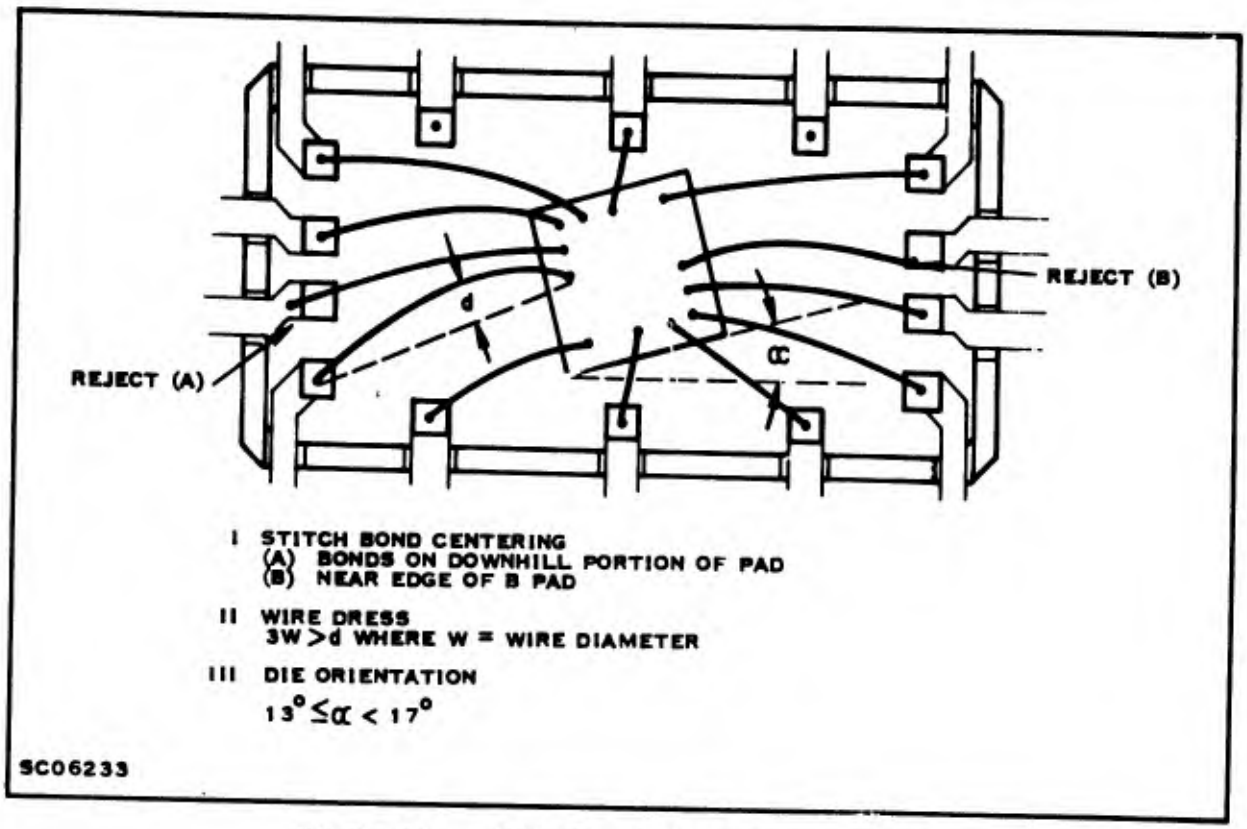


Figure 10. 20X Visual Package Inspection

4. DIE INSPECTION

A 100-percent die inspection screen using 70X direct lighting techniques is specified in the screening procedure. Inspection criteria are outlined in Table 4 of this section; they were developed from analysis of the precapsulation die photographs of devices subjected to the fixed and step stress program. The technique for analysis was briefly summarized in Section II of this report, while the relationships between failures and information which existed on the dice prior to stress is contained in Appendix D.

A summary of cracked die failures is given in Table 5. Note that nine failures were caused by die cracks under bonding pads and that seven of these were visible in the precapsulation photographs. It is believed that the remaining two were present when the photographs were taken, but were hidden by bond wires. Only one crack was found to extend as a result of stress which was 75,000 G constant acceleration. Since the device survived 60,000 G prior to failure, and since no other cracks were observed to propagate into the active region of the dice, the screening procedure requires only rejection for cracks which extend into the active area, defined by the outer periphery of metal or isolation diffusion as shown in Figure 11. It is interesting to note that only 16 percent of dice with cracks would have been rejected by this screening criteria; i.e., 84 percent of dice with cracks did not fail the high stress tests.

Table 4. Precap Visual Screening Procedure for Integrated Circuits (70X Direct Lighting Recommended)

Defect Classification	Reject Criteria
1. Cracked Bars	Cracks extending into active circuit area defined by the outer periphery of metal or isolation diffusion
2. Oxide Defects	Concentric circles in oxide within the active region
	Scratches which intersect contact metallization
	Particulate matter on die surface which could bridge between the minimum width of contact separation
3. Metal Scratches	Scratches which expose molybdenum or oxide and extend greater than 75-percent metal lead width

A summary of oxide defects is given in Table 6. A description of each of these failures is provided in Appendix D. The screening criteria for oxide defects shown in Table 4 were developed on the basis of these failures.

Only one failure caused by scratched metallization occurred during the test program. The scratch extended completely across the metal, exposing molybdenum. However, the precapsulation photographs, taken on devices which did not fail, revealed many severely scratched leads. (Refer to Section V for amplification.) For this reason the inspection criteria for scratched leads shown in Table 4 is specified from qualitative analysis; it is interesting to note that the criteria are less severe than many existing screening specifications for high reliability devices.

The selection of the visual inspection technique, 70X with direct lighting, was determined as a result of the following test. Dies with known faults were photographed at:

- 70X direct lighting, Figure 12.
- 40X diffused lighting, Figure 13.
- 40X oblique lighting, Figure 14.
- 40X direct lighting, Figure 15.

The value of 70X was chosen as it is the maximum magnification at which the full image of the die was encompassed in a single field of view. The 70X inspection with direct lighting was adequate for screening for cracks, oxide pinholes, spurious diffusions, masking misalignment, ball bond placement, metallization scratches, oxide scratches, and peeling metallization.

Table 5. Cracked Dice Failure Modes

Failure Mode	Number Failed	Number Observed in Precap Photo	Comments
1. Cracked Dice			
(a) Under bonding pad	9	7	Two cracks hidden by bond wires
(b) Propagated into active area	1	1	Crack propagated into active area at 75,000 G (survived 60,000 G stress)
(c) Propagated completely across die	1	0	Failed 300° C storage
Total	11	8	

Precap Analysis of Cracked Dice

Classification	Percent Observed
Under bonding pad	11
In active area (isolation diffusion)	5
Pointing toward active area	68
Not pointing toward active area	16
Total	100

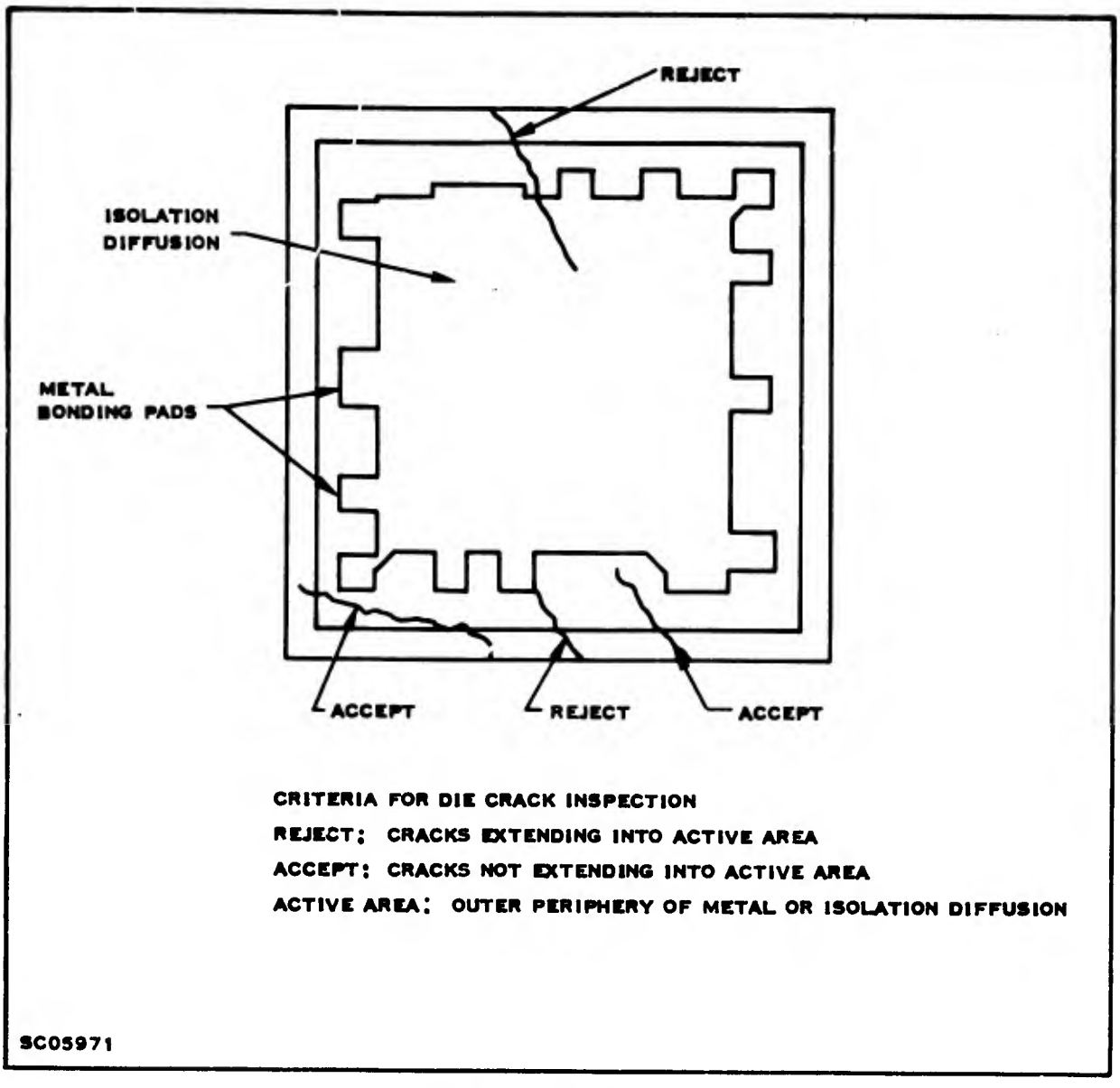


Figure 11. Visual Inspection for Cracked Dice

The 40X inspections with diffused lighting and oblique lighting revealed no information about die faults and gave only limited information about wire dress problems.

5. THERMAL-ELECTRICAL BURN-IN

Electrical stress and high temperature storage have caused several types of failures for which no preindicator of failure was found.

a. Electrical Burn-in

Three oxide pinhole failures under contact metallization were caused by electrical stress (160-200°C for 500 hours maximum). These defects could not be seen prior to failure since they were hidden by contact metal. Failures from other mechanisms

Table 6. Oxide Defects

Failure Mode	Number Failed	Visible In Precap Photo
1. Scratch under metal	1	Yes
2. Spurious diffusion near active area	1	Yes
3. Particulate surface contamination	1	Yes
4. Pinholes under metal	3	No

Precap Analysis of Oxide Defects

Classification	Percent of Dice with Observed Defect
Oxide scratches under metal	5
Spurious Diffusions	85
Particulate surface contamination	10

Figure 12. SN5420 Die Photo-70X Direct Light

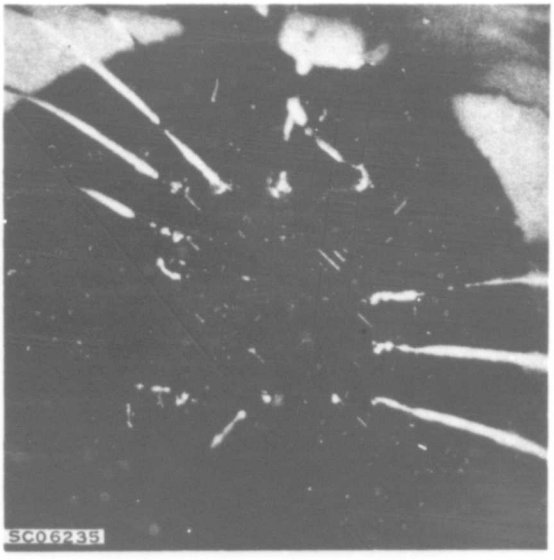


Figure 13. SN5420 Die Photo-40X Diffused Light

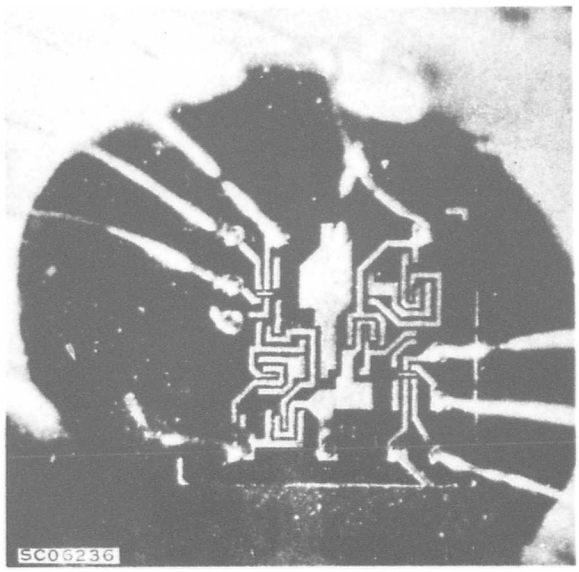


Figure 14. SN5420 Die-photo-40X Oblique Light

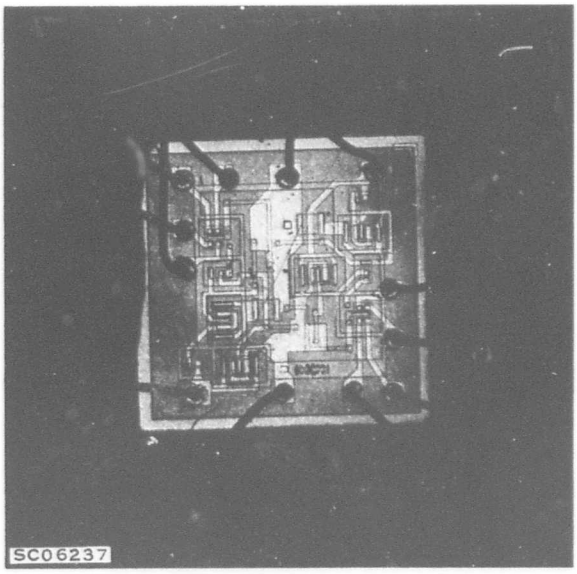


Figure 15. SN5420 Die-photo-40X Direct Light

were caused by electrical stress. However, other screening techniques such as shear bond strength (Level I) and precapsulation die inspection (Level II) are included in the screening procedure for these mechanisms. Two electrical stress circuits which were used in the test program, forward bias and ring counter, are suggested as candidates for screening devices similar to the SN5420. Circuit diagrams of these are shown in Appendix A (Figures A-3 and 4).

b. High Temperature Storage

Three failures were found to exhibit degraded junction characteristics which could not be reversed by baking or removal of expanded contact metallization. It is suspected that degradation of this type is caused by a mask or photoresist defect which leaves a small portion of the base region exposed beneath the emitter lead, which allows a resistive path to develop during stress.

One cracked die failure was caused by 300°C temperature storage for 108 hours. The crack was not visible in the precapsulation photographs and was most probably caused by thermal expansion coefficient mismatch between the die and package material. X-ray analysis indicates that the crack correlates with an "L-shaped" void extending from the edge of the die as shown in Appendix D, Figure D-17.

Six devices were found to degrade on output short circuit current caused by resistor degradation. Several parameters were found to preindicate these failures and are discussed in Section III. The computer program SERF was successfully used to determine the parameters and measurement limits which could be used to preindicate failure from prestress electrical data (Table 7). Five of the six failures would be eliminated by screening as shown in Table 7 .

Howeve SERF is not included in the screening procedure first because the results shown i Table 7 relate to less than 10 percent of the failures and secondly because further wor is needed to demonstrate the limits shown in the table can be used to screen other manufacturing lots.

The critical electrical parameters used to define failures throughout the program are specified in Table A-2. The failure limits assigned to each parameter, were determined by estimating the change in a parameter value necessary to indicate a significant physical change has occurred in the device.[3] These limits are far more severe than those which could be used to define the threshold between performance and nonperformance of a device.

Table 7 . Serf Screening Results

Parameter	Normal Data Sheet Parameter Limits		SERF Program Screening Limits		Percent of Population
	Min	Max	Min	Max	Removed
I_{OS}	25 mA	55 mA		39 mA	10%
T_{ON}		15 ns		8.6 ns	20%
V_{OFF}	2.4 V		2.7 V		10%

6. HERMETIC SEAL

Hermetic seal tests are recommended in Level III of the screening procedure since thin metal films (expanded contacts) are reactive to moisture, solvents or other agents which can be introduced in screening, installation, and operation of the device. Both fine (Veeco or Radiflo) and gross (ethylene glycol or equivalent) are recommended. It should be noted that no failures due to poor hermetic seals were encountered during the test program.

7. COST OF SCREENING

The work of the contract has resulted in a general approach to reliability screening for integrated circuits which consists of three levels. The following discussion uses the basic approach to reliability screening discussed in this section to consider some of the factors which affect screening costs.

Two plans (A and B) for reliability screening are shown in Table 8 which are organized according to the basic procedure (3 levels) developed during the study. Plan A typifies a maximum reliability screening procedure, where cost is considered to be secondary to reliability. Plan B is specified considering the cost effectiveness of screening. In one column is the estimated percent of failures removed by screening, as demonstrated by RADC tests. Similar columns under each of Plans A & B are given and reflect a more general estimate of the effectiveness of each screening step when considering this contract and other sources of reliability data. Total screening costs for Plan A range between $5.50 and $8.00 per device, while Plan B yields $2.10 to $3.60 per device. Not included in these cost estimates are basic device costs, yield loss resulting from screening, and cost of facilities.

Three general areas for discussion of costs are chosen as follows:

a) Costs of performing the screening tests.

b) Direct and indirect impact of screening techniques on total screening costs.

c) Relationships between cost of screening, data analysis, documentation and reporting.

A range of cost is shown in Table 8 for each of the screening techniques since the methods of performing tests may vary according to the user's specification and to the type of device screened. For example, the cost of performing the shear bond strength sampling test is dependent upon the number of bonds to be tested, the type of analysis required, and the number of devices to be handled during the test. The cost of precapsulation visual inspection is dependent upon the inspection criteria and on the size of the die. The costs of electrical burn-in depend on the complexity of the test circuits and equipment checkout and control procedures specified by the user. Another factor affecting the cost of screening is the compatability of the techniques used with existing manufacturing facilities which have been designed to handle larger device quantities. Constant acceleration (X-Z planes) and high temperature storage are examples which significantly increase the cost of screening. Constant acceleration performed in the X-Z plane must be performed on facilities designed to accommodate relatively small quantities. High temperature storage requires that devices be removed from the normal "in-process" carrier fixture since the fixture materials cannot withstand high temperature. The requirement for special handling indirectly affects the costs of other screens such as electrical burn-in, since more costly device handling procedures are incurred.

The requirements for electrical measurements, measurement failure criteria, analysis and reporting affect the cost of screening. Table 9 compares some of the differences between screening plans A and B. In Plan A, electrical measurements are recorded by device serial number four times during the screening procedure. Parameter degradation limits are specified, requiring the use of computers for data reduction and analysis. In Plan B, failure limits are assigned on the basis of absolute values, measurements are not recorded, and the number of electrical measurement intervals is reduced to one-half.

By comparing the relative costs of Plans A and B and relating these to the failures which have been estimated to be eliminated, the cost effectiveness of the screens may be estimated. Using Plan A as a reference, the data of Table 8 indicates that approximately 75% of the failures would be eliminated by Plan B at less than half the cost of Plan A. Failures not eliminated by Plan B are those affected by high temperature storage and constant acceleration (XZ planes) screens and by the measurement degradation failure criteria included in Plan A. Failure mechanisms affected by the

Table 8. Cost of Screening

Screening Level	% Total Failures Removed-Demonstrated By Test Program	Alternative Plans For Screening			
		Plan A (Maximum Reliability		Plan B (Minimum Cost)	
		Estimated % Failures Removed	Estimated Cost To Screen 1000 Devices	Estimated % Failures Removed	Estimated Cost To Screen 1000 Devices
I. Precapsulation Lot Acceptance					
• Shear Bond Strength	15	14%	$100 to 200	14%	$100 to 200
II. Precapsulation Visual Screen					
• 20 X Package Inspection	17	16%	$100 to 300	16%	$100 to 300
• 70 X Die Inspection	17	16%	$100 to 300	14%	$100 to 300
III. Postcapsulation Screen					
• Hermetic Seal	--	5%	$300 to 400	5%	$300 to 400
• Constant Acceleration (X-Z) Followed by X-ray	19	17%	$500 to 600	(Not Specified)	
• Constant Acceleration (Y_1)	15	14%	$300 to 400	14%	$100 to 200
• High Temperature Storage	12	5%	$300 to 400	(Not Specified)	
• Electrical Burn-in	5	12%	$500 to 1000	12%	$300 to 600
• Hermetic Seal	--	1%	$300 to 400	1%	$300 to 400
Electrical Measurements Data Reduction & Analysis, Final Report			$3000 to $4000 (Four Electrical Measurement Intervals)		$800 to $1200 (Two Electrical Measurement Intervals)

Table 9 . Requirements For Testing, Data Analysis and Reporting

	Plan A* (Maximum Reliability)	Plan B* (Minimum Cost)
1. Unit Identification	Device Serialization Required	Device Serialization Not Required
2. Parameter Failure Criteria	Degradation Limits Similar to Criteria For Test Program.	Absolute or Data Sheet Limits Only
3. Measurement Error Control	Measurement Control Samples Required (Refer to Section III)	Normal Equipment Maintenance and Calibration Procedures Only
4. Data Analysis	Computer Analysis to Define Degradation Failures	Lot Traveler to Record Quantity Surviving each Screening Step
5. Reporting	Formal Report including data history - Storage of Data for Permanent Record	Certificate of Compliance to Specified Procedure
6. Number of Electrical Measurements Intervals	Parameters Measured Four Times	Parameters Measured Two Times

* Reference Table 8.

screen tests, photolithographic faults, resistor degradation and die-wire dress, are probably the ones least likely to occur at use conditions. The reader is referred to previous discussions of this section and to Appendix D for discussions of these failure modes. For example, failure mechanisms caused by photolithographic faults were not encountered during electrical stresses conducted for as long as 2000 hours.

8. CONTRACT EXTENSION

During an extension to the contract, the reliability screening procedure shown in Table 1 and discussed previously in this section will be evaluated. Devices will be processed by production in the normal manner up to capsulation. Here a departure from the normal processing will be taken where special techniques consisting of shear bond strength measurements and precapsulation photographic analysis will be used to predict failure. After capsulation the devices will be subjected to a high stress program consisting of two parts, burn-in and reliability demonstration. Both high temperature storage (168 hr.) and electrical stress (168 hr.) will be used. The effectiveness of burn-in will then be demonstrated by tests consisting of storage, electrical and constant acceleration stresses.

Two computer programs, SERF and LINDA, developed for the RADC programs will be used for analyzing the results of the testing program. The SERF program will be used to isolate electrical parameters which are preindicators of failure and to develop nondestructive screening procedures for eliminating the less reliable devices in a production lot. The LINDA program will enable linear discriminant functions to be developed which will allow the classification of devices into the categories of more and less reliable devices.

Certain nonelectrical defects of the SN5420 such as scratched lead patterns and KMER defects will be identified and it will be determined if these defects are indicative of later failure under accelerated testing. Photographic analysis will reveal certain types of defects, the location of which will be recorded. An attempt will be made to see if a particular type of defect and location of defect are preindicators of failure.

SECTION V

CONTACTS AND INTERCONNECTIONS

1. INTRODUCTION

The molybdenum-gold expanded contact system is currently utilized in integrated circuits by Texas Instruments. The bimetal system is frequently referred to as the solution to "purple plague" associated with aluminum-gold system and has been shown to offer the following advantages: [6]

There is negligible solubility between gold and molybdenum and molybdenum and silicon.

No intermetallic compounds are formed between the metals, therefore, the system is metallurgically stable.

Gold is corrosion resistant and inert.

The system is an excellent electrical conductor, and good ohmic contact to highly doped silicon can be made.

The adherence to the thermally grown oxide substrate is excellent.

Gold wire is easily and reliably bonded to molybdenum-gold films.

The system is difficult to open by scratching due to the hard underlayer of molybdenum.

This study was conducted to (1) more clearly define the merits of the system and (2) determine the applicable failure modes, their cause, and the techniques to predict their occurrence.

2. TEST VEHICLE

The SN5420 Integrated Circuit was selected as the test vehicle for the study which was conducted to parallel the test program. Test samples were selected from the same manufacturing lots represented by devices used in the test program, and in most cases,

the studies were conducted on the actual devices used in the test program, including the Preliminary Investigation, Step Stress Series, Fixed and Step Stress Series, and Component Evaluation.

The contact system is represented in Figure 16. This drawing represents the situation in which two thin metal films are applied in such a way that the bottom layer (molybdenum) contacts silicon through an etched hole in the surface oxide and expands out over the oxide. The second film (gold) is applied directly over the molybdenum and is completely isolated from the silicon and oxide. A gold lead is attached by a thermo-compression ball bond. Data on the system under study are given below:

a)	Metal deposition method	evaporation
b)	Silicon-metal contact area	0.5×10^{-6} in^2
c)	Silicon oxide thickness under interconnect metal.	3000 - 5000 Å
d)	Metal width and thickness (moly-gold) . . .	0.4 mil (width) Mo — 13 μin Au — 26 μin

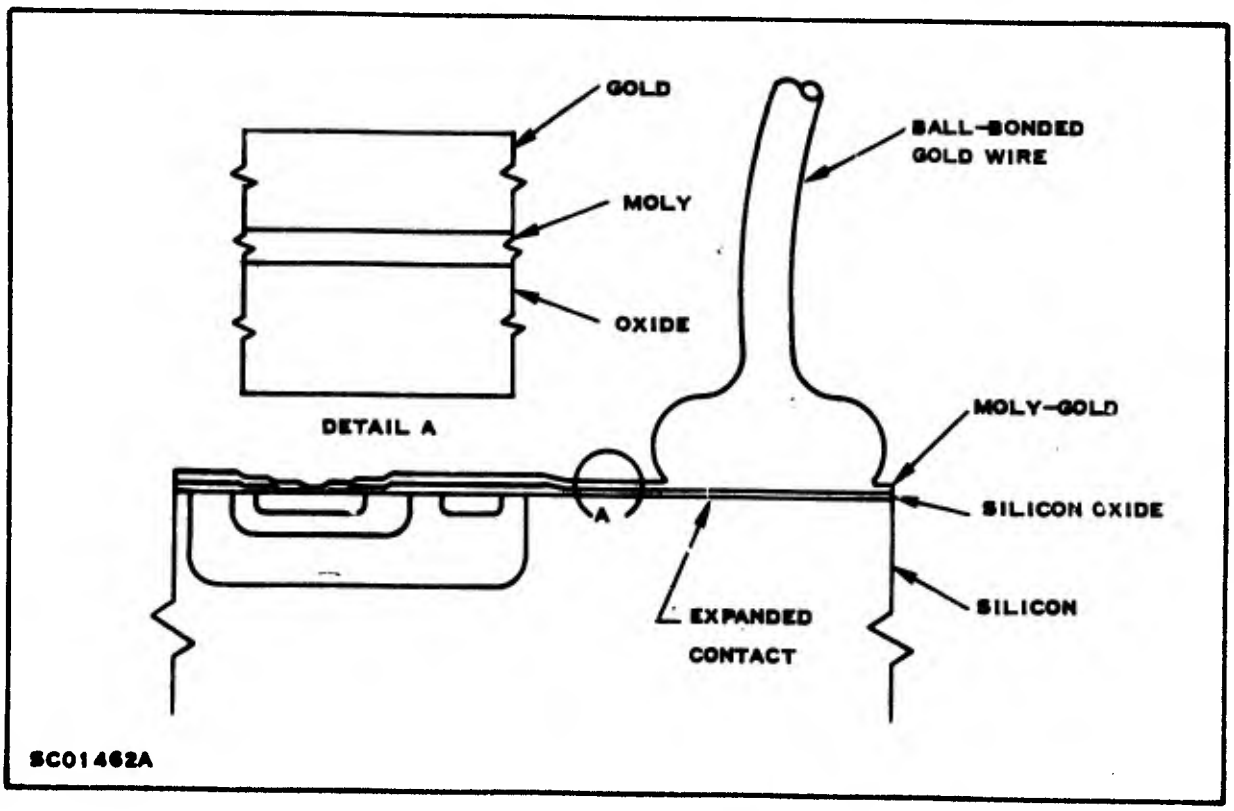


Figure 16. Sectional View of Moly-gold Interconnect System Used for Monolithic Integrated Circuits

e) Gold wire diameter . . . . . 0.7 mil

f) Approximate ball and contact area with moly-gold . . . . . 6×10^{-6} in^2

3. SUMMARY OF RESULTS

The silicon-metallization interface was studied for contact resistance degradation following a series of electrical and thermal stresses. The emitter-base junction of a transistor in the circuit was characterized at two dc current levels at periodic intervals during the test program. Increases less than 1% in contact resistance were observed through 350°C, while increases less than 7% were observed through 400°C stress. These results are supported by analyses of failures from the test program where resistive contacts were never encountered.

A study was performed to evaluate voids, thin spots, scratches and metallization resistance degradation by high thermal and electrical stresses. Studies performed at 400°C followed by electrical parameter measurements and metallurgical cross sections did not reveal the presence of voids in molybdenum which would have been indicated by the formation of gold silicon eutectic. Four-point probe resistance measurements of metallization, including metal over oxide steps, showed only slight increases (5 to 10%) to result from stresses through 400°C.

A study was conducted to investigate jointly bond strength and metallization adherence. A technique to measure shear bond strength was used to evaluate samples representative of different production periods, and the effects of temperature storage, impact shock, thermal shock and constant acceleration on bond strength. No significant degradation occurred as a result of the high stress tests. However, bond strength and metallization adherence was found to be highly lot dependent. A correlation between measured bond strength, the modes by which the bonds separated, and the incidence of failures due to peeling metallization on the test program was determined.

4. TECHNICAL DISCUSSION

The study was divided into three parts: silicon-metal interface, metal topology, and bond strength-metal adherence.

a. Silicon — Metal Interface

Devices used in the component evaluation discussed in Appendix B were selected to study the effects of high electrical and thermal stress on silicon metal interface resistance. The emitter base junctions of sixty transistors were forwarded biased and characterized at two dc current levels 0.5 and 5.0 mA, at periodic intervals during the stress program. Refer to Table B-1 of Appendix B for description of the stresses used.

No silicon contact resistance degradation was noted during any of the electrical stress tests. The results of storage step stress conducted through 400°C are presented in Figure 17. Data is plotted as percent variation of the difference in V_{BE} at the two current levels, 0.5 and 5.0 mA. The method of calculation is shown below:

$$\% \text{ Var. } \Delta V_{BE} = \frac{\Delta V_{BE}\left(\begin{matrix}\text{nth}\\ \text{interval}\end{matrix}\right) - \Delta V_{BE}\left(t = o\right)}{\Delta V_{BE}\ t = o} \times 100$$

where

$$\Delta V_{BE} = V_{BE}\left(5.0\text{ mA}\right) - V_{BE}\left(0.5\text{ mA}\right)$$

Tests conducted through 300°C did not produce variations in ΔV_{BE} greater than that attributed to measurement error, established by the control samples to be less than one percent. For a discussion of control samples to establish the measurement error of experiments the reader is referred to Section III of this report. A slight increase in the median value of ΔV_{BE} (approximately 4%) was observed following the 400°C stress interval. The first conclusion to be drawn would be contact degradation; however, the photomicrographs discussed in Section IV of this section shows the gold-molybdenum-silicon interface structure for an emitter contact of a device subjected to 300 - 400°C storage step stress for 540 hours had no visual indication of contact degradation.

Further, the components which demonstrated the ΔV_{BE} increase also decreased on h_{FE} between the 300°C and 400°C stress intervals. For more discussion the reader is referred to Appendix B of this report. The data suggests the presence of a mechanism which produces the following effects in silicon [7].

- Increased Resistivity
- Lowered Carrier Lifetime and Emitter Efficiency.

The suggested mechanism is gold migration into the emitter region after the gold-silicon eutectic (377°C) is exceeded.

b. Metal Topology Analysis

Devices subjected to the Fixed and Step Stress Series of the test program were studied. The three areas of investigation were metallization resistance, visual analysis, and microsections.

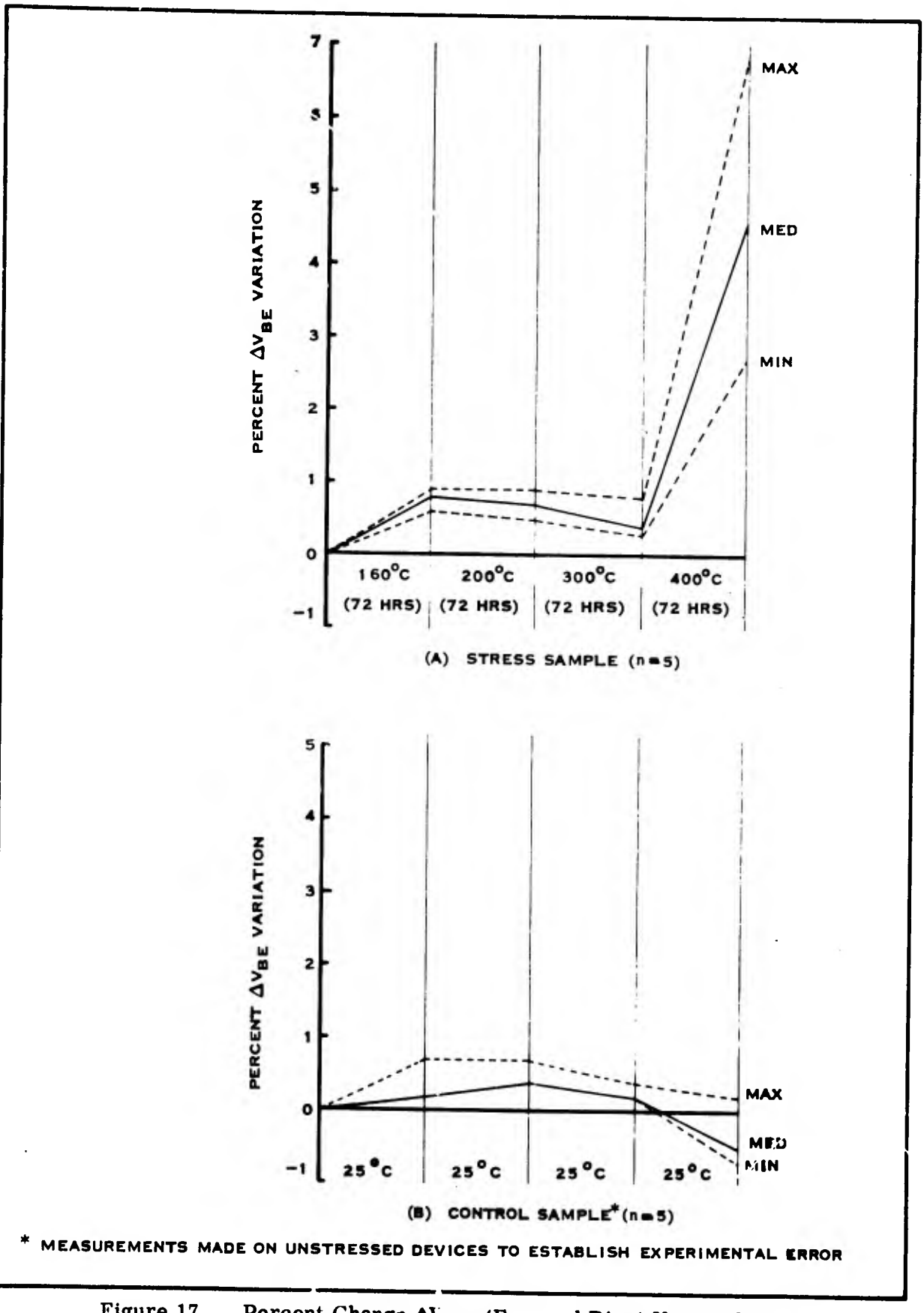


Figure 17. Percent Change ΔV_{BE} (Forward Bias) Versus Stress

(1) Metallization Resistance

Four-point probe resistance measurements were made prior to encapsulation and stress on 30 devices. A control sample (ten devices) not subjected to any stresses was used in the evaluation. Measurements were repeated following the stress program. The devices studied and the stresses to which they were subjected are shown in Table 10.

Table 10. Contact Resistance Measurement Study Conducted on Devices from Fixed and Step Stress Series

Device Serial Numbers	Stress Conditions
245	Forward Bias Life 160°C - 1000 Hr.
274, 275	Forward Bias Life 180°C - 1000 Hr.
304, 305	Forward Bias Life 200°C - 1000 Hr.
334, 335	Forward Bias Life 220°C - 1000 Hr.
161, 162	Storage Step Stress - 300°C, 325°C, 350°C, 375°C, 400°C - 108 Hr/S
181, 182	Storage Step Stress - 300°C, 325°C, 350°C, 375°C, 400°C - 108 Hr/S
201, 202	Storage Step Stress - 300°C, 325°C, 350°C, 375°C, 400°C - 108 Hr/S
221, 222	Storage Step Stress - 300°C, 325°C, 350°C, 375°C, 400°C - 108 Hr/S
481, 482, 483	Storage Life Test 300°C - 1000 Hr.
511, 512, 513	Storage Life Test 325°C - 1000 Hr.
541, 542, 543	Storage Life Test 350°C - 1000 Hr.
571, 572, 573	Storage Life Test 375°C - 1000 Hr.
361, 363	Ring Counter Life 160°C - 1000 Hr.
391	Ring Counter Life 180°C - 1000 Hr.
	Control Samples

A description of the measurement technique follows: A constant current of 10 mA was passed from external pin 2 to point "a" shown in Figure 18. Current was monitored continuously with a Hewlett Packard 412 Ammeter. Separate voltage probes were used with a Fluke precision voltmeter at points "b", "c", "d", "e", and "f" of Figure 18. These measurements allowed the calculation of resistance over a flat section of lead, the oxide step, and the bond to silicon interface. The point at which the probe was placed on the bond pad was found critical to the magnitude of the voltage measurement between the bond and bonding pad. For this reason, a description of the probe measurement technique should be mentioned here. First, the voltage probes were placed with the aid of a microscope and it was impossible to place the probe for post test measurements in the exact location of the pretest measurements. Secondly, the distance between the probes for each set of readings was recorded and for analysis purposes the measured resistance was divided by the distance between the probes to obtain an equivalent resistance per unit length value.

Results of the four point probe resistance measurements are shown in Figure 19 and 20, and Table 11. Data is plotted for two ranges of temperature stress, 160° - 220°C (Thermal-electrical) and 300° - 500°C (storage only). Control samples were used in the experiment.

Accuracy of the probe measurement technique was found to decrease in proportion to the distance between measurement probes. A summary of the variance in measurements made on control samples is shown in Table 12. The greatest error occurred in the measurements taken between the ball band and bonding pad (0.2 mil); the least, in measurements taken over the longer lengths of flat metal (4.0 mil). For this reason, resistance change as a function of stress could not be accurately determined. However, the following observations are significant

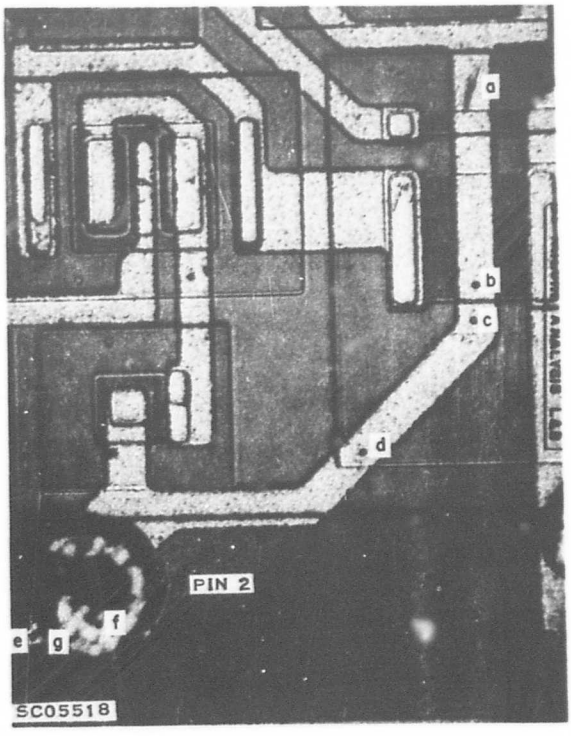


Figure 18. Diagram of SN5420 Metal Contact Pattern

Table 11. Analysis of Metal Resistance Measurements

Sample Size	Portion of Metal System Evaluated	Initial Values (Ohms/Inch)			Percent Change (%)		
		Minimum	Median	Maximum	Maximum Decrease	Median Change	Maximum Increase
	I. Metal Length						
10	1. 160°C - 200°C Stress	26	33	39	-38	-08	+17
20	2. 300°C - 400°C Stress	23	31	34	-29	+04	+59
10	3. Control (No Stress)	25	29	35	-18	-02	+19
	II. Oxide Step						
10	1. 160°C - 200°C Stress	29	36	76	-38	+05	+24
20	2. 300°C - 400°C Stress	18	42	56	-50.5	+09	+69
10	3. Control (No Stress)	30	39	49	-42	-12	+26
	III. Ball Bond to Metal Pad Interface						
10	1. 160°C - 200°C Stress	0.2	1.7	13.2	-99	-30	+197
20	2. 300°C - 400°C Stress	0.4	2.0	15.9	-93	-72	+318
10	3. Control (No Stress)	0.8	1.2	10.0	-92	-59	+66

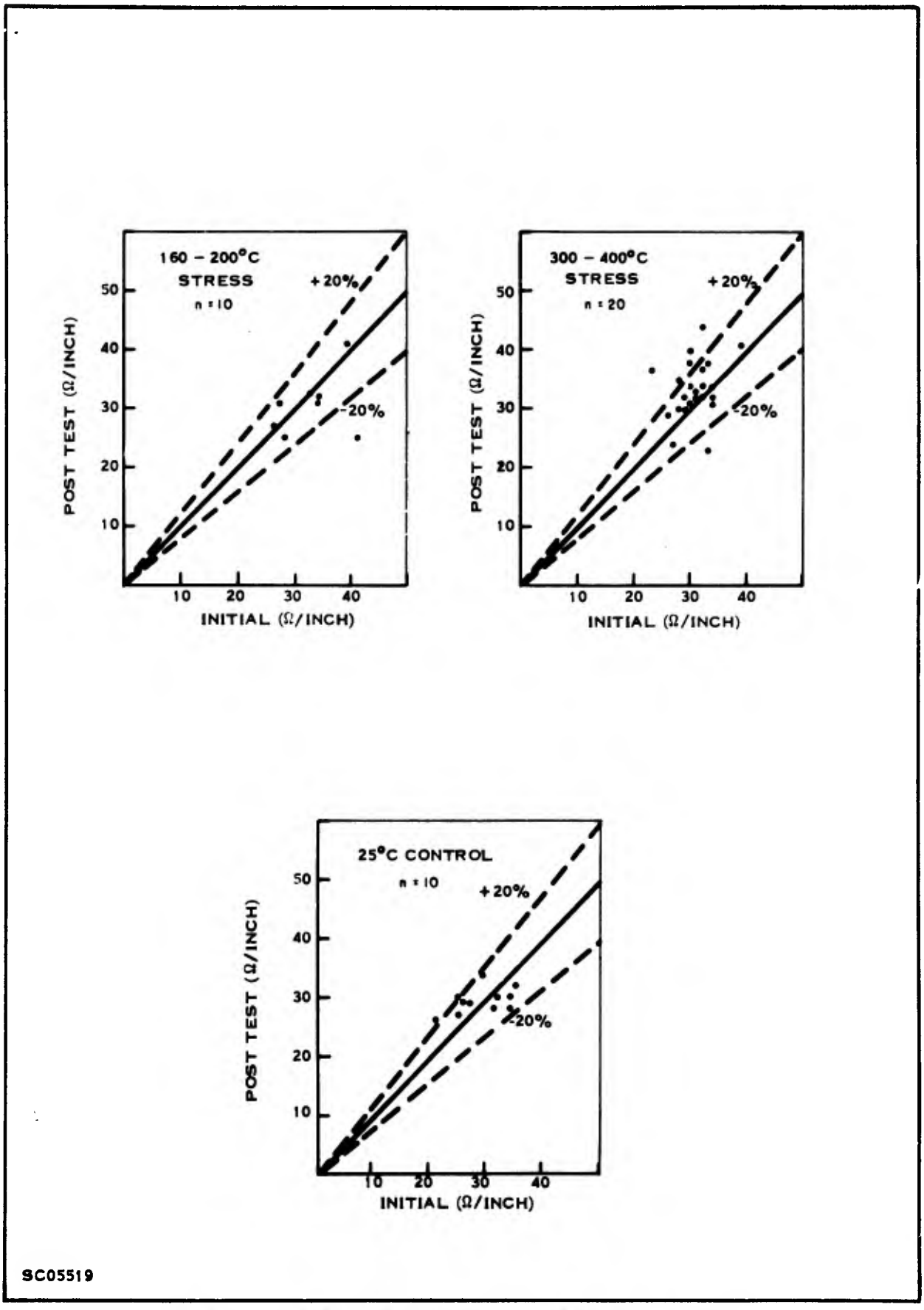


Figure 19. Scatter Plots of Metallization Resistance Measurements Initial Versus Post Stress for Metal Length

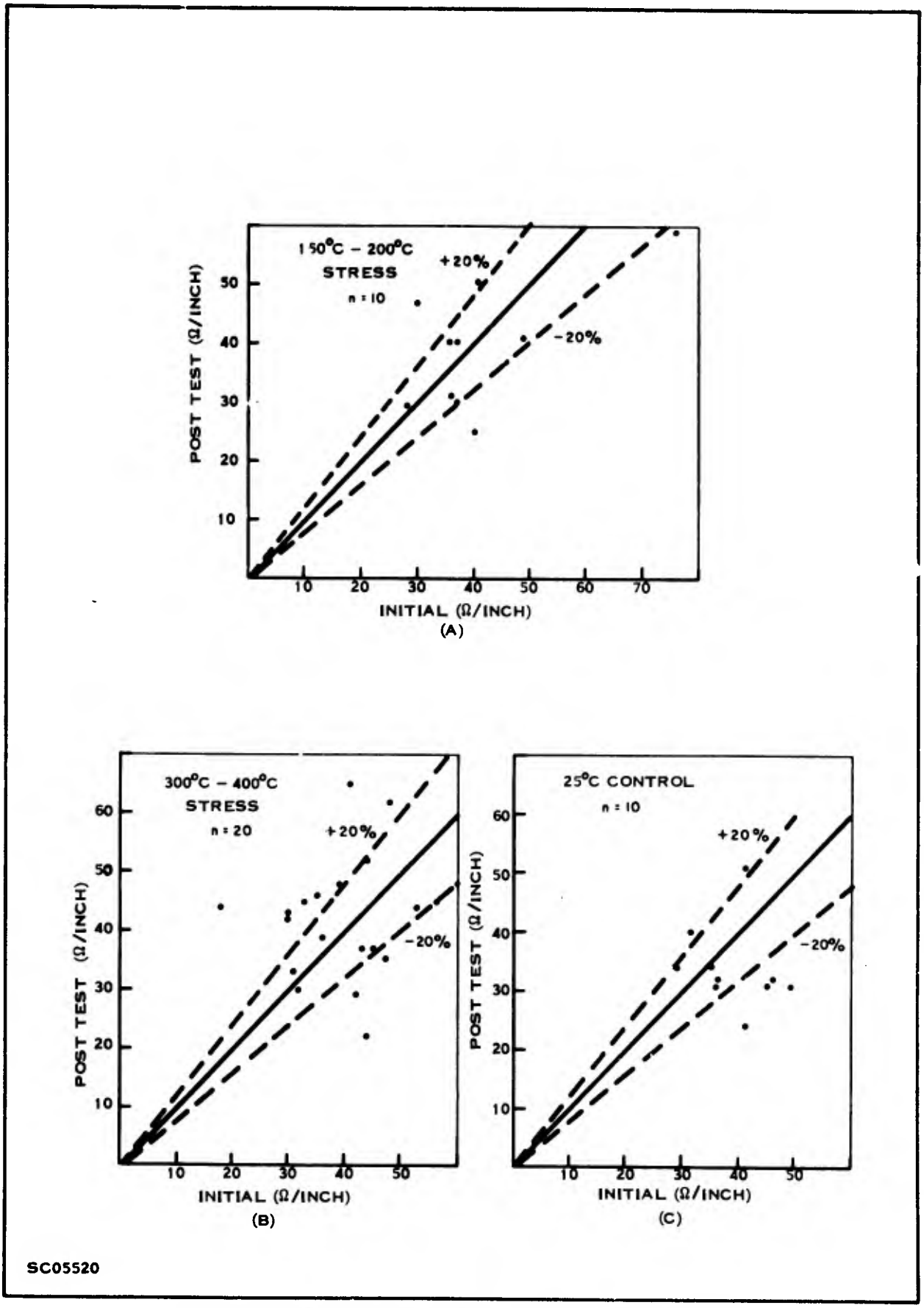


Figure 20. Scatter Plots of Metallization Resistance Measurements Initial Versus Post Stress for Oxide Step

- Analyses of median variations for flat metal lengths and oxide steps indicates a five to ten percent increase in resistance occurred from stresses in the 300° to 400°C range.

- One device subjected to 300°C storage was found to be a failure according to the parameter criteria established in the test program. Peeling metallization caused this failure which showed the maximum increase in bond-to-pad metallization resistance (318% increase indicated in Table 11). Data taken on the flat metal length and over oxide step of this device were well within the maximum variations observed in metal lengths and oxide steps. Hence peeling metallization caused this apparent increase in resistance. For further information concerning peeling metallization refer to Appendix D.

This study indicates that further investigation of metallization resistance by thermal and electrical stress is warranted. It is suggested, however, that special structures be used with permanently attached electrical connections for current control and voltage measurements.[8] This approach will reduce significantly the experimental error associated with studies of this type.

Table 12. Variance in Metal Resistance Measurements as a Function of Metal Length

Portion of Metal Measured	Typical Distance Between Probes	Range of Percent Change Observed in Control Samples (Refer to Table 11)
1. Flat Length	4.0 mil	37%
2. Oxide Step	1.0 mil	68%
3. Ball Bond to Pad	0.2 mil	158%

(2) Visual Analysis of Metal Surface

Fifty devices were subjected to a 200X microscopic topological analysis prior to capsulation and stress. A search for voids, scratches and thin spots in the metal system was conducted and the anomalies photographed. The devices were re-photographed after completion of the stress program. No evidence of voids or thin spots was indicated from the visual analysis. Four devices with metallization scratches were located, photographed, and subjected to high temperature electrical storage tests including 375°C storage for 1000 hours. None of the devices failed the high stress test. Analysis of the metal scratches following the stress program indicated no further deterioration occurred. The pre and post stress photographs of the device subjected to 375°C storage are shown in Figure 21.

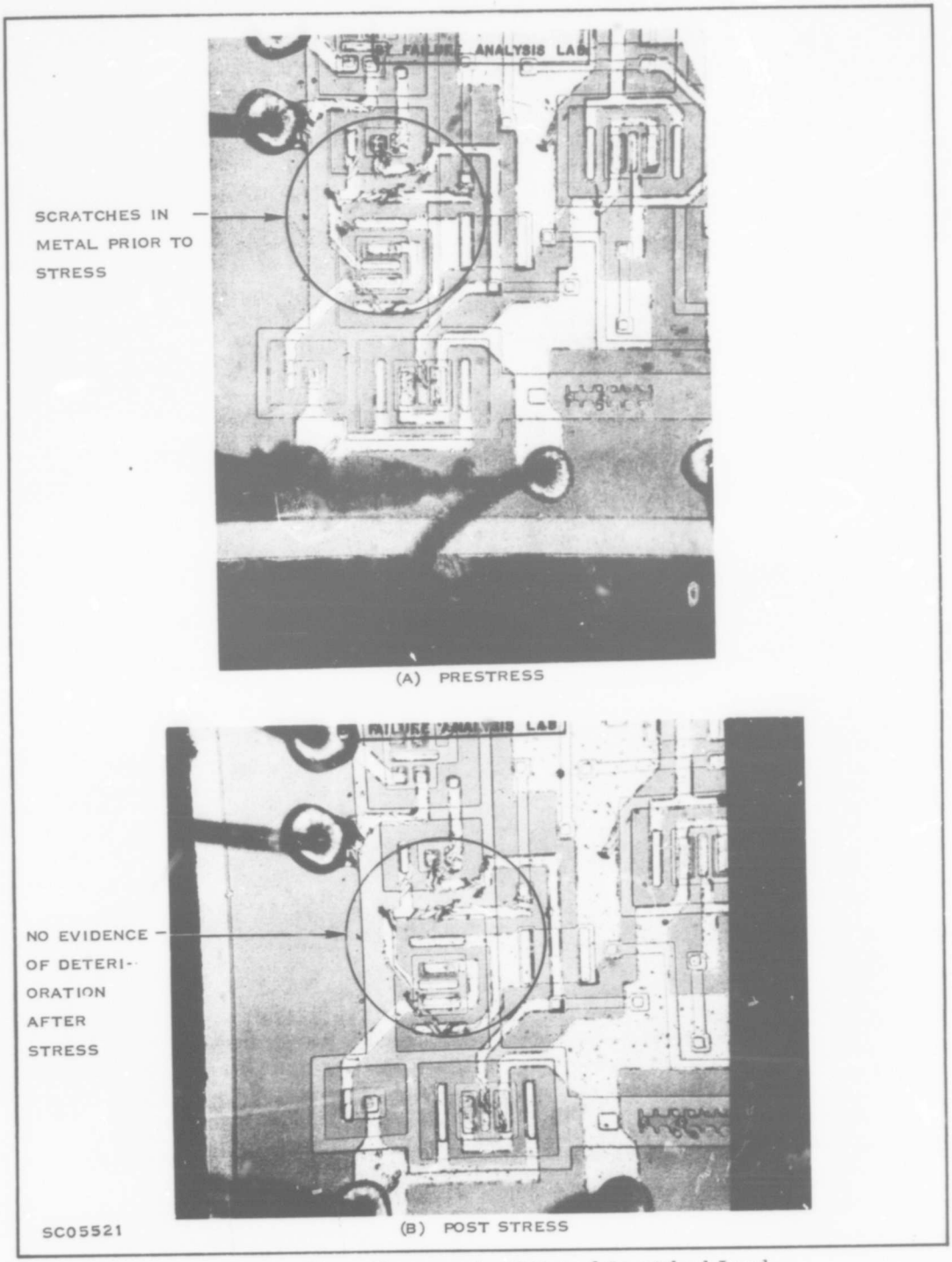


Figure 21. Photographs (200x) of Scratched Lead Before and After 375° Stress for 1000 Hrs.

(3) Metallurgical Cross Sections

Cross sections of the gold-molybdenum-oxide interfaces were made on three devices following high temperature storage at temperatures between 300°C and 500°C. The results are summarized below:

a) 300°C storage for 1000 hours (Figure 22A). No anomalies in the contact system were observed in the metallurgical section.

b) 300 - 400°C storage step stress for 540 hours (Figure 22B). No anomalies in the contact system were observed in the metallurgical section.

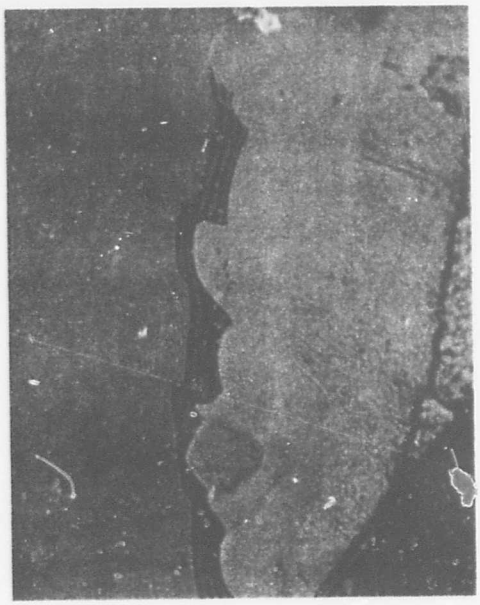
c) 300 - 500°C storage step stress for 540 hours (Figure 22C). Gross, deep invasion of the silicon by the contact metallization in many places. A large part of the total contact area was strongly discolored.

All of these devices had previously been subjected in production to temperatures of 465°C for approximately 30 minutes during the die mounting process. A cross section of a gold wire bonded to moly-gold is shown in Figure 23. The device was subjected to 400°C storage for 540 hours prior to the section analysis. No visual evidence of degradation between the bond to metal interface is indicated.

c. Bond Strength and Metal Adherence

For this evaluation samples from the three replicates of the test program were evaluated. The study was divided into two parts; (a) evaluation of bond strength before and after high stress tests, and (b) an analysis of the bonds and metal systems of samples taken after performing the three replicates of the test program.

For this study, a technique to evaluate shear bond strength was developed and used throughout the investigation. A lateral force was applied to each bond with a steel probe attached to a Scherr Tumico Dynamometer. The gram force necessary to cause bond separation was recorded. The technique has advantages over the classical "vertical pull" technique in that the force required to separate each bond can be determined.



A. 300° C STORAGE/1000 HOURS

B. 300° – 400° C STORAGE STEP STRESS/540 HOURS

C. 300° – 500° C STORAGE STEP STRESS/540 HOURS

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Figure 22. Contact Metal to Oxide Cross Section for Samples Subjected to High Temperature Storage

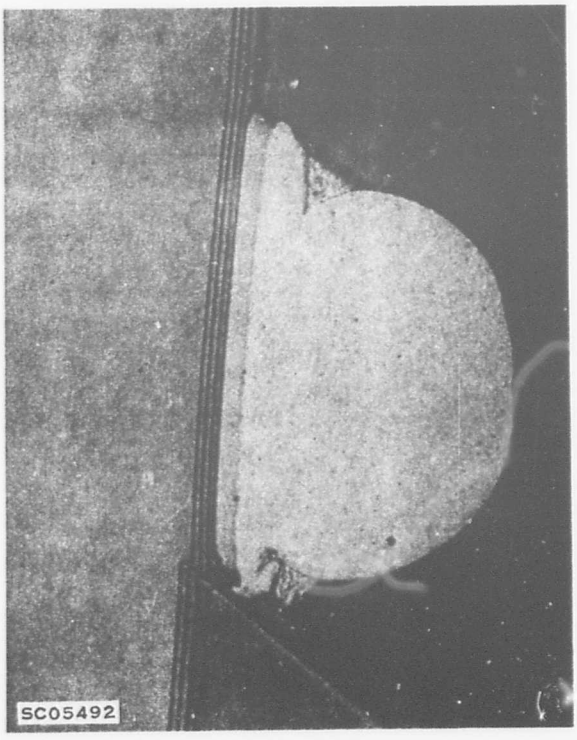

Figure 23. Cross Section of Gold Ball Bond to Metallization Interface Following 400°C Storage for 540 Hours

Vertical pull techniques normally result in wire breakage immediately above the ball bond, thereby eliminating a true measurement of bond strength. The tensil strength of 0.7-mil gold wire is estimated to be approximately four grams, while the mechanical strength of a gold bond to moly-gold interconnect system has been domonstrated from shear tests to be greater than 50 grams in many instances.

(1) Effects of High Stress Tests on Bond Strength

To investigate the effects of various stresses on bond strength, a series of high stress tests were performed on a sample of devices taken from the same manufacturing lot as the devices subjected to the Fixed and Step Stress Series.

Details of the stresses are outlined in Table 13. The shear bond strength technique was used; six of the twelve bonds on each device were sheared prior to stress, the remaining six after stress. Control samples which were not stressed were used to detect the presence of measurement error in the evaluation.

Table 13. Test Plan for Bond Strength Evaluation

I.	High Temp. Storage (500 hours)	Sample Size
	A. 200°C	7
	B. 300°C	6
	C. 350°C	6
	D. 400°C	6
II.	Thermal Shock	
	200°C to -65°C (50 cycles)	6
III.	Impact Shock	
	3000 G, 0.2 ms 50 blows	
IV.	Constant Acceleration Y_1 Orientation	
	A. 10 KG	5
	B. 30 KG	5
	C. 60 KG	5
	D. 100 KG	5

A shear force is applied to six (6) bonds on each unit before stress.

After stress the remaining six (6) bonds are subjected to shear.

The Kolmogorov-Smirnov[9] two sample analysis technique was used to compare the before - after bond strength distributions. This test determines within specified bounds of statistical error whether the two samples are representative of the some general population. Stress is assumed to cause change in bond strength if two populations are indicated by the analysis. The possible effects of measurement error are neutralized by data taken on control samples not subjected to stress.

To evaluate a particular stress, the range of measured bond strengths is divided into a collection of 20 cells for each of the two data sets. The number of bond strengths in each cell range is determined. This information may be conveniently represented in histogram form as in Figure 24 through 26. Next the cumulative percent of the bond strengths less than or in a particular cell range is calculated for each cell. The cumulative percents for the two data sets are compared, cell by cell, and the maximum percent difference noted. These maximum percent differences are summarized in Table 14. The maximum "allowable" percent difference, based on the 0.05 level of statistical significance is also shown in the table; this value changes as a function of the sample size, in this case the number of bonds sheared. Observed percent differences which are above the maximum allowable level indicates that a change in bond strength has occurred as a result of stress.

The Kolmogorov-Smirnov test indicates a significant difference in the bond strength distributions before and after thermal shock and constant acceleration stress. (Refer to Figures 25 and 26.) This change cannot be attributed to stress, however, since the distributions of the initial and final control sample bond strengths are also significantly different, even though the control sample was not stressed. Possibly there was an error in the post stress measurements. Applying the Kolmogorov-Smirnov two sample test to the post stress data and the final control sample data shows that the distributions are not significantly different, indicating that stress did not affect the bond strengths. This information is summarized in Table 15. Again using the Kolmogorov-Smirnov test, there is not any significant difference in the bond strength distributions of the pre and post high temperature storage tests nor in the initial and final control sample bond strength distributions, indicating that stress has not affected the bond strengths. This information is given in Table 14.

(2) Relating Bond Strength to Reliability

In addition to the work described above, samples from each of the three Main Test Program replicates were evaluated for bond strength and metal adherence. The purpose of this evaluation is to determine any difference in the strengths of devices representative of different production periods, and to compare the bond strength data with the failure modes determined from stress failures. Histograms of shear bond strength are shown in Figure 27 for the Preliminary Investigation, Step Stress Series, and Fixed and Step Stress Series. In addition a visual analysis was performed to determine the modes of bond separation; gold film left adhering to molybdenum gold film peeling from molybdenum and adhering to the separated ball bond; and bonds which separate with silicon attached. These results were related to those of high stress tests of the main test program , conducted on devices from the same manufacturing lots. Refer to Table 16 where bond strength data in terms of minimum, maximum and median strength for each sample is related to the modes of bond separation and to the incidence of peeling metal and ball bond failures determined from the test program.

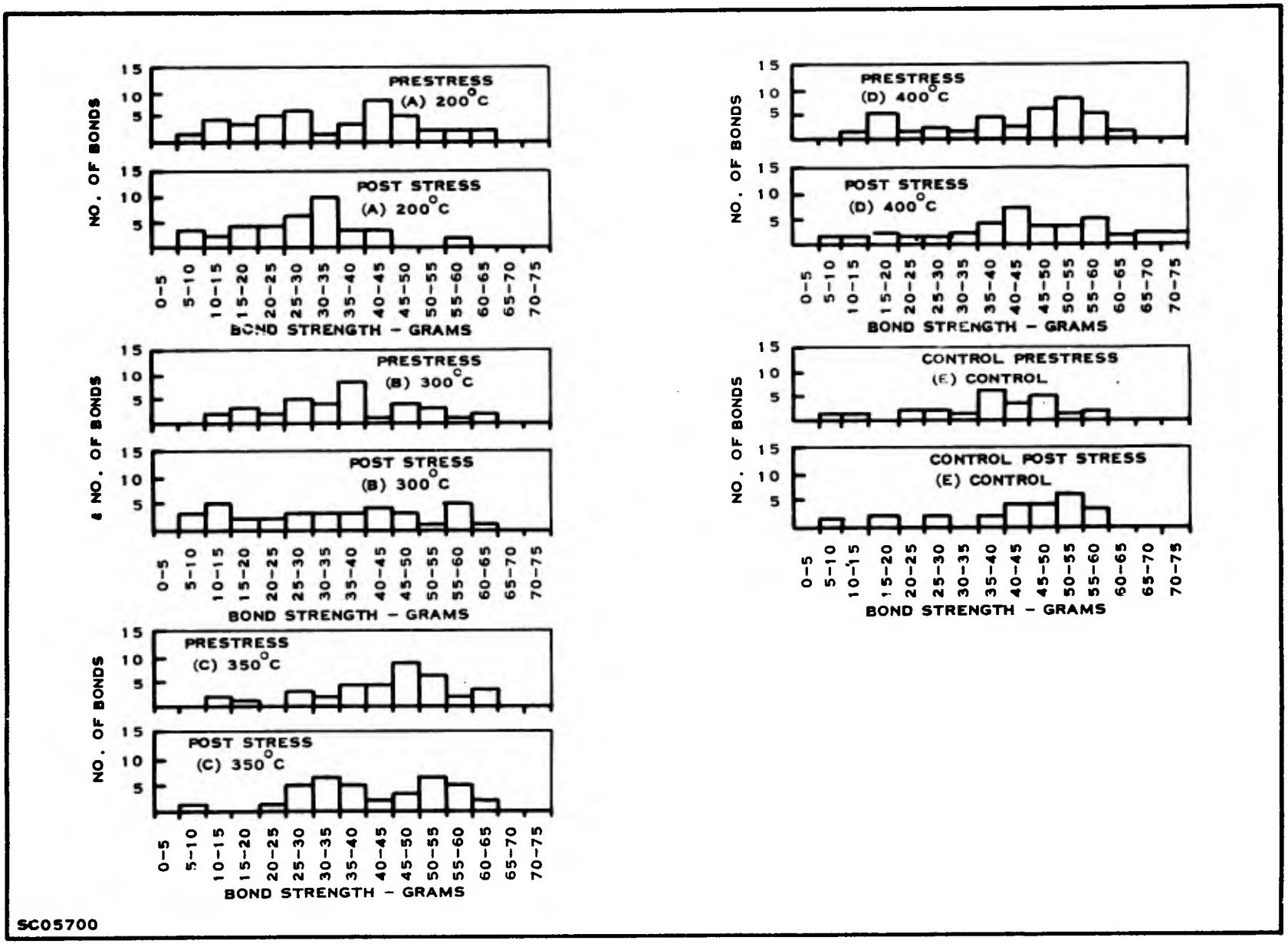

Figure 24. Comparative Histograms of Bond Strength before and after High Temperature Storage for 500 Hours

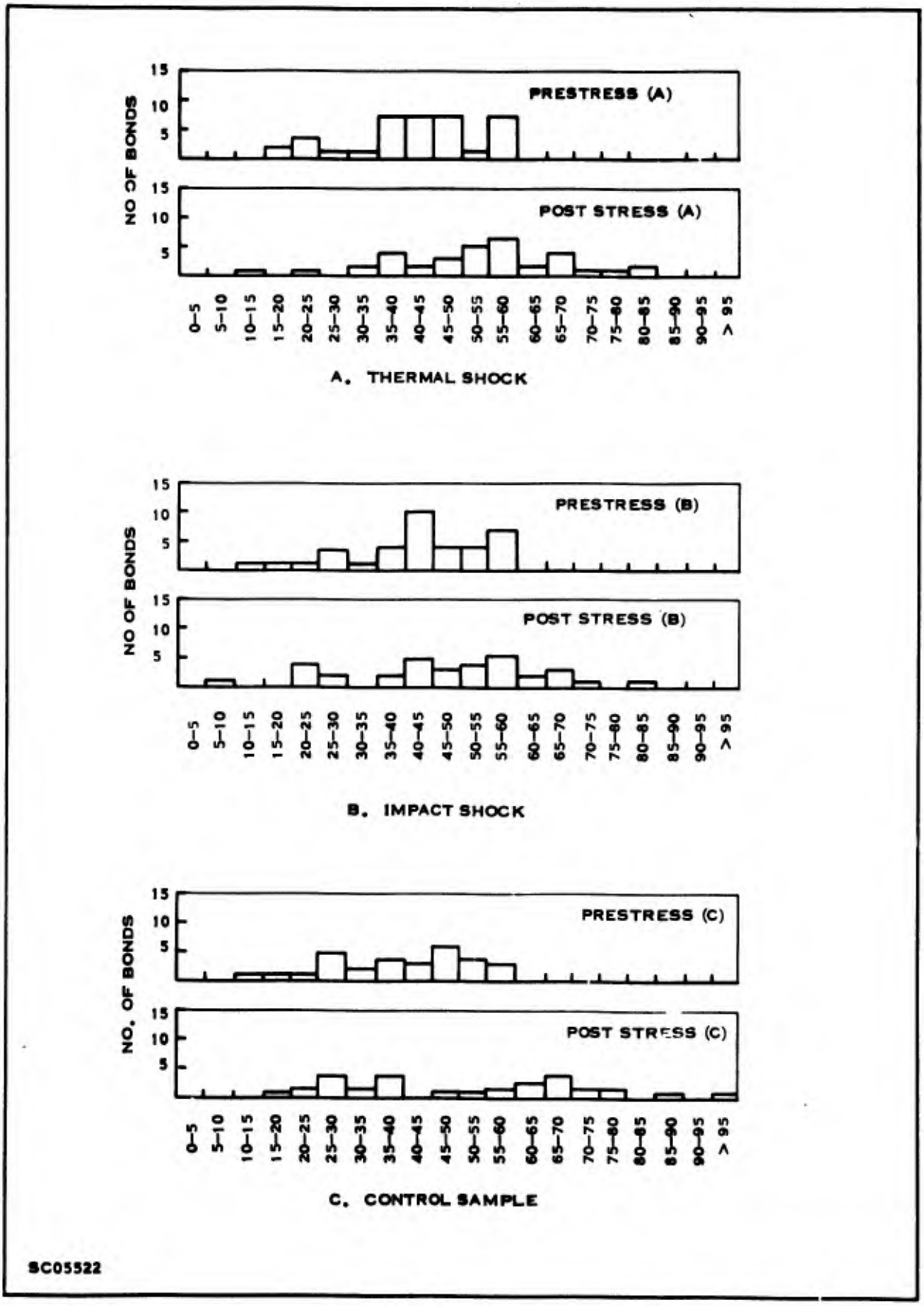

Figure 25. Comparative Histograms of Bond Strength before and after Thermal and Impact Shock

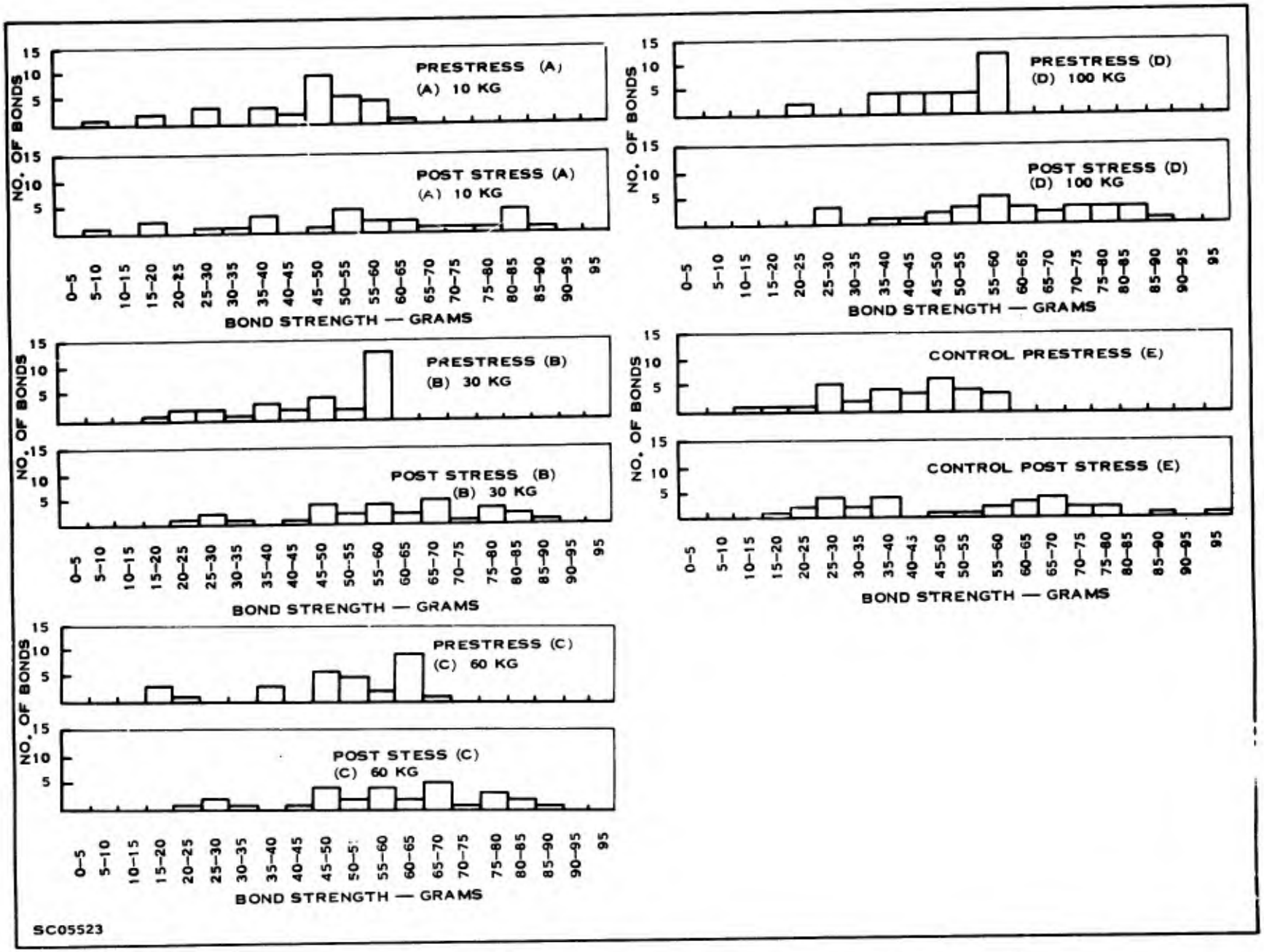

Figure 26. Comparative Histograms of Bond Strength before and after Constant Acceleration

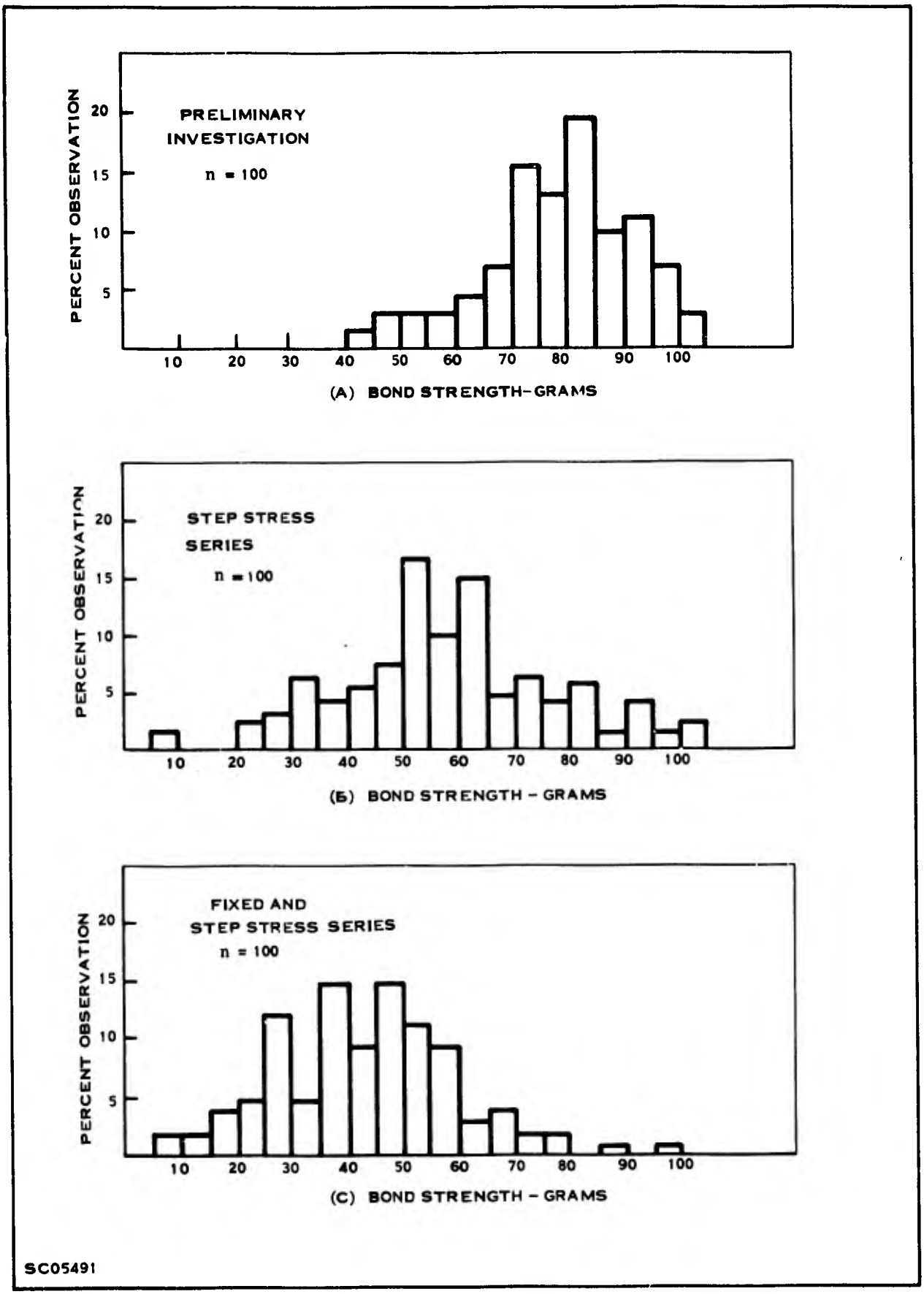

Figure 27. Comparative Histograms of Bond Strength Between Three Manufacturing Lots

Table 14. Comparison of Pre and Post Stress Strength Distributions using Kolmogorov-Smirnov Two-sample Test

(a) High Temperature Storage

	T_A				
	200°C	300°C	350°C	400°C	Control
Sample Size	42	35	35	35	24
Maximum Difference (%) Observed	28	17	16	12	25
(%) Allowed(α =0.05)*	28	31	31	31	38

(b) Thermal Shock and Mechanical Stress

	Thermal Shock	Impact Shock	Constant Acceleration				
			20 KG	30 KG	60 KG	100 KG	Control
Sample Size	35	35	30	30	30	30	30
Maximum Difference (%) Observed	42	21	29	43	45	50	43
(%) Allowed (α = 0.05)*	31	31	33	33	33	33	33

* Maximum difference between two cumulative distributions representing prestress and poststress band strength data. Allowed difference is that value which, if exceeded, indicates at the $\alpha = 0.05$ significance level that there is a difference in two distributions. This difference could be attributed to stress effects if the control sample indicated no measurement error.

Briefly, results may be summarized as follows: The Preliminary Investigation, which exhibited no failure modes due to peeling metal or weak bonds demonstrated the highest median bond strength with least variance, and in all cases the bonds separated leaving gold which adhered to the molybdenum film. The other two replicates demonstrated lower median bond strengths and wider variance, with evidence of gold peeling from the molybdenum surface when the bonds were sheared. Failure modes due to peeling metal and weak bonds were encountered in the other tests. The shear bond strength technique is presently being used by Texas Instruments for production process monitoring. The equipment used for this test is illustrated in Figure 28.

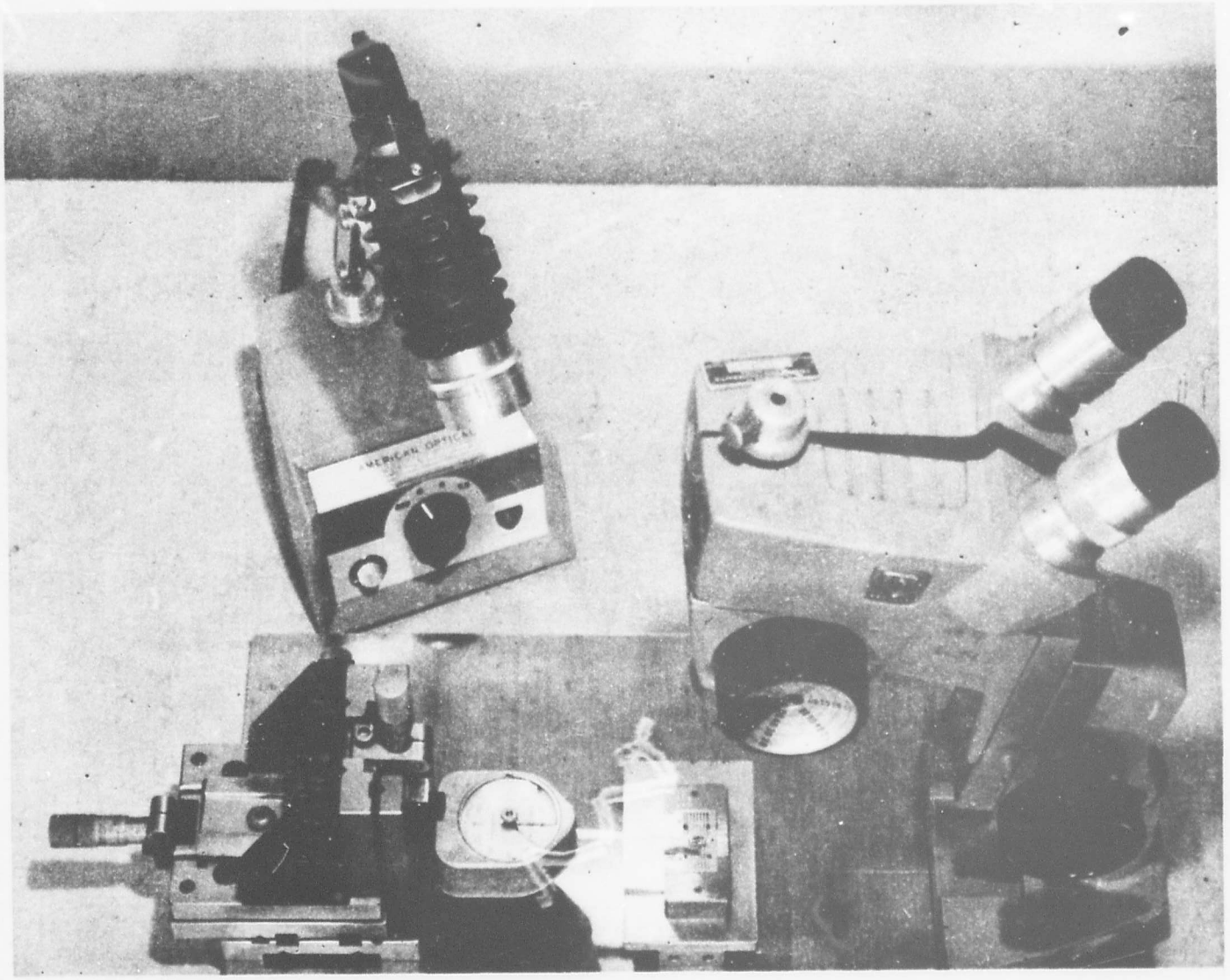

Figure 28A. Shear Bond Strength Tester for Production Monitoring (Test Set-up)

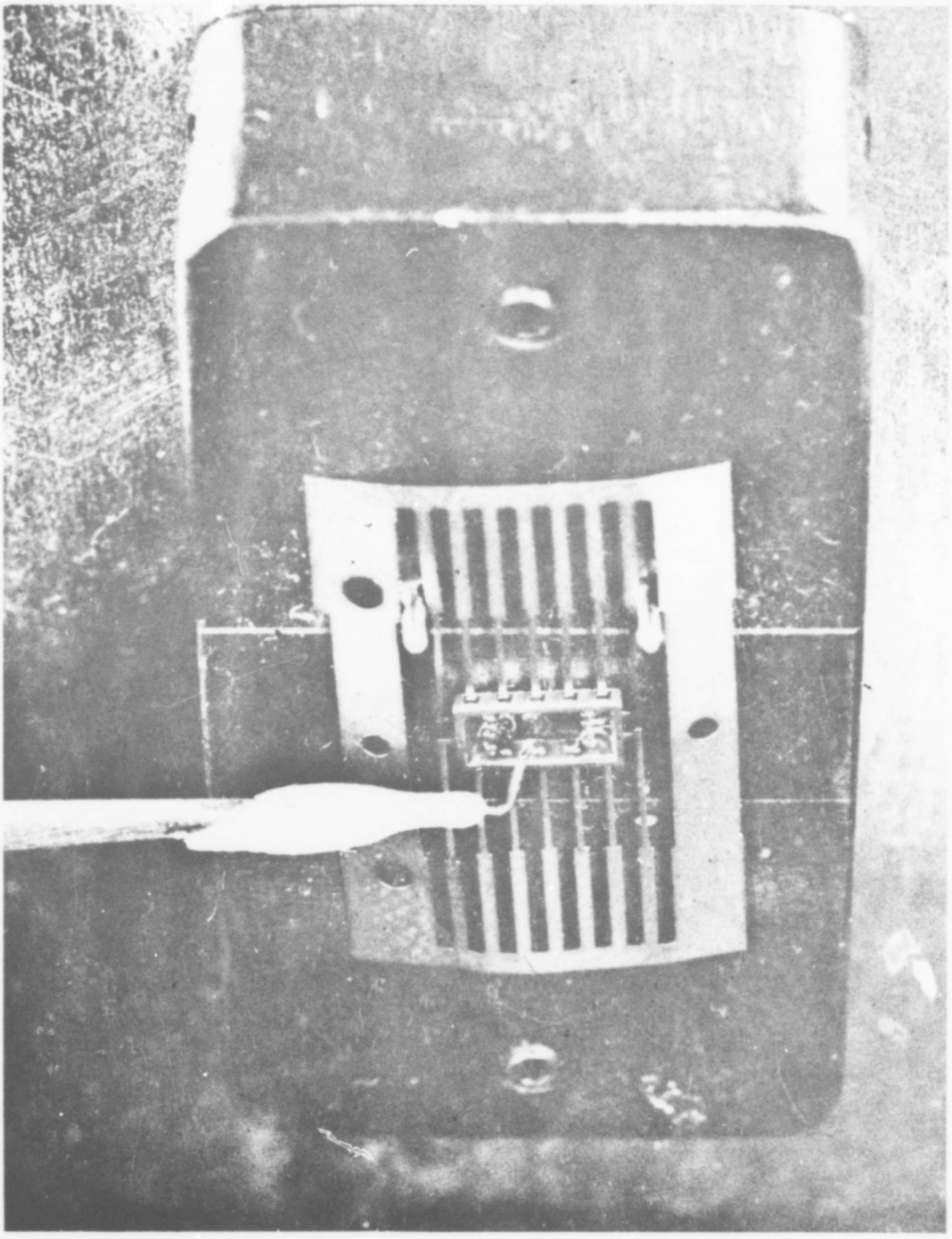

Figure 28B. Detail for Device and Shear Probe

Table 15. Comparison of Post Stress Bond Strength Distributions Between Stress Samples and Control Samples

	Thermal Shock	Impact Shock	Constant Acceleration			
			10 KG	30 KG	60 KG	100 KG
Sample Size	35	35	30	30	30	30
Maximum Difference						
(%) Observed	21	23	12	20	30	30
(%) Allowed ($\alpha = 0.05$)*	31	31	33	33	33	33

* Refer to Table 14.

Table 16. Relating Shear Bond Strength To Modes of Bond Separation and Incidence of Stress Failures

Device Lot Identification	Shear Bond Strength in Grams (Reference Figure 27)				Topology Analysis			Main Test Program Failure Analysis Results	
	Number of Bonds Sheared	Min	Med	Max	Number of Devices Evaluated (No. Bonds)	Mode of Bond Separation	Evaporated Lead Peeling	Ball Bond Separation	Peeling Evaporated Leads
1. Preliminary Investigation (Figure 27A)	100	40	80	100	4 (48)	Gold to Gold (48)	none	0	0
2. Step Stress Replicate I (Figure 27B)	100	5	55	100	1 (12)	Gold to Gold (1) Gold to Moly (5) Silicon (6)	none	2	1
3. Fixed and Step Stress (Figure 27C)	100	5	40	100	5 (60)	Gold to Gold (12) Gold to Moly (44) Silicon (4)	3 units with peeling evaporated leads	3	9

SECTION VI

CRITIQUE

1. INTRODUCTION

This section contains a critical review of the work performed on the contract. The objective of the program was to develop reliability screening and prediction methods for Integrated Circuits. Fundamental to this objective were the physics of failure programs which were divided between surface studies, contact and interconnection evaluations, and circuit analysis. Secondly, a test program coupled with data and failure analysis was performed to accelerate the failure mechanisms of the circuit and to integrate the results with the physics of failure program. From this work a reliability screening procedure for SN5420 was developed. In general, these objectives were accomplished in spite of a test program from which few failures could be obtained from stresses which far exceeded the normal rated conditions of the Integrated Circuit. This section summarizes the significant results determined from the program.

Fundamental oxide studies were primarily concerned with sodium contamination of thermally grown oxides on silicon. Techniques for the formation of clean oxides and the retention of cleanliness through the application of metal contacts, were developed; however, work was performed under laboratory conditions and efforts to relate this work to production oxides were not attempted. Early in the program it was decided to concentrate on the development of clean oxides in fundamental studies rather than shifting attention to the failure mechanisms which occurred from the test program. Clean oxides were necessary so that experiments to contaminate oxides in a controlled manner could be performed to duplicate surface related failure mechanisms encountered in actual devices. There was, consequently, no medium by which the oxides obtained by the clean-oxide technology could be compared with the oxides typical of production devices subjected to the test program. The problem was confounded by the lack of surface related failure mechanisms observed in failures from the stress program.

The SN5420 is a gold doped, low voltage circuit designed to be relatively insensitive to parameter variability incircuit components. Selection of a test vehicle with higher breakdown voltage, thereby permitting higher voltage stress, might have improved the opportunity of detecting failures caused from surface instability. However, it is doubtful whether this approach would have been sufficient in itself to relate the fundamental oxide work to the test program. A more realistic approach would

have included the fabrication of special MOS structures along with devices subjected to stress. MOS structures with production oxides could then be compared to MOS structures with clean oxides obtained under laboratory conditions. A very useful outcome of this approach would be the implementation of MOS techniques for production process control.

Other physics of failure studies consisting of contact and interconnection studies, circuit analysis and failure analysis, have played important roles ir the development of reliability prediction methods for Integrated Circuits. Their contribution is even more significant when considering the results of the test program where few failures could be obtained at use-relatable stress levels.

The technique to measure shear bond strength, developed from the contact studies, was demonstrated to predict the occurrence of peeling metallization and bond failures which occurred during the test program. However, efforts to measure metal resistance degradation on actual devices subjected to stress were not successful since resistance changes were near or below the level determined to be caused by the experimental error. Future studies of this type should be conducted on special thin-film structures with permanently connected contacts for current and voltage sensing[2/].

The nonfunctional parameter techniques developed during the circuit analysis studies demonstrated that changes in component parameters do occur under stress even through functional parameters do not reflect change. The gain parameter coupled with arbitrarily established failure criteria were used to calculate an activation energy of 0.23 electron volts for the devices subjected to electrical stress between 160° C and 200° C. However, the changes in these parameters in most cases did not predict failure, since devices which survived stress also exhibited similar changes. To fully determine the significance of the activation energy and other information provided by the nonfunctional technique, a thorough understanding of the mechanisms causing change is needed. Studies should be conducted to determine whether nonfunctional measurements can be used to eliminate the number of measurements required to detect or predict failure. Further analysis of existing data might provide some answers to this question. Secondly, the efficacy of this technique for process control needs to be studied. For instance, gain or output impedance might prove to be a reliable indicator of potential degradation in switching speed. Information of this type would be particularly useful in the testing of circuit arrays for large scale integration where difficulties in performing high-speed probe measurements are encountered.

Failure analysis coupled with the high-stress program played an important part in the development of the reliability screening procedure. Precapsulation photographs of the dies taken prior to stress on one replicate demonstrated how die related failure mechanisms such as cracks, could be traced to visual information which existed on the dice prior to stress. From these analyses criteria for visual die inspection were

included in the reliability screening procedure. A logical extension of this work might include feasibility studies to determine techniques for automating die inspection based on the physical location of anomilies on the die in addition to their geometric characteristics.

Relatively few failures occurred during the test program even though stresses were performed at levels approaching the physical limitations of both devices and stress equipment. Tests which were extended to include 2000 hours did not produce a significant increase in the number of failures observed. With the exception of high temperature storage, tightening the failure criterion of each parameter did not produce a significantly larger quantity of failures; consequently the distribution of these failures and therefore acceleration factors, could not be determined, nor were computer prediction techniques developed during the program, appropriate under these conditions.

The computer program SERF developed for this program was demonstrated to be of value in isolating the preindicators of failure for a few devices. However, a considerable amount of work needs to be done in correlating the non-functional measurements with the functional parameter changes and ultimately with device degradation. It should be emphasized that any prediction done was "after the fact". That is, devices which were already known to be failures were examined to determine if some earlier measurement preindicated failure. This is an acceptable procedure for an exploratory investigation, but these screening procedures must be verified using a number of samples from different manufacturing lots. This is the intent of the extension to the contract described in Section IV.

During the high-stress program it was demonstrated that some failure mechanisms occurred with equal probability throughout all stress intervals. The two observed in this program are cracked dies and peeling metallization. Screens consisting of precapsulation die inspection and shear bond strength tests were developed for these during the program. The shear bond strength technique served to demonstrate that nondestructive screening is not the only answer to reliability screening. It appears that screening of Integrated Circuits can best be implemented in the process prior to capsulation of the device. Screens are most effective when they are related to a particular technology of the process, such as metal deposition or die mounting technologies.

2. RECOMMENDATIONS FOR FUTURE STUDIES

During an extension of this contract, the reliability screening procedure developed during this contract will be evaluated. Shear bond strength tests and precapsulation die inspections will be conducted to predict failures. The devices will then be

subjected to high-stress divided between two phases. First, a burn-in will be conducted to eliminate devices with less than average lifetimes in the population. Finally, a stress program will be conducted on the same devices to demonstrate the effectiveness of the screening procedure.

It is recommended that feasibility studies be initiated to investigate possibilities of automating die inspection procedures on the premise that defects can be classified into defined geometrical patterns which discriminately identify potential failures from the remaining population.

Further analysis of the existing data in areas of non-functional parameters and switching data is recommended. It is possible that this technique can be used for process control and can be especially beneficial for highly complex Integrated Circuits, for high-speed switching measurements are difficult to adapt to probe-testing techniques.

A comparative analysis of all types of metal systems using the shear bond strength technique might prove beneficial in establishing the relative reliability of the various systems.

It is recommended that future programs place increased emphasis on developing techniques for process control. This will include measurements on MOS structures or other types, particular production processes can be characterized and techniques developed to preindicate failure in Integrated Circuits.

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APPENDIX A

FIXED AND STEP STRESS SERIES

1. INTRODUCTION

These tests are continuations of high stress tests performed as a part of the test program which is summarized in Section II. The tests discussed herein were designed and performed following the completion of two other major segments, the Preliminary Investigation and Step Stress Series.

2. STRESS AND MEASUREMENT

The stresses used in the program are outlined in Table A-1; parameter measurements, degradation limits and test circuits in Table A-2 and Figures A-1 and A-2. The tests consisted of fixed and step stress including forward bias and ring counter operating tests, high temperature storage, and constant acceleration. Parameter measurements included functional and non-functional (gain and output impedance) parameters. The work related to the development and use of non-functional measurements is contained in Section II. The 220°C operating life tests (ring counter and forward bias) were terminated at 1000 hours when it was learned that the stress temperature had degraded the stress sockets such that they were no longer operable. Diagrams of the electrical stress circuits are shown in Figures A-3 and A-4, respectively.

3. TEST RESULTS AND DATA ANALYSIS

Failures which occurred during the tests are shown in the bar graphs of Figures A-5 through A-8. A cross reference to relate the failures to failure mechanisms defined in Appendix D is provided in the figures. Electrical and storage stresses produced few failures even though some tests were extended to 2000 hours at stress levels approaching device and stress equipment limitations. Statistical theory relating fixed and step stress (Appendix E) was considered for data analysis; it was not found to be useful since failure distributions could not be determined from the few failures which occurred. However, another approach to data analysis was instrumental in developing the reliability screening procedure shown in Table 1. The mechanisms determined from analysis of failures were related to visible die anomalies determined from photographs taken prior to stress. Refer to Appendix D for discussions of failure and photographic analyses pertaining to these and other tests performed throughout the contract.

Table A-1. Test Plan for Fixed and Step Stress Series

A.	Step Stress			
		Sample Size		
1	Forward Bias (Figure A-3)	20 20 20 20	t = 275 hrs/step t = 350 hrs/step t = 425 hrs/step t = 500 hrs/step	Temp (°C) = 160,180,200,220 (Figure A-5a)
2	Ring Counter (Figure A-4)	20 20 20 20	t = 275 hrs/step t = 350 hrs/step t = 425 hrs/step t = 500 hrs/step	Temp (°C) = 160,180,200,220 (Figure A-6a)
3	Storage	20 20 20 20	t = 108 hrs/step t = 156 hrs/step t = 216 hrs/step t = 264 hrs/step	Temp (°C) = 300,325,350,375,400 (Figure A-7a)
4	Constant Acceleration	50	Stress (KG) = 15,30,45,60,75 (Figure A-8)	
B	Life Test			
		Sample Size		
1	* Forward Bias (Figure A-3)	30 30 30 30	Temp (°C) = 160 180 200 220	Readout times (hrs) = 275,350 425,500,1000,1500,2000 (Figure A-5b)
2	* Ring Counter (Figure A-4)	30 30 30 30	Temp (°C) = 160 180 200 220	Readout times (hrs) = 275,350 425,500,1000,1500,2000 (Figure A-6b)
3	Storage	30 30 30 30	Temp (°C) = 300	Readout times (hrs) = 108,156, 216,264,528,996 (Figure A-7b)

* 220°C Stress terminated at 1000 hours.

Limits for the dc parameters used to define failures are shown in Table A-2. The results of an analysis to determine the parameters most frequently indicating failure are provided in Table A-3, which is divided into two parts. First the percentage of failures indicated by each individual parameter is shown for three categories of stress: electrical, storage and constant acceleration. Secondly, the percentage of failures detected by successively summing the effects of individual parameters in the order shown in the table is given. Referring to Table A-3, Item II, 67% of the failures caused by electrical stress would have been detected by input leakage (I_{IL}) measurements only, 72% by the combined measurements of I_{IL} and I_{IN}, 79% by I_{IL}, I_{IN} and I_{OS}, etc. The results indicate all parameters would be required to define all failures in each of the three stress categories. However, the dominant indicator for each category is different. This is a logical result since the observed failure mechanisms (summarized in Table 2) varied with the type of stress used.

Analysis of the nonfunctional gain parameter data has proven useful in the study of acceleration factors. The nonfunctional parameters were not used to define functional failure during the test program; the results relating to these measurements are discussed in Section III (Test Results and Analysis).

4. PHOTOGRAPHIC ANALYSIS

Photographs of the test samples, taken prior to capsulation, were used to relate mechanisms causing failure to die anomalies observed prior to stress. Prior to stress, the photographs were analyzed and the observed anomalies classified into 15 groups shown in Table A-4. Results of this analysis are shown in Table A-5 for devices which failed under stress. These photographs were used by the Failure Analysis Laboratory to correlate visible defects causing failure to the stress. Refer to Appendix D for failure analysis discussions and Section IV for a visual die inspection procedure developed from this effort. The new inspection criteria shown in Table 4 permits more discriminant prediction of the types of defects causing failure, while the criteria used to analyze the photographs prior to stress (results are summarized in Table A-5) did not.

5. COMPARING SERIES 54 AND 74

Ten percent of devices subjected to the electrical and thermal stresses were type SN7420. These devices were used to utilize as fully as possible the precapsulation photographs taken prior to final electrical tests. A comparison of the stress results obtained for Series 54 and 74 devices is shown in Table A-6. There is no indication that Series 74 devices are less reliable than Series 54 counterparts.

6. RING COUNTER EVALUATION

An evaluation to determine the effects of load capacitors on ring counter operating life results was performed. The 160°C operating stress cell (n = 30) was divided into

Table A-2. Degradation and Catastrophic Failure Criteria for the SN5420

Parameter	Reference Figure A- (.)	Test Conditions	Initial Parameter Limits		Failure End Point Limits	
			Minimum Value	Maximum Value	Minimum Value	Maximum Value
Functional Parameters						
Input Leakage Current Current (I_{IL})	(1a)	V_{CC} = 5.5 V V_{IN} = 4.5 V		100 μA	Δchange < 5μA & % change < -50%	Δchange > 5 μA & % change > 100%
Input Current (I_{IN})	(1b)	V_{CC} = 5.5 V V_{IN} = 0.4 V		1.6 mA	-20% change	+ 20% change
Short Circuit Output Current (I_{OS})	(1c)	V_{CC} = 5.5 V	25 mA	55 mA	-20% change	+ 20% change
"Off" Voltage (V_{OFF})	(1d)	V_{CC} = 4.5 V V_{IN} = 0.8 V $I_{load} \geq 400\ \mu A$ R = 6 K Ω	2.4 V		-0.3 V Δchange	+ 0.3 V Δchange
"On" Voltage (V_{ON})	(1e)	V_{CC} = 4.5 V V_{IN} = 2 V $I_{SINK} \geq 16$ ma R = 256 Ω		0.4 V	-0.1 V Δchange	+ 0.1 V Δchange
V_{CC} "ON" Current (I_{ON})	(1f)	$V_{CC} = V_{IN}$ = 5 V				
V_{CC} "OFF" Current (I_{OFF})	(1f)	V_{CC} = 5 V V_{IN} = 0				
Propagation Time On (T_{ON})	(2a)	C_1 = 15 pf N = 10		15 ns	Δchange > 3 ns & % change > 20%	Δchange > 3 ns & % change > 20%
Propagation Time Off (T_{ON})	(2a)	C_1 = 15 pf N = 1		30 ns	Δchange > 3 ns & % change > -20%	Δchange > 3 ns & % change > 20%
Nonfunctional Parameters						
Voltage Gain (G)	(2b)					
Output Impedance (Z_{OUT})	(2b)					

Table A-3. Summary of Failing Parameters by Test

Item	Parameter (n)				
	I_{IL} (1)	I_{IN} (2)	I_{OS} (3)	I_{OFF} (4)	V_{ON} (5)
I. Percent of Failures Indicated by Individual Parameter					
A. Electrical Stress	67%	49%	8%	59%	33%
B. Storage Stress	7%	20%	73%	53%	33%
C. Constant Acceleration	90%	82%	18%	86%	32%
II. Cumulative Percent of Total Failures Indicated by $\sum_{1}^{n} P_i$					
A. Electrical Stress	67%	72%	79%	90%	100%
B. Storage Stress	7%	20%	73%	87%	100%
C. Constant Acceleration	90%	90%	93%	93%	100%

Table A-4. Classifications of Anomalies Revealed by Precapsulation Photographic Analysis (70X Magnification)

A	Scratches in the lead pattern — The criteria here were scratches that were shallow enough not to remove the contact material down to the oxide.
B	Bonds not centered on the pads — This criterion is that the bond appears to be miscentered enough for some of the bond to be on the oxide instead of the metal on the pad.
C	Bonds near the edge of the bar — This would only occur when the bar was scribed and broken outside the normal scribe area in such a way as to place the bond pads close to the edge of the bar.
D	Blemish on lead pattern — This can be detected only superficially at this magnification and is not conclusive.
E	Peeling metallization — This is difficult to identify at this magnification and was mainly indicated when the adjacent area was bare of metallization.
F	Misalignment of photomask — This is almost impossible to identify at this magnification and probably exists only on a very low order in this sample.
G	Diffusion damage — This is limited only to those holes that are large enough to have a definite depth to them.
H	Photomasking anomaly — Anomalies caused by the photomasking operations have a character to them that is readily identified. However, only those anomalies that were large enough to be definitely identified as such were enumerated.
I	Surface contaminations — Many anomalies that are otherwise unidentifiable are in this category.
J	Metallization missing on surface or contact heavily damaged — This is the more severe form of Category A.
K	Gold-silicon eutectic — Difficult to identify at this magnification and very infrequent in occurrence.
L	Oxide anomalies (scratches, blotches, star patterns, etc.) — This includes a large number of otherwise unidentifiable anomalies. All anomalies in the oxide too small for positive identification are in this category.
M	Bar cracked into apparently two separate pieces — This anomaly is indicated whenever it appears that a crack has separated the bar into two pieces or a chip is terminated back at the same edge of the bar that it started from.
N	Bar crack radiating from the scribe region — This includes what appears to be fairly short hairline cracks radiating from the bar edge.
O	Frit over edge of the bar — Whenever the frit overruns the bar edge and is identifiable as such, this anomaly is indicated.

Table A-5. Comparing Stress Failures to Anomalies Revealed by Photographic Analysis

Test Description	No Fail	Type of Anomaly*													
		A	B	C	D	E	F	G	H	I	J	K	L	M	N
Electrical															
Forward Bias Step Stress n = 80	10	7/48	3/31	0/2	3/28	2/11	0/0	0/2	5/43	6/36	4/39	0/1	5/51	0/5	5/32
Forward Bias Life Test n = 120	7	4/67	4/58	0/2	0/18	0/19	0/0	1/6	1/55	3/60	3/45	0/0	4/50	0/3	3/54
Ring Counter Step Stress n = 80	12	9/56	2/27	0/1	3/19	2/24	0/0	0/3	6/54	3/34	4/27	0/0	12/60	1/4	6/37
Ring Counter Life Test n = 120	10	6/74	1/30	0/0	0/21	2/22	0/0	0/3	2/55	0/45	3/50	0/1	5/53	0/1	7/42
Total	39	26/245	10/146	0/5	6/86	6/76	0/0	1/14	14/205	12/173	14/161	0/2	26/214	1/13	21/165
Storage															
Storage Step Step Stress n = 80	6	5/64	4/39	0/3	2/36	2/20	0/0	0/9	3/46	4/38	3/34	2/2	4/59	0/1	0/25
Storage Life Test n = 120	9	8/92	1/63	0/1	4/39	0/25	0/0	1/4	4/68	7/57	4/52	0/0	4/81	1/5	4/70
Total	15	13/156	5/102	0/4	6/75	2/45	0/0	1/13	7/114	11/95	7/86	2/2	8/140	1/6	4/95
Constant Acceleration Step Stress n = 50	28	26/42	17/30	0/0	11/21	10/21	0/0	0/0	10/21	12/21	8/17	1/1	19/33	0/1	15/25

*Numerator indicates number of failures with anomaly.

Denominator indicates number of devices with anomaly.

Table A-6. A Comparison of Stress Results Obtained For Series 54 and 74 Devices

Series	SN5420		SN7420	
Stress	n	% Defective	n	% Defective
Electrical Stress	144	28	16	19
Electrical Life Test	216	19	24	4
Storage Step Stress	72	11	8	0
Storage Life Test	108	8	12	8

twenty 3-gate ring counter cells. Five of the cells were "loaded" with 10 μF capacitors attached to the outputs of each gate. This loading effect reduced the oscillation frequency from 20 MHz to 10 MHz, and increased the dc current from 5 mA/gate to 10 mA/gate. The results shown in Figure A-6 (only one failure) indicate no significant difference in reliability of devices stressed in the two circuit configurations.

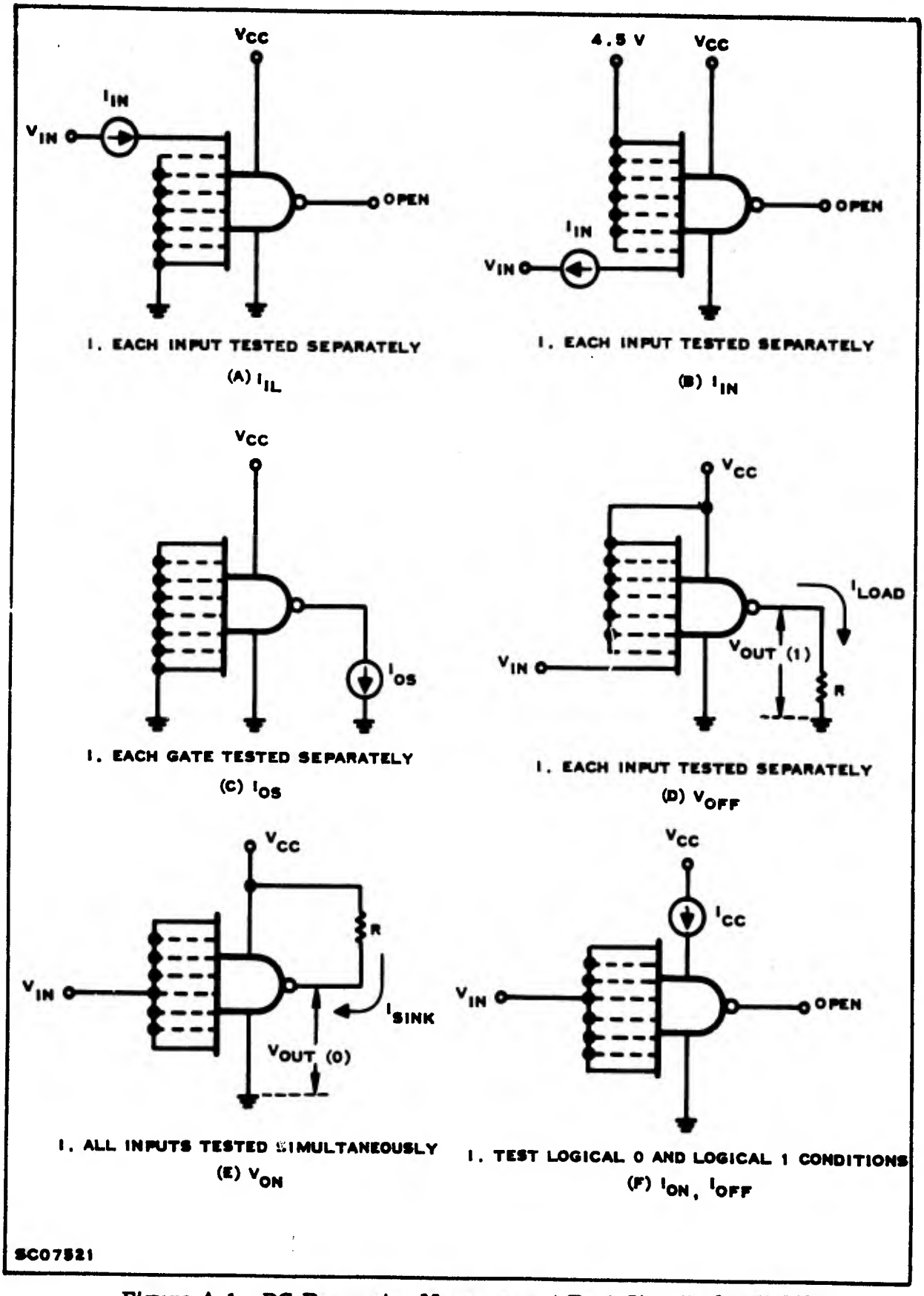
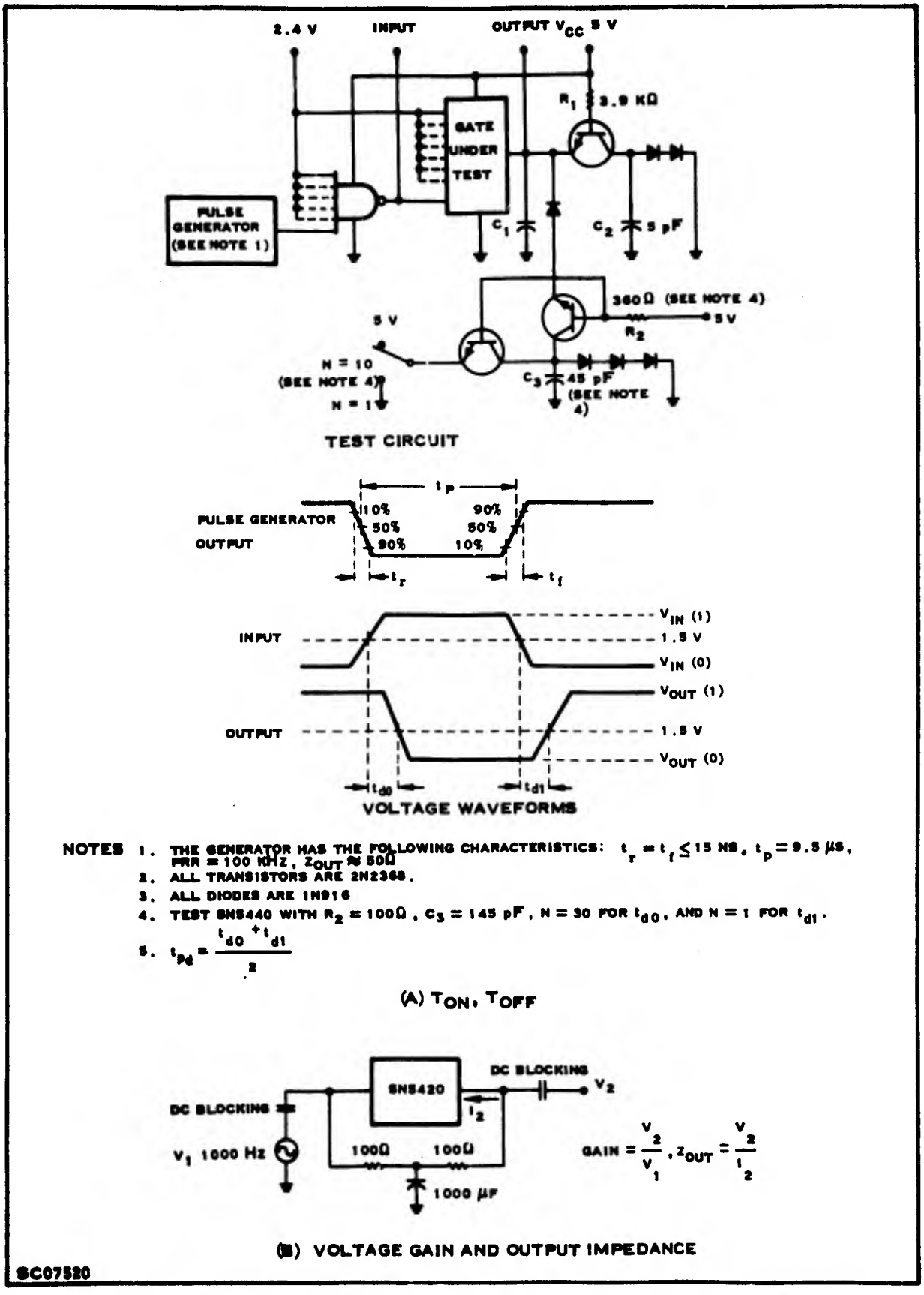


Figure A-1. DC Parameter Measurement Test Circuits for SN5420



NOTES

1. THE GENERATOR HAS THE FOLLOWING CHARACTERISTICS: $t_r = t_f \leq 15$ NS, $t_p = 9.5$ μS, PRR = 100 KHz, $Z_{OUT} \approx 50\Omega$
2. ALL TRANSISTORS ARE 2N2368.
3. ALL DIODES ARE 1N916
4. TEST SN5440 WITH $R_2 = 100\Omega$, $C_3 = 145$ pF, N = 30 FOR t_{d0}, AND N = 1 FOR t_{d1}.
5. $t_{pd} = \frac{t_{d0} + t_{d1}}{2}$

Figure A-2. Test Circuits for Switching and Nonfunctional Parameter Measurements

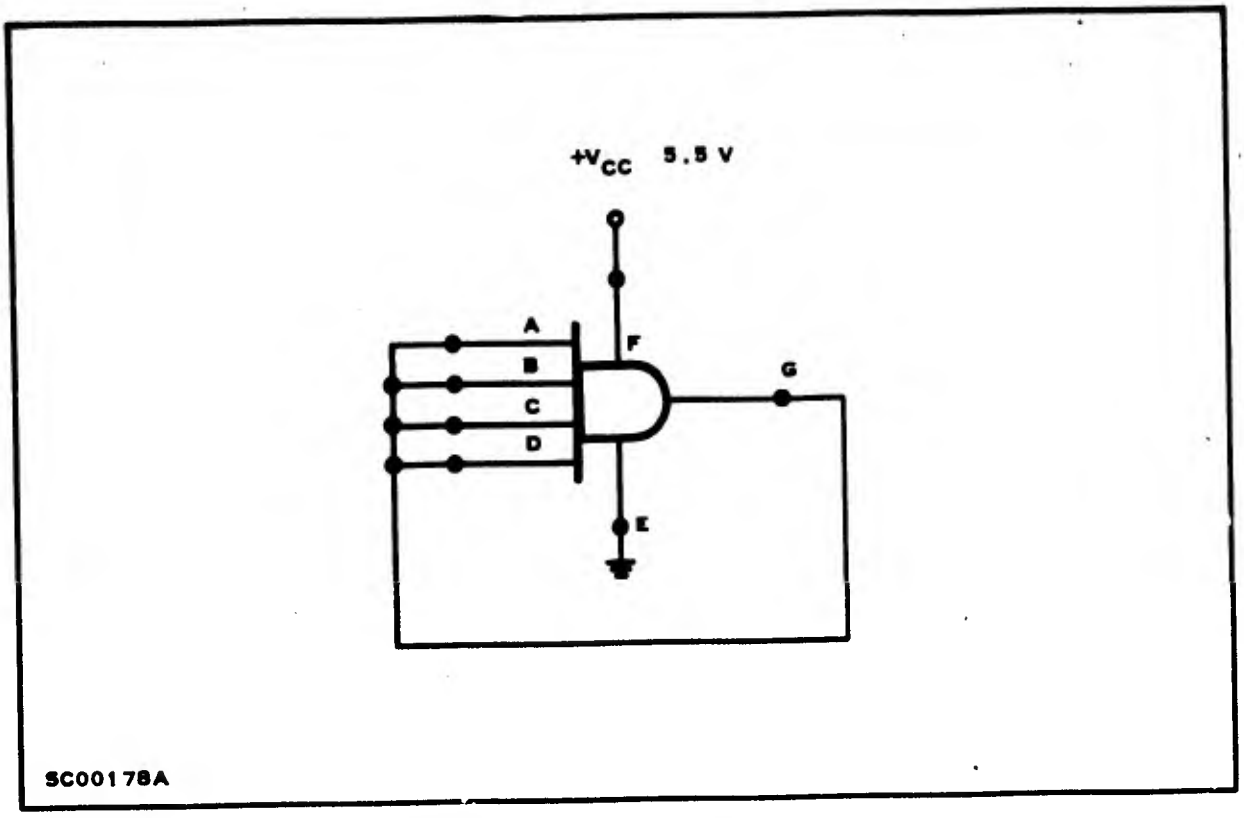


Figure A-3. Forward Bias Test Circuit

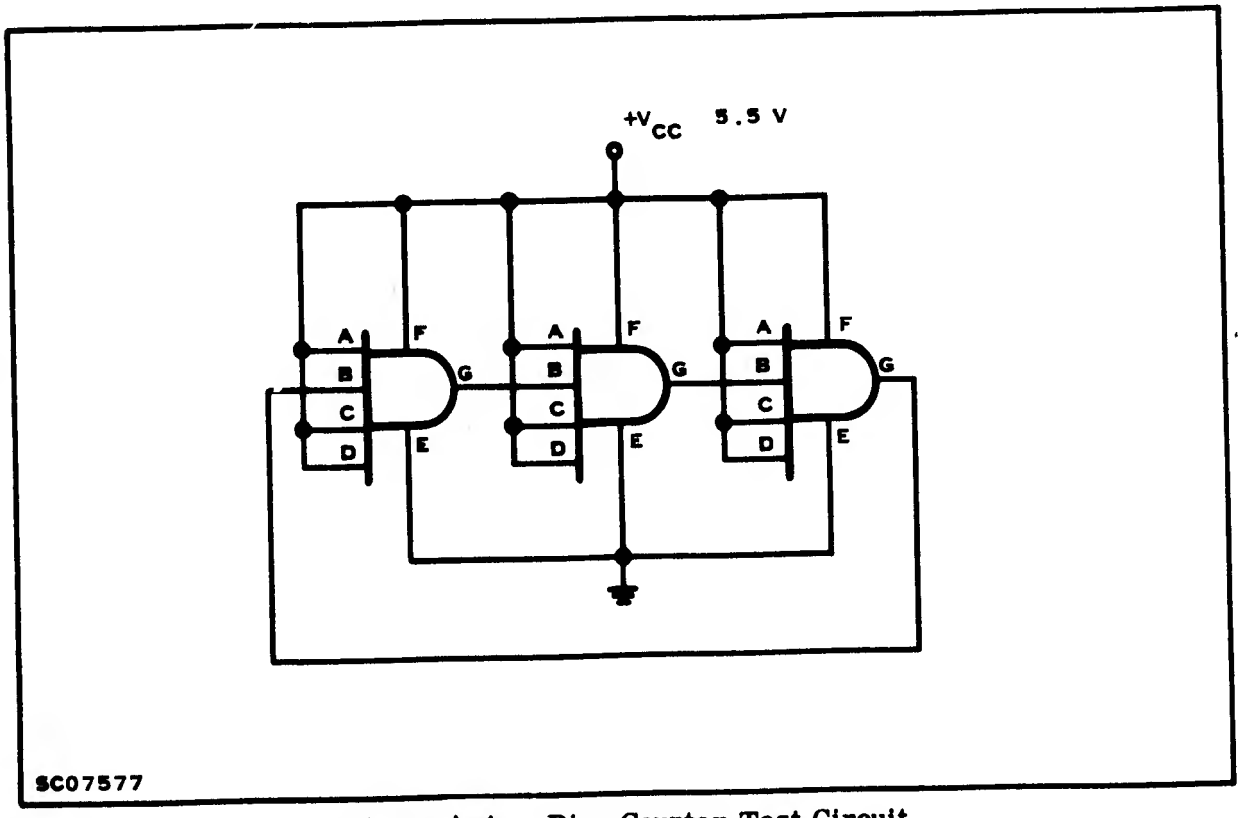


Figure A-4. Ring Counter Test Circuit

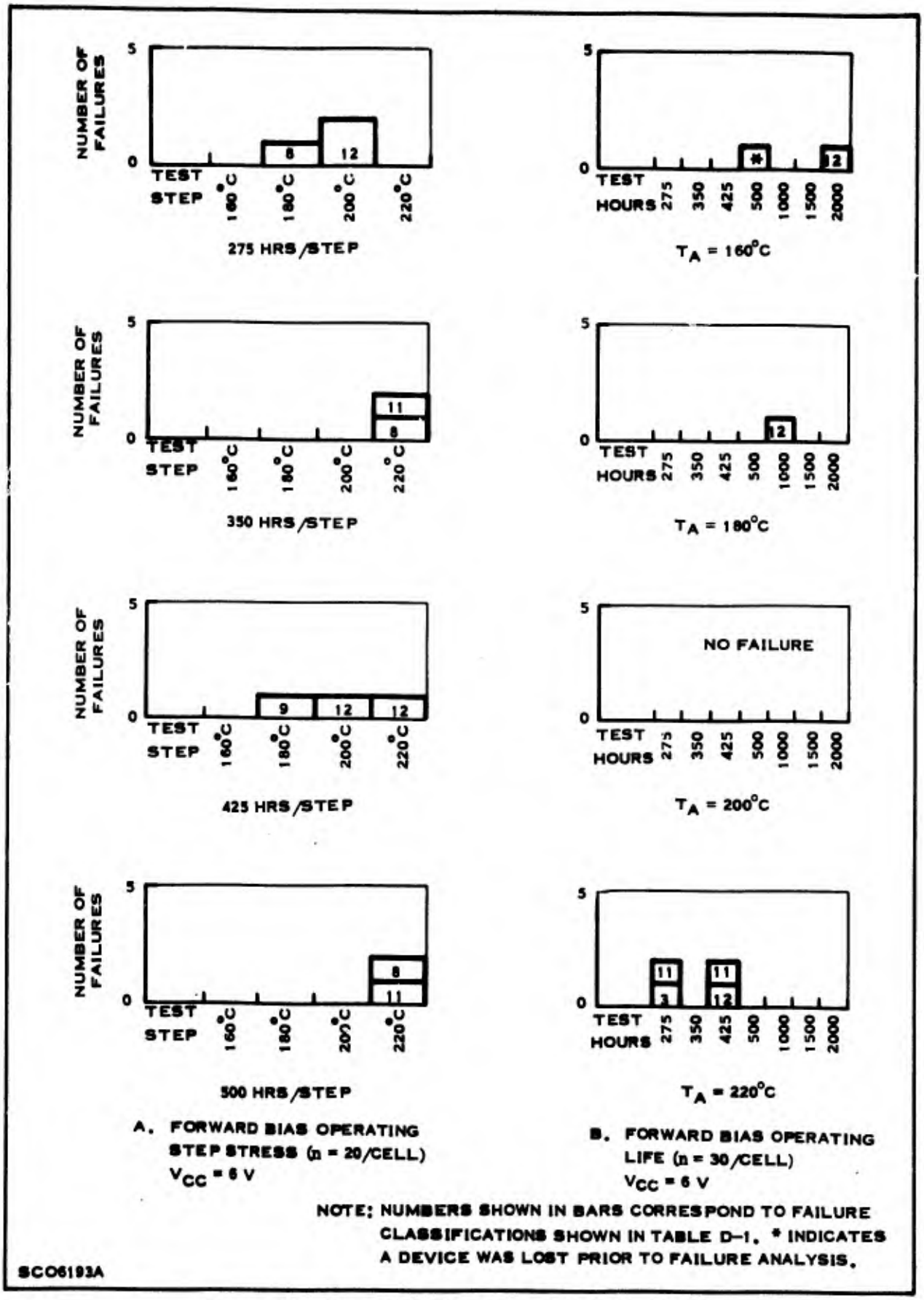
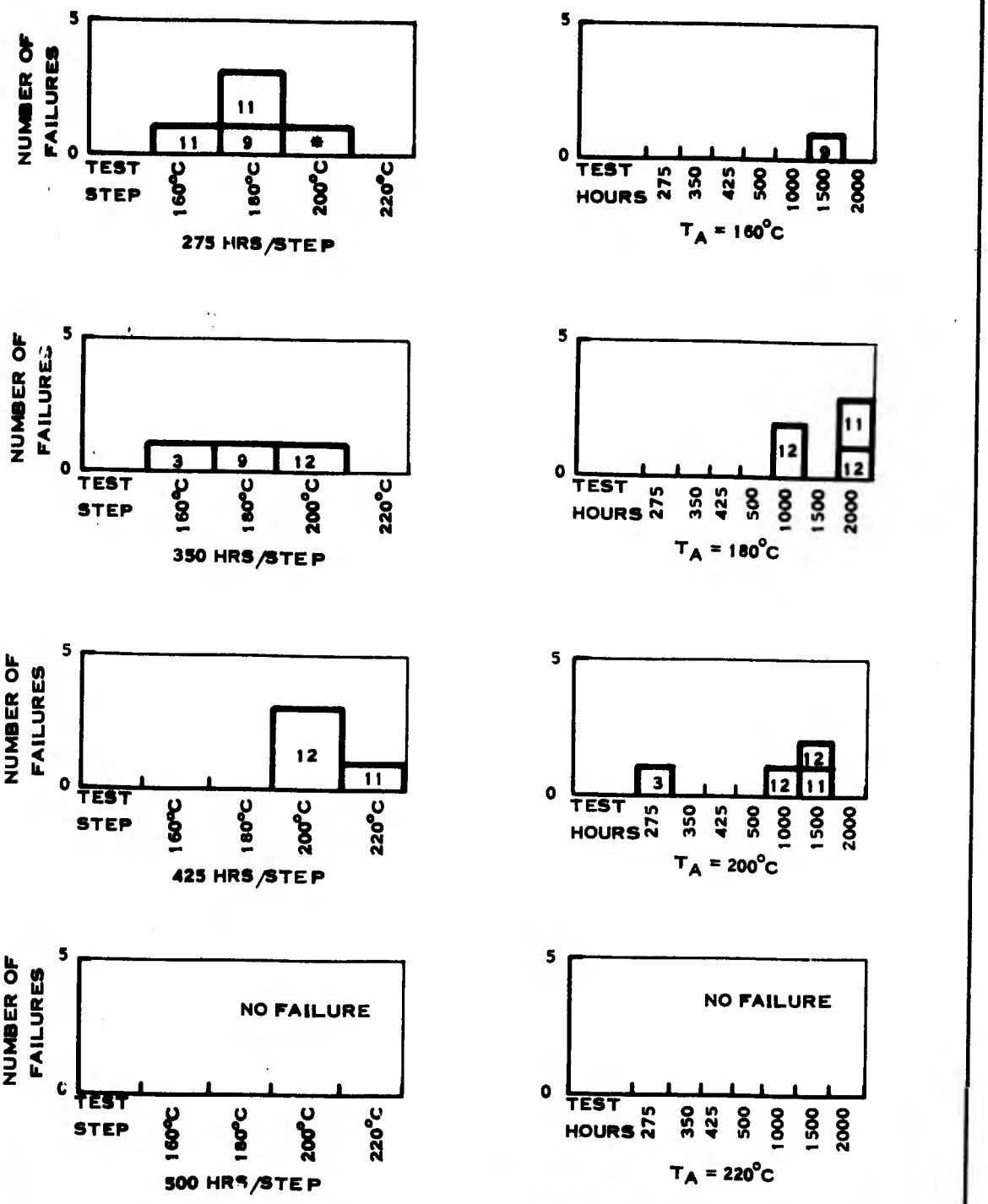


Figure A-5. Forward Bias Step Stress and Life Test Results



A. RING COUNTER OPERATING STEP STRESS (n = 20/CELL) V_{CC} = 6 V

B. RING COUNTER OPERATING LIFE (n = 30/CELL) V_{CC} = 6 V

NOTE: NUMBERS SHOWN IN BARS CORRESPOND TO FAILURE CLASSIFICATIONS SHOWN IN TABLE D-1. * INDICATES A DEVICE WAS LOST PRIOR TO FAILURE ANALYSIS.

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Figure A-6. Ring Counter Step Stress and Life Test Results

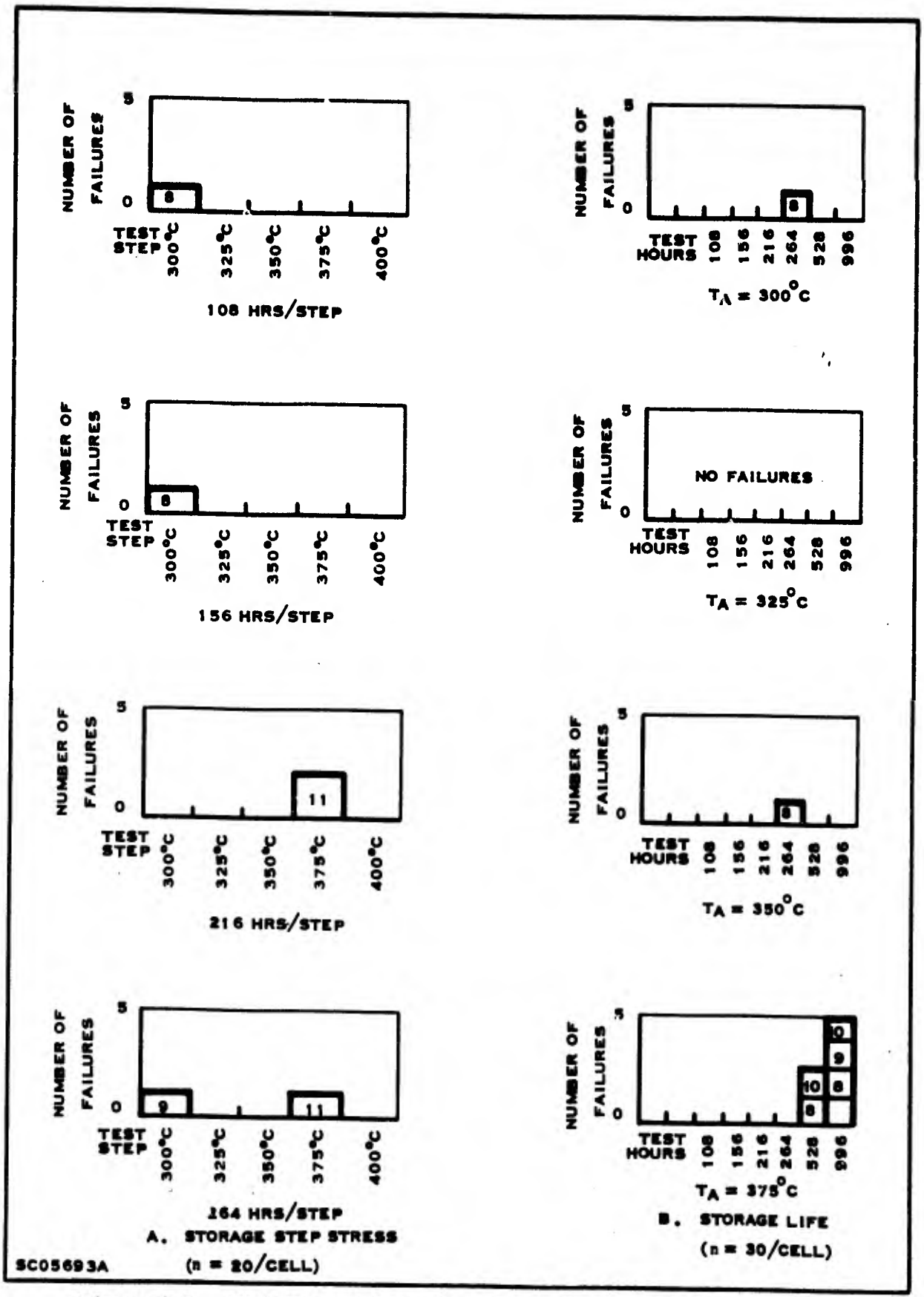


Figure A-7. High Temperature Storage Step Stress and Life Test Results

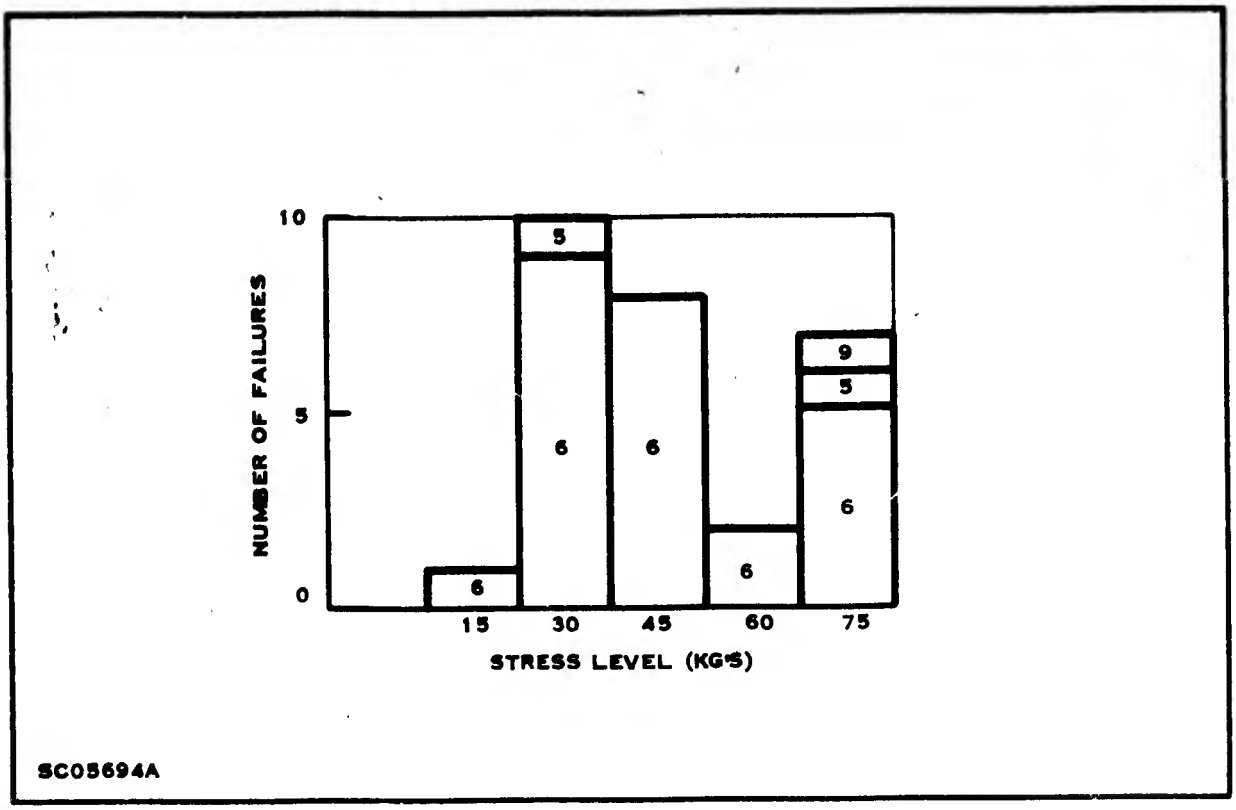


Figure A-3. Constant Acceleration Step Stress Results

APPENDIX B

COMPONENT EVALUATION

1. INTRODUCTION

A step stress program was conducted to evaluate components of the SN5420. Special masks were used to route lead patterns from component terminals to external package pins. Transistors, diodes, and resistors were subjected to power disipation, reverse bias, and high temperature storage tests. Data from these tests were used to study failure mechanisms and as an aid in interpreting results of tests on complete networks.

2. TEST VEHICLE

The components subjected to the step stress program are shown in Figure B-1. Two emitters of the input transistor were used in the study.

3. TEST PLAN

The stresses to which the components were subjected are described in Table B-1. Four stress steps each 72 hours duration, were used. Diagrams of the electrical stress circuits are shown in Figure B-2. Twenty monolithic bars, each containing five components, were divided into four cells of five bars each. The stresses for similar components within a cell were similar, but changed from cell to cell. For instance, each input transistor (Q1) of five bars was subjected to reverse bias in Cell II, non-operating storage in Cell III, and power dissipation in Cell IV. Refer to Table B-2 for amplification. A total of 100 components were stressed with an additional sample of 25 components tested as control samples.

The parameters shown in Table B-3 were measured before and after each stress interval. Failure limits were defined by measuring correlation samples and analyzing the data to determine experimental measurement error. A discussion of the use of control samples is contained in Section III. Parameter deviations in stress data greater than measurement error were treated as candidates for investigation and analysis.

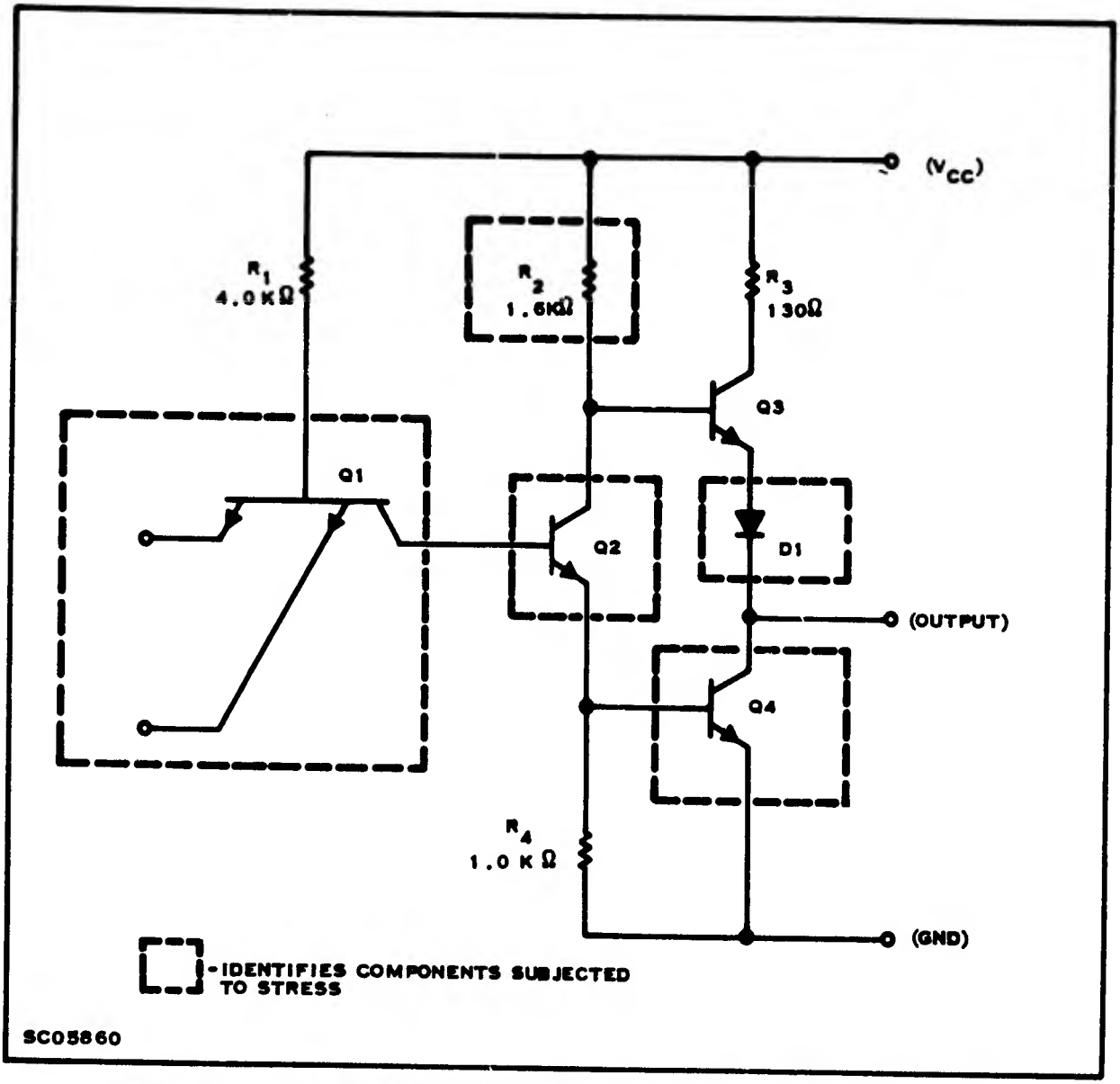


Figure B-1. One Gate of Type SN5420 Dual 4-Input Positive NAND Gate

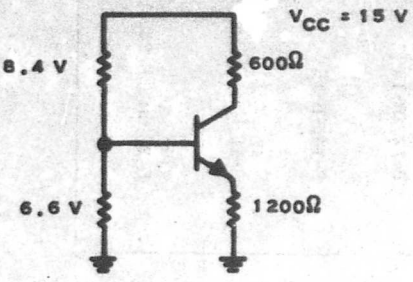
4. SUMMARY OF RESULTS

The most significant parameter variation was that of h_{FE} on reverse bias step stress. The median value showed a decrease of 60% after the first step of stress (140°C). Additional but less significant decreases in h_{FE} were observed following this interval. Emitter-base diode channeling was determined as the cause of degradation. Changes of less than 60 nA in reverse leakage current were observed in a few diodes and transistors as a function of stress. Refer to Table B-4 for a summary of the devices indicating parameter instability.

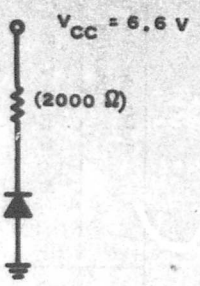
Table B-1. Test Plan for Component Evaluation

Stress	Test Conditions	Sample Size	Reference Figure Numbers
1. Storage Step Stress (All Components)	T_A = 160°C, 200°C, 300°C, 400°C	25	B-3 thru B-7, B-27
2. Storage Step* Stress (All Component types)	T_A = 140°C, 160°C, 180°C, 200°C	30	B-17 thru B-21
3. Power Dissipation Step Stress (Transistors)	T_A = 140°C, 160°C, 180°C, 200°C P_c = 30 mW V_{CB} = 6.6 V	15	B-8, B-9, B-28
4. Reverse Bias Step Stress (Transistors)	T_A = 140°C, 160°C, 180°C, 200°C V_{CB} = 6.6 V, V_{EB} = 6.6 V	15	B-10, B-11, B-30, B-31
5. Forward Bias Step Stress (Diodes)	T_A = 140°C, 160°C, 180°C, 200°C I_F = 10mA	5	B-12, B-13
6. Reverse Bias Step Stress (Diodes)	T_A = 140°C, 160°C, 180°C, 200°C V_R = 6.6 V	5	B-14, B-15
7. Resistor Step Stress	T_A = 140°C, 160°C, 180°C, 200°C V_R = 7.5 V P_R = 35mW	5	B-16
8. Control Sample Data (No Stress)		25	B-22 thru B-26, B-29

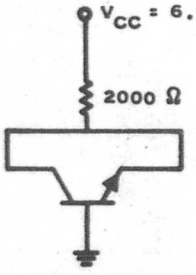
*These components were located on bars with other components subjected to electrical stress.



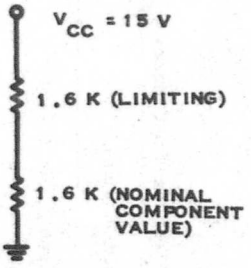
(A) TRANSISTOR POWER DISSIPATION (30 mW)



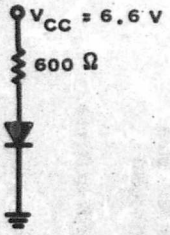
(D) DIODE REVERSE BIAS STEP STRESS



(B) TRANSISTOR REVERSE BIAS STEP STRESS



(E) RESISTOR STEP STRESS



(C) DIODE FORWARD BIAS STEP STRESS

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Figure B-2. Circuit Diagrams for Operating Stress Circuits

Table B-2. Stress Cells for Component Tests

Cell	Stress
I.	Storage Step Stress Through 400°C
II.	Operating and Storage Step Stress Through 200°C Q_1 - Reverse Bias Q_2 - Storage Q_4 - P_c = 30 mW R_2 - P_c = 25 mW D_1 - Storage
III.	Operating and Storage Step Stress Through 200°C Q_1 - Storage Q_2 - P_c = 30 mW Q_4 - Reverse Bias R_2 - Storage D_1 - Reverse Bias
IV.	Operating and Storage Step Stress Q_1 - P_c = 30 mW Q_2 - Reverse Bias Q_4 - Storage R_2 - Storage D_1 - Forward Bias

5. TEST RESULTS

The behavior of parameters as a function of stress are shown in Figures B-3 thru B-26. The figures which apply to a particular stress are shown in Table B-1. Data is plotted in the following manner:

I_{CBO}, I_R	Absolute changes relative to the initial parameter value are plotted for maximum increase, median change and maximum decrease.
Resistance, h_{FE}, BV_{CBO}, BV_R	Percent changes relative to the initial parameter value are plotted for maximum increase, median change, and maximum decrease.

Table B-3. Parameter Descriptions and Limits

Parameter	Component	Parameter for Study	Degradation Limit	Equipment Used	Test Conditions
1	Transistor	h_{FE}	±20% Change	Tektronix Type 575 Curve Tracer	I_B = 10 μA, V_{CE} = 3.0 V
2	Transistor	I_{CBO}	±10 nA Change	HP Model 425A DC Micro Volt-Ammeter	V_{CBO} = 3.0 V
3	Transistor	BV_{CBO}	±10% Change	Tektronix Type 575 Curve Tracer	I_R = 500 μA
4	Transistor	V_{BEO} versus I_B	(See Figure B-29)	Fluke Differential Voltmeter Model 883AB, Hewlett-Packard 425A Microvolt-Ammeter, Ballantine Precision Calibrator Model 421	V_{BE} = 0.3, 0.35, 0.4, 0.45, 0.5, 0.55, 0.6 V (Q_1 only)
5	Diode	I_R	±10 nA Change	HP Model 425A DC Micro Volt-Ammeter	V_R = 3.0 V
6	Diode	BV_R	±10% Change	Tektronix Type 575 Curve Tracer	I_R = 500 μA
7	Resistor	Resistance	±10% Change	Tektronix Type 575 Curve Tracer	I_{RESIS} = 1.0 mA

Table B-4. Component Parameter Data History for Parameter Changes Greater Than Limits Defined in Table B-3

Bar Number	Component	Stress	Parameter Changed (Reference Figure)	Parameter	Component Parameter History				
					Initial	Step 1	Step 2	Step 3	Step 4
1	Transistor (Q1)	Storage 160°C - 400°C	h_{FE} > 20% (Figure B-3)	h_{FE}	42	44	45	53*	40
				I_{CBO} (nA)	1.5	1.5	1.6	1.5	2.3
4	Transistor (Q1)	Storage 160°C - 400°C	$h_{FE} \geq \pm 20\%$ (Figure B-3)	h_{FE}	58	59	56	65	45*
				I_{CBO}	0.3	0.3	0.3	0.3	0.4
9	Transistor (Q4)	Storage 140°C - 200°C	$h_{FE} \geq -20\%$ (Figure B-17)	h_{FE}	45	43	44	17*	34
				I_{CBO}	1.1	1.2	1.4	0.2	1.4
7	Transistor (Q1)	Power Dissipation 140°C - 200°C	h_{FE} > 20% (Figure B-8)	h_{FE}	18	23*	20	24	23
				I_{CBO}	2.2	1.8	1.6	1.7	1.8
17	Transistor (Q1)	Reverse* Bias 140°C - 200°C	$h_{FE} \geq -20\%$ (Figure B-10)	h_{FE}	63	9*	4	4	6
				I_{CBO}	0.3	0.3	0.3	0.3	0.4
16	Transistor (Q2)	Storage 140°C - 200°C	$\Delta I_{CBO} \geq \pm 10$ nA (Figure B-18)	h_{FE}	40	38	38	44*	41
				I_{CBO}	0.1	0.3	0.1	0.1	13.0
16	Transistor (Q1)	Reverse Bias 140°C - 200°C	$\Delta I_{CBO} \geq \pm 10$ nA (Figure B-11)	h_{FE}	52	19	17	18	23
				I_{CBO}	26	13.6*	11.0	11.5	13.0
5	Diode	Storage 160°C - 400°C	ΔI_R (Figure B-5)	ΔI_R	9	19*	20	10	7
				BV_R	6	6.5	6.5	6.3	6.5
8	Diode	Forward Bias 160°C - 200°C	$\Delta I_R \geq \pm 10$ nA (Figure B-12)	I_R	1.1	21.0*	43.0	16.0	62.0
				BV_R	6.3	6.6	6.7	6.5	6.6
3	Resistor	Storage 160°C - 400°C	Resis. $\geq \pm 10\%$ (Figure B-7)	Resistance	2.4	1.4*	2.5	2.5	2.5
6	Resistor	Storage 140°C - 200°C	$\Delta R \geq \pm 10\%$ (Figure B-21)	Resistance (K ohms)	2.4	2.3	2.7	2.5	2.5

* Indicates First Step at which Failure Occurred.

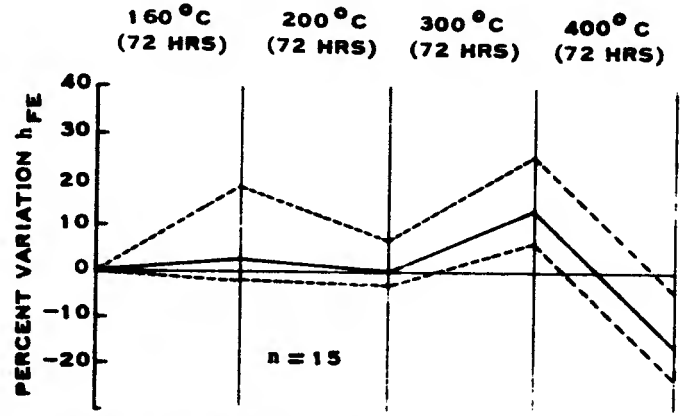


FIGURE B-3 PERCENT TRANSIENT OR h_{FE} VARIATION OF STORAGE STEP STRESS

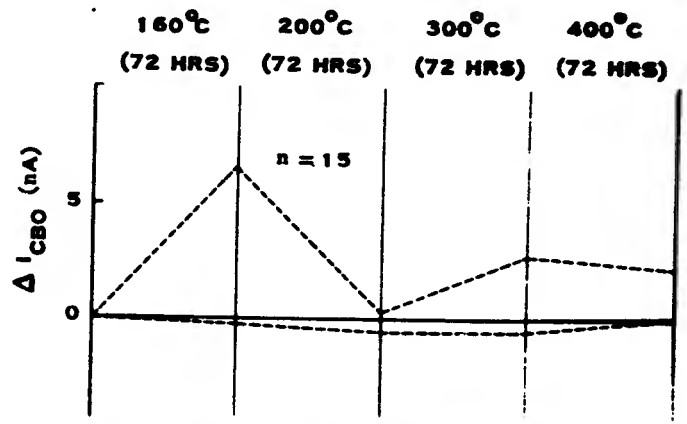


FIGURE B-4 TRANSISTOR I_{CBO} VARIATION WITH STORAGE STEP STRESS

LEGEND:
--- MAX. INCREASE
—— MED. CHANGE
--- MAX. DECREASE

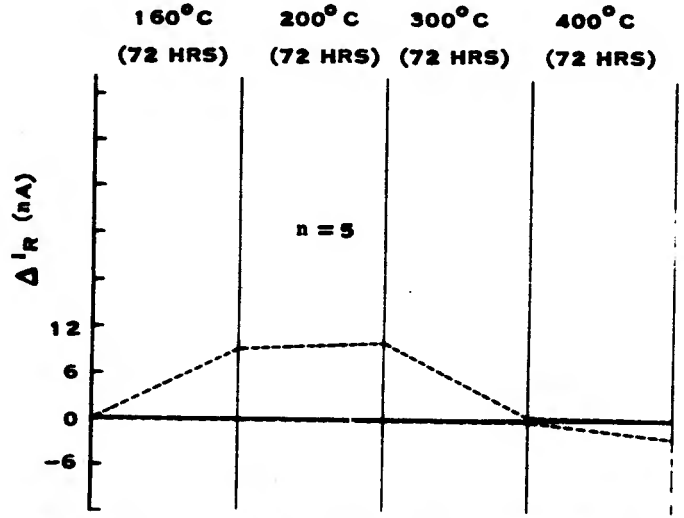


FIGURE B-5 DIODE I_R VARIATION WITH STORAGE STEP STRESS

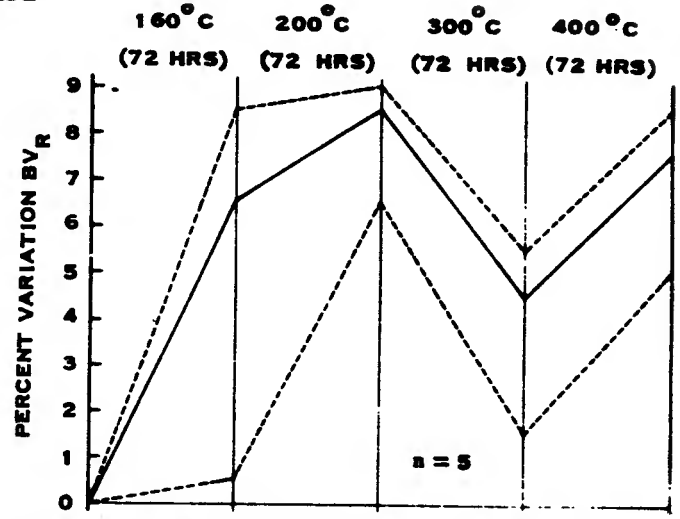


FIGURE B-6 PERCENT DIODE BV_R VARIATION WITH STORAGE STEP STRESS

SC07114

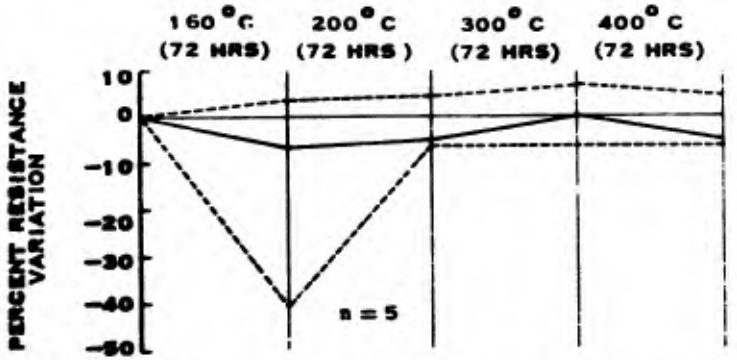


FIGURE B-7 PERCENT RESISTOR VARIATION WITH STORAGE STEP STRESS

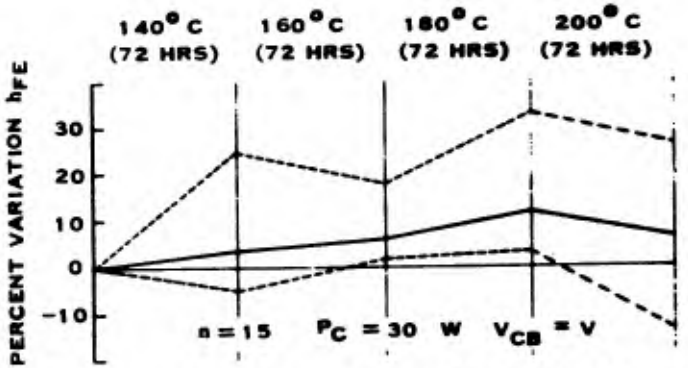


FIGURE B-8 PERCENT TRANSISTOR h_{FE} VARIATION WITH POWER DISSIPATION STEP STRESS

LEGEND:

--- MAX. INCREASE

—— MED. CHANGE

- - - MAX. DECREASE

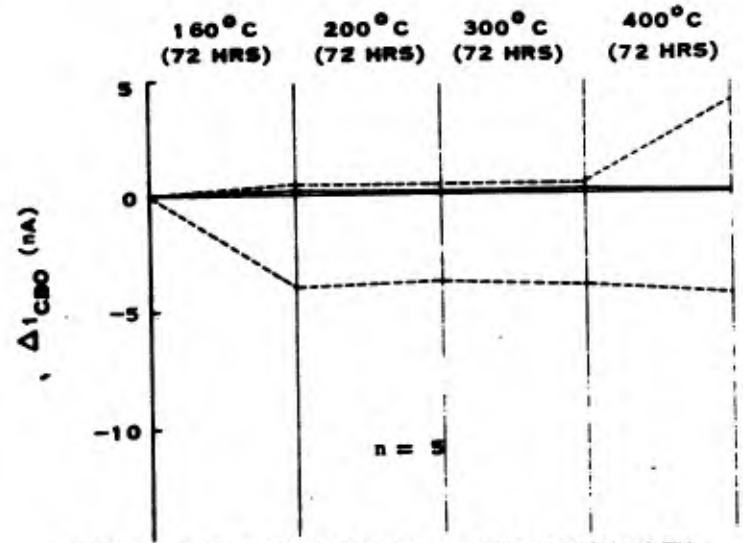


FIGURE B-9 TRANSISTOR I_{CBO} VARIATION WITH POWER DISSIPATION STEP STRESS

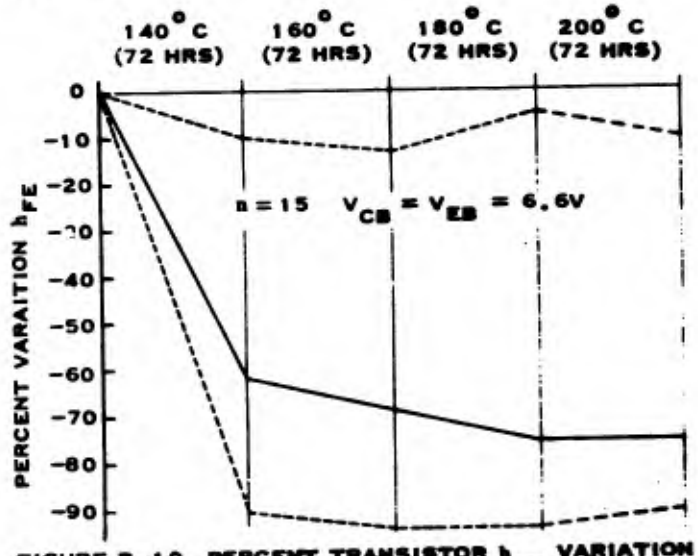


FIGURE B-10 PERCENT TRANSISTOR h_{FE} VARIATION WITH REVERSE BIAS STEP STRESS

SC07115

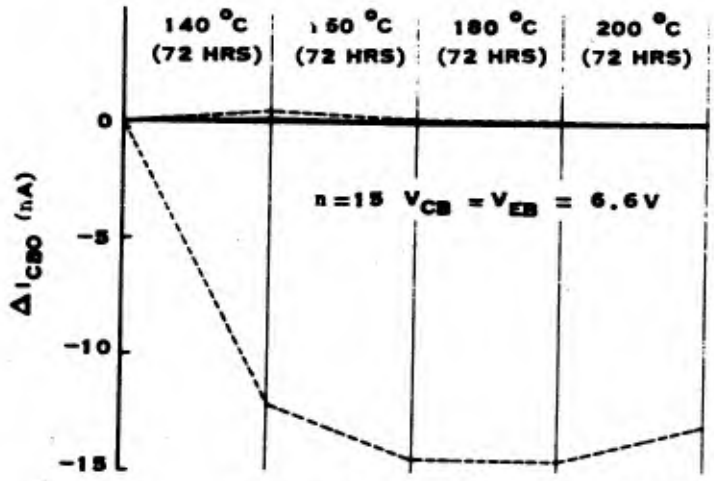


FIGURE B-11 TRANSISTOR I_{CBO} VARIATION WITH REVERSE BIAS STEP STRESS

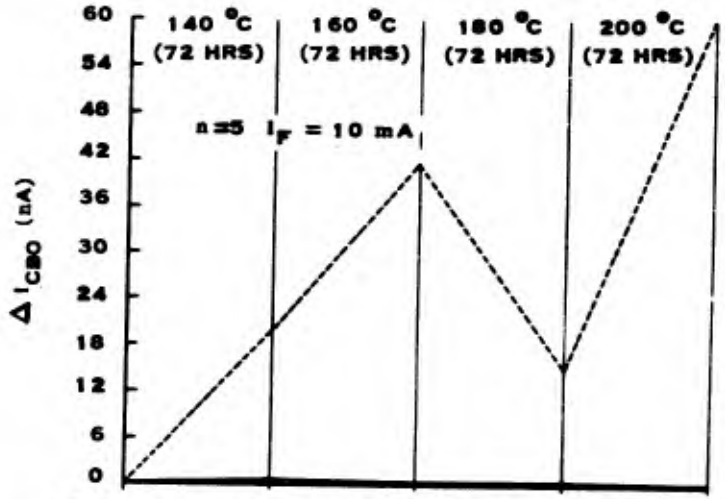


FIGURE B-12 DIODE I_R VARIATION WITH FORWARD BIAS STEP STRESS

LEGEND:
--- MAX. INCREASE
—— MED. CHANGE
--- MAX. DECREASE

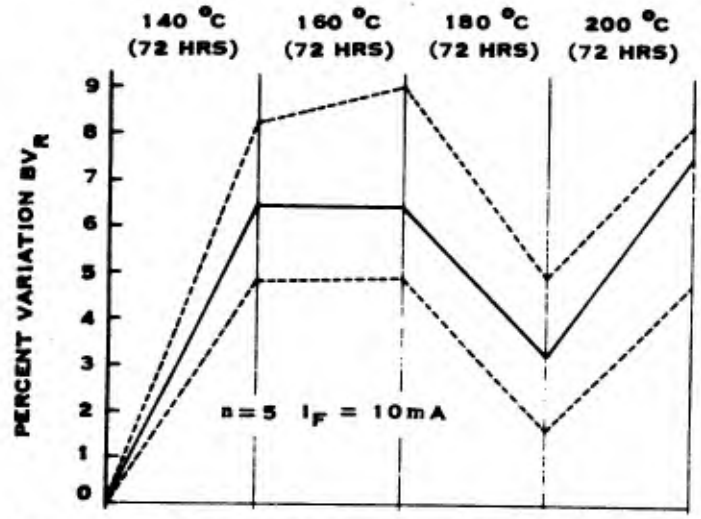


FIGURE B-13 PERCENT DIODE BV_R VARIATION WITH FORWARD BIAS STEP STRESS

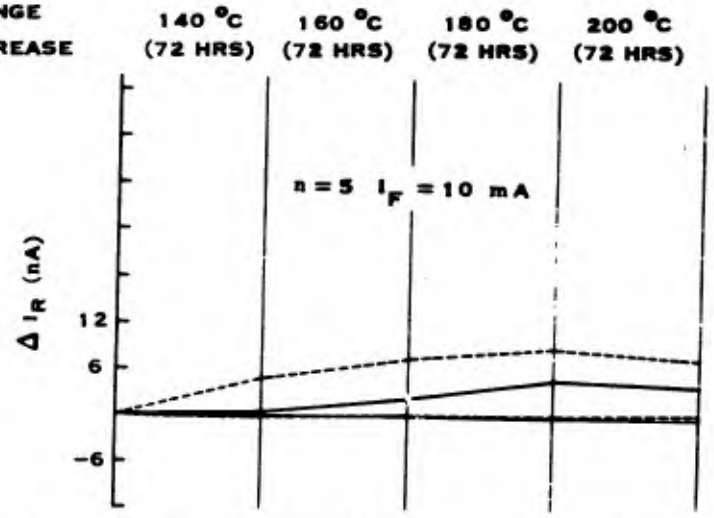


FIGURE B-14 DIODE I_R VARIATION WITH REVERSE BIAS STEP STRESS

SC07116

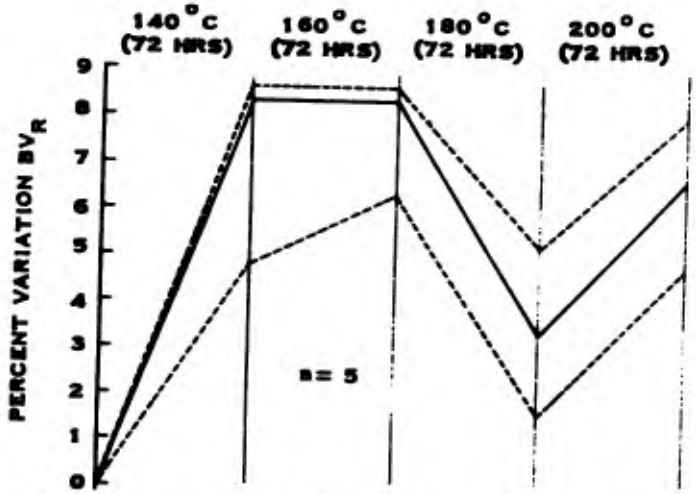


FIGURE B-15 PERCENT DIODE BV_R VARIATION WITH REVERSE BIAS STEP STRESS

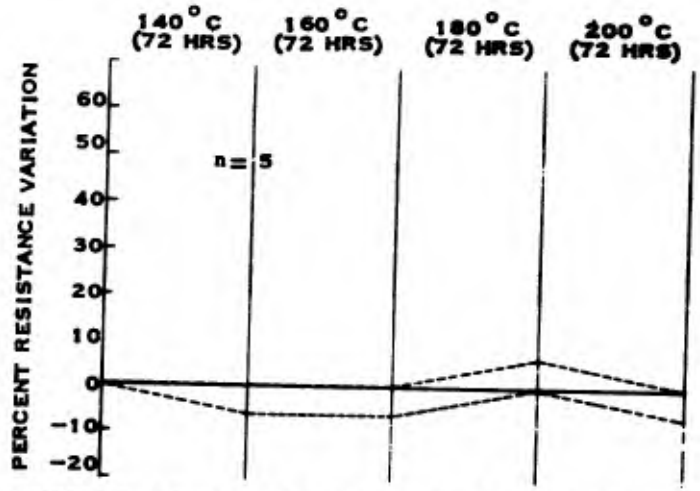


FIGURE B-16 PERCENT RESISTOR VARIATION WITH STORAGE STEP STRESS

LEGEND:
- - - MAX. INCREASE
—— MED. CHANGE
- - - MAX. DECREASE

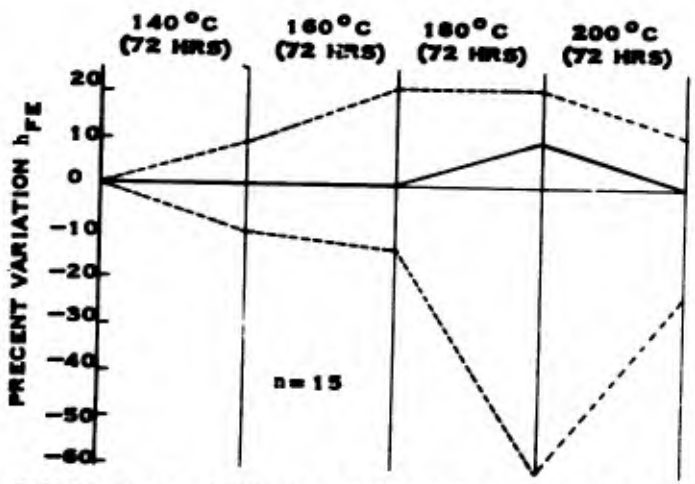


FIGURE B-17 PERCENT TRANSISTOR h_{FE} VARIATION WITH STORAGE STEP STRESS

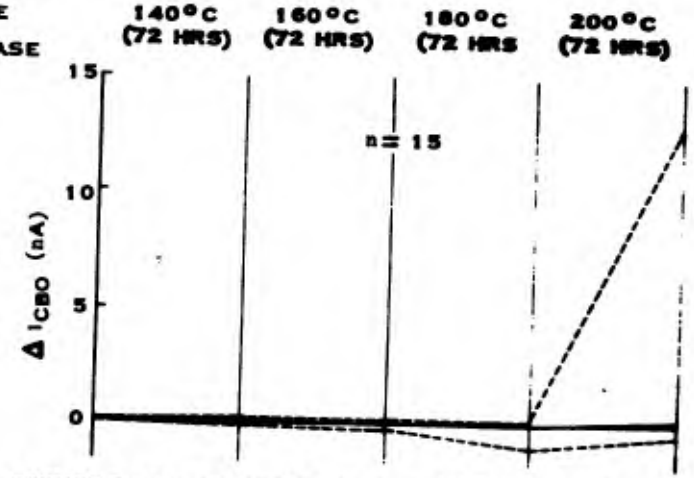


FIGURE B-18 TRANSISTOR I_{CBO} VARIATION WITH STORAGE STEP STRESS

SC07117

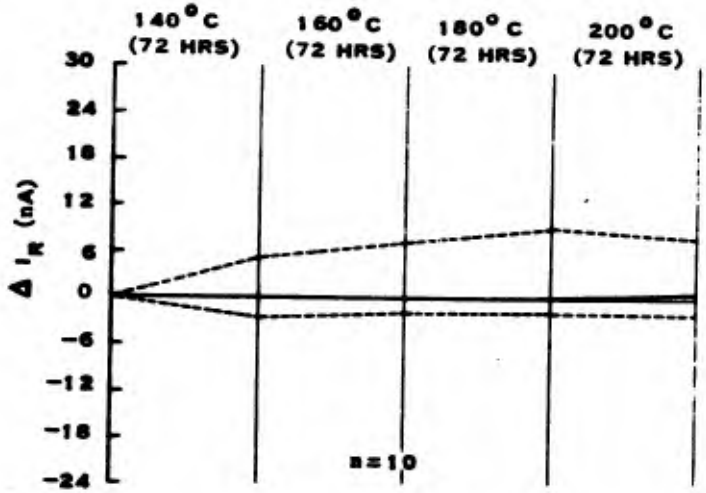


FIGURE B-19 DIODE I_R VARIATION WITH STORAGE STEP STRESS

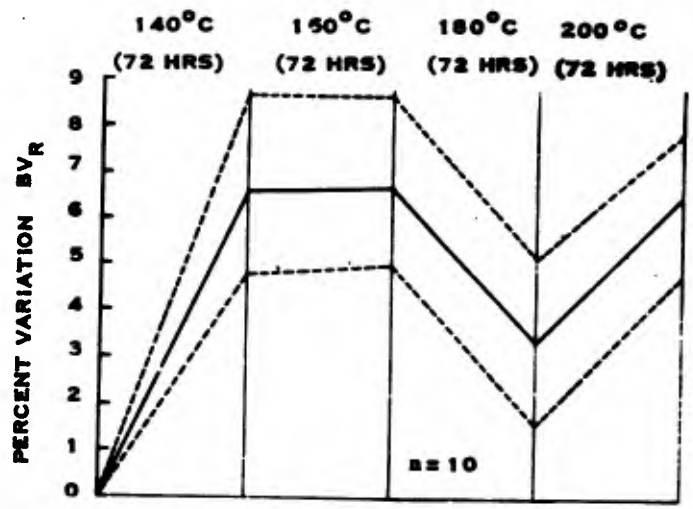


FIGURE B-20 PERCENT DIODE BV_R VARIATION WITH STORAGE STEP STRESS

LEGEND:

--- MAX. INCREASE

—— MED. CHANGE

- - - MAX. DECREASE

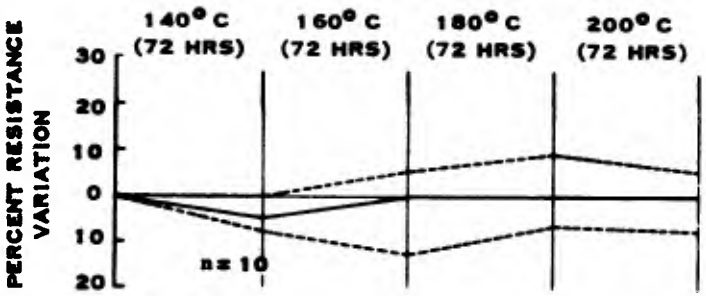


FIGURE B-21 PERCENT RESISTOR VARIATION WITH STORAGE STEP STRESS

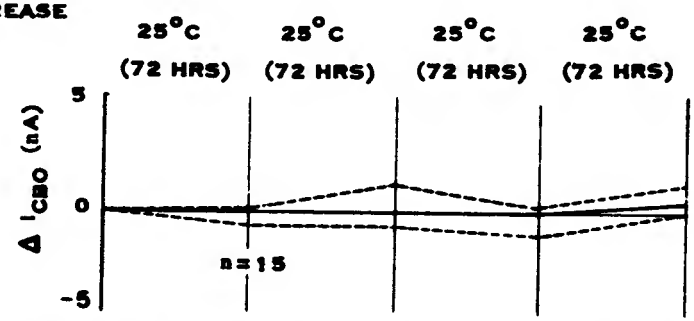


FIGURE B-22 TRANSISTOR I_{CBO} VARIATION; 25 °C CONTROL SAMPLE DATA

SC07118

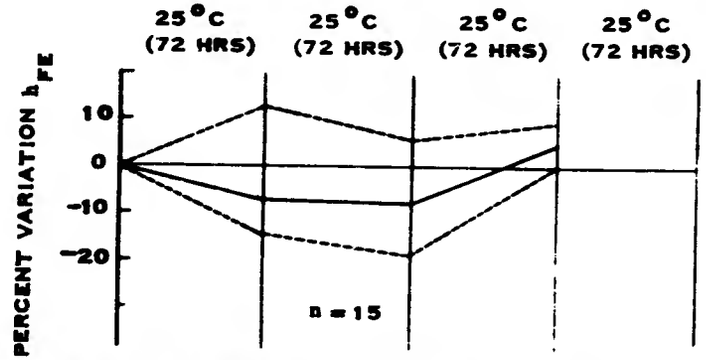


FIGURE B-23 PERCENT TRANSISTOR h_{FE} VARIATION 25°C CONTROL SAMPLE

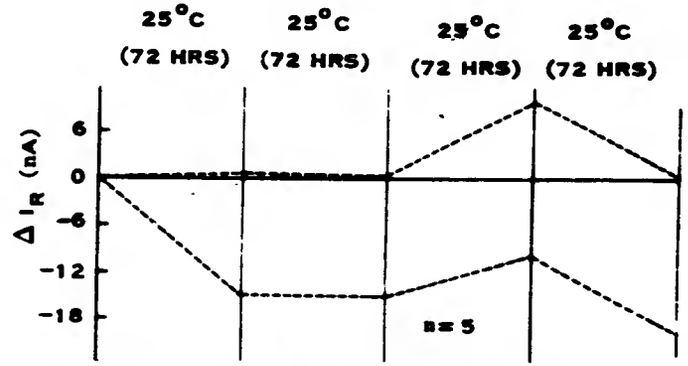


FIGURE B-24 DIODE I_R VARIATION; 25°C CONTROL SAMPLE

LEGEND:

--- MAX. INCREASE

—— MED. CHANGE

--- MAX. DECREASE

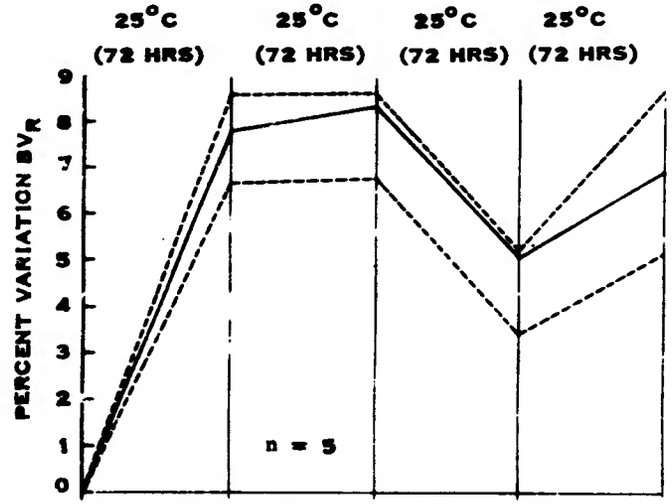


FIGURE B-25 PERCENT DIODE BV_R VARIATION; 25°C CONTROL SAMPLE

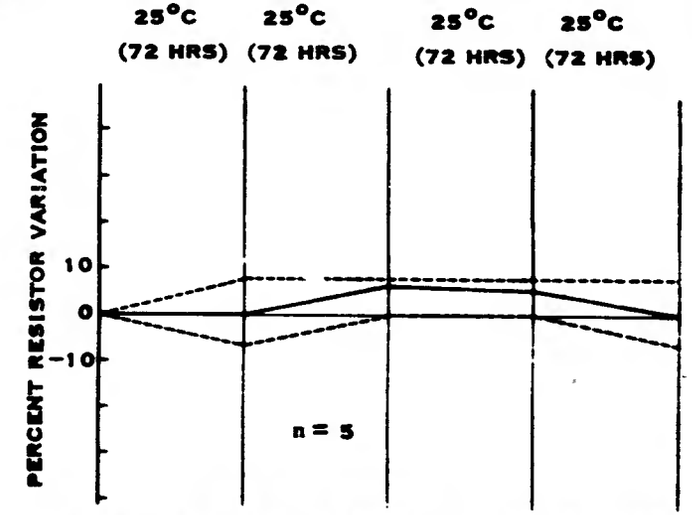


FIGURE B-26 PERCENT RESISTOR VARIATION; 25°C CONTROL SAMPLE

SC07119

The input transistor of bar number 1 showed an increase in h_{FE} after Step number 3 of the storage step stress test followed by a decrease after Step number 4. The V_{BEO} measurements plotted in Figure B-27 indicate that a slight channel is p.esent initially and that it is reduced at each successive step until the 4th step, where it suddenly increases to a value in excess of the initial value. This is probably due to the slight degradation of the devices when subjected to the excessive storage temperature of 400°C.

On the input transistor of bar number 4 the same phenomena was observed as with bar number 1. However, the V_{BEO} measurements indicated only a slight degradation in the higher level characteristics of the forward diode. This could account for the drop in h_{FE} after the fourth step.

On the output transistor of bar number 9 during the storage step stress test there was a decrease in h_{FE} and I_{CBO} after the 3rd step, followed by a recovery on the 4th step. The cause for this phenomenon is not known or explainable in terms of the information available from the test.

The input transistor on bar number 7 exhibited an increase in h_{FE} between the initial reading and the completion of the first step. The component was on power operating step stress from 140°C to 200°C. The initial data on V_{BEO} shown in Figure B-28 indicates that a slight channel is present and that it changed erratically during the test. This could well explain the slight h_{FE} instability displayed by the input transistor.

The input transistor on bar numbers 16 and 17 exhibited a drastic degradation in h_{FE} between the initial and the completion of the first step. The unit was subjected to reverse bias step stress from 140°C to 200°C. The V_{BEO} measurements shown in Figures B-29 and B-30 indicate that a severe channel was formed during the first step and that subsequent steps caused it to approach a saturation value. V_{BEO} measurements of a typical control sample not subjected to any stress are shown in Figure B-31.

The small transistor on bar number 16 was subjected to storage step stress from 140°C to 200°C. On the fourth step there was an increase in I_{CBO}. The exact cause for this is unknown.

The input transistor on bar number 16 was subjected to storage step stress from 140°C to 200°C. After the first step of the stress test there was a decrease in h_{FE}. At the same time I_{CBO} decreased to about one-half its initial value. The V_{BEO} measurement indicated a channel had developed at the E-B junction. It is suspected that the same factors that caused h_{FE} to decrease caused I_{CBO} to decrease.

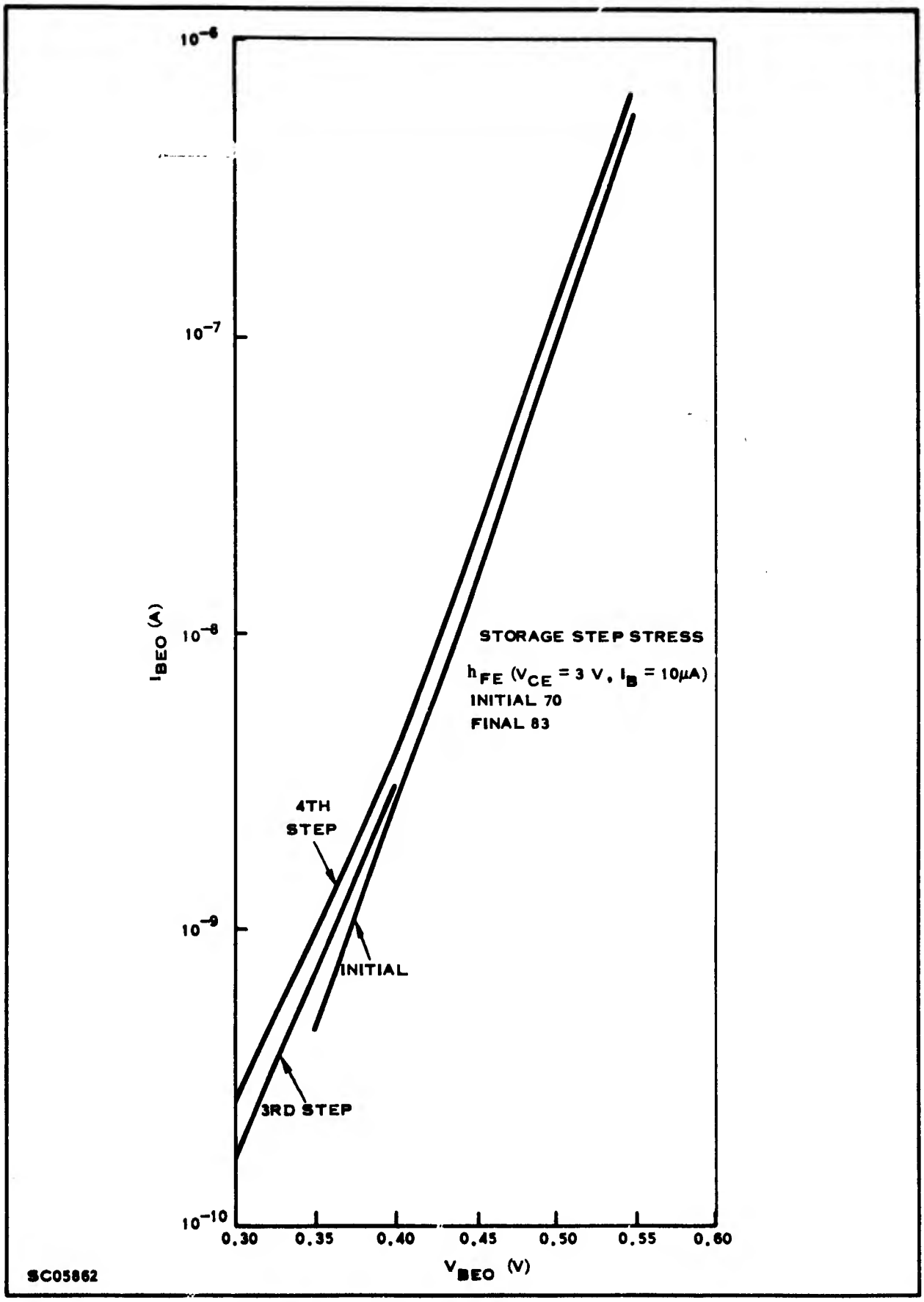


Figure B-27. I_{BEO} vs V_{BEO} for Unit No. 1

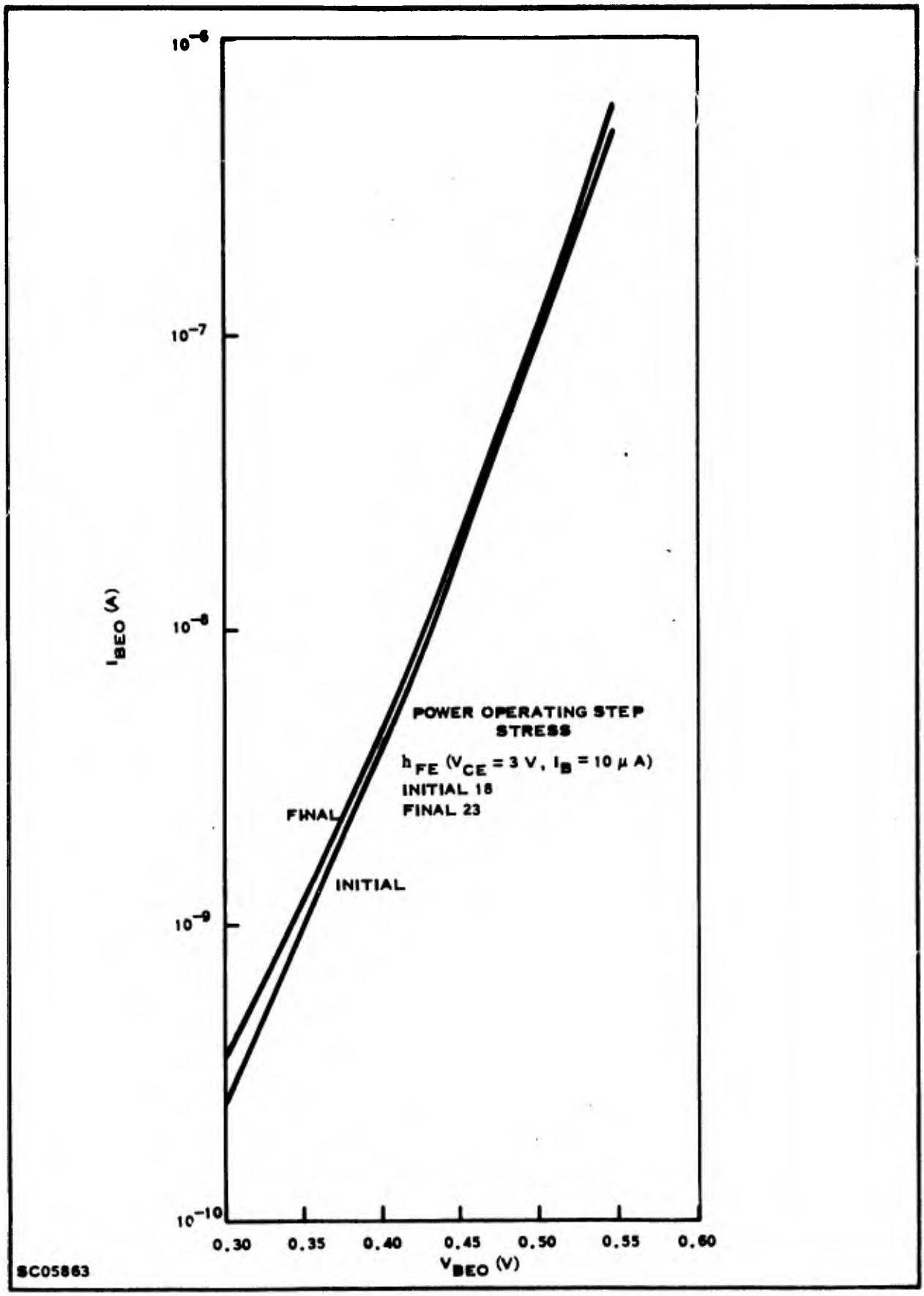


Figure B-28. I_{BEO} vs V_{BEO} for Unit No. 7

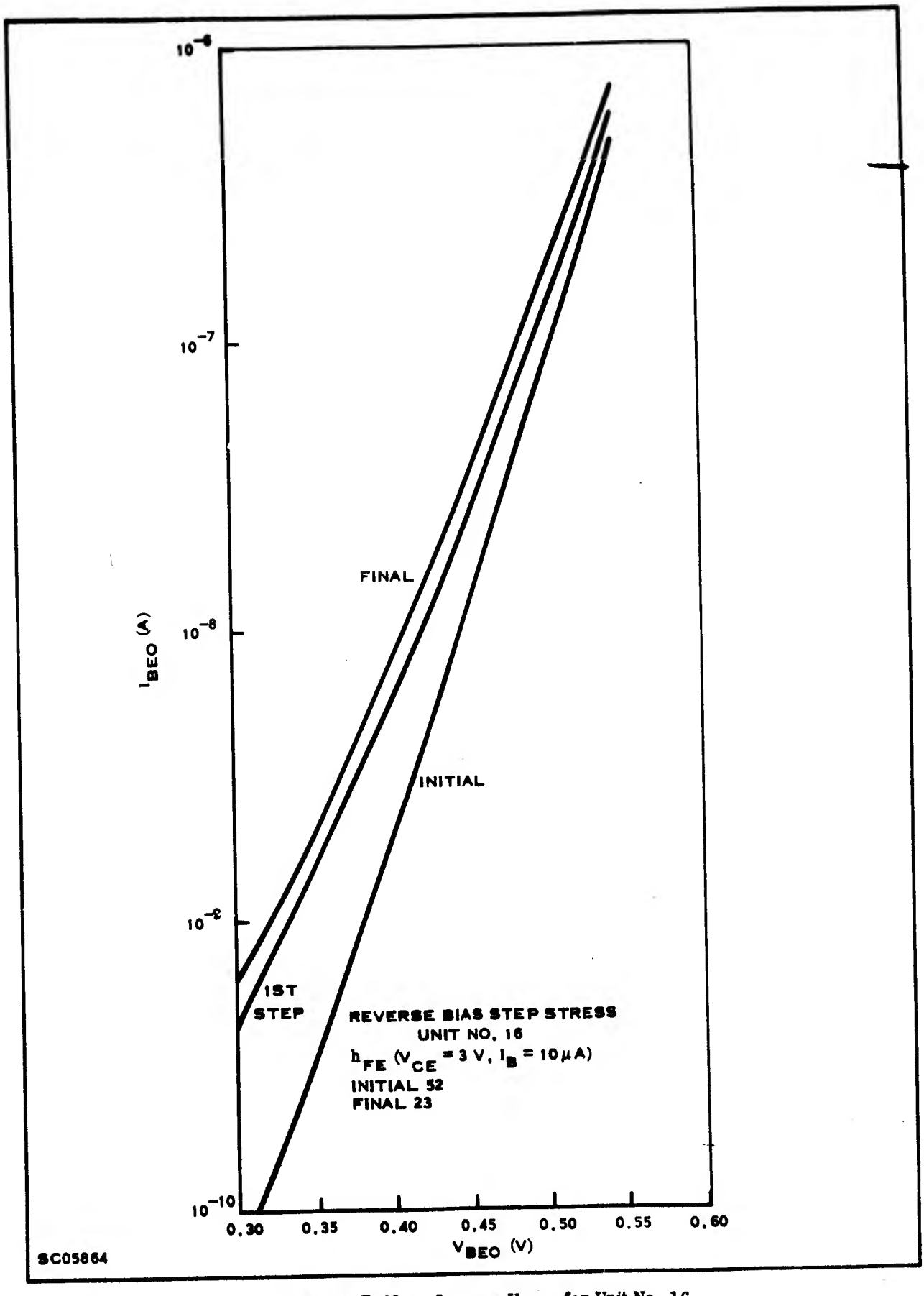


Figure B-29. I_{BEO} vs V_{BEO} for Unit No. 16

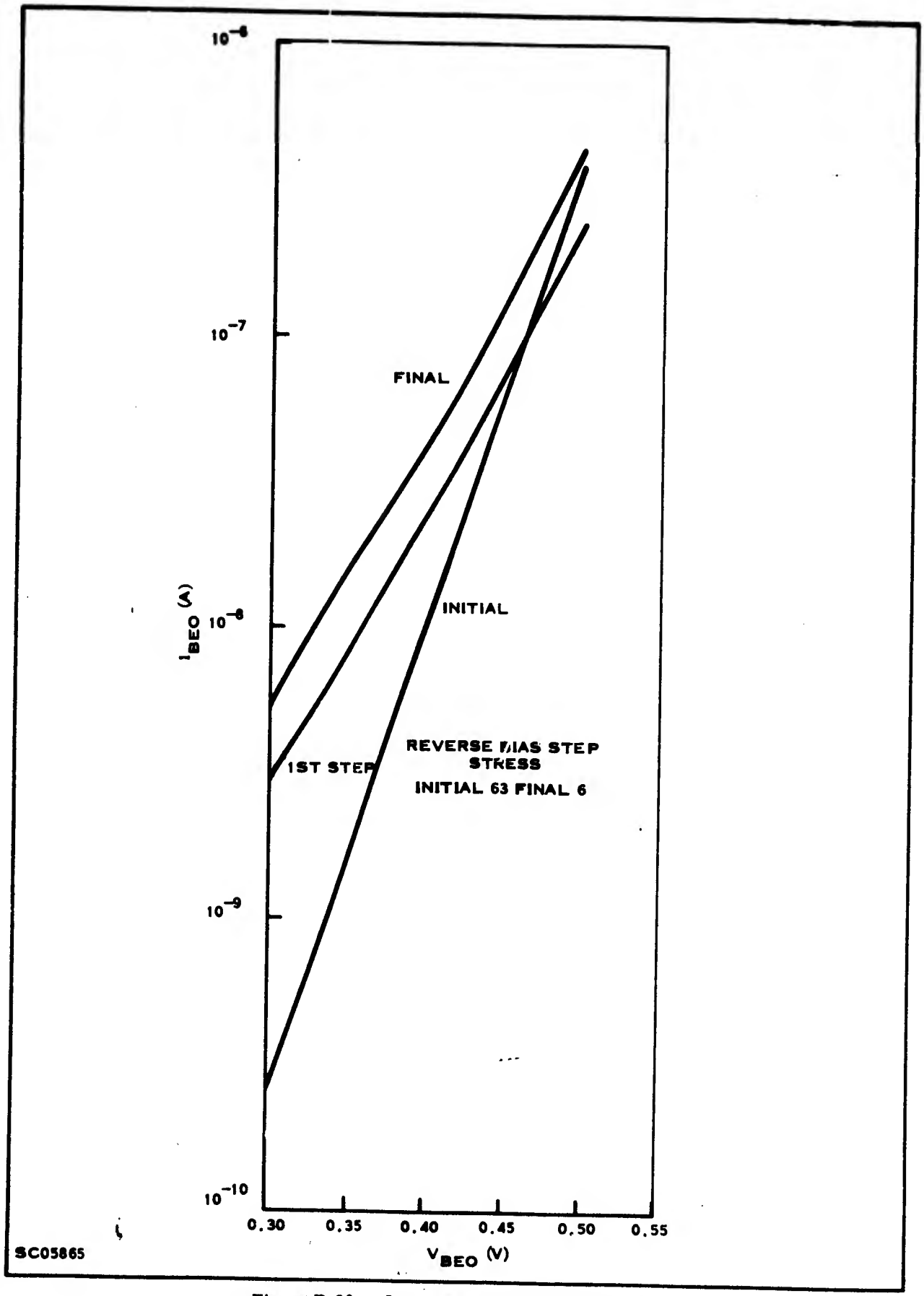


Figure B-30. I_{BEO} vs V_{BEO} for Unit No. 17

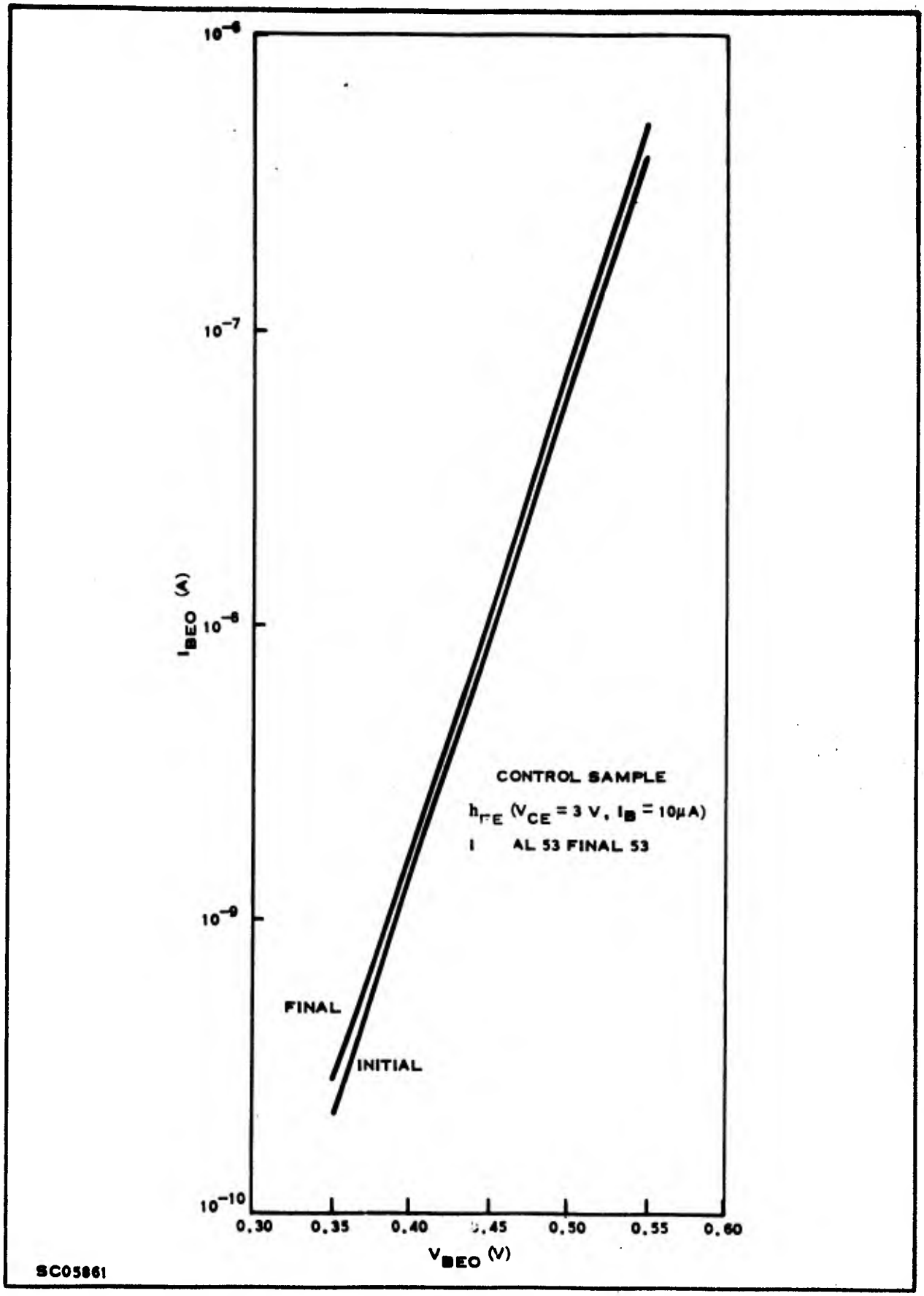


Figure B-31. I_{BEO} vs V_{BEO} for Unit No. 24

The diode on bar number 5 exhibited an increase in I_R after the initial step of stress which was storage at 160° C. No explanation for this behavior can be made at this time.

The diode on bar number 8 showed an increase in I_R after being subjected to forward bias conditions. Such large changes are probably due to surface contamination, a defect in the oxide or a similar physical defect in the device.

The resistor on bar number 3 displayed a large decrease in resistance on the first stress level of storage step stress. Since all the later step readings are well within tolerance it is suspected that the first step reading is erroneous.

The resistor on bar number 6 was slightly out of tolerance after the second step of storage step stress. Since the later steps returned the component to within tolerance, no determination of the out of tolerance condition could be made.

6. TECHNICAL DISCUSSION

The common emitter forward current gain can be degraded by the reverse biasing of the emitter-base junction into the avalanche region. The phenomenon can be accelerated by elevated ambient temperatures. This effect is more easily produced on devices having a narrow base region and shallow diffusions. The forward emitter-base current characteristics are an excellent indicator of the cause of h_{FE} degradation. This characteristic was measured initially and after each step in the stress program. Figures B-27, B-28, B-29, B-30 and B-31 are representative characteristics, respectively, of units 1, 7, 24, 16, and 17. Note that unit number 7, a typical unit from power operating step stress, is essentially no different from a typical control unit (number 24). Neither unit exhibited any h_{FE} degradation.

Unit number 1 from storage step stress exhibited a slight increase in the slope of the exponential emitter-base current characteristic when plotted against forward bias voltage. This unit also demonstrated a slight degradation in h_{FE}. The suspected mechanism is channeling of the emitter-base junction, described by Sah, Moyce and Shockley [10, 11, 12] to be caused by inversion of N-type silicon. While cause of the channel formation is not known with certainty, mismatch of thermal expansion coefficients between oxide and silicon, and the presence of impurities in oxide such as sodium are possibilities.

A more pronounced increase in slope of the V_{BEO}-I_B data is observed in devices subjected to reverse bias step stress. Refer to Figures B-30 and B-31 for illustrations. These results also indicative of emitter-base channel formation, correlate well with the severe h_{FE} degradation which occurred in these devices.

APPENDIX C

COMPUTER PROGRAMS — SERF AND LINDA

For ease of reference this Appendix is in two parts. The first part contains a general description of the computer program SERF followed by a flow chart (Figure C-1). The last part contains a discussion of the theory relevant to linear discriminant analysis LINDA.

1. SERF

One of the computer programs written to isolate preindicators of failure and to establish screening criteria is an adaptation of the reliability screening techniques developed by Bevington and Ingle.[13] The SERF program (Screening Efficiency Reliability Factors) described here embodies some of the major features of the Sigma 6 program used by the above authors. The relative screening efficiencies of up to 40 measured parameter values, as well as delta and percent change of these values, a total of 120 parameters on up to 100 components are determined from input data. We use the term parameter in the following discussion to mean any electrical quantity together with the conditions (e.g., time, thermal stress, electrical stress, etc.) under which it is measured.

We may use the electrical parameter data at any readout step to predict the failures which were detected at a later readout step. One group of control cards read in with the measurement data are "failure cards" which identify at which readout step each failure was first detected. All devices which become failures at a later readout step than the readout step at which screening is being done are included, along with the devices, in the sample to be screened.

The optimum screening criterion is derived by maximizing either the screening efficiency

$$e = \frac{\% \text{ failures removed}}{\% \text{ population removed}}$$

or

$$e^* = 0.5 + 0.5\,(F_f - F_g)$$

where

F_f = fraction of total failures removed

and

F_g = fraction of total good devices removed.

for a fixed number of screening levels for each parameter; the criterion is expressed as a series of truncation levels for the parameters considered in the calculation. Basically the program provides a means of evaluating the predictive efficiency obtainable by using varying parameters and varying test conditions.

We will assume that we are screening n devices ($n \leq 100$) having m parameters ($m \leq 40$). After the input data has been read in, the range of each parameter is partitioned into 20 subintervals (cells) and the two out-of-limits categories added to bring the total number of cells for each parameter to 22. Parameter values for each component are then examined, and the number NT_{ij} of components whose i^{th} parameter value lies in cell j recorded, producing an m x 22 matrix of values. Simultaneously, the number NF_{ij} of later failures "in" each cell is recorded, producing a second m x 22 matrix.

Next, the cumulative number CN_{1jk} (and the number CF_{1jk} of later failures) which would be removed by screening of parameter 1 at the jth lower level and kth upper level ($1 \leq j \leq k \leq 22$) is computed and the resulting 22 x 22 matrices are used to calculate the screening efficiency values

$$E_{1jk} = \left(\frac{CF_{1jk}}{F}\right) \Big/ \left(\frac{CN_{1jk}}{N}\right) \tag{1}$$

or

$$E^*_{1jk} = \frac{1}{2} + \frac{1}{2}\left(\frac{CF_{1jk}}{F} - \frac{CN_{1jk} - CF_{1jk}}{N - F}\right) \tag{2}$$

The maximum value of E_{1jk} (or E^*_{1jk}), $E_{1j_1k_1}$ (or $E^*_{1j_1k_1}$) is calculated and stored along with j_1 and k_1. If the maximum is not unique, the number of components removed is maximized in selecting the optimum screening state (j_1, k_1). This procedure is continued for all m parameters and the maximum value of all these screening efficiencies, $\tilde{E}_{ij_ik_i}$ is calculated and stored, along with i, j_i and k_i. Devices having parameter i values in cells 1 to j_i and k_i to 22 are the screened devices.

The components to be deleted are identified by serial number. The following information is printed:

screening criterion (parameter number and level)

sample size

number screened

number of failures screened

percent of sample removed in screening

percent failures in screened group

percent failures and good present at the end of the previous screening level which were removed by the current screening

cumulative percent of the number of prescreening failures and good which were removed at the end of the current screening

screening efficiency achieved.

The specified termination mode is then examined and the problem terminated if the criterion is satisfied. If not, the parameter data is revised by deletion of the components screened; the data is revised to reflect the number of components and later failures remaining, and a second screening pass initiated.

In summary, the SERF program may be used to select the sequence of screening levels on a set of parameter values which produce the optimum screening efficiency as indicated above. By altering the combinations of parameters and/or failure criteria, information may be extracted concerning the best indicators of specific failure modes. Both failure and parameter are used here in the broadest sense. Any condition of interest may be used to identify elements as "failures"; any condition or quality to which a meaningful numerical value can be assigned may be used as a parameter.

The results of the screening analysis may be used to identify sensitive indicators of particular conditions, or to establish practical screening levels as required. The sequence of screening passes may be terminated at any level in establishing such screens, contingent on the percentage of the failures or total population it is desired to remove.

A number of options are provided to increase the usefulness of the program. Changing the failure criteria will redefine failures and could result in entirely different screening results. By simply changing the "failure cards" the data can be screened again to explore the effects of the new failure criteria.

Screening may be terminated either by specifying the number of screening passes or else by supplying a lower boundary on the screening efficiency below which screening is terminated.

Upper and lower limits for the range of each parameter are used for the 20 cell partitioning as well as the specification of the two out of range cells. A good cell selection will use cells as small as possible to minimize clustering of many parameter values of both good and bad devices in a few cells, preventing clean separation of the outliners. One option for constructing the cells uses the maximum and minimum parameter values as the upper and lower limits. After the parameter values have been distributed among the cells, the cells are examined in sequence starting from both the lowest and highest cell until a cell is detected at each end which contains a parameter value of a good unit. The parameter values which define the lower limit of this low cell and the upper limit of this high cell are used as the new lower and upper limits of the parameter range. A new set of cells is then constructed. Thus in effect the parameter values of the bad units are moved to the out of range cells and the resolution of the cell partitioning increased.

Alternatively the user may specify his own upper and lower limits or else, assuming the parameter values are normaily distributed, and the mean and standard deviation of each parameter is computed and $\mu-3\sigma$ is used as the lower limit and $\mu+3\sigma$ used as the upper limit.

Provision has been made to allow screening on any subset of the parameters read in and further to allow specification of a list of parameters to be screened on one at a time and in the order specified.

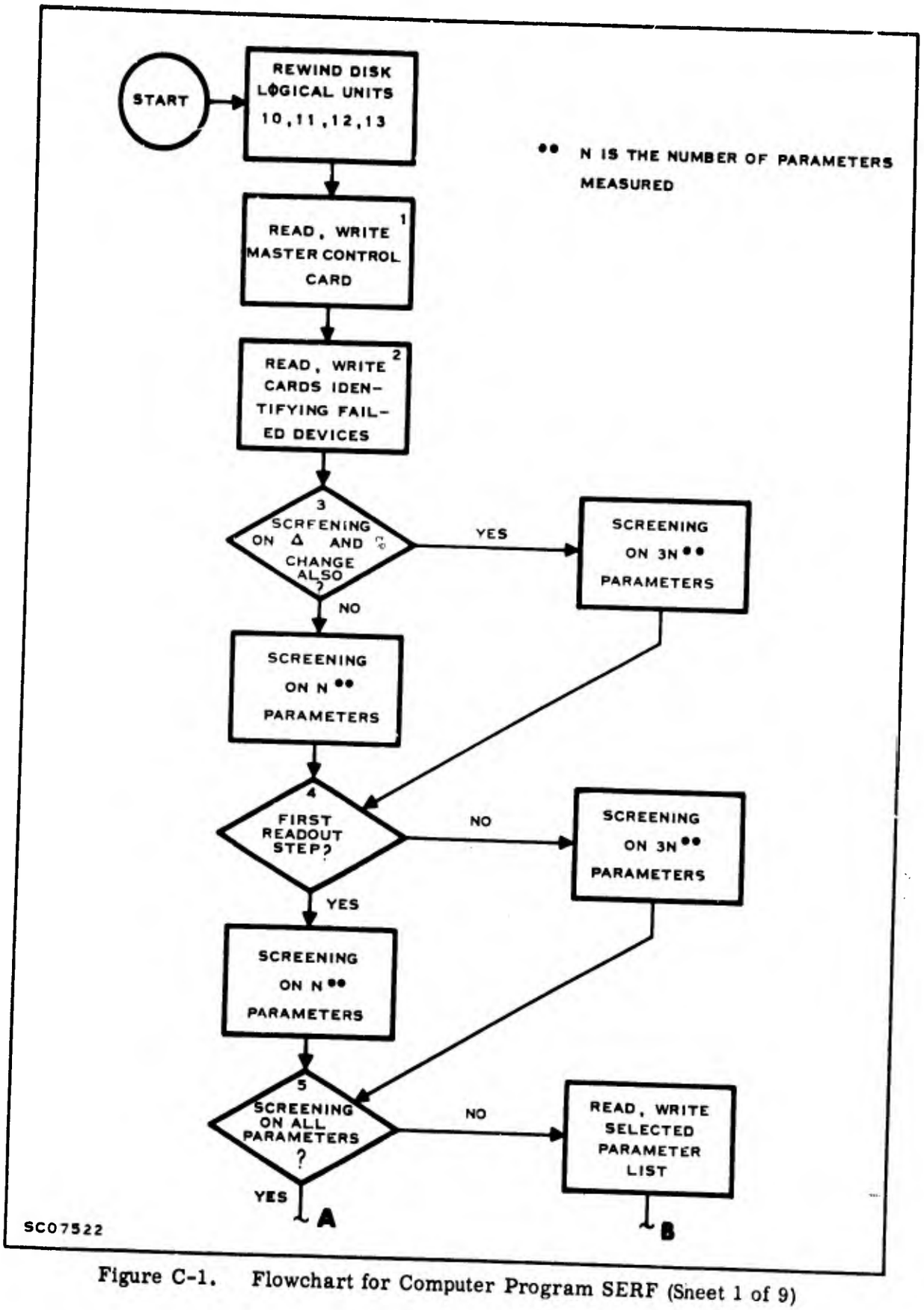


Figure C-1. Flowchart for Computer Program SERF (Sheet 1 of 9)

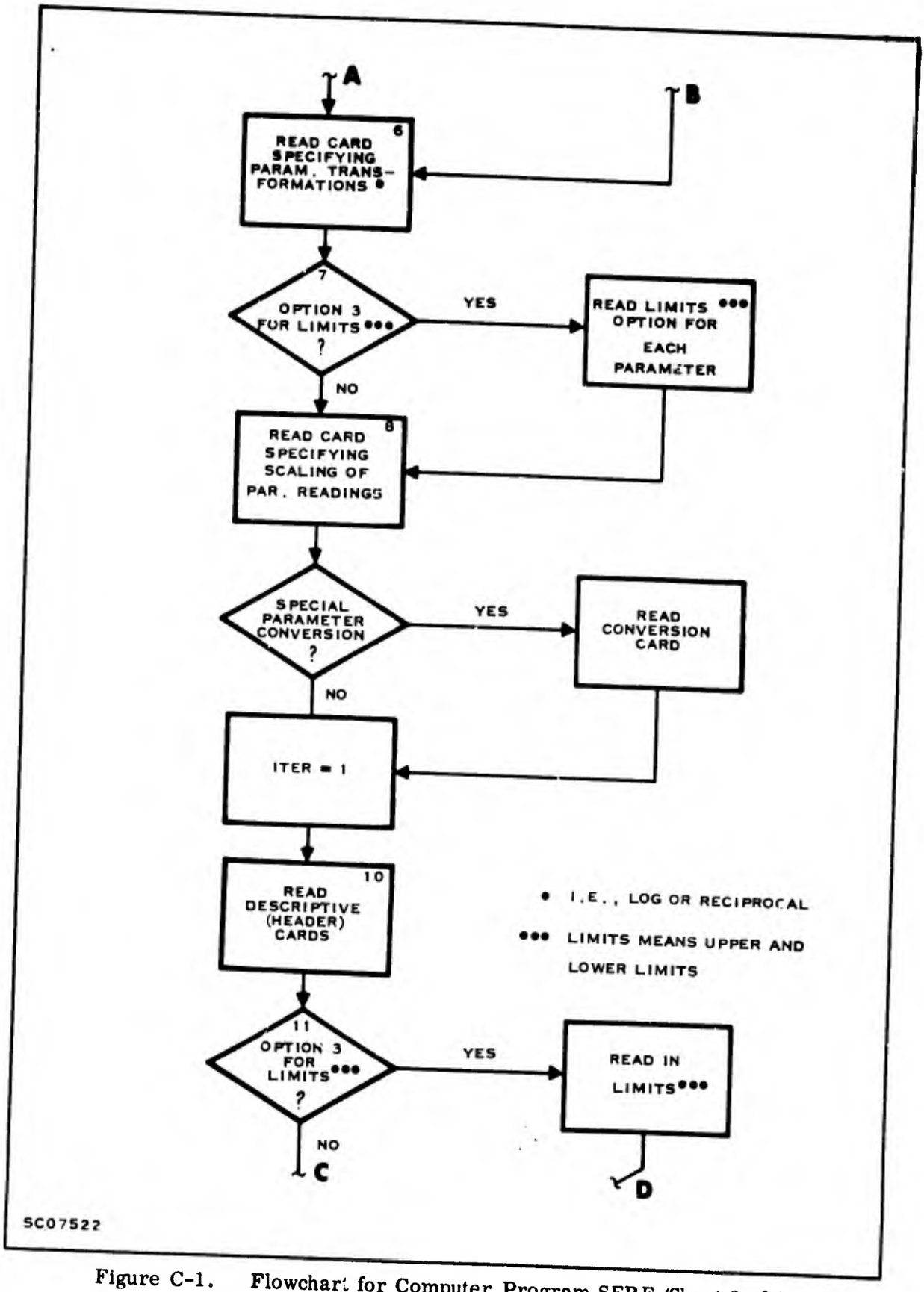


Figure C-1. Flowchart for Computer Program SERF (Sheet 2 of 9)

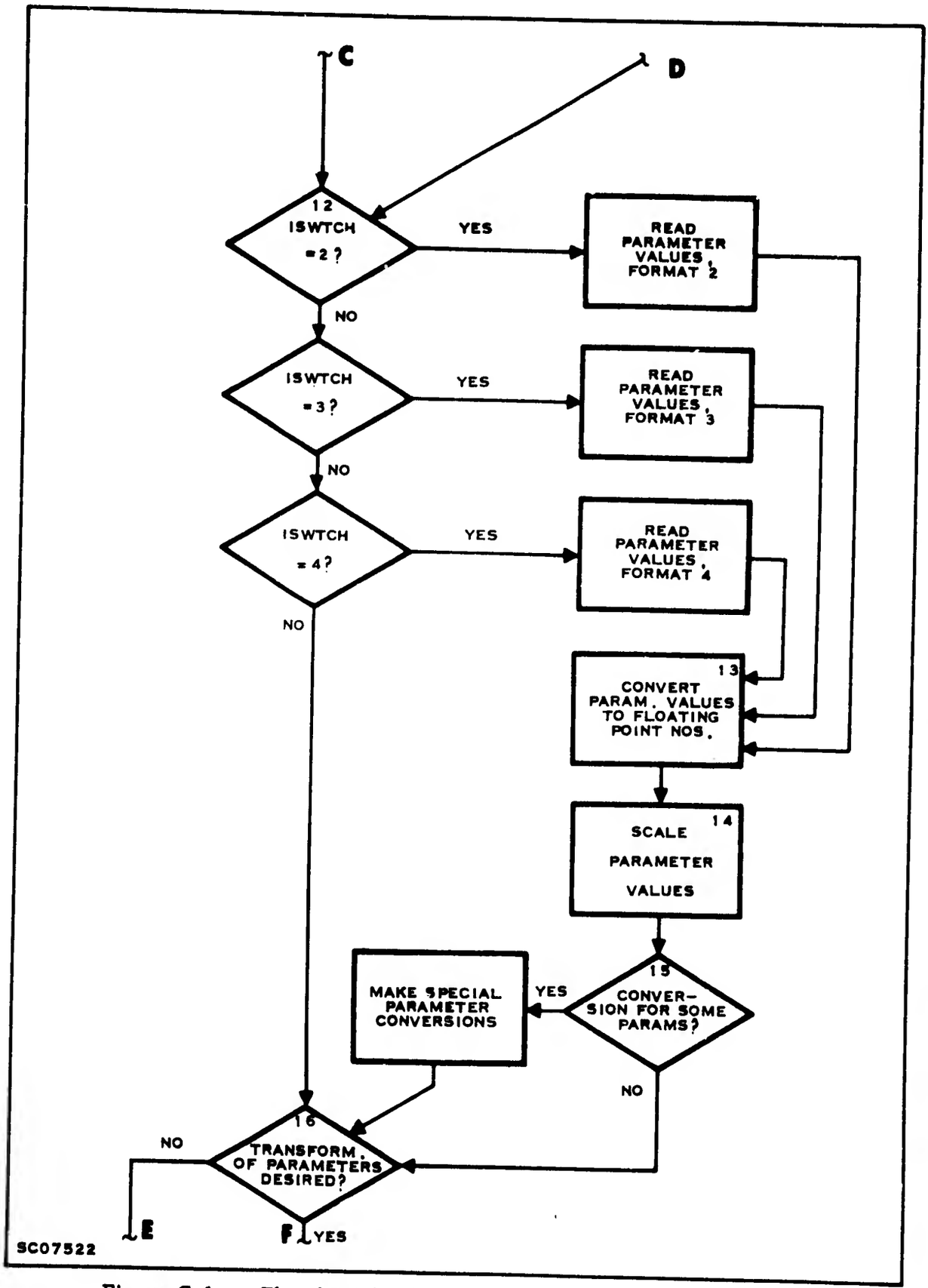


Figure C-1. Flowchart for Computer Program SERF (Sheet 3 of 9)

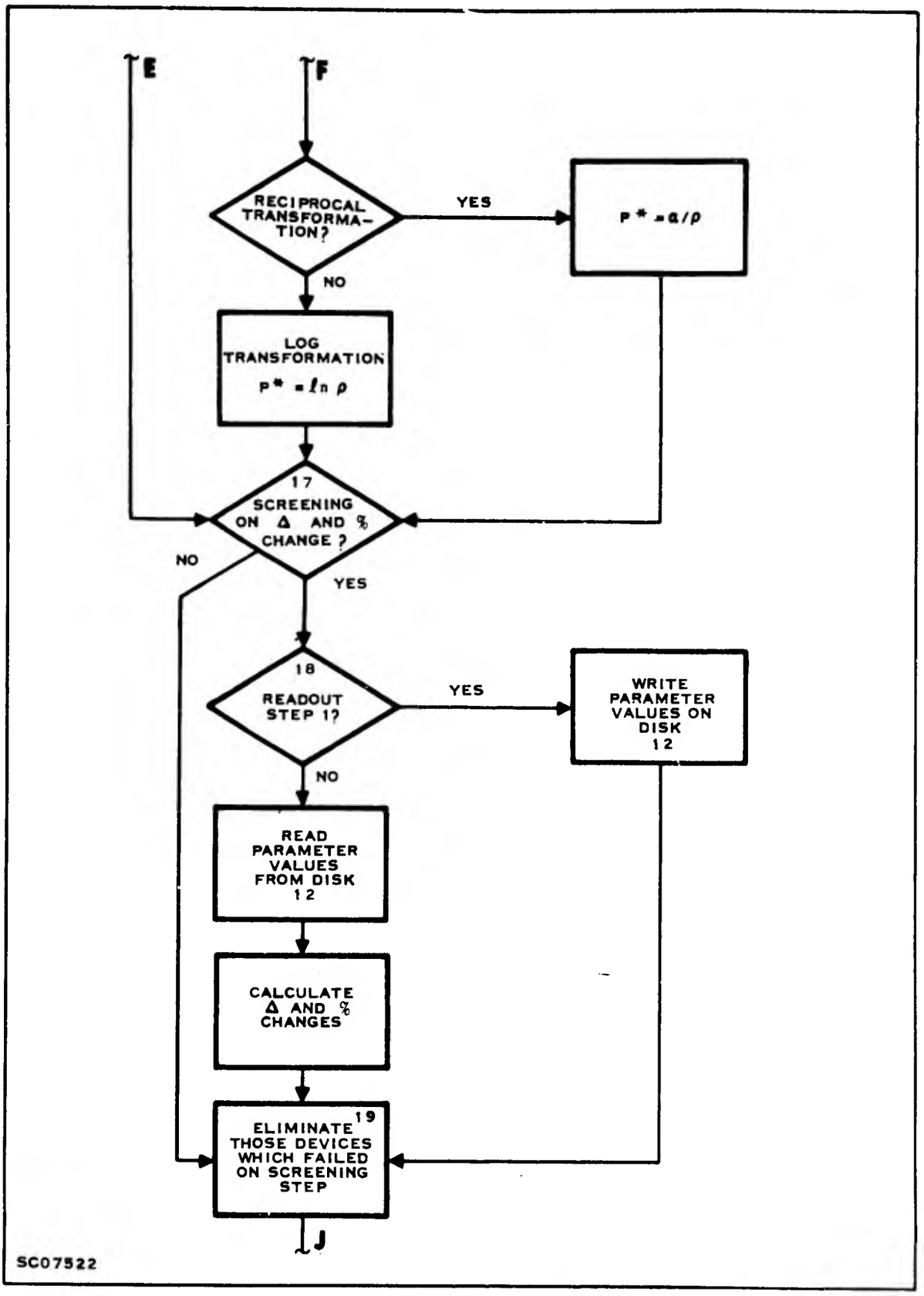


Figure C-1. Flowchart for Computer Program SERF (Sheet 4 of 9)

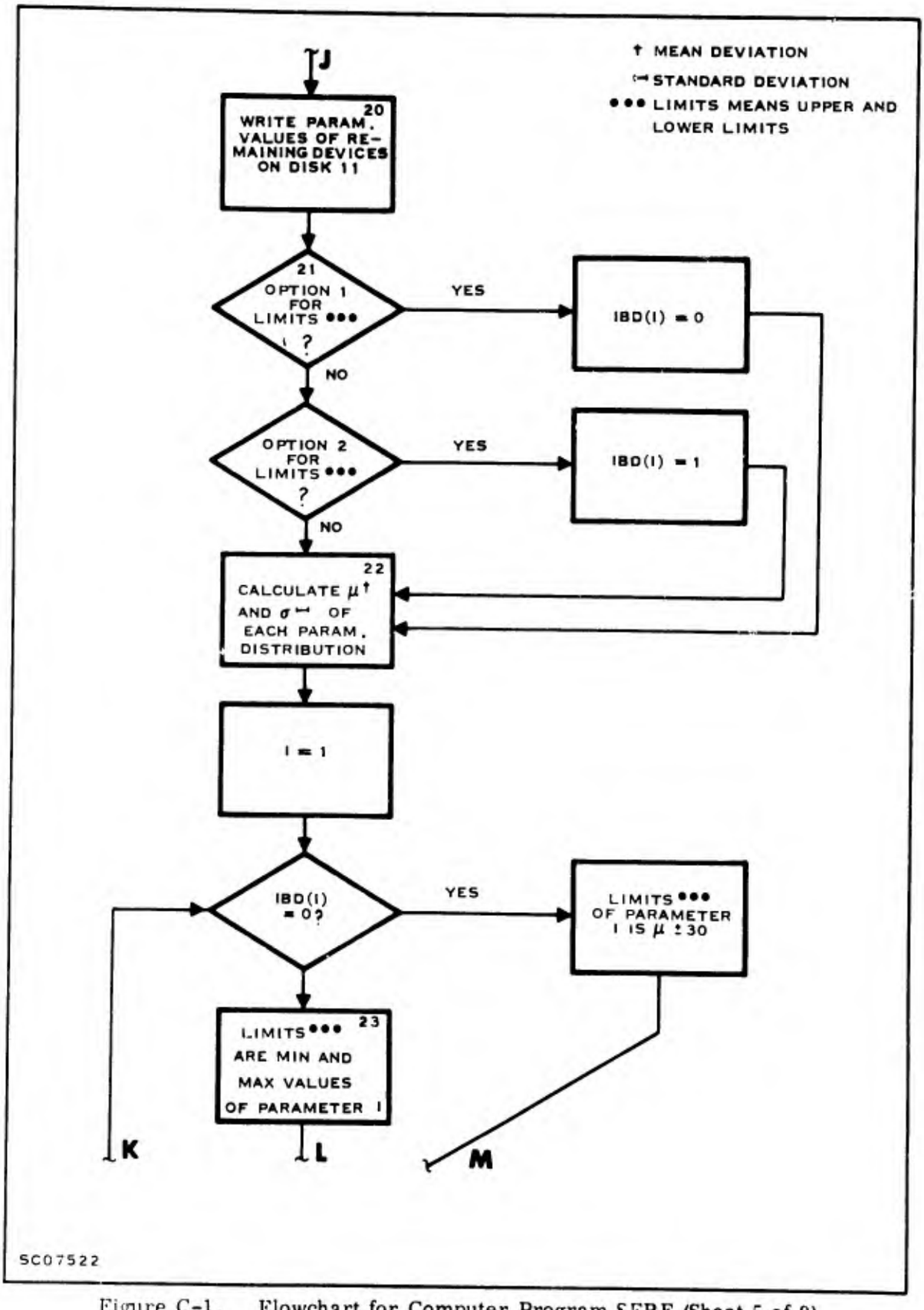


Figure C-1. Flowchart for Computer Program SERF (Sheet 5 of 9)

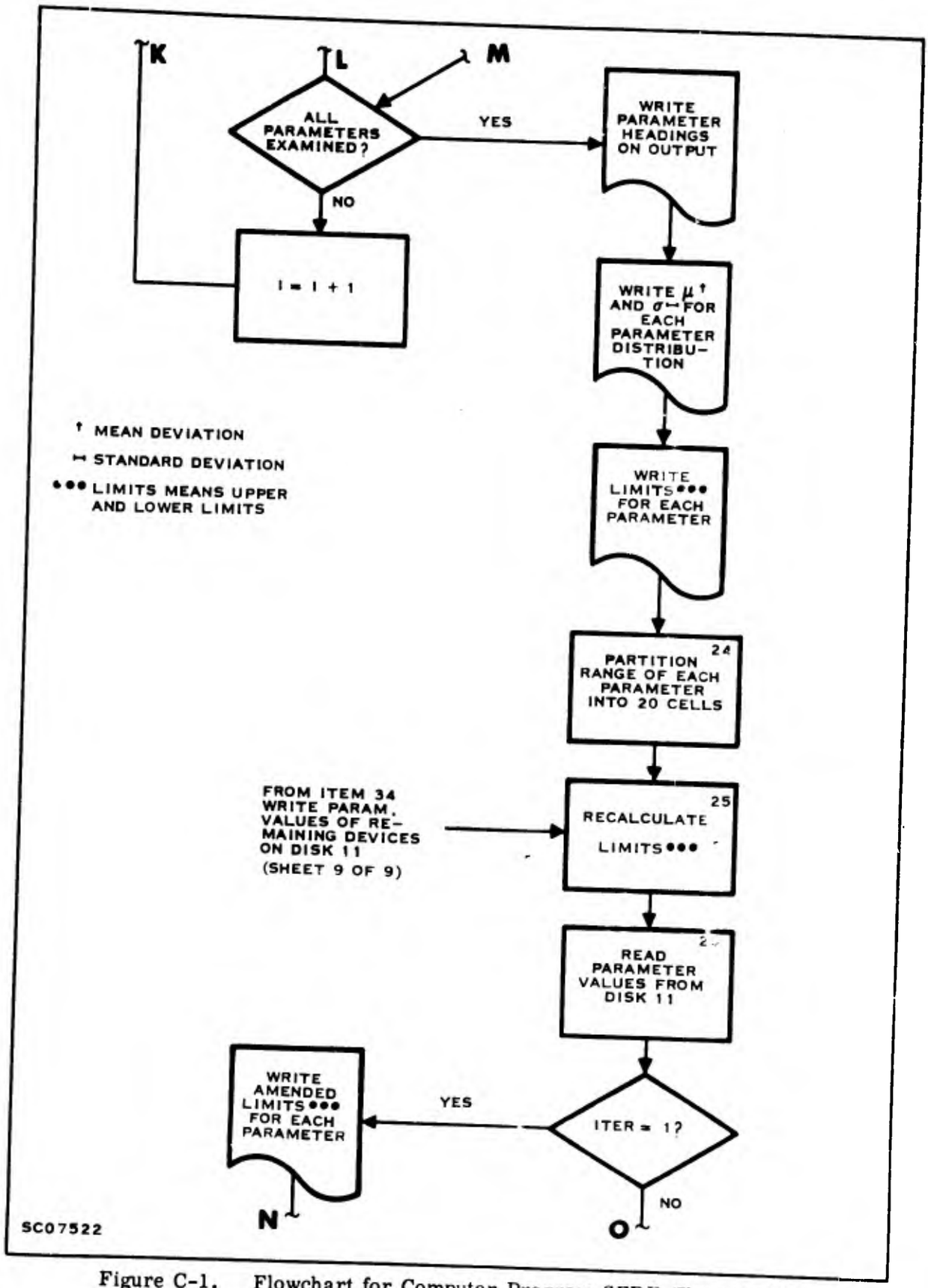


Figure C-1. Flowchart for Computer Program SERF (Sheet 6 of 9)

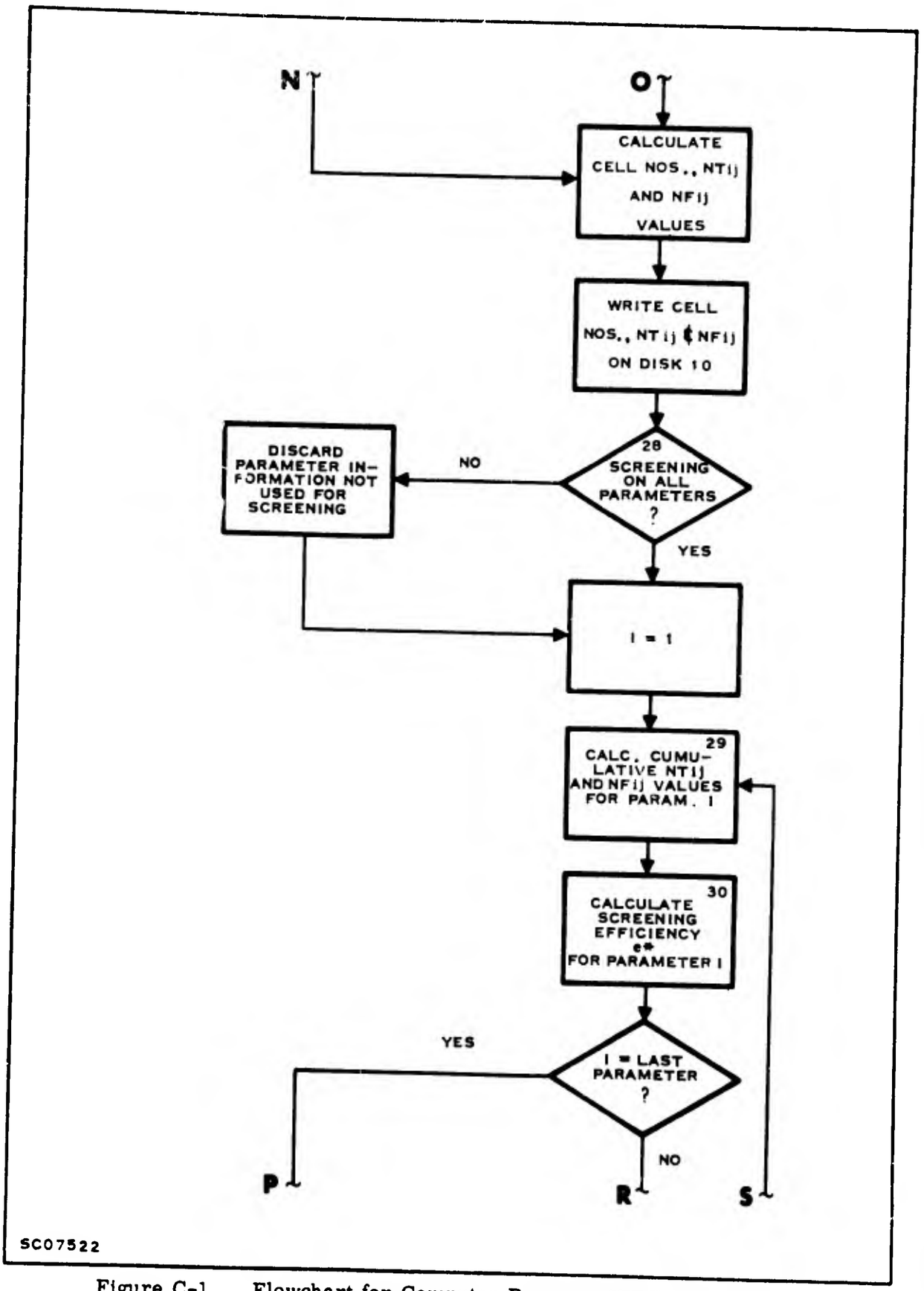


Figure C-1. Flowchart for Computer Program SERF (Sheet 7 of 9)

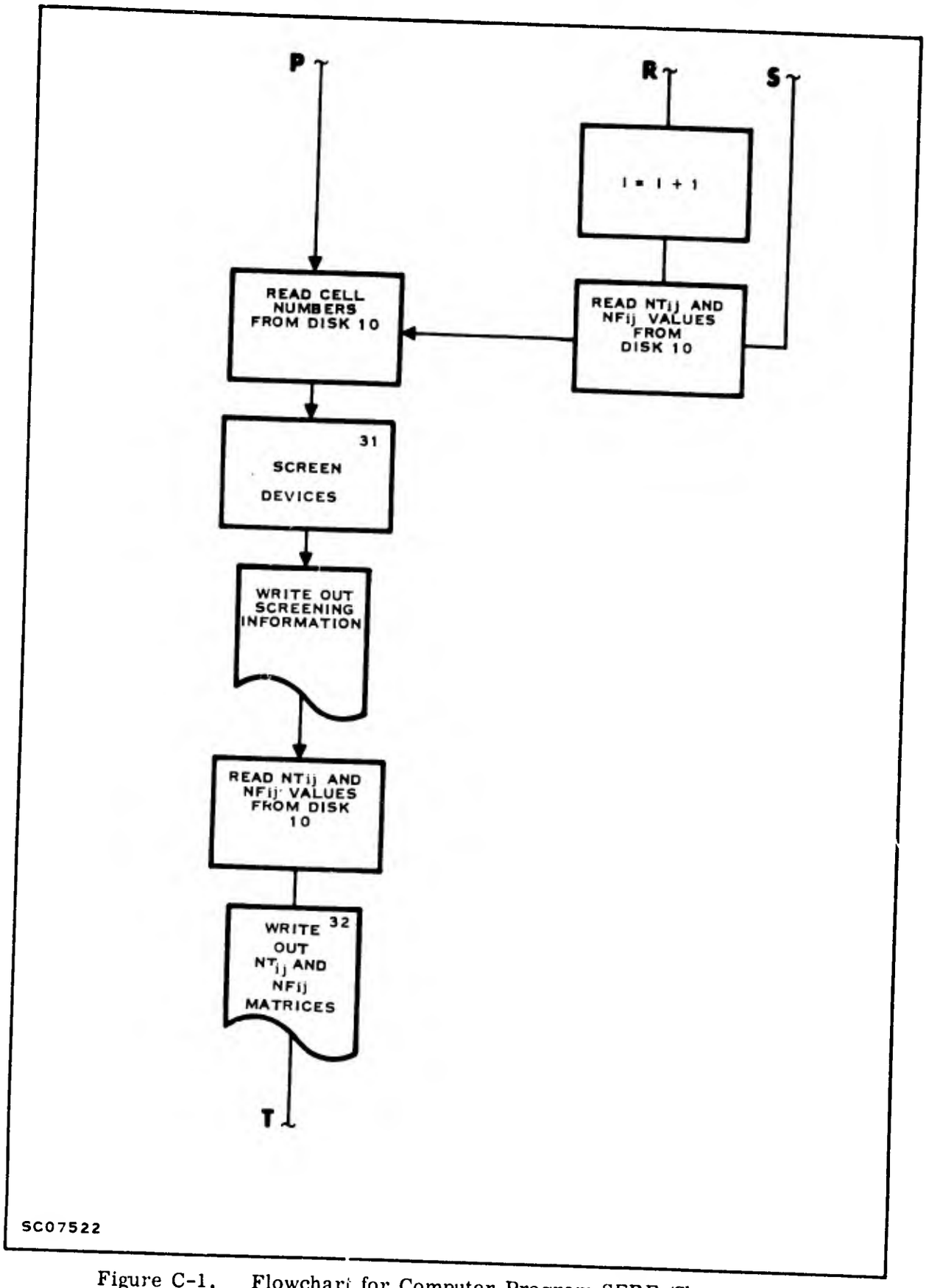


Figure C-1. Flowchart for Computer Program SERF (Sheet 8 of 9)

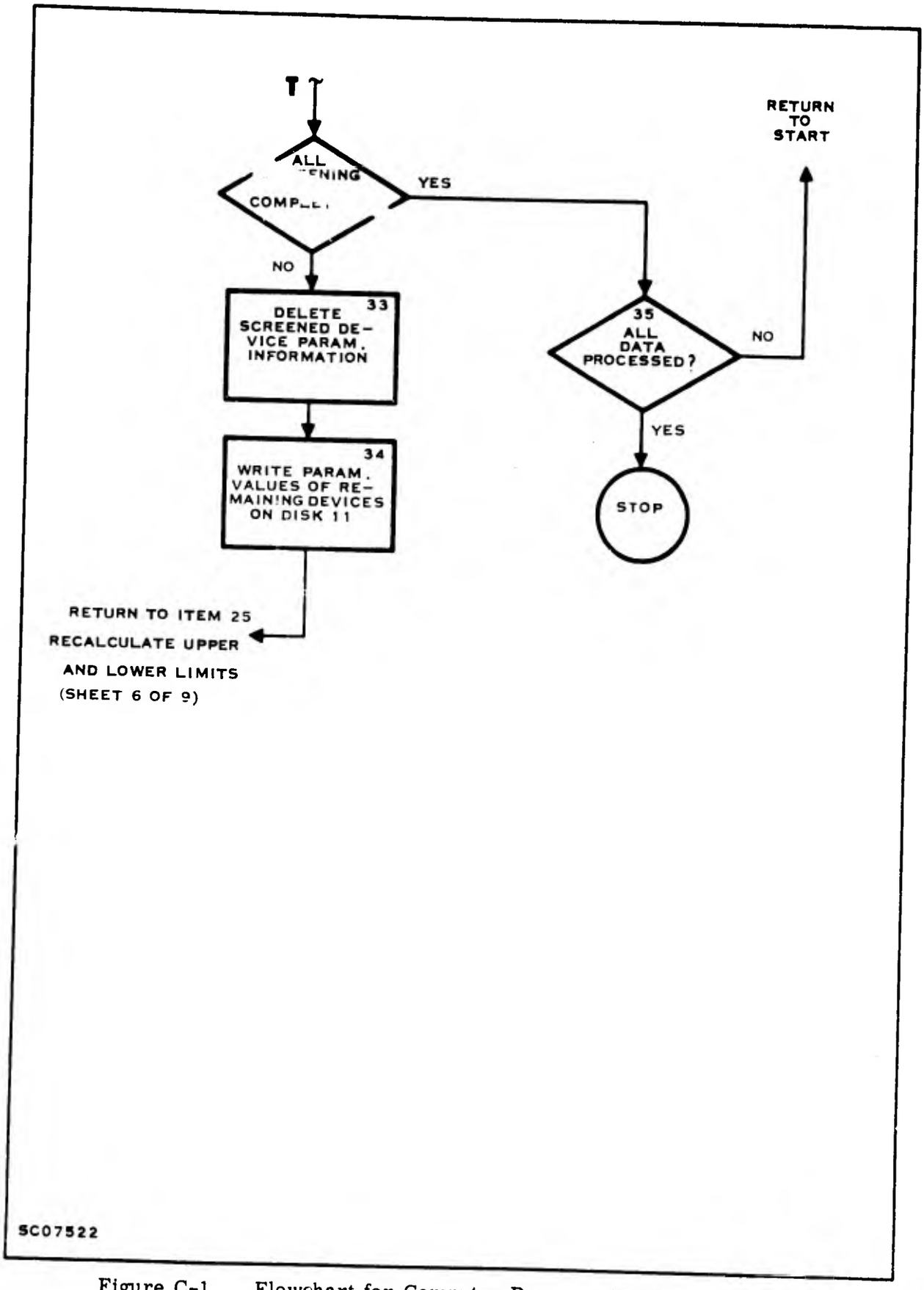


Figure C-1. Flowchart for Computer Program SERF (Sheet 9 of 9)

2. LINEAR DISCRIMINANT ANALYSIS (LINDA)

In this discussion it is assumed that several parameter measurements be used to predict whether or not a device will perform satisfactorily over a period of time. The problem can be expressed as one of classification[14] where there are two populations, satisfactory and unsatisfactory; it is desired to classify a given device into one of these on the basis of parameter measurements. The theory behind the classification procedure has been worked out for the case where the underlying populations are multivariate normal. The classification criterion turns out to be a linear combination of the elements of the vector of measurements on the device. This is a convenient criterion to employ, and it would be useful to know how the criterion behaves when the underlying populations are non-normal. The assumption is made consistently that the satisfactory and unsatisfactory populations share a common covariance matrix, although, in practice this assumption may be questioned. Another problem of interest is the determination of which variates constitute the best classifiers.

a. Theory

What follows is a summary of the theory given in Reference 14. Let π_1 and π_2 be the two populations into one of which we wish to classify an observation $\underset{\sim}{x}$ (mxl). Assume that π_1 is multivariate normal with mean $\underset{\sim}{\mu}^{(1)}$ (mxl) and covariance matrix $\underset{\sim}{\sum}$ (mxm), and that π_2 is multivariate normal with mean $\underset{\sim}{\mu}^{(2)}$ (mxl) and covariance matrix $\underset{\sim}{\sum}$(mxm). Let $p_i(\underset{\sim}{x})$, i = 1, 2, be the probability density functions associated with π_i, i = 1, 2, respectively. Let R = (R_1, R_2) denote a classification rule, i.e., if $\underset{\sim}{x}$ lies in region R_1, we classify $\underset{\sim}{x}$ into π_1, and if $\underset{\sim}{x}$ lies in R_2, we classify $\underset{\sim}{x}$ into π_2.

Let

$$P(2/1, R) = \int^{R_2} P_1(\underset{\sim}{x})\, d\underset{\sim}{x}$$

and

$$P(1/2, R) = \int^{R_1} P_2(\underset{\sim}{x})\, d\underset{\sim}{x}$$

where $dx = dx_1\, dx_2 \ldots\ldots dx_m$. Then P(2/1, R) is the probability of classifying $\underset{\sim}{x}$ into π_2 when $\underset{\sim}{x}$ is really from π_1, and P(1/2, R) is the probability of classifying $\underset{\sim}{x}$ into π_1 when $\underset{\sim}{x}$ is really from π_2. These are the P(i/j, R) probabilities of misclassification.

Let q_1 and q_2 be the probability that a random observation comes from π_1 and π_2 respectively. Further, let C(2/1) denote the cost of classifying $\underset{\sim}{x}$ into π_2 when $\underset{\sim}{x}$ is really from π_1, and let C(1/2) denote the cost of classifying $\underset{\sim}{x}$ into π_1 when $\underset{\sim}{x}$ is really from π_2. Then for a given classification rule, R = (R_1, R_2), the total expected cost of misclassifying the observation $\underset{\sim}{x}$ is

$$C(2/1)\, q_1\, P(1/2) + C(1/2)\, q_2\, P(2/1).$$

We seek a rule R such that the total expected cost of misclassification is minimized. We must take two cases into consideration: 1) the probabilities of a random observation coming from π_1 or π_2 are known, and 2) these probabilities are not known.

Case 1: Suppose q_1 and q_2 are known. The rule that minimizes the total expected cost of misclassification is

$$R_1 = \left\{ \underset{\sim}{x}: \frac{p_1(\underset{\sim}{x})}{p_2(\underset{\sim}{x})} \geq \frac{q_2\, C(1/2)}{q_1\, C(2/1)} \right\}$$

$$R_2 = \left\{ \underset{\sim}{x}: \frac{p_1(\underset{\sim}{x})}{p_2(\underset{\sim}{x})} < \frac{q_2\, C(1/2)}{q_1\, C(2/1)} \right\}.$$

Note that R can also be expressed as

$$R_1 = \left\{ \underset{\sim}{x}: \log \frac{p_1(\underset{\sim}{x})}{p_2(\underset{\sim}{x})} \geq \log k \right\}$$

$$R_2 = \left\{ \underset{\sim}{x}: \log \frac{p_1(\underset{\sim}{x})}{p_2(\underset{\sim}{x})} < \log k \right\},$$

where $k = q_2 C(1/2) / q_1 C(2/1)$. The classification procedure defined by R is called a Bayes procedure.

Case 2: If q_1 and q_2 are not known, one must look for the class of "admissible" classification procedures, i.e., the class of procedures which cannot be improved upon. It turns out that the class of admissible procedures is identical with the class of Bayes procedures. Hence in the search for a classification rule, one should restrict himself to the class of Bayes procedures. One such Bayes procedure is the minimax procedure. If R* is a classification rule, $r(1, R^*) = C(2/1)\, P(2/1, R^*)$ and $r(2, R^*) = C(1/2)\, P(1/2, R^*)$, then R* is minimax if $\max r(i, R^*)$ is a minimum with respect to all admissible R. The minimax procedure requires that $r(1, R^*) = r(2, R^*)$. Thus our rule is

$$R_1^* = \left\{ \underset{\sim}{x}: \log \frac{p_1(\underset{\sim}{x})}{p_2(\underset{\sim}{x})} \geq \log k \right\}$$

$$R_2^* = \left\{ \underset{\sim}{x}: \log \frac{p_1(\underset{\sim}{x})}{p_2(\underset{\sim}{x})} < \log k \right\},$$

where $\log k = c$ is determined so that $r(1, R^*) = r(2, R^*)$.

In any event we must examine the ratio $p_1(\underset{\sim}{x}) / p_2(\underset{\sim}{x})$. Now

$$p_i(\underset{\sim}{x}) = \frac{1}{(2\pi)^{m/2}\sqrt{|\underset{\sim}{\Sigma}|}} \exp\left[-1/2\,(\underset{\sim}{x} - \underset{\sim}{\mu}^{(i)})'\,\underset{\sim}{\Sigma}^{-1}(\underset{\sim}{x} - \underset{\sim}{\mu}^{(i)})\right], \quad i = 1, 2.$$

$$\text{Thus } \log \frac{p_1(\underset{\sim}{x})}{p_2(\underset{\sim}{x})} = \log \exp \; -1/2\left[(\underset{\sim}{x}-\underset{\sim}{\mu}^{(1)})'\,\underset{\sim}{\Sigma}^{-1}(\underset{\sim}{x} - \underset{\sim}{\mu}^{(1)}) - (\underset{\sim}{x} - \underset{\sim}{\mu}^{(2)})'\,\underset{\sim}{\Sigma}^{-1}(\underset{\sim}{x} - \underset{\sim}{\mu}^{(2)})\right]$$

$$= \underset{\sim}{x}'\,\underset{\sim}{\Sigma}^{-1}(\underset{\sim}{\mu}^{(1)} - \underset{\sim}{\mu}^{(2)}) - 1/2\,(\underset{\sim}{\mu}^{(1)} + \underset{\sim}{\mu}^{(2)})'\,\underset{\sim}{\Sigma}^{-1}\,(\underset{\sim}{\mu}^{(1)} - \underset{\sim}{\mu}^{(2)}) \; .$$

If $U = \underset{\sim}{X}'\,\underset{\sim}{\Sigma}^{-1}\,(\underset{\sim}{\mu}^{(1)} - \underset{\sim}{\mu}^{(2)}) - 1/2\,(\underset{\sim}{\mu}^{(1)} + \underset{\sim}{\mu}^{(2)})\,\underset{\sim}{\Sigma}^{-1}\,(\underset{\sim}{\mu}^{(1)} - \underset{\sim}{\mu}^{(2)})$, it is easy to show that U has a normal distribution with mean $1/2\,\alpha$ and variance α if $\underset{\sim}{x}$ is from π_1, and with mean $-1/2\,\alpha$ and variance α if $\underset{\sim}{x}$ is from π_2, where $\alpha = (\underset{\sim}{\mu}^{(1)} - \underset{\sim}{\mu}^{(2)})\,\underset{\sim}{\Sigma}^{-1}\,(\underset{\sim}{\mu}^{(1)} - \underset{\sim}{\mu}^{(2)})$. Thus probabilities of misclassification are easy to compute. We have

$$P(2/1) = \int_{-\infty}^{c} \frac{1}{\sqrt{2\pi\alpha}}\, e^{-1/2\frac{(u - 1/2\,\alpha)^2}{\alpha}}\, du$$

$$= \int_{-\infty}^{\frac{c-1/2\,\alpha}{\sqrt{\alpha}}} \frac{1}{\sqrt{2\pi}}\, e^{-1/2y^2}\, dy,$$

and

$$P(1/2) = \int_{c}^{\infty} \frac{1}{\sqrt{2\pi\alpha}}\, e^{-1/2\,\frac{(u + 1/2\,\alpha)^2}{\alpha}}\, du$$

$$= \int_{\frac{c + 1/2\,\alpha}{\sqrt{\alpha}}}^{\infty} \frac{1}{\sqrt{2\pi}}\, e^{-1/2\,y^2}\, dy.$$

If q_1 and q_2 are known, $c = \log k = \log q_2 C(1/2) / q_1 C(2/1)$. For the minimax solution we choose c so that

$$C(1/2) \int_{\frac{c + 1/2\,\alpha}{\sqrt{\alpha}}}^{\infty} \frac{1}{\sqrt{2\pi}} e^{-1/2y^2} dy = C(2/1) \int_{-\infty}^{\frac{c-1/2\alpha}{\sqrt{\alpha}}} \frac{1}{\sqrt{2\pi}} e^{-1/2\,y^2} dy.$$

Of course, in most cases $\underset{\sim}{\mu}^{(1)}$, $\underset{\sim}{\mu}^{(2)}$, and $\underset{\sim}{\Sigma}$ are not known. Hence they must be estimated before the above theory can be applied. Suppose we have a sample,

$$\underset{\sim}{x}_1^{(1)}, \ldots, \underset{\sim}{x}_{N_1}^{(1)},$$

from π_1 and a sample,

$$\underset{\sim}{x}_1^{(2)}, \ldots, \underset{\sim}{x}_{N_2}^{(2)},$$

from π_2. The estimates of $\underset{\sim}{\mu}^{(1)}$ and $\underset{\sim}{\mu}^{(2)}$ are $\overline{\underset{\sim}{x}}^{(1)}$

$$= \frac{1}{N_1} \sum_{i=1}^{N_1} \underset{\sim}{x}_i^{(1)} \quad \text{and} \quad \overline{\underset{\sim}{x}}^{(2)}$$

$$= \frac{1}{N_2} \sum_{i=1}^{N_2} \underset{\sim}{x}_i^{(2)}.$$

An estimate of $\underset{\sim}{\Sigma}$, say $\underset{\sim}{S}$, may be defined by

$$(N_1 + N_2 - 2)\,\underset{\sim}{S} = \sum_{i=1}^{N_1} (\underset{\sim}{x}_i^{(1)} - \overline{\underset{\sim}{x}}^{(1)})\,(\underset{\sim}{x}_i^{(1)} - \overline{\underset{\sim}{x}}^{(1)})'$$

$$+ \sum_{i=1}^{N_2} (\underset{\sim}{x}_i^{(2)} - \overline{\underset{\sim}{x}}^{(2)})\,(\underset{\sim}{x}_i^{(2)} - \overline{\underset{\sim}{x}}^{(2)})' .$$

Then we use

$$V = \underset{\sim}{x}' \; \underset{\sim}{S}^{-1} \left(\bar{\underset{\sim}{x}}^{(1)} - \bar{\underset{\sim}{x}}^{(2)} \right) - 1/2 \left(\bar{\underset{\sim}{x}}^{(1)} + \bar{\underset{\sim}{x}}^{(2)} \right)' \; \underset{\sim}{S}^{-1} \left(\bar{\underset{\sim}{x}}^{(1)} - \bar{\underset{\sim}{x}}^{(2)} \right)$$

as our classification statistic. It can be shown that the limiting distribution of V is the distribution of U. (Investigations of the distribution of V can be found in References 15 and 16. We shall use the asymptotic results only.)

b. Computer Programs

Two computer programs based on linear discriminant analysis have been written. One computer program, LINDA 1, is applicable when the covariance matrices of the populations of good devices and of bad devices are equal. Two different procedures are used in this computer program, depending on whether the user's problem falls under Case 1 or Case 2 as defined in the previous discussions.

The second computer program, LINDA 2, is applicable whether or not the covariance matrices are equal. This program is based on the theoretical work of Anderson and Bahadur [17] and the outline of the computer programs written by Welch and Wimpress [18]. Basically, LINDA 2 calculates the vector $\underset{\sim}{b}$ from the equation

$$\underset{\sim}{b} = \left[y \underset{\sim}{\Sigma}_1 + (1 - y) \underset{\sim}{\Sigma}_2 \right]^{-1} \left(\underset{\sim}{\mu}^{(2)} - \underset{\sim}{\mu}^{(1)} \right)$$

where

$$\underset{\sim}{\Sigma}_1, \; \underset{\sim}{\mu}^{(1)} \text{ and } \underset{\sim}{\Sigma}_2, \; \underset{\sim}{\mu}^{(2)}$$

are the covariance matrices and mean vectors for populations 1 and 2, respectively, and y ($0 \leq y \leq 1$) is the solution of the equation

$$\left\{ \left[y \underset{\sim}{\Sigma}_1 + (1 - y) \underset{\sim}{\Sigma}_2 \right]^{-1} \left(\underset{\sim}{\mu}^{(2)} - \underset{\sim}{\mu}^{(1)} \right) \right\}' \left\{ y^2 \underset{\sim}{\Sigma}_1 - (1 - y) \underset{\sim}{\Sigma}_2 \right\} \left\{ \left[y \underset{\sim}{\Sigma}_1 + (1 - y) \underset{\sim}{\Sigma}_2 \right]^{-1} \left(\underset{\sim}{\mu}^{(2)} - \underset{\sim}{\mu}^{(1)} \right) \right\} = 0$$

If

$$\underset{\sim}{X} = \begin{pmatrix} X_1 \\ X_2 \\ \vdots \\ X_n \end{pmatrix}$$

is the vector of parameter measurements, then if

$$\underset{\sim}{b}' \underset{\sim}{X} + p \geq 0, \quad \underset{\sim}{X} \text{ belongs to population 1}$$

$$\underset{\sim}{b}' \underset{\sim}{X} + p < 0, \quad \underset{\sim}{X} \text{ belongs to population 2.}$$

where b' is the transpose of the vector b. The scalar p is calculated from the equation

$$p = - \frac{\left(\underset{\sim}{b}' \sum_{\sim 2} \underset{\sim}{b}\right)^{1/2} \underset{\sim}{b}' \underset{\sim}{\mu}^{(1)} + \left(\underset{\sim}{b}' \sum_{\sim 1} \underset{\sim}{b}\right)^{1/2} \underset{\sim}{b}' \underset{\sim}{\mu}^{(2)}}{\left(\underset{\sim}{b}' \sum_{\sim 1} \underset{\sim}{b}\right)^{1/2} + \left(\underset{\sim}{b}' \sum_{\sim 2} \underset{\sim}{b}\right)^{1/2}}$$

APPENDIX D

FAILURE ANALYSIS

1. INTRODUCTION

Failure analysis has played an increasingly significant role in this contract toward developing reliability screening procedures for integrated circuits. At the beginning of the program, analysis of failures was performed on a sampling basis, since major emphasis was placed on SERF and LINDA computer programs to predict failure on the basis of device electrical parameters. As the program progressed it became obvious that the mathematical approach should be supplemented with a complete failure analysis program since many stress failures could not be predicted from analysis of electrical parameters prior to failure. The results of all failures analyzed on the program, including all failures which occurred from the Fixed and Step Stress Series, are presented in this Appendix.

2. SUMMARY OF RESULTS

Failure analysis results are shown in Table D-1. Each of the categories are included in the detailed discussions. Results show that the major failure modes of each replicate were different primarily due to process variations. However, all of these modes have been previously encountered on many other classes of monolithic circuits.

a. Photolithographic Faults

Photolithographic faults are caused by improper oxide removal and/or metal etching. Table D-2 lists a brief procedural outline of the photolithographic process utilized in semiconductor manufacture and indicates possible faulty areas.

Three failures from the Preliminary Investigation were found to exhibit degraded junction characteristics (diode action still present) which could not be reversed by baking on removal of expanded contact metallization. It is suspected that degradation of this type is caused by a mask or photoresist defect as shown in Figure D-1 which leaves a small portion of the base region exposed beneath the emitter lead.

Table D-1. Summary of Failures

	Preliminary Investigation (n = 270)	Step Stress Replicate 1 (n = 365)	Fixed and Step Stress* (n = 650)	Stress Causing Failure	Stress Interval or Level to Produce All Failures
1. Photolithographic Fault	3	0	0	300°C Storage	500 Hours
2. Surface Contamination	0	0	1 (1)	Electrical -200°C	275 Hours
3. Oxide Defect	2	1	3 (2)	Electrical 160°C - 200°C	500 Hours
4. Die Delamination	10	0	0	Constant Acceleration	75,000 G
5. Ball Bond Separation	0	2	3 (3)	Constant Acceleration	75,000 G
6. Die and Wire Dress	0	5	24	Constant Acceleration	75,000 G
7. Metallization Scratches	1	0	0	300°C Storage	500 Hours
8. Peeling Metalization	0	1	9	Electrical-storage 160°C-375°C	2,000 Hours
9. Die Cracks	0	0	11 (8)	Electrical 160°C-200°C	2,000 Hours
10. Resistor Degradation	0	0	6	Electrical-storage 375°C-460°C	2,000 Hours
11. Unknown	0	0	13	Electrical 160°C-200°C	2,000 Hours
12. Overstress	0	0	5	Electrical 160°C-200°C	2,000 Hours

*A precapsulation photographic analysis was performed on devices in the Fixed and Step Stress Series. The quantity of devices with visible precapsulation defects causing failure are shown in parenthesis.

Table D-2. Photolithographic Techniques and Related Faults

Step	Technique	Faults
1	Photoresist, a light sensitive material, is spread evenly over the surface of a semiconductor slice.	Variation in thickness of photoresist may produce thin spots which will not mask etchants used later in the process on thick spots which produce image spreading.
2	A photolithographic mask is placed over the slice.	Incorrect positioning of the mask, commonly referred to as misalignment, may cause any number of faults. A few typical examples are metallization removed from all or a portion of a contact window, an emitter diffusion spreading across a base diffusion, or a contact window being opened away from the diffusion to which contact was to be made.
3	The photoresist that is not covered by an opaque portion of the mask is exposed to ultraviolet light.	Transparent regions in the opaque area of the mask produce exposed areas. These areas later prevent etchants from removing oxide on excess material. This may produce lack of ohmic contact, metallization shorts, etc. Opaque regions in the regions of the mask which are supposed to be transparent produce unexposed areas. These areas allow etchants to attack oxide on metallization at incorrect locations. They may produce pinholes in the oxide or voids in the metallization.
4	The unexposed photoresist is removed by washing.	If unexposed photoresist is not removed by washing, it produces effects identical to those produced by opaque areas in the photomask.
5	The oxide or metal is removed by etching.	If the photoresist does not adhere to the surface properly, etch may undercut the material being etched.
6	The exposed photoresist is removed by washing.	If the photoresist is not removed, it may block contact formation, block diffusions, or serve as a trap for etchants which subsequently attack metallization on oxide.

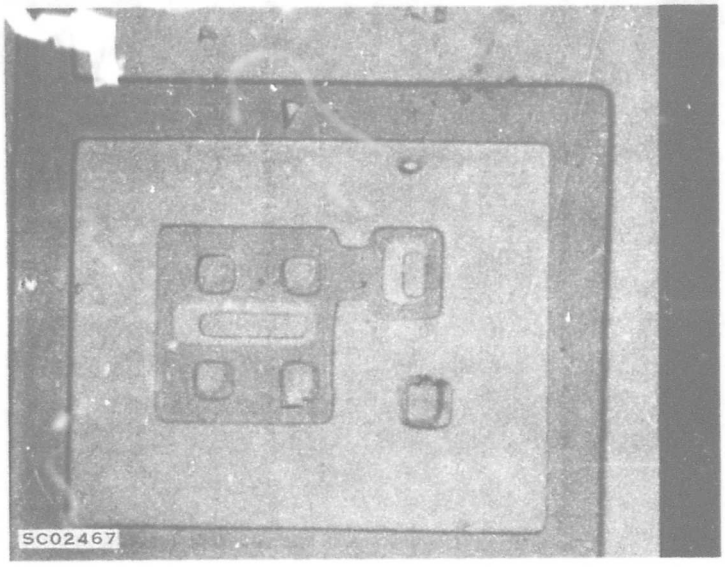
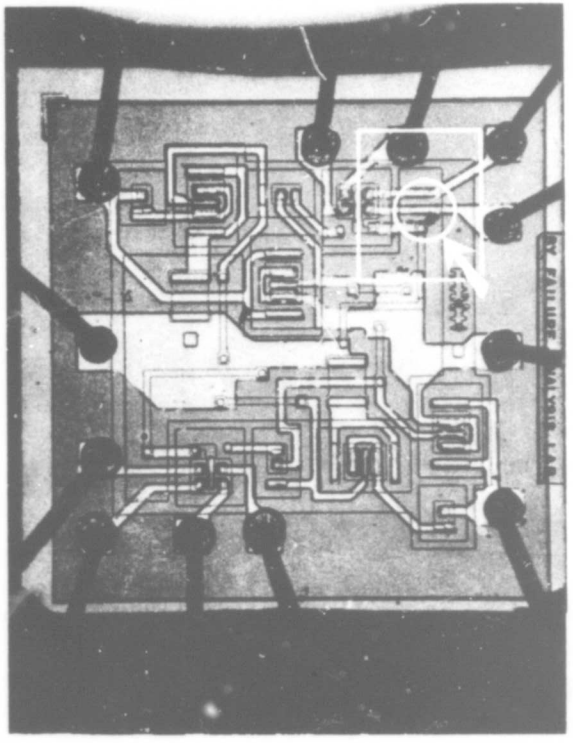


Figure D-1. Masking Misalignment or Defect

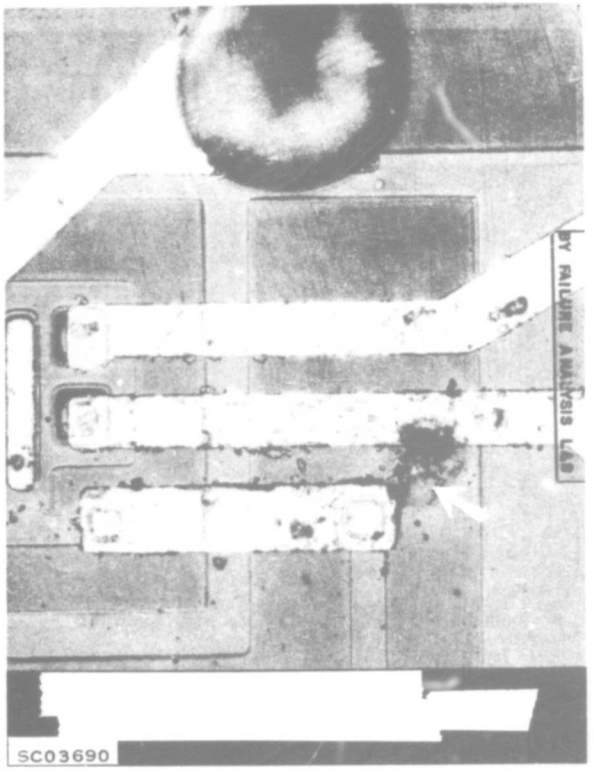
b. Surface Contamination (Restricted to Visible Contamination)

Surface contamination may result from incomplete cleaning or from ambient particles in any stage of slice preparation or packaging. Some of the particularly troublesome areas are residual photoresist trapping etchants, "back streaming" of vacuum pump oil, flaking of gold plating, weld splatter, gold "overhang" from badly undercut molybdenum in the gold-molybdenum metallization system, and dust particles containing active etchants.

During this program, only one failure resulting from surface contamination was encountered. This was from the Ring Counter Step Stress at 200° C, after 275 hours. Microscopic examination of the failed device revealed a conductive lead. Removal of the material caused the circuit to function properly. The material was visible in the pre-cap photograph. Unfortunately, in removing it from its location on the integrated circuit it was lost, hence no further analysis was possible. Its appearance suggested that it was most probably residual photoresist containing etchants which reacted with the molybdenum thereby producing the short circuit. Refer to Figures D-2a and D-2b for illustrations of these effects.



(A) PRECAPSULATION PHOTO REVEALS PRESENCE OF MATERIAL CONNECTING METAL LEAD PATTERNS



(B) REMOVAL OF MATERIAL AFTER STRESS CAUSED THE CIRCUIT TO FUNCTION PROPERLY

Figure D-2. Example of Surface Contamination

c. Oxide Defects

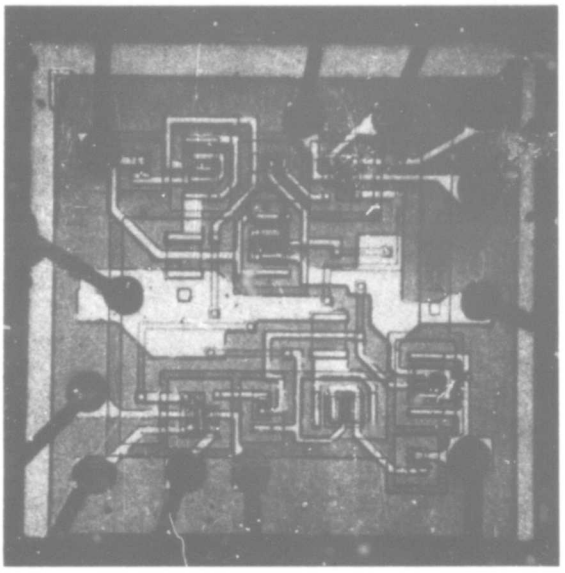
Oxide defects may be subdivided into pinholes, spurious diffusion sites, and oxide scratches. A total of six failures resulting from oxide defects were encountered during the program; namely, four pinholes, one spurious diffusion site and one oxide scratch.

Spurious diffusion sites are isolated diffused regions associated with oxide pinholes that were formed early enough in the manufacturing procedure to serve as entry ports for subsequent diffusions, in particular the N^+ diffusion used to form emitters of NPN transistors. A photograph of a spurious diffusion site is given in Figure D-3. Spurious diffusion at this site lowered the breakdown (below operating voltages) of the associated transistor's collector at the substrate junction, and resulted in device failure. Figure D-3.b is a micrograph of the diffusion site after device failure. Note the rings about the site. This results from a direct lighting effect and indicates the oxide is thin about the site. A localized hot spot was produced at the site when the circuit conditions exceeded the low breakdown voltage. The hot spot produced high reverse leakage and further degradation of the junction. The basic causes for spurious diffusion sites are synonymous with those for pinholes which are discussed below.

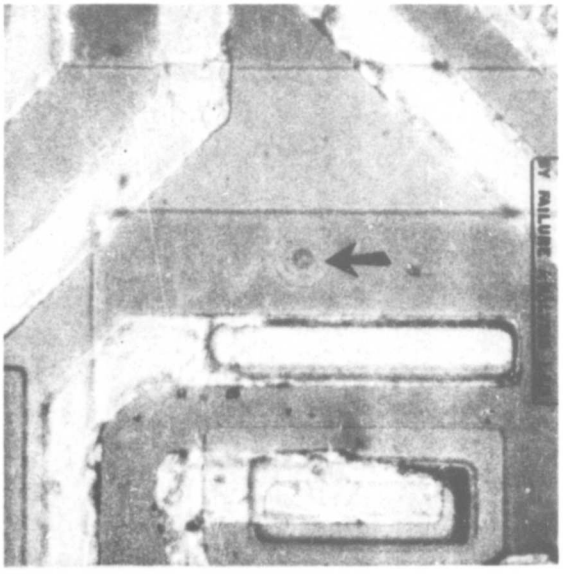
Oxide scratches that are reliability problems are those which reduce oxide thickness to the level where subsequent diffusions are not masked and/or metallization-to-silicon isolation is not maintainable. Hence, oxide scratches, which usually result from misapplication of tweezers, differ from pinholes only in physical dimensions. An example of an oxide scratch is shown in Figure D-4. The scratch lowered the oxide thickness and the voltage applied during device operation punched through the oxide.

A pinhole is a discontinuity or an isolated region with a low dielectric breakdown in the oxide. Those located beneath a metallization pattern allow metal to contact the underlying silicon. A photomicrograph of an integrated circuit that failed as a result of a pinhole is presented in Figure D-5. The metallization has been removed by the Failure Analysis Laboratory. The dashed line approximates the location of a metallized area which was shorted to the silicon through the pinhole indicated by the arrow.

Oxide pinholes are caused by factors which locally prevent oxidation, such as inadequate photoresist masking, lack of photoresist adhesion, photomask faults preventing exposure of the photoresist, fast-etching sites produced by conglomeration of P_2O_5 molecules during diffusion, and surface contamination.



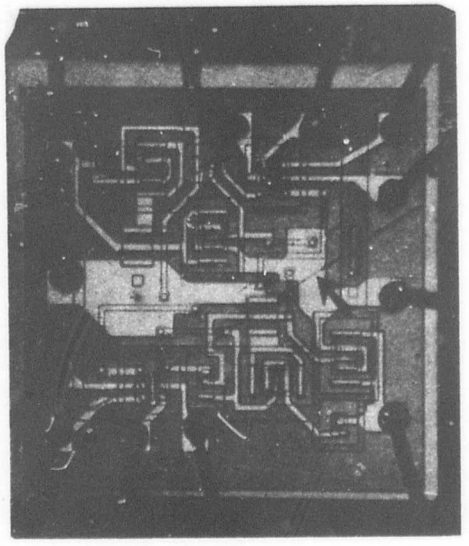
(A) PRE-CAP PHOTOGRAPH REVEALING SPURIOUS DIFFUSION SITE (NOTE CIRCLED AREA)



(B) POST TEST PHOTOGRAPH OF SPURIOUS DIFFUSION SITE (NOTE INTERFERENCE LINES ABOUT SITE)

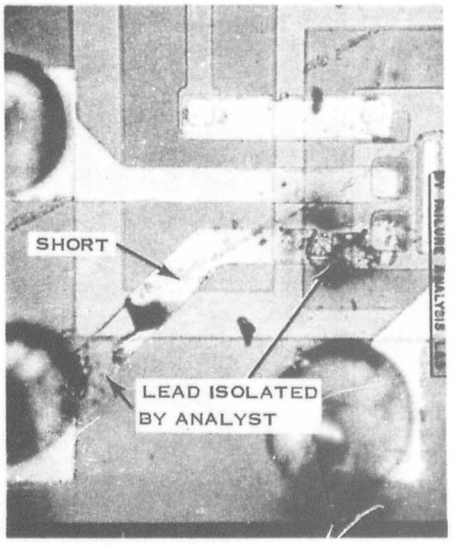
SC05684

Figure D-3. Photographs of a Spurious Diffusion Site Which Resulted in Device Failure



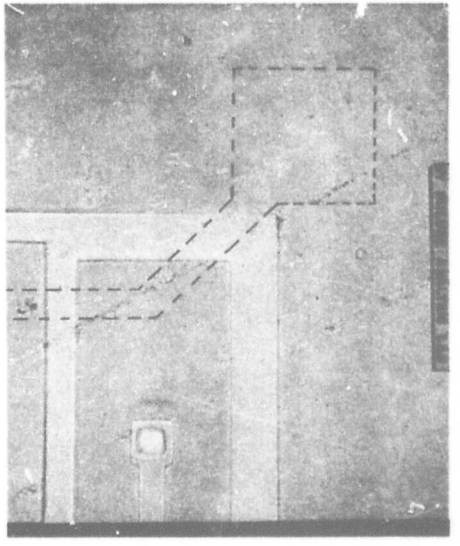
(A)

PRE-CAP PHOTOGRAPH REVEALING PARALLEL TWEEZER MARKS



(B)

EVAPORATED LEAD ISOLATED TO DETERMINE LEAD SHORT TO SUBSTRATE AND RESISTOR ISOLATION PRODUCED BY TWEEZER MARKS



(C)

POST LEAD REMOVAL. DOTTED AREA IS PIN 7 EVAPORATED LEAD'S FORMER LOCATION

SC06260

Figure D-4. Example of an Oxide Scratch

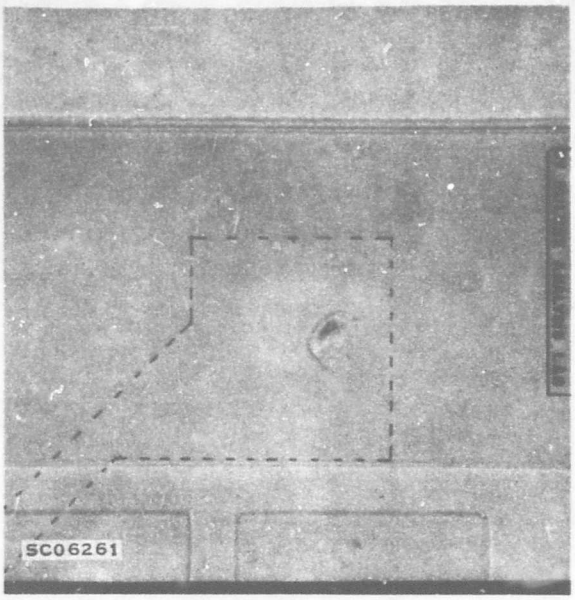


Figure D-5. Oxide Fault (Pinhole) Under Bond Pad

d. Die Delamination

In the period of transition to a new header design, devices used in the preliminary investigation were manufactured with the following die-to-case contact configuration: silicon-glass frit-gold plate-nickel plate-Kovar. The glass frit to gold plate interface did not form a chemical bond, hence failure to adhere occurred during subsequent stresses. This was corrected by removing the gold plate and nickel plate in the area of the die bond to the package. Refer to Figure D-6 for an example of a die delamination failure. This mechanism existed only in devices used in the Preliminary Investigation.

e. Ball Bond Separation

Five ball bonds separated during the Step Stress Series and the Fixed and Step Stress Series of the test program. No bond failures were observed on the Preliminary Investigation.

Three of the bonds failed after surviving 15,000 G's constant acceleration. Two bonds failed due to inadequate pressure or temperature in the bonding operation. Refer to Figures D-7a and b for illustrations of these failures.

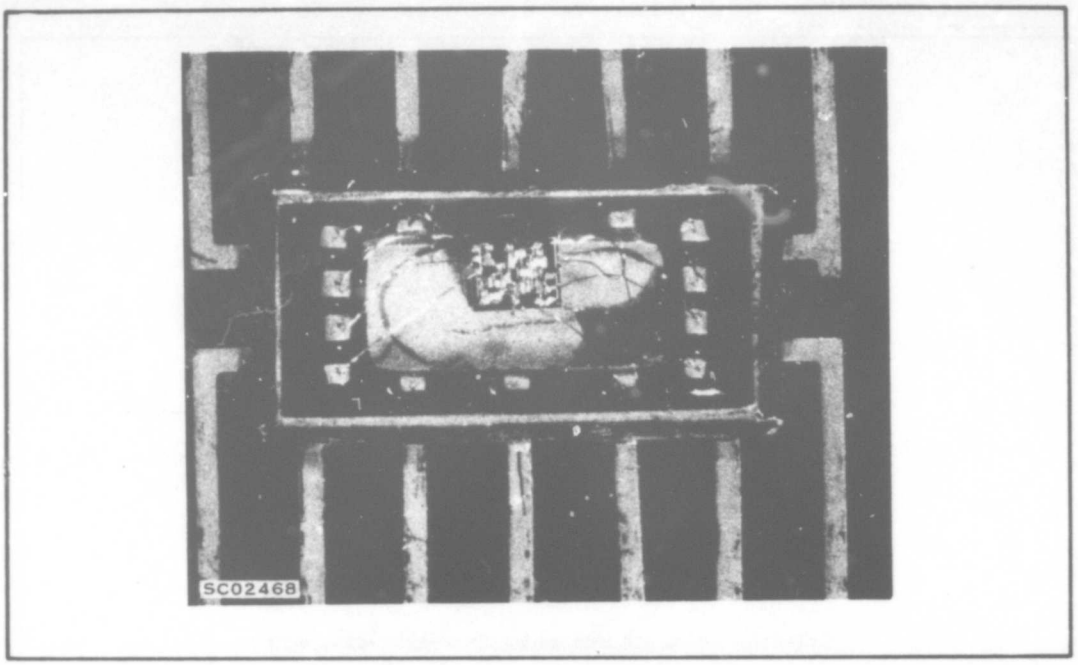
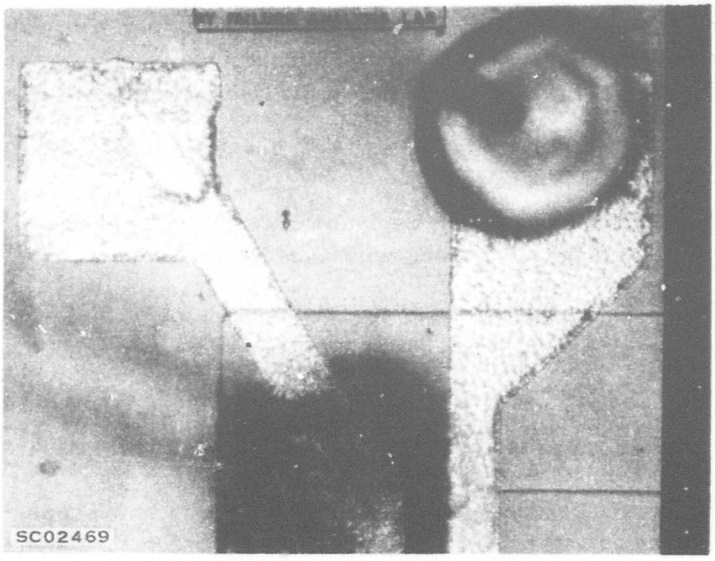


Figure D-6. Die Delamination at Glass Frit-gold Plate Interface

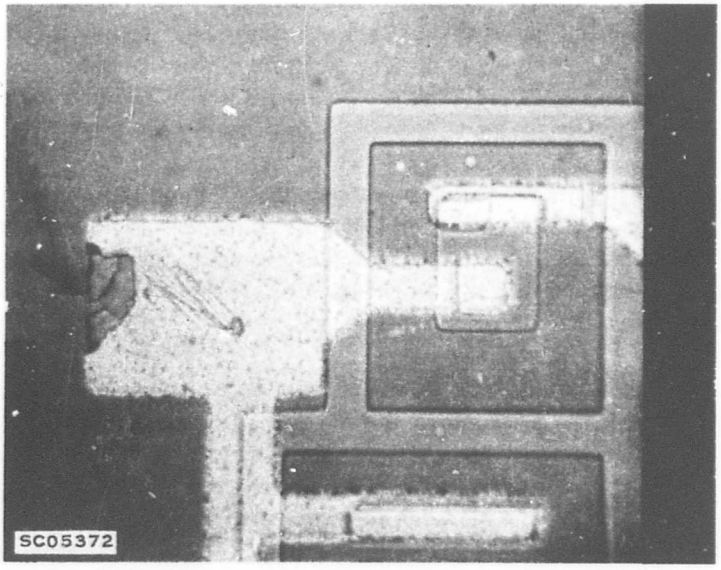
In addition, it has been determined that relative strengths of the various contact metal interfaces may be ranked in order of decreasing strength as follows:

- $Si-SiO_2$
- SiO_2-Mo
- Au-Au
- Mo-Au

This is the expected result, as all interfaces excepting moly-gold are chemically bonded. The Mo-Au interface is further weakened by Au overhang when the Mo is over etched and/or when the Mo was allowed to become oxidized prior to Au evaporation.



(A) BOND FAILURE CAUSED BY INADEQUATE TEMPERATURE OR PRESSURE



(B) NONCENTERED BALL BOND SEPARATED FROM BONDING PAD DURING 75,000 G'S AFTER WITHSTANDING 60,000 G'S.

Figure D-7. Examples of Ball Bond Failure

No relation was found to exist between die tilt and bond strength. The histograms shown in Figure D-8 clearly display this fact. They represent samples with a minimum of 50 microns from the horizontal plane (maximum tilt) and a maximum of 15 microns (minimum tilt). A Kolmogarov-Smirnov[9] two sample test was performed and indicated no differences in the two samples at the five percent level of significance.

f. Die and Wire Dress

Three factors have been found which affect the incidence of wafer and wire stress failures during high-stress mechanical tests:

- Excessive slack in bond wires.
- Stitch-bonds which connect the internal wire to external lead are either non-centered, or formed with excessive pressure.
- Dies that are not properly oriented in the package.

A study was conducted to determine techniques which could be used to preindicate failures due to wafer and wire dress. The approach consisted of analyzing top view X-ray photographs of devices taken before and after constant acceleration stress.

Pre-stress X-rays revealed the presence of slack wires; however many of the wires which caused failure in the devices did not appear to be slack in the pictures. Slack wires with high vertical arcs not seen initially, "folded" over when subjected to constant acceleration in the X and Z planes. Many of these shorted to other wires causing failure as shown in Figure D-9.

Dies that are improperly oriented in the package, can cause a high incidence of wire to wire shorts even though wires are well dressed. Figure D-9 is also an excellent example of this. Note that the wafer was mounted in the package with the edges parallel to the sides of the package. Such orientation tends to minimize the spacings between the bond wires at the corners of the bar.

Stitch-bonds are adversely affected by lack of taut wire dress. Wire movement during stress results in fatigue of the wire at the stitch bond and may result in fracture. This situation was observed to worsen when the stitch bond was applied with excessive pressure or was formed to near the edge of the terminal. Figure D-10 illustrates these problems. Two methods for detecting die and wire dress problems were studied.

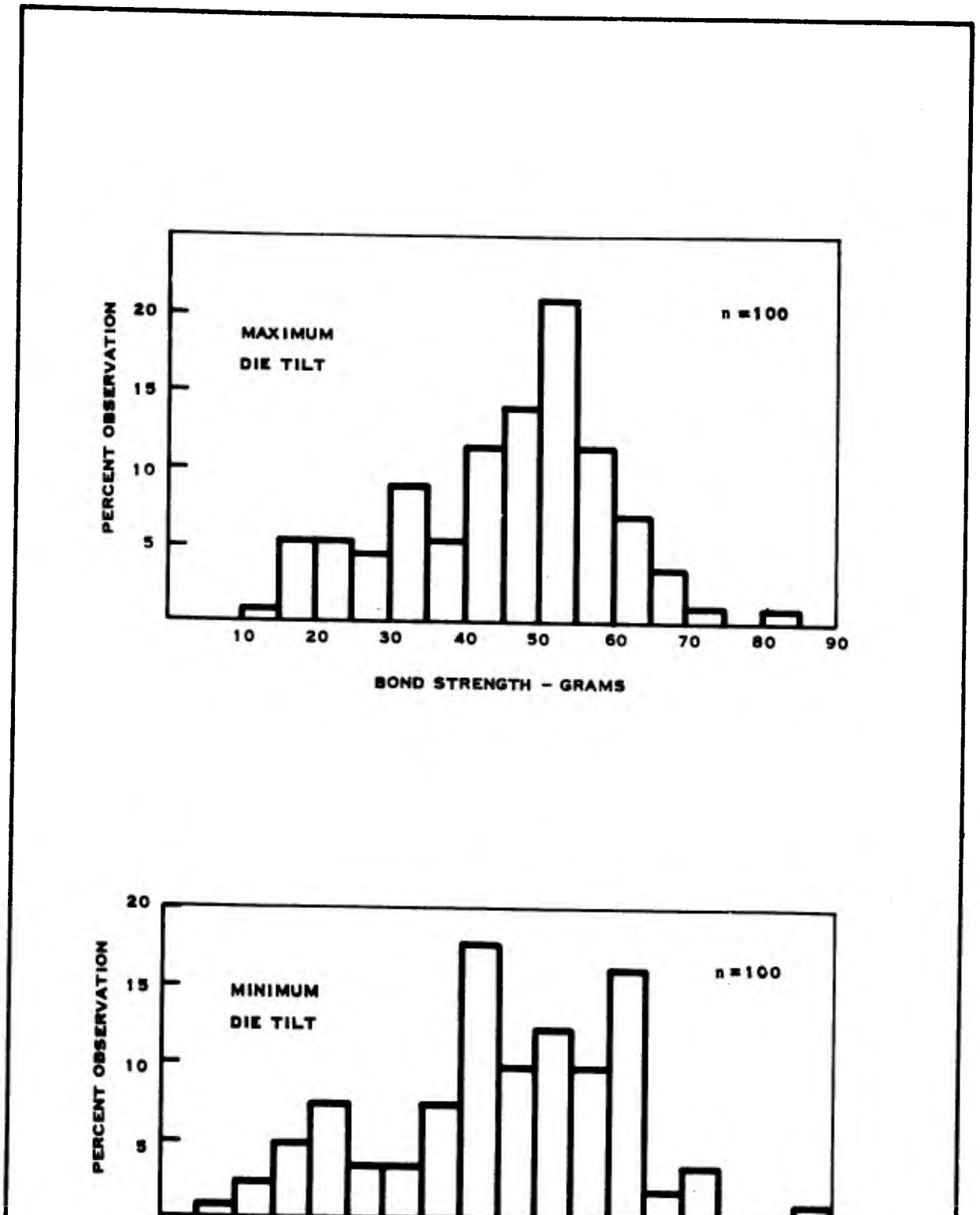
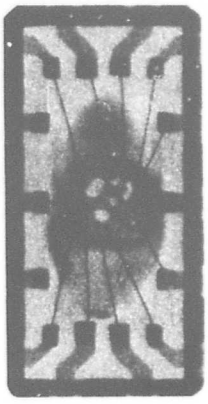
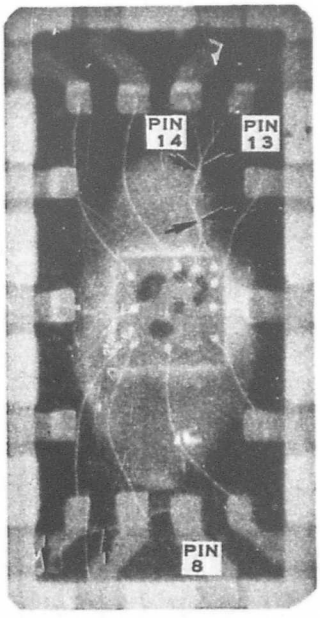


Figure D-8. Samples Taken from Manufacturing Lot Representing Fixed and Step Stress Test Series



TOP VIEW X-RAY OF
UNIT PRIOR TO STRESS
(NOTE ONLY TWO WIRES
APPEAR SLACK.)



SAME UNIT FOLLOWING
STRESS (NOTE ALL
WIRES APPEAR SLACK)

SC05969

Figure D-9. X-ray Before and After Constant Acceleration Stress

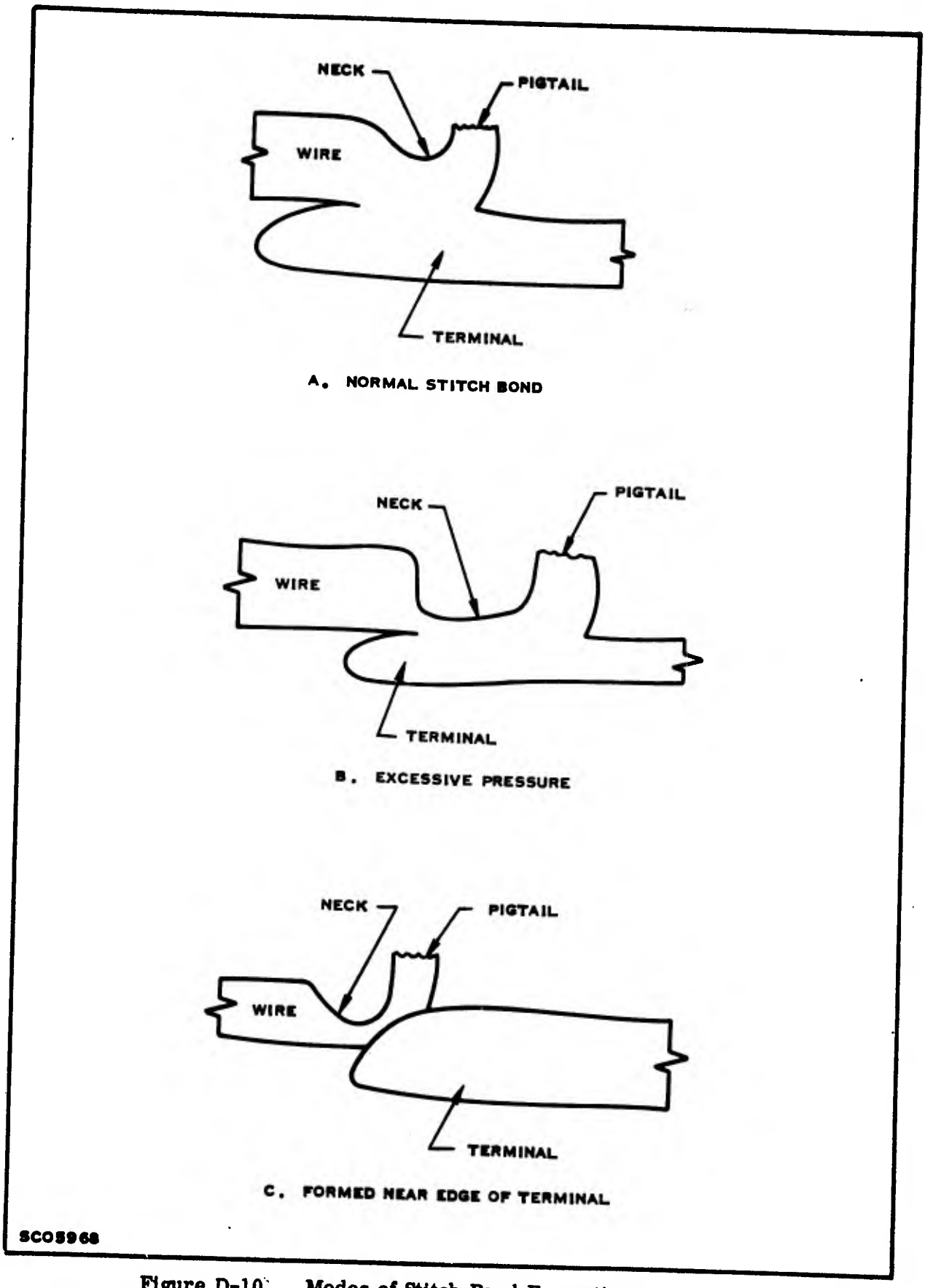


Figure D-10. Modes of Stitch Bond Formation

- A 20 X microscope package inspection prior to capsulation was evaluated. Refer to Figure D-11 where the single view clearly indicates that all stitch bonds are well centered and the die is properly oriented. However, the technique is limited because of wires with high arcs, which cannot be seen from this view.

- A constant acceleration test in the XZ planes followed by a top-view X-ray was conducted. Refer to Figure D-12. This figure demonstrated how constant acceleration performed in the X and Z plane, followed by X-ray, causes wires to fold over. Those with excessive slack can be detected by a top view X-ray as shown in Figure D-12B.

On the basis of this analysis, a suggested screening procedure is constant acceleration, 20000 Gs, X-Z planes only, followed by view X-rays to screen for slack wires and stitch bond placement. This screen is also effective for screening potential ball bond failures.

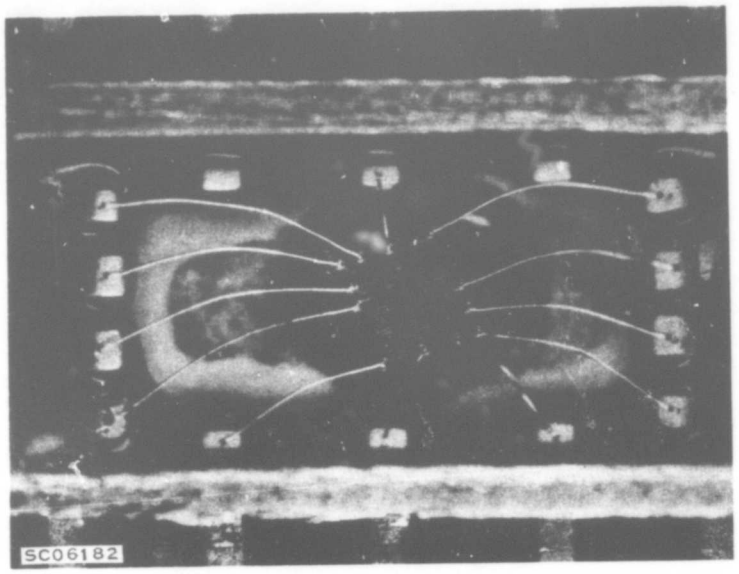


Figure D-11. 20X Picture of Unencapsulated SN5420 Integrated Circuit

The basic problem associated with wire dress is that of the package design, where relatively long wires are needed to connect the die bonding pads to external package pins. Small dies, such as the SN5420, are particularly vulnerable to wire dress problems because of relatively longer bond wire lengths. As a solution to this problem a new packaging concept has evolved by the design of a "cavity package," shown in Figure D-13. External pin connections are moved closer to the die to reduce the bond wire lengths, thereby reducing the probability of failure due to slack wires. Use of this package will eliminate the necessity of screening for slack wires. By changing the size of the cavity for different die dimensions, wire lengths can be minimized for dies of all dimensions.

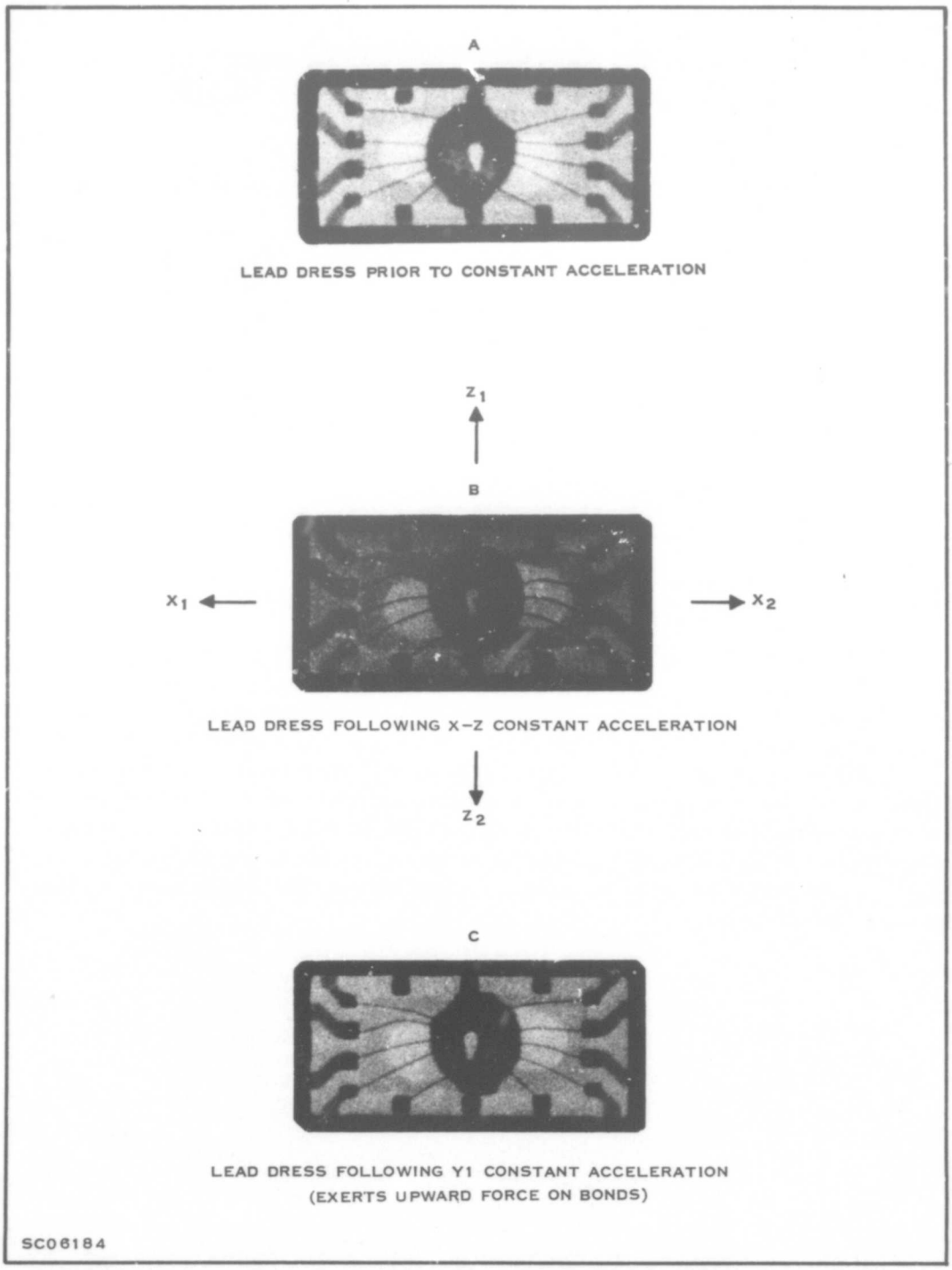


Figure D-12. Lead Dress Before and After Constant Acceleration Stress
(Note that die is properly oriented in package.)

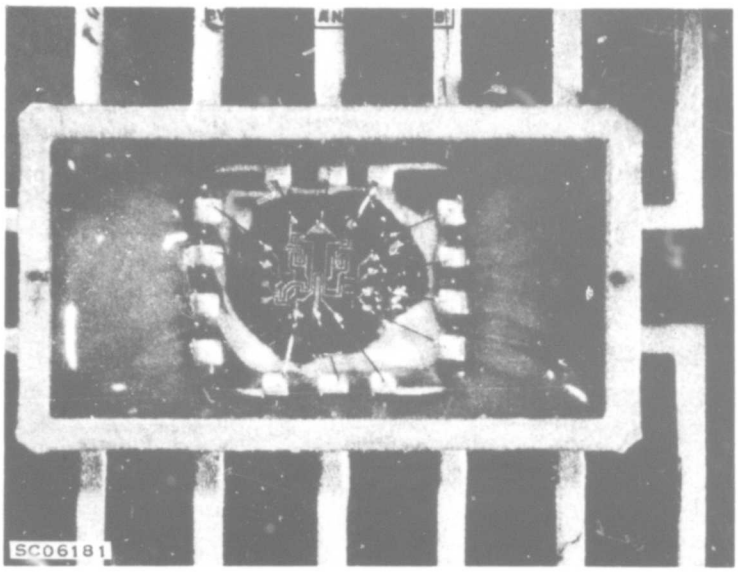


Figure D-13. 30X Picture of New "Cavity" Package
(Note the Relatively Shorter Bond Wire Lengths)

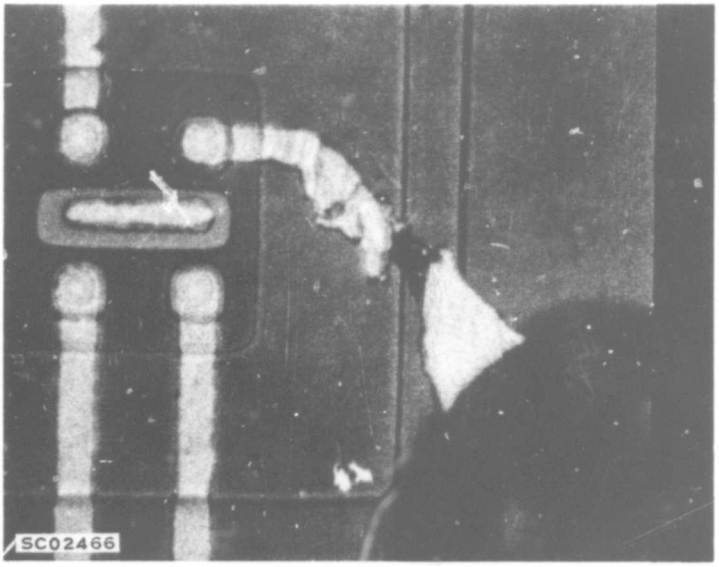


Figure D-14. Failure of Scratched Lead
(Note the Scratch Occurred at Oxide Step)

g. Metal Scratches

Scratches on the molybdenum-gold evaporated metalization do not normally present a reliability problem. However, prolonged exposure to elevated temperatures such as 300°C may weaken scratched leads to the failure point. The suspected failure mechanism is oxidation of the exposed Mo substrate resulting in a high resistance area in the pattern. Power dissipation in the region during electrical testing then causes destruction of the lead. Only one failure due to scratched metallization occurred during the test program and is shown in Figure D-14. To illustrate the ability of severely scratched leads to survive stress, refer to Figure 21 of Section V. This device survived 375°C for 1000 hours.

h. Peeling Metallization

Ten peeling metallization failures occurred during the main test program. Evidence of this failure mode was found from both electrical and storage stresses, with equal probability of occurrence at all stress intervals. An example of a peeling metal failure is shown in Figure D-15. This failure mechanism is caused by:

- Undercutting of the molybdenum layer
- Lack of adhesion between the moybdenum layer and the gold layer

Undercutting of the molybdenum layer is caused by reaction of molybdenum with etching solutions. It is difficult to control the removal of excess molybdenum to the degree required to prevent undercutting. Lack of adhesion between molybdenum and gold results when molybdenum is allowed to oxidize prior to evaporation of gold.

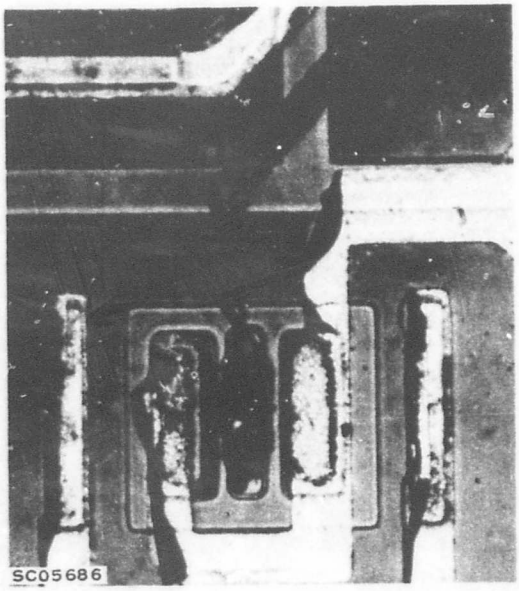


Figure D-15. Unit #171 (300°C Storage — 108 Hours) Peeling Gold Evaporated Lead Resulting in Open Base of Pin 10 Output Transistor

j. Cracked Dies

Cracked dies may be classified in the following manner:

- Cracks radiating from bonding areas

A photomicrograph of this type of crack is shown in Figures D-16.a and D-16.b. These cracks may result from stress induced during the bonding operation. They are often concealed beneath a ball bond on a bonding pad in their early stage. Figure D-16.c demonstrates the lack of correlation between this type failure and voiding.

- Cracks through active areas of die

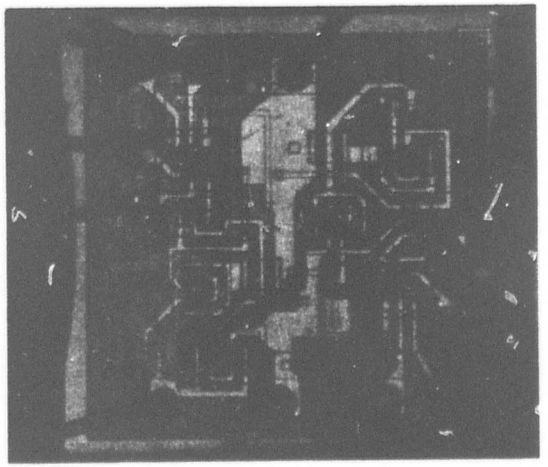
These result from the propagation of scribe line cracks or are produced directly by thermal mismatch between die and package material. They may be caused also by mechanical handling of the device during or after packaging. Refer to Figure D-17 for an example of a crack crossing active regions. This crack was not visible in the pre-cap photograph shown as Figure D-17.a. Figure D-17.c indicates that the crack correlates with an "L-shaped" void extending from the edge of the die.

- Cracks around periphery of die

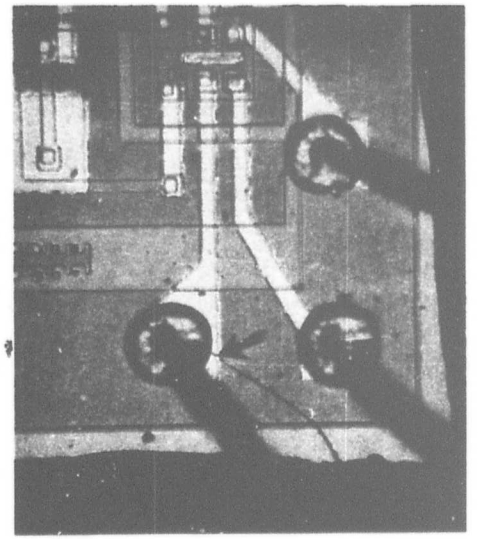
The terminology, cracks around periphery of die, is used to refer to those radiating from the scribe area of the die toward the interior surface area but not crossing any active junction. These cracks are probably caused by stress induced in the silicon during scribing and breaking, coupled perhaps with bulk crystalline defects. Refer to Figure D-18 for an illustration.

Photographic analysis of 900 devices used in the fixed and step stress tests reported in Appendix A revealed that 53% of the dies possessed cracks radiating from the scribe area. These cracks were categorized in the following manner according to their frequency of occurrence.

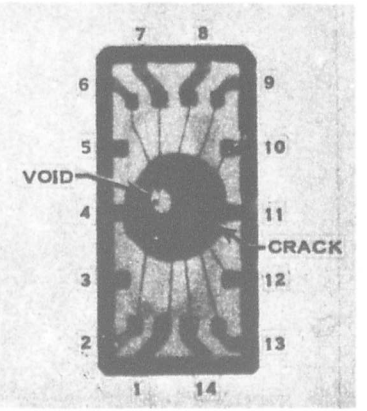
- Under bonding pad: 11%
- From scribe across one junction: 3%
- In scribe area: 68%
- In scribe not pointing toward active area: 16%
- From scribe across more than one junction: 2%



A. CRACK RADIATING FROM BONDING PAD PRIOR TO STRESS



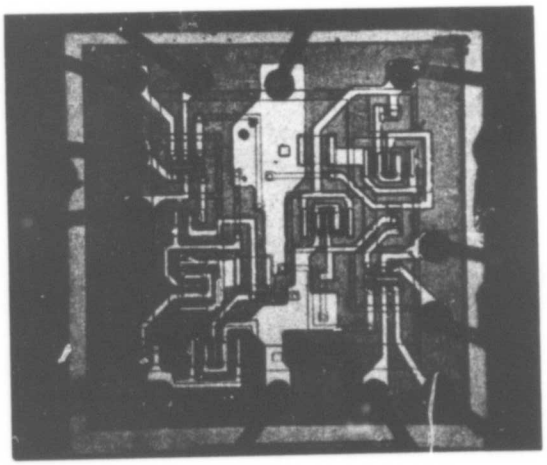
B. STRESS INDUCED FAILURE CAUSED BY SAME CRACK



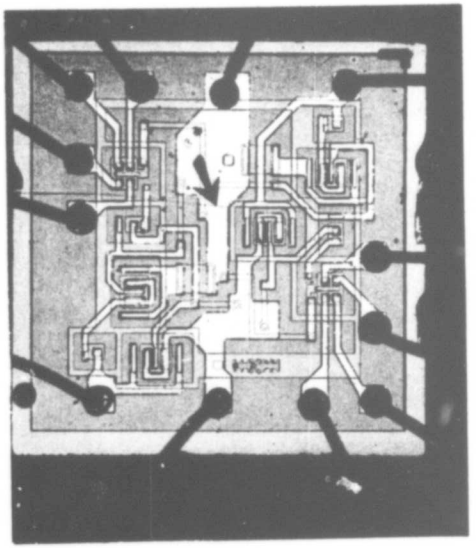
C. TOP VIEW X-RAY OF SAME UNIT. (NOTE VOID EXISTS NEAR PINS 4 AND 5 BUT CRACK OCCURRED UNDER PIN 12 PAD)

SC05688

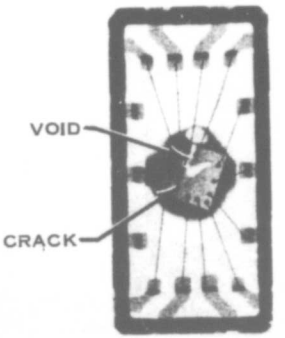
Figure D-16. Crack Through Pin 12 Bond Pad



A. PRE-CAP PHOTO OF DEVICE SHOWING NO CRACK EXISTS PRIOR TO STRESS



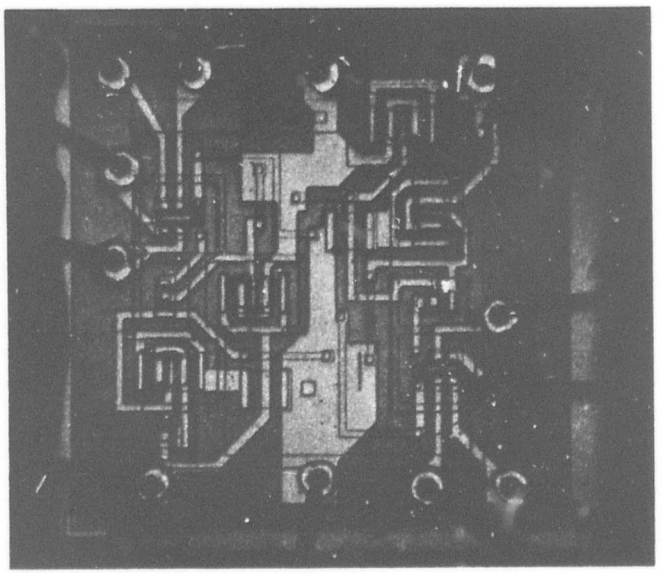
B. POST STRESS (300°C STORAGE) PHOTO OF SAME DEVICE REVEALING DIE CRACK WHICH CAUSED FAILURE



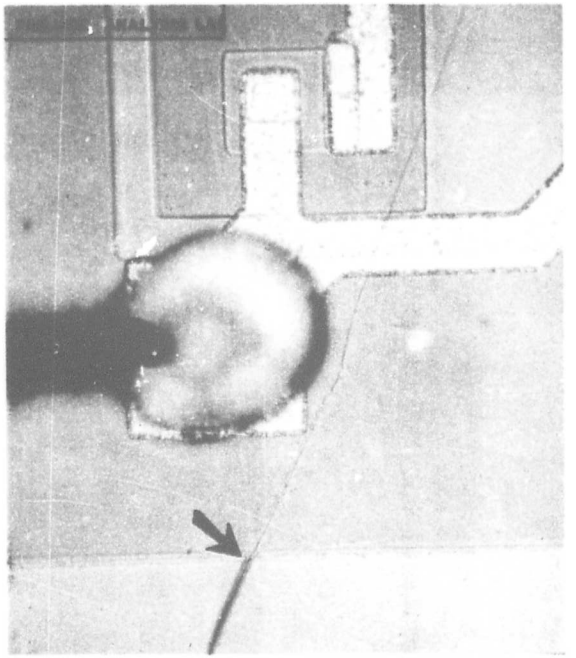
C. CORRELATION BETWEEN L-SHAPED VOID AND CRACKED DIE

SC06185

Figure D-17. Example of a Crack Crossing Active Regions



A. PRECAPSULATION PHOTO OF CRACK RADIATING FROM SCRIBE AREA TOWARD ACTIVE AREA PRIOR TO STRESS



B. PROPAGATION OF CRACK INTO ACTIVE AREA BY STRESS BY 75,000 G CONSTANT ACCELERATION (DEVICE SURVIVED 60,000 G PRIOR TO FAILURE)

SC06191

Figure D-18. Unit #0611 Crack in Die

Eleven cracked die induced failures were observed on the fixed and step stress replicate. Nine of the 11 failures resulted from cracks under bonding pads. The remaining failures were caused by:

- Crack propagated from scribe area into the active area of device. This device survived 60 KG and failed at 75 KG constant acceleration.
- Crack formed at 300°C stress, not visible at pre-cap. The crack was correlated to L-shaped void.

To evaluate the effectiveness of thermal shock (200°C to -168°C, 50 cycles, maximum transfer time of 10 seconds) and impact shock (6 KG, 50 blows all planes, 0.2 millisecond duration) as a screen for crack dice, two samples were selected from units that had survived electrical stressing. One sample contained 50 units with cracks and the other 50 units without cracks as determined from precapsulation photos. No failures were caused by either stress.

k. Resistor Degradation

Six devices from the fixed and step stress replicate were found to degrade on output short circuit current (I_{OS}). The stresses which caused these are:

- Storage Step Stress (400°C max - 1080 hours) 3 failures
- Storage Life (375°C - 528 hours) 3 failures

Typically, a decrease from 35 mA to 25 mA was observed. Extensive probing of the devices traced the cause of degradation to resistors R_2 and R_3 (see Figure B-1) but the exact cause of failure could not be determined. Refer to Sections III and IV for discussions of SERF screening and the analysis of nonfunctional parameters which relate to this failure mechanism.

l. Unknown

All functional d-c parameters were measured additionally by the Analysis Laboratory upon receipt of failures from the test program. This procedure revealed that the parameters of eight devices were well within the defined parameter failure criteria shown in Appendix C of this report. Subsequent investigations such as threshold tests and visual inspection revealed nothing irregular in the devices. Since the devices passed all d-c parameters, and since there was no evidence to show that a failure had occurred, a failure mode could not be determined. It is significant to note that all failures in this category occurred from electrical stress.

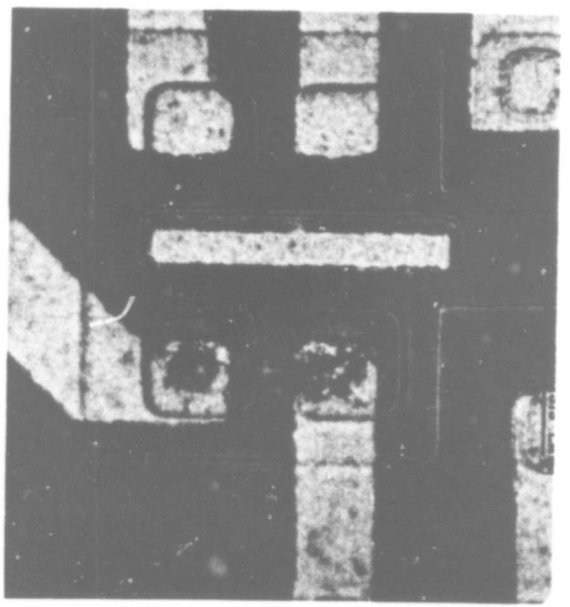
Five devices were found to have degraded functional parameters upon receipt in the Failure Analysis Laboratory. Three of the devices had actually improved (a decrease in input leakage current). Since only slight changes in the parameters occurred, failure modes could not be determined.

m. Overstress

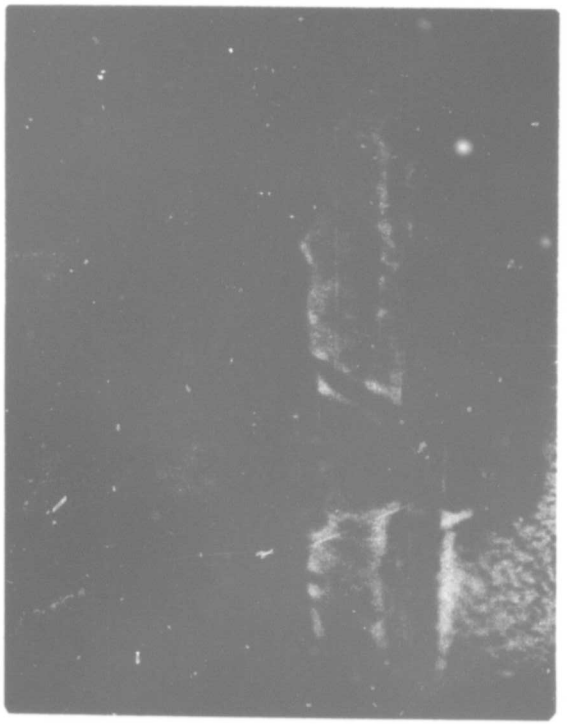
A total of 20 devices was caused to fail by overstress; namely, two from the Preliminary Investigation, six from the Step Stress Series, and twelve from the Fixed and Step Stress Series. These overstressed units were of two general types; namely, open evaporated patterns and flash-over shorts.

Figure D-19a and D-19b, respectively, are typical top view and cross-sectional views of a flashover short. The flashover short is one of the most frequently occurring failure modes resulting from electrical overstress. The visual symptom of this failure mode is a thin strip of metallic appearing substance between the two evaporated leads. The most common flashover shorts occur across the emitter-base junction, sometimes extending to the collector. This short has been frequently observed between two emitters of multiple emitter transistors. This failure mode is believed to be caused by voltages applied to the junction which are in excess of the reverse breakdown voltage.

The open evaporated patterns were the result of conduction most probably triggered by transients from power supplies turning on parasitic transistors. The existence of flashover shorts indicates that transients were present in the stress circuitry. It is logical to assume that transients that would turn-on transistor action also existed, as well as those of a reverse bias nature that caused flashover. Further evidence that these failures were stress circuit induced is the fact that bridging the open patterns caused the majority of the devices to function normally. Refer to Figure D-20 for illustration of an overcurrent failure.



A. TOPOLOGICAL VIEW OF FLASHOVER SHORT DUE TO ELECTRICAL OVERSTRESS



B. MICROSECTION REVEALING FLASHOVER SHORT TO BE AT OXIDE–SILICON INTERFACE

SC05687

Figure D-19. Typical Views of a Flashover Short

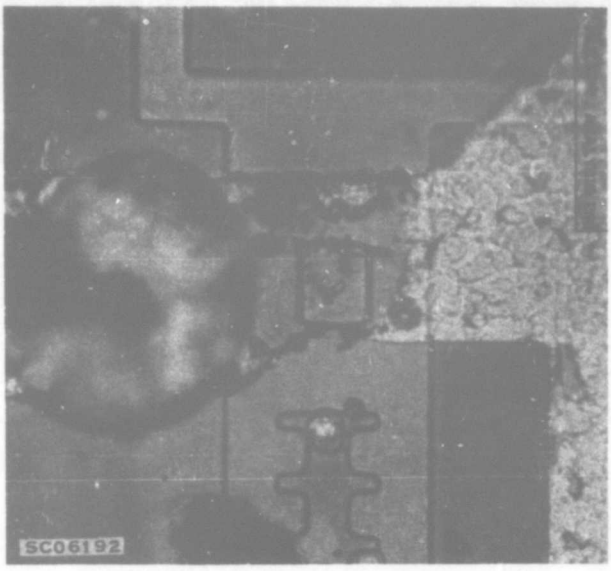


Figure D-20. Open to Substrate Window Due to Deterioration of Gold-molybdenum Materials Caused by Electrical Overstress

APPENDIX E

THEORY OF FIXED AND STEP STRESS TESTING

A brief discussion of the theory relating fixed to step stress will be given here. A more complete discussion is given in References 19, 20, 21, 22, and 23. If a sample of devices is exposed to a stress level S_2 and the number of devices failing at each read-out time is recorded during the stressing, a distribution of the number of failures as a function of time will be obtained. This is represented by B in Figure E-1. Subjecting another sample of devices to a different stress level such as S_1 will provide another distribution such as C. None of these distributions are necessarily normal. If the time for median failure for each stress level is plotted, the non-linear acceleration curve in Figure E-1 is obtained. Suitable transformations of stress and time can make the acceleration curve linear, such as the curve in Figure E-2. To be of value, these transformations must satisfy the following conditions:

a) The transformed distributions are normally distributed.

b) The standard deviations, σ, are constant and independent of the mean, μ.

c) The acceleration curve mentioned above should be linear with respect to the transferred scale.

The asterisks used in Figure E-2 denote transformed stress and time variables and the resulting transformed distributions. In Figure E-2, the stress variable is transformed by some function f_2. The same transformations are not used for both stress and time; the asterisks merely indicate that the variable has been transformed. An appropriate transformation for thermal stress is 1/T (°K) and for time is the logarithm of time. Knowing the standard deviation of the transformed normal distribution, the acceleration curve for other cumulative percent failures may be obtained. Thus the dotted line in Figure E-2 is the acceleration curve for a cumulative 3% failure (2 standard deviations from the mean).

An alternative method of generating the acceleration curve is by means of step stress testing, where a constant time for application of the stress is maintained and the stress levels are varied. In this type of testing, a group of devices is exposed to a certain stress level for a given time and then the surviving devices are exposed to the next higher stress level for the same length of time. This is usually continued until all or most of the devices have failed. It is assumed that the probability of failure at

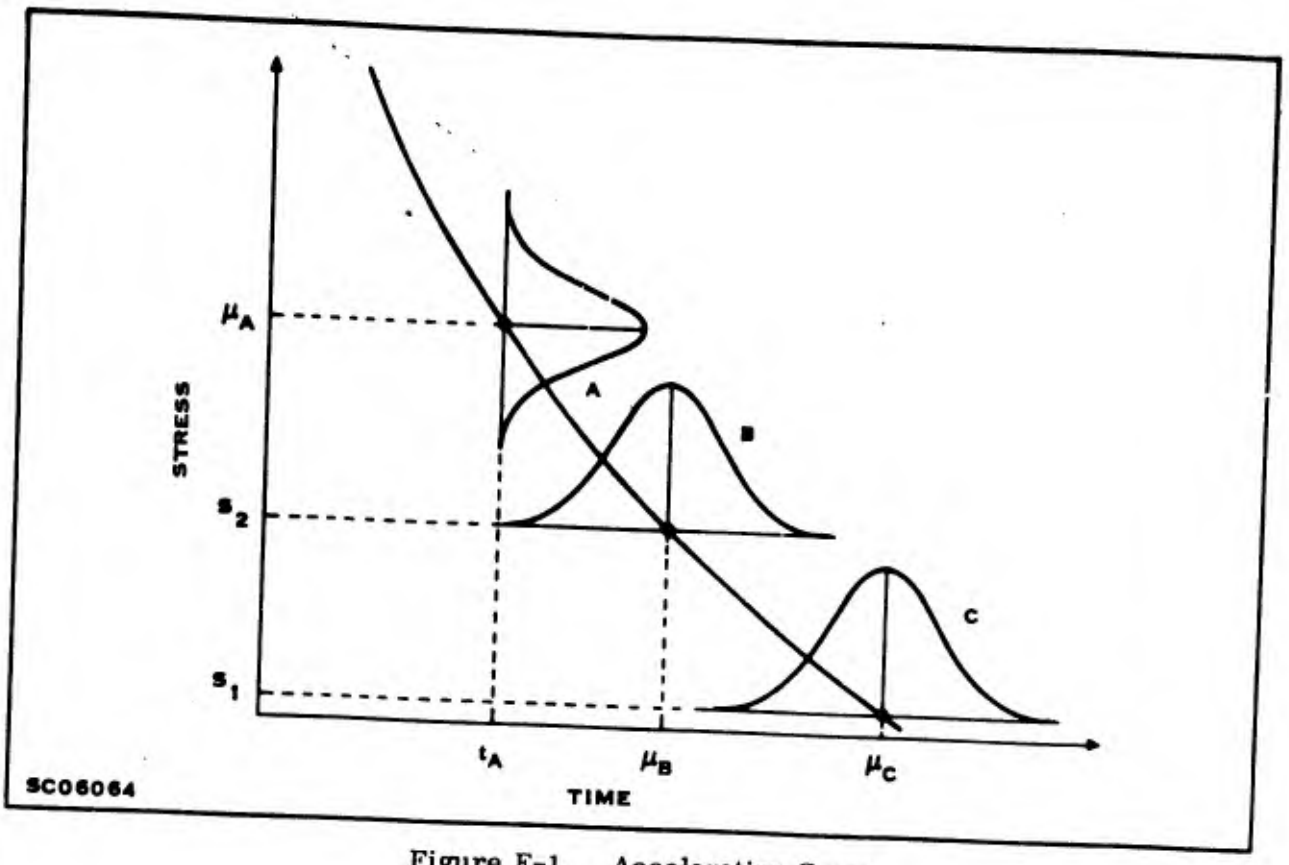


Figure E-1. Acceleration Curve

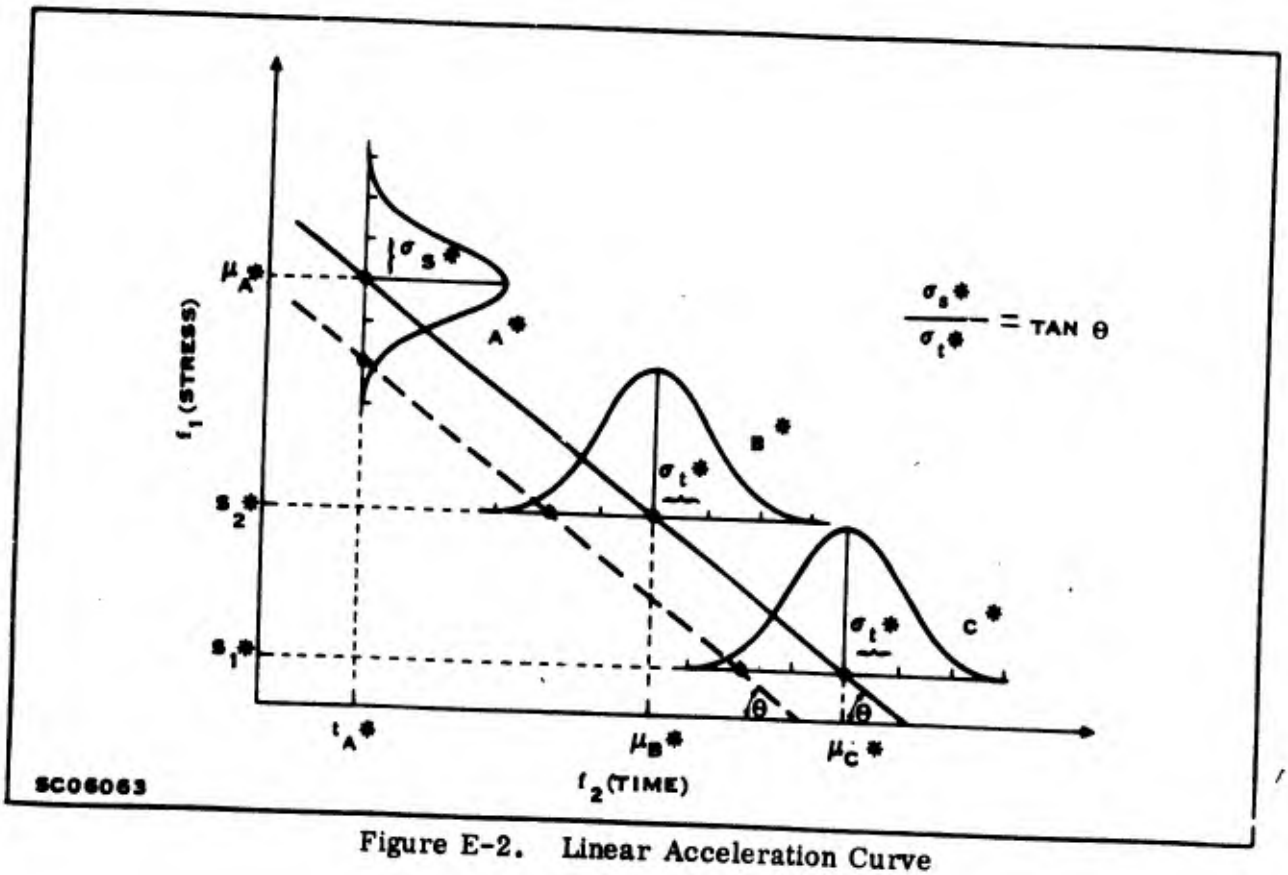


Figure E-2. Linear Acceleration Curve

a given point in the stress-time domain is independent of the path used to arrive at that point. For example, if a sample of devices is placed on a step stress test with tread-length t and the number of devices surviving after stress level S is noted, this same number of survivors should be obtained by using a constant stress test at level S for t hours. Using this assumption, the distribution of the number of failures as a function of stress obtained. An example of this is represented by A in Figure E-1. None of these distributions are necessarily normal. The median failure stresses, when plotted in the stress-time domain, should yield the same acceleration curve that is obtained by constant stress testing. Using the same transformations mentioned above, as well as assumptions a, b, and c, a linear acceleration curve such as the one in Figure E-2 may be obtained. This transformed constant time acceleration curve should be the same as the transformed constant stress acceleration curve. The transformed standard deviations of the stress and time distributions are not independent; they are related by the equation:

$$m(\text{slope of acceleration curve}) = \tan\theta = \frac{\sigma_s^*}{\sigma_t^*} \qquad \text{(E-1)}$$

The asterisks denoting transformed variables will not be used in subsequent discussions. It will be assumed, however, that in the discussions transformed stress and time is meant.

A number of other assumptions are implicit in the discussion above. First, it is assumed that the devices have been selected at random from a manufacturing process. Second, it is assumed that measurement error is very small relative to the measurement of the stress levels. Third, it is assumed that the dominant failure mechanism is being accelerated and that this dominant failure mechanism does not change over the extrapolation range. A discontinuity in either the cumulative percent failure curve or the acceleration curve may be indicative that true acceleration is not being considered. The linear approximations to the nonlinear curve may be studied in the same way that the linear curve has been studied above.

The statistical model mentioned above has not yet been tied to the actual physical degradation process. This is done by assuming that there is a predominant reaction among all the complex chemical reactions which could be taking place during degradation. This predominant reaction may be characterized by some equation which allows the degradation rate observed at high stress to be related to that at low stress.

The analysis is based on the assumption that the Arrhenius equation adequately relates reaction rate to temperature. If Q is some parameter which indicates the extent of degradation then the rate equation will be

$$\frac{dQ}{dt} = R(T) = e^{A-B/T}$$

where T is absolute temperature and A and B are constants. Integrating from some initial time t_0 to any later time t, and assuming R(T) is independent of time

$$\int_{Q_0}^{Q} dQ = \int_{t_0}^{t} R(T)\, dt$$

or

$$Q - Q_0 = R(T)\ \ (t-t_0)$$

Substituting for R(T) and taking the log of both sides we have

$$\ell n\ (Q - Q_0) = A - B/T + \ell n\ (t - t_0)$$

or (assuming for the sake of simplicity that $t_0 = 0$),

$$\frac{1}{T} = \frac{1}{B}\ell n\ t + \frac{A - \ell n\ (Q - Q_0)}{B}$$

Letting

$$\frac{A - \ell n\ (Q - Q_0)}{B} = C$$

where C is a constant the equation relating temperature and time for a fixed amount of degradation is given below. This equation is referred to as the acceleration equation.

$$\frac{1}{T} = \frac{1}{B}\ \ell nt + C$$

Using logarithms to the base 10, we would have

$$\frac{1}{T} = \frac{2.303}{B}\ \log_{10} t + C \qquad \text{(E-2)}$$

Thus if we were to plot 1/T versus $\log_{10} t$, the slope, m, would be equal to 2.303/B. Furthermore,

$$B = \frac{q E_A}{k}$$

where:

q = electron charge, 1.592×10^{-19} coulombs

E_A = activation energy (electron volts)

k = Boltzmann's constant, 1.38×10^{-23} Joules $^{\circ}C^{-1}$

Having determined the slope of (2), E_A may be calculated:

$$m = \frac{2.303}{B} = \frac{2.303k}{qE_A}$$

or

$$E_A = \frac{2.303k}{qm} = \frac{1.996 \times 10^{-4}}{m} \text{ eV} \qquad \text{(E-3)}$$

All that has been done above is to assume a simple rate equation and to derive a relation between 1/T and $\log_{10} t$. Numerous investigators have found that life test data indicates that the relation between temperature and time to failure is of the form $1/T = a \log_{10} t + b$, supporting the assumptions that often the numerous complex reactions taking place may be considered as one reaction, that the Arrhenius equation adequately describes this combination of reactions, and that it may be used to relate high stress results to low stress results.

Next a procedure is described which is used to determine the acceleration curves for fixed stress. First the cumulative percent failures versus time for each level of stress is plotted to see if the lognormal distribution is indicated. A least square fit is made of each linear section of the curve if there is a discontinuity. Some cumulative percent number is selected and the time to produce this percent failure calculated from the least square line. A point is obtained for each stress level and these are plotted as 1/T (effective temperature) versus time. The resulting 1/T versus $\log_{10} t$ points are fitted by least squares. The resulting curve is the acceleration curve for a given cumulative percent failure. The slope of the acceleration curve is available from the least square line and is used in calculating activation energy and acceleration factors.

For step stress tests the cumulative percent failure versus stress level is plotted to determine if a normal distribution is indicated. If indicated, a least square fit of the points is made. Next a certain cumulative percent failure is selected and the stress necessary to produce that percent failure determined. One point is obtained from each step stress test. These are plotted as 1/T (effective temperature) versus time to obtain an acceleration curve for the step stress data.

Plotting a normal cumulative distribution function on probability paper will give a straight line. The cumulative percent failure axis, however, is not linear. For ease in curve fitting and analysis, the cumulative percent failure points are converted to the appropriate "probit" value, λp, since the probit scale on normal probability paper is linear. The regression equations obtained from the test data are then expressed in probits. A short table of probit values for some cumulative percent points is given in Table E-1. A more complete table can be found in Reference 24. Additional information about the normal distribution and probit values can be found in Reference 25.

The constant stress tests will provide plots of cumulative percent failure versus $\log_{10} t$ and the step stress tests will provide plots of cumulative percent failure versus 1/T (°K). Converting these cumulative percent failure points to probability units and fitting a least square line will yield an equation of the form

$$\lambda^{(1)}_p = a_1 + b_1 \log_{10} t \qquad \text{(E-4)}$$

or

$$\lambda^{(2)}_p = a_2 + b_2 \times 10^3 \left(\frac{1}{T}\right) \qquad \text{(E-5)}$$

The superscripts in Equations (E-4) and (E-5) are used here to avoid confusing the fixed stress and step stress data. These superscripts will not be used in Section VI since each equation is clearly described. The terms b_1 and $b_2 \times 10^3$ are reciprocals of standard deviations G_t and G_s respectively, shown in Figure E-2. It has been shown in Equation (E-1) that σ_t and σ_s are related by the equation $\sigma_s/\sigma_t = \tan\theta = m$. Knowing these σ values allows the comparison of the fixed and step stress results.

An example is now used to illustrate the use of some of the equations mentioned in this Appendix. Suppose the following regression equations are derived from the hypothetical step stress data presented graphically in Figure E-3.

$$\lambda p = 23.0 - 10.0 \frac{1000}{T} \quad \text{(8 hr/step)} \qquad \text{(E-6)}$$

Table E-1. Probit Values for Selected Cumulative Percent Points

Cumulative Percent	Probit Value
5	3.36
10	3.72
15	3.96
20	4.16
25	4.33
30	4.48
35	4.61
40	4.75
45	4.87
50	5.00
55	5.12
60	5.25
65	5.39
70	5.50
75	5.67
80	5.84
85	6.04
90	6.28
95	6.65

$$\lambda p = 23.7 - 10.0 \frac{1000}{T} \quad \text{(16 hr/step)} \tag{E-7}$$

$$\lambda p = 25.1 - 10.0 \frac{1000}{T} \quad \text{(64 hr/step)} \tag{E-8}$$

The stress necessary to produce 50% failure in the 8 hour/step stress data will be calculated. Referring to the probit listing in Table E-1, the probit value corresponding to 50% failure is 5.00, so substituting in Equation (E-6),

$$5.00 = 23.0 - 10.0 \frac{1000}{T}$$

or

$$T = 555°K \ (= 272°C)$$

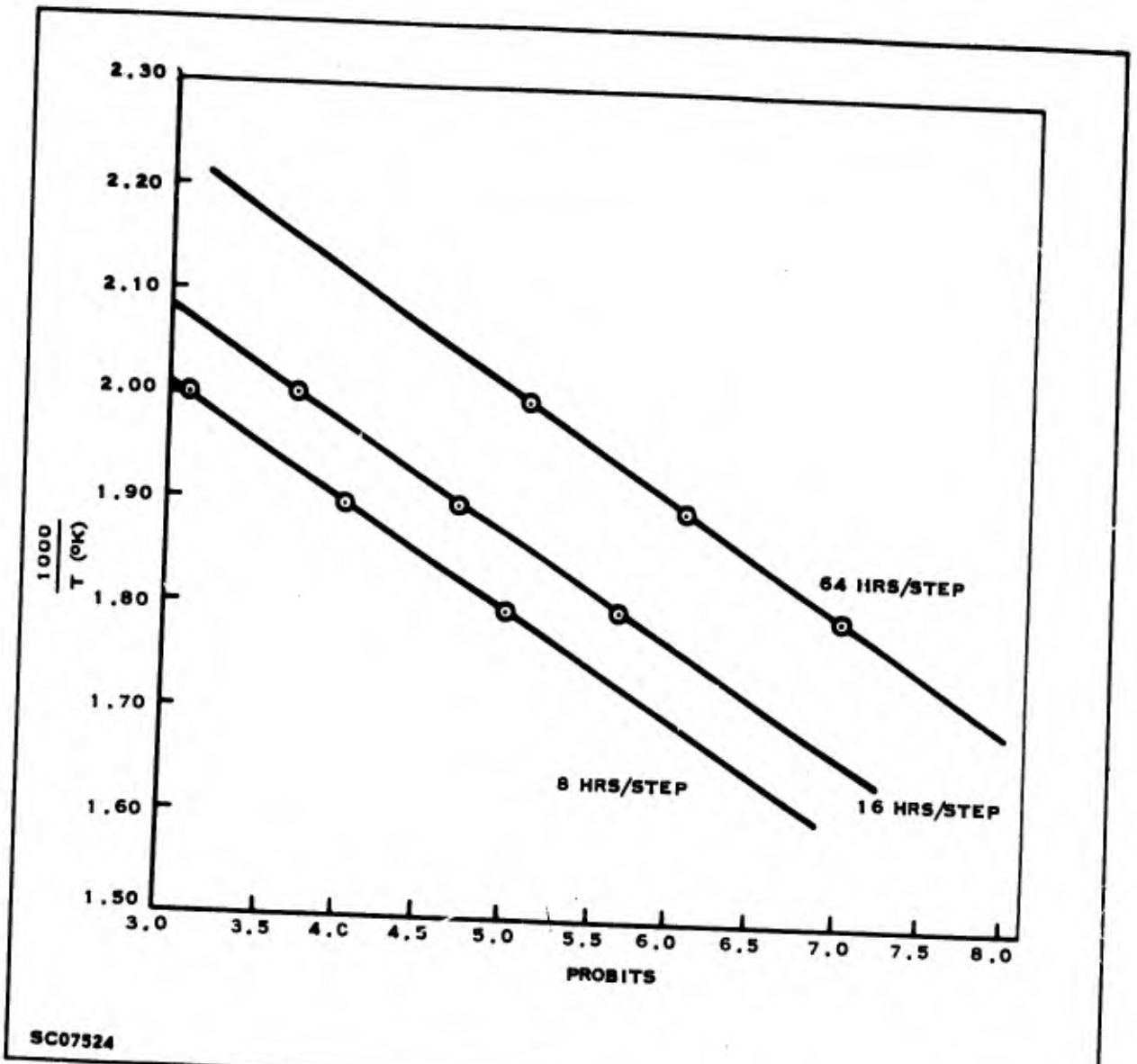


Figure E-3. Illustrative Cumulative Percent Failure Curve

Thus according to the 8 hr/step stress results, 50% failure occurs at 272°C. Conversely, if it were desired to calculate the cumulative percent failure of the 8 hr/step stress tests up to a temperature of 272°C, Equation (E-6) could be used to solve for λp in probits and thus connected to cumulative percent failure as noted in Equation (E-6), the standard deviations of these normal distributions are simply the reciprocals of the coefficients of the 1/T term. In this case the standard deviation, G_s, of these three cumulative percent failure curves would be $1/(10 \times 10^3) = 1.0 \times 10^{-4}$.

The temperature for 50% failure on each of the 3 step stress tests is plotted in Figure E-4. A least square fit to these points is the acceleration curve,

$$\frac{1000}{T} = 1.60 + 0.230 \log_{10} t$$

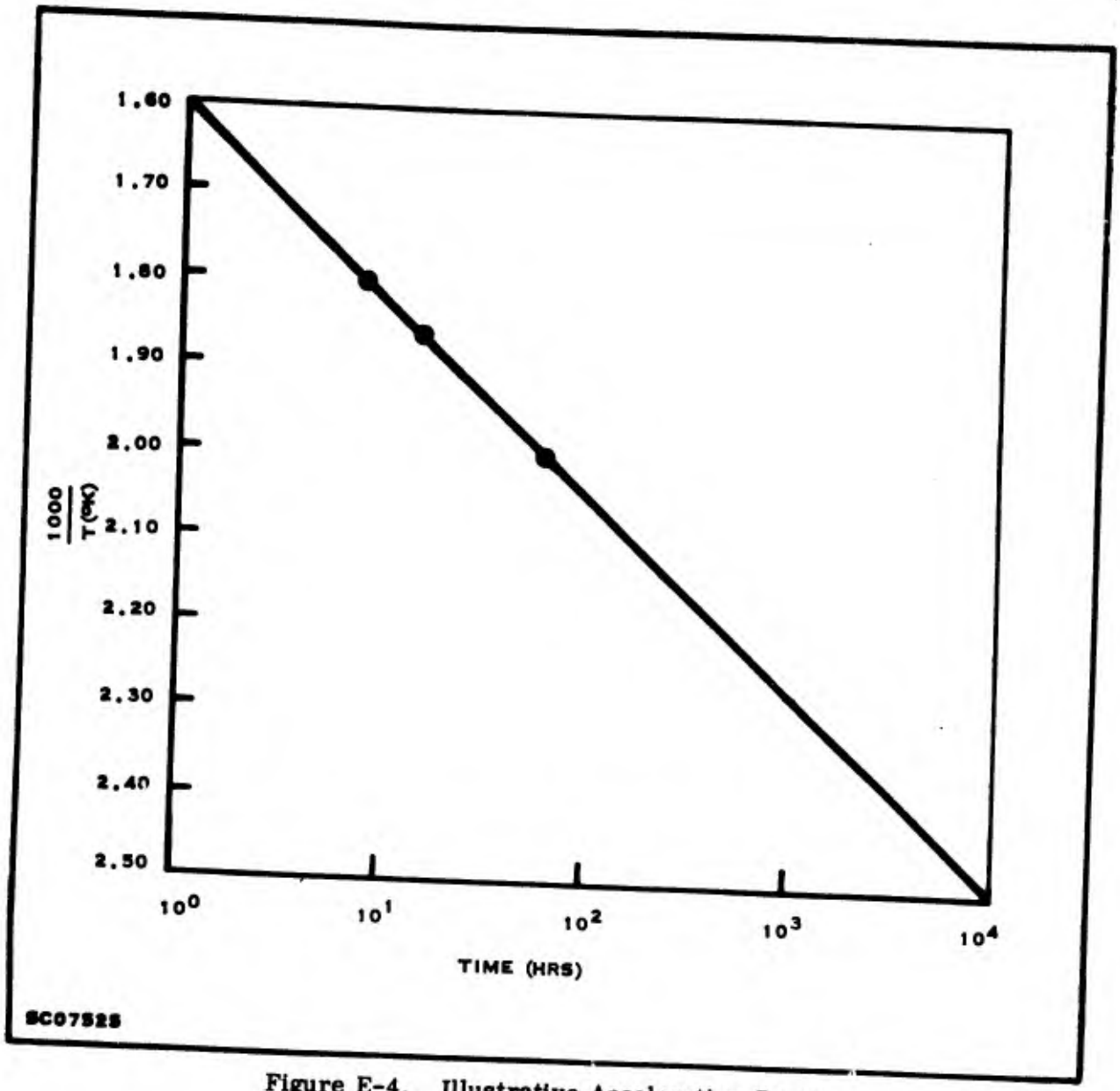


Figure E-4. Illustrative Acceleration Curve

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13. ABSTRACT

This report is the last in a series of three reports relating to the work performed by Texas Instruments under this contract. The work is divided into four parts: (1) Data analysis and preliminary tests to determine failure mechanisms for early direction in the study; (2) a physics of failure program consisting of fundamental oxide studies, metal contact and interconnection evaluations, and circuit analysis; (3) a test program including data and failure analysis and consisting of two major segments; and (4) the development of a reliability screening procedure for integrated circuits. Three computer programs, SERF, LINDA 1 and LINDA 2 were written to assist in the analysis of data.

The physics of failure program consisted of fundamental surface studies to produce stable metal-oxide-silicon (MOS) systems, circuit analysis of the SN5420 integrated circuit, and a study of the molybdenum-gold expanded contact system.

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14. KEY WORDS	LINK A		LINK B		LINK C	
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