AD NUMBER: AD0818971

LIMITATION CHANGES

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AUTHORITY

AFWL ltr dtd 30 Nov 1971

HANDBOOK FOR PREDICTING SEMICONDUCTOR DEVICE PERFORMANCE IN NEUTRON RADIATION

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The Bendix Corporation
Research Laboratories Division
Southfield, Michigan 40876

Contract AF 29(601)-7110

TECHNICAL REPORT NO. AFWL-TR-67-54
August 1967

AIR FORCE WEAPONS LABORATORY
Research and Technology Division
Air Force Systems Command
Kirtland Air Force Base
New Mexico

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REPLY TO ATTN OF: WLDN

18 Aug 1967

SUBJECT: Status Letter #1

TO: Handbook Users

1. This handbook presents a neutron damage prediction technique for minority carrier semiconductors as a guide to hardened electronics circuit designers and systems planners. It involves an empirical approach dependent upon electrical measurements of physical characteristics and experimental determination of specific device-type damage factors. Its objective is to provide a nondestructive radiation-effects prediction technique useful as an engineering design tool, for quality assurance, or survivability/vulnerability analysis.

2. The present status is limited to a one-dimensional treatment of long term permanent degradation of minority carrier semiconductor devices due to neutron displacement damage. Current deficiencies include the inability to predict surface damage, short term annealing behavior, gain operation in saturation, and secondary breakdown.

3. The handbook employs a radiation damage exposure measurement technique based on Radiation Damage Units (RDU's). The RDU concept is very useful in situations where adequate conventional dosimetry is not available. The user is cautioned not to consider the RDU concept as a method to replace foil activation dosimetry. The RDU concept was included so that the prediction technique would not be limited in use to those facilities that could provide adequate conventional foil activation dosimetry.

4. The Air Force Weapons Laboratory (AFWL) will continue to improve and expand this handbook. The first planned revision will be on gain operation in saturation. Any suggested revisions or improvements originated by users are encouraged and should be submitted to AFWL for inclusion in future editions.

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CARL J. SCHRA, Maj, USAF
Chief, Nuclear Power Branch

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FOREWORD

This report was prepared by the Bendix Research Laboratories, Southfield, Michigan, under Contract AF 29(601)-7110. The research was performed under Program Element 6.24.05.06.4, Project 1831, Task 183108.

Inclusive dates of research were October 1965 to June 1967. The report was submitted 7 June 1967 by the Air Force Weapons Laboratory Project Officer, Captain Richard L. Walker (WLDN).

The handbook was written by Max Frank, with contributions by Carl D. Taulbee, Allen E. McCardell, and Rudolf Six. Major editorial contributions were made by Captain Richard L. Walker and Frank Larin. Lt Charles Ramsey, Dale C. Jones, and Richard H. Wagner also commented generously.

The analytical procedures described in the handbook were developed primarily by Max Frank and Frank Larin. Valuable contributions were made by many other Bendix personnel in the course of the three years leading to this handbook, including the following from the Research Laboratories: Frank Adams, James Brosko, Harold Chambers, Ramiro Del Rosario, Charles Flint, David Nelson, Donald Niehaus, Frank Poblenz, Tory Sebring, Richard Sweet, Ken Van Landingham, and Richard Wagner, and Hy Newman and Chuck Carrol of Bendix Semiconductor Division. Semiconductor manufacturers were very cooperative in supplying proprietary dimensions and doping properties of their devices. Leo Flores and others at the White Sands Missile Range Fast Burst Reactor provided valuable assistance in the performance of the radiation tests.

This technical report has been reviewed and is approved.

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ABSTRACT

(Distribution Limitation Statement No. 2)

Procedures are presented for predicting transistor and diode electrical performance after permanent damage from neutron radiation. The prediction techniques are illustrated with examples of step-by-step calculations to facilitate use by circuit designers familiar with semiconductor device operation but not familiar with radiation damage effects in the devices. The handbook contains predictions of transistor current gain, saturation voltage, forward voltage, breakdown voltage, leakage current and switching time, forward voltage of power diodes, and transistor current gain in microelectronic configurations. Measurements of important physical device parameters needed in the prediction equations are described in detail. Also described is a procedure for measuring radiation test exposure in Radiation Damage Units (RDU) by using transistor Radiation Damage Monitors (RDMs).

PREFACE

An increasing proportion of the electronic systems being developed must be capable of operating in environments of electromagnetic and neutron radiation generated by nuclear reactors for power and propulsion purposes and by nuclear weapons. The capability of electronic systems for reliable operation in a radiation environment is usually limited by the performance of the individual semiconductor components. Prediction of the behavior of electronics in radiation is limited by the ability to predict the behavior of individual components. This handbook has been compiled for electronic circuit designers as a source of detailed descriptions of the techniques now available for predicting the effects of neutron displacement radiation damage to individual silicon semiconductor components. Transient effects due to ionization by radiation are not included.

The electronic circuit designer using this handbook is assumed to have a working knowledge of semiconductor devices, terminology and electrical behavior but to be unfamiliar with radiation or radiation effects terminology. The radiation information is therefore treated in greater detail than the semiconductor aspects.

In theory, both the pre-irradiation and post-irradiation electrical behavior of semiconductor devices are completely described by the material characteristics and physical dimensions, that is, the geometry, impurity concentration and minority carrier lifetime in each region of the device. The ideal method for predicting the effect of radiation would be by measuring the change in the semiconductor material lifetime and impurity concentration. The general approach of this handbook is based on the analytical relations between material properties, physical dimensions and electrical characteristics of semiconductor devices whenever this approach leads to a simple and accurate technique for prediction of component behavior. In most instances, the analytical approach is used to obtain the form of the electrical parameter dependence on the physical characteristics, using experimentally determined empirical factors that give reasonably accurate predictions. An important result of the extensive studies that led to this handbook is the conviction that the essential problem in predicting damage effects to semiconductor devices is understanding the material, geometry and electrical parameter relationships. Where these are well understood, the prediction of the device behavior in radiation is relatively straightforward. Conversely, those parameters whose behavior without radiation is not well understood are the most difficult to predict after radiation.

The emphasis in this handbook is on silicon devices, discrete transistors and diodes and the displacement damage from neutron radiation. Although this includes a large fraction of the applications for

hardened electronics, more effort is required, particularly to develop similar prediction techniques for other types of components such as silicon controlled rectifiers and unijunction transistors, and measurement techniques for microelectronic circuits.

The initial objective of the development programs that led to this handbook was the prediction of component behavior for nuclear aerospace power systems. Fortunately, almost all of the results that are applicable to nuclear reactor applications are also applicable to the prediction of permanent displacement damage from nuclear weapons.

The handbook is divided into eight major sections. The first two sections summarize the understanding of radiation, radiation measurement, and radiation damage effect to silicon material. The third section discusses measurement of radiation exposure. Sections 4 through 8 present detailed techniques for predicting the effect of radiation exposure to transistors, diodes, and microelectronic active elements. The electrical measurement circuits and measurement techniques are described in Appendices A and B. Of greatest importance is the base transit time measurement procedure given in Appendix A.

NOTE: The application of this technique is not limited to the use of the reference RDU (White Sands Fast Burst Reactor) employed in this handbook. Any convenient fast neutron radiation environment with an acceptable neutron-to-gamma ratio can be used or a reference exposure to calibrate RDMs for subsequent testing. In this case, however, the values of the empirical damage factors reported in the handbook cannot be employed directly. To use the values reported in this handbook, it is necessary to calibrate the new reference exposure to the White Sands reference exposure with RDMs as explained in section 3.

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SYMBOLS

A - Area, area of junction (cm^2)

A - Constant in f_T bridge equation

A_E - Emitter area (cm^2)

A_j - Area of junction (cm^2)

α - Short circuit current gain of base transport for the intrinsic transistor

α' - Common base short circuit current gain, includes influence of C_{TE} on α but not that of r_b' and C_{TC}

α_o - Low frequency short circuit common base current gain

B - Constant in f_T bridge equation

BV - Breakdown voltage (V)

BV_{CBO} - dc breakdown voltage collector-base reverse biased, emitter open-circuited (V)

BV_{CEO} - dc breakdown or sustaining voltage collector-emitter reverse biased, base open-circuited (V)

C - Base transit time bridge external capacitance in base arm (F)

C_{DE} - Diffusion capacitance at emitter (F)

C_{TC} - Collector transition layer capacitance (F)

C_{TE} - Emitter transition layer capacitance (F)

C_c - Collector transition layer capacitance at collector-base voltage V_{cb} (F)

C_c - Collector stray capacitance in transit time bridge (F)

$\bar{C}_c$ - Average capacitance from graphical integration C_c versus V_{cb} curve over operating range of V_{cb} from zero volts to cut-off voltage (F)

C_{cbo} - Capacitance between collector-base terminals, emitter open-circuited (F)

C_j - Junction capacitance (F)

D - Diffusion coefficient (cm^2/s)

D - Damage

D(E) - Damage cause by each neutron of energy E

D_n - Diffusion coefficient for electrons in p-type (cm^2/s)

D_p - Diffusion coefficient for holes in n-type (cm^2/s)

D_r - Damage in reference neutron environment

D_x - Damage in unknown neutron environment

Δ - Increment of variable

E - Energy (eV)

e - Base of natural logarithm

ε - Dielectric constant, permittivity (F/cm)

F - Neutron spectrum correlation factor

F(E) - Neutron spectrum correlation factor for neutrons of energy E

F_x - Neutron spectrum correlation factor of unknown environment

f - Frequency (Hz)

f_T - Common emitter current gain-bandwidth product (Hz)

$f_{T(max)}$ - Maximum common-emitter current gain-bandwidth product (Hz)

f_α - Alpha cutoff frequency (Hz)

$f_{\alpha b}$ - Common base cutoff frequency (Hz)

$f_{\alpha e}$ - Common emitter cutoff frequency (Hz)

g_e - Short circuit common base input conductance of intrinsic transistor (Ω^{-1})

h_{FE} - Common emitter dc current gain

$h_{FEO}(0)$ - Common emitter dc current gain before irradiation

h_{FEO} - Unirradiated common emitter dc current gain

h_{fe} - Common emitter small signal short circuit current gain

h_{feo} - Preradiation common emitter small signal short circuit current gain

$h_{fe}(o)$ - Low frequency common emitter small signal short circuit current gain

I_B - Total dc base current (A)

$I_B(0)$ - Base current at instant of turn-on pulse (A)

I_{B1} - Turn-on base current (A)

I_{B2} - Turn-off base current (A)

I_C - Collector current (A)

I_{CBO} - Collector-base reverse current, emitter open-circuited (A)

$I_{CBO}(0)$ - Collector-base reverse current, emitter open-circuited before irradiation (A)

I_D' - Diffusion current from base into emitter (A)

I_E - Emitter current (A)

I_F - Diode forward current (A)

I_R - Reverse current at junction (A)

I_{RB} - Base current component due to base region recombinations (A)

I_{RG} - Current due to carrier recombination-generation in junction transition layer, base current component due to carrier recombinations in forward-biased emitter transition layer (A)

I_S - Base current component due to surface effects (A)

i_b - ac base current (A)

i_c - ac collector current (A)

i_{cx} - ac current through C_{TC} in equivalent transistor circuit (Figure A-2) (A)

i_d - ac diffusion current of intrinsic transistor defined by

$$i_d = \alpha_o i_{g_e} / \alpha \quad (A)$$

i_e - ac emitter current (A)

i_{g_e} - ac current through conductance g_e of intrinsic transistor (A)

J - Current density (A/cm^2)

J_E - Emitter current density (A/cm^2)

j - Imaginary unit ($j^2 = -1$)

K - Empirical damage factor* $(RDU\text{-}s)^{-1}$

K_N - Carrier removal rate coefficient in bulk material* $(cm^3\text{-}RDU)^{-1}$

K_N' - Carrier removal rate coefficient in junction transition layer* $(cm^3\text{-}RDU)^{-1}$

---

*Note that 1 RDU = 1 n/cm^2 at a particular spot in the White Sands Fast Burst Reactor $\approx$ 0.8 n/cm^2 fission energy spectrum.

K_{rg} - Radiation damage coefficient for junction transition layer* $(RDU\text{-}s)^{-1}$

K_{ω} - Radiation damage factor at high injection* $(RDU\text{-}s)^{-1}$

K_{τ} - Minority carrier lifetime radiation damage factor* $(RDU\text{-}s)^{-1}$

K_{τ}' - Reciprocal of K_{τ}* (RDU-s)

$K_{\tau\gamma}$ - Gamma radiation minority carrier lifetime radiation damage factor $(R\text{-}s)^{-1}$

k - Boltzmann's constant (1.38×10^{-16} erg/°K)

k - Constant proportional to volume of collector-base transition layer (A-s)

L - Diffusion length for injected minority carriers (cm)

L - Inductance in collector arm of base transit time bridge (H)

M - Constant in f_T bridge equation

N - Impurity concentration after radiation ($atoms/cm^3$)

N' - Impurity concentration for one ohm-cm silicon ($atoms/cm^3$)

N_A - Acceptor impurity concentration ($atoms/cm^3$)

N_D - Donor impurity concentration ($atoms/cm^3$)

$N_{FBR}(E)$ - Normalized White Sands Fast Burst Reactor neutron spectrum (n/MeV)

N_o - Unirradiated impurity concentration ($atoms/cm^3$)

n - Neutrons (n)

n - Exponent in BV_{CEO} (equation 6-5)

n - Electron concentration (cm^{-3})

---

*Note that 1 RDU = 1 n/cm^2 at a particular spot in the White Sands Fast Burst Reactor ≙ 0.8 n/cm^2 fission energy spectrum.

Δn - Excess or injected minority carrier electron concentration (cm^{-3})

n_i - Intrinsic concentration of holes, electrons (cm^{-3})

n - Reciprocal forward V-I slope factor

p - Hole concentration (cm^{-3})

Q_b - Excess charge stored in the base region due to diffusion current injected from the emitter (C)

q - Charge of an electron (1.6×10^{-19} coulomb)

R - Roentgen

R - Recombination rate per carrier (s^{-1})

RDU - Radiation Damage Unit (see Section 3.1 for general definition). In this handbook 1 RDU = 1 n/cm^2 at a particular spot in the White Sands Fast Burst Reactor $\doteq$ 0.8 n/cm^2 fission energy spectrum.

RDU_x - Radiation exposure of unknown environment in radiation damage units (RDU)

R_B - Base resistance (Ω)

R_C - Collector resistance (Ω)

R_E - Emitter resistance (Ω)

R_F - Diode forward resistance (Ω)

R_L - Collector load resistance (Ω)

R_o - Preradiation recombination rate per carrier (s^{-1})

r - Base transit time bridge external resistance in collector arm (Ω)

r_b' - Extrinsic base resistance (Ω)

ρ - Resistivity (Ω-cm)

T - Temperature (°K), (°C)

t - Time (s)

t - Base transit time (s)

t' - Total delay time for carriers crossing from emitter to collector (s)

t_d - Delay time (s)

t_f - Fall time (s)

t_r - Rise time (s)

t_s - Storage time (s)

t_s - Switching time (s)

τ - Minority carrier lifetime (s)

τ_c - Minority carrier lifetime in the collector (s)

τ_o - Initial or preradiation minority carrier lifetime (s)

V - Voltage, applied voltage (V)

V_{BB} - Base supply voltage (V)

V_{BE} - dc base-emitter voltage (V)

$V_{BE(SAT)}$ - Base-emitter saturation voltage (V)

V_{CB} - dc collector-base voltage (V)

V_{CBO} - dc collector-base voltage, emitter open-circuited (V)

V_{CC} - Collector supply voltage (V)

V_{CE} - dc collector-emitter voltage (V)

$V_{CE(SAT)}$ - Collector-emitter saturation voltage (V)

V_F - Diode forward voltage (V)

V_{IN} - Pulsed input voltage (V)

V_R - Junction reverse voltage (V)

V_T - Built-in or electrostatic potential difference across the junction transition layer at zero applied voltage (V)

V_{cb} - Collector-base voltage during switching (V)

V_j - Junction voltage (V)

$V_o(t)$ - Open circuit junction voltage after forward conduction pulse (V)

v - Velocity (cm/s)

W - Length of diode base region (cm)

W_C - Length of collector region (cm)

W_b - Width of transistor base region (cm)

W_j - Width of junction (cm)

ϕ - Neutron fluence* (RDU)

$\phi^*(t)$ - Effective neutron fluence required to produce the damage at time t after burst (n/cm^2)

ϕ_r - Neutron fluence in reference neutron spectrum* (RDU)

ϕ_x - Neutron fluence in unknown neutron environment* n/MeV

ϕ_γ - Gamma radiation exposure (R)

ω - Angular frequency (radians/s)

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*Note that 1 RDU = 1 n/cm^2 at a particular spot in the White Sands Fast Burst Reactor ≈ 0.8 n/cm^2 fission energy spectrum.

SECTION 1

RADIATION ENVIRONMENT

1.1 NEUTRON RADIATION TERMINOLOGY

The two types of radiation considered in this document, neutrons and gammas, emanate from nuclear reactors and nuclear weapons. The radiation exposure from a reactor or weapon is given in units of fluence. For neutrons, the fluence is the number of neutrons passing through a sphere one square centimeter in cross section, with units of n/cm^2 or nvt. The radiation rate is called the neutron flux with units of n/cm^2-s or nv. The symbols n/cm^2 and nvt are both used for fluence. They are the same unit except the n in nvt means neutron density while the n in n/cm^2 is only a number. Thus

$$\phi\ (nvt) = \frac{n}{cm^3} \times \frac{cm}{s} \times s = \frac{n}{cm^2} \qquad (1\text{-}1)$$

These neutrons are not monoenergetic but are distributed over a range of energies from thermal energy (approximately 0.026 eV) to 14 MeV. Neutrons generated in a fission process in a nuclear reactor or nuclear weapon have an initial unique energy distribution given in Figure 1-1 by the curve labeled Watts fission spectrum. This curve gives the percentage of neutrons with energies greater than E at any given energy for a fission source. As these neutrons leave their source, they interact with surrounding materials and their energy distribution is modified. Radiation from a fission plate in a conventional reactor or a bare fuel assembly, such as the White Sands Missile Range Fast Burst Reactor, have spectra approaching a fission spectrum.[1] The integral neutron spectrum for the Fast Burst Reactor (FBR) is compared in Figure 1-1 with a Watts fission spectrum. The mean neutron energy of the FBR is about 1 MeV, compared to 1.64 MeV for the Watts fission spectrum.

A pure monoenergetic 14 MeV flux from a fusion weapon, or a fission spectrum from a fission weapon or reactor is not encountered in practice. The spectrum is always modified and therefore is almost impossible to simulate. The largest deviation from a fission spectrum results from a thermal reactor, such as a water-moderated, swimming-pool reactor, in which many of the neutrons are deliberately slowed to thermal energy. As the energy of the neutron is reduced, the damage it is capable of producing in a semiconductor material is also reduced. The energy dependence of radiation damage is discussed in Section 2.5.

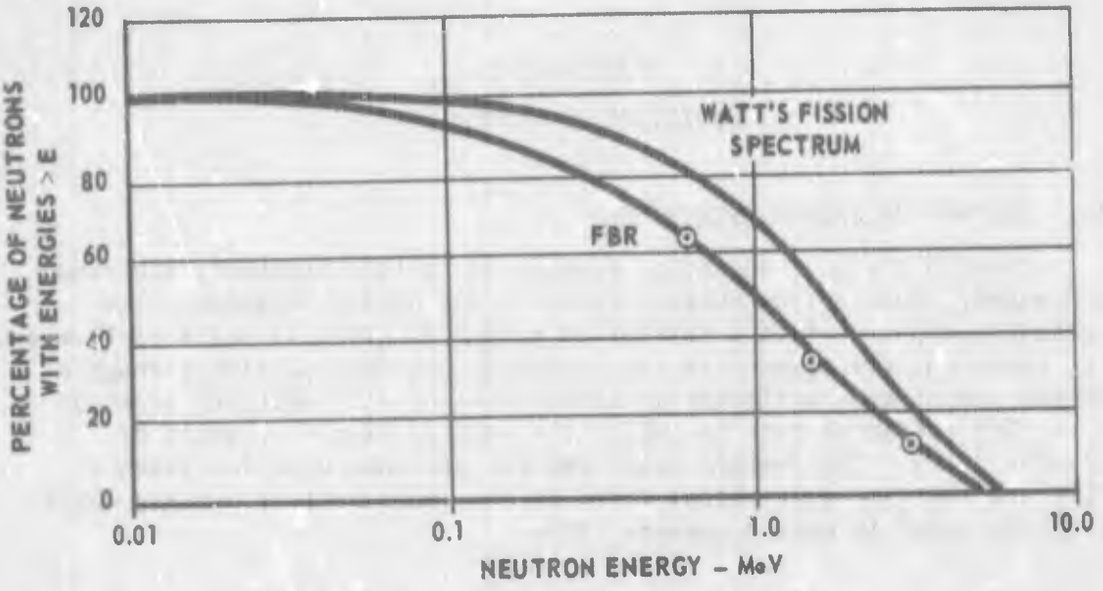

Figure 1-1. Comparison of Watts fission spectrum and White Sands Fast Burst Reactor spectrum

The neutron radiation environment is frequently given in two numbers: thermal neutrons, i.e., those neutrons at an energy equivalent to the ambient temperature; and fast or epithermal neutrons, i.e., those neutrons with energies above some arbitrary level. The arbitrary level most frequently used is 0.1 MeV. Thermal neutrons cause no damage to the semiconductor material itself; i.e., do not displace atoms from their lattice positions, but rather interact inelastically to cause nuclear transformations. These are not significant in the general problem of radiation effects in semiconductors.

1.2 GAMMA RADIATION TERMINOLOGY

The other radiation from a nuclear reactor or nuclear weapon is electromagnetic or gamma radiation.

The most convenient unit to describe the amount of gamma radiation exposure for radiation damage studies is the rad. While fluence is an indication of the number of photons, the rad is an indication of the effect of radiation in a material. One rad is the amount of radiation that deposits 100 ergs of energy per gram of specific material. The material of interest in semiconductor damage is usually silicon. Thus one rad (silicon) indicates a radiation that deposits 100 ergs in a gram of silicon.

A related unit used to describe gamma radiation is the roentgen (R), which is defined in terms of the amount of ionization the radiation produces in air. Numerically, one R and one rad (silicon) are approximately the same for most gamma ray energies. At 1 MeV, a rad (silicon) is about 15 percent larger than a roentgen.

There are two types of gamma radiation: prompt gammas and delayed gammas. Prompt gammas are those given off directly during fission, which move through space with the speed of light and are first to arrive at the target, causing a bulk transient ionization effect. Delayed gammas stem from the radioactive decay of materials made radioactive by the capture of the neutrons. Since neutrons move through space with a velocity that is energy-dependent, the gammas that result from neutron activation are delayed in time from the prompt gammas.

SECTION 1 - REFERENCE

1. "Characteristics of Nuclear Effects Branch Radiation Facilities and Operational Procedures," White Sands Missile Range Memorandum, March 1966.

SECTION 2

DAMAGE EFFECTS IN SEMICONDUCTORS

2.1 RADIATION DAMAGE TERMINOLOGY

The effects of neutron and gamma radiation to silicon are divided into two major categories, displacement effects and ionization effects. Displacement damage efffects are those due to the physical displacement of atoms from their normal lattice positions in a silicon crystal. Ionization effects are those due to the temporary freeing of the orbital electrons of an atom. As a first approximation, neutrons can be assumed to cause the displacement effects and gammas the ionization effects.

Neutrons cause large defect clusters or disordered regions of hundreds of atoms. The mass of the neutron is big enough to transfer a large amount of energy to an individual silicon atom. This atom in turn interacts with other atoms to result in hundreds of displacements. Most of the predictions that follow are predictions of the effect of these large defect clusters on the electrical properties of silicon devices.

Gamma radiation like neutron radiation has an energy spectral dependence with a mean energy between 2 and 3 MeV. The gammas ionize the semiconductor materials through photoelectric, Compton, and pair-production processes. The resulting energetic electrons in turn damage the material by displacing atoms from their lattice sites, causing Frenkel pairs or vacancy-interstitials. Since 15 to 30 eV of energy must be transmitted to a silicon atom to displace it from its lattice site and since about 10^4 as much energy is required in the electron to deliver the 15 eV to the silicon atom, the threshold for displacement damage from electromagnetic radiation is 150 keV photons. As this is an inefficient process, the effects of gamma rays, as a first approximation, are associated with ionization effects only.

Simulation of the 2 to 3 MeV gamma photon energy displacement damage is difficult because the damage caused by electrons in the 0.5 to 10 MeV range is a very strong function of energy. Cobalt-60 sources with photon energies of about 1 MeV are often used to study nuclear reactor and nuclear weapon gamma displacement damage; however, the results can be misleading since the displacement damage for the 2 to 3 MeV photons is several times larger.

The other important aspect of the gamma radiation is its intensity. In power reactors such as SNAP, 2, 10 A, and 50, the gamma intensity can be quite significant in as assessment of displacement damage. If the neutron-to-gamma ratio is larger than 10^7 n/cm^2 per rad (silicon) the gamma displacement effects can be neglected. In nuclear weapons the

gamma intensity is insignificant in causing displacement damage. Gamma radiation is always important in surface damage effects, although nuclear weapon environments produce less surface effects for the same exposure than longer-delivery-time nuclear reactor environments.

Ionization effects can be further subdivided into transient bulk effects and surface effects. Transient bulk effects are the electrical result of high rates of ionization which affect the resistivity of the silicon and which cause spurious currents to flow by the same photoelectric mechanism that produces useful currents in a solar cell or photodiode. These currents decay typically within hundreds of nanoseconds after a radiation pulse.

The surface effect of ionization can be very stable. The mechanisms producing this type of damage are the generation, migration and accumulation of charges on, in, and near the surface of a semiconductor chip. These charges affect the electrical behavior of the semiconductor device.

2.2 SEMICONDUCTOR TERMINOLOGY

An attempt has been made in this handbook to present prediction techniques in a manner that requires a minimum understanding of semiconductor device technology. Intelligent application of the data, however, does require a knowledge of semiconductor nomenclature and the general electrical behavior of semiconductor devices. A number of excellent texts are available[1,2,3,4] that present the basic semiconductor concepts and device relationships. These references should be used when further discussion is required on semiconductor device technology.

The three important characteristics of semiconductors that the electronics designer can profitably review are impurities, carriers and generation and recombination of carriers.

The impurities added to pure silicon to make it into a semiconductor material are either acceptors $N_A(cm^{-3})$ (usually boron) or donors $N_D(cm^{-3})$ (usually phosphorus). The general term "dopant" refers to the impurity atoms deliberately added to make silicon a semiconductor material. The term carriers refers to electrons $n(cm^{-3})$ or holes $p(cm^{-3})$ that can carry charge. Thus the terms dopant impurity, acceptor and donor apply to atoms, which are fixed in position; while the terms carriers, holes and electrons apply to carriers of electrical charge, which are mobile. Each impurity atom added to silicon provides one free charge carrier. Boron-doped silicon has a preponderance of carriers that are holes and is designated as p-type silicon. Phosphorus doped silicon has a large number of electrons and is called n-type silicon.

Carriers are called either minority carriers or majority carriers. For boron-doped p-type material with a large number of holes, the holes are the majority carriers and the electrons are the minority carriers. For phosophorus-doped n-type silicon, the electrons are the majority carriers and the holes are the minority carriers.

The equilibrium minority carrier concentration is very small. When additional minority carriers are present, usually by flow across a junction between n-type and p-type regions of a device, they recombine with the majority carriers to reduce the concentration. If the minority carrier concentration is suddenly increased and allowed to decay, the carrier concentration will be reduced as exp $(-t/\tau)$ where t is time and τ is the minority carrier lifetime. At time $t = \tau$ the number of minority carriers has decayed to 1/e of the initial concentration.

The term used to describe the relative carrier concentration is "injection level," which is the ratio of the minority carrier concentration Δn (carriers/cm^3) to the doping level N_o(atoms/cm^3) or $\Delta n/N_o$. The symbol Δn is the excess minority carriers over and above the very small thermal equilibrium value, and N_o is the impurity level or doping concentration. Although the excess holes in n-type silicon are designated Δp, the symbol $\Delta n/N_o$ represents either $\Delta n/N_A$ or $\Delta p/N_D$.

Neutron and gamma radiations introduce defects into the silicon material which reduce the minority carrier lifetime and the apparent impurity concentration as a function of the radiation. These two physical parameters are discussed in the following two sections. A third physical parameter called carrier mobility is also changed, but its change is assumed to be negligible.

2.3 CHANGES IN MINORITY CARRIER LIFETIME

The minority carrier lifetime is reduced by the defects introduced by the radiation. The change in the reciprocal lifetime R or recombination rate is directly proportional to the radiation exposure

$$R = R_o + K_\tau \phi \tag{2-1}$$

or

$$\frac{1}{\tau} = \frac{1}{\tau_o} + K_\tau \phi \tag{2-2}$$

where

R = post irradiation recombination rate, s^{-1}

R_o = pre irradiation recombination rate, s^{-1}

K_τ = minority carrier lifetime radiation damage factor, $cm^2/n\text{-}s$

ϕ = neutron exposure, n/cm^2

τ = post irradiation minority carrier lifetime, s

τ_o = pre irradiation minority carrier lifetime, s

Some authors prefer to express equation (2-2) as

$$\frac{1}{\tau} = \frac{1}{\tau_o} + \frac{\phi}{K'_\tau} \qquad (2\text{-}3)$$

where K'_τ is simply the reciprocal of K_τ.

Some authors also prefer to use the terminology, "radiation damage constant," for K_τ rather than radiation damage factor. We recommend the use of radiation damage factor, as K_τ is not really a constant but is a function of a number of parameters. Most important of these fuactional depependencies are the energy of the neutron radiation, the temperature, the impurity concentration N, and the injection level ratio $\Delta n/N$.

The neutron energy dependence of neutron damage is discussed in Section 2.5. Temperature is important both during the radiation exposure, when the defects are formed, and in subsequent modification and annealing behavior of the defects. Some of the characteristics to be expected are discussed in Section 2.6.

The impurity concentration dependence refers to the variation of K_τ with the concentration of the dopant atoms N_o in the silicon. The injection level dependence refers to the variation of K_τ with the injection level $\Delta n/N_o$. Both of these are shown qualitatively in Figure 2-1, in which a number of curves are sketched between experimental end points. The low injection level data $\Delta n/N_o = 10^{-4}$ are from a mean curve drawn through O. L. Curtis's data.[5] The high injection data are from calculations by Messenger[6] and from experiments by Frank.[7] Experimental data for a 2N1613 transistor were used as a midpoint reference.[8] The designer should note that the injection level is a function of the emitter current density and that increasing operating current densities result in a lower radiation damage coefficient.

In the actual prediction of device behavior, detailed knowledge of the radiation damage coefficient K_τ as a function of both impurity and carrier concentrations, as illustrated in Figure 2-1, might be used directly. This information, however, is quite difficult to obtain experimentally and there are a number of problems associated with determining the device impurity and carrier concentrations and in considering second-order effects. In practice, a composite radiation damage coefficient K is obtained from device behavior as a function of the current density in the device. Predictions are made ignoring the dependence of the damage coefficient on impurity concentration and using current density as the variable that accounts for the variation with carrier concentration. Even though the basic silicon material behavior is not used directly in device predictions, examination of the available data presented in Figure 2-1 is helpful in understanding why silicon devices degrade in neutron radiation as they do.

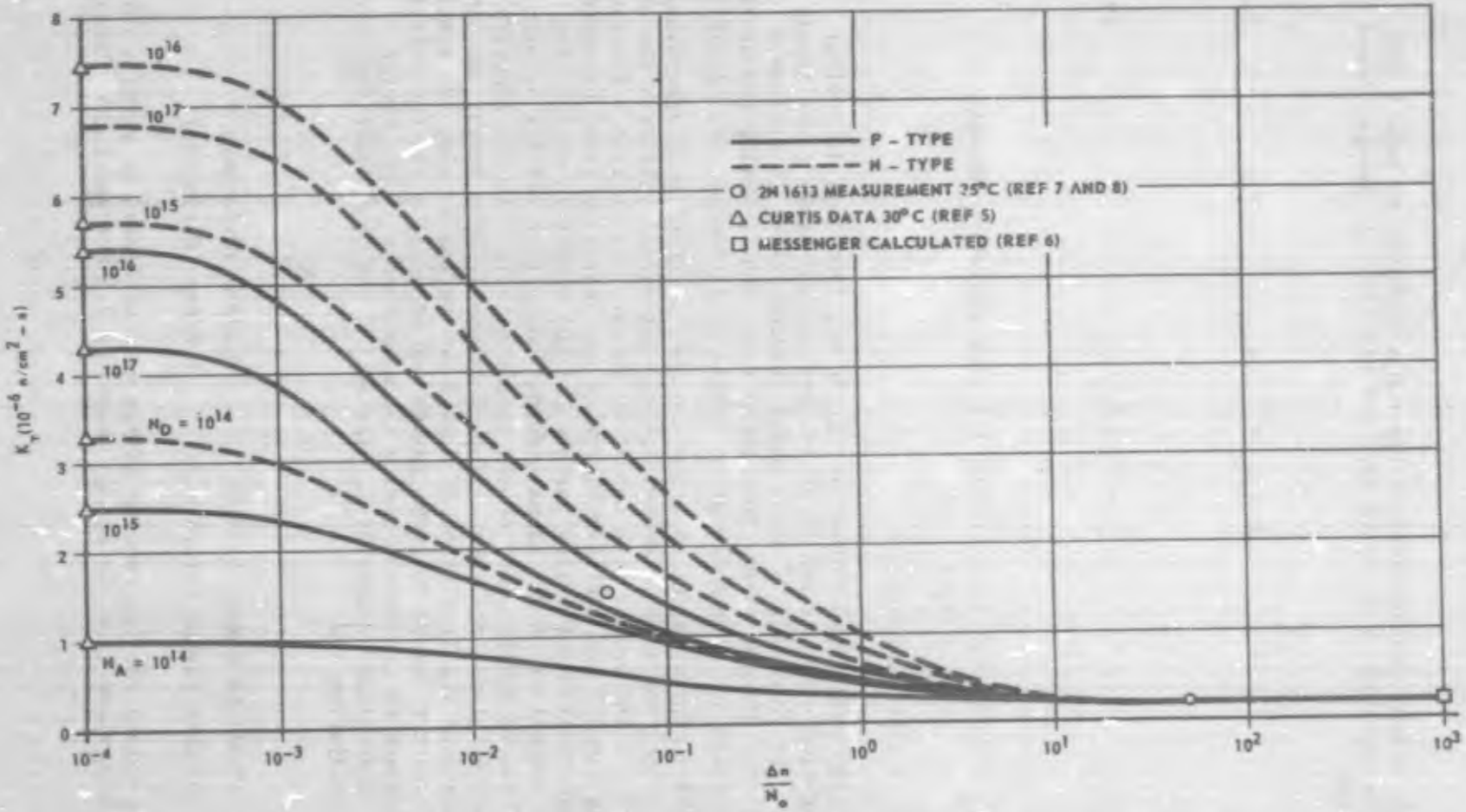

Figure 2-1. Estimated injection level behavior of the radiation damage coefficient K_τ for silicon

The linear proportionality between recombination rate R and radiation exposure ϕ is valid also for displacement damage caused by gamma rays.

$$R = R_o + K_{\tau\gamma}\,\phi_\gamma \tag{2-4}$$

or

$$\frac{1}{\tau} = \frac{1}{\tau_o} + K_{\tau\gamma}\,\phi_\gamma \tag{2-5}$$

where

$K_{\tau\gamma}$ = gamma minority carrier lifetime radiation damage factor, $R^{-1}s^{-1}$

ϕ_γ = gamma exposure, R

Though gamma displacement damage is not important in nuclear weapon environments, it can be in nuclear reactor space power applications. The shielding of space power reactors tends to attenuate neutrons to a greater extent than gamma rays, thus reducing the neutron-to-gamma ratio and making the gamma displacement damage more significant.

Like K_τ for neutrons, $K_{\tau\gamma}$ has a number of functional dependencies. It is a strong function of energy, which partially invalidates the simulation of reactor gammas with Cobalt-60 gammas. It is also a function of doping level N but exhibits little if any injection level dependence. The damage coefficient varies between silicon materials of the same impurity concentration for gamma-induced damage (but not for neutron damage), due to interactions of the simple defects with the impurity atoms, oxygen atoms, and crystal imperfections. These variations limit the accuracy of the prediction of damage due to gamma rays. No single ratio of neutron damage to gamma damage can be used, since the relative damage depends on conditions during the measurement of the damage effect. Approximate values of $K_{\tau\gamma}$ for 40.5°C and no carrier injection during irradiation are

	$K_{\tau\gamma}$
Cobalt-60 gammas (1 MeV)	0.2/R-s (reference 9)
Reactor gammas (2.5 MeV)	1.0/R-s (estimated)

The values for the reactor gammas were estimated by using a ratio of 5 as determined from the damage caused by 2.5 MeV and 1 MeV electrons.[10]

2.4 CHANGES IN IMPURITY CONCENTRATION

When a neutron creates a defect cluster in silicon, the cluster can function as either acceptor or donor atoms. In p-type material the cluster behaves as a donor, and reduces the effective impurity concentration. This causes an increase in the resistivity of the silicon. In n-type material, the cluster acts as an acceptor, which reduces the number of electrons available for conduction and again causes an increase in resistivity. This effect is most important in lightly doped silicon where the fractional change in the impurity concentration can be large.

In the prediction procedures described in later sections, the change in the impurity concentration is formulated as

$$\Delta N = N_o - K_N \phi \qquad (2\text{-}6)$$

where K_N is the carrier removal coefficient (n^{-1} cm^{-1}). To obtain the correct values for device behavior, a value of K_N of about 1.3/n-cm is recommended for all impurity concentrations N_O for predicting changes in bulk material resistivity. Smaller values are recommended, as presented in Section 6.3, for predicting junction breakdown voltage, which also depends on impurity concentration.

The recommended values of K_N are smaller than those obtained by Stein[11,12] and Curtis, Bass, and Germano[13] in experiments on bulk silicon material. The values of these investigations range from 1 to 4 carriers/n-cm (Curtis et al) to 4 to 15 carriers/n-cm (Stein), increasing as a function of increasing impurity concentrations. Application of the data reported in the literature yields semiconductor device parameter changes larger than experimentally observed.

2.5 ENERGY DEPENDENCE OF NEUTRON DAMAGE

As mentioned earlier, the amount of displacement damage which results from neutron radiation is a function of the energy of the neutron. Figure 2-2 taken from Smith et al[14] shows the characteristics of the energy damage dependence. The curve is the computed energy deposited from elastic scattering of the neutrons compared with discrete experimental data points for carrier removal from Cleland, Bass, and Crawford.[15] There are no comparable experimental data for the energy dependence of carrier lifetime damage; therefore the dependence of K_τ is assumed to be the same as the dependence of K_N, which closely follows the analytical energy deposited curve.

Smits[17] has made a very useful comparison of the damage ratio of 14 MeV neutrons with the damage resulting from the near fission energy spectrum at the Sandia Pulsed Reactor. The Sandia Pulsed Reactor is identical in structure to the White Sands Fast Burst Reactor. Smits

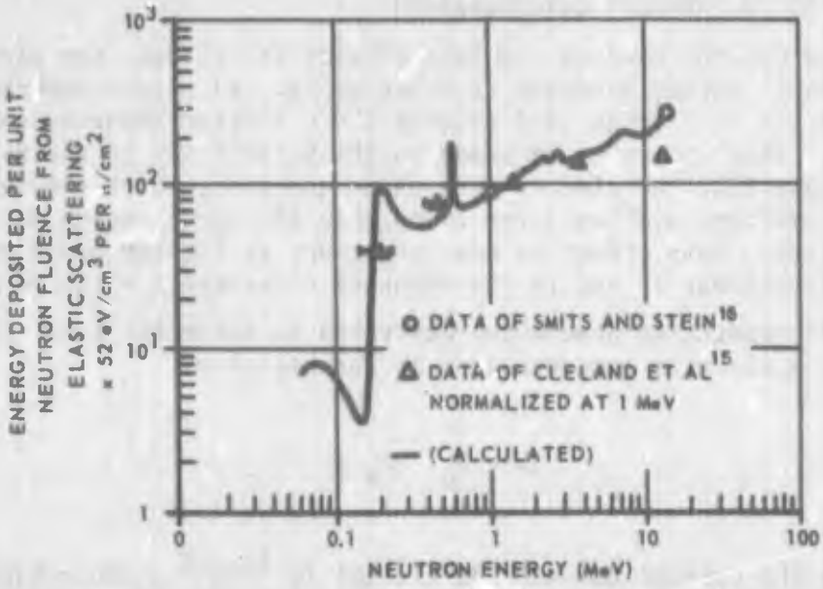

Figure 2-2. Computed and experimental energy deposition in silicon from neutrons (source: Reference 14)

obtained damage ratios of 3.4 for carrier lifetime changes in transistors, 2.2 for carrier lifetime changes in solar cells, and 3.0 for carrier removal in moderately doped bulk silicon. He concludes that for most engineering purposes the damage ratio of 14 MeV neutrons to the near fission spectrum from a pulsed reactor can be taken as 3 ± 1. This means that for an environment spectrum of 50 percent fission neutrons and 50 percent 14 MeV neutrons the damage would be, at most, 2.5 times as damaging as a pulsed reactor environment ($1/2 \times 1 + 1/2 \times 4$).

The data and predictions given in this handbook are based on the damage from neutron spectra of pulsed reactors such as the White Sands Fast Burst Reactor and the Sandia Pulsed Reactor. The pulsed reactor spectrum neutron is about 20 percent less damaging than a Watts fission spectrum neutron. Any other spectrum can be converted to an equivalent FBR spectrum by using the function F(E) in Figure 2-3 derived from Figure 2-2. The function F(E) is normalized so that

$$\int_0^\infty F(E)\, N_{FBR}(E)\, dE = 1 \qquad (2\text{-}7)$$

where $N_{FBR}(E)$ is the normalized FBR differential energy spectrum also shown in Figure 2-3. Any neutron spectrum $\phi_x(E)$ can be converted to an equivalent FBR spectrum by the integration

$$\phi(FBR) = \int_0^\infty F(E)\, \phi_x(E)\, dE \qquad (2\text{-}8)$$

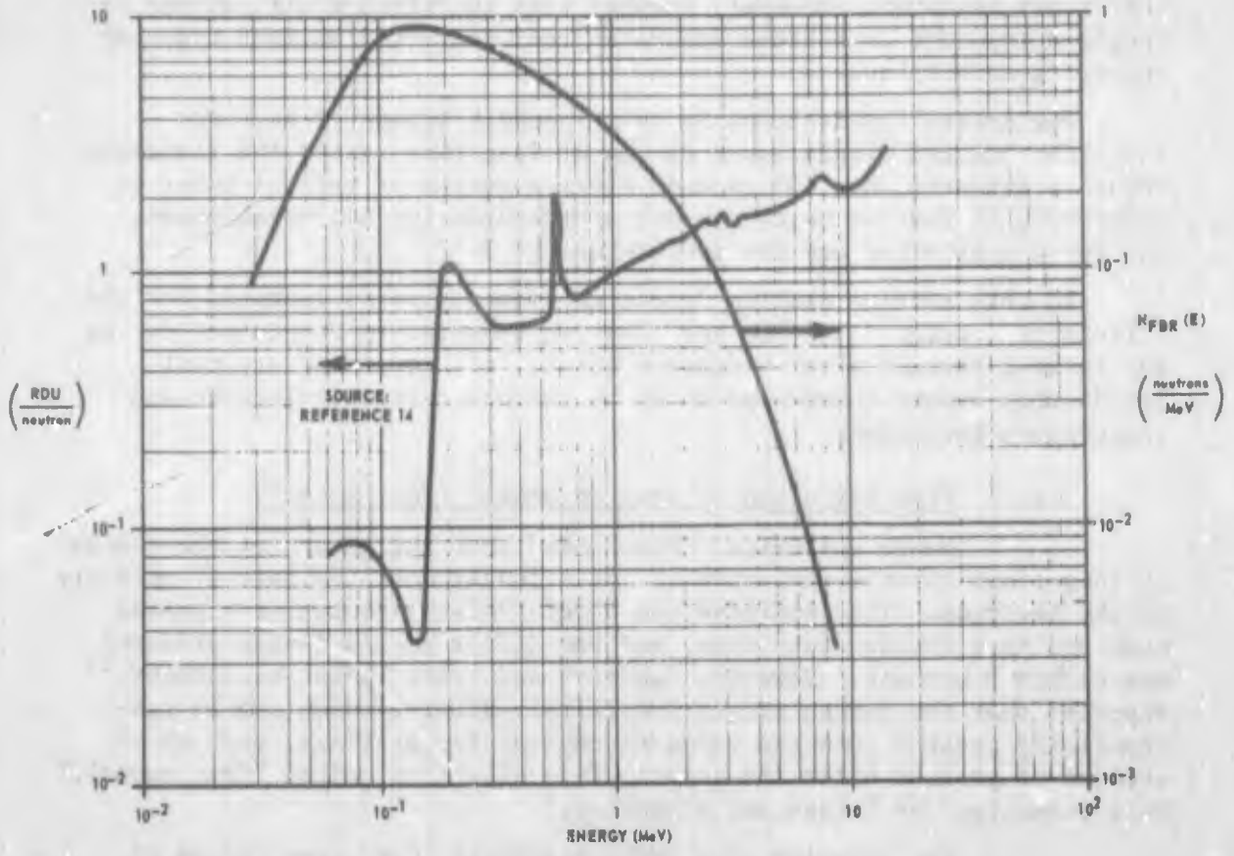

Figure 2-3. The White Sands Fast Burst Reactor reference spectrum and the neutron energy dependence of silicon damage

2.6 DEFECT MODIFICATION

Radiation-induced defects in semiconductor materials are not permanently entrenched lattice changes that can never be altered. On the contrary, they can be removed by thermal annealing to restore the original lattice structure, or reordered to change the defect structure and its effectiveness as a recombination center. The defects are influenced during irradiation or at the time of formation by temperature and carrier injection and, after irradiation, by shelf storage, temperatures above room temperature, and by the injection of carriers, e.g., normal operating currents.

At the present time the effects of defect modification cannot be accurately predicted. The general phenomenon is described in this section to provide the electronics designer with background information so that he will recognize when errors in prediction can be caused by

defect modification and be able to estimate roughly the magnitude of the errors involved. However, further work in defect modifications is required in order to achieve accurate predictions for various types of operating conditions.

The general predictions in this handbook apply for neutron-radiation-induced displacement damage at long times after the radiation exposure (greater than 10^4 seconds after a weapon or reactor burst of neutrons), to devices which are not operated during the irradiation, and for a controlled ambient temperature of 35°C.

In this section neutron damage in transistors is examined for the effects of carrier injection and elevated temperature maintained during and several seconds after a neutron burst. Also examined are post-irradiation damage changes produced by various carrier injection and temperature treatments.

2.6.1 Time Variation of Neutron Damage (Fast Anneal)

Moore and Smits[19] have shown that the amount of the damage at long times after irradiation is not a function of the rate of delivery of the neutrons. They operated the Sandia Pulsed Reactor in a pulsed mode and in a steady state mode, and the difference in damage produced was within 5 percent. However, Sander[20] and later Sander and Gregory[21] reported that the damage effect immediately after a burst can be substantially greater than the value reached at longer times, such as 10^4 seconds or greater after the burst. This effect is called "fast anneal," "beta annealing" or "transient annealing."

The behavior of a 2N914 transistor over many orders of magnitude in time, reported by Sander and Gregory, is shown in Figure 2-4 for four different temperatures. The relative damage is given in terms of an "annealing factor," for a damage effect that is proportional to the radiation exposure. The annealing factor is defined by

$$\text{Annealing factor} = \frac{\phi^*(t)}{\phi} = \frac{D(t)}{D(t=\infty)} = \frac{\frac{1}{h_{fe}(t)} - \frac{1}{h_{feo}}}{\frac{1}{h_{fe}(t=\infty)} - \frac{1}{h_{feo}}} \qquad (2\text{-}9)$$

where ϕ is the radiation exposure (n/cm^2) and $\phi^*(t)$ is the effective radiation exposure (n/cm^2) from a slow neutron rate source that produces the same damage as that obtained at time t immediately following a nuclear burst. D is the damage effect and $1/h_{fe}$ is the reciprocal small signal common emitter current gain.

Two conclusions can be drawn from Figure 2-4. First, for the temperatures of interest ($T \geq 27°C$), temperature is not an important parameter in the magnitude of the damage correction required at short

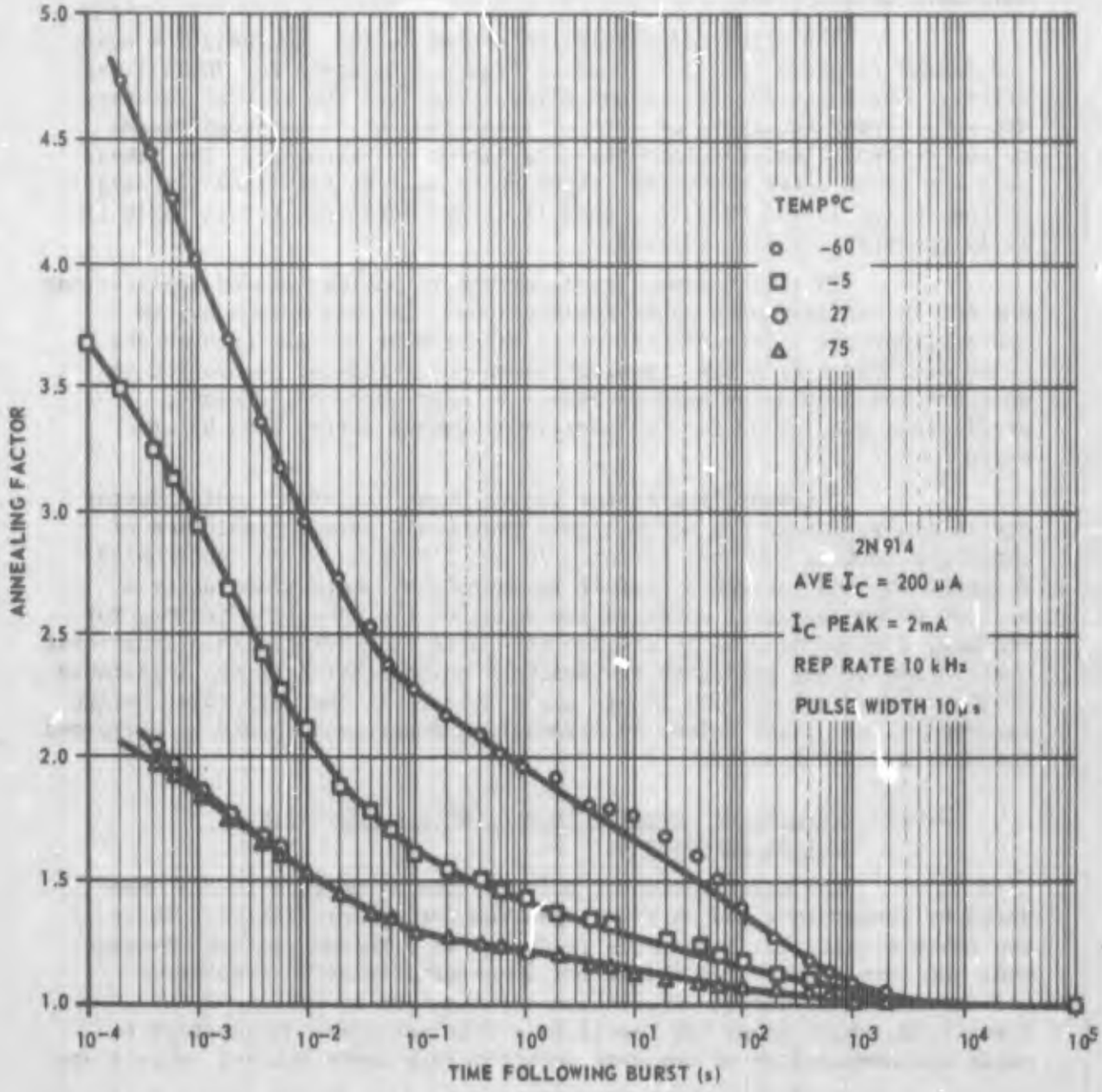

Figure 2-4. Curves of annealing factor versus time following a neutron burst exposure of a 2N914 transistor (average current density 2.5 A/cm^2) at four temperatures (source: Reference 21)

times after the nuclear burst. Secondly, large errors in prediction at short times result if the effect of fast or transient annealing is not taken into account.

The effect of carrier injection during the radiation pulse and damage recovery is illustrated in Figure 2-5, again for 2N914 transistors. The magnitude of the annealing factor and the rate of recovery are very strong functions of carrier injection, which is proportional to the current flowing during the irradiation and recovery. The damage at short times after a nuclear weapon burst will be significantly larger if the device is not operating than if it is operating, particularly if it is operating at high currents.

This fast anneal is important in nuclear weapon applications but not in nuclear space power applications. In some weapon system applications the electronic circuitry either must operate through the pulse or recover from the transient-gamma-pulse-induced saturation to an operation mode as quickly as possible. For such applications, predictions must allow for the additional damage during this brief period.

The annealing factor varies among different semiconductor device types, but so far correlations that would permit prediction of annealing factors have not appeared in the literature. An electronics designer who must design a circuit to operate at short times after a neutron pulse can use a conservative value of the annealing factor, for example, a value of 3 at 10 milliseconds after the burst. This additional degradation factor will give the designer an indication of the importance of the fast anneal problem in his application. If the particular design is marginal with this value, an irradiation experiment should be performed for more precise results.

2.6.2 Effects of Temperature and Carrier Injection During Irradiation

The modification of defects considered next is that produced by temperature and carrier injection during irradiation. These can cause significant reductions in damage in a pulsed neutron environment and even greater reductions for long-term radiation exposures. Carrier injection during irradiation results from operation of the transistor, which alone may result in sufficient power dissipation to raise the temperature of the semiconductor chip above ambient temperature.

Table 2-1 shows the importance of device operation during pulsed irradiation.[22] Measurements were made prior to and long after exposure in the White Sands Fast Burst Reactor at the conditions shown. Power was removed from the transistors several seconds after the reactor burst so that little post-irradiation annealing occurred. The average reduction in damage produced by current alone was 20 percent; by current plus voltage, 25 percent.

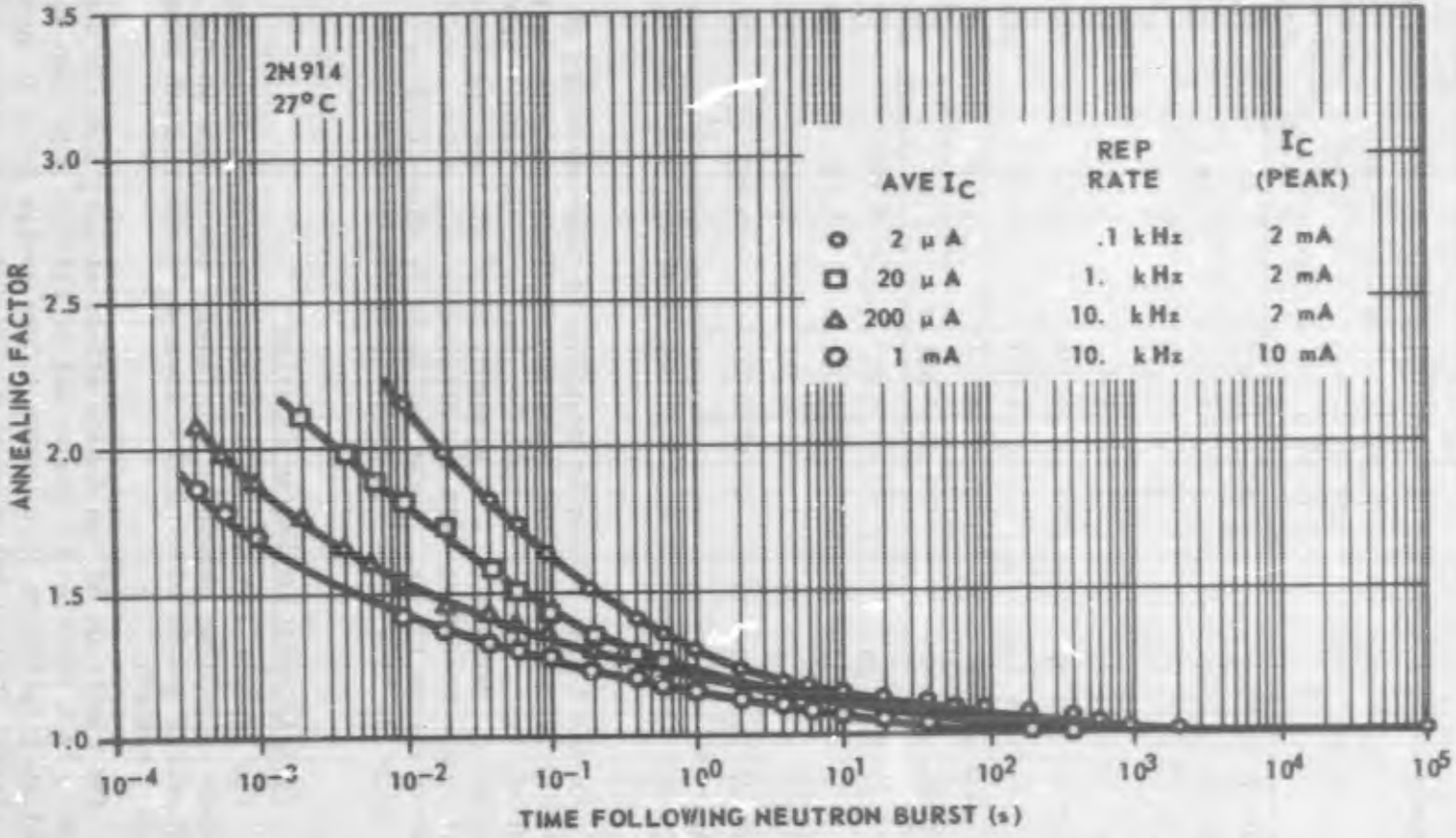

Figure 2-5. Curves of annealing factor versus time for a 2N914 transistor at 27°C comparing different injection levels for the same temperature (source: Reference 21)

Table 2-1. Effect of operating conditions during irradiation

Device	Operating conditions	$\Delta\left(\frac{10^3}{h_{FE}}\right)$	t (ns)	$K = \frac{1}{t\phi}\Delta\left(\frac{1}{h_{FE}}\right)$ $(10^{-6}\ cm^2/n\text{-}s)$	Junction temperature (°C)
2N1613-1	Terminals open	169.4	1.490	1.61	25
2N1613-2	Terminals open	161.0	1.353	1.69	25
2N1613-3	I_C = 100 mA, V_{CB} = 0	112.7	1.199	1.33	42
2N1613-4	I_C = 100 mA, V_{CB} = 0	112.1	1.127	1.41	42
2N1613-5	I_C = 100 mA, V_{CB} = 6V	122.4	1.274	1.36	175
2N1613-6	I_C = 100 mA, V_{CB} = 6v	124.2	1.392	1.27	175
2N914-7	Terminals open	30.3	0.376	1.19	25
2N914-8	Terminals open	30.8	0.381	1.15	25
2N914-9	I_C = 25 mA, V_{CB} = 0	23.19	0.363	0.906	35
2N914-10	I_C = 25 mA, V_{CB} = 0	23.98	0.369	0.922	35
2N914-11	I_C = 25 mA, V_{CB} = 12 V	18.89	0.308	0.869	175
2N914-12	I_C = 25 mA, V_{CB} = 12 V	19.88	0.337	0.837	175

Measurement conditions: T = 35°C, V_{CB} = 5V, I_E = 10 mA

In the future it may be possible to take advantage of the lower damage effects resulting from operation of the transistor during the radiation exposure, after this behavior has been thoroughly studied and is predictable. Meanwhile it is probably wiser to base the design on the larger damage resulting from the assumption of passive irradiation. If this estimate causes the particular design to be classified as marginal, a radiation test under the exact operating conditions is recommended.

2.6.3 Post Irradiation Damage Behavior

Two aspects of the post-irradiation behavior of neutron radiation damage to silicon should be mentioned: the change in the device damage effect due to electrical measurements and thermal annealing of the radiation damage.

The magnitude of the damage effect at long times after a neutron exposure is a function of the amount of carrier injection at constant junction temperature that occurs in the device prior to measurement of the damage. Typical behavior of the reciprocal dc gain (I_B/I_C)

of a 2N1613 transistor is shown in Table 2-2.[8] The damage effect increases with successive measurements and is restored by several days' storage at room temperature without operation. The effect depends on the magnitude of current (or carrier concentration) during the measurements; this is evidenced by small increases in the last three readings when the currents were limited to 10mA. Increases of about 15 percent have been observed for large injected currents maintained for 5 minutes with the semiconductor chip at 40°C. This behavior is illustrated in Table 2-3 for 5, 15, and 30 minutes of current injection. The cause of this phenomenon is either a reordering of the defects or carrier trapping. In trapping, the carriers are captured in a defect and held for a short period of time during which they are not available to carry current.

In making post-irradiation measurements care must be exercised to avoid comparing results between devices which have been measured differently. Until additional work has been done to clarify this effect, the electronics designer working with devices on which post-irradiation measurements have been made should account for this effect by assuming an additional factor of 1.15 degradation.

Two illustrations of post-irradiation temperature annealing are presented in Figures 2-6 and 2-7 to illustrate the general effect. Figure 2-6 is a plot of the constant temperature damage annealing of a 2N1613 transistor irradiated at the White Sands Fast Burst Reactor.[23] After 30 minutes at 310°C, the damage, which was measured several times at 35°C, had reached a residual plateau where about 80 percent had annealed and about 20 percent remained. Note the high early annealing rate, revealed by the fact that almost 60 percent of the damage had annealed in the first 5 minutes at 310°C.

Isochronal annealing data are shown in Figure 2-7. Temperatures of over 220°C are required in order to reduce the damage effect by a factor 2. Figures 2-6 and 2-7 indicate that the large displacement damage predicted for many power transistors may be smaller in actual operation because of annealing from operation at high temperatures. Again, lower damage rates should be used with caution as this regime has not been studied carefully. This is especially important if the circuit must operate within milliseconds after a nuclear weapon burst.

Table 2-2. $10^3\ h_{FE}^{-1}$ post irradiation variations with time, transistor 2N1613-6, V_{CB} = 5V, T = 35°C

DATE	CYCLE	COLLECTOR CURRENT (amperes)					
		10^{-1}	10^{-2}	10^{-3}	10^{-4}	10^{-5}	10^{-6}
		$10^3/h_{FE}$					
2-22	No. 1	186.3	264.6	536.3	1000	1740	3192
	No. 2	188.0	287.1	561.4	1012	1753	3203
	No. 3	188.9	290.4	566.4	1015	1754	3208
	No. 4	189.2	294.4	568.5	1008	1741	3192
2-23		187.9	281.4	561.4	1018	1756	3208
2-24		187.7	284.3	562.9	1017	1754	3194
2-28		--	268.6	537.3	977.8	1689	3072
3-8	No. 1	181.6	261.3	517.2	932.9	1603	2900
	No. 2	184.1	281.9	541.4	949.6	1626	2929
3-14	No. 1 AM	181.6	262.9	523.3	945.4	1624	2933
	No. 2 PM	183.5	282.0	544.3	959.7	1639	2966
4-6		179.4	257.4	509.8	914.9	1557	2780
4-22	No. 1	179.6	257.7	510.2	916.4	1561	2785
	No. 2	182.8	281.9	539.3	940.8	1595	2871
	No. 3	183.7	284.5	543.9	946.8	1604	2892
	No. 4	184.3	286.1	547.2	950.7	1611	2910
4-27	No. 1	--	261.5	518.2	927.5	1583	2810
	No. 2	--	265.4	521.4	926.9	1577	2841
	No. 3	--	267.2	523.7	928.0	1580	2840

Table 2-3. Effect of current injection on post irradiation gain and leakage current measurements

Measurement I_C(A) (V_{CB} = 5V, T = 35°C)	$10^3\ h_{FE}^{-1}$ Before current injection	$10^3\ h_{FE}^{-1}$ After current injection (I_E = 100 mA, V_{CB} = 0)		
Time		5 min	15 min	30 min
Column Nos.	3	4	5	6
10^{-7}	7428	8316	7809	7389
10^{-6}	3943	4309	4066	3864
10^{-5}	2250	2441	2322	2222
10^{-4}	1333	1480	1422	1374
10^{-3}	733	853.6	829.0	808.7
10^{-2}	371.1	421.2	408.5	378.6
	I_{CBO}(nA) at V_{CBO} = 5V, T = 35°C			
	13.65	16.5	16.6	15.2

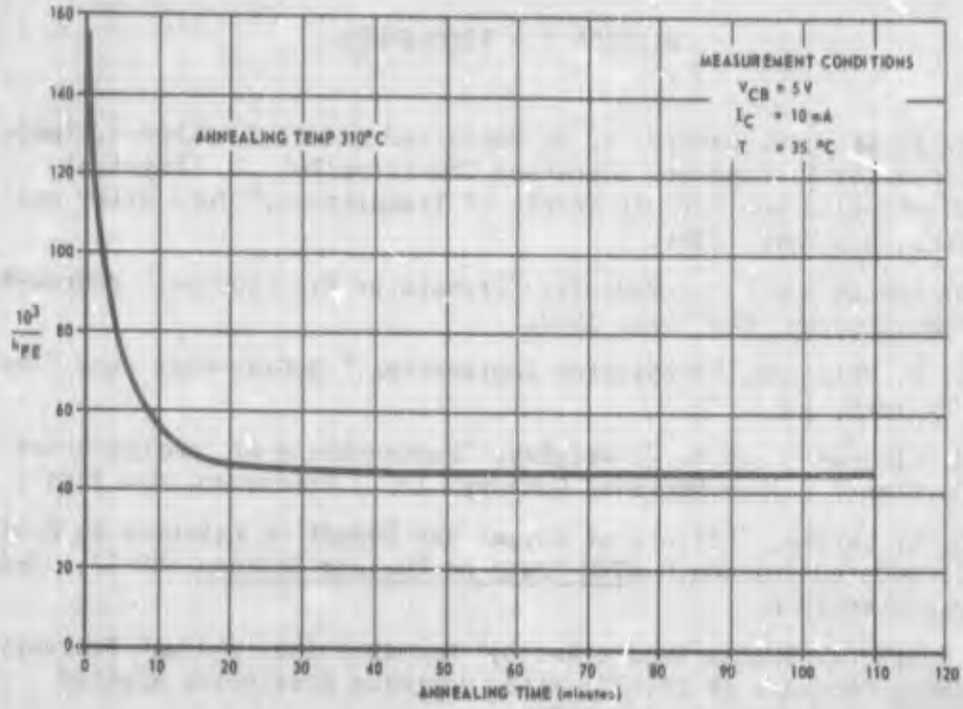

Figure 2-6. Constant temperature annealing of an irradiated 2N1613 transistor

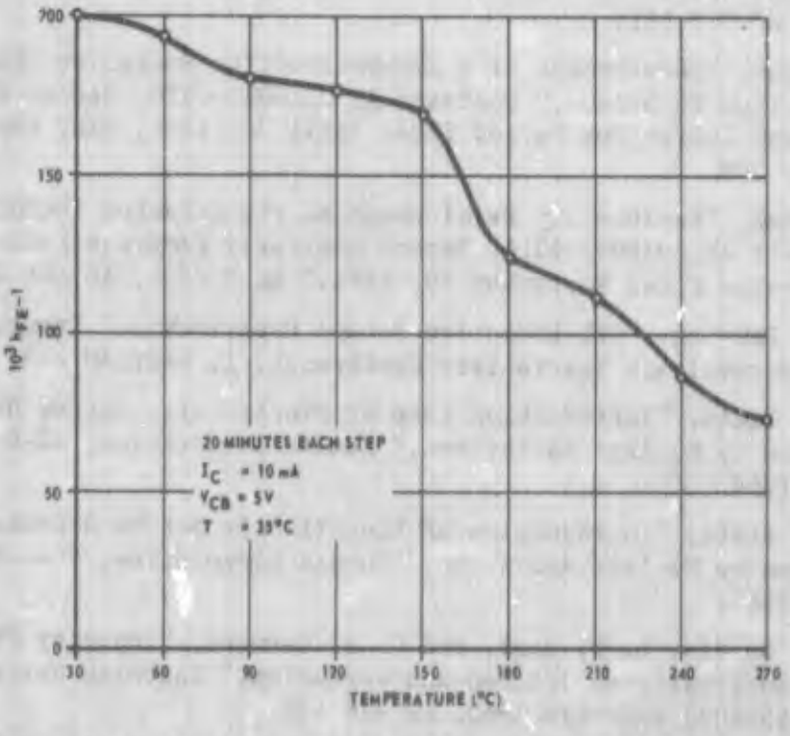

Figure 2-7. Isochronal annealing of a 2N1613 transistor

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SECTION 3

SPECIFICATION OF DISPLACEMENT RADIATION DAMAGE EXPOSURE

This section discusses the use of specially calibrated transistors called Radiation Damage Monitors (RDMs) to measure radiation exposure in Radiation Damage Units (RDUs).

3.1 DEFINITION OF RADIATION DAMAGE UNIT (RDU)

The nature of the neutron radiation environment as a function of neutron energy was discussed in Section 1.1, and the present knowledge of the damaging effect of neutrons of various energies was outlined in Section 2.5. The total damage caused by a neutron environment is given by the integral

$$\text{Total Damage} = \int_0^E \phi(E)\ D(E)\ dE \qquad (3\text{-}1)$$

where

$\phi(E)$ is the number of neutrons of energy E

D(E) is the amount of damage caused by each neutron of energy E

A deficiency which impedes radiation damage studies, and therefore prediction and the evaluation of the results of prediction, is the lack of a good measurement of $\phi(E)$ and F(E). Neutron radiation exposures are usually measured by activiation foils, i.e., by counting the activity in a material exposed to the radiation. Frequently the exposure is simply given as, for example, 10^{13} neutrons per cm^2 or 10^{13} nvt of energy greater than 0.1 MeV. As discussed in Section 2.5, if all these neutrons are 14 MeV, the damage is about 3 times greater than it would be for the 1.05 MeV average energy of a bare pulsed reactor. Or, if all the neutrons are thermal neutrons there is essentially no damage. Thus the number of incident neutrons does not adequately describe the exposure.

To be truly meaningful, a neutron radiation specification should include both the neutron number and a value of its damaging effect. A way of accomplishing this was proposed independently by Frank Larin of Bendix[1] and A. D. Rossin of Argonne National Laboratory.[2] Both recommended the conversion of damage rates in different neutron spectrum environments to a common damage in a reference neutron spectrum. In addition, Rossin proposed a measurement unit for radiation exposure, which he called a Radiation Damage Unit or RDU; and he suggested a neutron fission spectrum as the reference spectrum. In general, the RDU may be defined as that quantity of neutron radiation which produces the same amount of damage

in a particular material as one reference spectrum neutron/cm^2.

By definition,

$$\frac{D_r}{\phi_r} = \frac{D_x}{F_x \phi_x} = \frac{D_x}{RDU_x} \qquad (3\text{-}2)$$

where

D = damage

F = neutron spectrum correlation factor

and subscript r refers to reference and x to unknown. A damage rate in an unknown environment D_x/ϕ_x can be converted to a damage rate in a reference spectrum D_r/ϕ_r using equation (3-2). The product $F_x\phi_x$ or RDU for silicon can be determined if ϕ_x and its energy distribution are accurately measured and F_x is calculated from the two spectra and the neutron energy dependence of silicon damage. An estimate of this integration can be made from equation (2-7) and the data in Figure 2-3.

A simpler procedure is to define a reference spectrum and to use a linear damage effect in silicon to determine in RDU the exposure of other experiments using

$$RDU_x = \frac{D_x}{D_r/\phi_r} \qquad (3\text{-}3)$$

In this technique, a device is calibrated in terms of the reference spectrum by determining D_r/ϕ_r by an irradiation in the reference spectrum or by making electrical measurements of the device and predicting the calibration D_r/ϕ_r.

The constants and data given in RDU in this handbook are referenced to a particular location in the White Sands Fast Burst Reactor. The neutron spectrum for this location is approximately a fission energy spectrum as shown in Figure 1-1. (1 RDU = 0.8 n/cm^2 fission spectrum).

3.2 IMPLEMENTATION OF RDU MEASUREMENT

Equation (2-5) in Section 2 indicates that the minority carrier lifetime relationship

$$\frac{1}{\tau} = \frac{1}{\tau_o} + K_\tau \phi \qquad (3\text{-}4)$$

can be used to measure silicon damage in RDU because its reciprocal is linear with radiation exposure. Changes in lifetime can be measured in bulk semiconductor materials, or semiconductor device parameters proportional to carrier lifetime can be measured and the lifetime changes inferred from these measurements. Two transistor parameters are linearly proportional to lifetime over part of their operating range. These are reciprocal gain h_{FE}^{-1} and transistor base-collector junction leakage current I_{CBO}. The equations are respectively

$$\frac{1}{h_{FE}} = \frac{1}{h_{FE}(0)} + t\,K\,\phi \qquad (3\text{-}5)$$

and

$$I_{CBO} = I_{CBO}(0) + k\,K_{rg}\phi \qquad (3\text{-}6)$$

where

h_{FE} = transistor gain

t = transistor base transit time, s

K = empirical damage factor, $s^{-1}RDU^{-1}$

ϕ = radiation exposure RDU

and

I_{CBO} = collector-base junction leakage current, A

k = constant proportional to the volume of the base-collector junction depletion region, A-s

K_{rg} = radiation damage coefficient for carrier lifetime in the base collector junction depletion region, s^{-1} RDU^{-1}

The parenthetical zero refers to the preirradiation measurements. Examples of the application of these equations and a description and measurement of each term are given in Section 5.1 for gain and Section 6.5 for leakage current.

Although leakage current is linear with neutron exposure, it is a difficult parameter to measure and not recommended except for estimating purposes as a last resort. Therefore it is not further discussed.

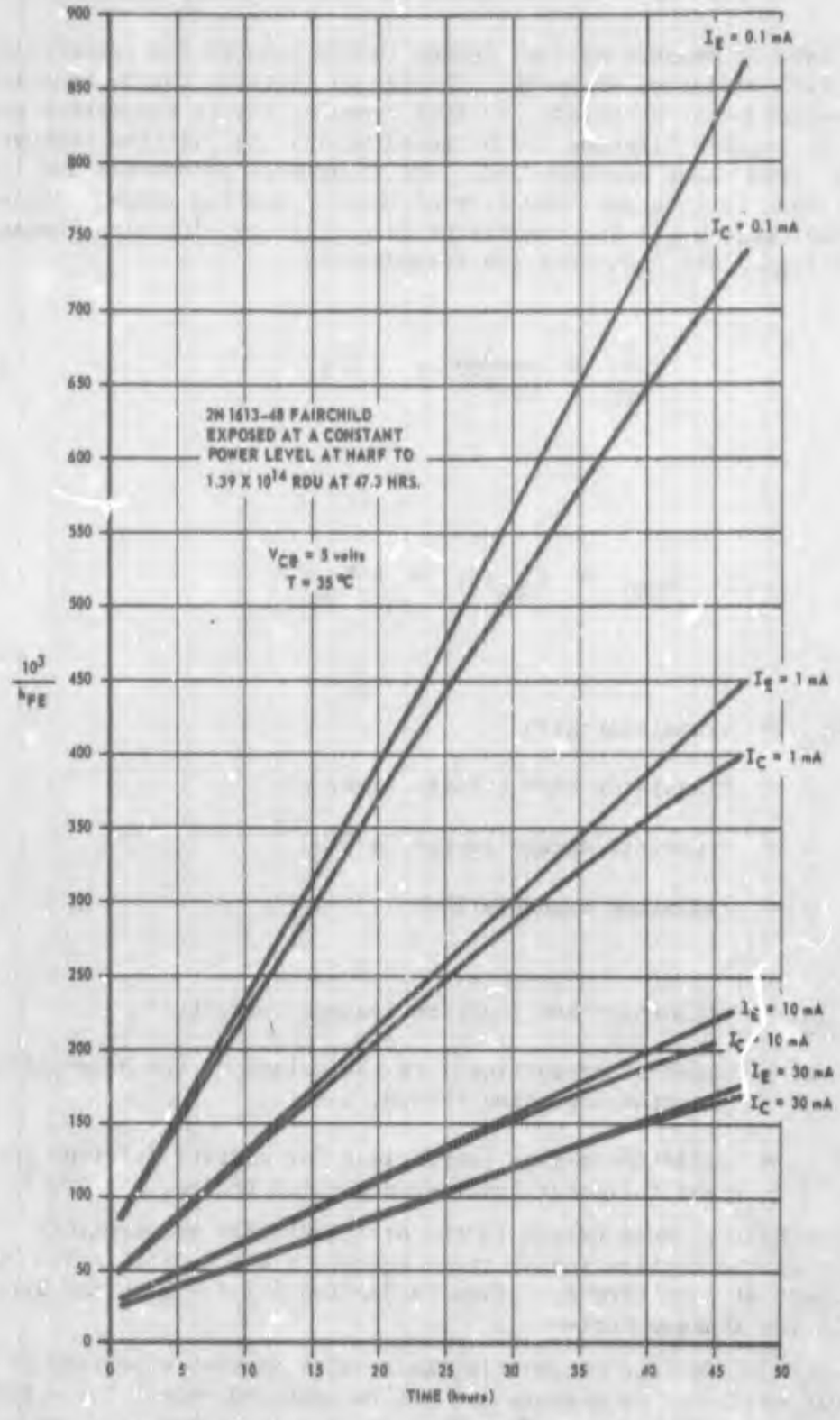

Figure 3-1. Linearity comparison of I_E and I_C for reciprocal gain as a function of neutron fluence

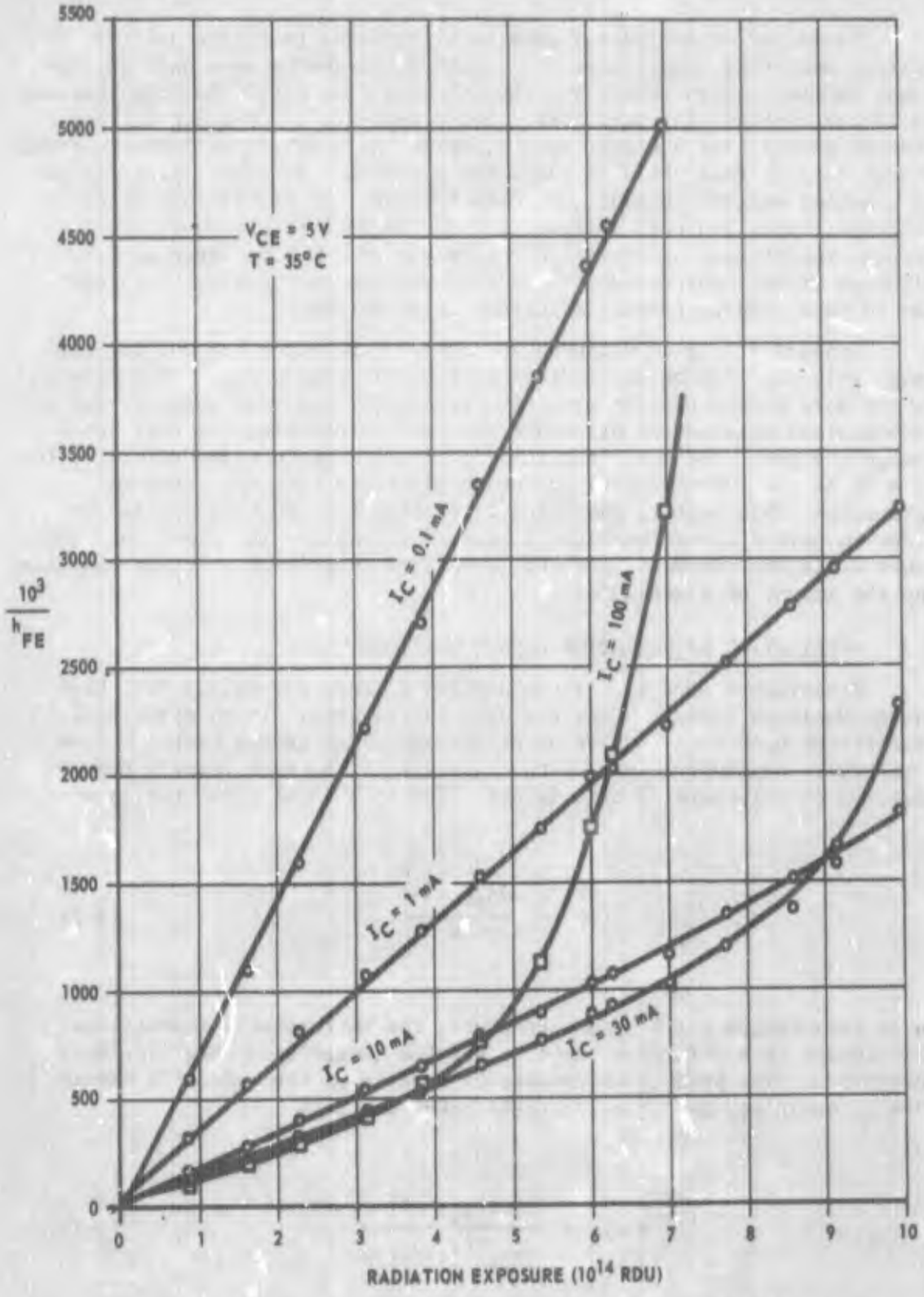

Figure 3-2. Effect of large degradation on h_{FE} of 2N1613 transistor

Linearity of reciprocal gain is illustrated in Figure 3-1 for various measuring conditions.[3] The gain measurements were made at constant emitter current (I_E), and the discrete data points for the constant collector current (I_C) were determined graphically. Constant emitter current curves have a slight upturn, while the constant collector current curves tend to fall off with radiation exposure. Straight lines fitted to constant emitter current gain data for over 100 transistors of 20 different types indicate a linear fit of the data points to within 1 percent coefficient of variation for values of $t\ K\ \phi$ as large as 0.3. Although either constant emitter current or constant collector current can be used, constant emitter current is preferred.

Linearity of gain measured at constant collector current for very large gain degradation on a 2N1613 is shown in Figure 3-2.[4] The spread in the data points results from flux gradients, spectral changes, and an inconsistent measurement procedure not fully accounting for fast anneal damage changes. The sharp nonlinear increase in gain degradation for the I_C = 30 mA and 100 mA curves is due to the transistor operating in saturation. This region, discussed in Section 5.3, must be avoided in order to have a linear reciprocal gain relationship with exposure. The lower collector currents, 1 mA to 10 mA, are surprisingly linear considering the amount of degradation.

3.3 APPLICATION OF RADIATION DAMAGE MONITORS

Transistors used to measure neutron fluence are called Radiation Damage Monitors (RDMs). They are used in two ways. In an electrical calibration procedure, the value of the empirical damage factor K from a reference exposure is used with the value of the base transit time t measured on unirradiated transistors. Equation (3-5) takes the form

$$\phi(x) = \frac{\Delta h_{FE}^{-1}(x)}{t\ K_r} \tag{3-7}$$

In an irradiation calibration procedure, the unirradiated transistors are exposed in a reference exposure and the damage rate $\Delta h_{FE}^{-1}(r)/\phi(r)$ determined. The product tK cancels in a ratio of the reference damage rate in question, and equation (3-5) takes the form

$$\phi(x) = \frac{\Delta h_{FE}^{-1}(x)}{\Delta h_{FE}^{-1}(r)/\phi(r)} \tag{3-8}$$

Table 3-1. Application of Radiation Damage Monitors

Device	Test r $\phi_r = 1.83 \times 10^{13}$ n/cm^2 = 1.83×10^{13} RDU			Test x		
	$\Delta\left(\frac{10^3}{h_{FE}}\right)\Big\|_r$	t $(10^{-9}$s$)$	$K = \frac{\Delta h_{FE}^{-1}\Big\|_r}{t\,\phi_r}$ $(10^{-6}$ cm^2/s-n$)$	$\Delta\left(\frac{10^3}{h_{FE}}\right)\Big\|_x$	$\phi_x = \frac{\Delta h_{FE}^{-1}\Big\|_x}{t\,K_r}$ $(10^{13}$ RDU$)$	$\phi_x = \left(\frac{\Delta h_{FE}^{-1}\Big\|_x}{\Delta h_{FE}^{-1}\Big\|_r}\right)\phi_r$ $(10^{13}$ RDU$)$
1	38.01	1.060	1.96	30.43	1.41	1.468
2	43.15	1.180	1.99	34.55	1.44	1.468
3	45.09	1.191	2.07	35.71	1.48	1.445
4	59.14	1.633	1.98	45.88	1.38	1.420
5	53.41	1.367	2.13	42.65	1.54	1.464
	Average K_r		2.03	Mean ϕ_x	1.45	1.453
	Coefficient of variation		3.16%	Coefficient of variation	3.85%	1.21%

Irradiation temperature - 25°C

Measurement conditions

T = 35°C

I_C = 10mA

V_{CB} = 5V

Examples of electrical calibration and irradiation calibration are shown in Table 3-1. Five RDMs are irradiated together in reference Test r. The electrically measured values of t are then used along with the foil measured fluence of 1.83 x 10^{13}n/cm2 above 0.1 MeV to compute a value of K for the reference exposure. This value is 2.03 x 10^{-6} per RDU-s.

Five other unirradiated RDMs are then calibrated electrically by measurement of their base transit times followed by exposure in the unknown neutron irradiation source x. In the example the same transistors are used to illustrate both the electrical and irradiation calibration procedures. Equation (3-7) is then used to compute the value of the unknown exposure ϕ_x in RDU. The average value for the five RDMs is 1.45, with a coefficient of variation of 3.85 percent.

An irradiation calibration procedure also is illustrated in Table 3-1. The five RDMs are exposed in a reference exposure of ϕ_r = 1.83 x 10^{13} RDU and the damage rate $\Delta h_{FE}^{-1}(x)$ measured. Equation (3-8) is used to compute the unknown exposure, which in the example is 1.453 x 10^{13} RDU with a coefficient of variation of 1.21 percent.

Typical coefficients of variation under near ideal conditions are 1 percent for irradiation calibration and 4 percent for electrical calibration.

Radiation damage monitors are also used to determine the damage gradient across an experiment, which, in some instances, is more important than determining the damage exposure. This is done by exposing a group of RDMs, closely packed together or on a rotating disc, in a steady-state reactor operation and then spreading them out across the experiment in which the damage gradients are to be determined. The gradients as illustrated in Table 3-1 can be determined to about 1 percent for irradiation-calibrated devices and to about 4 percent for electrically-calibrated devices.

In a program to develop the practical application of RDMs in RDU measurements, five device types have been chosen to cover the exposure range of 10^{11} to 10^{15}n/cm^2 ($\sim$ fission spectrum) or 10^{11} to 10^{15} RDU. These are illustrated in Figure 3-3. Two hundred units have been irradiation-calibrated and an additional one hundred, electrically calibrated. These units in limited quantity along with use instructions are available for special experiments.*

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*Radiation Damage Monitors are available from:

Captain Richard L. Walker or Lt. Charles Ramsey, WLDN-2
(telephone: 505-247-1744 Ext. 3121 or 2345)
Air Force Weapons Laboratory
Research and Technology Division
Air Force Systems Command
Kirtland Air Force Base, New Mexico 87117

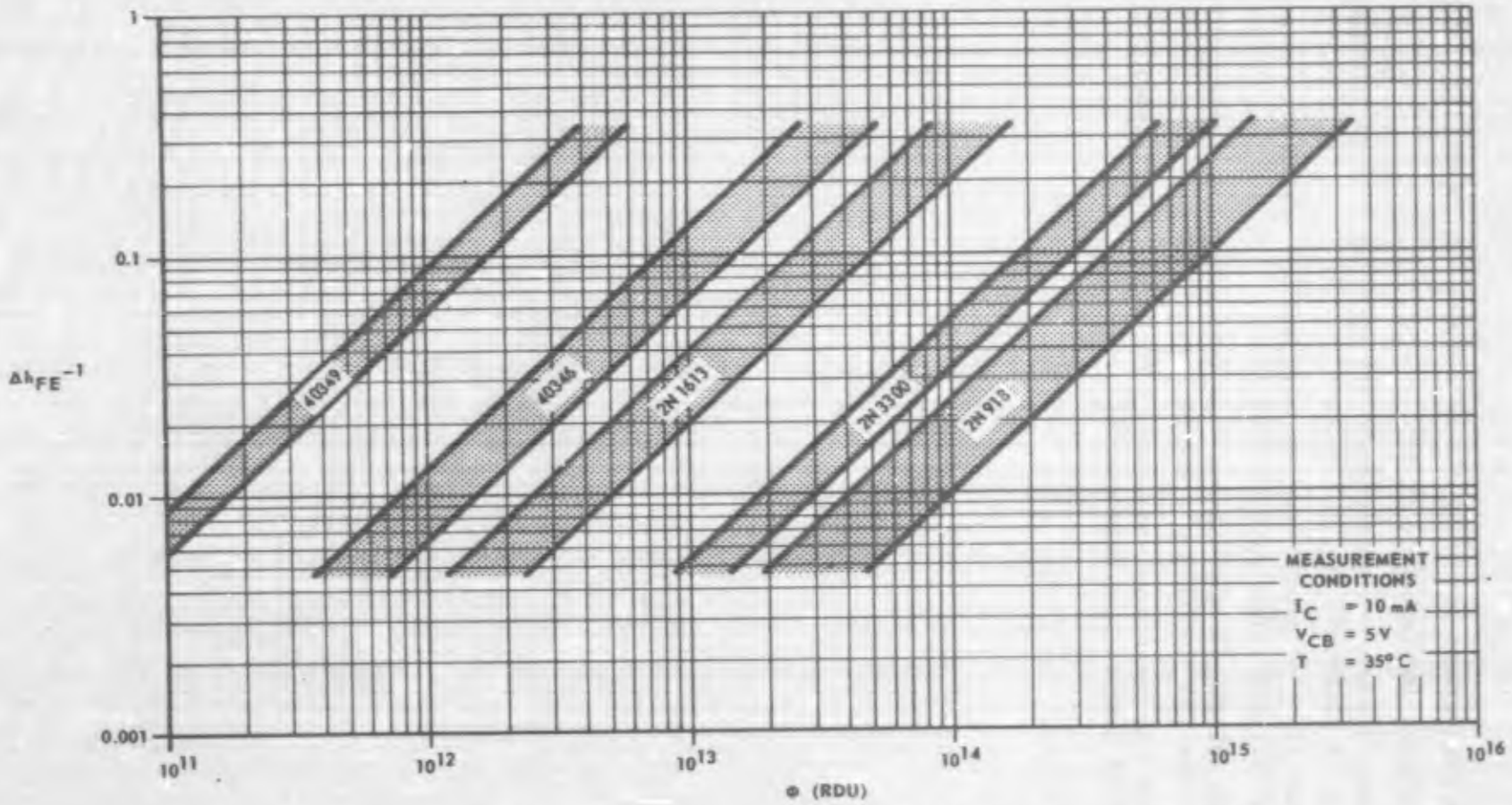

Figure 3-3. Damage versus irradiation for Radiation Damage Monitors

Some suggestions for using the RDMs listed in Figure 3-3 follow.

-- Measure and irradiate at 35°C

-- Good h_{FE} measuring conditions are I_E or I_C = 10 mA; constant I_E is preferred; V_{CB} = 5 volts

-- Measure just prior to an exposure and at a constant time period after, preferably greater than 10^5 s

-- Do not subject the RDMs to high temperatures or large current injections during their use period

-- Use the procedures suggested in Section 5.2 and Appendix A for base transit time measurements

SECTION 3 - REFERENCES

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SECTION 4

INTRODUCTION TO RADIATION EFFECTS IN TRANSISTORS

To predict changes in transistor performance with radiation, the designer should have an elementary understanding of transistor construction and of the currents influencing gain. These areas are briefly discussed in this section. A detailed description is beyond the scope of this handbook. Many texts on transistors are available if the designer wishes to delve more deeply into transistor characteristics and mechanisms affected by radiation damage. Selected semiconductor texts are listed in the Bibliography. However, the prediction procedures described in this handbook can be performed without an extensive solid state physics background.

The designer will also find it helpful to know qualitatively the transistor performance parameters that are sensitive to radiation, the relative degree of sensitivity, and the direction of the change. Under certain environment and/or transistor operating current levels, transistor performance is governed by surface effects, which are not predictable at this time. It is important that the designer be able to recognize when surface effects exist.

4.1 PHYSICAL DESCRIPTION OF PLANAR TRANSISTORS

Modern planar transistors are fabricated by diffusing both n-type (phosphorus) and p-type (boron) impurities into the top surface of a previously doped piece of silicon. A cross-sectional view of a typical epitaxial planar transistor is given in Figure 4-1. The basic unit of depth below the surface is a micron (μm), which is 10^{-4} cm. One mil (0.001 inch) is approximately equal to 25 microns.

The manufacturing procedure is first to form a silicon dioxide layer on the surface of a predoped silicon chip. A photo-etching technique is then used to form masks on the silicon dioxide surface that permit etching off the silicon dioxide in those areas where the base and emitter diffusions are desired. After the diffusion process, the surface silicon dioxide layer is reformed to isolate and protect the surface and emitter-base and collector base junctions. The distribution of diffused impurities is controlled by their initial surface concentration and the time and temperature of diffusion. A typical impurity concentration through an epitaxial planar transistor is shown in Figure 4-2. The word "epitaxial" refers to the region from the heavily doped substrate to the surface. The epitaxial layer is made by deposition of a thin layer of uniformly doped silicon upon a predoped silicon substrate.

The upper portion of Figure 4-2 shows the total concentration of impurities in the epitaxial layer (constant n) and the impurities diffused

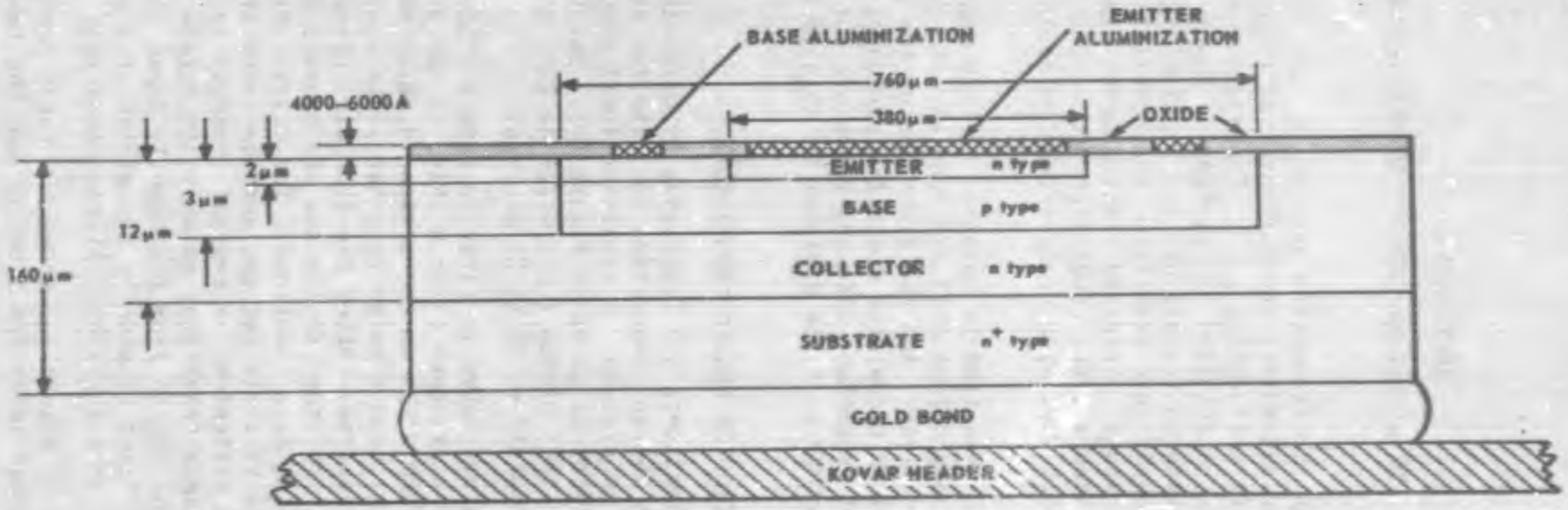

Figure 4-1. Cross section and typical dimensions of an n-p-n epitaxial planar transistor

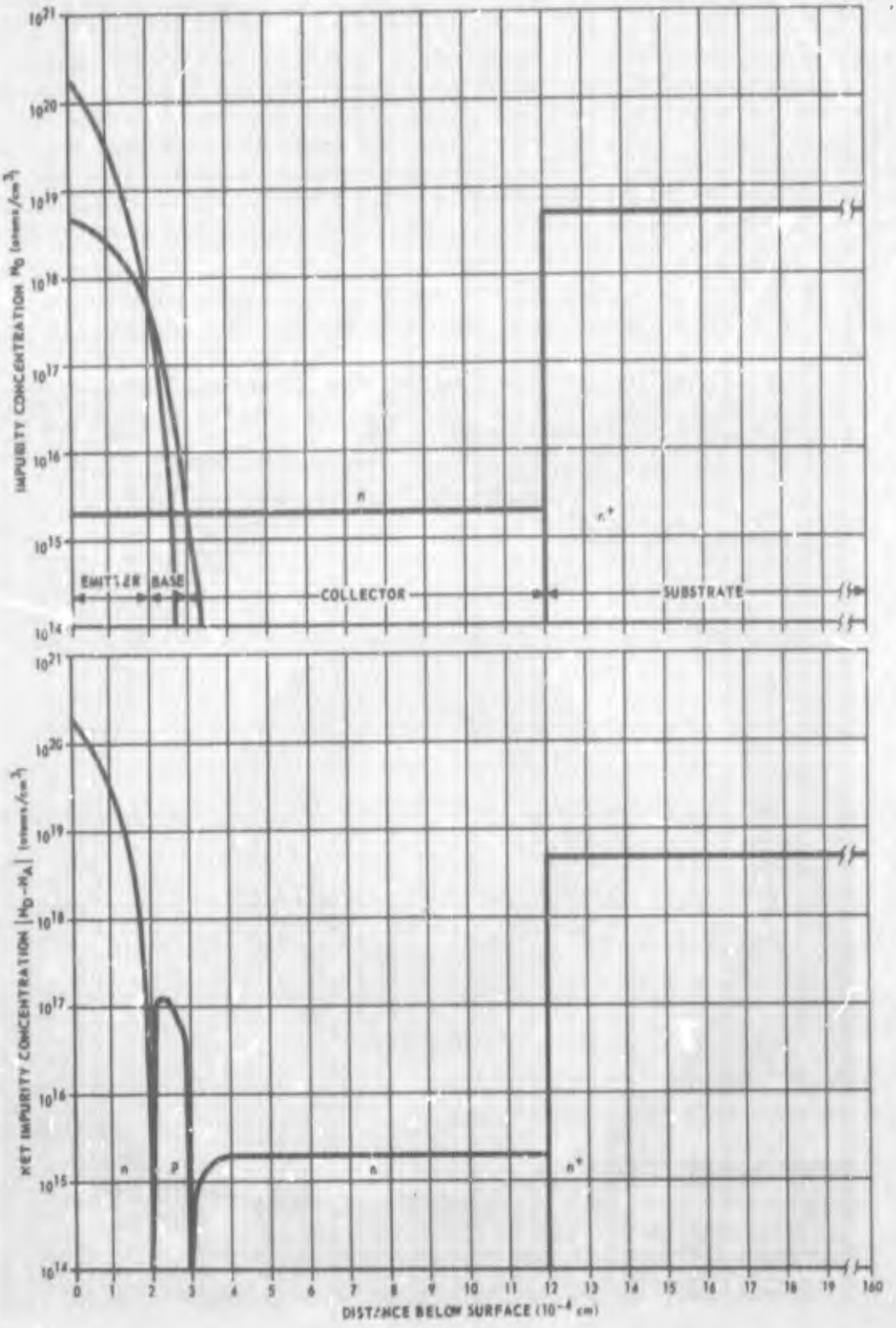

Figure 4-2. Cross section of an epitaxial planar transistor showing typical impurity concentrations and net donor and acceptor concentrations

into the silicon during the formation of the base and emitter regions. Since acceptors and donors cancel each other, the net impurity concentrations shown in the lower part of the figure are the effective impurity concentrations in a transistor. The plane where the acceptors p equal the donors n (and the net impurity concentration is zero) is called the metallurgical junction. Between the n and p regions is an ionized layer called the space charge region, the depletion region, the transition region or simply the junction.

Figure 4-3 is a photograph of the top of a typical transistor. The emitter-base and collector-base junctions and the emitter and base contacts

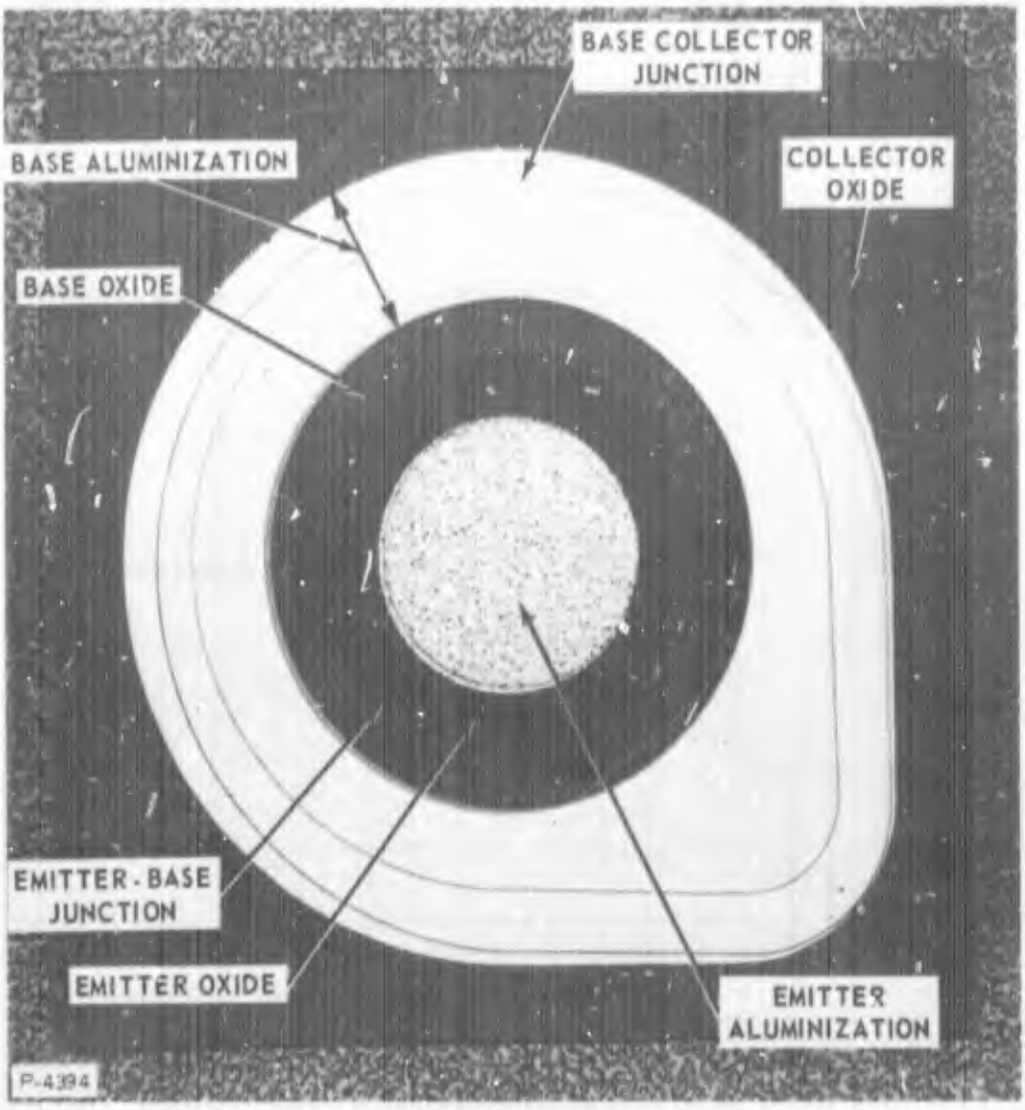

Figure 4-3 - Top view of circular geometry planar transistor

can be identified by comparing the photograph with the cross-sectional view in Figure 4-1. For other transistors, emitter and collector areas necessary for prediction can be easily measured from similar pictures. The emitter and base contacts are shown, while the collector contact is at the bottom of the chip of silicon through the gold bond and Kovar header shown in Figure 4-1.

A nonepitaxial transistor differs from the epitaxial transistor illustrated here in that it has no heavily doped substrate and its lightly doped collector region extends to the collector contact.

The large variations in current capability between transistor types results from the emitter area, which can be less than 10^{-5} cm^2 for small switching transistors and larger than 10^{-2} cm^2 for large power transistors. At high current levels the emitter perimeter rather than the emitter area determines current handling capacity. This is because the current flow is crowded to the periphery of the emitter by the transverse voltage of the base current flowing across the base resistance under the emitter. Large current transistors have high perimeter-to-area ratios. Differences in frequency response are primarily due to variations in the thickness of the base region. The voltage capability is determined by the doping level in the collector including the thickness of the collector for epitaxial transistors, while the saturation voltage at high currents is set primarily by the resistance of the collector region.

4.2 EFFECTS OF DISPLACEMENT RADIATION DAMAGE ON TRANSISTOR PERFORMANCE

Of all of the transistor performance parameters, gain is the most important and the most sensitive to bulk radiation damage. The common emitter dc current gain h_{FE} is defined as the ratio of collector current I_C to base current I_B. For a constant emitter current, I_C decreases slightly with radiation (about 20% for h_{FE} degraded from 100 to 4), but I_B for the same degradation in h_{FE} increases enormously (about 20 times). Consequently I_B is the critical radiation-sensitive current component affecting transistor current gain degradation. The base current is made up of several current components, with each assuming special importance over different ranges of collector current. Figure 4-4 shows one-half the cross-section of a silicon planar transistor and the current components for operating in a normal amplifying mode. The reciprocal of the dc current gain expressed in terms of the base current components is

$$\frac{1}{h_{FE}} = \frac{I_S + I_D' + I_{RG} + I_{RB} + I_{CBO}}{I_C} \qquad (4\text{-}1)$$

where

I_S = current due to surface effects at the emitter-base junction

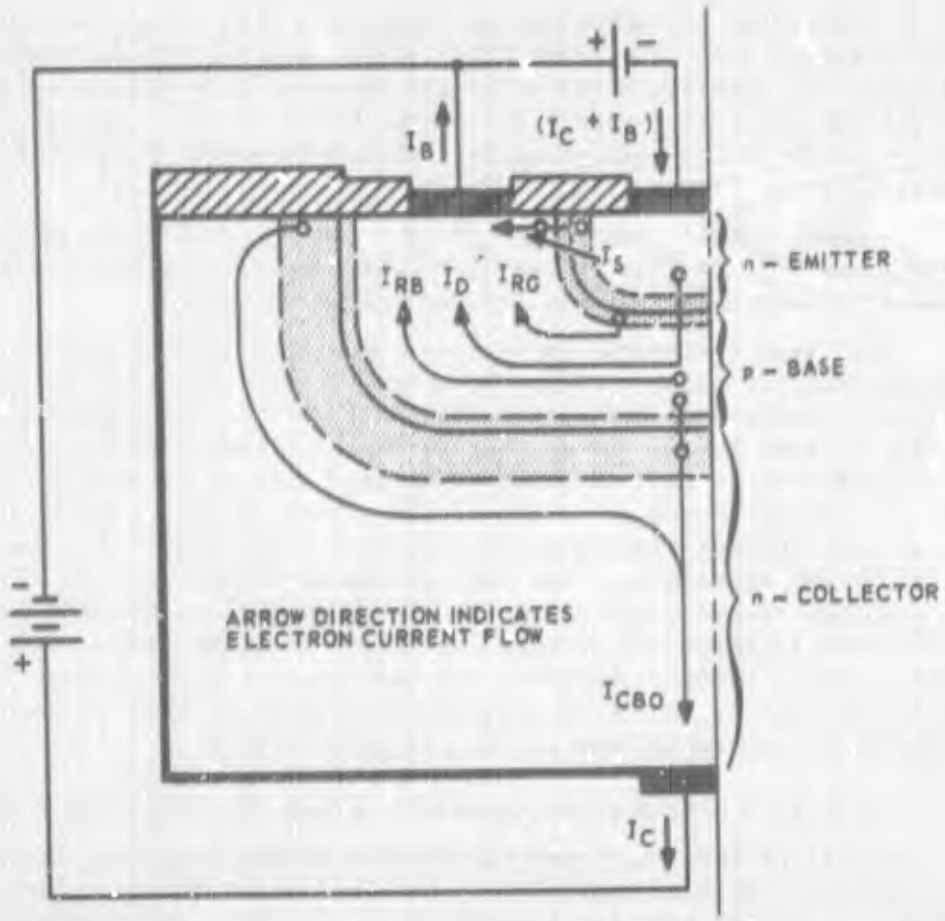

Figure 4-4. Schematic of n-p-n planar transistor current components

I'_D = current due to injection of majority carriers from base to emitter

I_{RG} = current due to recombinations in the emitter-base transition layer

I_{RB} = current due to recombinations in the base, and

I_{CBO} = total leakage current at the collector-base junction.

At very low collector current – approximately four to eight decades below the current where transistor gain is a maximum – the surface current dominates and prediction of h_{FE} is impractical. At collector currents approximately two to four decades below current for peak gain, the recombination-generation current in the emitter transition layer is the major component of I_B, and it increases linearly with fluence. At I_C

levels from about two decades of current below the peak gain I_C to current near peak gain, the recombination current in the base region is the most significant term, and it too increases linearly with fluence. At still higher collector currents, the base current increases because I_D' increases and also because the collector-base junction eventually becomes forward-biased and the transistor goes into saturation. Accurate prediction of h_{FE} at such high currents has not yet been accomplished, but investigations are continuing.

By excluding both extreme ranges of the collector current, accurate prediction of h_{FE} can be performed using the relationship

$$\frac{1}{h_{FE}} = \frac{1}{h_{FEO}} + t K \phi \qquad (4\text{-}2)$$

where

h_{FEO} = preradiation common emitter dc current gain

t = average base transit time (s)

K = empirical damage factor $(RDU\text{-}s)^{-1}$

ϕ = neutron fluence (RDU)

In the current range where equation (4-2) is valid, the leakage current I_{CBO} is negligible. The empirical damage factor K is a composite damage factor, which at low currents represents the combined damage effects of carrier recombinations in the base region and in the emitter transition layer region. At normal currents the latter type carrier recombinations are negligible in comparison with carrier recombinations in the base; however, K at high currents also includes the effects of current crowding, which is discussed in Section 5.3.1.

Another transistor performance parameter of major importance, in addition to gain, is saturation voltage $V_{CE(SAT)}$. Of less interest, though still important, are forward voltage V_{BE}, breakdown voltages BV_{CBO} and BV_{CEO}, leakage current I_{CBO} and switching time t_s. The effects of radiation on these are summarized below:

Parameter	Effect of Radiation	
$V_{CE(SAT)}$	INCREASE	Important at moderate to high currents because $V_{CE(SAT)}$ is primarily dependent on collector resistance, which increases due to reduced minority carrier lifetime and carrier removal effects in the collector

Parameter	Effect of Radiation	
		region. Note that the increase is very large if the transistor comes out of saturation, which occurs when the gain h_{FE} degrades to the level of the drive ratio (I_C/I_{B1}), where I_{B1} is the base current in saturation.
$V_{BE(SAT)}$	INCRZASE	The effect is negligible.
V_{BE}	INCREASE	Important at moderate to high currents when voltage drop (base current across base resistance under the emitter to base terminal) increases due to increased base current from additional base region carrier recombinations.
BV_{CBO}	INCREASE	Produced by carrier removal effects in the collector region. The effect is usually small, however.
BV_{CEO}	INCREASE	Primarily produced by decrease in h_{FE} but also proportional to BV_{CBO}
I_{CBO}	INCREASE	Primarily produced by increased carrier recombinations in the base-collector junction (silicon devices at room temperature).
t_s	DECREASE	Net effect is decreased time. The switching time has four components: delay time, which is not affected; rise time, which increases due to decreased h_{FE}; storage time, which decreases due to reduced minority carrier lifetime in the collector; and fall time, which decreases due to decreased h_{FE}.

4.3 SURFACE DAMAGE EFFECTS IN TRANSISTORS

Ionizing radiation, such as gammas (discussed in Section 1) can cause important changes in transistor performance. The two most important parameters affected are current gain, particularly at low collector current where the base current consists primarily of the surface current component, and junction leakage current.

Ionizing radiction results in a charge buildup on or in the silicon dioxide passivation layer. Accumulation of this charge affects the electric potential, the carrier recombination velocity and the carrier concentration at the silicon-silicon dioxide interface in the vicinity of the junction. Changes in these surface variables, in turn, affect the surface current component of base current and junction leakage current.[1,2,3] The predominant damage mechanism is an increase in the surface recombination generation current produced by an enlarged junction transition layer region in combination with defects in the silicon-silicon dioxide interface. The greatest surface effect damage occurs when a junction is reverse-biased, for two reasons: (1) reverse-biasing produces the largest possible fringing field at the junction, which results in a large transition layer volume near the surface, thereby enhancing the magnitude of the surface current; (2) an electric field exists between the transistor can and the semiconductor, which aids the migration of ionized gas to the surface of the device. The case of a reverse-biased collector-base junction is illustrated in Figure 4-5. The surface damage effect is less for the passively irradiated transistor (high impedance between terminals) and least for the transistor irradiated with forward-biased junctions.

Since surface effect damage cannot be predicted from electrical measurements at this time, the designer must be able to recognize its

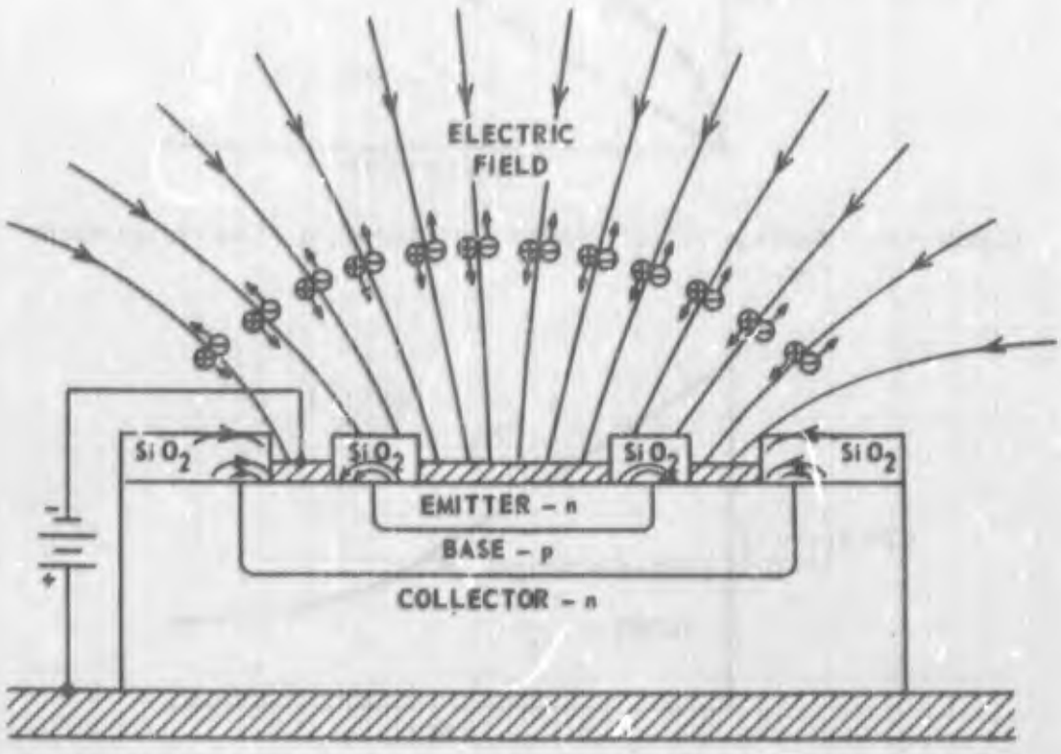

Figure 4-5. Interaction of electric fields and transistor surface (source: Reference 2)

existence from experimental data and must be able to estimate its relative importance to transistor performance. For radiation environments where the neutron/gamma ratio is $> 10^8 \frac{n/cm^2}{R}$ the surface effects of the ionizing radiation are so small with respect to the displacement neutron damage that they can be neglected. Where the neutron/gamma ratio is not known, surface effect damage can be detected from data of the type shown in Figures 4-6 and 4-7. If measurement data as a function of fluence are available, then nonlinear behavior of the reciprocal gain versus fluence curve at low radiation exposures indicates an ionizing radiation damage component. Surface effect damage saturates but bulk damage increases linearly with fluence; hence the relative importance of the two damage effects can be evaluated for a particular radiation exposure. Typical behavior is illustrated in Figure 4-6 for a fixed measurement current and

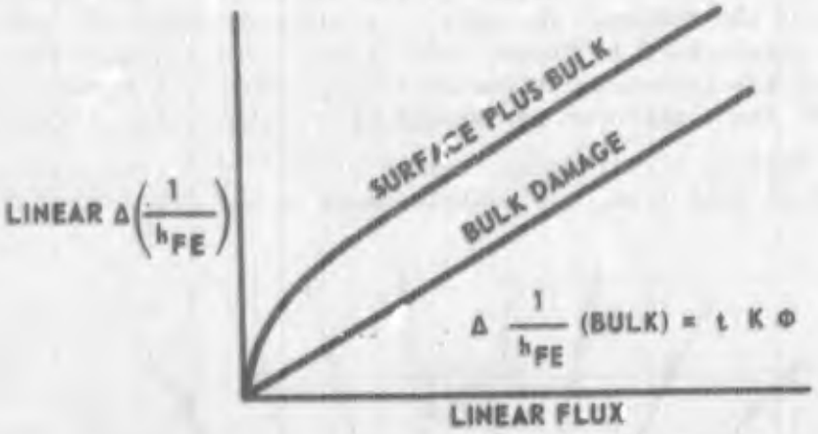

Figure 4-6. Surface effect damage detected at a fixed measurement current

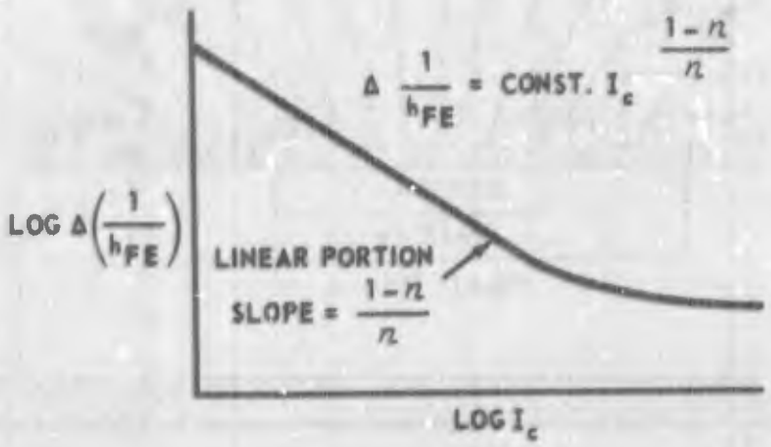

Figure 4-7. Surface effect damage detected at a fixed fluence as a function of current

voltage. When surface effects exist, they become more important as the collector measurement current decreases.

The presence of surface effect damage can also be detected from initial behavior of junction leakage current versus fluence at a constant reverse voltage. Nonlinearity, as in Figure 4-6 for reciprocal gain, indicates that surface effect damage exists. If measurement data are available of the radiation-induced change in reciprocal gain as a function of collector current for a fixed fluence, then a plot of the logarithm of these variables as shown in Figure 4-7 will disclose a surface effect damage component if the slope $[(1/n - 1)]$ has a value of $n = 2$ or greater at low currents. Note that surface damage may also be present when n is less than 2 but greater than 1; however, it is difficult to detect with this technique because bulk damage produces a change in the base current component I_{RG} with a similar range of values for n. Junction capacitance measurements can also be used to identify surface currents.[1]

Experiments have shown that the effect of the ionizing radiation is roughly proportional to the total exposure not the rate when the predominant effect is ionization of the oxide. A given measurement, in rads, of the ionization from a nuclear weapon should cause about the same effect, within a factor of three, as the same exposure from a pulsed reactor, a power reactor, or a Cobalt-60 source.[4]

SECTION 4 - REFERENCES

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SECTION 5

PREDICTION OF TRANSISTOR CURRENT GAIN

5.1 INTRODUCTION

The common emitter dc current gain h_{FE} is predicted using the relationship

$$h_{FE} = \frac{h_{FEO}}{1 + h_{FEO}\, t\, K\, \phi} \qquad (5\text{-}1)$$

where

h_{FEO} = preradiation common emitter dc current gain

t = average base transit time (s)

K = empirical damage factor $(\text{RDU-s})^{-1}$

ϕ = neutron fluence (RDU)

The reciprocal of equation (5-1) is proportional to the base current and varies linearly with fluence. The current components that comprise the base current and the range of collector currents for which equation (5-1) is valid are discussed in Section 4.2.

Since the initial gain can be easily measured, techniques for predicting degraded gain are primarily concerned with determining the base transit time t and the proper value of the empirical damage factor K for use in equation (5-1). The dependencies of the base transit time and the empirical damage factor are explained in order to permit the prediction of transistor gain for a maximum range of operating conditions.

5.2 BASE TRANSIT TIME

The base transit time t, which is the average time injected carriers spend crossing the neutral base region from the emitter to the collector, is the key transistor parameter in the determination of gain degradation with radiation. For most applications the collector current is in a range where the gain degradation is largely due to the increase in base current caused by the radiation-induced higher recombination rate in the base region. The magnitude of this base current is directly proportional to the time that carriers spend in the base region moving from the emitter to the collector. While the base transit time can be roughly calculated

from the width of the base region and the doping distribution in the base region, a simpler and more accurate method of determining this time for specific transistors is by nondestructive electrical measurements.

The base transit time is determined from a set of data of total delay time t' as a function of reciprocal emitter current I_E measured with a bridge instrument of the type described in Appendix A. Figure 5-1 is a typical plot of such data. The total delay time for carriers traveling from emitter to collector includes: (1) an emitter delay (the RC time constant of the emitter junction capacitance and the dynamic resistance of the junction), (2) the base transit time, (3) the time for carriers to cross the collector transition layer, (4) the collector delay (the RC time constant of the collector junction capacitance and collector body resistance), and (5) any influence from the mounting package. The

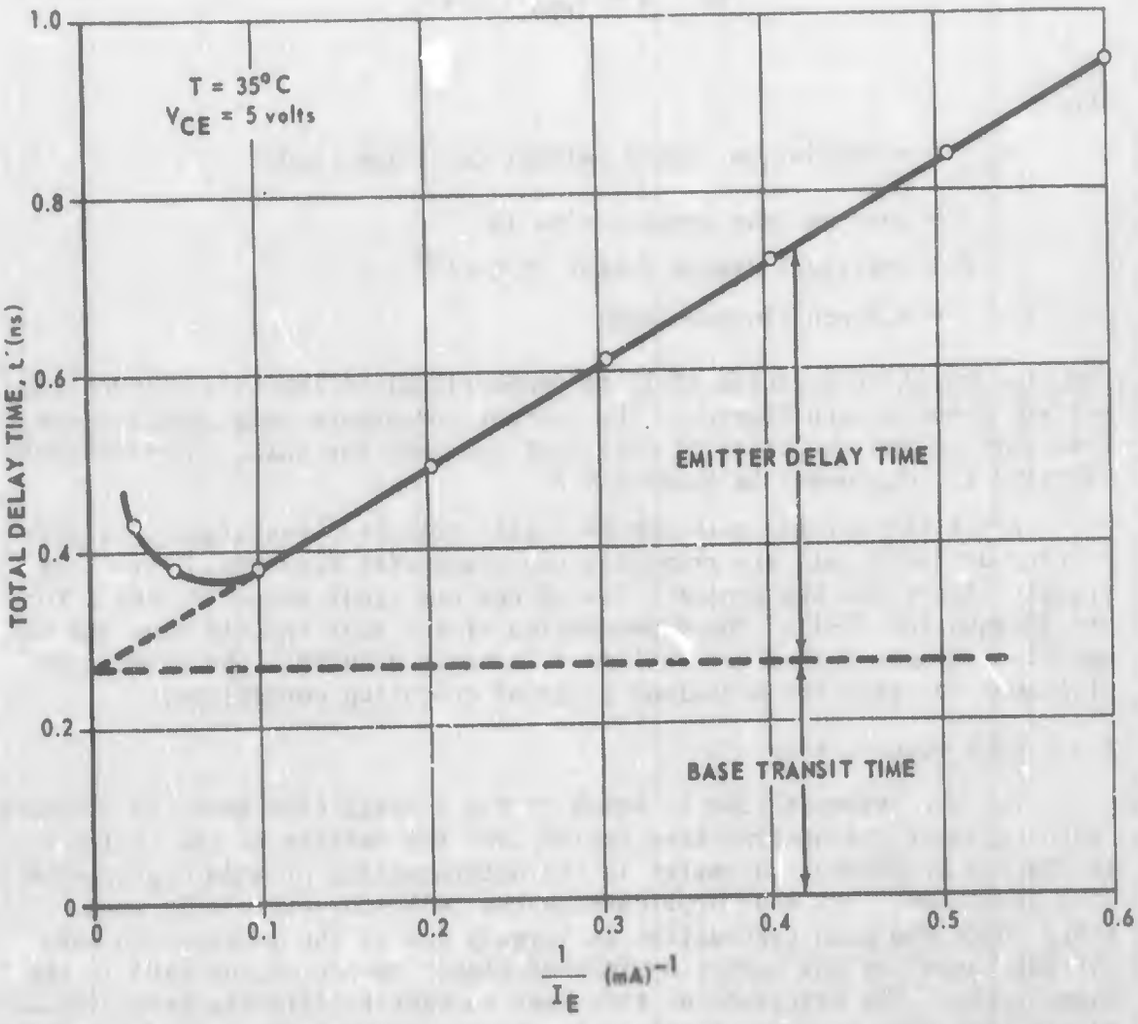


Figure 5-1. Plot of t' versus $1/I_E$

last three delays are assumed to be negligible. The emitter delay is inversely proportional to emitter current since the dynamic resistance of the junction is inversely proportional to this current. The base transit time, which is constant at currents below the current where the total delay time is a minimum, is determined by extrapolating the t' data to infinite I_E.

Measurement data of the type in Figure 5-1 should be obtained with the test device collector-to-emitter voltage V_{CE} at the same value as that applied to the transistor in the circuit. Increasing V_{CE} decreases the effective base thickness and therefore the base transit time; however, the effect of V_{CE} on t is generally small.

For transistors with dc gains above 25, changes in the ambient case temperature in the vicinity of 35°C have a negligible effect on the base transit time. Data at very high or low temperature are not available, however. For transistors operated at temperatures much different from 35°C, base transit time should be measured at the corresponding operating temperatures. For low gain transistors, the temperature should also be controlled.

At high operating currents the total delay time t' as an inverse function of I_E becomes nonlinear and increases significantly above the minimum value of t'. In this current range the transistor is operating in saturation, and equation (5-1) is not directly applicable. Operation in this region is discussed further in Section 5.3.1.

If instrumentation to measure base transit time is not available, t may be computed from data of the gain-bandwidth product f_T as a function of $1/I_E$, where f_T is related to t' by the equation

$$t' = \frac{1}{2\pi f_T} \qquad (5\text{-}2)$$

f_T can be measured with an instrument such as the General Radio Type 1607A Immittance Bridge. The f_T data are actually ac gain (h_{fe}) measurements multiplied by the measurement frequency f. The measurement frequency is important since t in the equation f_T is defined for the region where the gain-frequency characteristic exhibits attenuation of 6dB per octave. The frequency should be selected to give h_{fe} values ranging from about 10 to 2 for typical transistor types.

5.3 EMPIRICAL DAMAGE FACTOR

The base transit time accounts for the differences in the physical base properties of the transistor in the prediction equation. The empirical damage factor accounts for the base material properties of the transistor in the prediction equation, including the effects of the

transistor operating conditions of current and temperature. The empirical damage factor has a large dependency on current and a small dependency on temperature. The damage factor also varies with the dopant type, concentration, and distribution in the base region. The use of equation (5-1) for accurate h_{FE} prediction requires a knowledge of the empirical damage factor as a function of each of these different dependencies. To completely specify K for the large number of transistor types currently available and the wide range of operation conditions, would necessitate accumulation of an enormous amount of data. Fortunately, the use of a single mean value of K for all transistor types gives errors that are generally acceptable in radiation damage prediction. These errors can be reduced for a specific transistor type by a simple passive irradiation of a few transistors of that particular type.

Empirical damage factors were determined as a function of emitter current, for five each of 21 different n-p-n device types and a smaller number of p-n-p device types.[1] A mean curve was computed of the damage factors normalized as a function of emitter current density $J_E = I_E/A_E$, where A_E denotes the total physical emitter area of the specific transistor. The measured damage factors are summarized in Figure 5-2. The data apply to passive (open terminals) irradiation at a nominal operating temperature of 35°C and with $V_{CE} = 5$ volts. The level of collector voltage selected precludes most transistors from entering the voltage saturation mode of operation or experiencing collector-to-emitter voltage breakdown at the high measurement currents. Satisfactory gain predictions can be made using the mean damage factor curve and the measured t for the device. Accuracy is improved by correcting the damage factors given in Figure 5-2 to include the effect of the operating current and temperatures other then 35°C during irradiation. However, only limited data are available for such corrections.

The most accurate gain prediction for a specific transistor type is achieved by using a value for K that is experimentally determined from a radiation test of a few transistors at fixed operating conditions of current, voltage and temperature. Accurate prediction of gain degradation is usually required for only the most vulnerable transistors in radiation-hardened electronics and for determining the reliability of a final hardened design. The majority of circuit designs, particularly preliminary designs, can be made with transistor gain degradation predicted from the mean damage factor data in Figure 5-2. The limitations of the empirical K data should be understood and pertinent corrections in K applied to improve prediction accuracy. These limitations will be discussed next.

5.3.1 Dependence of K on Current

Because K is an empirically derived damage factor, equation (5-1) may be used over a wide range of emitter current densities. Prediction of gain is most accurate for current levels near maximum

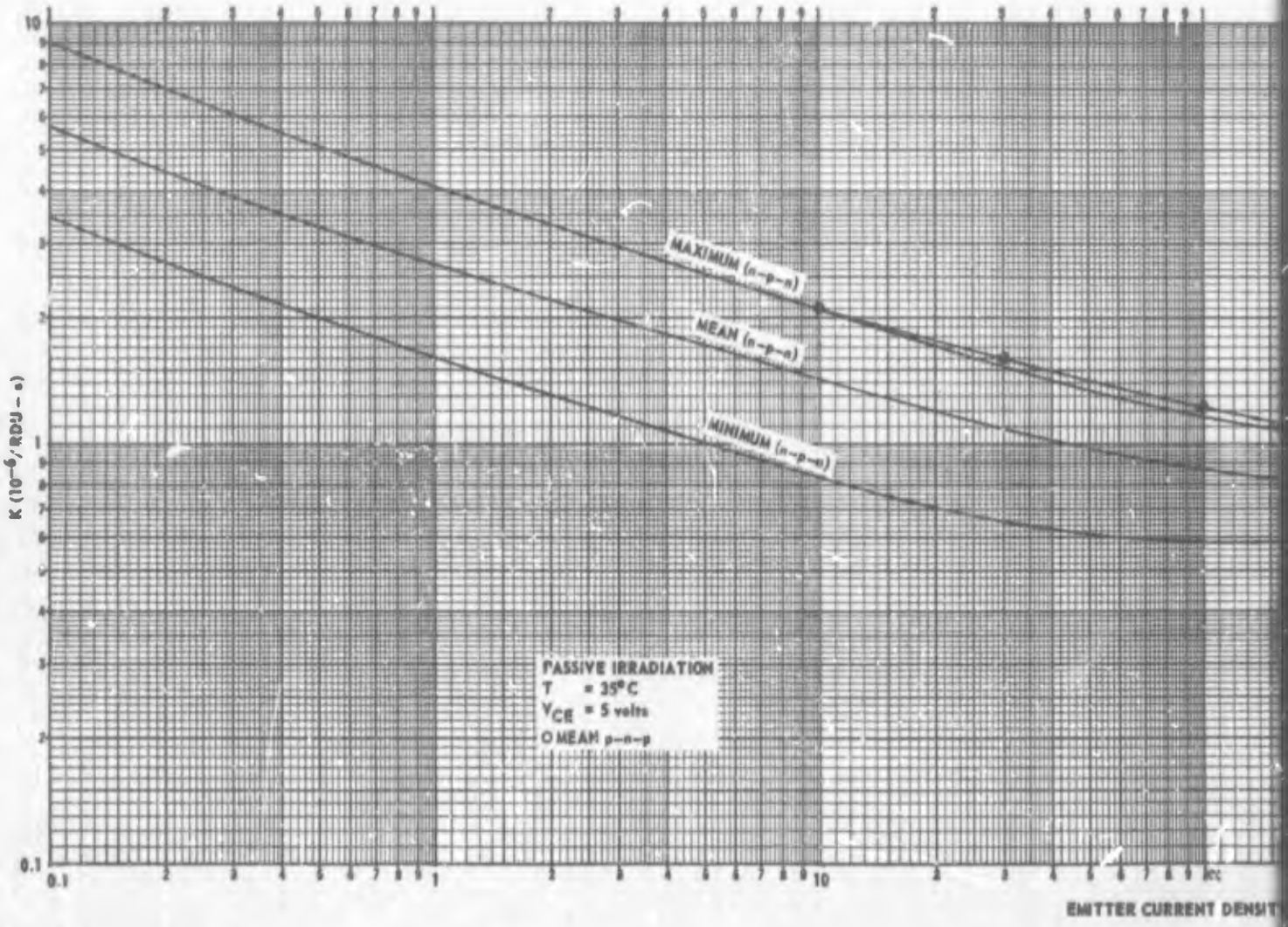
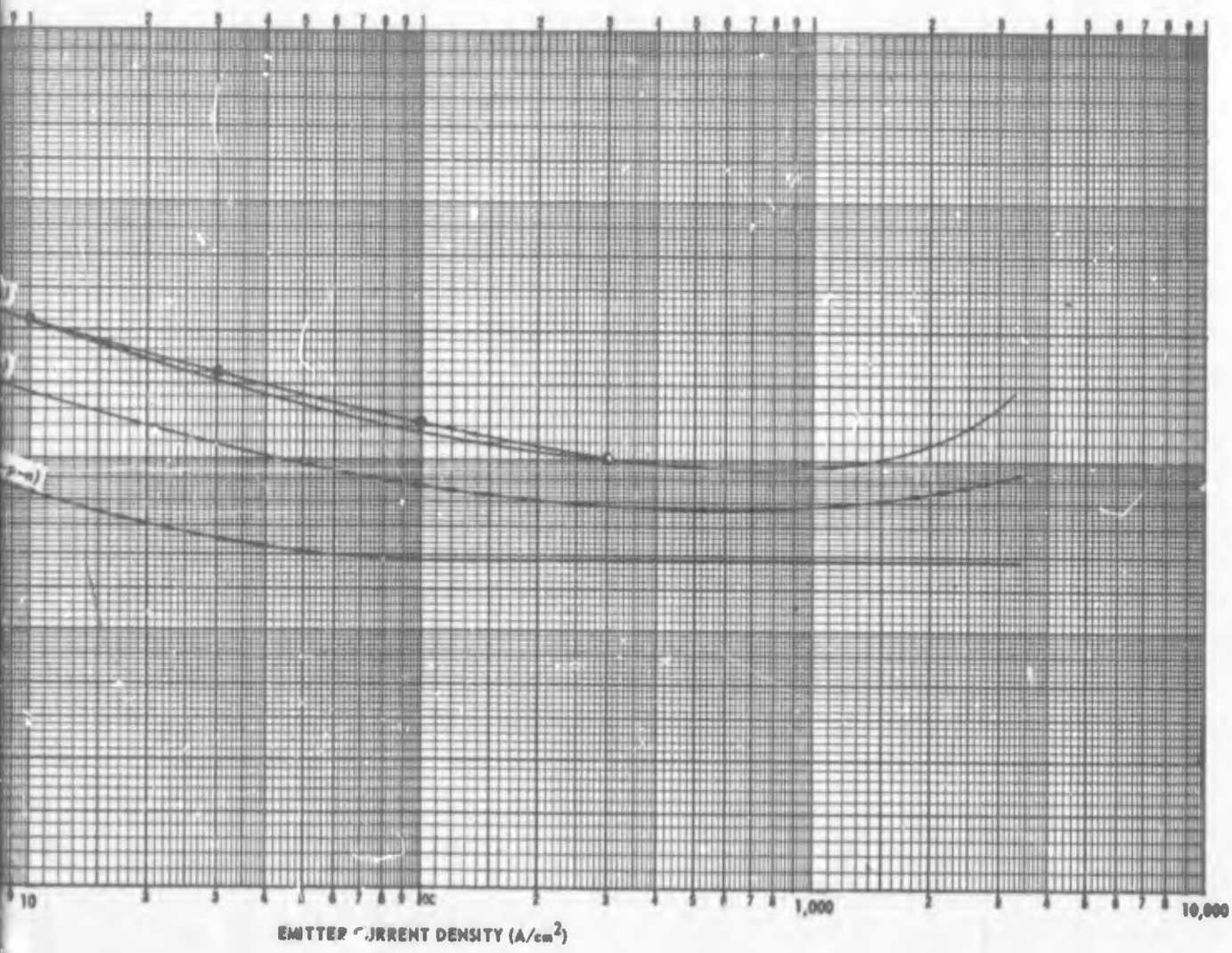


Figure 5-2. Mean empirical damage factor as a function of emi



al damage factor as a function of emitter current density

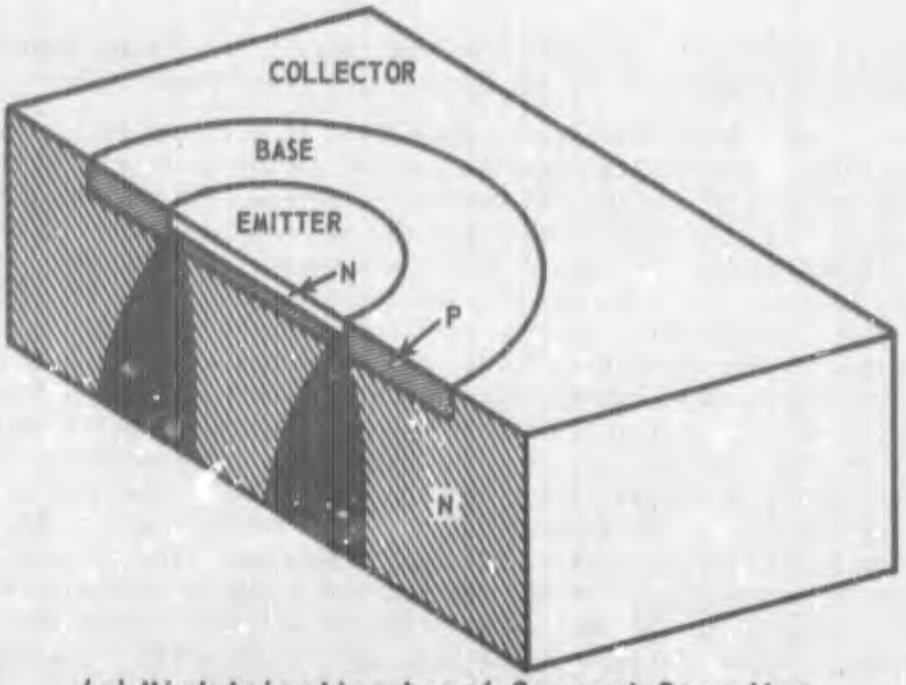
gain in the transistor's typical operating range. Prediction accuracy decreases at both lower and higher operating current densities.

At low currents gain degradation is governed by carrier recombinations in the neutral base region and in the emitter junction transition layer. As the current density decreases, the recombination current in the emitter junction becomes the dominant component of base current. Equation (5-1) is based on the assumption that carrier recombinations in the base are the only degradation mechanism. The recombinations of carriers in the emitter junction transition layer should be dependent on the volume of the transition layer; yet in experimental data of h_{FE} at low current densities, where emitter junction recombinations dominate transistor gain, h_{FE} correlates better with t between different devices than with emitter junction volume. The difficulty in correlating with the emitter junction volume is due to two factors: (1) the lack of a precise description of the exponential emitter-base voltage of this current component, which shows a different dependency with current level for different device types and (2) the lack of a simple technique for accurately determining the emitter junction volume from capacitance measurements. Recombinations in the base and in the emitter junction both increase linearly with ϕ. Consequently, for reasonably good prediction at low current densities, it is more desirable at present to use equation (5-1) with an empirically derived damage factor correlated with t than to attempt to resolve the total base current into components and express the emitter transition layer component separately as a function of transition layer volume. Surface damage effect contributions to gain degradation are ignored since they cannot be reliably predicted at this time. If the surface damage is appreciable, the prediction accuracy at low current densities decreases.

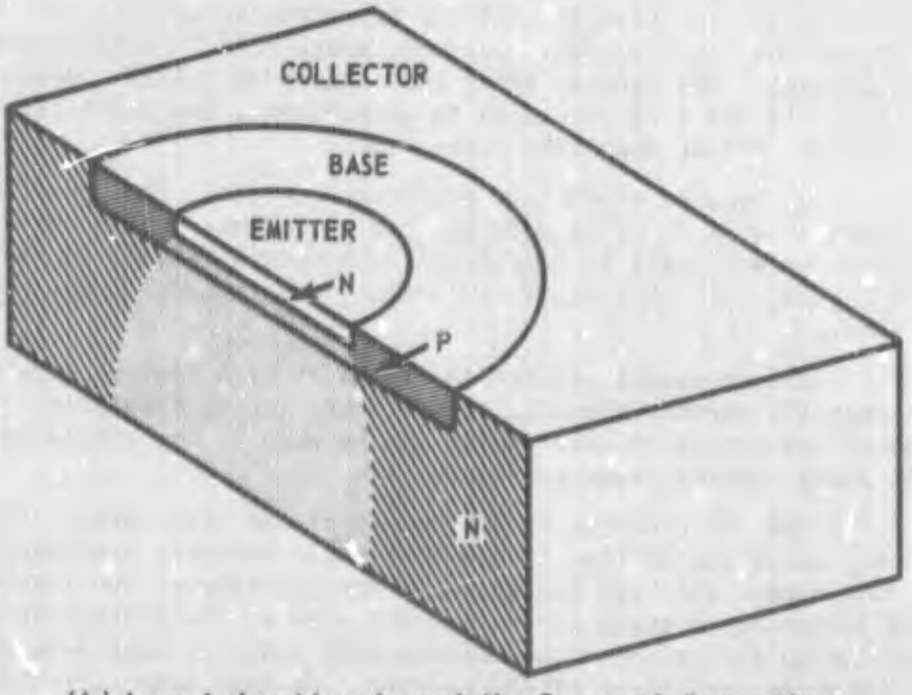
At typical transistor operating currents, the contributions to gain degradation from surface damage and recombinations in the emitter transition layer are small in comparison with recombinations in the neutral base region. For this range of current, predictions of h_{FE} have minimum error.

The increased prediction errors at high current levels are due to either (1) current crowding or (2) operation in saturation. The magnitude of the errors in this regime can be seen by the spread in the empirical damage factor shown in Figure 5-2.

Current crowding is the result of the base current flowing transversely under the emitter to the base ohmic contact, producing a voltage drop across the base resistance. The polarity of the resultant potential difference between the center and edge of the emitter is in the direction to forward-bias the emitter-base junction much more at the periphery than at the center of the emitter. At high base currents, the current flow is forced to the periphery of the emitter, as shown in Figure 5-3, giving a higher current density than would exist without current crowding.



(a) High Injection Level-Current Crowding



(b) Low Injection Level-No Current Crowding

Figure 5-3. Emitter current crowding

A more serious problem at high currents is the effect of operation in saturation. For relatively low collector-emitter voltages (V_{CE} < 10V) and high collector currents, the voltage drop across the collector body resistance can be large enough to forward-bias the collector-base junction, causing additional base current operation in this regime as illustrated in Figures 5-4 and 5-5, where gain is plotted as a function of collector current, with V_{CE} as a parameter. Both transistors were irradiated passively.

The 2N1613 has a relatively thick and high resistivity collector region and therefore is easily driven into saturation. In general, operation in saturation is a problem for high-breakdown-voltage nonepitaxial transistors since these types have both thick and high resistivity collectors. The 2N914, although about one-tenth as large as the 2N1613, exhibits a smaller effect of operation in saturation because it is a lower voltage epitaxial transistor with a low collector body resistance.

The prediction of gain in saturation is essentially the same problem as predicting saturation voltage as a function of "forced beta" or I_C/I_B in saturation. The development of prediction techniques for operation in saturation has not been completed. The transistor is assumed to be operating in saturation whenever the emitter current is above the level where the total time delay t' is a minimum. Until suitable prediction techniques are developed, estimates of gain degradation at these high currents can be made using equation (5-1) and the base transit time determined from emitter currents below the level where t' is a minimum. The prediction accuracy will decrease with increasing current and decreasing collector voltage as indicated in Figures 5-4 and 5-5.

For transistor types where the base region has an impurity concentration significantly less than the collector, the increase in the total time delay at high currents is due to an actual increase in the base transit time and not because the transistor is operating in saturation. Such operation is typical for alloy type devices. Prediction of h_{FE} for such transistors is made using equation (5-1) and a base transit time value obtained by subtracting the emitter time delay from the total time delay at the specific emitter operating current.

5.3.2 Dependence of K on Operating Temperature

When a transistor is irradiated passively, equivalent to high resistance between terminals, or at low operating currents so that the case temperature is the only temperature variable, the damage factor behaves as follows:

(1) Increasing temperature results in decreased damage effect

(2) Increasing currents produce a smaller temperature correction for the damage factor.

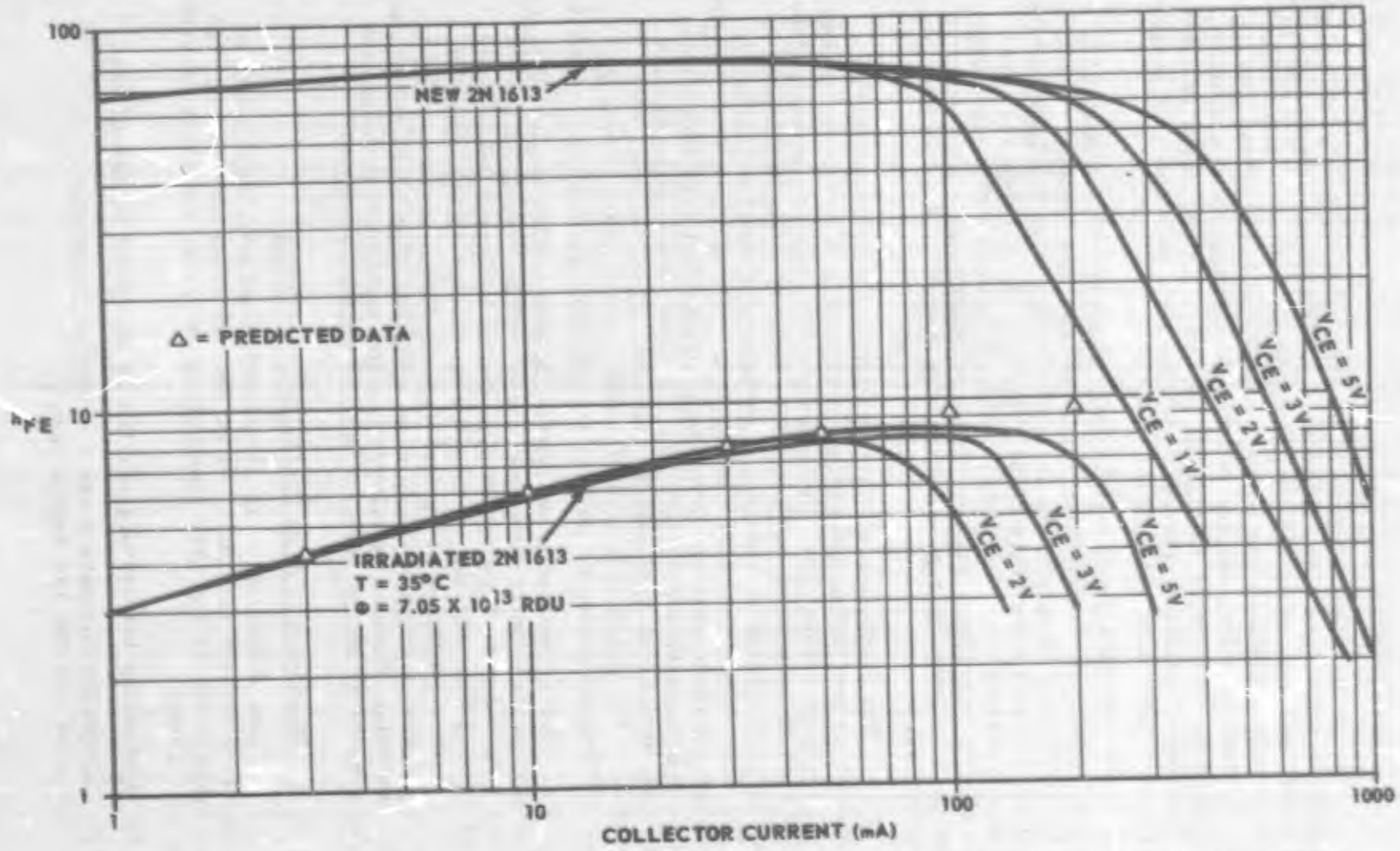


Figure 5-4. Gain variation with collector current and voltage for 2N1613 transistor

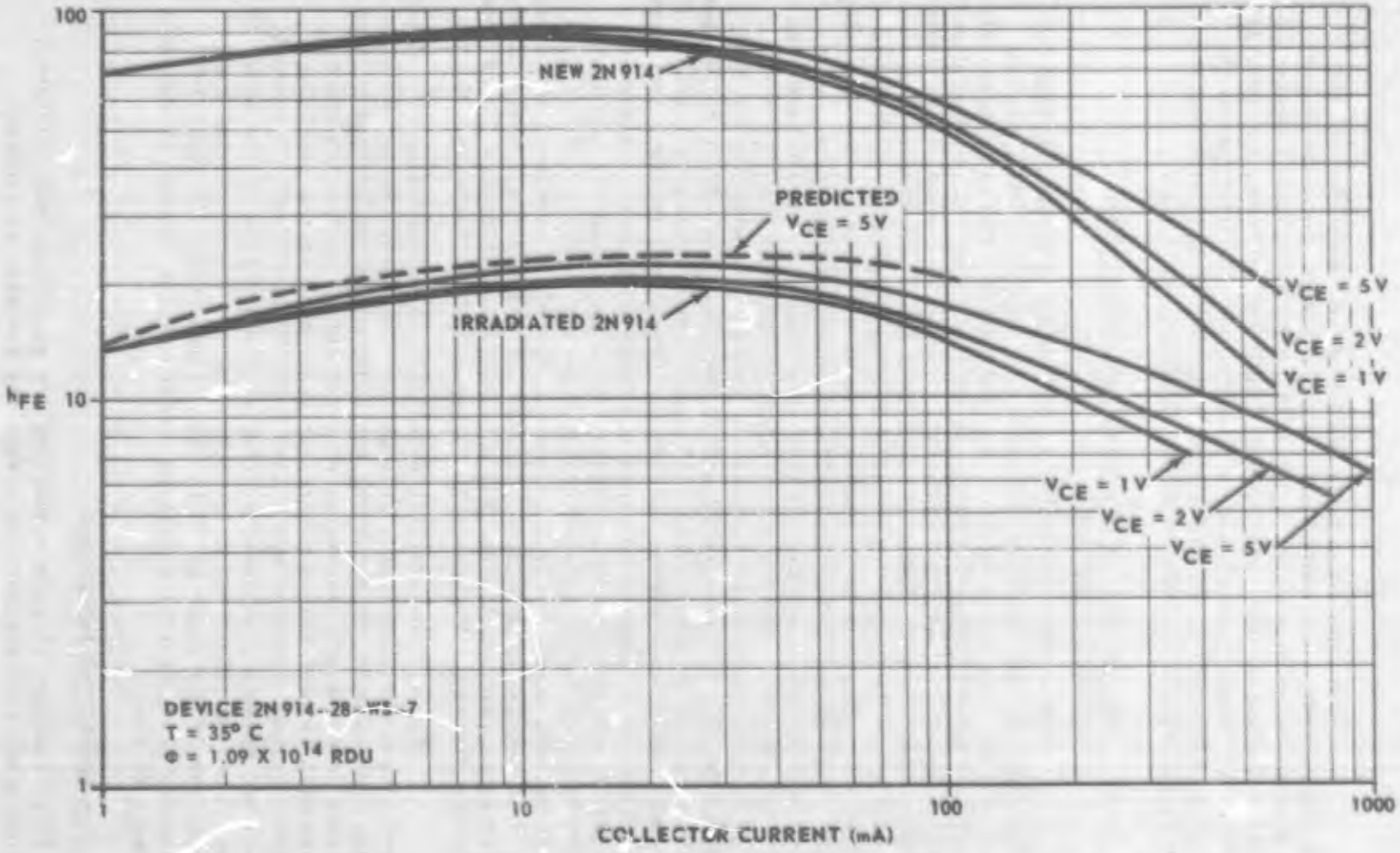


Figure 5-5. Gain variation with collector current and voltage for 2N914 transistor

These conclusions are supported by data obtained for 2N1613 transistors. The curves are shown in Figure 5-6. It is not known whether other transistor types will exhibit the same temperature correction factors at the same current densities; however, the general behavior with temperature should be similar. If the temperature is expected to vary during the transistor's operation in radiation, the damage factor should include an averaged correction factor.

5.3.3 Dependence of K on Current and Temperature During Irradiation

Transistors operating at high current densities show less gain degradation than predicted by using the empirical damage factor curve in Figure 5-2, which is based on transistors irradiated passively. If the collector-emitter voltage V_{CE} is sufficient to cause power dissipation(V_{CE} I_C)at the two junctions which results in a significant temperature rise, then the gain degradation is even less. Experimental data given earlier in Table 2-1 for 2N914 and 2N1613 transistors, indicate damage factor reductions of 22 and 17 percent respectively for operating currents of 25 mA and 100 mA and collector-base voltage V_{CB} = 0 volt. Assuming emitter areas without current crowding, the current densities are 310 and 88A/cm^2. For the same current levels but with V_{CB} = 6 and 12 volts respectively, which results in junction temperatures of 175°C, the damage factors are reduced 27 and 20 percent. The effect of increased junction temperature added to that of high current operation resulted in only a small additional damage reduction. These data indicate that high current alone is sufficient to cause the major portion of the damage reduction; however, only two transistor types were studied, and more data are required before general conclusions may be drawn. Other data taken at current densities of 12.5 A/cm^2 indicated no change in the damage factor from passive irradiation. Neither did transistors irradiated with both junctions reversed-biased show any change in the damage factor from passive irradiation. The curves in Figure 5-7 summarize these results.

For minimum error in prediction, the transistor duty cycle and operating modes of current, voltage and temperature should be considered. For example, in switching applications the percentage of time a transistor is on or off determines what percentage of the radiation exposure will be used with a particular value of K in the prediction equation. Pulsed operation may reduce K due to the effect of current, but need not produce a temperature rise at the junction if the power is applied in narrow pulses and a low duty cycle. Typical thermal time constants are of the order of 10 to 100 milliseconds. In amplifier applications the quiescent operating conditions may be used to estimate the damage factor.

5.4 GAIN PREDICTION PROCEDURES

Three examples of gain prediction are presented, with different levels of prediction accuracy to enable the designer to evaluate

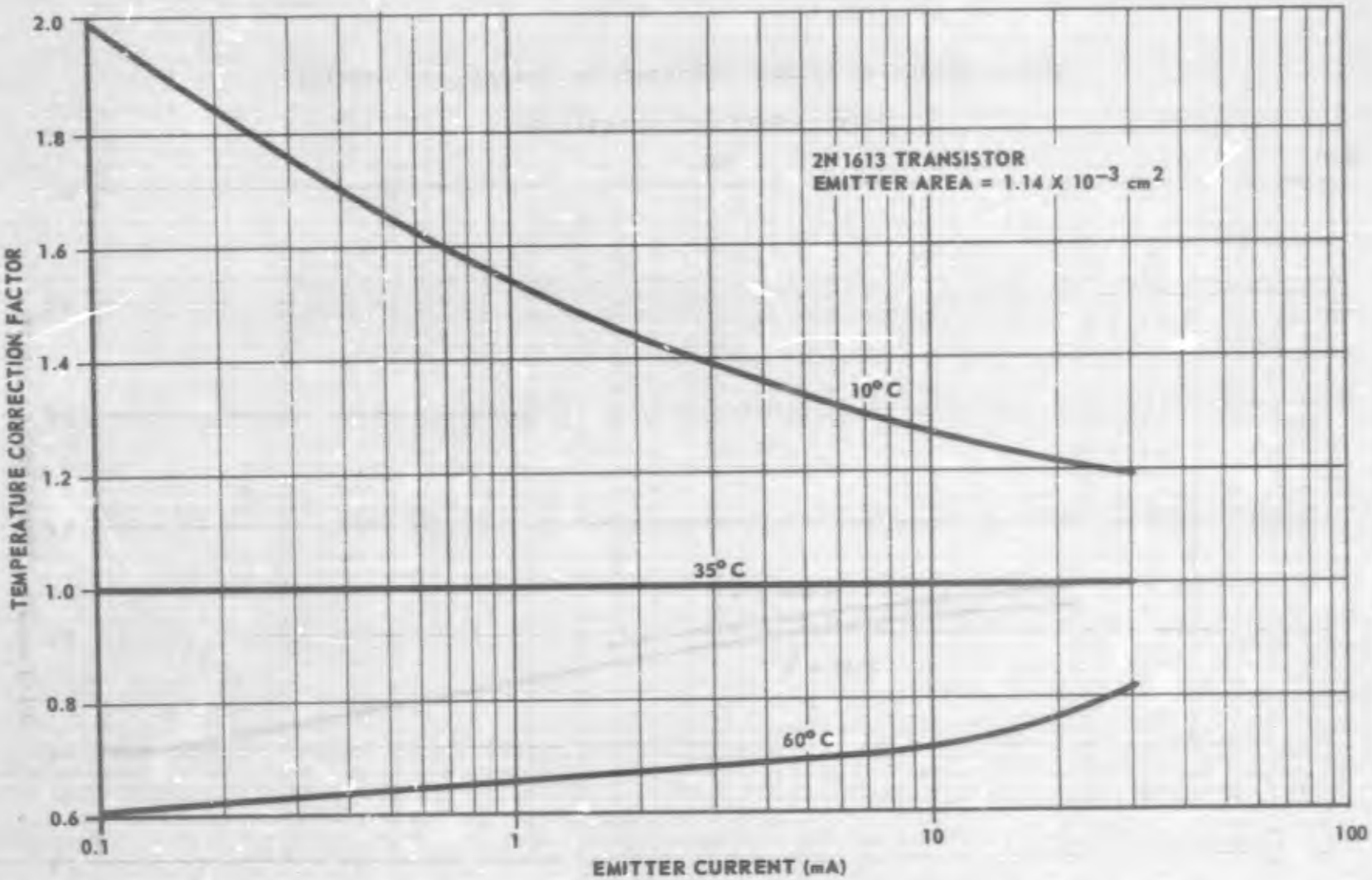


Figure 5-6. Effect of operating temperature as a function of emitter current

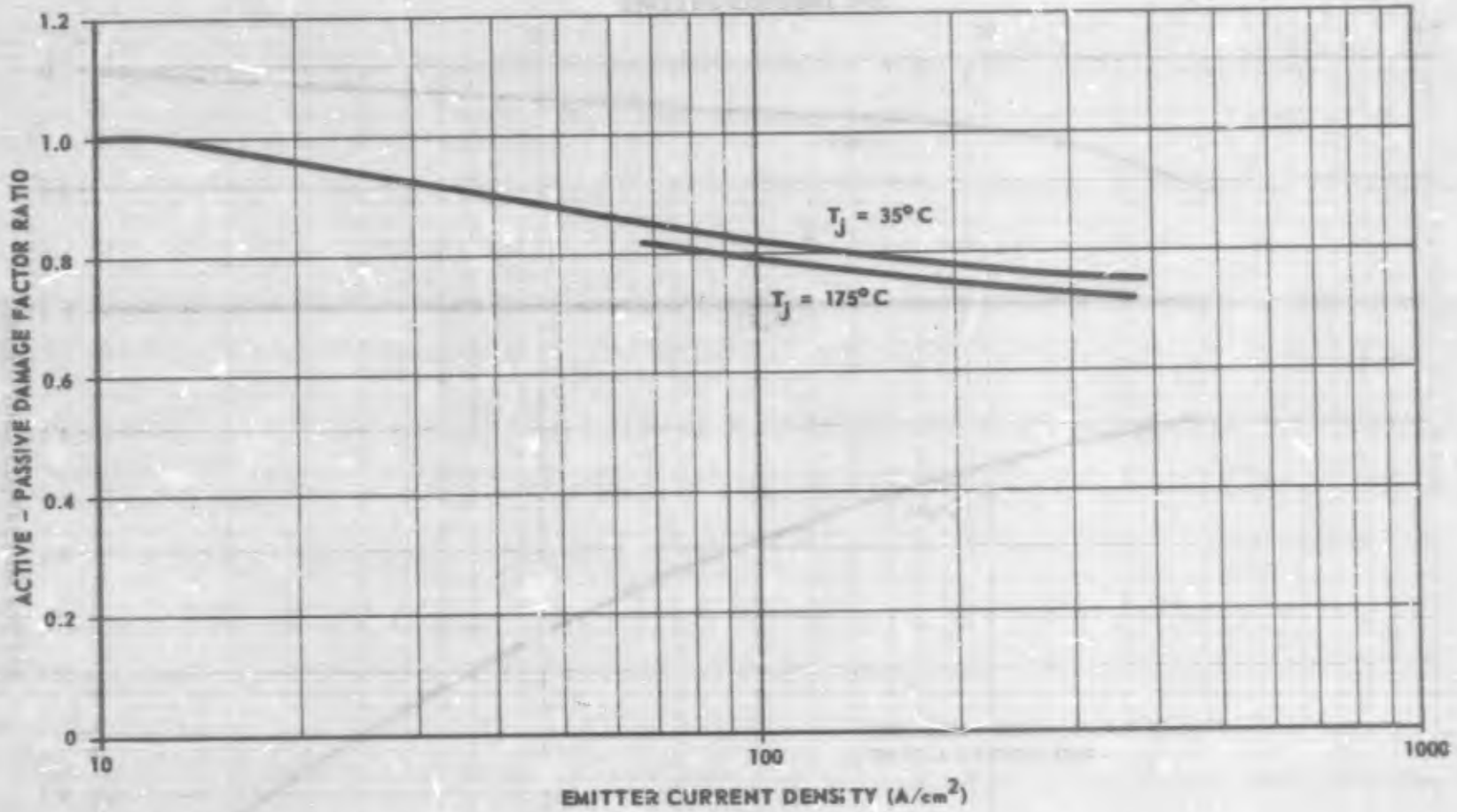


Figure 5-7. Effect of operating current on damage factor

trade-offs between prediction accuracy and the extent of device measurements required. The direct approach without measurements uses manufacturer's typical data and generally results in gain predictions within a factor of 2 for devices in their normal operating current range. If the specific device base transit time is measured and used with a mean damage factor from Figure 5-2, the gain prediction is generally within 25 percent. The most accurate prediction, with error less than 10 percent, is obtained by employing the specific device base transit time together with an empirical damage factor previously determined for the same transistor type and manufacture and for similar operating conditions. The above prediction errors are based on: (1) precise measurement of the radiation environment using radiation damage monitors as discussed in Section 3; (2) controlled temperature nominally at 35°C during irradiation and measurements, and (3) controlled current during measurement, performed in the case of a neutron burst at least 10^4 seconds after the burst. The neutron/gamma ratio is assumed to be $\geq 10^8 \frac{n/cm^2}{R}$.

5.4.1 Gain Prediction Using Manufacturer's Typical Device Data and Mean Empirical Damage Factor

Step 1 Calculate the emitter current density using the equation

$$J_E = \frac{I_E}{A_E} = \frac{I_C(1 + 1/h_{FEO})}{A_E} \qquad (5\text{-}3)$$

where I_E is the operating emitter current and A_E is the total physical emitter area. Obtain the area information by contacting the manufacturer or from photomicrographs of the top surface of a transistor of the same type and manufacture. Changes in the emitter area due to current crowding effects discussed in Section 5.3.1 are not considered since these effects are incorporated in the empirically derived mean damage factor. I_C in the second portion of equation (5-3) is the operating collector current and h_{FEO} the preradiation gain, which is usually available on the device data sheet in the form of dc gain versus I_C at constant V_{CE} and temperature. An estimate of h_{FEO} is sufficient since the effect of this parameter in equation (5-3) is small. In the prediction equation (5-1), accurate h_{FEO} is important only if the gain degradation is small or the initial gain is low.

Step 2 Obtain the mean empirical damage factor K from the curve in Figure 5-2 (pages 5-5 and 5-6). For applications in steady-state radiation environments the effect on K, of the operating

conditions of current and temperature, are neglected since these corrections are small compared with the errors resulting from the use of typical device data. For a weapon application where circuits must function immediately after the neutron burst, increase K from Figure 5-2 for the operating temperature and time after burst by using the fast anneal correction factor data of Sander and Gregory,[2] in Figures 2.4 and 2.5.

If A_E is not available and a crude prediction of h_{FE} is acceptable, the designer may assume a typical K value of 10^{-6}/RDU-s at the normal operating currents indicated on the data sheet for the specific device.

Step 3 Estimate base transit time t from typical gain-bandwidth product data, usually shown on the manufacturer's device data sheet. Obtain the approximation of t by using the equation

$$t = \frac{1}{2\pi f_{T(max)}} \qquad (5\text{-}4)$$

where $f_{T(max)}$ is the peak value of f_T as a function of collector current. The f_T data published by the manufacturer are assumed to be $f_{T(max)}$. This is generally the case since manufacturers prefer to show peak performance for their devices. Exceptions to this rule are high-gain, low-current-level devices, where the manufacturer usually specifies f_T at a low current level. These data apply when the designer operates such devices at low currents. If they are used at higher currents, f_T will be considerably higher and the manufacturer should be consulted for applicable f_T data. In general, however, operation of transistors above the manufacturer's f_T measurement current is not recommended because at high currents and low voltages the transistor may be forced to operate in saturation as discussed in Section 5.3.1.

If f_α appears on the data sheet, the approximation $f_\alpha \simeq f_{T(max)}$ may be assumed.

Many manufacturers do not specifically list the f_T data but give instead the high frequency current gain h_{fe} and the frequency of measurement f. In such cases the designer assumes the measurement frequency is in a range where the equation $f_T = h_{fe} \cdot f$ applies, and calculates the f_T value from the given data. Usually the data shown are typical for the particular device type. If the minimum f_T value is listed, the designer should contact the manufacturer directly and obtain typical data; otherwise the prediction can be overly conservative. It is not uncommon for typical data to be a factor of 3 higher than minimum data.

Step 4 Predict the dc current gain using Steps 1-3 and equation (5-1)

$$h_{FE} = \frac{h_{FEO}}{1 + h_{FEO}\ t\ K\ \phi}$$

where the preradiation gain is estimated from the manufacturer's data sheet for the device.

5.4.2 Gain Prediction Using Measured Device Data and Mean Empirical Damage Factor

Step 1 Same as Step 1 in Section 5.4.1.

Step 2 Obtain the mean empirical damage factor K from the curve in Figure 5-2 (pages 5-5 and 5-6). For applications in steady-state radiation environments, estimate the effect on K of the ambient temperature during irradiation, from Figure 5-6 (page 5-13). The effect on K of current and voltage during irradiation is estimated from Figure 5-7 (page 5-14). If the radiation environment is from a weapon burst, the designer is advised not to reduce K due to the nominal operating conditions during irradiation by using the correction factors in Figures 5-6 and 5-7. Sander and Gregory[2] report that rapid annealing due to the operating conditions is still in progress 10^3 seconds after the radiation pulse. If circuits are required to function milliseconds or sooner after the pulse, make the gain prediction at the lowest operating current density using the passive value of K from Figure 5-2 with the correction factor from Figure 2-4 (page 2-11) for K for the proper operating temperature and time after burst.

Step 3 Measure each transistor individually and determine its base transit time from data of total delay time t' versus reciprocal emitter current at constant collector voltage and temperature. These measurements may be made either with the base transit time bridge instrumentation or with frequency response equipment, such as the General Radio Type 1607A Immittance Bridge described in Appendix A. Data should be taken at the same collector voltage with which each transistor will operate in the circuit. If at the voltage set by the circuit requirements, current is greater than the current to give minimum indication of base transit time (about $1/I_E < 0.1$ in Figure 5-1), the transistor will be operating in saturation

with the possibility of significant additional gain degradation. If the current and voltage levels cannot be changed and saturated operation is indicated, the designer may select a different transistor type with a larger area, which will reduce the current density; or a lower BV_{CBO}, which will reduce the collector resistivity; and thereby avoid operating in a saturation mode.

Step 4 Predict the dc current gain using Steps 1-3 and equation (5-1), where the preradiation gain h_{FEO} is measured at the operating current and voltage levels for the transistor, with the case temperature constant at the ambient temperature expected during operation. These measurements can be made with either a transistor curve tracer instrument or pulsed dc equipment.

5.4.3 Gain Prediction Using Measured Device Data and Device Type Empirical Damage Factor

Step 1 Same as Step 1 in Section 5.4.1.

Step 2 The most accurate prediction of gain is made using an empirical damage factor obtained experimentally on transistors of the same type and manufacture as those being used in the circuit. A sample size of five results in a typical coefficient of variation of 5 percent at normal operating currents, which is usually adequate. If possible the sample devices should be irradiated at the same operating conditions of current, voltage and temperature as exist in the circuit. If this is not practical, the devices may be passive during irradiation but with the measurements of h_{FE} made at the operating currents, voltages, and temperature. Corrections of the type indicated in Figures 5-6 and 5-7 can then be applied to the computed damage factor to include the effect of the operating conditions during irradiation. Determine the empirical damage factor from the gain degradation data using the relation

$$K = \frac{1}{t} \frac{\Delta(1/h_{FE})}{\Delta \phi} \qquad (5\text{-}5)$$

With an empirical device type damage factor, accurate prediction is possible even at high currents where the transistor may be operating in saturation. However, the designer must be consistent and make the gain measurements for the K determination at the same current, voltage, and ambient temperature as exist in the circuit. If he uses the constant low level base transit time to represent the device base characteristics, the effect of the operating conditions

will be reflected in the empirical K determined with equation (5-5). This will reduce errors in prediction of the type indicated in Figures 5-4 and 5-5 at high current.

At low operating currents prediction accuracy is also improved. For current levels where the gain degradation is dominated by recombinations in the emitter transition layer, $1/h_{FE}$ correlates very well with t, particularly for devices of the same type and manufacture. Only at very low currents, where surface effects degradation of h_{FE} varies between devices, is accurate prediction difficult.

Step 3 — Same as Step 3 in Section 5.4.2.

Step 4 — Same as Step 4 in Section 5.4.2.

5.5 SAMPLE GAIN PREDICTION (MANUFACTURER'S TYPICAL DEVICE DATA)

Given: Fairchild 2N1613 transistor

$\phi = 1.1 \times 10^{14}$ RDU

$T = 35°C$

Required: h_{FE} for I_E = 1, 10, 30 and 100 mA at V_{CE} = 5 volts where a transistor is assumed to be operating at each current.

Step 1 — A photomicrograph of the top surface of a similar Fairchild 2N1613 transistor indicates a circular emitter geometry with a 15 mil diameter. This information was confirmed by data from the manufacturer (see Figure 4-3). The emitter area is therefore

$$(\pi/4)(15 \times 10^{-3})^2(2.54)^2 = 1.14 \times 10^{-3} cm^2$$

Step 2 — The mean empirical damage factors are obtained from Figure 5-2 (pages 5-5 and 5-6).

I_E(mA)	J_E(A/cm^2)	K(10^{-6}/RDU-s)
1	0.88	2.78
10	8.8	1.48
30	26.4	1.12
100	88	0.885

The effect on K, of the operating conditions of current and temperature are neglected for a steady-state radiation environment, since these corrections are small compared with the errors resulting from the use of typical device data. For a weapon environment, K should be increased using the correction factors in Figure 2-4 (page 2-11).

Step 3 From the manufacturer's data sheet for the 2N1613 transistor, typical high frequency current gain at f = 20 MHz is 4. Hence

$$f_{T(max)} \approx h_{fe}\, f = (4)(20) = 80 \text{ MHz}$$

The manufacturer's measurement conditions for $f_{T(max)}$ were I_C = 50 mA and V_{CE} = 10 volts. These conditions suggest that at the required operating current and voltage of I_E = 100 mA and V_{CE} = 5 volts, the transistor may be operating in saturation with both emitter-base and collector-base junctions forward-biased. This will be established as true or false when the measured transit time for the specific device is determined as shown in Section 5.6. Although the designer is advised to avoid operation in saturation, particularly for a nonepitaxial transistor, as discussed for Figure 5-4, the gain prediction includes this high current point in order to illustrate the prediction techniques.

Step 4 The preradiation current gain data are obtained from the manufacturer's data sheet for an ambient temperature of 25°C and V_{CE} = 10 volts. These measurement conditions are sufficiently like the required conditions to be directly applicable since h_{FEO} is not a sensitive factor in the prediction equation.

I_C(mA)	h_{FEO}
1	65
10	80
30	85
100	82

From equation (5-1)

$$h_{FE} = \frac{h_{FEO}}{1 + h_{FEO}\, t\, K\, \phi}$$

and the data in the preceding steps, the predicted gains are

I_E(mA)	Predicted h_{FE}	Predicted h_{FE} (K = 10^{-6}/RDU-s)	Measured h_{FE}
1	1.6	4.2	2.5
10	3.0	4.3	4.9
30	3.9	4.3	5.5
100	4.8	4.3	6.2

The third column gives the predicted gains when A_E is not known and the approximate value of K is 10^{-6}/RDU-s. The negligible influence of accurate h_{FEO} data when significant gain degradation has occurred is evident. The test transistor was irradiated passively. Note that for an application in a steady-state radiation environment, the measured h_{FE} data would be slightly higher for I_E = 30 mA and 100 mA, in accordance with the data in Figure 5-7. For a weapon application and times less than 10^3 seconds after the burst, the above measured and predicted h_{FE} values would be decreased by the fast anneal correction factors given in Figure 2-4 (page 2-11) that are applied to K.

5.6 SAMPLE GAIN PREDICTION (MEASURED DEVICE DATA AND MEAN EMPIRICAL DAMAGE FACTOR)

Given: Fairchild 2N1613 transistor

$\phi = 1.1 \times 10^{14}$ RDU

T = 35°C

Required: h_{FE} for I_E = 1, 10, 30 and 100 mA at V_{CE} = 5 volts where a transistor is assumed to be operating at each current.

Step 1 In Section 5.5 the physical emitter area of the Fairchild 2N1613 transistor was determined as $1.14 \times 10^{-3} cm^2$.

Step 2 For applications where passive irradiation data should be employed, the mean empirical damage factors are obtained from Figure 5-2 (pages 5-5 and 5-6).

I_E(mA)	J_E(A/cm^2)	K(10^{-6}/RDU-s)
1	0.88	2.78
10	8.8	1.48
30	26.4	1.12
100	88	0.885

For applications in a steady-state radiation environment it is necessary to reduce K using data from Figure 5-7 (page 5-14). The operating currents of 30 mA and 100 mA are affected. The operating junction temperature T_j is determined from the values of operating current and voltage. For V_{CE} = 5 volts, the power dissipated at the transistor chip is approximately

$$I_E = 100 \text{ mA}: \quad V_{CE} I_C = (5)(100) = 500 \text{ mW}$$

$$I_E = 30 \text{ mA}: \quad V_{CE} I_C = (5)(30) = 150 \text{ mW}$$

From the manufacturer's data sheet the junction-to-ambient thermal resistance is 4.56 mW/°C. Since the ambient temperature is 35°C, the junction temperatures are

$$T_j = 35 + 500/4.56 = 145°C \qquad (J_E = 88 \text{ A/cm}^2)$$

$$T_j = 35 + 150/4.56 = 68°C \qquad (J_E = 26.4 \text{ A/cm}^2)$$

Hence, from Figure 5-7, K is reduced approximately 19 percent at 100 mA and about 8 percent at 30 mA. Since the experimental test transistor was irradiated passively, these corrections for K were not introduced into the prediction calculations below.

Step 3 The base transit time for the test transistor is 1.19 ns, determined from measured data at V_{CE} = 5 volts and T = 35°C using methods discussed in Appendix A. The data are shown in Figure 5-8. Note that the transistor will be operating in saturation at V_{CE} = 5 volts for currents above 50 mA (minimum t', $1/I_E$ = 0.02 in Figure 5-8). Although this transistor should not be operated in a neutron radiation environment at currents above 50 mA, the 100 mA point is retained to illustrate the prediction technique.

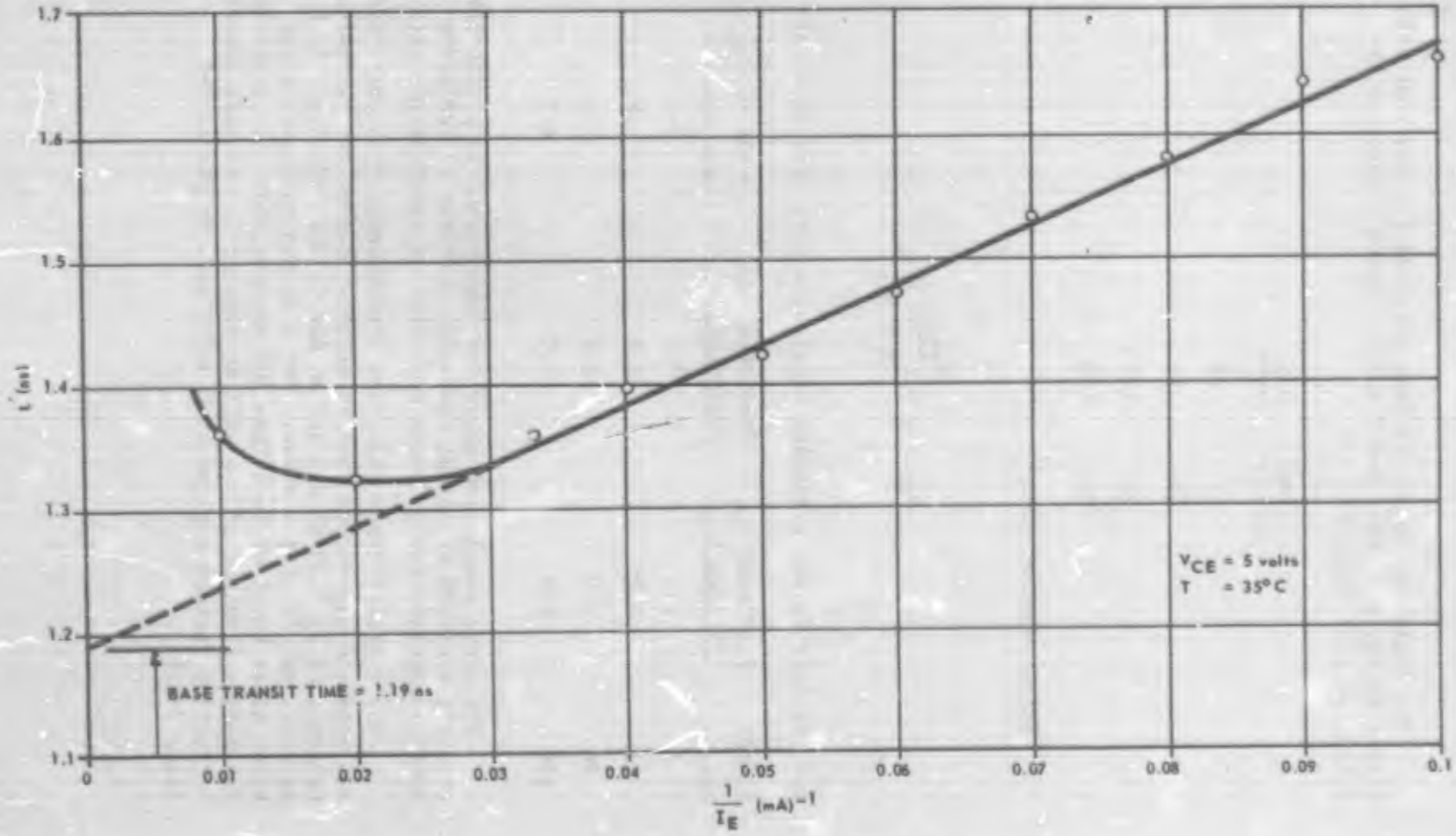


Figure 5-8. Base transit time data for test 2N1613 transistor

Step 4 The following h_{FEO} data were obtained for the test transistor at V_{CE} = 5 volts and T = 35°C, using a Birtcher Type 70 pulsed dc test instrument:

I_C(mA)	h_{FEO}
1	66
10	97
30	102
100	100

Using equation (5-1)

$$h_{FE} = \frac{h_{FEO}}{1 + h_{FEO}\, t\, K\, \phi}$$

and the data in the preceding Steps, the predicted gains are

I_E(mA)	Predicted h_{FE} (Typical t)	Predicted h_{FE} (Measured t)	Measured h_{FE}
1	1.6	2.6	2.5
10	3.0	4.9	4.9
30	3.9	6.4	5.5
100	4.8	8.0	6.2

The above tabulation shows the improvement in prediction accuracy achieved at normal operating currents by replacing typical manufacturer's device data with measured device data.

For a steady-state radiation environment, both the predicted and measured h_{FE} values will be slightly higher for operating currents of I_E = 30 mA and 100 mA due to the reductions in K as discussed in Step 2 above. For a weapon environment and times after burst of less than 10^3 seconds, both the predicted and measured values of h_{FE} will be reduced by the fast anneal correction factors applied to K using data in Figure 2-4 (page 2-11).

5.7 SAMPLE GAIN PREDICTION (MEASURED DEVICE DATA AND TYPICAL DEVICE TYPE DAMAGE FACTOR)

Given: Fairchild 2N1613 transistor

$\phi = 1.1 \times 10^{14}$ RDU

$T = 35°C$

Required: h_{FE} for I_E = 1, 10, 30 and 100 mA at V_{CE} = 5 volts where a transistor is assumed to be operating at each current.

Step 1 In Section 5.5 the physical emitter area of the Fairchild 2N1613 transistor was determined as 1.14×10^{-3} cm^2.

Step 2 From a passive irradiation test of other Fairchild 2N1613 transistors, performed at T = 35°C and with V_{CE} = 5 volts, the following empirical damage factors were computed from the gain degradation data and measured individual transit times using equation (5-5).

$$K = \frac{1}{t} \frac{\Delta(1/h_{FE})}{\Delta \phi}$$

and averaging the K values for the transistors at the fixed emitter currents:

I_E(mA)	$K(10^{-6}$/RDU-s)
1	2.86
10	1.42
30	1.23
100	1.13

Step 3 In Section 5.6 the measured base transit time of the transistor was determined as 1.19 ns.

Step 4 The following h_{FEO} data were obtained for the test transistor at V_{CE} = 5 volts and T = 35°C, using a Birtcher Type 70 pulsed dc test instrument:

I_C(mA)	h_{FEO}
1	66
10	97
30	102
100	100

Using equation (5-1)

$$h_{FE} = \frac{h_{FEO}}{1 + h_{FEO}\ t\ K\ \phi}$$

and data in the preceding steps, the predicted gains are

I_E(mA)	Predicted h_{FE}	Measured h_{FE}
1	2.6	2.5
10	5.1	4.9
30	5.9	5.5
100	6.3	6.2

The predicted error for each of the operating currents is less than 10 percent. This is a reasonable goal with this technique when careful measurements are made for the damage factor determination, the base transit times, and the radiation exposure using radiation damage monitors.

Since the test transistor was irradiated passively, both the predicted and measured h_{FE} values will be slightly higher for operating currents of I_E = 30 mA and 100 mA due to the reductions in K as discussed in Section 5.6, Step 2, for steady-state radiation environments. Because the device type K value is experimentally determined in Step 2 of this section, in some instances irradiating the transistors actively at the required operating conditions may be more desirable than applying correction factors to passively determined K values. The discussions in Section 5.5 and 5.6 for a weapon environment application also apply in this section.

The sample calculation of Section 5.6 shows that at I_E = 100 mA the transistor operates in saturation. A predicted gain of 8.0 compared to a measured gain of 6.2 was obtained using a mean empirical damage factor based on 21 different n-p-n transistor types. The higher predicted gain agrees with similar data previously discussed in Figures 5-4 and 5-5 and shows the spread that can be expected with this procedure when the transistor operates in saturation at high currents. However, when a specific device type K is used, as in the above sample calculation, the predicted gain is 6.3. This illustrates the improvement that can be achieved with a more precise analog using an empirical damage factor based on similar transistors, operating conditions and an equivalent or higher radiation exposure. Note that operation in saturation should normally be avoided because of poor prediction accuracy when the radiation exposure and/or operating current are sufficient to cause the transistor to operate in a range where the gain falls sharply with increasing current, as shown in Figure 5-4 at high currents. This did not occur in the above example because the gain after irradiation was still increasing with current.

SECTION 5 - REFERENCES

1. M. Frank, "Development of a Non-Destructive Radiation Effects Prediction Technique," Contract AF 29(601)-7110, Fourth Quarterly Progress Letter for the Period Ended December 31, 1966, BRLD 3841.

2. H. H. Sander and B. L. Gregory, "Transient Annealing in Semiconductor Devices Following Pulsed Neutron Irradiation," IEEE Trans on Nuclear Science, NS-13, 53-62, December 1966.

SECTION 6

PREDICTION OF OTHER TRANSISTOR PERFORMANCE PARAMETERS

6.1 SATURATION VOLTAGE

6.1.1 Prediction Procedure for Collector-Emitter Saturation Characteristic

The transistor is defined to be operating in a voltage saturation mode when both the emitter-base and collector-base junctions are forward-biased. When the emitter-base junction is forward-biased and the collector-base junction is reverse-biased, the transistor operates in its normal or active state. At the present time accurate prediction cannot be made of the complete voltage saturation characteristics. It is possible, however, to accurately predict the base current I_B, where the transistor changes from a saturated to an active operating state. If the preradiation saturation characteristics are available, they can assist the designer in estimating the change in saturation voltage that will occur due to radiation.

The collector-emitter saturation voltage $V_{CE(SAT)}$ is composed of the following voltage drops:

$$V_{CE(SAT)} = V_{BE} - V_{CB} + I_E R_E + I_C R_B + I_C R_C \qquad (6\text{-}1)$$

Because the emitter is heavily doped, $I_E R_E \approx 0$ and can be neglected. Since the longitudinal resistance in the base R_B is usually very low, the voltage drop $I_C R_B$ can also be neglected. The net junction voltage $(V_{BE} - V_{CB})$ is small and changes little with base drive and with radiation. The voltage drop in the collector region depends on collector current and is of interest primarily when the collector current is high.

If the collector current is low, the change in $V_{CE(SAT)}$ with radiation is negligible, as long as the transistor is operated at a current-drive ratio I_C/I_B that is sufficiently low to allow it to remain in saturation after the radiation exposure. Since the current-drive ratio where the transistor comes out of saturation can be accurately predicted, changes in $V_{CE(SAT)}$ with radiation are not a problem at low collector currents.

If the collector current is high, the voltage drop in the collector $I_C R_C$ is the major component of $V_{CE(SAT)}$. Although the collector resistance is initially low, radiation reduces the minority carrier lifetime in the collector, which reduces the collector conductivity and

when the collector length W_c is large, the collector resistance can show a substantial increase, causing $V_{CE(SAT)}$ to increase proportionately. If the radiation exposure is sufficiently large to cause carrier removal effects, the collector resistance and $V_{CE(SAT)}$ will increase even more. The changes in the collector resistance cannot be predicted at this time, since these changes are influenced by a complex interaction of current crowding, changes in conductivity, and carrier removal. Consequently, in high current applications and where minimum $V_{CE(SAT)}$ must be maintained, it is recommended that the designer select a transistor having: (a) epitaxial construction to minimize W_c, (b) low BV_{CBO} to minimize resistivity, and (c) large junction areas. For such transistors a close estimate of the effect of radiation on $V_{CE(SAT)}$ can be made by using preradiation data and graphical construction.

The following procedure is employed in the prediction of $V_{CE(SAT)}$.

Step 1 Obtain preradiation data of V_{CE} as a function of base current at the constant collector operating current of the transistor. The range of I_B should extend from the level where the transistor comes out of saturation to the level where $I_B = I_C$. These data are taken at the operating ambient temperature of the device. A pulsed low duty cycle dc test instrument similar to the Birtcher Model 70 or Fairchild 500 should be used to make the $V_{CE(SAT)}$ measurements.

Step 2 Plot the data as shown in the examples of Figures 6-1 and 6-2. Draw lines tangent to the curve where the transistor is out of saturation and where it is in saturation. These lines intersect in point P.

Step 3 Determine the base current where the transistor comes out of saturation from the equation

$$I_B(post) = I_B(pre) + (t\ K\ \phi)\ I_C \qquad (6\text{-}2)$$

Here $I_B(pre)$ is the preradiation base current where the transistor comes out of saturation. The base transit time t may be determined from typical manufacturer's data as described in Section 5.4.1 for an approximate prediction of $I_B(post)$ or measured for the specific transistor as described in Appendix A and Section 5.2 for accurate $I_B(post)$ prediction. Similarly, for approximate prediction the empirical damage factor K may be taken from the mean data in Figure 5-2 (pages 5-5 and 5-6); or for accurate prediction of $I_B(post)$, K may be experimentally determined on transistors of the same type and manufacture, as described in Section 5.4.3.

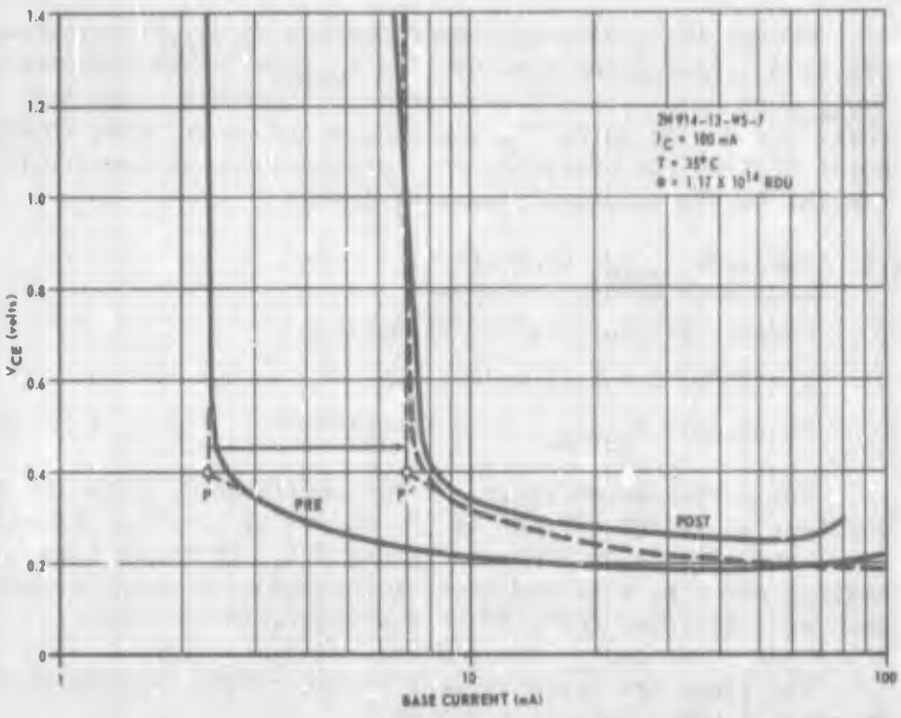


Figure 6-1. V_{CE} versus I_B for 2N914 transistor

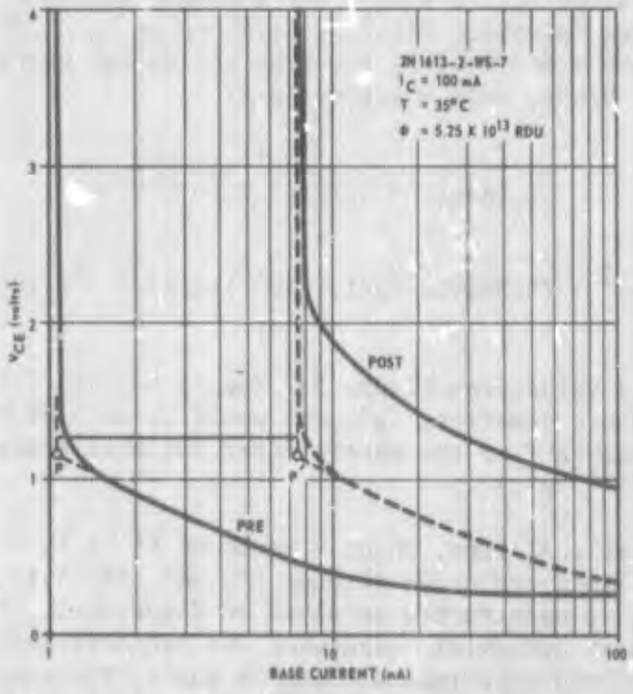


Figure 6-2. V_{CE} versus I_B for 2N1613 transistor

Step 4 Obtain the predicted post-radiation $V_{CE(SAT)}$ characteristic by displacing the preradiation $V_{CE(SAT)}$ characteristic from $I_{B(pre)}$ to $I_{b(post)}$ as illustrated in Figures 6-1 and 6-2. Point P moves to point P', the tangent lines are draw through point P', and the preradiation characteristic is constructed tangent to the parallel displaced lines.

6.1.2 Sample $V_{CE(SAT)}$ Prediction

Given: Fairchild 2N914 transistor

$T = 35°C$, $\phi = 1.17 \times 10^{14}$ RDU

Required: $V_{CE(SAT)}$ as a function of I_B for $I_C = 100$ mA

Step 1 The preradiation $V_{CE(SAT)}$ characteristic is obtained at a constant collector current of 100 mA and at constant temperature, and plotted as shown in Figure 6-1. To avoid junction heating effects, a pulsed dc test instrument should be used, such as a Birtcher Model 70 or a Fairchild Model 500.

Step 2 Two lines are drawn tangent to the curve that intersect in point P where $I_B(pre) = 2.3$ mA.

Step 3 The measured base transit time for the transistor, using methods discussed in Appendix A, is 0.358 ns. The empirical damage factor is 1.1×10^{-6}/RDU-s when experimentally determined from other Fairchild 2N914 transistors at $I_C = 100$ mA and $T = 35°C$, with t measured in the same way as the prediction sample device. Hence, from equation (6-2)

$$I_B(post) = I_B(pre) + (t\ K\ \phi)\ (I_C)$$

$$I_B(post) = 2.3\times10^{-3} + (0.358\times10^{-9})(1.1\times10^{-6})(1.17\times10^{14})(100\times10^{-3}) = 6.9\ mA$$

(If the K value from Figure 5-2 (pages 5-5 and 5-6) were used in the above equation, $I_B(post)$ would be at 5.63 mA. The emitter area obtained from the manufacturer for this transistor was 80.8×10^{-6} cm^2.)

Step 4 After radiation, point P moves to P' at $I_B = 6.9$ mA. The tangent lines are drawn through P', and the post-radiation $V_{CE(SAT)}$ is constructed as shown in Figure 6-1. The 2N914 transistor is an epitaxial transistor and the correlation between predicted and experimental data is good. The prediction of $V_{CE(SAT)}$ would be even better if another epitaxial transistor

could be selected with the same f_T and BV_{CBO}, but with a larger junction area. At 100mA the 2N914 is operating at a current density of 1240A/cm^2 when the current is assumed to flow over an area equivalent to the emitter area. Larger area would give less change in $V_{CE(SAT)}$ with radiation, due to resistance change. Figure 6-2 shows the same prediction procedure applied to a nonepitaxial 2N1613 transistor. Although accurate prediction of the base current where the transistor comes out of saturation is possible, the increase in $V_{CE(SAT)}$, which is primarily due to the increase in collector resistance, cannot be predicted as accurately.

6.1.3 Base-Emitter Saturation Characteristic

A prediction procedure for this parameter is not given because of the small change of the base-emitter saturation voltage $V_{BE(SAT)}$ induced by radiation. Figure 6-3 shows typical data of the effects of radiation on $V_{BE(SAT)}$ for a 2N1613 transistor.

6.2 FORWARD VOLTAGE

6.2.1 Prediction Procedure for Emitter-Base Forward Voltage

When the transistor is operating in its active state and at low operating currents, the forward base-emitter voltage V_{BE} changes very little with radiation. The small increase in voltage that occurs can be neglected. At moderate and at high operating current, however, the change in V_{BE} with radiation can be significant. Base current flowing under the emitter produces current crowding effects that normally cause V_{BE} to increase (ΔV) in excess of the value required by the ideal diode equation as shown in Figure 6-4. Radiation increases the base current, which intensifies current crowding as shown in Figure 5-3; consequently V_{BE} is based on the assumption that the same $I_B R_B$ voltage drop (ΔV), due to the base current and transverse base resistance, will occur before and after radiation at collector currents defined by the respective common emitter current gains of the transistor. This approximation is valid providing (ΔV) data are not taken from the high injection region of transistor operation, since at such currents the exponential dependence of the ideal curve changes from exp (q V_{BE}/kT) to exp (q V_{BE}/n kT) where n differs from unity.

The prediction procedure for V_{BE} involves the following sequence of steps

Step 1 Construct the ideal diode characteristic of log I_C versus V_{BE} from data obtained at low currents, where the voltage changes by approximately 61mV/decade of I_C at 35°C, and extrapolate the linear curve plotted in semilog form to about a decade or more above the desired operating level of I_C. The measuring circuit to use is shown in Appendix B.

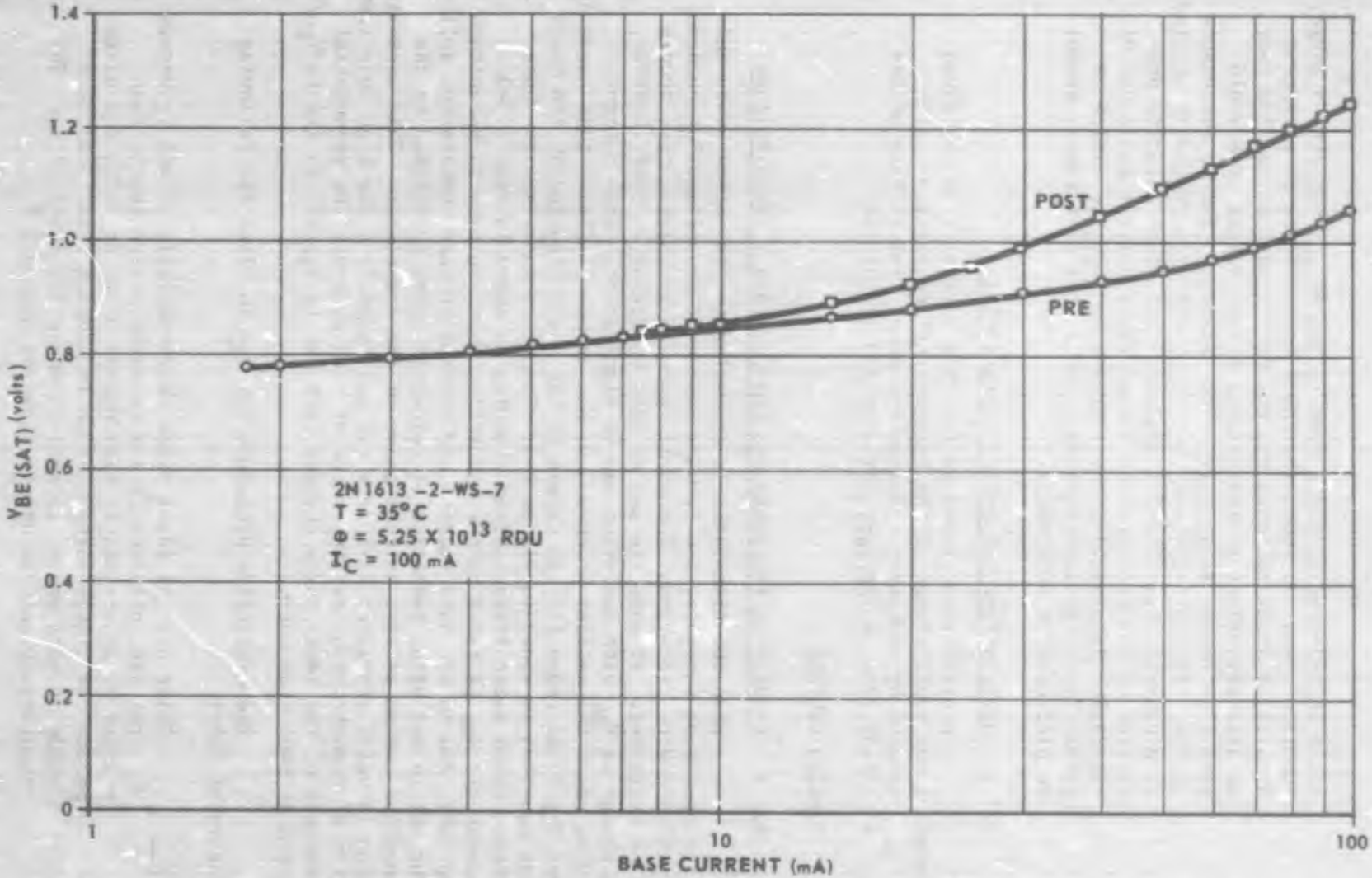


Figure 6-3. $V_{BE(SAT)}$ versus I_B for 2N1613 transistor

Step 2 Obtain the actual preradiation V_{BE} - I_C characteristic using a pulsed dc instrument to prevent junction heating at high currents. Reverse-bias the collector-base junction with a voltage sufficiently high to assure that the transistor is not operating in its saturation mode at the high collector currents. Take data to current levels a decade or more above the desired operating point. The case temperature of the transistor must be maintained constant during measurements because V_{BE} is very temperature-dependent.

Step 3 Estimate the base transit time from the manufacturer's data sheet or measure for the specific transistor according to the procedures given in Sections 5.4.1 or 5.2 respectively.

Step 4 Obtain data of h_{FEO} versus I_C at the desired operating V_{CE} and temperature using a pulsed dc test instrument.

Step 5 Obtain the empirical damage factors at a number of selected collector current levels, either from Figure 5-2 (pages 5-5 and 5-6) or experimentally for transistors of the same type and manufacturer, following the procedure of Section 5.4.3.

Step 6 Measure collector currents at each of the selected (ΔV) segments from the ideal curve to the actual preradiation curve, as shown in Figure 6-4. Construct each (ΔV) segment from the ideal curve to the predicted post radiation V_{BE} characteristic at the corresponding post radiation collector current given by the equation

$$I_C(\text{post}) = \frac{1}{1 + h_{FEO}\, t\, K\, \phi} \cdot I_C(\text{pre}) \qquad (6\text{-}3)$$

The empirical damage factor in Equation 6-3 pertains to the collector current level before radiation.

6.2.2 Sample Prediction for Emitter-Base Forward Voltage

Given: Fairchild 2N914 transistor

$$\phi = 4.8 \times 10^{14} \text{ RDU}, \quad T = 35°C$$

Required: V_{BE} for I_C from 8 mA to 50 mA

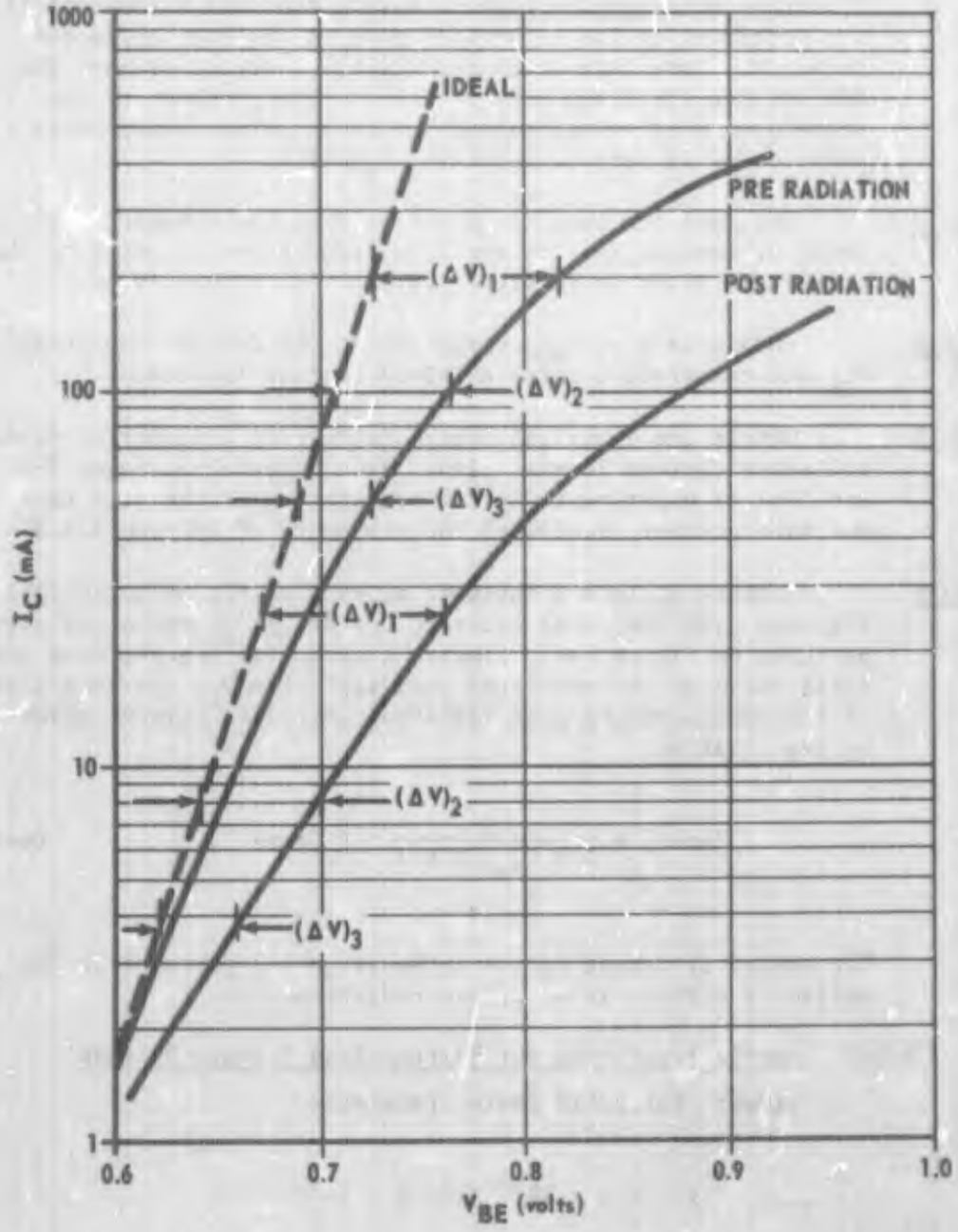


Figure 6-4. Prediction of forward voltage

Step 1 The ideal diode characteristic of log I_C versus V_{BE} is constructed from measured data for currents from 10^{-8} to 10^{-6} A and extrapolated to higher currents by following a slope of 61 mV/decade of I_C at 35°C. The plotted data are shown in Figure 6-5. The data were obtained using the circuit for low level V_{BE} measurements in Appendix B.

Step 2 The moderate to high current V_{BE} - I_C data were obtained for V_{CE} = 5 volts and T = 35°C and plotted in Figure 6-5. A Birtcher Model 70 pulsed dc instrument was used to make these measurements.

Step 3 With the methods discussed in Appendix A, the measured base transit time for the transistor was 0.202 ns.

Step 4 The measured h_{FEO} at V_{CE} = 5 volts and T = 35°C with a Birtcher Model 70 pulsed dc instrument were

I_C(mA)	200	100	50
h_{FEO}	41.2	57.5	72.9

Step 5 The emitter area obtained from the manufacturer for this transistor type is 80.8 x 10^{-6} cm^2. From Figure 5-2 (pages 5-5 and 5-6)

K(10^{-6}/RDU-s)	0.875	0.795	0.770
I_C(mA)	200	100	50

Step 6 From Figure 6-5 (ΔV) is measured at I_C(pre) of 200, 100 and 50 mA. Equation 6-3 is used with data from Steps 3, 4 and 5 to calculate I_C(post). The computed results are

I_C(pre) (mA)	ΔV (mV)	I_C(post) (mA)
200	105	44.6
100	62	18.4
50	37	7.77

The post radiation V_{BE} at I_C(post) are obtained by adding the corresponding ΔV to the ideal curve as shown in Figure 6-5.

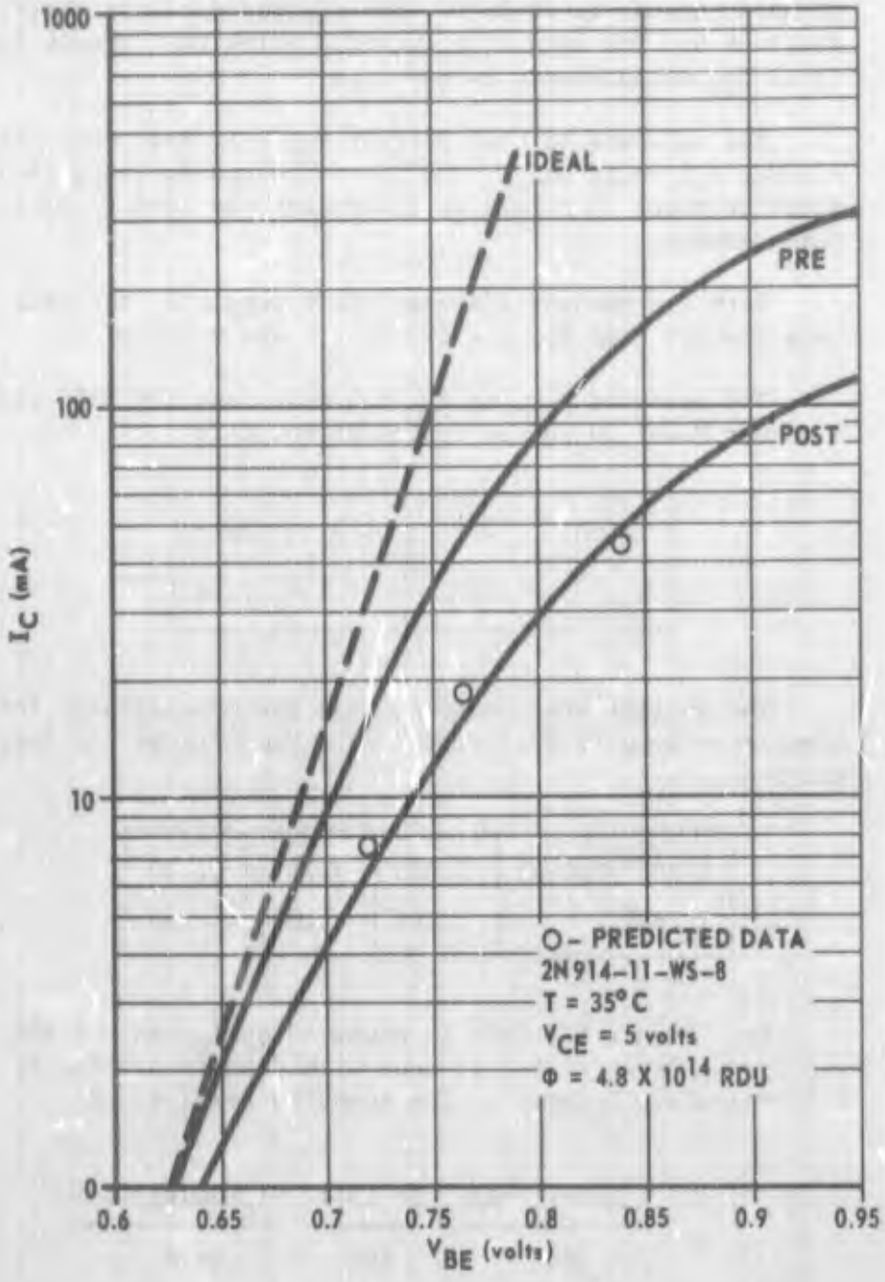
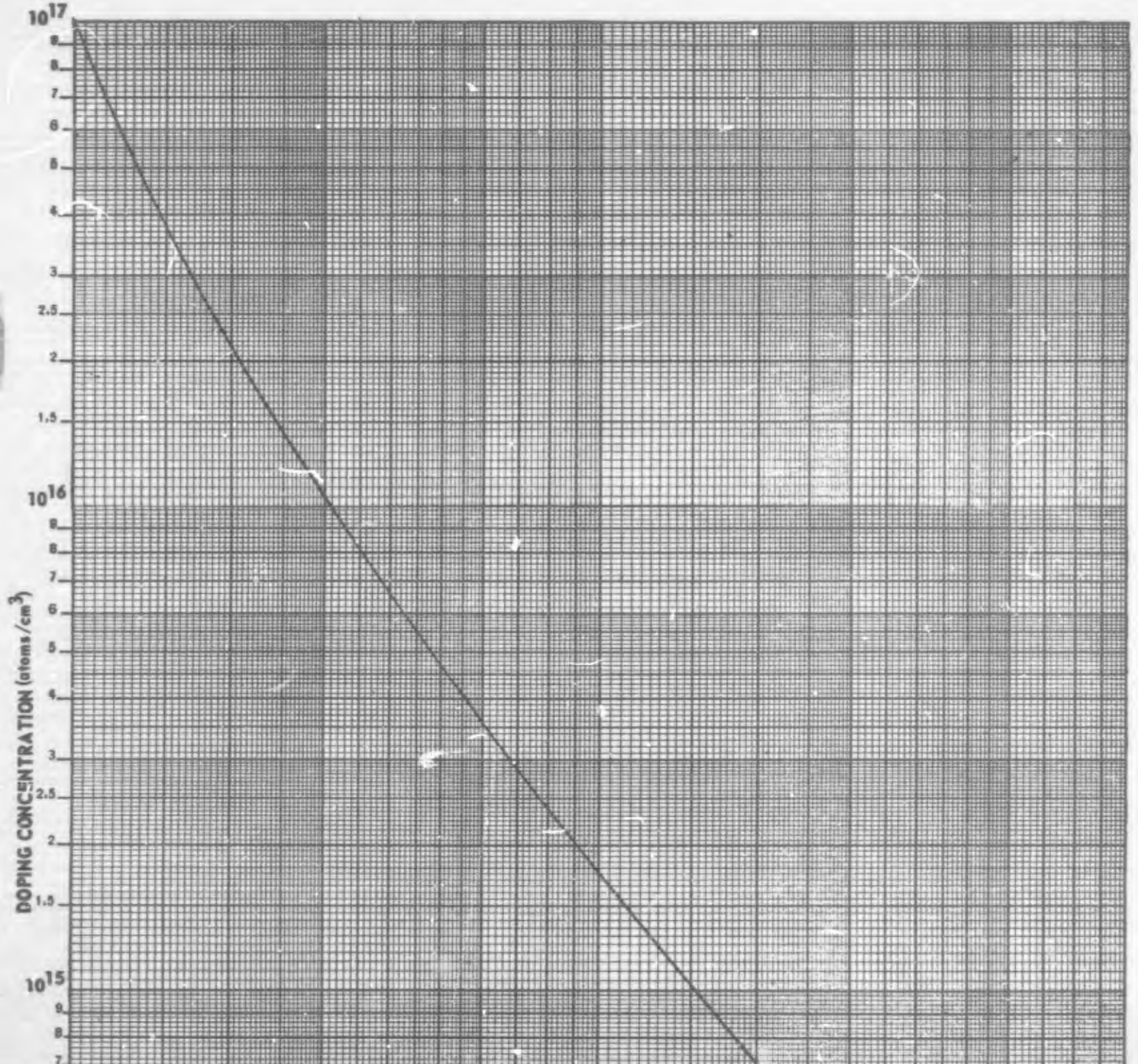


Figure 6-5. I_C versus V_{BE} for 2N914 transistor


DOPING CONCENTRATION (atoms/cm³)
10¹⁷
10¹⁶
10¹⁵

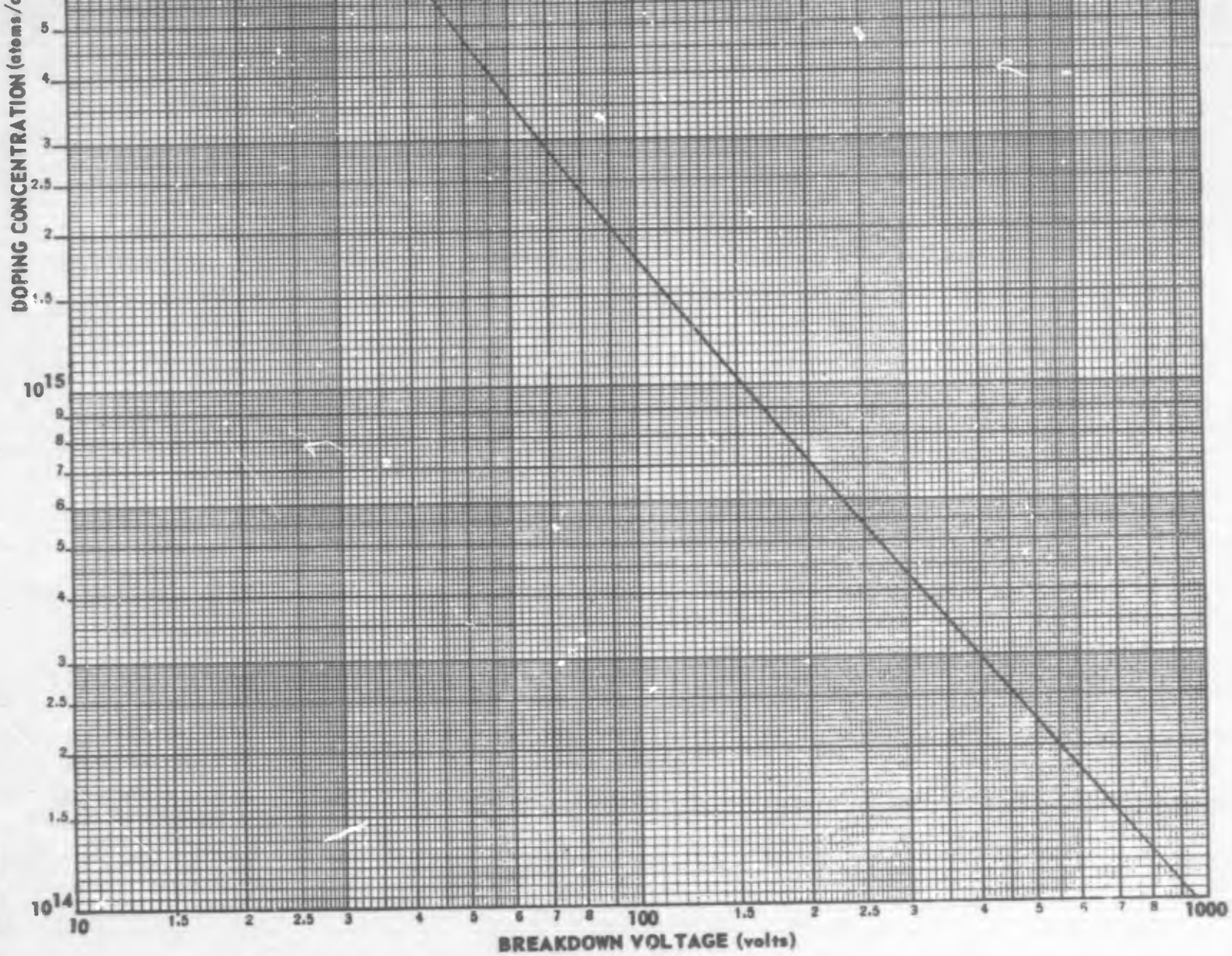


Figure 6-6. Doping concentration versus junction breakdown voltage (source: Reference 1)

6.3 JUNCTION BREAKDOWN VOLTAGE

6.3.1 Prediction Procedure for Junction Breakdown Voltage

The avalanche breakdown voltage of a semiconductor junction increases with radiation exposure. Carrier removal effects increase the resistivity of the material, and the junction is able to withstand a higher voltage before breaking down. Consequently, an approximate prediction of this performance parameter is generally sufficient for the circuit designer.

Obtain the preradiation doping concentration N_o in the lightly doped side of the junction, which determines junction breakdown, either from direct contact with the manufacturer, from capacitance measurements at the junction (Appendix B), or from data of measured breakdown voltage (BV_{CBO}) and Figure 6-6. This figure is based on abrupt junction[1] data with the voltage breakdown associated with the lightly doped region. For transistors, any changes in breakdown voltage with radiation usually occur at the collector junction, since the emitter and base regions are generally heavily doped; hence, other transistor performance parameters fail before the emitter breakdown voltage is affected. For epitaxial and nonepitaxial planar and mesa type transistors, the collector is lightly doped in comparison with the base, and the assumption of an abrupt junction is valid. Figure 6-6 gives an approximate determination of N_o because the breakdown voltage depends not only on doping but also on the radius of curvature at the edges of the junction and on whether the junction corners are cylindrical or spherical in shape.[2] Hence, the breakdown voltage-doping concentration data cannot be represented by a single curve. However, for the breakdown voltage computations, Figure 6-6 is adequate. The following prediction procedure is employed:

Step 1 — Experimentally measure the junction breakdown voltage before radiation at a sufficiently high reverse current to assure that bulk avalanche breakdown is occurring and not some surface phenomenon.

Step 2 — From Figure 6-5 obtain the doping concentration of the lightly doped side of the junction N_o, using the measured breakdown voltage from Step 1. An alternate approach to finding N_o is to use junction capacitance measurements as described in Appendix B.

Step 3 — Compute the post-radiation doping concentration N using empirically derived carrier removal coefficients in the equation

$$N = N_o - K_N' \phi \qquad (6\text{-}4)$$

where $K_N' = 0.5$ carrier/cm^3-RDU for a radiation exposure of $\phi = (0.1 \text{ RDU-cm}^3)\ (N_o)$ and $K_N' = 0.2$ carrier/cm^3-RDU for a radiation exposure of $\phi = (0.75 \text{ RDU-cm}^3)\ (N_o)$. Since K_N' is based on limited data, the designer must extrapolate or interpolate the above coefficients for different radiation exposures. Note that K_N', the carrier removal coefficient within the junction transition layer, differs from K_N, the carrier removal coefficient external to the junction transition layer.

Step 4 Estimate the breakdown voltage after radiation from Figure 6-5 using N from Step 3.

6.3.2 Sample Prediction of Junction Breakdown Voltage

Given: Fairchild transistors

2N1613-1, $\phi = 1.1 \times 10^{14}$ RDU

2N1613-2, $\phi = 9.7 \times 10^{14}$ RDU

Required: Collector-base breakdown voltage for each transistor

Step 1 The measured preradiation BV_{CBO} at $I_{CBO} = 1$ mA was 115 volts for each transistor. The measurements were made with a Tektronix Type 575 Curve Tracer.

Step 2 From Figure 6-5, $N_o = 1.46 \times 10^{15}/cm^3$ for each transistor.

Step 3 The post-radiation N is determined using Equation 6-4. For transistor 2N1613-1, where $\phi = 1.1 \times 10^{14}$ RDU, $K_N' = 0.5$, since $0.1\ N_o = (0.1)\ (1.46 \times 10^{15}) = 1.46 \times 10^{14} \approx 1.1 \times 10^{14}$ RDU.

Thus,

$$N = N_o - K_N' \phi = 1.46 \times 10^{15} - (0.5)\ (1.1 \times 10^{14}) = 1.405 \times 10^{15}/cm^3$$

For transistor 2N1613-2, where $\phi = 9.7 \times 10^{14}$ RDU, $K_N' = 0.2$, since $0.75\ N_o = (0.75)\ (1.46 \times 10^{15}) = 1.1 \times 10^{15} \approx 0.97 \times 10^{15}$ RDU.

Thus,

$$N = N_o - K_N' \phi = 1.46 \times 10^{15} - (0.2)\ (9.7) \times 10^{14} = 1.266 \times 10^{15}/cm^3$$

Step 4 With N from Step 3, the predicted BV_{CBO} voltages from Figure 6-5 are

2N1613-1, BV_{CBO} = 118 volts (Measured BV_{CBO} = 118 volts)

2N1613-2, BV_{CBO} = 128 volts (Measured BV_{CBO} = 128 volts)

6.4 COLLECTOR-TO-EMITTER BREAKDOWN VOLTAGE

6.4.1 Prediction Procedure for Collector-to-Emitter Breakdown Voltage

The collector-to-emitter breakdown voltage BV_{CEO}, sometimes referred to as the sustaining voltage, increases with radiation exposure due to carrier removal effects which increase avalanche junction breakdown voltage, and minority carrier lifetime degradation in the base which decreases current gain. The avalanche voltage BV_{CEO} is defined by the equation

$$BV_{CEO} = \frac{BV_{CBO}}{(1 + h_{FE})^{\frac{1}{n}}} \qquad (6\text{-}5)$$

where n is an empirical constant. Therefore BV_{CEO} increases with BV_{CBO} and approaches BV_{CBO} as h_{FE} degrades to zero. Since the BV_{CEO} performance parameter improves with radiation, an approximate prediction of this variable will suffice for most applications. The following procedure may be used to predict BV_{CEO}.

Step 1 Measure BV_{CBO} at a sufficiently high I_{CBO} to assure true avalanche breakdown of the base collector junction.

Step 2 Measure BV_{CEO} at the desired I_{CEO} level.

Step 3 Measure h_{FEO} at the operating current level corresponding to I_{CEO}.

Step 4 Using the data from Steps 1, 2 and 3, empirically determine n from the equation

$$n = \frac{\ln\left(1 + h_{FEO}\right)}{\ln\left(\frac{BV_{CBO}}{BV_{CEO}}\right)} \qquad (6\text{-}6)$$

Step 5 Predict the post-radiation BV_{CBO} using the procedure of Section 6.3.

Step 6 Predict h_{FE} after radiation at the I_{CEO} current level using any of the gain prediction methods of Section 5.

Step 7 Using n from Step 4, BV_{CBO} from Step 5, and h_{FE} from Step 6, predict the post-radiation BV_{CEO} at the current level I_{CEO} by solving Equation 6-5.

6.4.2 Sample Prediction of Collector-to-Emitter Breakdown Voltage

Given: Fairchild 2N1613 transistor

$$\phi = 1.1 \times 10^{14} \text{ RDU}$$

Required: Collector-to-emitter breakdown voltage

Step 1 The measured preradiation BV_{CBO} at I_{CBO} = 1 mA was 115 volts. This measurement was made with a Tektronix Type 575 curve tracer.

Step 2 At I_{CEO} = 50 mA, the measured preradiation BV_{CEO} was 45.5 volts as determined from a Tektronix Type 575 curve tracer.

Step 3 The measured h_{FEO} at V_{CE} = 5 volts, T = 35°C, and $I_E \simeq I_C$ = 50 mA was 100. This measurement was made with a Birtcher Type 70 pulsed dc instrument.

Step 4 From Equation 6-6

$$n = \frac{\ln(1 + h_{FEO})}{\ln\left(\frac{BV_{CBO}}{BV_{CEO}}\right)} = \frac{\ln(1 + 100)}{\ln\left(\frac{115}{45.5}\right)} = 4.97$$

Step 5 Since the BV_{CEO} prediction is being made for the same transistor and radiation exposure as given in Section 6.3, the post-radiation predicted BV_{CBO} is 118 volts.

Step 6 From Figure 5-2 (pages 5-5 and 5-6) at $J_E = 43.9$ A/cm^2 (A_E of 2N1613 transistor is 1.14×10^{-3} cm^2), $K = 10^{-6}$/RDU-s. Using methods discussed in Appendix A, the measured base transit time of the transistor is 1.12ns. From Equation 5-1 the post-radiation gain is

$$h_{FE} = \frac{h_{FEO}}{1 + h_{FEO}\, t\, K\, \phi} = \frac{100}{1 + (100)\,(1.12 \times 10^{-9})\,(10^{-6})\,(1.1 \times 10^{14})} = 7.52$$

Step 7 From Equation 6-5 the predicted BV_{CEO} is

$$BV_{CEO} = \frac{BV_{CBO}}{(1 + h_{FE})^{\frac{1}{n}}} = \frac{118}{(1 + 7.52)^{\frac{1}{4.97}}} = 76.6 \text{ volts}$$

The measured post-radiation BV_{CEO} for this device was 68 volts at $I_{CEO} = 50$ mA.

6.5 JUNCTION LEAKAGE CURRENT

6.5.1 Prediction Procedure for Junction Leakage Current

When the surface leakage current at a silicon semiconductor junction is negligible, the reverse current I_R that is measured at approximately room temperature is essentially the current produced by carrier generation in the transition layer volume. For devices where the change in the surface leakage current with radiation is appreciable, the total reverse current cannot be predicted. In environments where the neutron/gamma ratio is $\geq 10^8 \frac{n/cm^2}{R}$, the increase in the surface leakage current is ignored and the change in the reverse current ΔI_R at reverse junction voltage V_j is described by the equation

$$\Delta I_R = q\,[\text{Junction transition layer volume}]\,[\text{Carrier generation rate}]$$

$$= q\,[A_j\, W_j]\,[n_i\, K_{rg}\, \phi] = (\text{Constant})\,\frac{A_j^2}{C_j}\,\phi \qquad (6\text{-}7)$$

where q is electronic charge; A_j is the area of the junction; W_j is the width of the junction, which is determined from the measured capacitance at the junction C_j at voltage V_j; n_i is the intrinsic carrier concentration; K_{rg} is the radiation damage coefficient for recombination and generation of carriers in the junction transition layer; and ϕ is the fluence. When the area is expressed in square centimeters, the capacitance in farads and the fluence in RDU, then at 35°C

$$\Delta I_R = \frac{A_j^2}{C_j} \cdot \phi \cdot 10^{-28} \text{ (amperes)} \qquad (6\text{-}8)$$

If the semiconductor material is gold-doped or contains radiation induced defect sites, the measured capacitance is frequency-sensitive when measured at frequencies below 100kHz.[3] Junction capacitance measurements should be performed at signal frequencies above 100kHz for devices that are gold-doped. A second junction capacitance effect, which is an important consideration in prediction, is the difference in characteristics between planar and mesa type transistor constructions. To circumvent this problem the correction factor curve shown in Figure 6-7 has been derived to empirically correlate the difference in measured capacitance as a function of reverse voltage between planar and mesa device types. These data were experimentally obtained for Fairchild 2N1613 transistors and RCA 2N3439 transistors. To predict the reverse current at a given reverse voltage V_j, Equation 6-8 is multiplied by the correction factor of Figure 6-7 for the given reverse voltage. The steps in predicting ΔI_R are

Step 1 — Obtain the junction area A_j either directly from the manufacturer or from photomicrographs on similar devices of the same type and manufacture.

Step 2 — Measure junction capacitance C_j at the desired reverse junction voltage (See Appendix B for measurement procedure). An estimate of C_j can be made by measuring the junction breakdown voltage, determining the doping concentration N_o from Figure 6-6 (page 6-12) and solving the step junction equation

$$C_j = A_j \sqrt{\frac{q \varepsilon N_o}{2(V_T + V_j)}} = A_j \sqrt{\frac{8.28 \times 10^{-32} N_o}{(V_T + V_j)}} \qquad (6\text{-}9)$$

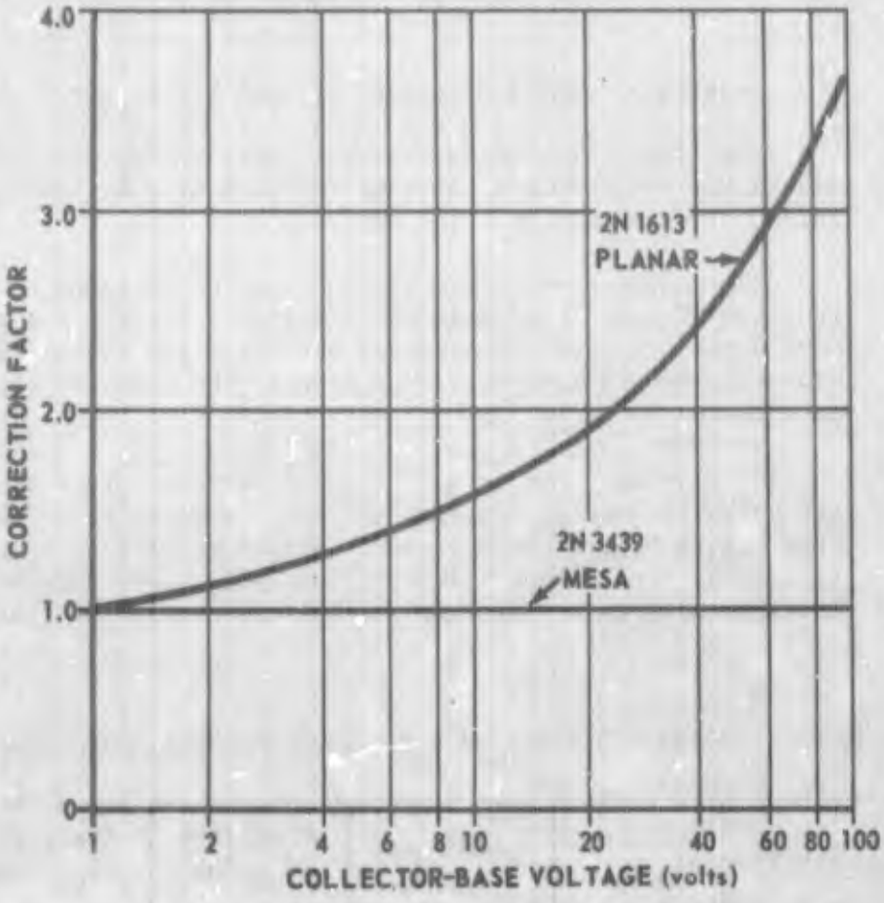


Figure 6-7. Correction factor as a function of reverse voltage

where V_T = junction built-in potential and is approximately 0.6 to 0.8 volt for silicon transistors. The latter method for determining capacitance is suitable for gold-doped transistors where junction capacitance is frequency-sensitive. The effects of carrier removal are not included in Equation 6-9.

Step 3 Compute the reverse current using Equation 6-8, if the device is a mesa type. If the device is of planar construction, multiply Equation 6-8 by a correction factor taken from Figure 6-7.

6.5.2 Sample Prediction of Junction Leakage Current

Given: Fairchild 2N1613 transistor

$$\phi = 2.14 \times 10^{14} \text{ RDU}, \quad T = 35°C$$

Required: Junction leakage current for V_{CBO} = 1 to 100 volts

Step 1 The area of the collector-base junction for the 2N1613 transistor obtained from photomicrographs of other Fairchild 2N1613 devices is $4.56 \times 10^{-3} cm^2$.

Step 2 The collector-base transition layer capacitance as a function of reverse voltage was obtained following the measurement procedure given in Appendix B. The stray capacitance was measured and subtracted out to give the junction capacitance data listed in Table 6-1.

Step 3 The reverse currents at the collector-base junction I_{CBO} are calculated using Equation 6-8 and the correction factors from Figure 6-7, since the sample device is of planar construction. The results are shown in Table 6-1. The measured leakage currents are also listed for comparative purposes.

Table 6-1. Reverse current as a function of reverse voltage

V_{CBO}(volts)	C_{TC}(pF)	Correction factor	Predicted ΔI_{CBO}(nA)	Measured ΔI_{CBO}(nA)
1	28.22	1.0	15.8	16.8
2	23.61	1.20	22.6	24.1
5	17.83	1.35	33.7	34.9
10	13.91	1.60	51.2	58.3
20	10.49	1.85	78.6	88.5
30	8.79	2.15	109	116
50	7.04	2.65	168	170
80	5.88	3.30	250	265
100	5.05	3.65	322	355

6.6 SWITCHING TIMES

The transistor switching times are described by a turn-on time and a turn-off time. The turn-on time consists of a delay time t_d and a rise time t_r. The turn-off time consists of a storage time t_s and a fall time t_f. These times are illustrated in typical waveforms shown in Figure 6-8.

After the turn-on voltage is applied, base current flows to change the voltages across the emitter and collector junctions. The delay time is the time these junction voltages take to readjust to the point where they change the transistor from a cutoff operating mode with both

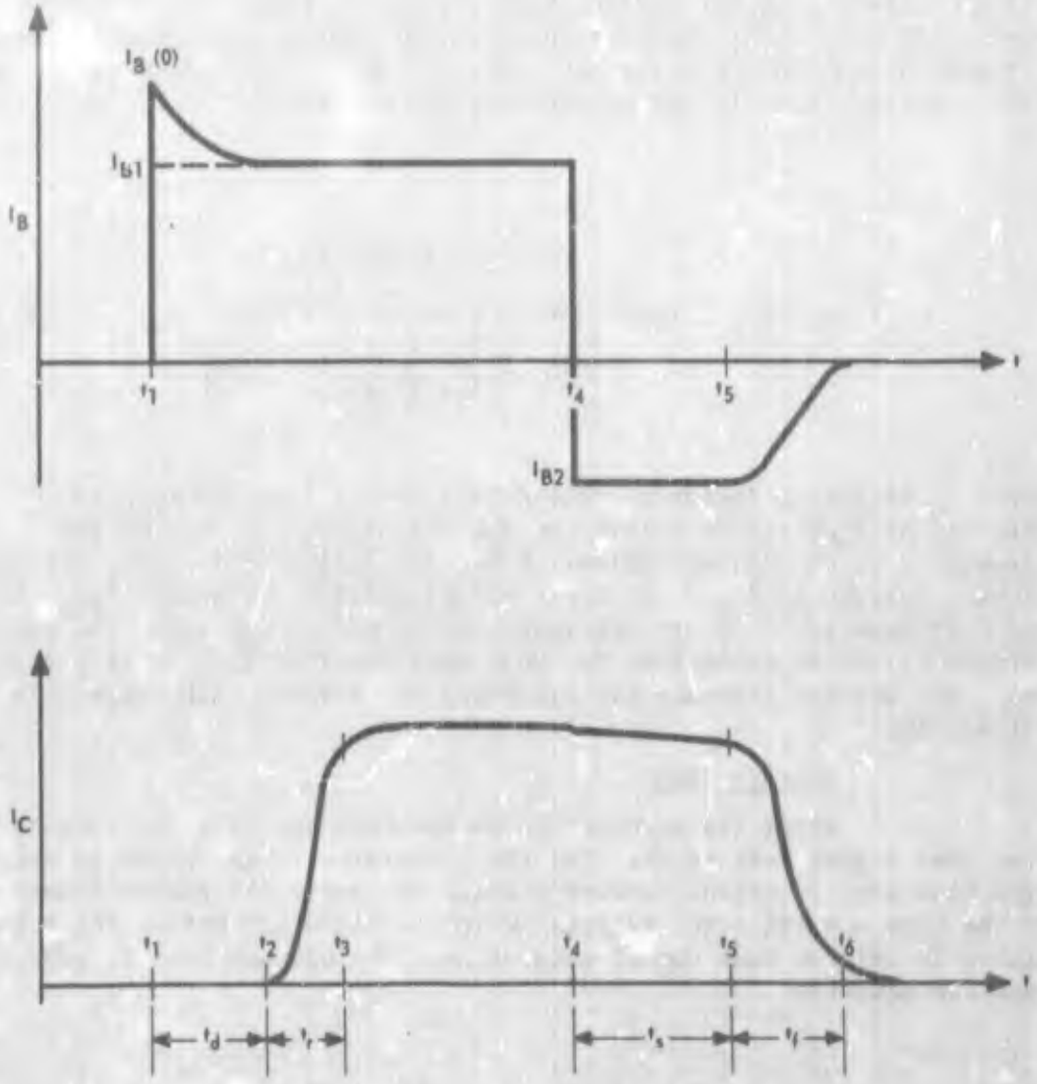


Figure 6-8. Switching time waveforms

emitter and collector junctions reverse-biased to an active operating mode, in which the emitter is forward-biased, the collector remains reverse-biased, and collector current just begins to flow. The change in delay time with radiation is usually insignificant and can be neglected. Prediction of the other times with radiation is discussed below.

6.6.1 Prediction Procedure for Switching Times

Rise Time

In the rise time interval (See Figure 6-8) the base current supplies charge to the emitter and collector junctions to permit voltage changes, and to the neutral base region to establish the necessary charge distribution for current flow across the base. In this time period the transistor operates in its normal active mode with the emitter forward-biased and the collector reverse-biased. The change in the rise time with radiation is determined from the equation[3,4]

$$t_r(\text{post}) = t_r(\text{pre}) \frac{\left[1 - \frac{1}{2}\frac{I_C}{I_{B1}}\frac{1}{h_{FEO}}\right]}{\left[1 - \frac{1}{2}\frac{I_C}{I_{B1}}\left(\frac{1}{h_{FEO}} + t\,K\,\phi\right)\right]} \qquad (6\text{-}10)$$

where I_C is the collector current during the ON time and h_{FEO} is measured at $I_C/2$ and at a level of V_{CE} sufficiently high that the transistor is not in saturation. K is also defined for $I_C/2$. The turn-on base current is I_{B1}. The important prediction parameters h_{FEO}, t and K in Equation 6-10 are determined using any of the gain prediction methods described in Section 5. Note that the rise time is radiation-sensitive and can increase significantly for devices with large gain degradation.

Storage Time

After the turn-off pulse has been applied, the storage time (See Figure 6-8) is the time the transistor takes, while in saturation with both junctions forward-biased, to remove the excess charge in the base and collector regions, which is necessary before the transistor is able to come out of saturation. The storage time is predicted from the equation[3]

$$t_s = \frac{1}{2}\left(t + \frac{1}{\frac{1}{\tau_c} + K_\infty\,\phi}\right) \ln\left[\frac{|I_{B1}| + |I_{B2}|}{|I_{B2}| + I_C\left(\frac{1}{h_{FEO}} + t\,K\,\phi\right)}\right] \qquad (6\text{-}11)$$

where

τ_c = preradiation collector minority carrier lifetime

K_∞ = high injection level damage factor experimentally determined to be 0.2×10^{-6}/RDU-s

I_{B2} = turn-off base current

If τ_c is known from the manufacturer, Equation 6-11 may be used directly to predict t_s by determining h_{FEO}, t, and K using any of the gain prediction methods described in Section 5. Both h_{FEO} and K are defined for a level of I_C one-half the saturated operating current. If τ_c is not known, measure the preradiation storage time experimentally on the test device, and solve Equation 6-11 for τ_c with $\phi = 0$. Then obtain the post-radiation t_s from Equation 6-11 by inserting the appropriate K and ϕ. Note that the storage time is reduced with radiation exposure. This is a beneficial effect, and the circuit designer may accept approximate prediction rather than perform the required device measurements needed for Equation 6-11.

Fall Time

After the removal of the excess charge in the base and collector regions, the transistor comes out of saturation and operates in its normal active mode with the emitter forward-biased and the collector reverse-biased. The fall time (See Figure 6-8) is defined as the interval between the time at which the transistor comes out of saturation to the time at which the collector current has decreased to 10 percent of its saturated mode operating level. The fall time is predicted from the equation

$$t_f = \frac{\frac{I_C}{I_{B2}} \; f\left[1/f_T\right]}{\left[1 + \frac{1}{2}\frac{I_C}{I_{B2}}\left(\frac{1}{h_{FEO}} + t\,K\,\phi\right)\right]} + 2.3\,R_L\,\bar{C}_c \qquad (6\text{-}12)$$

where $f\left[1/f_T\right]$ is a function of f_T[3,4] and $\bar{C}_c$ is defined by

$$\bar{C}_c = \frac{\int_{V_{cb}(\text{cut-off})}^{V_{cb}=0} C_c \, d\,V_{cb}}{V_{cb}(o) - V_{cb}(\text{cut-off})} \qquad (6\text{-}13)$$

The capacitance $\bar{C}_c$ is obtained from numerical integration of the experimental data of C_c versus V_{cb} over the operating range of V_{cb} from zero volts to cutoff. Since $f[1/f_T]$ involves measurements at the operating conditions where the transistor comes out of saturation and this region of operation is not clearly defined, it is preferable to determine $f[1/f_T]$ by solving Equation 6-12 before radiation using an experimentally determined t_f for the test device. The post-radiation t_f is determined using Equation 6-12 with the appropriate K and ϕ. Both h_{FEO} and K are defined for a collector current one-half the saturated operating current level. The parameters h_{FEO}, t and K may be determined using any of the gain prediction methods given in Section 5. Note that the fall time decreases with radiation, which is a desirable effect.

6.6.2 Sample Prediction of Switching Times

Given: Fairchild 2N1613 transistor

$$I_C = 15.4 \text{ mA}, \; I_{B1} = 6 \text{ mA}, \; I_{B2} = 6 \text{ mA}$$

$$\phi = 7.05 \times 10^{13} \text{ RDU}, \; T = 35°C$$

Required: t_d, t_r, t_s and t_f

Delay Time

The change in delay time with radiation in insignificant and can be neglected. Pre and post-radiation measurements made on the test device and shown in Figure 6-9 indicate a 50 ns delay time for both measurements. The step change in the waveform is the initiation of the delay time.

Rise Time

The rise time increases with radiation. The following procedure is followed to predict this increase.

Step 1 — The rise time is determined experimentally. From the waveform in Figure 6-9 the preradiation rise time for the test device is approximately 25 ns. The rise time interval is defined from zero output to 90 percent of saturated output.

Step 2 — The base transit time measured according to the procedure given in Appendix A and Section 5, is 1.54 ns.

Step 3 — From photomicrographs of a similar Fairchild 2N1613 transistor the emitter area is measured as 1.14×10^{-3} cm^2.

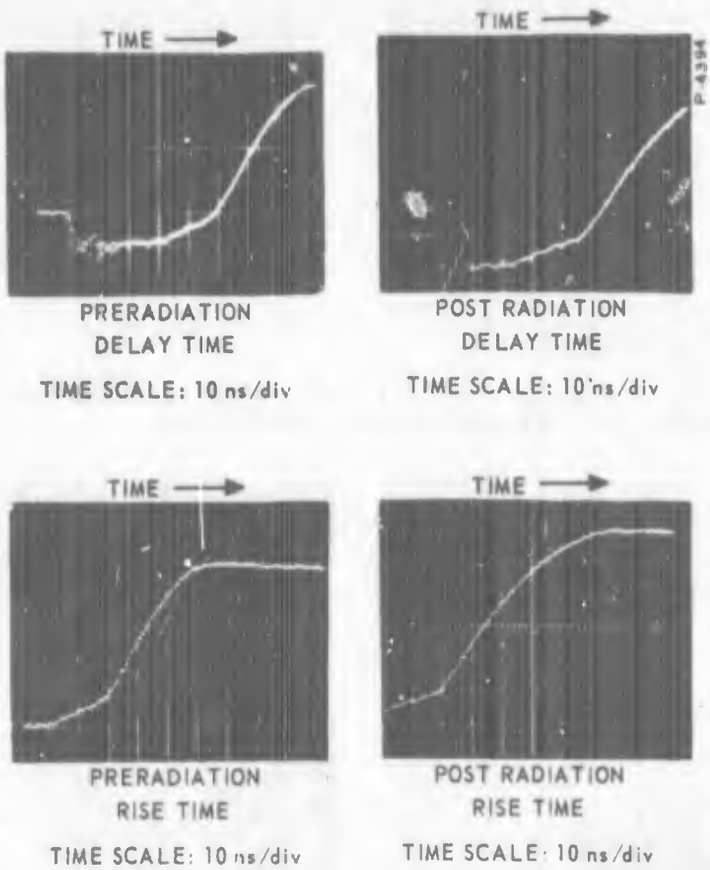


Figure 6-9 - Delay and rise times before and after radiation

Step 4 From Figure 5-2 (pages 5-5 and 5-6) the mean empirical damage factor is 1.6×10^{-5}/RDU-s at $J_E = 7.7/1.14 = 6.75$ A/cm^2.

Step 5 The measured preradiation gain h_{FEO} at $I_C/2 = 7.7$ mA and $V_{CE} = 5$ volts is 68. At $V_{CE} = 5$ volts the transistor is not in saturation.

Step 6 The rise time is determined from Equation 6-10. Hence,

$$t_r(\text{post}) = t_r(\text{pre}) \frac{\left[1 - \frac{1}{2}\frac{I_C}{I_{B1}}\frac{1}{h_{FEO}}\right]}{\left[1 - \frac{1}{2}\frac{I_C}{I_{B1}}\left(\frac{1}{h_{FEO}} + t\,K\,\phi\right)\right]}$$

$$t_r(\text{post}) = \frac{\left(25 \times 10^{-9}\right)\left[1 - \frac{1}{2}\left(\frac{15.4}{6}\right)\left(\frac{1}{68}\right)\right]}{\left[1 - \left(\frac{1}{2}\right)\left(\frac{15.4}{6}\right)\left(\frac{1}{68} + \left(1.54\right)\left(1.6\right)\left(7.05 \times 10^{-2}\right)\right)\right]} = 32.4 \text{ ns}$$

The measured post-radiation rise time indicated in Figure 6-9 is 45 ns.

Storage Time

The storage time for a transistor decreases with radiation. The following steps are employed in the prediction.

Step 1 Since τ_c is unknown, it can be determined by measuring the storage time and solving Equation 6-11 with $\phi = 0$. From the preradiation waveform in Figure 6-10, t_s is approximately 530 ns. The storage time is initiated when the turn-off pulse is applied, which occurs at the extreme left in the top waveforms of Figure 6-10. Because this transistor is not gold-doped,

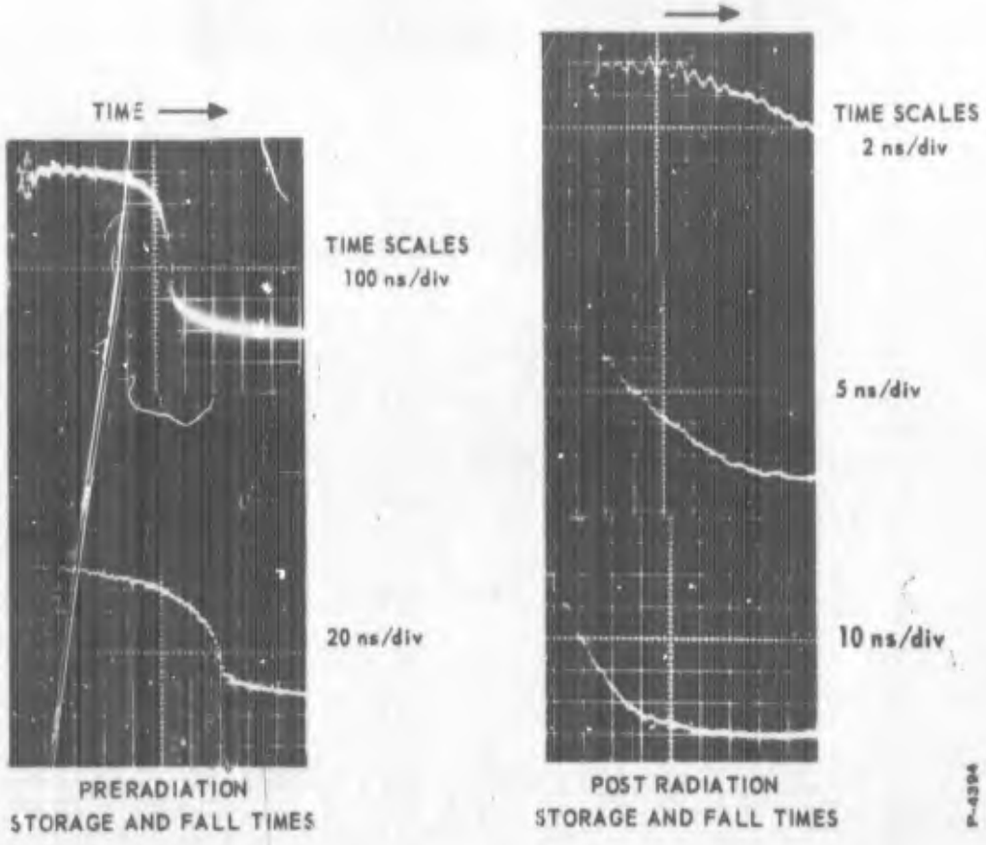


Figure 6-10 - Storage and fall times before and after radiation

it comes out of saturation slowly. The storage time in this case is measured from the time the turn-off current I_{B2} is applied, to the time at which the output has dropped about 30 percent below the saturation output. This arbitrary 30 percent level was chosen because it corresponds to the point where the fast fall time interval begins. For fast switching gold-doped transistors where t_s is about the same as t_f, t_s is measured from the time the turn-off pulse is applied, to the time when the output drops about 10 percent below saturated output.

The preradiation minority carrier lifetime in the collector is

$$\tau_c = \frac{2\ t_s}{\ln\left[\frac{|I_{B1}| + |I_{B2}|}{|I_{B2}| + I_C/h_{FEO}}\right]} - t$$

$$\tau_c = \frac{1060 \times 10^{-9}}{\ln\left[\frac{6+6}{6+15.4/68}\right]} - 1.54 \times 10^{-9}$$

$$= 1616 - 2 = 1614 \text{ ns}.$$

Step 2 The predicted post-radiation storage time for $\phi = 7.05 \times 10^{13}$ RDU and using Equation 6-11 is

$$t_s = \frac{1}{2}\left(t + \frac{1}{\frac{1}{\tau_c} + K_\infty\ \phi}\right)\ \ln\left[\frac{|I_{B1}| + |I_{B2}|}{|I_{B2}| + I_C\left(\frac{1}{h_{FEO}} + t\ K\ \phi\right)}\right]$$

$$t_s = \frac{1}{2}\left(1.5 \times 10^{-9} + \frac{1}{\frac{10^6}{1.61} + 14.1 \times 10^6}\right) \cdot$$

$$\ln\left[\frac{6+6}{6+15.4\left(\frac{1}{68} + (1.54)\ (1.6)\ (7.05) \times 10^{-2}\right)}\right]$$

$$t_s = 10.2 \text{ ns}$$

The measured post-radiation storage time indicated in Figure 6-10 is about 12 ns. Since the experimental storage time is now less than the fall time, it is measured to the point where the output has dropped 10 percent below the saturated output.

Fall Time

The fall time for a transistor decreases with radiation. It can be predicted from the following procedure.

Step 1 The capacitance is measured at the collector-base junction as a function of reverse voltage, and the average capacitance $\bar{C}_c$ is determined by numerically integrating from $V_{cb} = 0$ to V_{cb} = cutoff voltage, which for this application was 10 volts. The experimental curve of C_{cbo} versus V_{CBO} is shown in Figure 6-11. These data are for the transistor alone. Numerical integration of this curve to obtain the average capacitance according to Equation 6-13 gives $\bar{C}_c = 22.6$ pF. The stray capacitance of the switching time test fixture used to measure t_f should be included, particularly if the junction capacitance of the transistor is low. In this case the stray capacitance was 1.4 pF, hence $\bar{C}_c$ for use in Equation 6-12 is 24 pF. Note that for gold-doped transistors the capacitance is frequency sensitive and therefore should be measured at frequencies above 100 kHz.

Step 2 From the preradiation waveform of Figure 6-10 the measured fall time is approximately 35 ns. This time was measured in a circuit with a load resistance R_L of 260 ohms. Solving Equation 6-12 with $\phi = 0$ for the function $f[1/f_T]$ gives

$$f[1/f_T] = \left[\frac{\left(t_f - 2.3\, R_L\, \bar{C}_c\right)\left(1 + \frac{1}{2}\,\frac{I_C}{I_{B2}}\,\frac{1}{h_{FEO}}\right)}{\frac{I_C}{I_{B2}}} \right]$$

$$f[1/f_T] = \frac{\left[35 - \left(2.3\right)\left(260\right)\left(24\right)\left(10^{-3}\right)\right] 10^{-9} \left[1 + \frac{1}{2}\left(\frac{15.4}{6}\right)\left(\frac{1}{68}\right)\right]}{\frac{15.4}{6}}$$

$$f[1/f_T] = 8.22 \text{ ns}$$

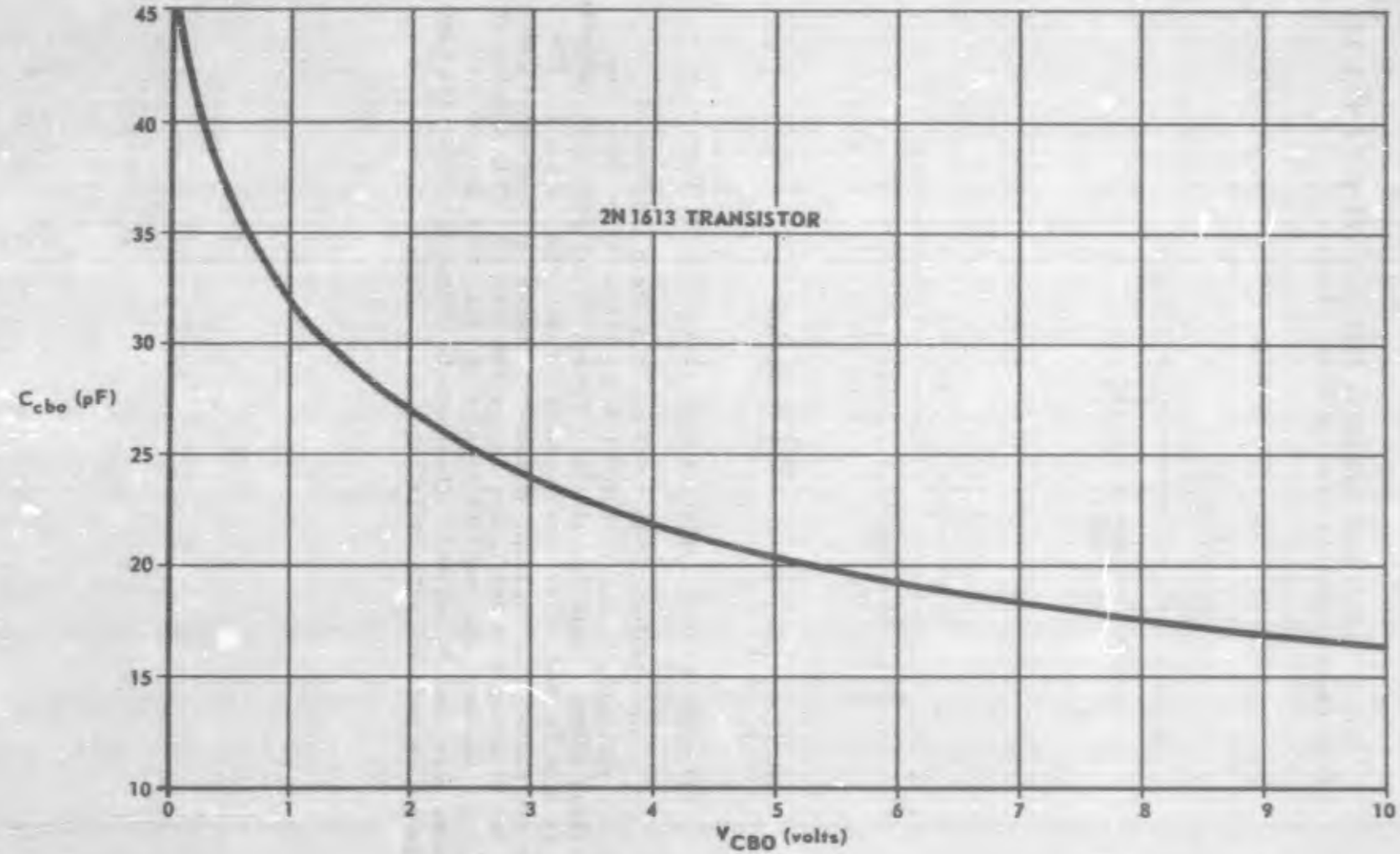


Figure 6-11. C_{cbo} versus V_{CBO}

Step 3 The predicted post radiation fall time for $\phi = 7.05 \times 10^{13}$ RDU is determined from Equation 6-12. Thus,

$$t_f = \frac{\frac{I_C}{I_{B2}} f\left[1/f_T\right]}{\left[1 + \frac{1}{2}\frac{I_C}{I_{B2}}\left(\frac{1}{h_{FEO}} + t K \phi\right)\right]} + 2.3 R_L \bar{C}_c$$

$$t_f = \frac{\left(\frac{15.4}{6}\right)\left(8.22 \times 10^{-9}\right)}{1 + \left(\frac{1}{2}\right)\left(\frac{15.4}{6}\right)\left[\frac{1}{68} + \left(1.54\right)\left(1.6\right)\left(7.05\right) \times 10^{-2}\right]}$$

$$+ \left(2.3\right)\left(260\right)\left(24 \times 10^{-12}\right) = 31.3 \text{ ns}$$

The measured post radiation fall time is about 30 ns.

The conclusions to be drawn from the prediction of transistor switching times are that with the exception of rise time, these times either remain essentially constant or decrease with radiation, which is usually desirable. The increase in rise time is small. Even if the transistor gain degrades to the point where the transistor just comes out of saturation and $I_C/I_{B1} = h_{FE}$, the rise time only doubles in magnitude. However, the combined storage and fall time generally decreases more than 50 percent. Therefore the total net switching time will generally decrease with radiation.

SECTION 6 REFERENCES

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2. S. M. Sze and G. Gibbons, "Effect of Junction Curvature on Breakdown Voltage in Semiconductors," Solid State Electronics 9, 831-845, 1966.

3. M. Frank, "Development of a Non-Destructive Radiation Effects Prediction Technique," Contract AF 29(601)-7110, Second Quarterly Progress Letter for Period Ended April 30, 1966, BRL Report 3433, AD 482 509.

4. H. John Kuno, "Rise and Fall Time Calculations of Junction Transistors," IEEE Trans on Electron Devices, ED-11, 151-155, April 1964.

SECTION 7

DIODES

The four major performance parameters of diodes are forward voltage, reverse current, breakdown voltage and reverse recovery time. The forward voltage characteristics are the most sensitive to radiation damage and usually the most critical in a circuit application. Both minority carrier lifetime degradation and carrier removal effects influence forward voltage, which for power diodes, increases with radiation at rated operating current levels. Signal level diodes, particularly devices with low breakdown voltage, show little change in forward voltage and may actually show a decrease in forward voltage for radiation exposures of 10^{14} RDU; hence they are not a problem. Diode reverse current and breakdown voltage effects are the same as in transistor junction behavior. These parameters are discussed in Section 6. Diode reverse recovery time, which is dependent on minority carrier lifetime, decreases with radiation. The discussion in this section is therefore devoted to the prediction of the forward voltage of power diodes and of p-n or n-p construction.

7.1 PREDICTION PROCEDURE FOR DIODE FORWARD VOLTAGE

The forward voltage V_F of a power diode can be predicted using data developed by Lieb, Jackson, and Root.[1] Although their theoretical analyses and computer solutions are for a planar abrupt-junction diode, these data also yield satisfactory predictions of V_F for diffused junction diodes. The model neglects recombination current in the junction transition layer; however, at moderate and high injection levels where power diodes normally operate, the contribution of this component of current is negligible. The effects of ohmic drop, electric fields, conductivity, and changes in the diode base region with current level are included. These are the effects that are of prime importance in predicting radiation changes of V_F for power devices. The diode performance data are normalized for one ohm-cm material into curves of constant W/L ratios and plotted as $J \rho W$ where $J \rho W = I_F \frac{\rho W}{A} = I_F R_F$. Correction of V_F for diode base resistivities other than one ohm-cm is readily accomplished. The radiation sensitive parameters are the resistivity ρ, which increases due to carrier removal effects, and the diffusion length L, which decreases due to minority carrier lifetime degradation. The following sequence of steps is used in the forward voltage prediction.

Step 1 Determine the junction capacitance C_j of the diode at large reverse voltage where the capacitance-voltage function approximates a square law relationship. The stray capacitance

should be subtracted from the capacitance measured at the terminals. The procedure for these measurements is described in Appendix B. If the diode is gold-doped, the capacitance should be measured at bridge frequencies of 100 kHz or higher.

Step 2 The doping concentration N_o in the base of the diode is calculated using the capacitance at the reverse voltage V_R measured in Step 1 and the equation

$$N_o = \frac{2(V_R + V_T)\left(\frac{C_j}{A}\right)^2}{q\,\epsilon} = 1.2 \times 10^{31}(V_R + V_T)\left(\frac{C_j}{A_j}\right)^2 \qquad (7\text{-}1)$$

where

V_T = built-in equilibrium voltage, which is assumed as approximately 0.6 volt for silicon power diodes.

A_j = area of the junction in cm^2, which should be obtained from the manufacturer.

C_j = junction capacitance in farads.

Note that the use of breakdown voltage data in Figure 6-6 is not recommended for determining N_o for diodes because of the approximation in N_o obtained with this method. Since the resistivity of the base for power diodes is usually high and carrier removal effects are significant, prediction accuracy is improved by using capacitance measurements.

Step 3 The post radiation doping concentration is determined from the equation

$$N = N_o - K_N \phi \qquad (7\text{-}2)$$

where

K_N = 1.3 carriers removed/cm^3-RDU

This carrier removal rate coefficient was determined from experimental data of changes in collector resistivity of 2N1613 transistors with radiation.

Step 4 The post radiation minority carrier lifetime is calculated from the equation

$$\frac{1}{\tau} = \frac{1}{\tau_o} + K_\infty \phi \qquad (7\text{-}3)$$

The quantity τ_o is the minority carrier lifetime in the base before radiation. The procedure for measuring it is given in Appendix B. Since power diodes normally operate at high injection, the damage factor $K_\infty = 0.2\ (10^{-6}/\text{RDU-s})$ is used.

Step 5 The diffusion length L after radiation is determined from the equation

$$L = \sqrt{D\,\tau} \qquad (7\text{-}4)$$

where

D = diffusion constant for material type which is determined from Figure 7-1 (page 7-5) using the post radiation doping level from Step 3. The data in Figure 7-1 are taken from Phillips.[2] The dopant type of the base should be obtained from the manufacturer.

Step 6 The factors (J ρ W) and (W/L) are calculated for use with the Lieb, Jackson, and Root curves[1] in Figures 7-2 through 7-5 (pages 7-7 to 7-13). The diode dopant type and geometry (area and base length W) should be obtained from the manufacturer. The current density is given by

$$J = \frac{I_F}{A} \qquad (7\text{-}5)$$

The resistivity ρ is obtained from Figure 7-6 (page 7-15)[3] using N from Step 3, and L is the quantity computed in Step 5. If the diode is gold-doped, the compensated value of N should be used to obtain ρ.

Step 7 Since the J ρ W versus V_F curves in Figures 7-2 through 7-5 are for one ohm-cm silicon, the forward voltage must be corrected for the post radiation resistivity of the specific device, using the equation

$$V = \frac{kT}{q} \ln\left(\frac{N}{N'}\right) \qquad (7\text{-}6)$$

where

$N' = 5.55 \times 10^{15}$ cm^{-3} (n-type base)

$= 1.45 \times 10^{16}$ cm^{-3} (p-type base)

and

N = predicted doping level from Step 3.

Thus,

$$V_F(\rho) = V_F(1 \text{ ohm - cm}) + V \qquad (7\text{-}7)$$

7.2 SAMPLE PREDICTION FOR DIODE FORWARD VOLTAGE

Given: Texas Instruments 1N645 diode

$$\phi = 8.7 \times 10^{13} \text{ RDU}, \quad T = 27°C$$

Required: Forward voltage at $I_F = 100$ mA

Step 1 Using the measurement procedure given in Appendix B, the terminal capacitance at $V_R = 100$ volts is 5.36 pF, and the diode stray capacitance is 0.8 pF. Hence the junction capacitance is $C_j = 5.36 - 0.8 = 4.56$ pF. This diode is not gold-doped, so the measurement bridge frequency is not important.

Step 2 The doping concentration before radiation is obtained from equation (7-1)

$$N_o = \frac{2(V_R + V_T)\left(\frac{C_j}{A}\right)^2}{q\,\varepsilon} = 1.2 \times 10^{31}(V_R + V_T)\left(\frac{C_j}{A_j}\right)^2$$

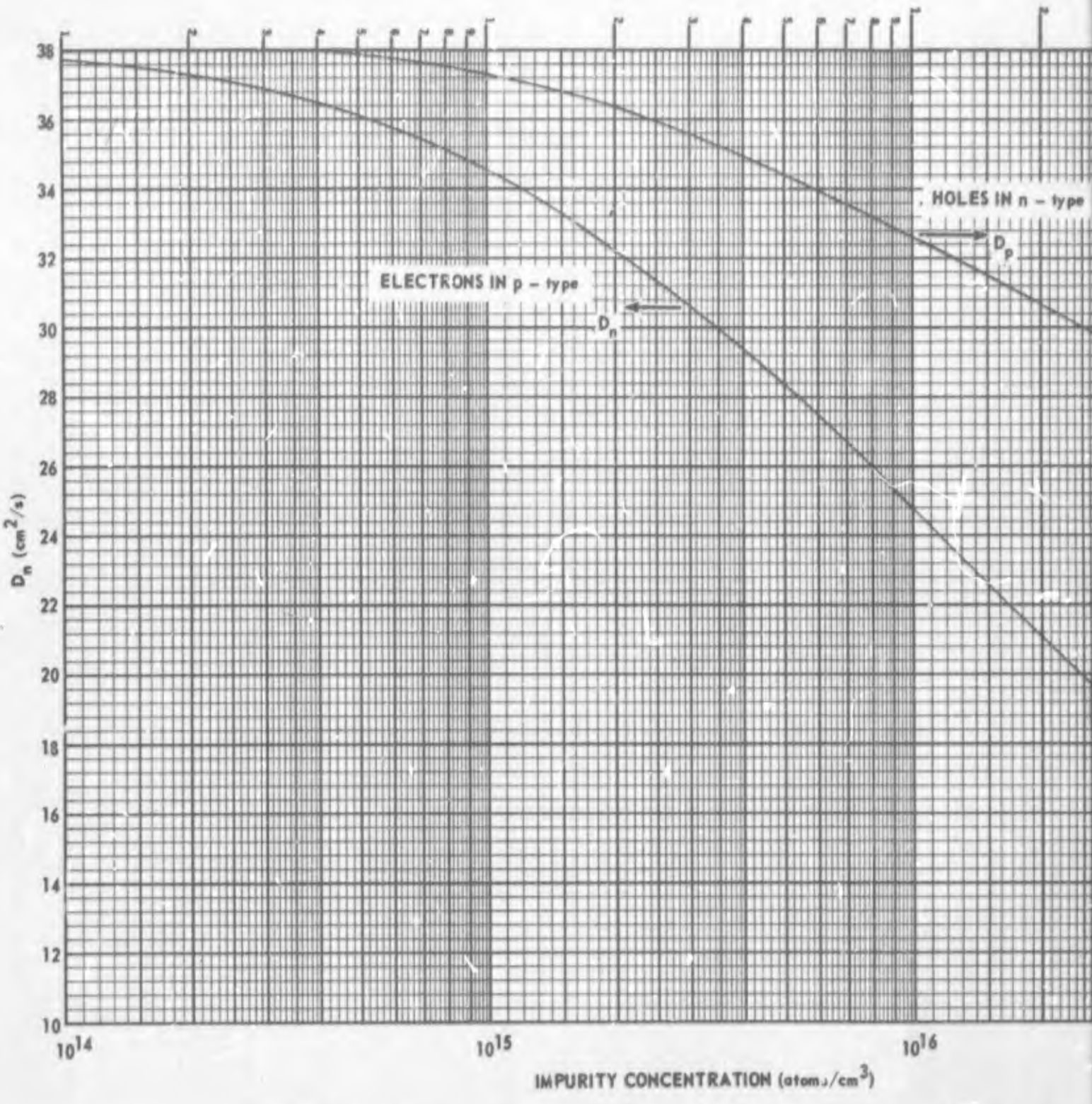
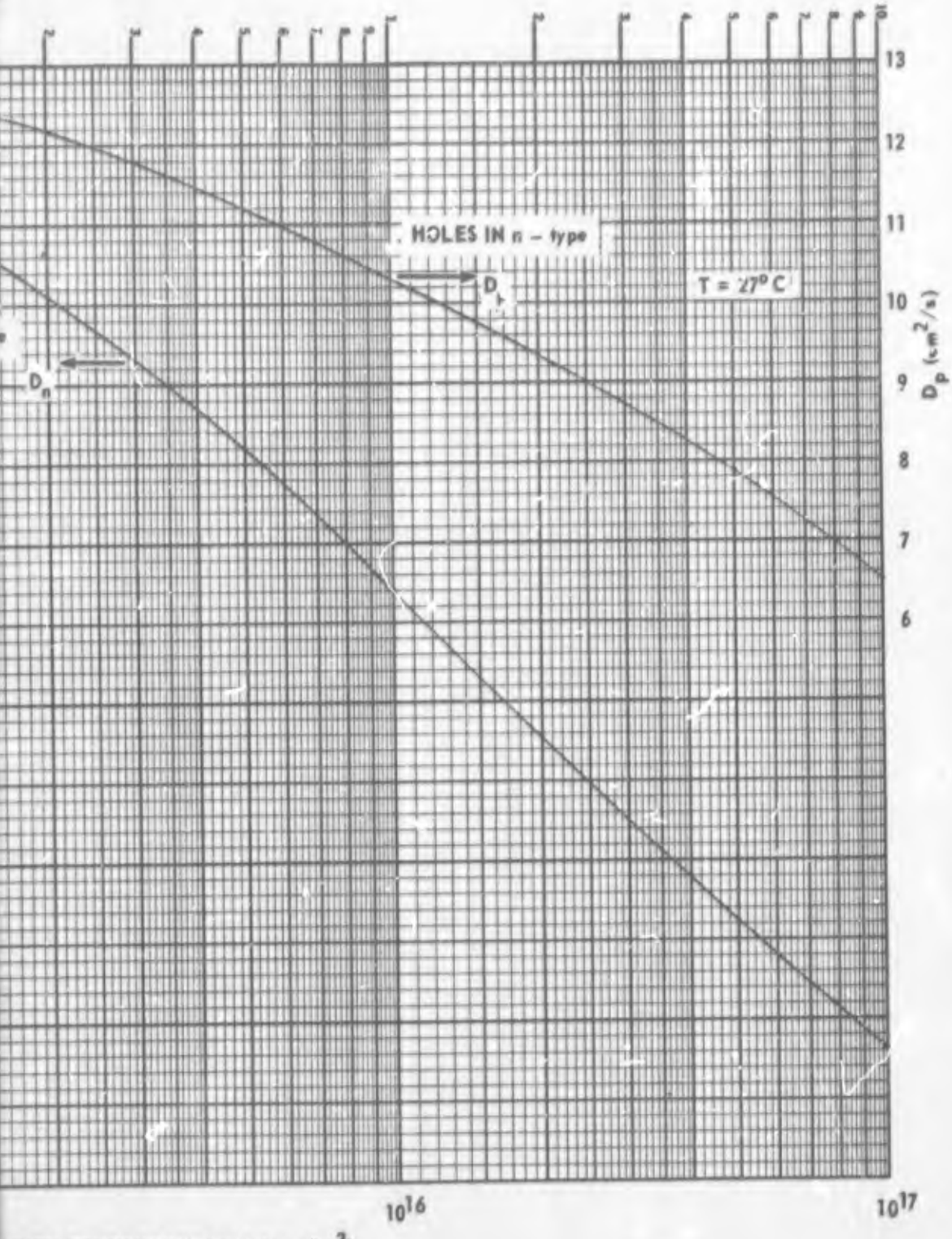


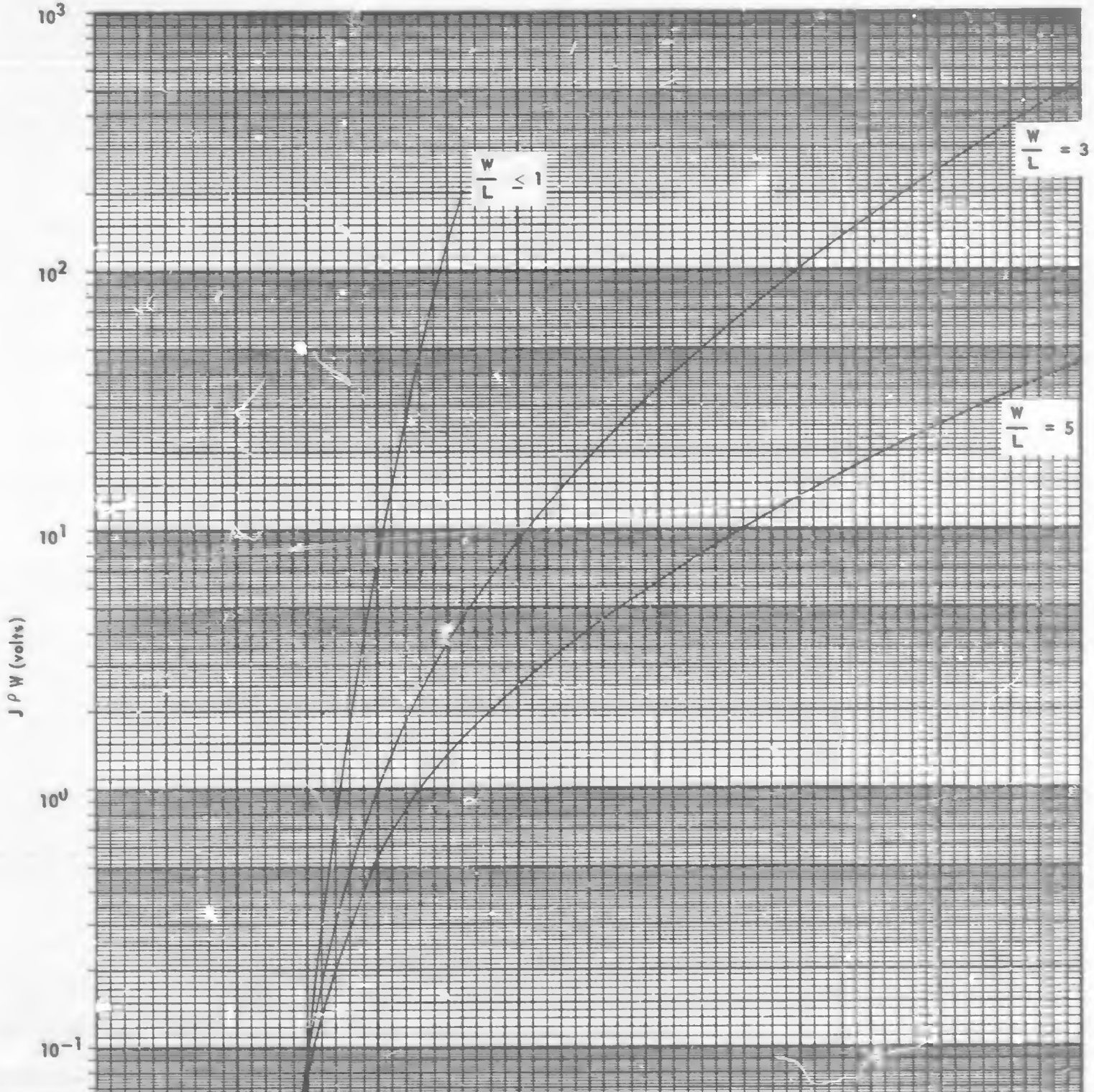
Figure 7-1. Minority carrier diffusion constant for silicon (source: Reference



URITY CONCENTRATION (atoms/cm^3)

iffusion constant for silicon (source: Reference 2)

2


10^3
10^2
10^1
10^0
10^{-1}
J ρ W (volts)
$\frac{W}{L} \leq 1$
$\frac{W}{L} = 3$
$\frac{W}{L} = 5$

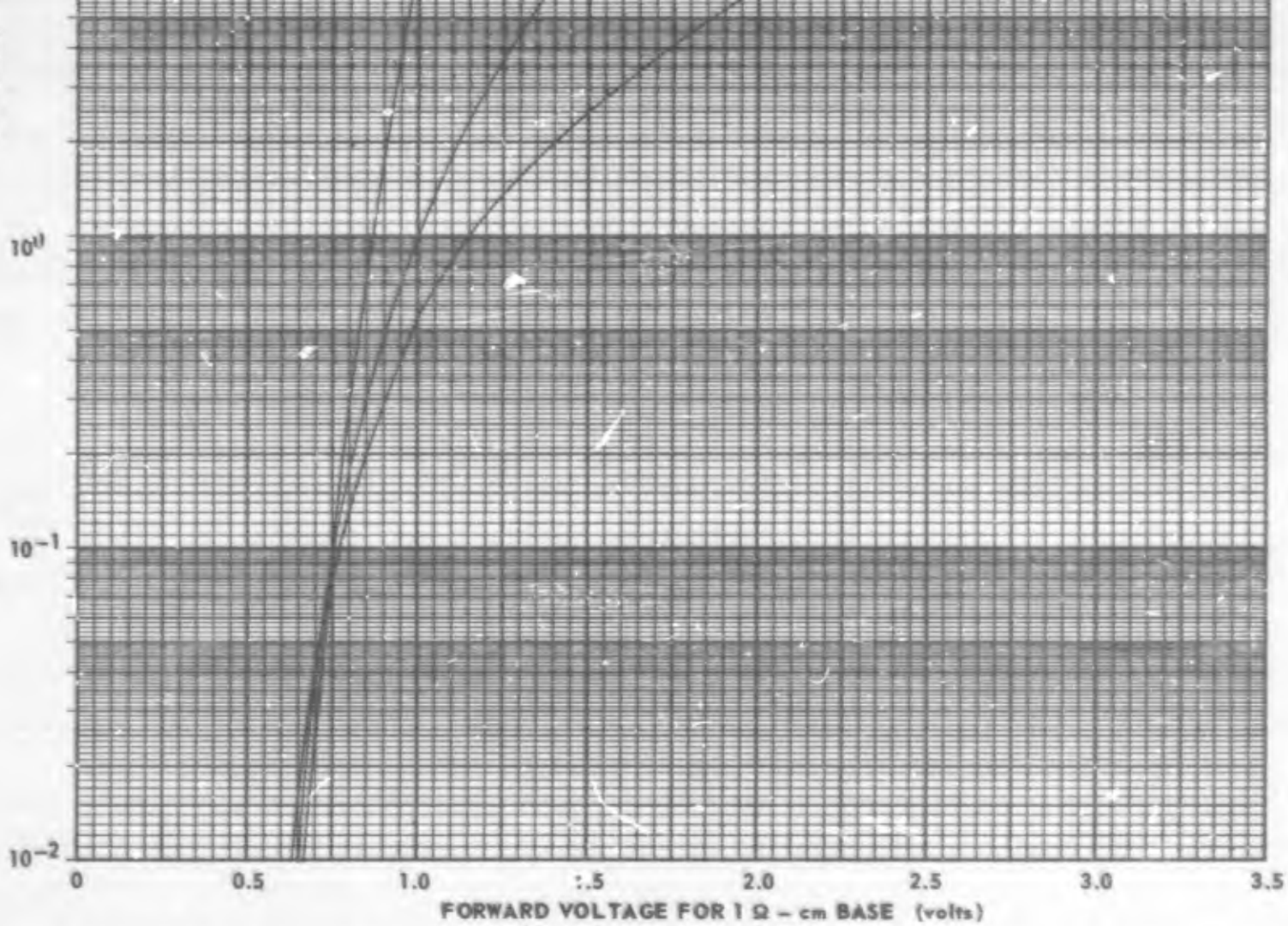
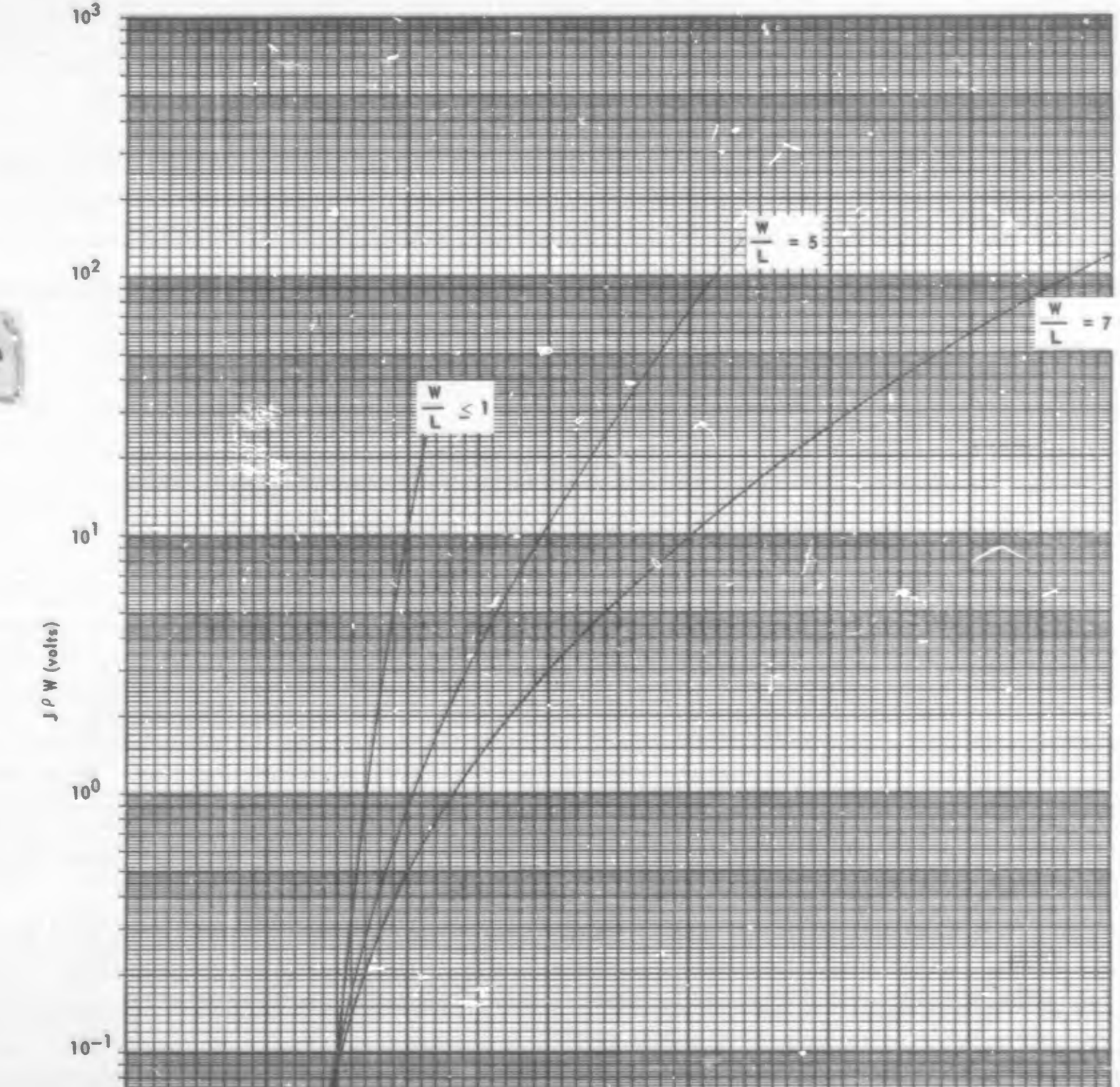


Figure 7-2. Forward voltage characteristics for n^+p diodes (source: Reference 1)


10^3
10^2
10^1
10^0
10^{-1}
J ρ W (volts)
$\frac{W}{L} = 5$
$\frac{W}{L} = 7$
$\frac{W}{L} \leq 1$

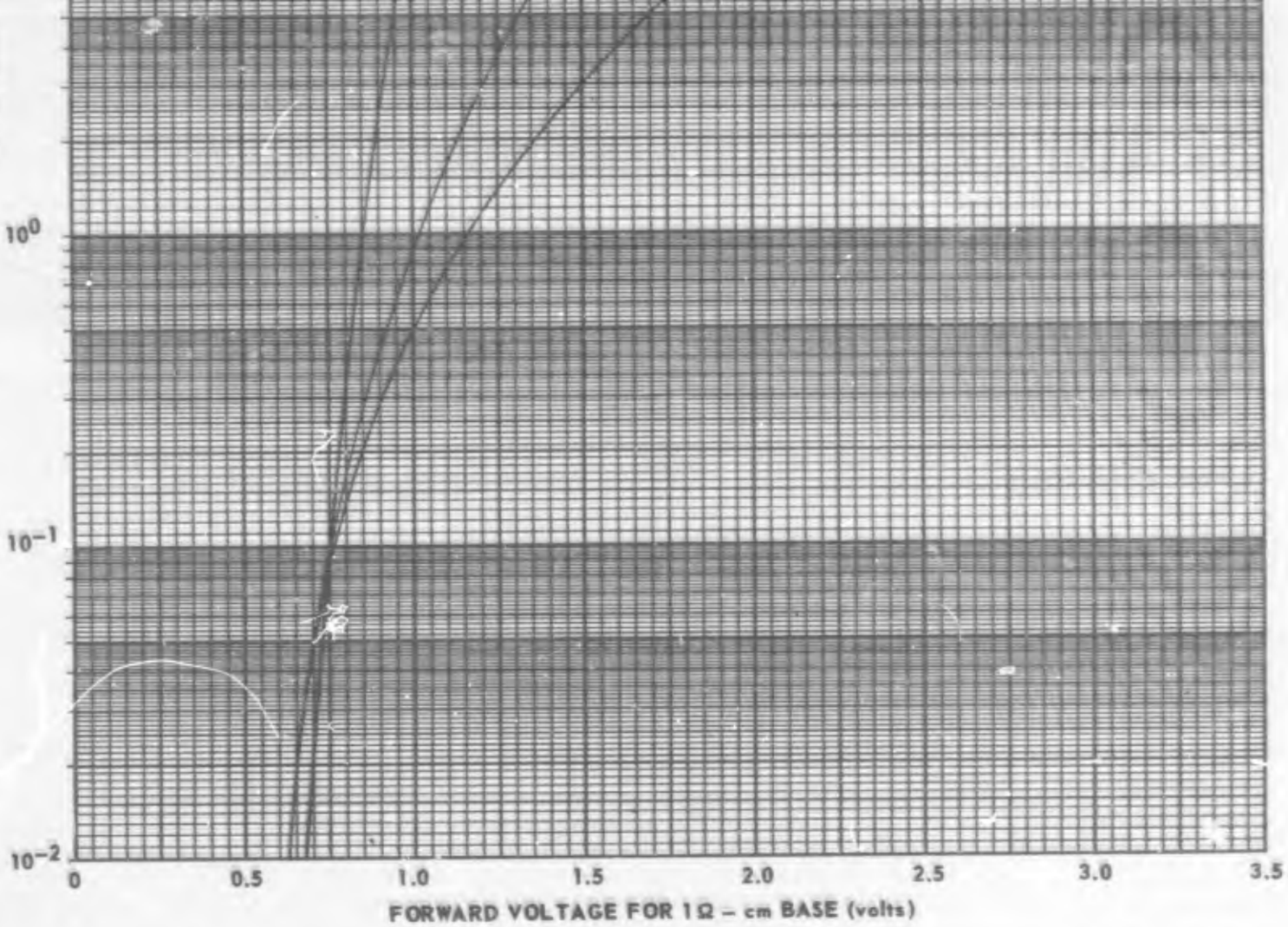


Figure 7-3. Forward voltage characteristics for p^+n diodes (source: Reference 1)

10^{-3}
10^{-2}
10^{-1}
10^{0}
10^{1}
10^{-1}
J_{PW} (volts)
$\frac{W}{L} = 10$
$\frac{W}{L} = 7$
$\frac{W}{L} = 5$
$\frac{W}{L} \leq 1$

1

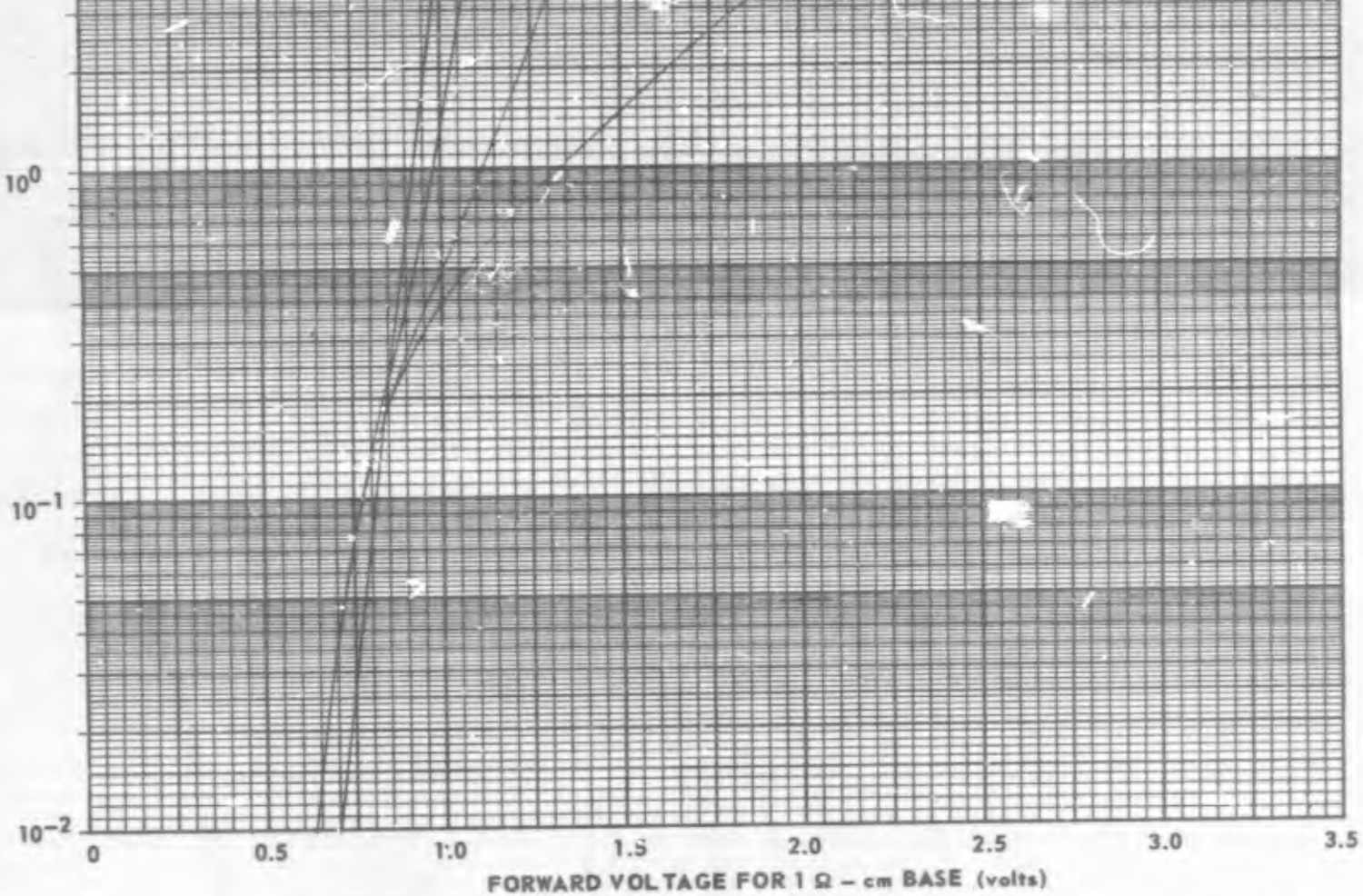


Figure 7-4. Forward voltage characteristics for p^+nn^+ diodes (source: Reference 1)

1

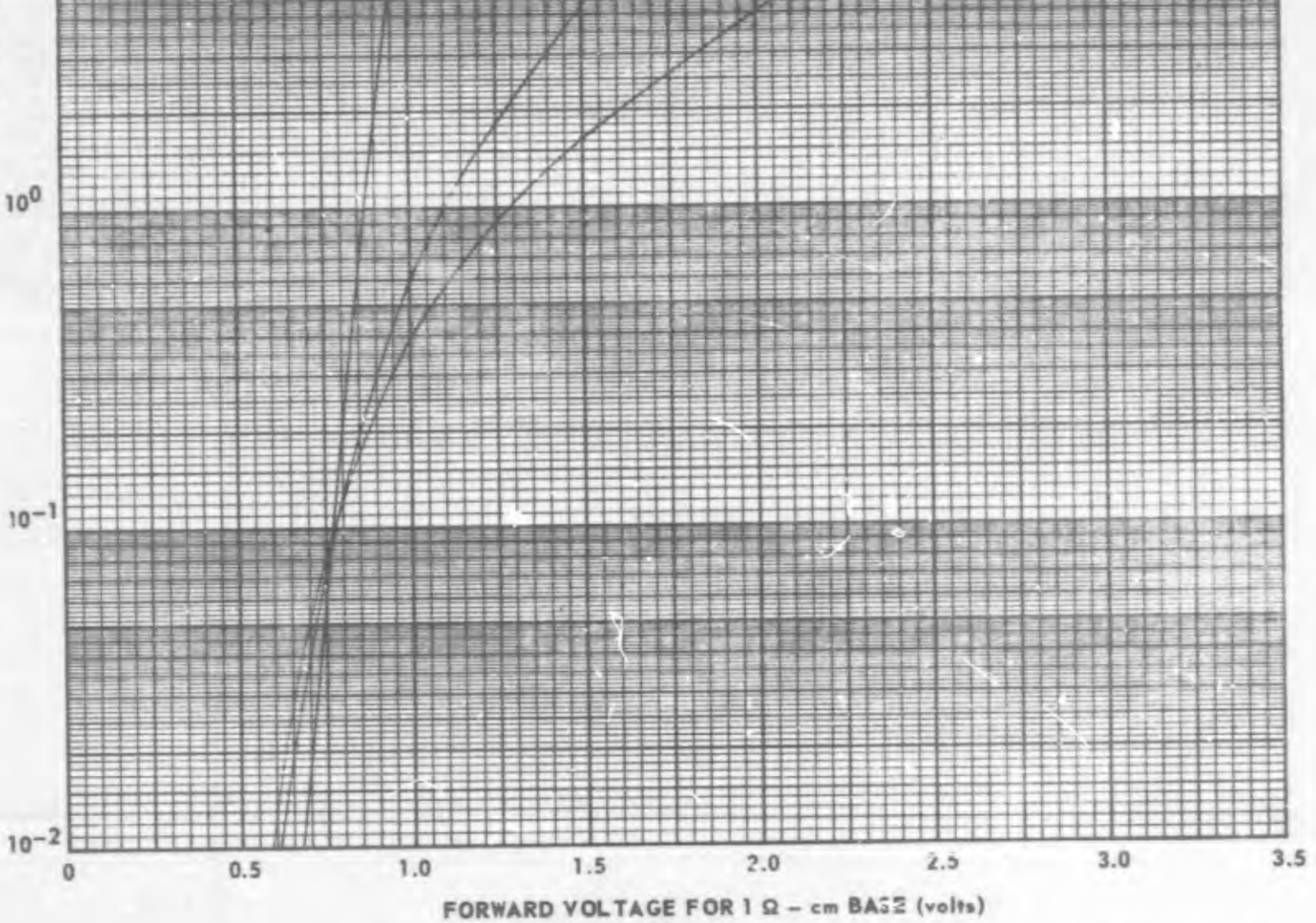


Figure 7-5. Forward voltage characteristics for n^+pp^+ diodes (source: Reference 1)

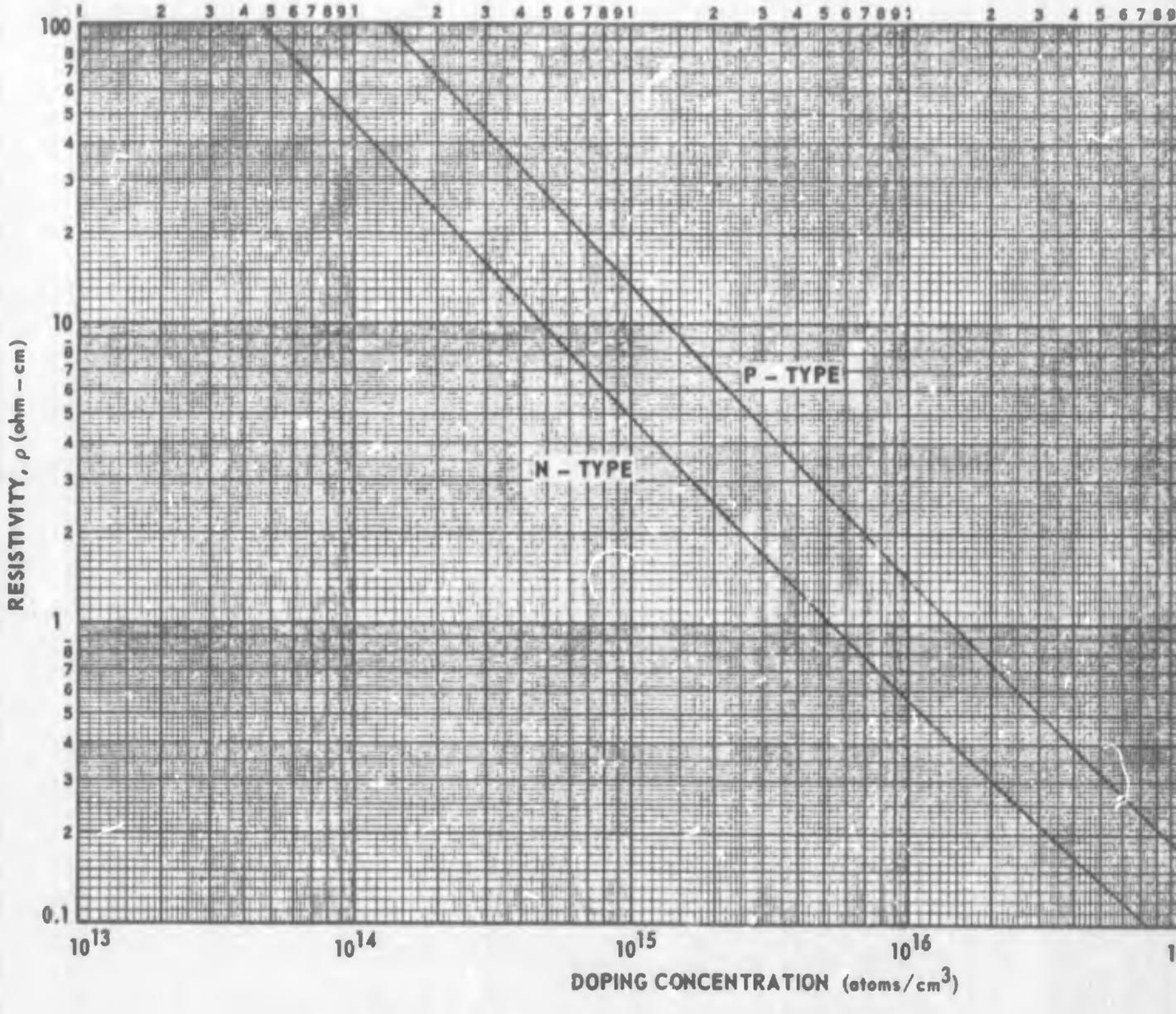
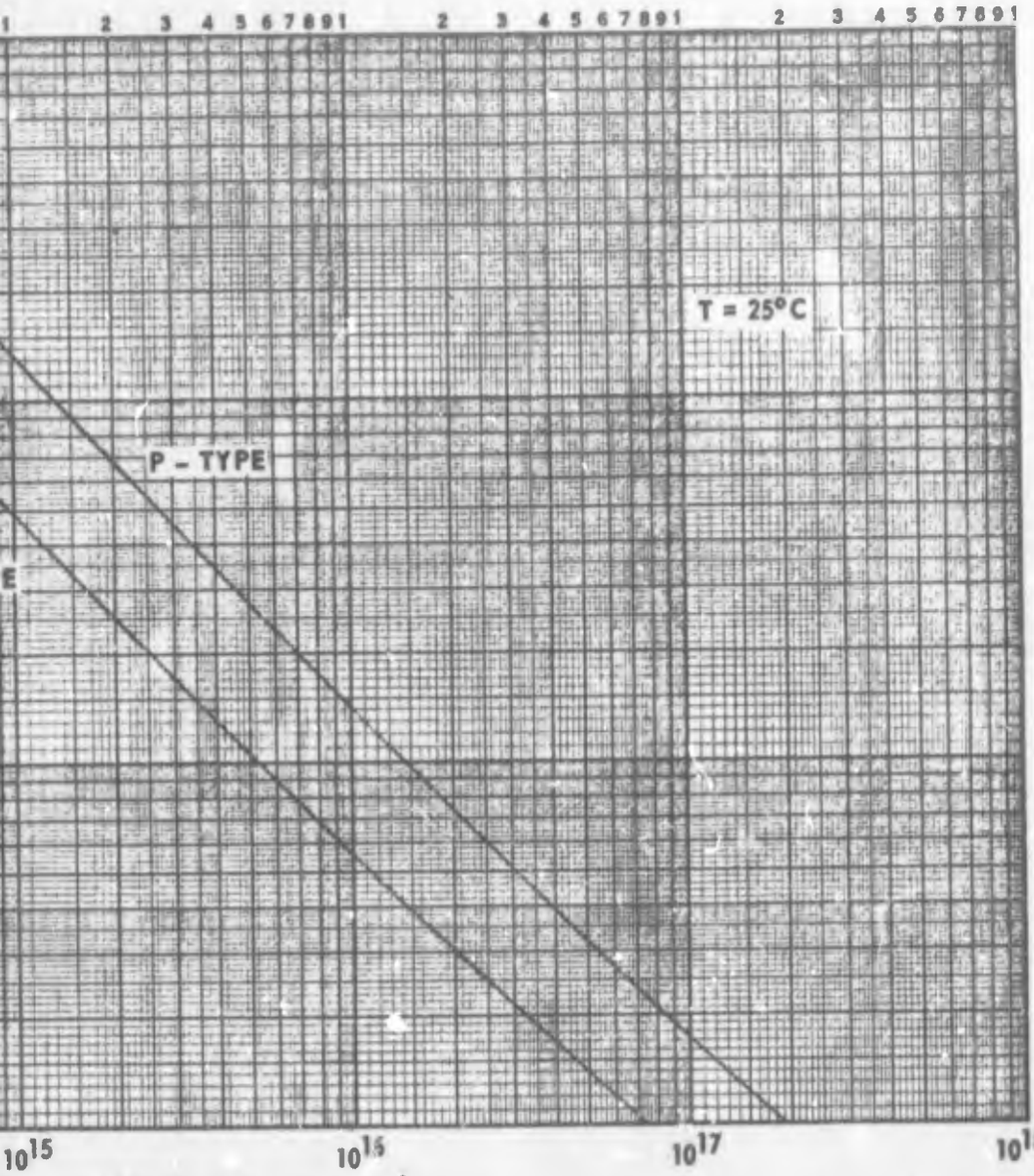


Figure 7-6. Resistivity versus doping concentration (source: Referenc

1



versus doping concentration (source: Reference 3)

$$N_o = 1.2 \times 10^{31}(100 + 0.6)\left(\frac{4.56 \times 10^{-12}}{10^{-2}}\right)^2 = 2.51 \times 10^{14}/cm^3$$

The area of the junction 10^{-2} cm^2 was obtained from the manufacturer.

Step 3 The doping concentration after radiation is obtained from equation (7-2)

$$N = N_o - K_N \phi = 2.5 \times 10^{14} - 1.3 \times 8.7 \times 10^{13} = 1.4 \times 10^{14}/cm^3$$

Step 4 By a method described in Appendix B, the preradiation minority carrier lifetime τ_o was measured as 2μs. The lifetime after radiation is computed from equation 7-3

$$\tau = \frac{1}{\frac{1}{\tau_o} + K_\tau \phi} = \frac{1}{\frac{10^6}{2} + (0.2 \times 10^{-6})\ (8.7 \times 10^{13})} = 55.9 \text{ ns}$$

Step 5 The diffusion length L is determined from equation 7-4

$$L = \sqrt{D\,\tau}$$

From Figure 7-1 (page 7-5) at $N = 1.4 \times 10^{14}/cm^3$, $D_n = 37.6$ cm^2/s. The manufacturer stated that the base was p-type.

Therefore, $L = \sqrt{(37.6) \times 55.9 \times 10^{-9}} = 14.5$ μm

Step 6 From the manufacturer, W = 0.0037" x 2.54 = 94 μm; hence

$\frac{W}{L} = \frac{94 \times 10^{-4}}{14.5 \times 10^{-4}} = 6.5$. The current density is $J = \frac{I_F}{A} = \frac{10^{-1}}{10^{-2}}$ $10A/cm^2$. With N from Step 3, the resistivity from Figure 7-6 (page 7-15) is 95 ohm-cm. Therefore,

$$J\,\rho\,W = (10)(95)(94 \times 10^{-4}) = 8.95 \text{ volts.}$$

The manufacturer stated that the diode construction is $n^+ p\ p^+$; hence from Figure 7-5 (page 7-13), the forward voltage is estimated as 2.25 volts.

Step 7 The forward voltage from Figure 7-5 is corrected using equations 7-6 and 7-7

$$V = \frac{kT}{q} \ln\left(\frac{N}{N'}\right) = (26 \times 10^{-3}) \ln\left(\frac{1.4 \times 10^{14}}{1.45 \times 10^{16}}\right) = -0.12 \text{ volt}$$

and

$$V_F = V(1 \text{ ohm - cm}) + V = 2.25 - 0.12 = 2.13 \text{ volts}$$

The measured post radiation voltage for the passively irradiated test sample was 2.69 volts, which indicates fair correlation with the predicted value. Since the forward voltage of power diodes can increase substantially with radiation, primarily due to a reduction in conductivity in the base, the designer is advised to select the device with the lowest measured breakdown voltage and lifetime τ_o that can be safely employed in the circuit. This will assure minimum base resistivity and reduced changes in conductivity from lifetime degradation, thereby keeping the forward voltage change with radiation to a minimum.

7.3 PREDICTION OF OTHER DIODE PERFORMANCE PARAMETERS

Breakdown Voltage

Refer to Section 6.3

Junction Leakage Current

Refer to Section 6.5

Reverse Recovery Time

Since this parameter decreases with radiation, which is a beneficial circuit effect, no prediction technique is given.

SECTION 7 - REFERENCES

1. D. P. Lieb, B. D. Jackson, and C. D. Root, "Abrupt Junction Diode Theory," IRE Trans on Electron Devices, ED-9, 143-153, March 1962.

2. A. B. Phillips, "Transistor Engineering," McGraw-Hill Book Company, New York, 1962, p. 68.

3. Dow Corning Corporation.

SECTION 8

MICROCIRCUITS

At the present stage of understanding and applying the theory of radiation effects in semiconductors, prediction of complete microcircuit performance is not feasible. In this section it will be shown that transistors in microcircuit configurations have the same essential characteristics as discrete transistors. The additional problems associated with microcircuits--isolation and parasitic capacitances--do not cause enough variation to alter the analysis of transistor gain degradation for discrete devices presented in Section 5. Consequently the techniques of damage prediction presented in Section 5 enable the designer to analyze the susceptibility of microcircuits to radiation by first determining gain degradation of the transistor elements and then determining the effect of this degradation on total circuit operation. For microcircuit elements in which the three individual transistor leads are accessible without parallel circuit elements, gain and base transit time measurements are easily made for prediction. When this is not possible, the base transit time can be estimated from manufacturers' data on base width and doping levels. For example,

$$t = \frac{W_b^2}{2D}$$

where D based on doping is obtained from Figure 7.1 (page 7-5).

Four types of integrated circuits are currently available: hybrid, thin film, monolithic, and compatible.[1] The hybrid approach uses discrete devices interconnected and packaged in a single can, hence is not different from conventional discrete devices. The thin film transistor type of circuit is still under development and not economically feasible at this time. The monolithic technique consists of a complete circuit or array of circuits in which the active and passive elements are all formed within a single silicon chip. The compatible integrated circuit contains active elements within the silicon chip, with thin film passive elements deposited on the surface of the chip. Consequently only the monolithic and compatible assemblies are considered, since these types consist of active components within the same silicon die.

Isolation of the components is an important factor in monolithic microcircuit operation. The two most common techniques of isolation are diode and dielectric. At present, diode or junction isolation is the most economical for mass production of monolithic microcircuits. However, the advantages of substituting a dielectric barrier for the isolation diode make dielectric isolation very attractive for monolithic circuits in the future when processing steps and costs are reduced.

A typical pair of monolithic integrated circuit transistors with their isolation diodes is shown in Figure 8-1. These are n-p-n transistors integrated in a low doped p-type substrate. Electrically the transistor pair can be represented as shown in Figure 8-2 as two discrete transistors and two isolation diodes. The p-sides of the isolation diodes are electrically connected and maintained at a negative potential to keep the diodes reverse-biased. The most important effect of the additional diode is the added parasitic capacitance associated with the diode. This capacitance is made as small as possible by low doping in the substrate and by a large reverse bias on the junction. Even so, the time delay associated with the relatively large isolation diode area and the large collector body resistance makes the frequency response of this transistor lower than the same transistor fabricated as a discrete component.

Another obvious difference between the discrete transistor and the monolithic integrated circuit transistor is the collector fabrication. Since the collectors must be electrically isolated, the collector contact is at the top surface rather than at the substrate. The collector current therefore travels a long circuitous path to the collector contact. This increases collector resistance and results in poor saturation voltage characteristics. A low resistance path for the collector current partially alleviates this problem. This is done by diffusing a heavily doped n^+ layer into the substrate before depositing the n-type epitaxial layer. The function of the n^+ regions directly under the collector contacts is to prevent the formation of a rectifying contact at the aluminum-silicon interface. For a good ohmic contact to n-type silicon, the n^+ region must have an impurity concentration greater than 5×10^{18} atoms/cm^3. The collector resistance can be reduced to that of a discrete transistor[2] by diffusing the n^+ regions under the collector contacts deep so that they penetrate through the n-type epitaxial layer to meet the n^+ buried layer. This step, however, requires extra processing and masks and results in higher costs.

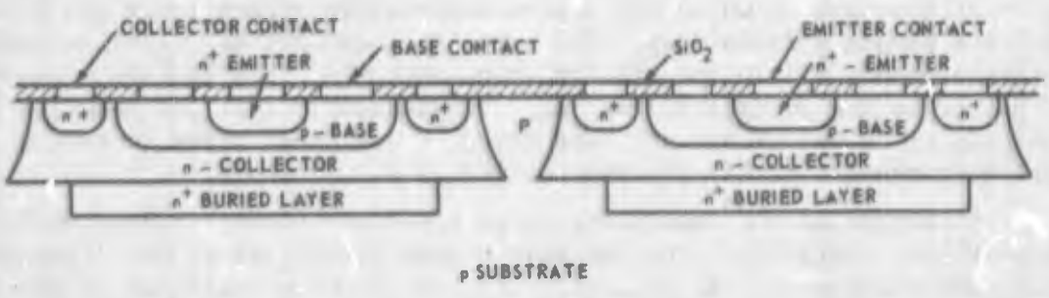


Figure 8-1. Monolithic microelectronic n-p-n transistors

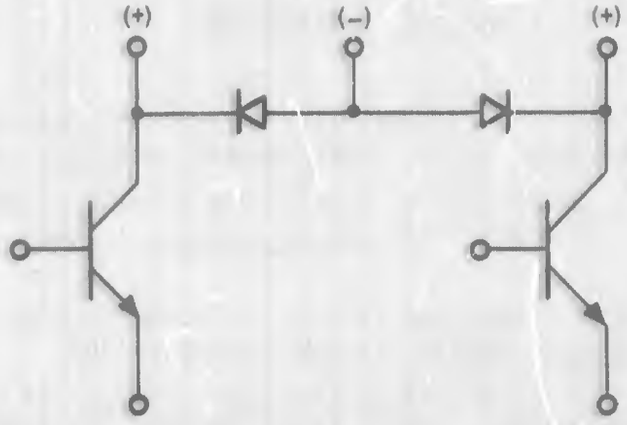


Figure 8-2. Two monolithic integrated circuit transistors with isolation diodes

The p-n-p base-collector-substrate region forms a parasitic transistor which has a typical low gain of the order of 0.04, and therefore is not a problem. This low gain results from poor emitter efficiency of the base region and low transport efficiency across the thick n layer. If the n layer is gold-doped, the gain is further reduced.

As in discrete transistors, the geometry and doping ranges of microcircuit transistors are determined by frequency, power and application. Consequently, the transistor elements in monolithic integrated circuits have the same doping and geometry as modern planar discrete transistors designed for the same range of performance characteristics.

The integrated circuit transistor is the same as the discrete epitaxial planar transistor except for the additional time delay due to the isolation diode and the increased saturation voltage due to the higher collector resistance. Consequently, the displacement and surface radition damage effects are similar. This was confirmed by reactor testing of transistors within integrated circuit chips. Only special types of transistor elements were tested, which did not have internal circuits attached to their base, collector or emitter leads. The empirical damage factors of these integrated circuit transistors were comparable to discrete transistor empirical damage factors. Messenger[3] and Hamman[4] also showed that the gain degradation of transistors behaved the same in integrated circuits as in similar discrete transistors. Hence, the prediction techniques from Section 5 may be directly applied to transistors in monolithic integrated circuits.

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3. G. C. Messenger, "Radiation Effects on Microcircuits," IEEE Trans on Nuclear Science, NS-13, 141-159, December 1966.
4. D. J. Hamman, "Space Radiation Effects in Integrated Circuits," IEEE Trans on Nuclear Science, NS-13, 160-167, December 1966.

ADDENDIX A

MEASUREMENT OF BASE TRANSIT TIME

A.1 BASE TRANSIT TIME BRIDGE

A.1.1 Introduction

Differences in the base region characteristics (doping gradients and base widths) between transistors can be characterized by frequency response measurements such as f_α or f_T, or bridge measurements of the average base transit time t. Both techniques theoretically should yield the same geometry correction. In practical application, however, the base transit time method offers greater accuracy and ease of measurement.

An improved bridge arrangement for measuring base transit time described by Das and Boothroyd,[1] utilizes a low frequency signal excitation. This system offers several advantages over common base or common emitter frequency cutoff measurements $f_{\alpha b}$ or $f_{\alpha e}$. For example, to measure the response of a typical high frequency transistor, test frequencies in the range of 500 MHz for $f_{\alpha b}$, or 50 MHz for $f_{\alpha e}$ are required; whereas 5 MHz is sufficient for use with the transit time bridge and results in greater precision in specifying the desired base characteristics.

Another advantage is that fewer readings are required in order to determine an intrinsic base transit time with the bridge arrangement than with frequency response methods.

A third advantage is the low temperature dependency with the base transit time technique. High operating currents produce junction heating, which affects gain. In the frequency response methods the measurements ($f_t = h_{fe}f$) are directly influenced by the gain dependency on temperature, whereas with the base transit time bridge, the dc gain variations cancel out for high gain unirradiated transistors. (See equation A-19). However, pulsed dc bias levels can be used with the frequency response techniques to eliminate the temperature problem.

The base transit time bridge circuit is shown in simplified form in Figure A-1. An RF voltage or current much smaller than the dc bias levels is applied at the emitter. The R and C parameters in the base lead are adjusted to give a null between collector and base terminals. This procedure is repeated at several different emitter currents. The base transit time is then computed from the set of resistance and capacitance values of the bridge arms. The equation relating the transistor base transit time with the variables of the measurement bridge is derived in Section A.1.2, using nomenclature employed by Das and Boothroyd.

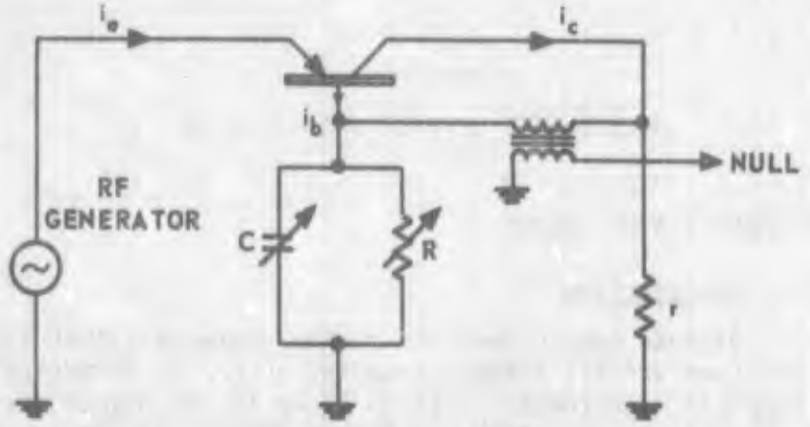

Figure A-1. Basic configuration of base transit time bridge

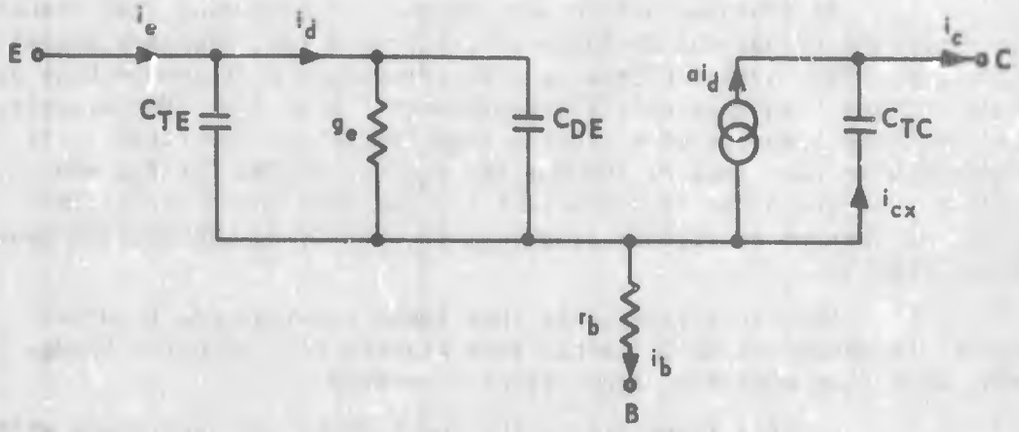

Figure A-2. Equivalent transistor circuit

A.1.2 Derivation of Base Transit Time in Terms of Bridge Parameters

The equivalent transistor circuit shown in Figure A-2 is used to derive the base transit time from the bridge balance equations. The relationship between the diffusion current in the base and the emitter current is

$$\frac{i_d}{i_e} = \frac{g_e + j\,\omega\,C_{DE}}{g_e + j\,\omega(C_{DE} + C_{TE})} \qquad \text{(A-1)}$$

The "intrinsic" or internal transistor short-circuit base transport current gain α is related to the common base short-circuit current gain α', including the effects of C_{TE} but not C_{TC} or r_b' as follows:

$$\alpha i_d = \alpha' i_e \tag{A-2}$$

Solving for α' and substituting in equation (A-1) gives

$$\alpha' = \alpha \left[\frac{1 + j\,\omega \dfrac{C_{DE}}{g_e}}{1 + j\,\omega \dfrac{C_{DE} + C_{TE}}{g_e}} \right] \tag{A-3}$$

Varnerin[2] defines the average base transit time as the ratio of the stored base charge to the emitter current. Hence,

$$t = \frac{Q_b}{I_E} \tag{A-4}$$

In terms of the equivalent circuit diagram

$$t = \frac{C_{DE}}{g_e} \tag{A-5}$$

which follows from equation (A-4) since $Q_b = C_{DE}\, V_{BE}$ and[3]

$$\frac{V_{BE}}{I_E} = \frac{1}{g_e} = \frac{kT}{q}\,\frac{1}{I_E} \tag{A-6}$$

Here V_{BE} is the emitter-base junction voltage.

The total time t' that injected carriers spend traveling from the emitter to the collector is given by

$$t' = \frac{C_{DE}}{g_e} + \frac{C_{TE}}{g_e} = t + C_{TE} \left(\frac{kT}{q} \right) \frac{1}{I_E} \tag{A-7}$$

where the delays at the collector junction and the influence of the transistor package are assumed to be negligible. From equation (A-3), α' becomes

$$\alpha' = \left[\frac{1 + j\,\omega\,t}{1 + j\,\omega\,t'}\right] \alpha \qquad \text{(A-8)}$$

Neglecting the effects of r_b' and C_{TC},

$$\alpha_o \, i_{g_e} = \alpha i_d \qquad \text{(A-9)}$$

where α_o is the low frequency, short circuit common base current gain.

The ratio of the currents (i_{g_e}/i_d) is given by

$$\frac{i_{g_e}}{i_d} = \frac{g_e}{g_e + j\,\omega\,C_{DE}} = \frac{1}{1 + j\,\omega\,\frac{C_{DE}}{g_e}} = \frac{1}{1 + j\,\omega\,t} \qquad \text{(A-10)}$$

Combining equations (A-8), (A-9) and (A-10) and solving for α' yields

$$\alpha' = \frac{\alpha_o}{1 + j\,\omega\,t'} \qquad \text{(A-11)}$$

At bridge balance $V_{cb} = 0$; therefore

$$i_b\, r_b' = \frac{i_{cx}}{j\,\omega\,C_{TC}} \qquad \text{(A-12)}$$

or

$$i_{cx} = i_b\, j\,\omega\, r_b'\, C_{TC} = (i_e - i_c)\, j\,\omega\, r_b'\, C_{TC} \qquad \text{(A-13)}$$

But,

$$i_c = i_{cx} + \alpha i_d = (i_e - i_c)\, j\, \omega\, r_b'\, C_{TC} + \alpha'\, i_e \qquad \text{(A-14)}$$

Combining equations (A-14 and (A-11) gives

$$\frac{i_c}{i_e} = \frac{\dfrac{\alpha_o}{1 + j\, \omega\, t'} + j\, \omega\, r_b'\, C_{TC}}{1 + j\, \omega\, r_b'\, C_{TC}} \qquad \text{(A-15)}$$

If the signal frequency is chosen so that

$$\omega\, r_b'\, C_{TC} << 1$$

then

$$\frac{i_c}{i_e} \simeq \frac{\alpha_o}{1 + j\quad t'} = \alpha' \qquad \text{(A-16)}$$

At bridge balance the detector arms of the bridge yield the equation

$$\frac{R\,(i_e - i_c)}{1 + j\, \omega\, RC} = r\, i_c \qquad \text{(A-17)}$$

Inserting α' from equation (A-16) into equation (A-17) and equating real and imaginary terms gives

$$\alpha_o = \frac{R}{r + R} \text{ or } h_{FE} = \frac{R}{r} \qquad \text{(A-18)}$$

and

$$t' = \frac{RC\, r}{R + r} = \frac{h_{FE}\, r\, C}{h_{FE} + 1} \qquad \text{(A-19)}$$

where h_{FE} = dc current gain.

In practice the ideal bridge in Figure A-1 is modified by stray capacity in the bridge arms and by capacitance and inductance associated with the resistive elements of the bridge. This means that C must include all the capacitance in the base, both the variable and the fixed; while in the collector arm, stray capacitance C_c must be included together with the inductance L of the external resistance r. Equation (A-17) can be solved with the equivalent impedance replacing r,

$$\frac{r + j\,\omega\,L}{(1 - L\,C_c\,\omega^2) + j\,\omega\,r\,C_c} \qquad \text{(A-20)}$$

to yield

$$t' = \frac{(RC\,r) + L - r^2\,C_c}{R + r - R\,L\,C\,\omega^2} \qquad \text{(A-21)}$$

since $L\,C_c\omega^2 \ll 1$ and $r\,C_c\,t'\,\omega^2 \ll 1$. The third term in the denominator is generally negligible; therefore, the delay time measurements are independent of frequency in the frequency range where suitable bridge nulls can be achieved. The contributions of the second and third terms in the numerator are small for unirradiated devices but becomes increasingly important for transistors with degraded gains. The inductive component of r can become a significant factor in the measurement of the response of ultrahigh frequency transistors since very small r and C values are required in order to achieve bridge balance.

A.1.3 Transit Time Bridge Instrumentation

The transit time bridge schematic is shown in Figure A-3. An important element in this bridge is the variable nonreactive resistance[4] in the base circuit, which has a typical range of 30 to 10,000 ohms. The variable resistance element is a photoconductor, which changes resistance when exposed to variable lamp illumination. The lamp illumination is controlled with a constant voltage power supply and a series wirewound 10-turn potentiometer. The dial settings of the potentiometer are calibrated in photoconductor resistance. Bridge balance is accomplished by adjusting the potentiometer R-Dial and the variable capacitance C in the base for a detector null. Regulated current and voltage supplies are used for precise settings of the dc bias levels of emitter current and the collector-base voltage. For a fixed set of measurement conditions, bridge balance can be repeated with an error of less than one percent.

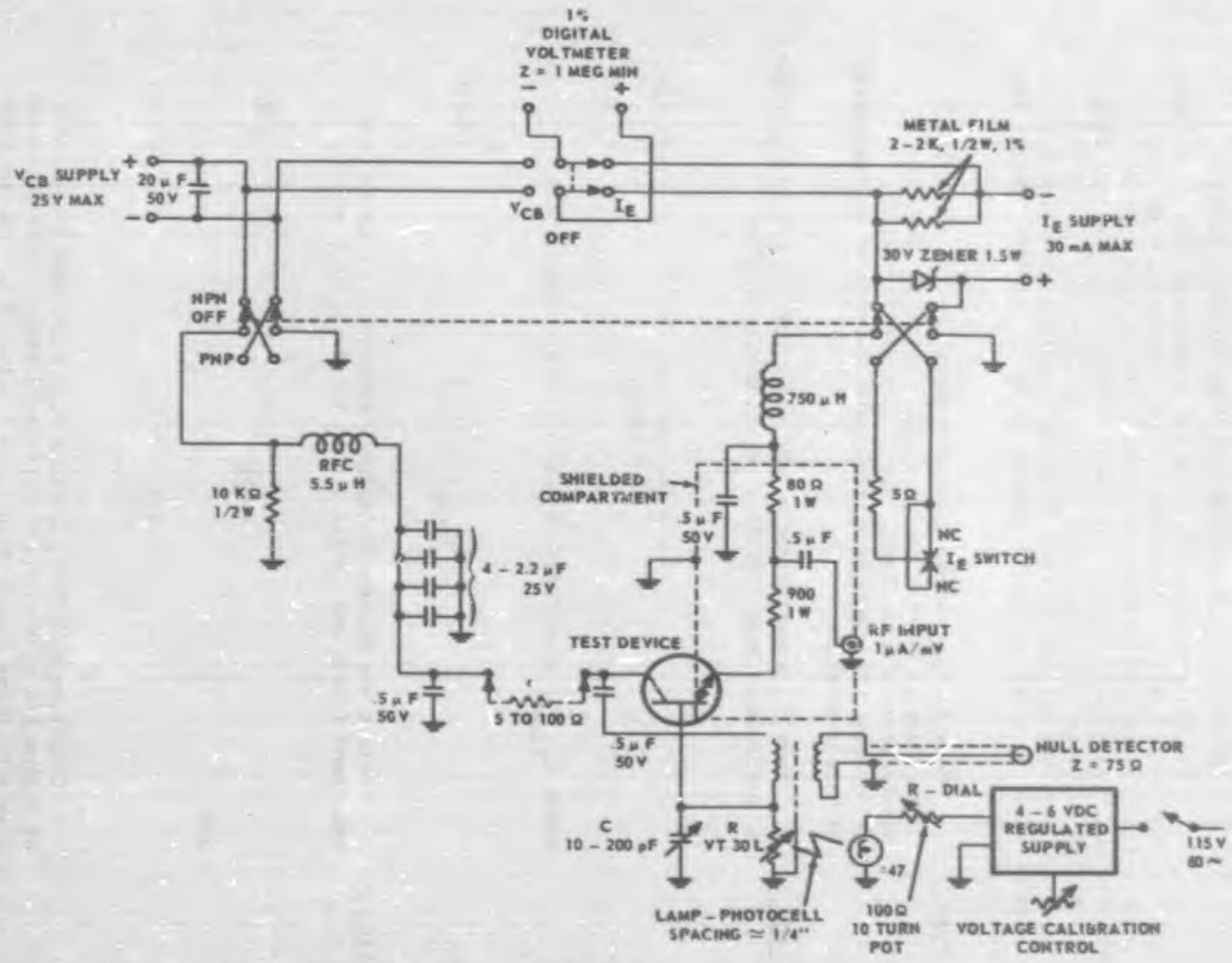

Figure A-3. Transit time bridge schematic

A.1.4 Procedure for Operating Base Transit Time Bridge

The following procedure is for a new transistor type that has not been tested previously on the bridge. Normally, when base transit time is measured on many transistors of the same type and manufacture, the same collector resistance, bridge frequency and range of emitter currents can be used for all the transistors. For a new type, however, the optimum of each of these important variables must be established in order to attain minimum error in the base transit time determination.

Step 1 Measure h_{FEO} versus I_C at the operating V_{CE} and ambient temperature to be used in the circuit or obtain from the manufacturer's data sheet. These data are for use in determining the approximate peak gain and current corresponding to this peak gain.

Step 2 From the manufacturer's data sheet for the device, calculate an approximate base transit time using the equation

$$t = \frac{1}{2\pi f_{T(max)}} \qquad \text{(A-22)}$$

where $f_{T(max)}$ is directly specified or determined from

$$f_{T(max)} = h_{fe} f \qquad \text{(A-23)}$$

Step 3 Select the proper collector resistance r by satisfying equations (A-24) and (A-25) within the range of R and C.

$$h_{FEO} = \frac{R}{r} \qquad \text{(A-24)}$$

and

$$t \simeq t' = r C \qquad \text{(A-25)}$$

Calculate r as R/h_{FEO}, using h_{FEO} from Step 1 and value of R from the middle of the resistance range. Then calculate r as t/C, using t from Step 2 and a value of C from the lower end of the capacitance range. If the values of r in the two calculations differ, select the value of r from equation (A-25) and readjust R to satisfy equation (A-24).

An exception to this rule is the low gain ultrahigh frequency transistor. Low gain in this case means that R is low if r is also required to be low from capacitance and high frequency response considerations. But the error in the bridge increases when R is near its lower limit because the photoconductor is near maximum conduction, which causes its resistance to be frequency-dependent as well as temperature-dependent. Therefore r should be increased to cause C to be as low as possible; but C must be given sufficient range to permit all measurements to be made for the desired range in emitter currents.

The lower limit of delay time measurement is set by the lower limits of r and C, since for unirradiated devices the gains are usually high and the range of R is not a problem. Values of r less than 5 ohms are not recommended because the series inductance L causes the inductance/resistance ratio of the resistor to increase as r decreases. The L component of r can be measured with a bridge such as the Boonton Radio Type 250-A RX instrument. Typical values of L are about 10nH. For minimum error in bridge measurements the same collector resistor r should be used for the complete range of emitter currents. The upper limit of delay time measurement is not a problem, because precision capacitors can be placed externally in parallel with the variable base capacitance C so that the total capacitance is the sum of the internal and external elements.

Step 4 — The proper RF bridge frequency for a particular type transistor is any frequency within a range of frequencies that results in the same R and C settings at bridge null for a fixed emitter current, collector-base voltage, and ambient case temperature. Since the same bridge frequency is required for a range of emitter currents, each end of the emitter current range must satisfy this condition. The correct emitter current range which is still unknown is arbitrarily defined initially to extend from the current level at peak h_{FEO} (Step 1) to a current level one decade lower. Typical bridge frequencies are 1MHz for transistors with base transit times from 1 to 2ns, to 5MHz for transistors with base transit times from 0.1 to 0.4ns. To minimize bridge errors (equations A-16, A-21), keep the frequency as low as possible but high enough for good null sensitivity.

Step 5 — Establish the proper emitter current range for the base transit time determination by making bridge measurements of the total delay time t' for equal increments of reciprocal emitter current, beginning with the current level at peak h_{FEO} (Step 1) and extending to levels approximately a decade lower. Compute

the time t' using equation (A-21) and plotting as a function of $1/I_E$ as shown in Figure A-4. Fit a straight line to this curve as near as possible to minimum t', but extend the line over a current range of at least a factor of 2.5 For subsequent transistors of the same type and manufacture measurements normally are needed only over the linear portion of the t' versus $1/I_E$ plot. For example, in Figure A-4 the indicated emitter current range for other Fairchild 2N1613 transistors is 25mA to 10mA. If measurement stability problems are encountered, subject all transistors to a surface stabilization cycle before measurement of base transit time, consisting either of heat treatment at 300°C for approximately 30 minutes or high current density operation with V_{CB} = 0 for several hours.

A.2 FREQUENCY RESPONSE MEASUREMENTS FOR DETERMINING BASE TRANSIT TIME

A.2.1 Introduction

The base transit time can be determined from data of the gain-bandwidth product f_T as a function of the reciprocal emitter current.

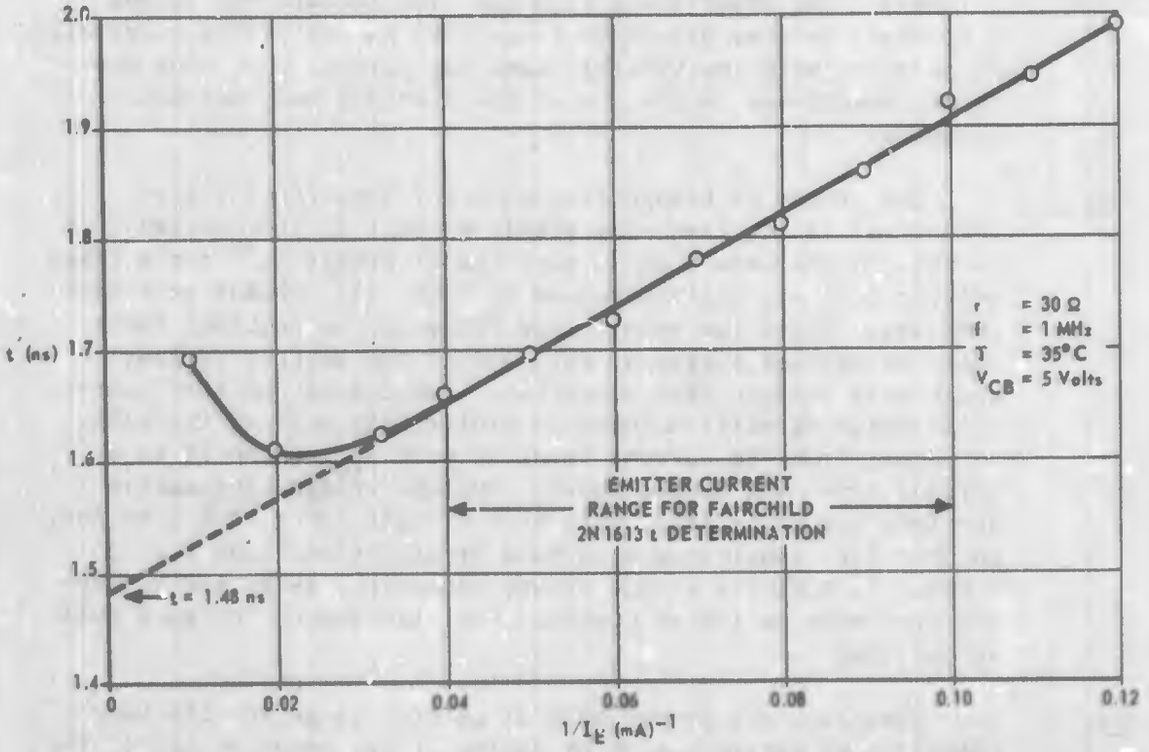

Figure A-4. Total delay time versus $1/I_E$ for 2N1613 transistor

The emitter-to-collector delay time t' is related to f_T by the equation

$$t' = \frac{1}{2\pi f_T} = \frac{1}{2\pi h_{fe} f} \qquad \text{(A-26)}$$

so that t may be determined from a plot of t' versus $1/I_E$ as discussed in Section A.1.2. The ac gain h_{fe} is measured on an immittance bridge, such as the General Radio Type 1607A bridge, using a measurement frequency f that is within a band of frequencies that produce a gain-frequency characteristic having 6dB attenuation per octave at constant emitter current and collector voltage (see Figure A-5). With the proper frequency, h_{fe} ranges from about 10 to 2 for typical transistor types. A narrow pulse bias current together with a low duty cycle reduce the possibility of junction heating. Measurements in room temperature ambients require no temperature control since the effect of temperature on low h_{fe} is negligible.

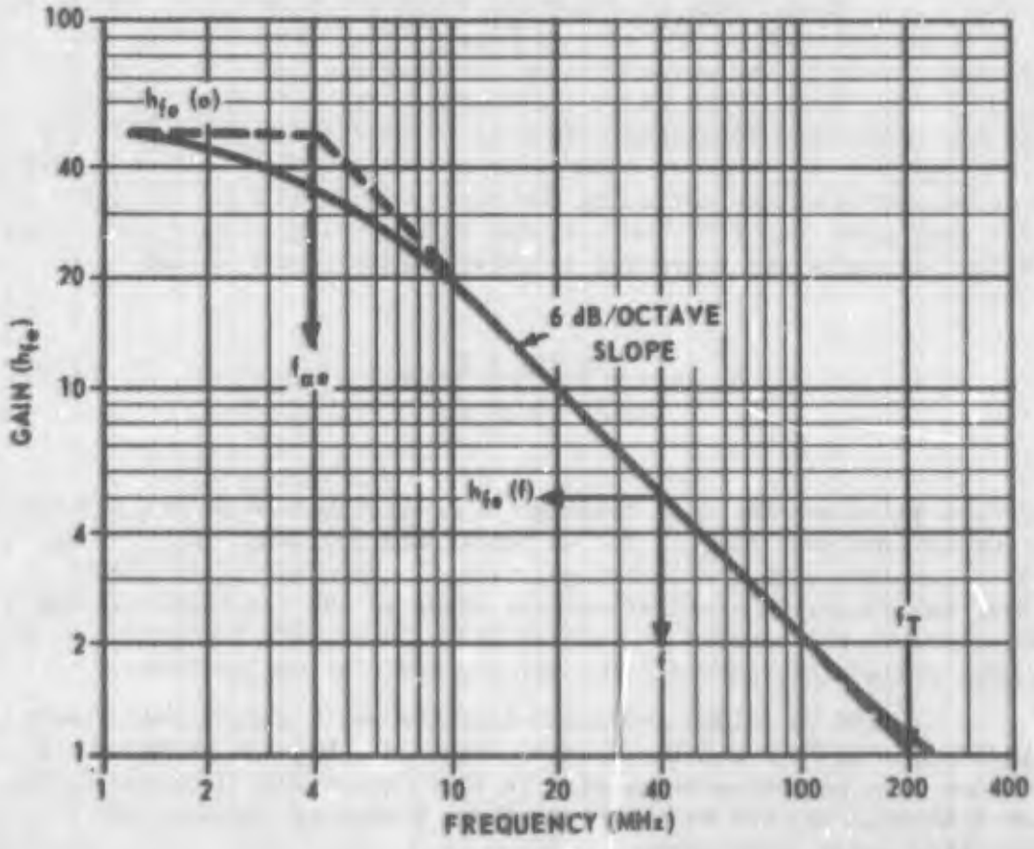

Figure A-5. Typical frequency response of a transistor at a constant emitter current and collector voltage

A.2.2 Test Configuration

The basic test arrangement as described in the General Radio manual is used for the GR-1607A bridge, with the exception of null detection, where an oscilloscope replaces the IF output meter. This change requires the use of a 20 kHz, approximately 85 percent sinusoidal modulation of the bridge RF signal frequency. These modifications are necessary for low duty cycle pulsed bias current, which the IF output meter is not capable of detecting. The input signal to the oscilloscope from the output of the IF amplifier must be dc-coupled to permit maximum resolution of the null. If a General Radio type 1216-A IF amplifier unit is used, the bridge output signal may be taken from the junction of the second detector and the cathode follower output stage. Bridge null for a fixed set of bias conditions is achieved by observing the oscilloscope waveform and adjusting the arms of the bridge for both an ac and a dc zero level for the output waveform. When the correct null is attained, the sinusoidal 20 kHz waveform is displaced above the zero level. Excellent results are obtained with 100μs current pulses having a repetition rate of 10 pulses per second.

A pulsed bias grounded-collector arrangement for measuring h_{fe} for n-p-n transistors is shown in Figure A-6. Transistor Q_1 normally conducts until the pulse generator supplies a negative pulse to the base of Q_1. This turns off Q_1, allowing current to flow through R_3 and R_4. The pulse developed across R_4 is used as the base bias for the test device. The emitter current is measured with a Tektronix current probe and is set by adjusting the base pulse with R_3. For the circuit configuration of Figure A-6, the bridge measures i_b/i_e, not h_{fe}. The bridge settings are converted to obtain h_{fe} by the equation

$$h_{fe} = \frac{B\,M + j\,A\,M}{(B\,M)^2 + (A\,M)^2} + 1 \qquad \text{(A-27)}$$

where B, M and A are the dial readings taken from the GR bridge and the sign conventions specified in the GR manual are followed. h_{fe} can be measured directly with the GR bridge, using a grounded-emitter connection, but parasitic oscillations may occur in the test device. The damper circuits recommended by General Radio, used with the grounded-collector connection, should eliminate any oscillation problems.

The GR Bridge 1607A has fixtures which permit measurement of transistors in TO-5 and TO-18 cans. However, chips in normal power transistor cans cannot be measured. In fact, commercial instrumentation is not available for the measurement of the frequency response of low transit time power transistors.

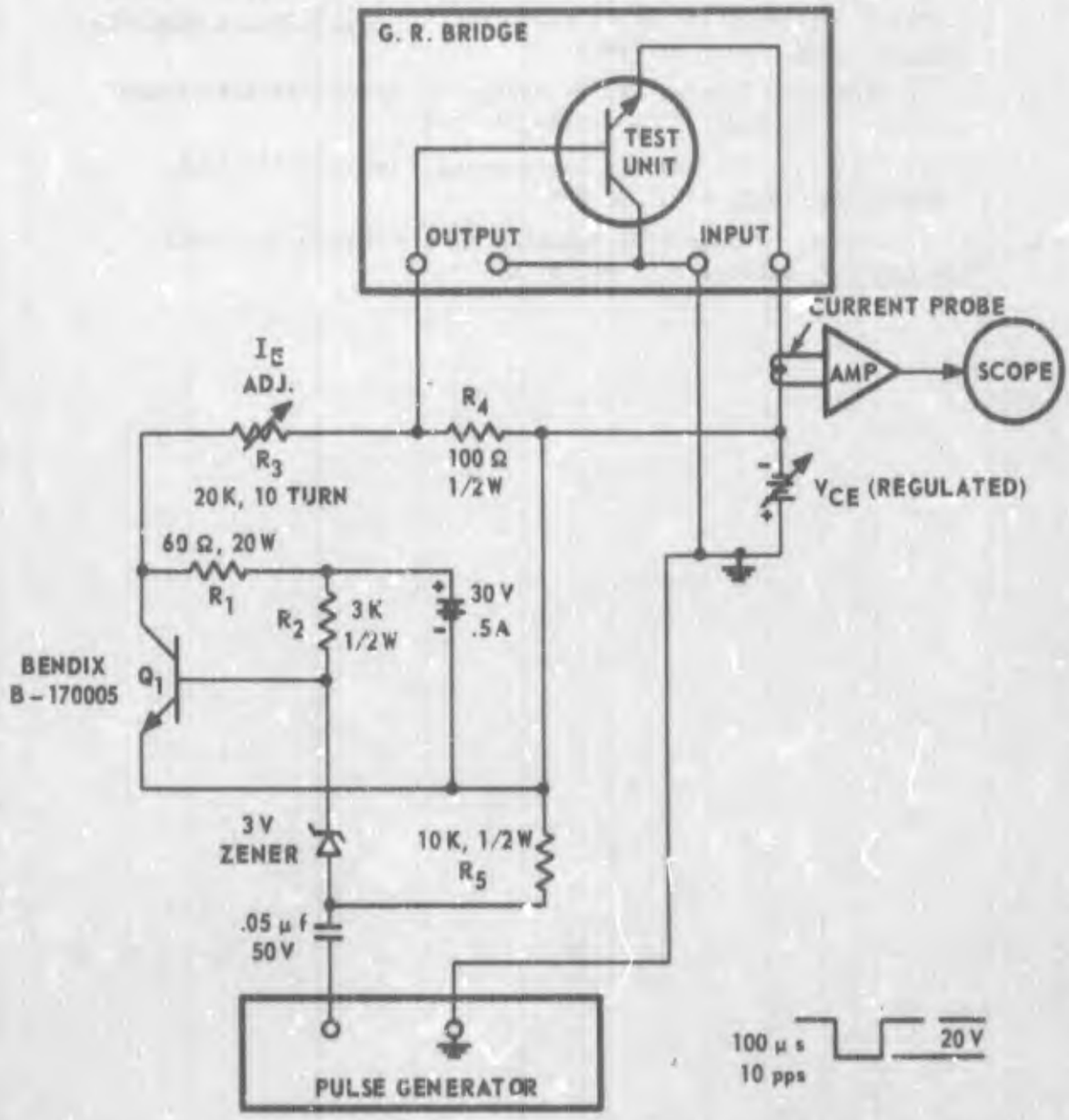

Figure A-6. n-p-n pulsed dc bias connections for GR 1607A bridge instrumentation

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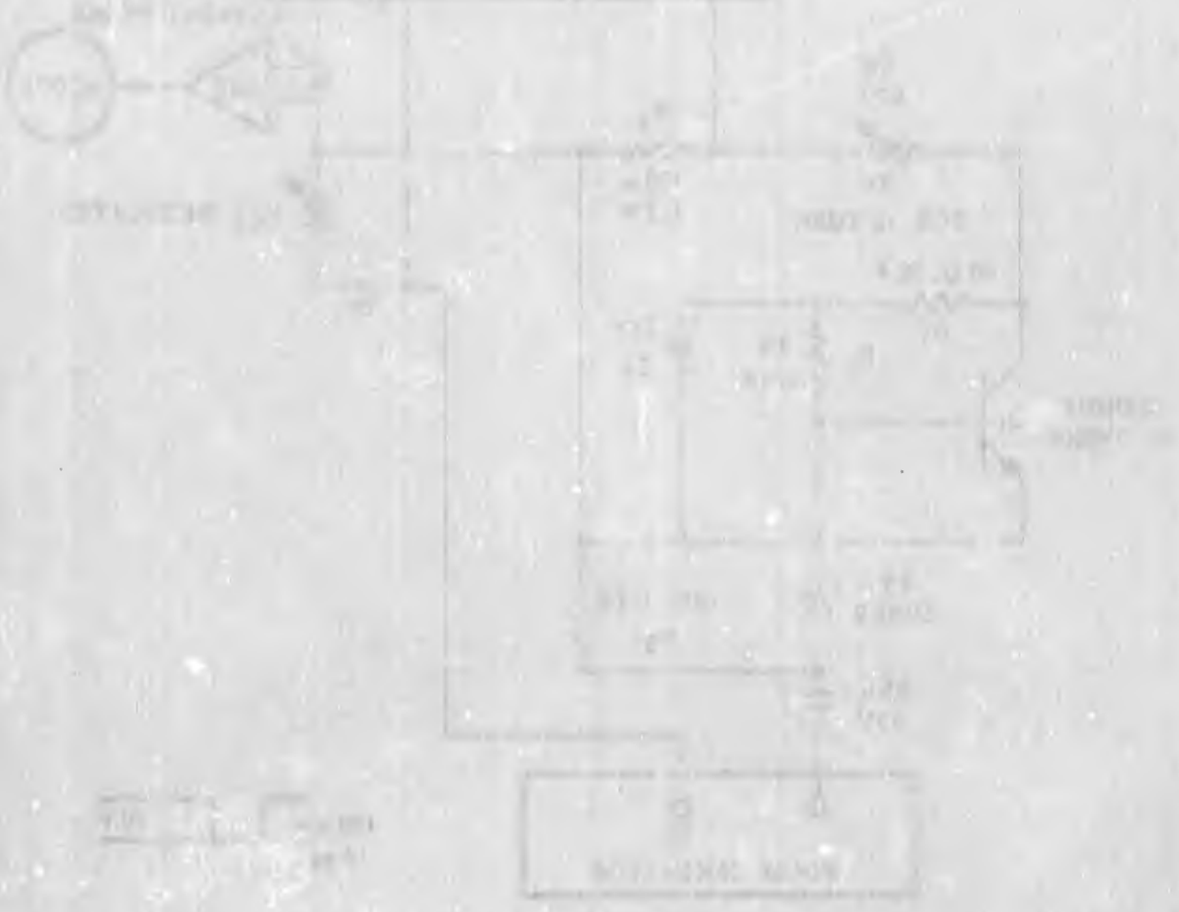

APPENDIX B

GENERAL MEASUREMENT CONSIDERATIONS

B.1 PERFORMANCE PARAMETERS

B.1.1 General

Pulsed measurement techniques are recommended for describing the performance parameters of h_{FE}, I_{CBO}, BV_{CBO}, BV_{CEO}, V_{BE} and $V_{CE(SAT)}$ for transistors, and V_F, I_R and BV for diodes. The pulse width of the applied current or voltage pulses must be sufficient to assure a steady state condition, and the pulse repetition rate must be kept low to prevent junction heating and time dependent surface effects. Standard testing pulse widths of 300 μs with a duty cycle ≤ 2 percent are acceptable. A curve tracer such as the Tektronix Type 575 oscilloscope may also be used when high accuracy is not required; however, for temperature sensitive performance parameters, care must be taken to avoid excess junction heating by photographing single pulse characteristics. The ambient case temperature must be very carefully controlled when measuring gain, leakage current and forward voltage since these parameters are very sensitive to temperature changes. Breakdown voltage and saturation voltage are less sensitive to temperature. A type of temperature controller that could be used to regulate the transistor case temperature above and below room temperature is shown in Figure B-1. This circuit uses a thermoelectric element and is capable of controlling any set temperature point to within ± 0.1°C over a range from 15°C to 160°C. The nominal operating temperature in this Handbook was chosen above room temperature at 35°C, so that the controller would always regulate in the heating mode Another reason for selecting 35°C is that most operating circuits result in transistor ambient case temperatures above room temperature. Equally good temperature regulation is possible below room temperature. At room temperature, however, alternate heating and cooling cycles are required, increasing the complexity of temperature control.

B.1.2 Low Level V_{BE}

Low level V_{BE} measurements are required in order to establish the ideal diode characteristic needed for prediction of post radiation V_{BE} at normal operating currents. The circuit shown in Figure B-2 may be used to obtain the low level V_{BE} - I_C data. It is very important to maintain a controlled ambient case temperature since V_{BE} is very sensitive to temperature changes. At T = 35°C, V_{BE} should change by approximately 61 mV per decade of I_C. These V_{BE} measurements are generally made from 10^{-9} to 10^{-6} A. The current measuring instrument should have a low meter drop of about 1 millivolt. The voltmeter should have high accuracy.

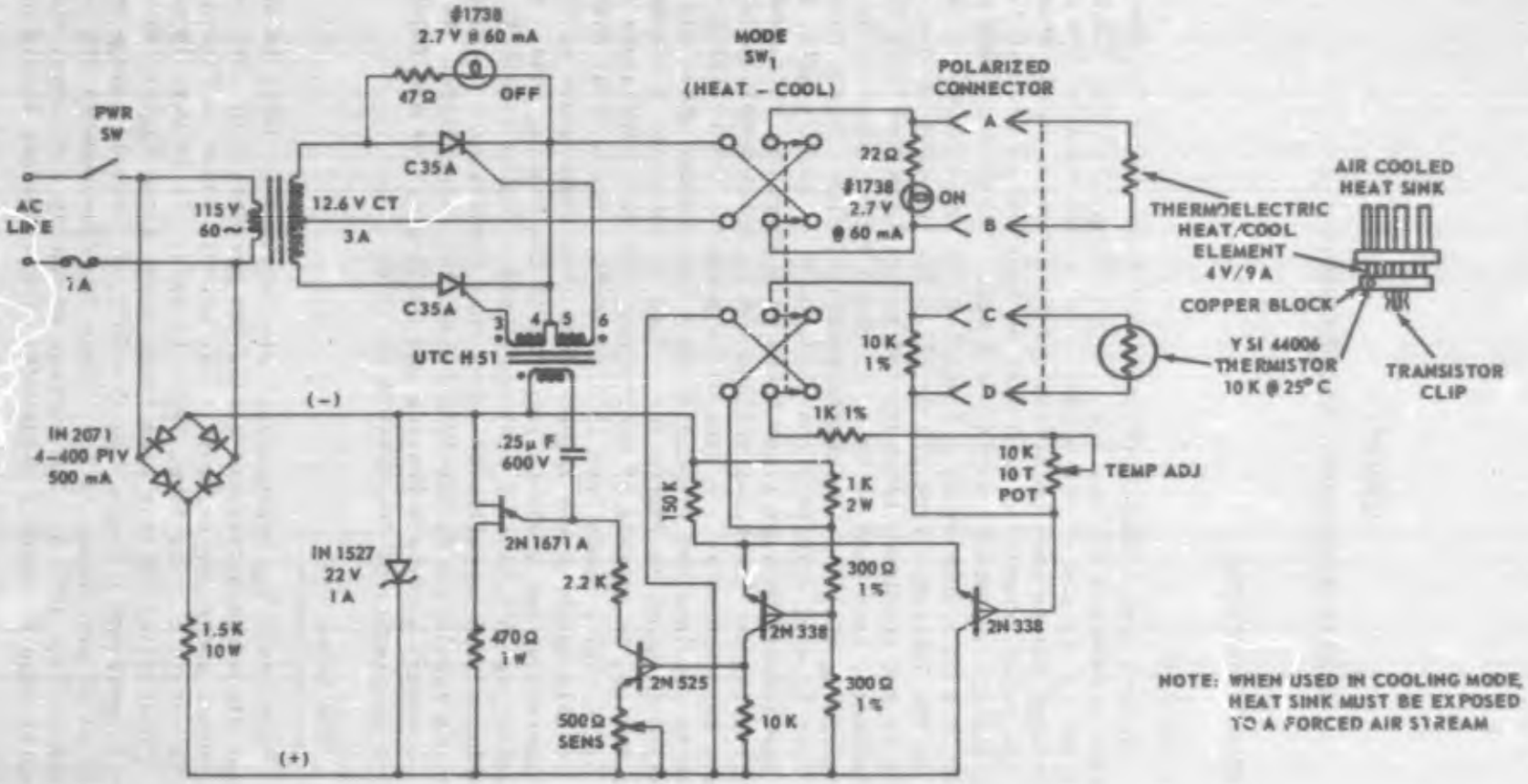

Figure B-1. Transistor temperature controller

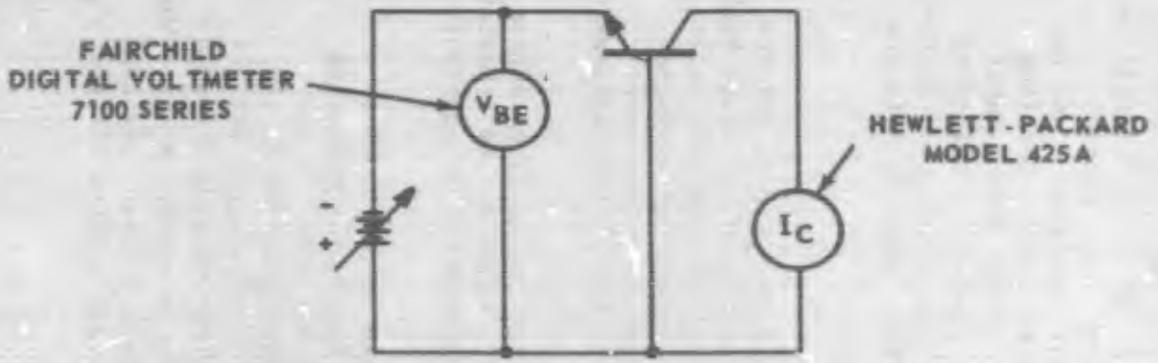

Figure B-2. Measurement circuit for low level V_{BE} - I_C data

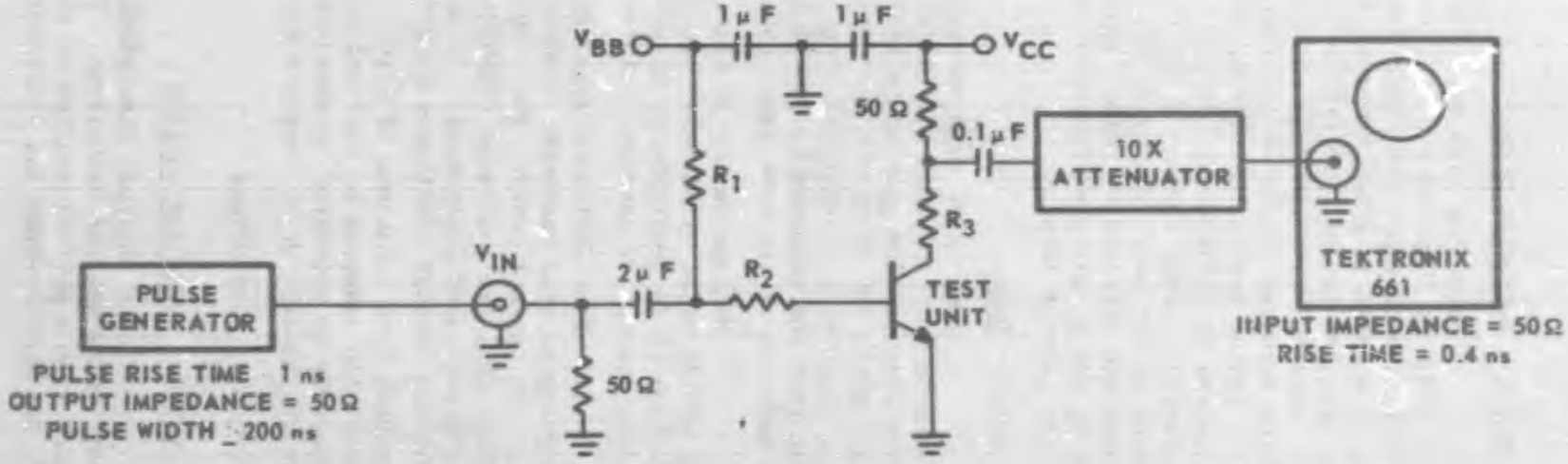

Figure B-3. Circuit for switching time measurements

B.1.3 Switching Times

Switching time measurements may be performed using the circuit shown in Figure B-3. The best switching waveforms are obtained when certain conditions are observed. First, all circuit components should be mounted as close together as possible but with the input and output circuits isolated to reduce coupling effects. Next, the test circuit together with the test transistor should be attached directly to the input terminal of the oscilloscope, eliminating output cabling. Finally, proper impedance matching between the test arrangement and the oscilloscope is achieved by using a tapped load resistance. Coupling the collector output through a capacitor directly to the 50-ohm input impedance of the oscilloscope is not recommended because the switching waveforms are affected by stray capacitance with this technique. Resistances R_1 and R_2 are used to adjust the base current, while R_3 sets the collector current level.

B.1.4 Gain

Commercial gain measuring instruments do not meet all the requirements for radiation effects work. These requirements include high accuracy over a wide gain range from h_{FE} = 0.1 to 1000, low duty cycle ($\leq$ 2 percent), 300 μs pulses and a wide range of current and voltages. The low duty cycle (preferably single pulse) is necessary to prevent heating from the measurement itself and assure that all of the measurements made are at the same junction temperature.

Minimum device ON time during the measurement also reduces damage modification or annealing in the test device which may be important. In addition it is desirable to be able to make measurements at constant collector current or constant emitter current.

Four different gain testers were used in the studies culminating in this handbook. Two were built by Bendix for measuring gain at low current levels; the other two, a Birtcher Model 70 and Fairchild 500, are available commercially. The Fairchild 500 is the most sophisticated instrument. It measures gain at constant collector current and through additional plug-in circuit boards extends the gain measurement from a minimum of 2 to 0.2 over a reduced current range. The Birtcher also measures at constant collector current. These data can subsequently be converted to measurements at constant emitter current either graphically or by computer program.

B.2 PHYSICAL PARAMETERS

B.2.1 Areas and Lengths

The physical dimensions of a semiconductor device can be measured using optical techniques. The emitter and base areas are obtained from a photomicrograph of the top surface of the semiconductor chip. The emitter-base and collector-base junction boundaries, the

metallization areas and the regions of silicon dioxide surface protection are clearly visible from photomicrographs, such as the example shown in Figure 4-3. If the device is nonepitaxial, the length of the collector region W_c can be obtained directly from a photomicrograph of a cross-sectional cut through the chip. For thin epitaxial transistors, the emitter depth, base depth and W_c are all obtained by beveling, staining and counting interference fringes on a photograph of a sectioned sample.[1,2]

B.2.2 Impurity Concentration from Junction Capacitance

The impurity concentration of the lightly doped side of an unirradiated non-gold-doped abrupt junction can be determined from junction capacitance measurements using the equation

$$N_o = \frac{2(V_j + V_T)}{q\,\epsilon}\left(\frac{C_j}{A_j}\right)^2 = 1.2 \times 10^{31}\,(V_j + V_T)\left(\frac{C_j}{A_j}\right)^2 \qquad \text{(B-1)}$$

where V_T = junction built-in potential, which varies from approximately 0.6 to 0.8 volt for silicon. If the device is irradiated or gold-doped, the measured junction capacitance is approximately correct for the N_o determination when the bridge frequency used to make the capacitance measurement is 100 KHz or higher. If the junction is not abrupt, equation (B-1) may still be used to find N_o providing large reverse voltages V_j are used in the capacitance measurements. Note that reverse voltage requires a summation of V_j and V_T. The junction capacitance C_j is the voltage dependent capacitance; therefore the voltage invariant capacitance must be subtracted from the measured capacitance between terminals. This is accomplished by plotting terminal capacitance as a function of $(V_j + V_T)^{-0.5}$ and extrapolating the curve to infinite voltage as shown in Figure B-4.

B.2.3 Diode Minority Carrier Lifetime

The minority carrier lifetime τ_o of a diode at different current levels I_F can be calculated from the equation

$$\tau_o = \frac{\left(\frac{2\ kT}{q}\right)}{\text{Slope of linear portion of } V_o(t) \text{ function}} \qquad \text{(B-2)}$$

where $V_o(t)$ is the transient decay of the open-circuit voltage across a diode that was conducting. The slope of the $V_o(t)$ versus t curve will be in volts, The circuit used to obtain the transient response $V_o(t)$ is shown in Figure B-5. A special-purpose mercury relay switch with normally closed contacts is employed to instantaneously open (approximately 2 ns) the circuit. The relay coil pulse input is about 10 ms with a one percent duty cycle. The diode conduction current is sensed by a current probe, amplified and displayed on an oscilloscope.

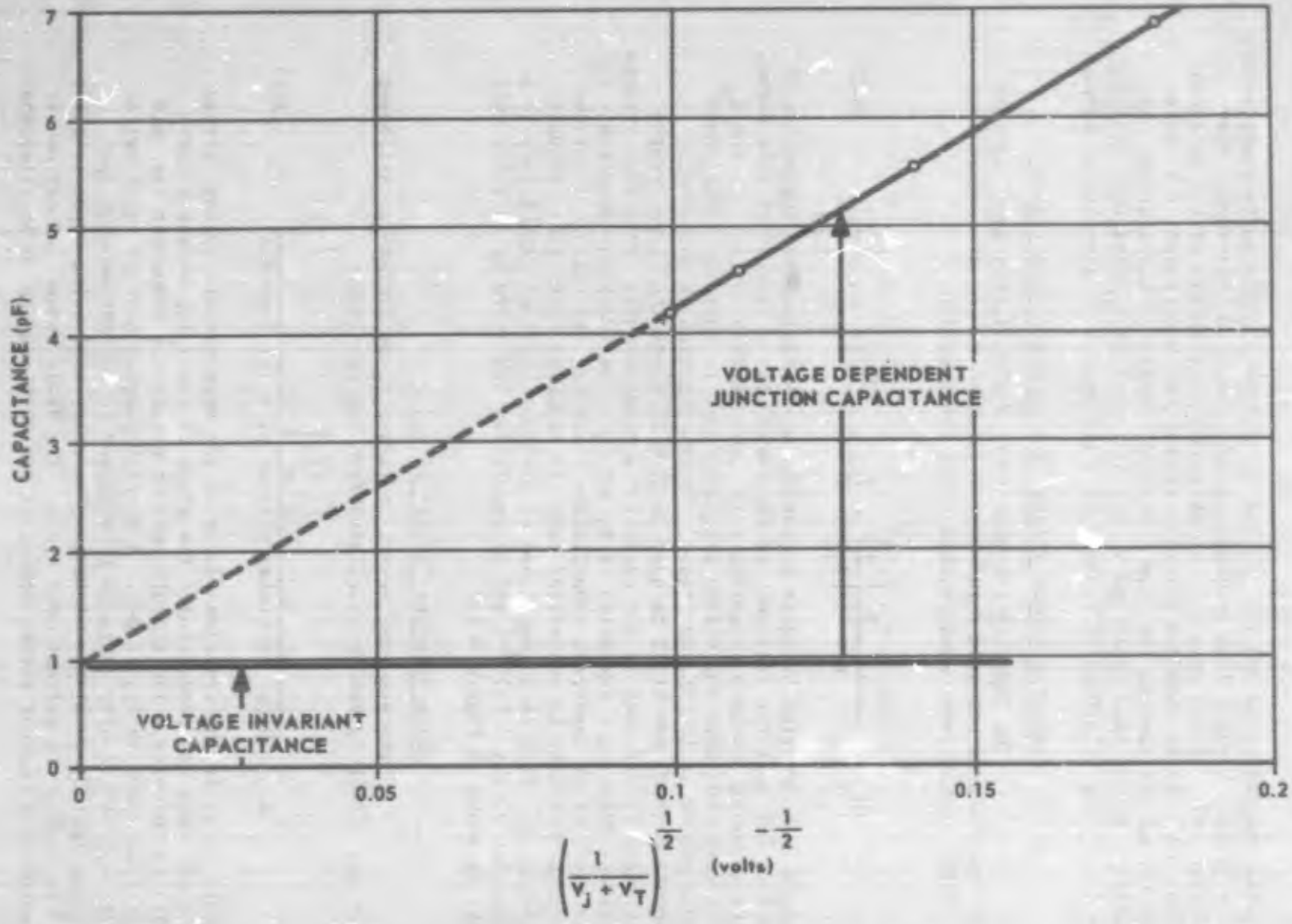

Figure B-4. Determination of junction capacitance

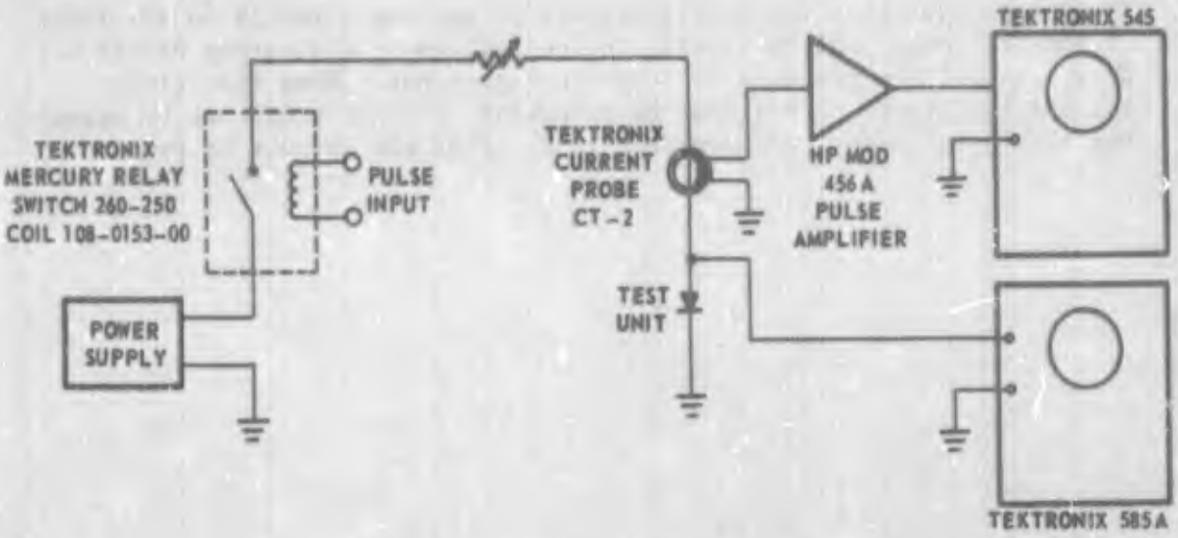

Figure B-5. Diode lifetime measurement circuit

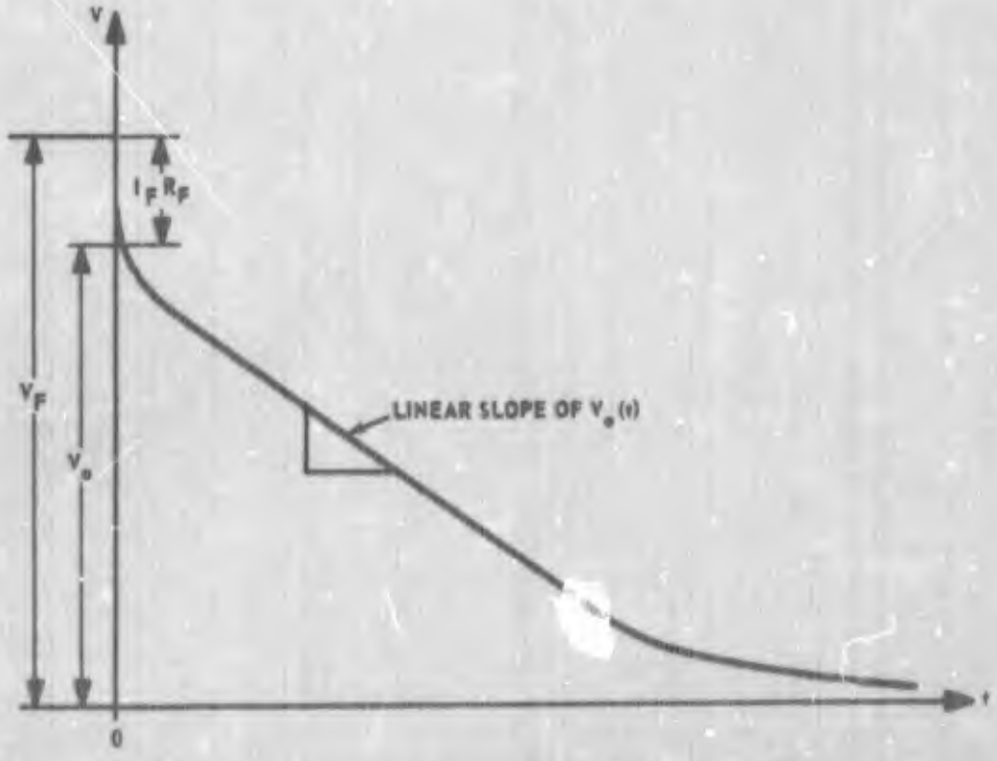

Figure B-6. Open circuit diode recovery voltage

It is important that the entire circuit be mounted directly to the input of the Tektronix 585A to reduce ringing effects in the output waveform. A typical voltage response is shown in Figure B-6. Note that diode forward resistance R_F may also be determined with this circuit by measuring the instantaneous voltage drop $I_F R_F$ after the circuit is ope-

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Radiation Damage Technology

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UNCLASSIFIED
Security Classification

DOCUMENT CONTROL DATA - R&D
(Security classification of title, body of abstract and indexing annotation must be entered when the overall report is classified)

1. ORIGINATING ACTIVITY (Corporate author) The Bendix Corporation, Research Laboratories Division Southfield, Michigan 40876	2a. REPORT SECURITY CLASSIFICATION UNCLASSIFIED 2b. GROUP

3. REPORT TITLE
HANDBOOK FOR PREDICTING SEMICONDUCTOR DEVICE PERFORMANCE IN NEUTRON RADIATION

4. DESCRIPTIVE NOTES (Type of report and inclusive dates)
October 1965-June 1967

5. AUTHOR(S) (Last name, first name, initial)
Frank, Max; Taulbee, Carl D.

6. REPORT DATE	7a. TOTAL NO. OF PAGES	7b. NO. OF REFS
August 1967	184	52

8a. CONTRACT OR GRANT NO. AF 29(601)-7110	9a. ORIGINATOR'S REPORT NUMBER(S)
b. PROJECT NO. 1831	AFWL-TR-67-54
c. Task No. 183108	9b. OTHER REPORT NO(S) (Any other numbers that may be assigned this report)
d.	

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11. SUPPLEMENTARY NOTES	12. SPONSORING MILITARY ACTIVITY
(Distribution Limitation Statement No. 2)	AFWL (WLDN) Kirtland AFB, NM 87117

13. ABSTRACT

Procedures are presented for predicting transistor and diode electrical performance after permanent damage from neutron radiation. The prediction techniques are illustrated with examples of step-by-step calculations to facilitate use by circuit designers familiar with semiconductor device operation but not familiar with radiation damage effects in the devices. The handbook contains predictions of transistor current gain, saturation voltage, forward voltage, breakdown voltage, leakage current and switching time, forward voltage of power diodes, and transistor current gain in microelectronic configurations. Measurements of important physical device parameters needed in the prediction equations are described in detail. Also described is a procedure for measuring radiation test exposure in Radiation Damage Units (RDU) by using transistor Radiation Damage Monitors (RDMs).

DD FORM 1 JAN 64 1473

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14. KEY WORDS	LINK A		LINK B		LINK C	
	ROLE	WT	ROLE	WT	ROLE	WT
Radiation effects						
Prediction techniques						
Silicon transistors						
Diodes and rectifiers						
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