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Low-Light-Level Limitations of Silicon Junction Photodetectors

by

Joseph S. Brugler

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ABSTRACT

The properties of silicon junction photodetectors have been investigated with the goal of improving low-light-level performance of a reading aid for the blind. This application requires an image-forming mosaic of photodetectors, which may be conveniently fabricated by use of integrated circuit technology. Solid-state imaging is particularly attractive because of the low resolution (100 to 200 elements) needed for the reading-aid system.

Attention is focused upon photodetector operation utilizing the charge-storage technique, because of the usefulness of this method in increasing the signal level in scanned image applications. The signal and noise transmission properties of the basic charge-storage circuit are analyzed, with the assumption of an ideal switching element. The primary contributors to output uncertainty are found to be dark current and its associated 1/f noise because of the lowpass nature of the circuit.

Practical charge-storage circuits, based upon the available bipolar and metal-oxide-semiconductor (MOS) technologies, are studied. Low-light-level performance is determined to be most severely limited by switch imperfections. The low-light-level operation of the charge-storage phototransistor is analyzed in detail. Performance is shown to be increasingly degraded as the light level is reduced due to influence of the emitter-base junction. The use of an MOS switch is considered, and capacitive feedthrough found to be excessive. A charge integration scheme is proposed to circumvent the feedthrough charge, leaving the most significant noise source to be an unusual "charge pumping" effect. The charge pumping phenomenon is studied in detail in order to establish its physical basis.

When photosensing arrays are investigated, spatial nonuniformities are found to limit low-light-level performance most severely. Optimum photosensing areas are determined for phototransistor and MOS arrays in the reading aid application. Design formulas for these optima are given. The MOS array is found to offer the best low-light-level performance of the two schemes, although requiring a relatively larger photosensing area.

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SYMBOLS

Symbol usage follows the IRE Standards on Letter Symbols for Semiconductor Devices, 56 IRE 28S1. For example $i_P = I_P + i_p$, where i_P = instantaneous total current, I_P = dc current, i_p = ac current. The subscript P designates photodiode parameters.

A area (cm^2 or mil^2)

- A_e area of phototransistor emitter
- A_g area of MOS transistor gate
- A_o area of letter element to be imaged
- A_p area of photodiode
- A_v area of MOS gate overlapping drain

C capacitance (F)

- C_e phototransistor emitter capacitance
- C_i input capacitance or integrator capacitance
- C_p photodiode capacitance
- C_{gd} gate-to-drain capacitance of MOS transistor
- C_{ox} oxide capacitance of MOS transistor
- C_{ea} phototransistor emitter capacitance per unit area (F/cm^2)
- C_{oa} MOS oxide capacitance per unit area
- C_{pa} photodiode capacitance per unit area

f frequency (Hz)

- f_d 3 dB bandwidth
- f_k Frequency for equivalent 1/f and shot noise
- f_n equivalent noise bandwidth
- f_o low-frequency 1/f noise breakpoint

F_{eff} lens effective F-number

F_{eq} lens equivalent F-number

f memory factor of charge-storage circuit

g generation rate per unit volume (cm^{-3}) or MOS channel conductance (mhos)

G dc forward transfer impedance of charge-storage circuit (Ω)

h_{FE} phototransistor dc current gain

H(f) frequency response function

i current (A)

- i_B instantaneous total switching diode current
- i_p instantaneous total photodiode current
- i_e ac excess noise current
- i_g ac generation noise current
- i_p ac photodiode noise current
- I_G dc generation current
- I_K dc peak output current
- I_p dc photodiode current
- I_T dc MOS transistor substrate current
- I_1 switching diode saturation current

L MOS transistor gate length (cm or mils)

m lens linear magnification

N total number of elements in array

N_T trap distribution in energy band gap ($cm^{-2}\ V^{-1}$)

Q		charge (C)
	Q_C	capacitive feedthrough charge
	Q_G	thermally generated charge
	Q_P	photogenerated charge
	Q_T	trapped charge under MOS gate
	Q_{FA}	free charge under MOS gate per unit area (C/cm^2)
	Q_{TA}	trapped charge under MOS gate per unit area
r		ratio of sample time to circuit time constant
R		load resistance of charge-storage circuit (Ω)
R_i		input resistance driven by charge-storage circuit
$S_{h_{FE}}^{\hat{V}}$		sensitivity of peak output voltage to phototransistor current gain
SNR		signal-to-noise ratio
t		lens transmission
T		absolute temperature (°K)
T_i		integration time (sec)
T_s		sample time
v		voltage (V)
	v_B	instantaneous total voltage across switching diode
	v_K	instantaneous total peak output voltage
	v_O	instantaneous total output voltage
	v_P	instantaneous total voltage across photodiode
	Δv_P	instantaneous total change in photodiode voltage during integration time
	v_k	ac noise in peak output voltage

V_G	MOS gate pulse amplitude
V_K	average peak output voltage
ΔV_P	average change in photodiode voltage during integration time
V_R	reverse bias on MOS transistor source and/or drain
V_T	MOS transistor threshold voltage
V_{TO}	MOS transistor threshold voltage when $V_R = 0$

W	depletion layer width (cm)
Z	MOS transistor gate width (cm or mils)
α	factor giving low-light-level limit of charge-storage phototransistor
β	fraction of free carriers under MOS gate that recombine in substrate
γ_{mos}	$\frac{\text{p-p pumped charge variation}}{\text{p-p leakage charge variation with } m = 1}$
γ_{pt}	$\frac{\text{emitter capacitance}}{\text{photodiode capacitance with } m = 1}$
Γ	photodiode dark current per unit area (A/cm^2)
ϵ	worst-case variation of thermally generated charge among elements of array
η	responsive quantum efficiency
λ	wavelength (μ)
μ	worst-case variation of pumped charge among elements of array
ρ_o	page reflectance
ρ_p	photodiode reflectance
τ	charge-storage circuit RC time constant (sec)

Φ_p	instantaneous total light flux density on photodiode (photons/cm^2 sec)
Φ_I	average ambient flux density on reading matter
$\Phi_{I\|minmos}$	minimum usable ambient flux density with MOS array
$\Phi_{I\|minpt}$	minimum usable ambient flux density with phototransistor array
Φ_p	average light flux density on photodiode
ψ_f	Fermi potential (V)
ψ_s^o	surface potential with zero gate voltage (V)
ψ_s^-	surface potential with negative gate voltage
Ω	constant of integration

Physical Constants

c	velocity of light (cm/sec)
h	Planck's constant (joule-sec)
k	Boltzmann's constant (joule/°K)
q	electronic charge (C)
μ_p	hole mobility in inversion layer (cm^2/V-sec)

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Chapter I

INTRODUCTION

This study of the factors limiting low-light-level operation of silicon junction photodetectors was motivated by the specific application of a tactile reading aid for the blind [1,2]. This application requires an image-sensing array having a few hundred elements, upon which is focused an image of the printed material to be read. A binary decision is made by threshold circuitry at the output of each element to determine whether its portion of the image was dark (ink) or light (paper). The resulting signals form the basis of a vibrating image to be felt by the blind reader. The present hardware [3] uses a parallel-channel approach that connects each picture element to its vibrating tactile counterpart on a separate wire. The photosensing array is composed of closely spaced discrete phototransistors. An internal light source is provided to illuminate the reading material. This illuminator consumes excessive power, especially for the battery-operated device envisioned. Neither the comparator accuracy nor the channel-to-channel uniformity is adequate to enable the system to operate at lower levels of illumination. This deficiency, then, presented the twofold problem: (1) How can the system be configured to operate at lower illumination levels? and (2) What are the ultimate limits to be expected?

The problem of fabricating an image-forming mosaic of photosensors was first posed by Carey nearly one hundred years ago [4]. The use of present-day integrated circuit technology for this task is a matter of considerable current interest [5,6,7,8,9]. The reading aid application seems particularly well-suited for this technique since the required number of elements is small enough to enable high manufacturing yields. This approach requires that the picture elements be sequentially scanned, television-style, in contrast to the present parallel readout. While this entails more complicated scan generating circuitry, it drastically reduces the number of signal channels. This enables the use of more sophisticated signal processing circuitry in order to provide an accurate low-level comparator function. Another important advantage is that

signal output uniformity across the image should be much improved when all of the photosensors are integrated on a single substrate. Thus integration of the photosensing mosaic is expected to enable system operation at lower illumination levels than presently employed. For this reason, as well as others, fabrication of such mosaics is contemplated at the Stanford integrated circuits facility. The use of these mosaics thus answers the first question of the preceding paragraph. The second question is the subject of the remainder of this report.

Attention will be focused upon present-day silicon monolithic technology, including both bipolar and MOS (metal-oxide-semiconductor) techniques. The photosensor for such applications is almost always the junction photodiode, operated in a charge-storage mode [10,11]. This mode requires a switch for periodic signal readout. In Chapter II the properties of the charge-storage photodiode are considered with the assumption of an ideal switch. Particular attention is directed toward the signal and noise transmission properties of the charge-storage circuit. In Chapters III and IV, the performance limitations imposed by nonideal switching elements are analyzed. Signal readout through a junction is considered in Chapter III. This case includes the commonly used charge-storage phototransistor which is shown to have low-level problems of transfer-characteristic nonlinearity, degraded transient response, and increased parameter sensitivity. Use of an MOS transistor switch is investigated in Chapter IV. Large switching transients are shown to exist, which may be circumvented by a proposed charge integration scheme. Performance is then limited by a hitherto unreported "charge-pumping" phenomenon. In Chapter V the low-light-level properties of photosensing arrays using the charge-storage schemes of Chapters III and IV are compared, with particular reference to the blind reading aid application. Different optimum photosensing areas were found for the two cases, with the photodiode-MOS switch combination having the best ultimate low-light-level capability. Chapter VI is a summary and indicates avenues for further research.

Throughout this work an attempt has been made to adhere to the dictum of the principle of parsimony [12]: "Concepts are not to be multiplied beyond necessity."

Chapter II

NOISE PROPERTIES OF THE CHARGE-STORAGE PHOTODIODE USING AN IDEAL SWITCH

The charge-storage principle, as originated by Zworykin [4], made possible the first television camera tube. It continues extant in present-day image orthicons [13] and vidicons [14], and was first applied to junction photodiodes by Reynolds [15]. The need for charge storage arises from the fact that, in sequentially scanned applications, each element of the scanned array is interrogated for a small fraction of the time. For example, if there are N elements to be scanned, the fractional dwell time on each element is roughly $1/N$. If N is large, the amount of charge that can be delivered to the load by photocurrent during the dwell time is very small. However, if charge is stored at an element while the others are being scanned, and then delivered to the load when the element is sampled, the average output signal current is greatly increased. This is the key idea of charge storage, and enables an effective current gain approximately equal to the number of scanned elements. The principle is also useful in nonscanned applications. In such cases, the total charge delivered to the load is not increased by use of charge storage, but is delivered to the load during a short fraction of the time. The output current waveform is thus a succession of pulses having much higher peak value than the average photocurrent, and use of charge storage can be considered to effect a gain-bandwidth trade.

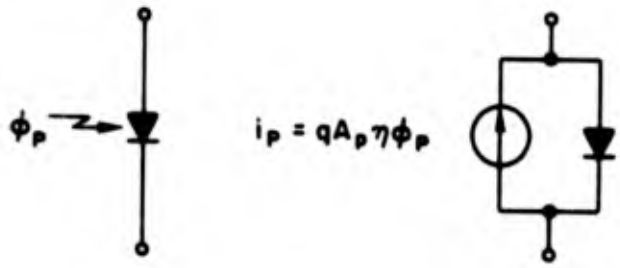
The essential requirements for the charge-storage mode of operation are therefore (1) a photoelectric source, (2) an energy storage element (always a capacitance), and (3) a switch. Requirements (1) and (2) are satisfied by the photocurrent and depletion-layer capacitance of a reverse-biased photodiode. This makes possible the use of photodiode arrays as targets in vidicon tubes [9,16], where commutation is accomplished by a scanning electron beam. This paper is concerned with all-solid-state imaging; in this connection requirement (3) is by far the biggest problem. At present, digital matrixing techniques are used in lieu of the scanning beam. In this chapter, an ideal switch will be assumed, and the discussion limited to diffused silicon planar devices.

The photoelectric and noise properties of the photodiode are first briefly examined. Charge-storage operation is then shown to be equivalent to low-pass filtering, and its properties are analyzed in terms of gain, bandwidth, and output signal-to-noise ratio.

A. The Silicon Planar Photodiode

1. Responsive Quantum Efficiency

We assume a diffused silicon planar p-n junction diode, with impinging radiation perpendicular to the plane of the junction. Photocurrent results from carriers liberated within the junction depletion region plus minority carriers created within the bulk that drift and diffuse to the depletion region. The latter component predominates for the diodes considered, since the carrier diffusion lengths are larger than the depletion region width [17]. For this case, a valid large-signal model for the photodiode [18] is shown in Fig. 1. The photogenerated current is represented by a current generator in parallel with



ϕ_p = absorbed flux density (photons $sec^{-1}cm^{-2}$)

η = responsive quantum efficiency

A_p = photodiode area (cm^2)

q = electronic charge (C)

i_p = photogenerated current (A)

Fig. 1. PHOTODIODE MODEL.

the diode having magnitude proportional to the impinging radiant flux. One can consider that the one-port I-V diode characteristic measured without illumination is simply shifted down the negative current axis a distance equal to the magnitude of the photocurrent. This simple model is valid for frequencies below values where carrier transit-time effects are important, and for reverse voltages below values where avalanche breakdown [19] is a factor.

The parameter η, called the responsive quantum efficiency [20], is here defined as the average number of carriers liberated per absorbed photon. It completely characterizes photodiode performance in the presence of radiation. Its magnitude is always less than unity (subject to the above condition of no avalanche effects) and depends on a number of device parameters, including radiation wavelength. Its maximum with respect to wavelength varies between the visible and near infrared depending on junction depth, and may be optimized [21,22] for the detection of contrast. A typical maximum value of η is 0.6.

2. Sources of Noise

a. Photocurrent Shot Noise

For all wavelengths to be considered ($< 1\ \mu$), the incident radiation is described by Maxwell-Boltzmann statistics [23]. The photons arrive as a "white" rain completely uncorrelated with one another. The mean square deviation in the photocurrent may be found by assuming random generation of current carriers with probability η. This is akin to the problem of partition noise in vacuum tubes [24] and gives the result that noise in the photocurrent is described by the full shot noise formula:

$$\overline{i_p^2} = 2qI_p\,df \qquad (2.1)$$

b. Generation Current

The photodiode is generally reverse biased, in which case a dc dark current flows. In silicon at room temperature, this

current is attributed mainly to carrier generation from mid-band impurity centers within the depletion region [25]. Its magnitude is given by

$$I_G = qgWA_p \triangleq \Gamma A_p \tag{2.2}$$

where

g = generation rate per cubic centimeter

W = depletion layer width (cm)

For linearly graded junctions, the generation current is therefore proportional to the cube root of the reverse bias. Measured values using discrete Fairchild FPM-100 collector-base junctions indicate that Γ may be 10^{-9} A/cm^2 at a few volts bias. Assuming that the diodes are fabricated with low dark current as a goal and that the photodiode voltage is approximately constant, this value will be used in subsequent calculations. As junction area is reduced, the ratio of diode area to perimeter decreases, and a perimeter-sensitive correction factor to Eq. (2.2) may be needed [8]. Its magnitude will be very dependent on device processing.

A randomness is associated with the generation current. Scott and Strutt [26] show that, since electron and hole emission are independent, the generation current exhibits two-thirds full shot noise:

$$\overline{i_g^2} = \frac{2}{3}(2qI_G\ df) \tag{2.3}$$

c. 1/f Noise

Low-frequency excess noise was found by Gianola [27] to be an important contaminating effect in diffused silicon photodiodes. Its mean square magnitude was directly proportional to junction current. The 1/f law clearly must break down at dc, but, though measurements have been made to frequencies as low

as 6×10^{-5} Hz [28], the low-frequency breakpoint is still not well defined. For purposes of comparison, we assume the following somewhat a priori excess noise formula:

$$\overline{i_e^2} = 2q(I_P + I_G) \frac{f_k}{\left(f^2 + f_o^2\right)^{\frac{1}{2}}} df \qquad (2.4)$$

In the above, f_o is the low-frequency breakpoint, and f_k defines the "knee" frequency where shot and excess noise components are equal. A typical value for f_k is 200 Hz [29], which is many orders of magnitude larger than f_o.

B. Storage Mode Low-Level Features

1. Transfer Function

The efficacy of the charge-storage technique in increasing the average signal current from scanned imaging devices is well described in the literature [4]. As mentioned at the beginning of the chapter, the current gain is found to be approximately equal to the number of scanned elements. For the reading aid application, a periodic decision is desired as to whether each individual element is lighted or dark. A periodically excited voltage comparator is used to accomplish this. Peak output voltage, rather than average current, is therefore the output variable of chief interest throughout this discussion.

Figure 2a depicts the charge-storage circuit. The photodiode is reverse biased and periodically sampled. The switch is closed during

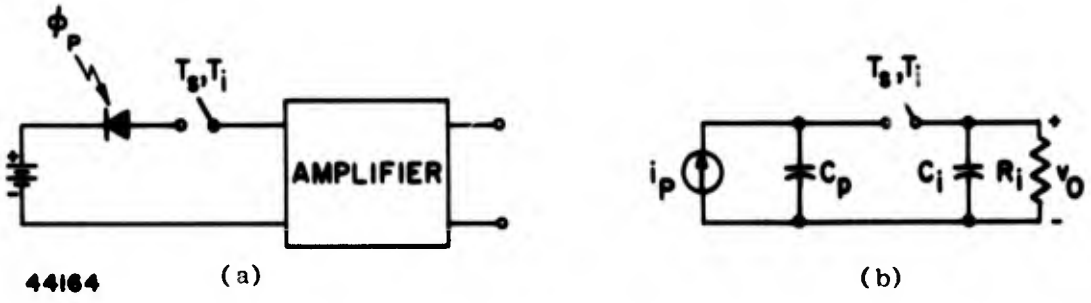


Fig. 2. CHARGE STORAGE PHOTODIODE AND CIRCUIT MODEL.

the sampling time T_s and its signal applied to the input of an amplifier (or voltage comparator). The switch is opened for a much longer period T_i, the integration time. Figure 2a may only represent one of a large number of diodes that are sequentially sampled to create a continuous signal. In the circuit model of Fig 2b, the reverse-biased photodiode is replaced by its circuit model, which consists of a current source in parallel with the depletion-layer capacitance (dark current neglected). The battery is removed since it just charges C_p to a steady value, and the amplifier is modeled by its input resistance and capacitance, R_i and C_i. The large-signal features of this configuration, accounting for the voltage dependence of C_p, have been analyzed by Weckler [10]. The concern here is small-signal, low-level properties so C_p is assumed constant.

A transfer function is desired between input current and peak output voltage, which is designated by v_K. The input is continuous but the output discrete, so sampled-data techniques are necessary. Two assumptions, $T_i/T_s \gg 1$ and $R_iC_i \ll T_i$, are well satisfied in practice. The first assumption is almost a requirement for useful charge-storage operation, and enables one to neglect the effects of the current source i_p during T_s. During the $(n-1)^{th}$ sample period, the output voltage v_O decays to a fraction f of its peak value at the beginning of the sample period. This fractional decay f equals $\exp(-T_s/\tau)$, where $\tau = R_i(C_i + C_p)$. The sampling switch then opens and v_O decays to zero, while the voltage across C_p increases by an amount

$$\Delta v_p = \frac{1}{C_p} \int_0^{T_i} i_p \, dt$$

Just after the switch again closes, the charge on C_p is shared with C_i to give the next peak output voltage $v_K[nT_i]$. The difference equation describing this cycle is:

$$v_K[nT_i] = \frac{C_p}{C_i + C_p} \left(\Delta v_p + f \; v_K[(n-1)\; T_i] \right)$$

or

$$v_K[nT_i] = \frac{1}{C_i + C_p} \int_0^{T_i} i_p \, dt + f \frac{C_p}{C_i + C_p} v_K[(n-1)\ T_i] \qquad (2.5)$$

The above equation describes the dynamics of the charge-storage mode. It is represented in transfer function form by Fig. 3. The integration of the photocurrent is accomplished by the finite-time integrator (FTI) [30]. The FTI has a rectangular impulse response that, when convolved with the input, gives an instantaneous output Δv_p proportional to the area under the input waveform over the preceding T_i seconds. Its frequency response is the sinc function shown (sinc x = sin x/x). The feedback term is simply a delay of T_i seconds and a "memory" factor $fC_p/(C_i + C_p)$. Its output is added to samples of the FTI output to form the desired $v_K[nT_i]$ sequence, per Eq. (2.5). This block diagram is used in the following sections to characterize the low-level signal processing features of the circuit.

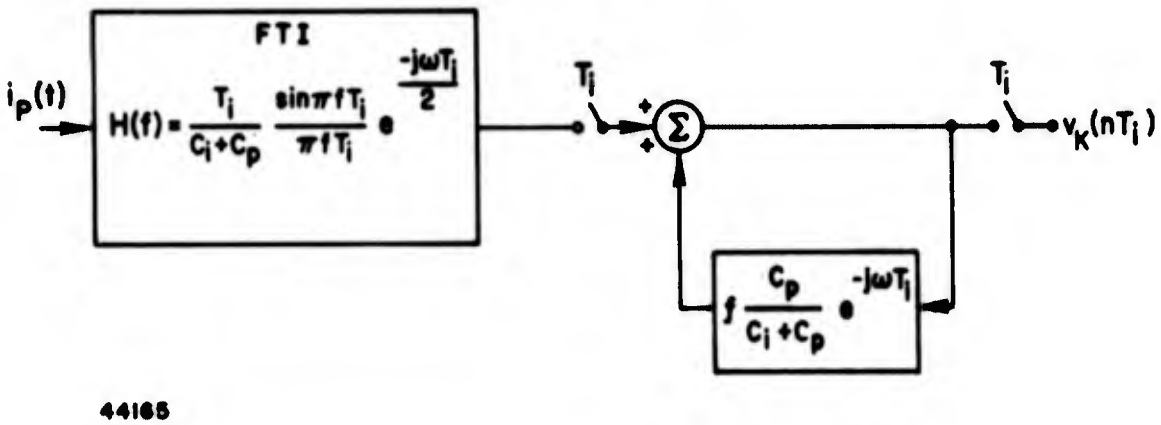


Fig. 3. BLOCK DIAGRAM OF CHARGE STORAGE MODEL.

2. Gain and Bandwidth

The useful gain term, for the purposes at hand, is the steady-state ratio of peak output voltage to input dc photocurrent. With reference to Fig. 3, the FTI dc gain is simply $T_i/(C_i + C_p)$. The steady-

state gain of the sampled portion is calculated by the final-value theorem [31] to be $[1 - fC_p/(C_i + C_p)]^{-1}$. The product of these two factors gives

$$G \triangleq \frac{V_K}{I_p} = \frac{T_i}{C_i + C_p(1 - f)} \tag{2.6}$$

Three limiting cases may be distinguished:

(1) When $T_s \gg \tau$, then $f \to 0$, and

$$G = R\,\frac{T_i}{\tau} \qquad \frac{T_s}{\tau} \gg 1 \tag{2.7}$$

(2) When $T_s \ll \tau$, and C_i is negligible, then

$$G = R\,\frac{T_i}{T_s} \qquad \frac{C_i}{C_p} \ll \frac{T_s}{\tau} \ll 1 \tag{2.8}$$

(3) When the amplifier capacitance dominates the response,

$$G = \frac{T_i}{C_i} \qquad \frac{C_i}{C_p} \gg 1 - \exp(-T_s/\tau) \tag{2.9}$$

The concept of bandwidth is a bit vague due to the continuous input-sampled output nature in Fig. 3. In the following section, an "equivalent noise bandwidth" is calculated that describes how white noise passes through the filter. An alternative "3 dB" bandwidth may also be computed. When the "memory factor" f is significant relative to unity, the sampled portion of the block diagram dominates the transient response. Its natural mode is a geometric sequence, as shown by the scope photograph, Fig. 4. Each peak output is a fixed fraction, $fC_p/(C_i + C_p)$ of the previous peak output. The envelope of the pulses is exponential, with a readily calculated time constant $T_i/\ell n[(C_i + C_p)/fC_p]$. We may then define a "3 dB" bandwidth

$$f_d = \frac{\ell n \left(\frac{C_i + C_p}{f C_p} \right)}{2\pi T_i} \tag{2.10}$$

and gain-bandwidth product

$$G \times f_d = \frac{1}{2\pi C_p} \frac{\ell n \frac{1}{f} + \ell n \left(1 + \frac{C_i}{C_p} \right)}{1 - f + \frac{C_i}{C_p}}$$

Substituting $f = \exp(-T_s/\tau)$,

$$G \times f_d = \frac{1}{2\pi C_p} \frac{\frac{T_s}{\tau} + \ell n \left(1 + \frac{C_i}{C_p} \right)}{1 - \exp(T_s/\tau) + \frac{C_i}{C_p}}$$

If $T_s \ll \tau$ and $C_i \ll C_p$,

$$G \times f_d = \frac{1}{2\pi C_p} \tag{2.11}$$

Thus, when C_i is small and the sample time short relative to the $R_i(C_i + C_p)$ time constant, the gain-bandwidth product is invariant. This is exactly analogous to the continuous case of a capacitor shunted current source. Gain and bandwidth are exchanged by varying the ratio of integration time to sample time [Eq. (2.8)]. This technique is presently being used for automatic gain control in a photosensing array [32].

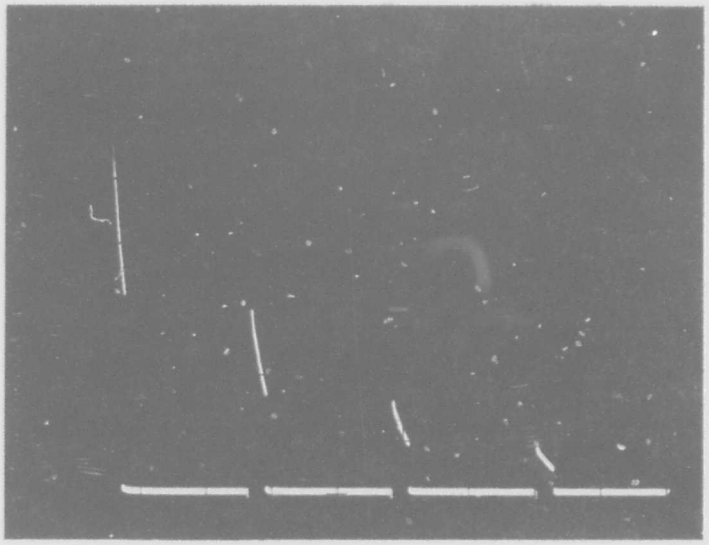


Fig. 4. GEOMETRIC DECAY OF OUTPUT.

3. Equivalent Noise Bandwidth

In order to determine the output signal-to-noise ratio, the noise transmission properties of the charge-storage filter must be analyzed. Consider that white shot noise, having spectral density $2qI_P$, is applied to the input and that (for simplicity) C_i may be neglected. The mean square output of the FTI will be [33]

$$\overline{\Delta v_p^2} = 2qI_P \int_0^\infty |H(f)|^2 \, df \qquad (2.12)$$

Evaluation of the above, using the FTI frequency response, gives the result:

$$\overline{\Delta v_p^2} = \frac{qI_P T_i}{C_p^2} \qquad (2.13)$$

It is interesting to note that the rms charge deviation $C_p\left(\overline{\Delta v_p^2}\right)^{1/2}$ is simply the geometric mean of the electronic charge and the photogenerated charge over the integration time.

The transmission of noise through the sampled-data portion of Fig. 3 is particularly simple when the input samples are "white," i.e., uncorrelated with each other. In this case, the mean square output equals the mean square input times the sum of the squares of the impulse response [31]. (This is analogous to the continuous situation.) The impulse response is a decaying geometric sequence (Fig. 4). The sum of the squares of this sequence is $1 + f^2 + f^4 + \ldots = 1/(1 - f^2)$, so

$$\overline{v_k^2} = \frac{1}{1 - f^2}\,\overline{\Delta v_p^2} = \frac{1}{1 - f^2}\,\frac{q^2 p T_i}{C_p^2} \tag{2.14}$$

The ratio of output peak signal to rms noise, for an input current exhibiting shot noise, may now be written with the aid of Eqs. (2.6) and (2.14):

$$\mathrm{SNR} = \frac{V_K}{\sqrt{\overline{v_k^2}}} = \left(\frac{I_p T_i}{q}\,\frac{1 + f}{1 - f}\right)^{1/2} \tag{2.15}$$

If a shot noise current source is applied to an ideal lowpass filter with cutoff frequency f_n, the output SNR is readily calculated to be:

$$\mathrm{SNR} = \left(\frac{I_p}{2qf_n}\right)^{1/2} \tag{2.16}$$

Comparing Eqs. (2.15) and (2.16), the charge-storage circuit gives the same output SNR as an ideal lowpass filter with bandwidth

$$f_n = \frac{1}{2T_i}\,\frac{1 - f}{1 + f} \tag{2.17}$$

Equation (2.17) defines the equivalent noise bandwidth of the charge-storage filter. This bandwidth is reduced, while gain and SNR are increased, if the integration time T_i is lengthened and/or the memory factor f made larger. As f approaches unity, the sampled portion of the transfer function dominates the response, and the equivalent noise bandwidth is $\pi/2$ times the 3 dB bandwidth defined in the preceding section. This is exactly analogous to the case of a continuous single-pole filter [34]. If the memory factor f is negligible, the FTI noise bandwidth, $1/2T_i$, predominates.

In preparation for the next section, the mean square output noise due to the excess noise input will now be computed using the equivalent noise bandwidth approximation. This approximation is quite good, since the power density in the $1/f$ spectrum is concentrated at low frequencies. Assuming an ideal lowpass filter with gain G and bandwidth f_n, and using Eqs. (2.4) and (2.12):

$$\overline{v_k^2} = 2q(I_P + I_G)\, f_k G^2 \int_0^{f_n} \frac{df}{\left(f^2 + f_o^2\right)^{1/2}}$$

which gives the $1/f$ component, assuming $f_n \gg f_o$,

$$\overline{v_k^2} = 2q(I_P + I_G)\, f_k G^2 \ln\left(\frac{2f_n}{f_o}\right) \qquad (2.18)$$

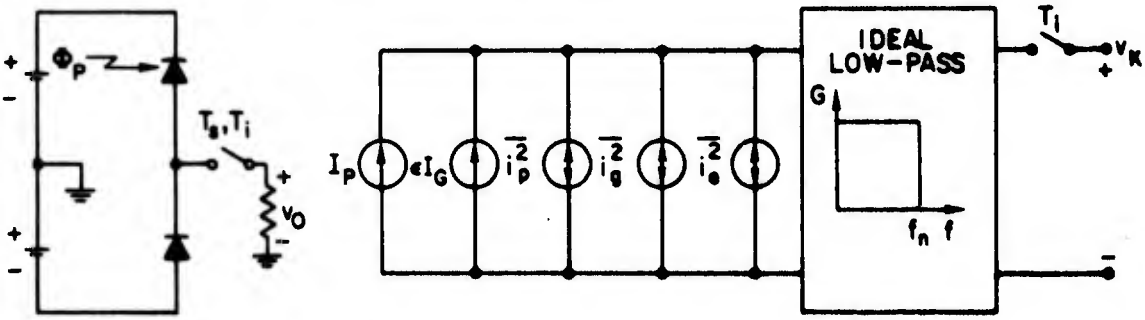
4. Comparison of Noise Sources

The relative importance of the various noise sources described in Section A may now be evaluated. We assume the circuit of Fig. 5a, in which first-order compensation of the dc generation current is accomplished by an additional diode electrically matched to the photodiode but shielded from light [35]. The model of Fig. 5b is used, with dc signal photocurrent I_P and a number of contaminating noise generators. The generation current is assumed to be reduced by a fraction ϵ due to the compensating photodiode. The noise sources associated with the diode generation currents

are assumed uncorrelated, so their mean square values are doubled. Using the previously derived results for transmission by an ideal lowpass filter, the output signal-to-noise ratio is

$$SNR = \frac{I_p}{\epsilon I_G + \left[2qI_p f_n\left(1 + \frac{f_k}{f_n}\ln\frac{2f_n}{f_o}\right) + 4qI_G f_n\left(\frac{2}{3} + \frac{f_k}{f_n}\ln\frac{2f_n}{f_o}\right)\right]^{1/2}} \quad (2.19)$$

The first term of the denominator of Eq. (2.19) represents dc uncertainty due to imperfect compensation by the extra diode. The second term is the rms uncertainty from shot and excess noise due to current flow. The terms in parentheses are a measure of the relative importance of excess and shot noise. Using representative numbers f_n = 30 Hz, f_k = 200 Hz,



(a) (b)

I_p = dc photogenerated current, $q\eta\Phi_p A_p$

ϵI_G = uncompensated generation current, $\epsilon J A_p$

$\overline{i_p^2}$ = mean square photocurrent shot noise per unit bandwidth, $2qI_p$

$\overline{i_g^2}$ = mean square generation current noise per unit bandwidth, $\frac{4}{3}(2qI_G)$

$\overline{i_e^2}$ = mean square excess noise per unit bandwidth,

$$2q(I_p + 2I_G)\frac{f_k}{\left(f^2 + f_c^2\right)^{1/2}}$$

Fig. 5. COMPENSATED CHARGE STORAGE PHOTODIODE AND NOISE MODEL.

and $f_o = 10^{-5}$ Hz, one finds the 1/f noise component to be about two orders of magnitude the larger. This result is not unexpected, since the lowpass filter nicely matches the 1/f spectrum. Assuming a diode area $A_p = 10^{-3}$ cm^2 and $\Gamma = 10^{-9}$ A/cm^2 [Eq. (2.2)], the two denominator terms are plotted vs I_p in Fig. 6. The dashed lines are the dc generation current uncertainty for several values of ϵ. The dotted line represents the rms 1/f noise. It is constant at low values of I_p, due to the fixed generation current contribution. When the sum of the dotted and appropriate dashed curves equals the solid line, representing I_p, then SNR = 1. It is clear that this point will occur at a value of I_p where the generation term dominates the right side of the denominator of Eq. (2.19). Hence the conclusion that the most significant noise sources are imperfect compensation of the dc generation current and excess noise in the generation current. Unless the dc compensation is very good ($\epsilon = 0.04$ in Fig. 6), its uncertainty will be the major contaminating source.

In view of the above, Eq. (2.19) may be simplified at low levels to:

$$\text{SNR} \cong \frac{I_P}{\epsilon I_G + \left(4qI_G f_k \ell n \frac{2f_n}{f_o}\right)^{1/2}} \qquad (2.20)$$

If we assume $\epsilon = 0.04$, then SNR = 1 at $I_p = 10^{-13}$ A. This photocurrent corresponds to an incident flux density $\Phi_p = I_p/qA_p\eta$ equaling 10^9 photons/sec cm^2 ($\eta = 0.6$). At $\lambda = 0.55\ \mu$ the incident power density is equal to $10^9\ hc/\lambda = 3.6 \times 10^{-10}$ watt/cm^2. This can be put in photometric terms, using the fact that 1 watt = 685 lumens at 0.55 μ [36], to give SNR = 1 at an incident illuminance of 2.3×10^{-4} ft-candle.

If the integration time is lengthened, f_n is reduced, and thereby the excess noise term in Eq. (2.20) is decreased. As photodiode area is reduced, the excess noise term becomes relatively more important, since it varies as $\sqrt{A_p}$ and the other terms vary directly with A_p.

This effect is probably neutralized in practice by an effective increase in ϵ due to greater tolerance difficulties in small geometries, and to an increase in Γ due to diode perimeter leakage currents.

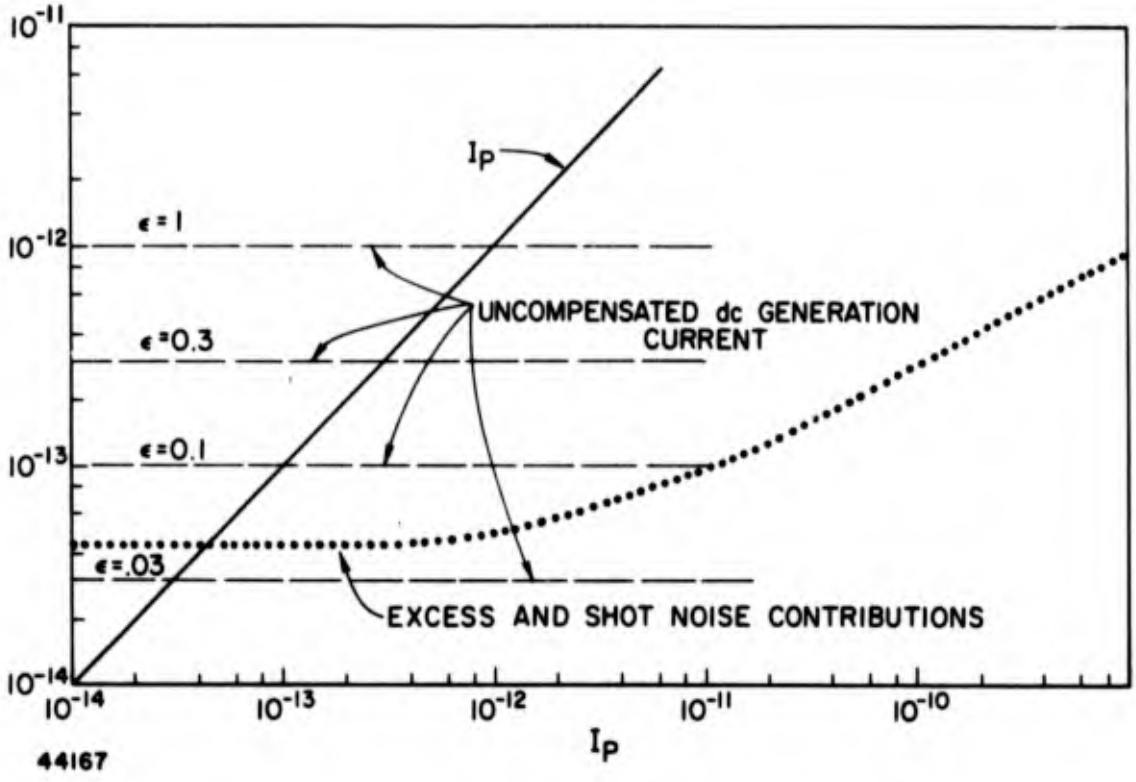


Fig. 6. OUTPUT SIGNAL AND NOISE, $A_p = 10^{-3}$ cm^2.

C. Summary

The basic low-level properties of the photodiode charge-storage circuit were described. A block diagram representing the circuit transfer function was derived, and the circuit was shown to be basically a lowpass filter. Because of its lowpass nature, dc uncertainties and 1/f noise are the major contaminating signals. For this reason, the high gain of the charge-storage mode is not obtained without a sacrifice in noise performance.

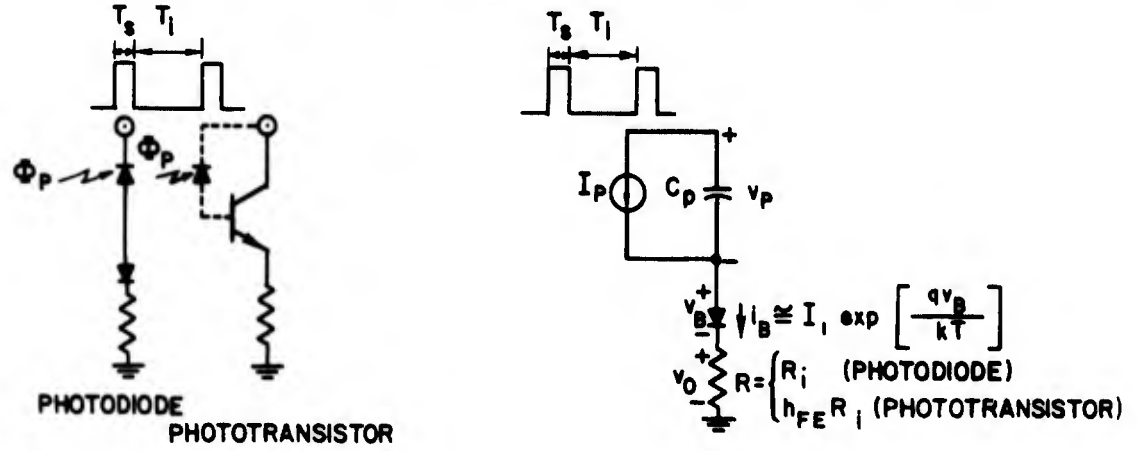
Chapter III

THE CHARGE-STORAGE PHOTODIODE AT LOW LEVLLS--DIODE SWITCH CASE

In many practical array applications, readout of the charge stored on a photodiode exposed to radiation is accomplished by alternatively forward and reverse biasing a junction diode. This situation, which includes the common charge-storage phototransistor [3,11,38], is analyzed in this chapter. It is shown that, because of the nonideal characteristic of the junction diode switch, circuit properties are very nonlinear. As a result, the static and dynamic properties of the charge-storage filter become very dependent on the level of the incident flux.

A. The Circuit and Its Model

Both the photodiode and phototransistor versions of the circuit to be considered are depicted in Fig. 7a. The operation of the photodiode-switching diode combination is quite simple. During the sampling period, the depletion-layer capacitance of the photodiode is charged approximately to the amplitude of the sampling pulse. When the sampling pulse returns to zero, the switching diode is reverse biased and the capacitance is discharged by photogenerated current and thermally generated



a. The circuit

b. Circuit model

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Fig. 7. CHARGE-STORAGE CIRCUITS AND MODEL USING DIODE SWITCH.

dark current. The charge thus removed during the integration time is replaced at the next sampling time to complete the classical charge-storage cycle. The photodiode remains reverse biased at all times, commutation being performed by the switching diode as it ranges from conduction to cutoff. In the phototransistor case, the basic operation is the same. The switching function is provided by the emitter-base diode, and the collector-base junction functions as the photodiode. Transistor action and photogeneration may be conceptually separated in order to clarify circuit operation. This is done in the figure by representing the phototransistor by the parallel combination of a photodiode and an ordinary transistor.

The circuits of Fig. 7a are both represented by the first-order model shown in Fig. 7b. This model is the same as that in Fig. 2b, except for the addition of the series junction diode and the assumption of negligible amplifier capacitance C_i. The only distinction between the model for the photodiode and phototransistor circuits is in the circuit resistance value chosen. The transistor current gain is accounted for in the latter case by increasing this resistance value by the factor h_{FE}. As was done in Chapter II, the photodiode junction capacity is assumed constant. The switching diode is assumed to have an exponential I-V characteristic. Sources of stored charge, such as switching diode capacitance and the transistor base region, and photodiode dark current are neglected. These two assumptions will be looked into in more detail later on in the chapter. Another important supposition for the phototransistor is that the dc current gain, h_{FE}, is independent of current level. While this does not hold at very low currents, it greatly simplifies the analysis without seriously invalidating the results. In fact, one of the salient features of phototransistor charge-storage operation is that it enables operation at large enough collector currents to get high h_{FE}. In spite of the simplicity of the model of Fig. 7b, good agreement of analytical and experimental results was obtained.

B. Mathematical Analysis of the Model

1. Differential Equation

A relationship is desired between peak output voltage and dc photocurrent. To this end, the differential equation governing circuit behavior during T_s must be derived and solved, subject to appropriate boundary conditions. The necessary mathematics is done in this section. This mathematical manipulation is followed by an interpretive discussion in the following section.

With reference to Fig. 7b, during the sampling period one may write

$$C_p \frac{dv_P}{dt} + I_P = i_B$$

and

$$v_P + v_B + Ri_B = 0$$

which combine to give

$$C_p \frac{dv_B}{dt} + \tau \frac{di_B}{dt} + i_B - I_P = 0$$

where $\tau \triangleq RC_p$. Using

$$i_B = I_1 \exp\left(\frac{qv_B}{kT}\right)$$

$$di_B = \frac{qi_B}{kT} dv_B$$

$$\frac{dv_B}{dt} = \frac{kT}{qi_B} \frac{di_B}{dt} \qquad (3.1)$$

gives the differential equation

$$\left(\frac{kTC_P}{qi_B} + \tau\right)\frac{di_B}{dt} + i_B - I_P = 0 \qquad (3.2)$$

The differential equation is easily separated

$$-\frac{dt}{\tau} = \left(\frac{kT}{qRi_B}\right)\frac{di_B}{i_B - I_P} + \frac{di_B}{i_B - I_P} \qquad (3.3)$$

At this point, the key simplifying assumption will be made that $i_B \gg I_P$ during the sampling period. This assumption was also taken in Chapter II, and holds well in practice as long as the ratio of integration time to sampling time is high. Equation (3.3) may then be written

$$-\frac{dt}{\tau} = \frac{kT}{qR}\frac{di_B}{i_B^2} + \frac{di_B}{i_B} \qquad (3.4)$$

Equation (3.4) may be put in an alternative form

$$\frac{1}{i_B}\frac{di_B}{dt} = -\frac{1}{\tau}\left(\frac{1}{1 + kT/qRi_B}\right)$$

or (3.5)

$$\frac{1}{v_O}\frac{dv_O}{dt} = -\frac{1}{\tau}\left(\frac{1}{1 + kT/qv_O}\right)$$

Equation (3.5) indicates that, as long as the output voltage v_O is much greater than kT/q (26 mV at room temperature), the logarithmic derivative of the output voltage decay is constant [37]. This implies that the output voltage decays exponentially with time constant τ, and is the situation analyzed in Chapter II, when the switching diode conductance is

high enough to be disregarded. On the other hand, if $v_o < kT/q$, the logarithmic derivative decreases, and the output voltage decays at a much-slower-than-exponential rate. The physical reason for this is that the switching diode small-signal conductance, qi_B/kT [Eq. (3.1)], varies directly with current level. At low currents, this conductance therefore dominates the transient response, causing very sluggish low-level transient response. The "crossover," when the switching diode conductance becomes significant, is seen by Eq. (3.5) to be simply when

$$\frac{qi_B}{kT} = \frac{1}{R} \tag{3.6}$$

Crossover occurs at the value of i_B when switching diode small-signal conductance equals the circuit conductance $1/R$. At lower values of current the junction diode is significantly nonideal as a switch in this application as a result of its exponential I-V characteristic.

The differential equation (3.4) is readily integrated to give

$$-\frac{t}{\tau} = -\frac{kT}{qR}\frac{1}{i_B} + \ell n\ i_B + \Omega \tag{3.7}$$

where Ω is the constant of integration. Equation (3.7) cannot be solved explicitly for i_B as a function of time, so evaluation of Ω is not easy. A somewhat indirect approach will be taken. First Eq. (3.7) will be used to find a relationship between peak output voltage and fractional memory of output voltage during the sample time. Then the boundary condition will be evaluated to determine a relationship between these variables and the input photocurrent. The resulting two equations are then simultaneously solved.

Using $Ri_B(0) = RI_K$, where I_K is the peak output current, and $Ri_B(T_s) = fRI_K$, where f is the fractional memory of output per cycle, Eq. (3.7) becomes

$$0 = -\frac{kT}{qRI_K} + \ell n\ I_K + \Omega \qquad \text{at} \quad t = 0 \tag{3.8}$$

and

$$-\frac{T_s}{\tau} = -\frac{kT}{qfRI_K} + \ell n\ fI_K + \Omega \qquad \text{at} \quad t = T_s \tag{3.9}$$

Subtracting Eq. (3.9) from Eq. (3.8) gives

$$\frac{kT}{qRI_K}\left(\frac{1-f}{f}\right) = \frac{T_s}{\tau} + \ell n\ f$$

Using normalized variables $\frac{RI_K}{kT/q} \triangleq \hat{V}$ and $\frac{T_s}{\tau} \triangleq r$, this becomes

$$\underline{\hat{V}(r + \ell n\ f) = \frac{1-f}{f}} \tag{3.10}$$

which is the desired equation relating peak output voltage and fractional decay.

2. Boundary Condition Evaluation

The boundary condition is that of conservation of charge, i.e., in steady state the charge stored during the integration time is all removed during the sample time. This may be written

$$\int_0^{T_s} i_B\ dt = I_P T_i \tag{3.11}$$

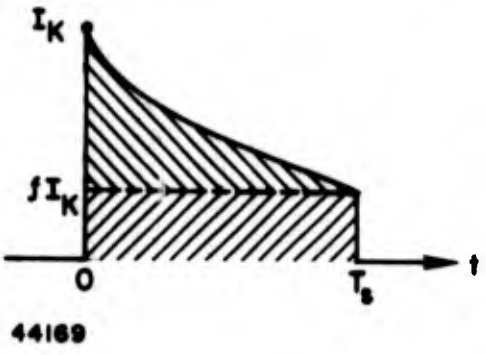


Fig. 8. CURRENT PULSE DURING SAMPLE TIME.

The integral on the left side of Eq. (3.11) is represented by the total area under the $i_B(t)$ waveform shown in Fig. 8. Since Eq. (3.7) can only be solved for t as a function of i_B, we express this area as the sum of the two hatched areas in the following way:

$$\int_{fI_K}^{I_K} t\ di_B + fI_K T_s = I_P T_i \tag{3.12}$$

Substituting Eq. (3.7) gives

$$\frac{kTC_p}{q}\int_{fI_K}^{I_K}\frac{di_B}{i_B} - \tau\int_{fI_K}^{I_K}\ell n\ i_B\, di_B - \Omega\tau\int_{fI_K}^{I_K} di_B + fI_K T_s = I_p T_i$$

and integrating,

$$-\frac{kTC_p}{q}\ell n\ f - \tau[I_K\ \ell n\ I_K - fI_K\ \ell n\ (fI_K)] + \tau(1-\Omega)\ I_K(1-f) + fI_K T_s = I_p T_i \tag{3.13}$$

Multiplying Eq. (3.8) by τI_K and Eq. (3.9) by $\tau f I_K$ and subtracting gives

$$-\tau[I_K\ \ell n\ I_K - I_K\ \ell n\ (fI_K)] - \tau\Omega I_K(1-f) + fI_K T_s = 0 \tag{3.14}$$

Equation (3.14) simplifies Eq. (3.13) to

$$-\frac{kTC_p}{q}\ell n\ f + \tau I_K(1-f) = I_p T_i$$

or

$$\frac{RI_K}{kT/q}(1-f) - \ell n\ f = \frac{I_p T_i/C_p}{kT/q}$$

Using

$$\hat{V} \triangleq \frac{RI_K}{kT/q} \quad \text{and} \quad \Delta\hat{V} \triangleq \frac{\Delta V_p}{kT/q} = \frac{I_p T_i/C_p}{kT/q}$$

the above equation becomes

$$\underline{\hat{V}(1-f) - \ell n\ f = \Delta\hat{V}} \tag{3.15}$$

Equation (3.15), together with Eq. (3.10), furnishes the basis for the low-level analysis in the succeeding section. An alternative derivation of Eq. (3.15) is possible [3].

3. Sensitivity of Peak Voltage to Transistor Current Gain

Another parameter of important practical interest when a phototransistor is used is the sensitivity of the peak output voltage to variations in transistor dc current gain h_{FE}. The sensitivity parameter is defined as

$$S_{h_{FE}}^{\hat{V}} = \frac{d\hat{V}}{dh_{FE}} \frac{h_{FE}}{\hat{V}}$$

and may be derived from Eqs. (3.10) and (3.15). Using Eq. (3.15), with $\triangle\hat{V}$ fixed,

$$d\hat{V} - \hat{V}d f - f\, d\hat{V} - \frac{df}{f} = 0$$

which gives

$$\frac{df}{1 - f} = \frac{d\hat{V}}{\hat{V} + 1/f} \tag{3.16}$$

Taking the logarithm of Eq. (3.10),

$$\ell n\, \hat{V} = \ell n\, (1 - f) - \ell n\, f - \ell n\, (r + \ell n\, f)$$

and differentiating:

$$\frac{d\hat{V}}{\hat{V}} = - \frac{df}{1 - f} - \frac{df}{f} - \frac{dr + df/f}{r + \ell n\, f}$$

Using Eq. (3.10) to replace $r + \ell n\, f$ gives

$$\frac{d\hat{V}}{\hat{V}} = - \frac{df}{1 - f} - \frac{df}{f} - \frac{f\hat{V}\, dr}{1 - f} - \frac{\hat{V}\, df}{1 - f} \tag{3.17}$$

Also

$$r = \frac{T_s}{h_{FE} R_i C_p}$$

$$dr = r \frac{dh_{FE}}{h_{FE}} \tag{3.18}$$

Substituting Eqs. (3.16) and (3.18) in Eq. (3.17):

$$\frac{d\hat{V}}{\hat{V}} = \frac{- d\hat{V}}{\hat{V} + 1/f} + \frac{(1 - 1/f)d\hat{V}}{\hat{V} + 1/f} + \frac{dh_{FE}}{h_{FE}} \left(\frac{rf\hat{V}}{1 - f} \right) - \frac{\hat{V}\, d\hat{V}}{\hat{V} + 1/f}$$

$$\frac{d\hat{V}}{\hat{V}} = - d\hat{V} + \frac{dh_{FE}}{h_{FE}} \frac{rf\hat{V}}{1 - f}$$

$$\frac{d\hat{V}}{\hat{V}} (1 + \hat{V}) = \frac{dh_{FE}}{h_{FE}} \frac{rf\hat{V}}{1 - f}$$

$$S^{\hat{V}}_{h_{FE}} = \frac{d\hat{V}}{dh_{FE}} \frac{h_{FE}}{\hat{V}} = \frac{rf}{1 - f} \frac{\hat{V}}{1 + \hat{V}} \tag{3.19}$$

C. Input-Output Properties of the Low-Level Model

The mathematical results achieved above are graphically displayed and interpreted in this section. The important equations are summarized below:

$$\hat{V}(r + \ell n\, f) = \frac{1 - f}{f} \tag{3.10}$$

$$\hat{V}\,(1 - f) - \ell n\, f = \Delta\hat{V} \tag{3.15}$$

$$S^{\hat{V}}_{h_{FE}} = \frac{r\,f}{1 - f} \frac{\hat{V}}{1 + \hat{V}} \tag{3.19}$$

The variables are:

$$\hat{V} = \frac{V_K}{kT/q} = \text{normalized peak output voltage}$$

$$\Delta\hat{V} = \frac{\Delta V_p}{kT/q} = \frac{I_p T_i / C_p}{kT/q} = \text{normalized capacitor voltage change during integration time}$$

f = memory factor; the ratio of output voltage at end of sample period to that at beginning of sample period

$r = T_s/\tau$ = the number of circuit RC time constants in the sample time

The equations are transcendental, and somewhat awkward to manipulate, so that the solutions are best exhibited graphically. These graphical displays constitute the most important results of this chapter.

1. Transfer Characteristic

Figure 9 plots curves of output $\hat{V}$ vs input $\Delta\hat{V}$ for several values of r. Experimental points, in good agreement with the theory, are also shown. The larger values of r are seen to result in a more pronounced "thresholding" effect and lower dc gain. Thus the longer the sample time is relative to the circuit time constant, the more nonlinear the transfer characteristic will be.

2. Memory Factor

Equation (3.15) in the following form

$$\hat{V} = \frac{1}{1 - f}\left(\Delta\hat{V} - \ell n \frac{1}{f}\right)$$

represents lines of constant f in the input-output plane, as shown in Fig. 10. Two results are immediately apparent: (1) the higher the gain, i.e., the bigger $\hat{V}$ for a given $\Delta\hat{V}$, the better the memory (bigger f). This means that higher gain automatically implies more-sluggish transient

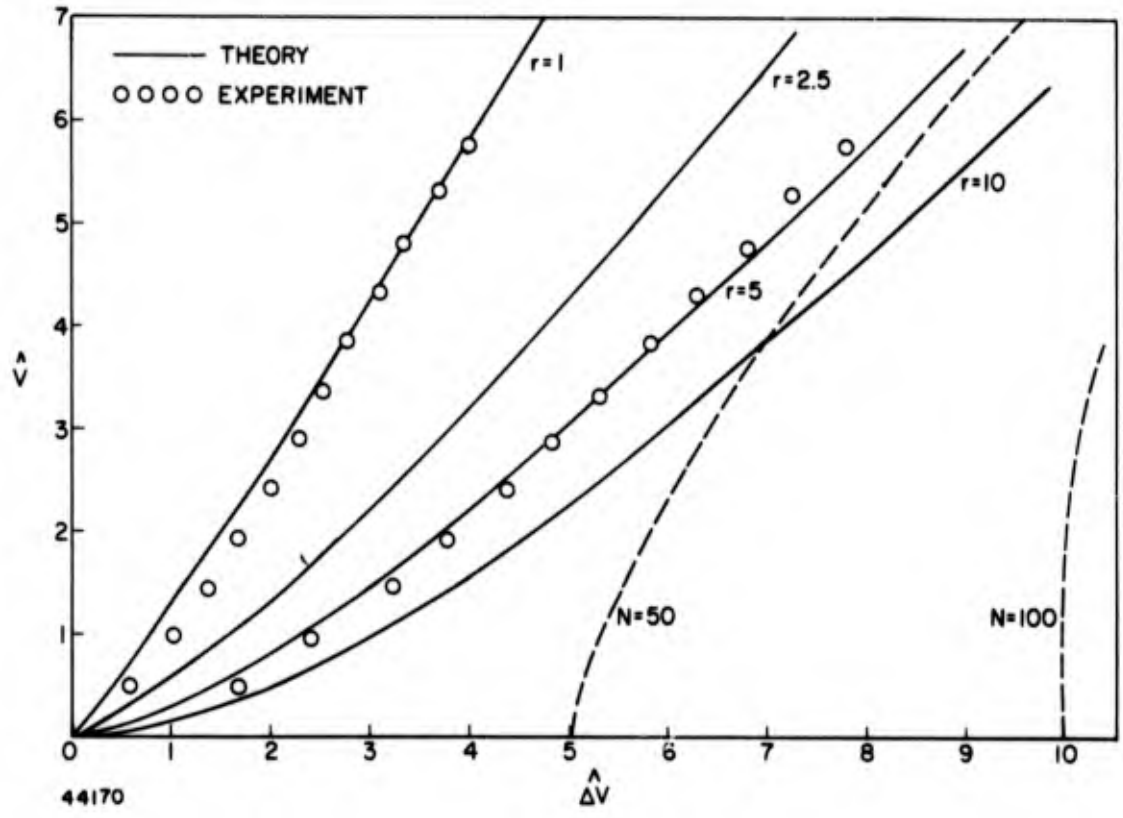


Fig. 9. INPUT-OUTPUT CHARACTERISTIC.

response. This is an extension of the gain-bandwidth trade mentioned in Chapter II. (2) As the input $\Delta\hat{V}$ decreases, the memory must increase, no matter what the gain. The minimum memory for a given $\Delta\hat{V}$ occurs for the limiting case of zero gain (along the abscissa), and is given by the formula

$$f_{min} = e^{-\Delta\hat{V}} \tag{3.20}$$

In imaging systems, it is generally desirable to keep the memory small to avoid smearing of moving images. Similar considerations apply to the reading aid in order to preserve reading rate. Equation (3.20) shows, however, that image smear cannot be avoided at low light levels when a diode switch is used.

By superposing the transfer characteristic (Fig. 9) on Fig. 10, curves of f vs $\Delta\hat{V}$ for various values of r may be plotted. This is

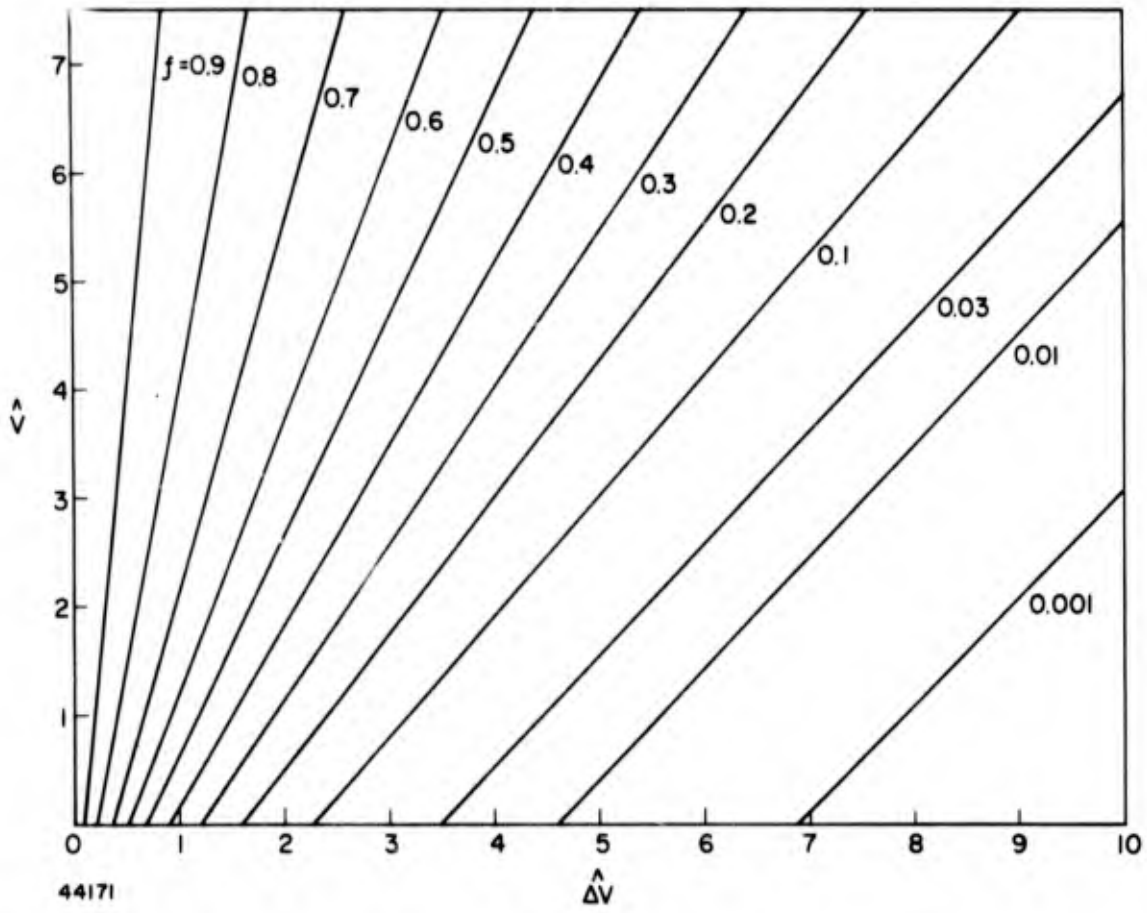


Fig. 10. LINES OF CONSTANT f IN INPUT-OUTPUT PLANE.

done in Fig. 11. The bound, Eq. (3.20), is also shown, as well as a few verifying experimental points. All curves are seen to monotonically approach $f = 1$ as $\Delta\hat{V}$ approaches zero. The physical reason for this is that, as previously stated, the switching diode "on" conductance becomes very small at low current levels.

3. Current Gain Sensitivity of Peak Output Voltage

Curves of constant $S^{\hat{V}}_{h_{FE}}$ can be plotted in the $\hat{V}$ - $\Delta\hat{V}$ plane by use of the formulas, and are shown in Fig. 12. These curves illustrate that increased sensitivity results from operation near either axis. In particular, a minimum sensitivity is possible at any input level. By superposition of the transfer characteristics for various values of r on the curves of Fig. 12, sensitivity may be plotted vs input level, as in Fig. 13. Sensitivity, like memory, is seen to increase monotonically

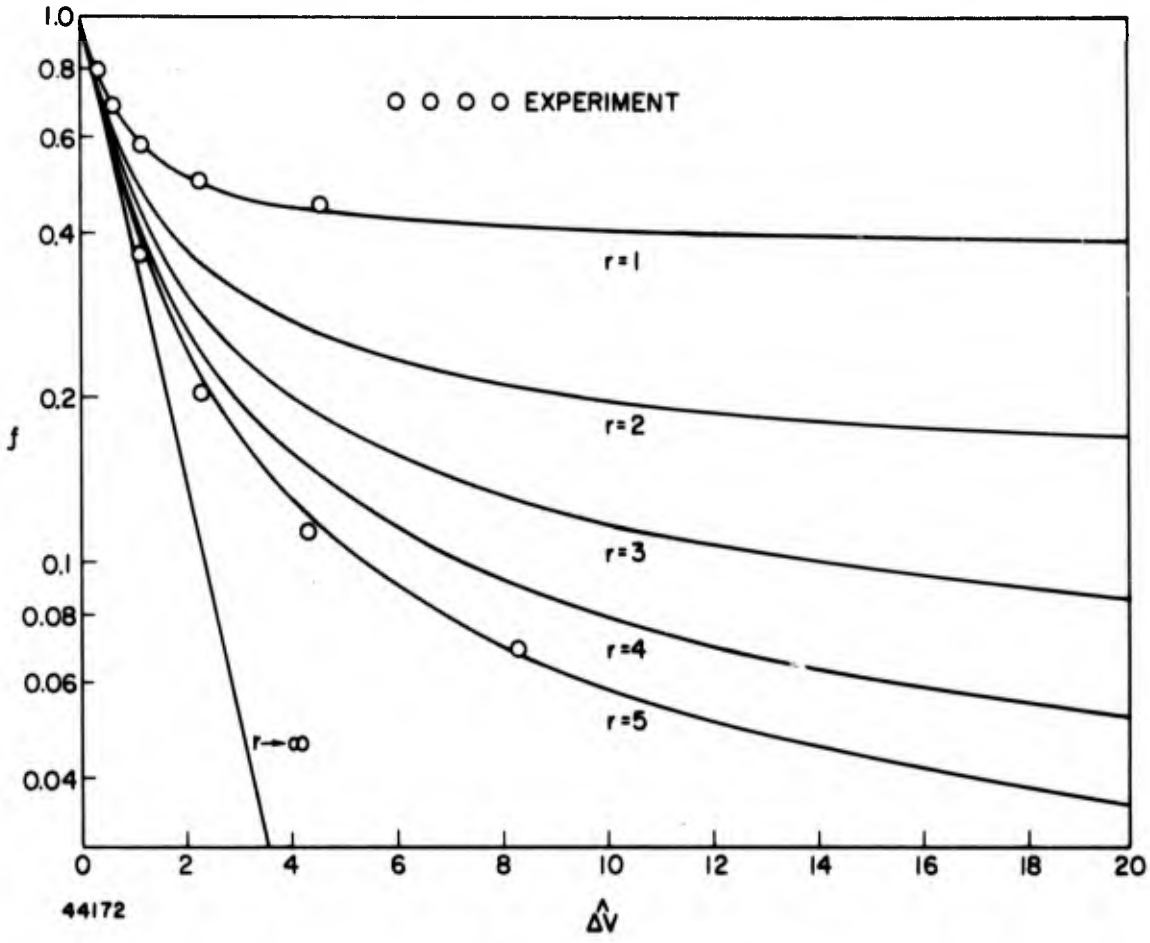


Fig. 11. f vs $\Delta\hat{V}$ FOR VARIOUS VALUES OF r.

with decreasing $\Delta\hat{V}$. An interesting "crossover" effect occurs, so that curves with greater sensitivity at high input levels have smaller sensitivity at low inputs. The minimum possible sensitivity $S^{\hat{V}}_{h_{FE}|\,min}$ is also plotted. It shows that for $\Delta\hat{V} \cong 4$, or $\Delta V_p \cong 0.1$ V, the sensitivity cannot be less than 0.5, and for $\Delta V_p \cong 0.2$ V, the minimum sensitivity is about 0.25. Thus, unless the uniformity of h_{FE} in array applications is quite good, element-to-element nonuniformity can become a low-level problem. The physical origin of this effect is again the influence of the emitter-base diode conductance.

D. Analysis of Transient Decay

As indicated above, circuit memory f increases, hence transient response becomes more sluggish when the peak output voltage is below

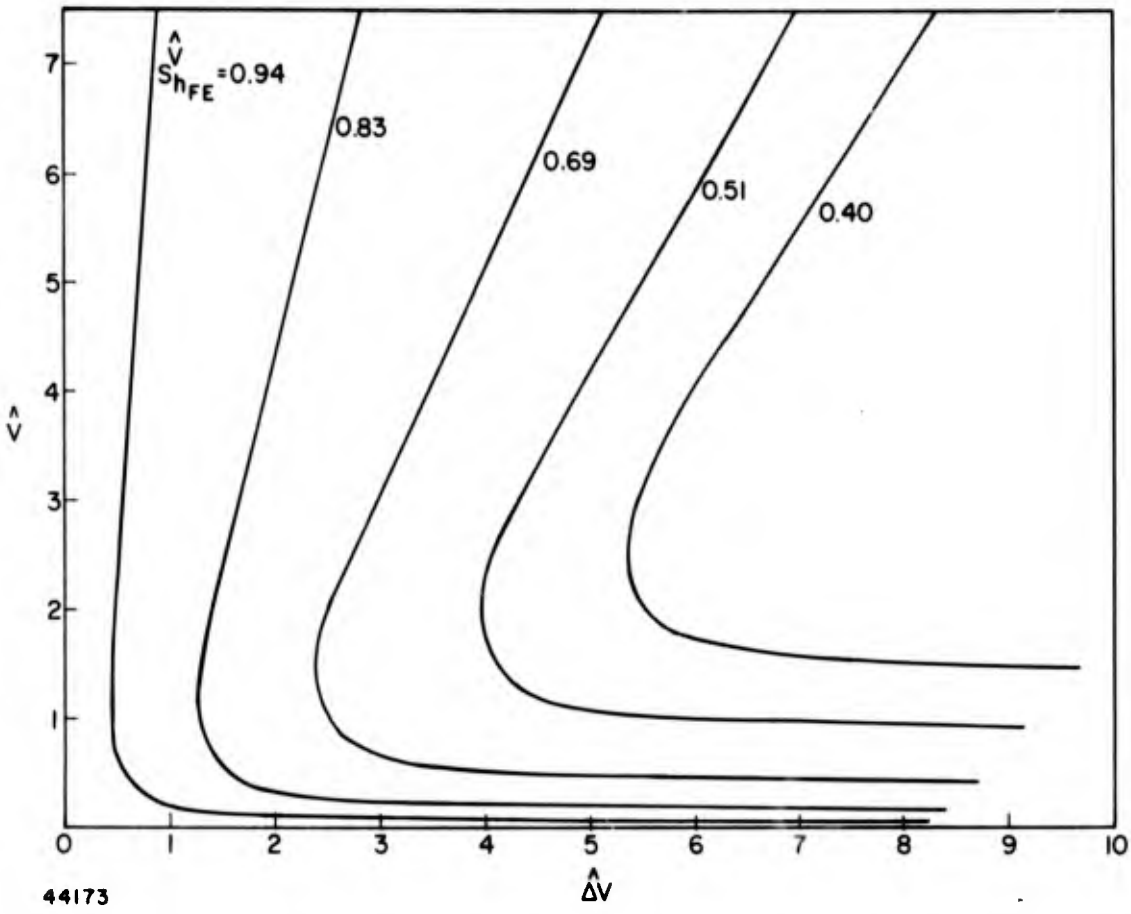


Fig. 12. CURVES OF CONSTANT $S^{\hat{V}}_{h_{FE}}$ IN INPUT-OUTPUT PLANE.

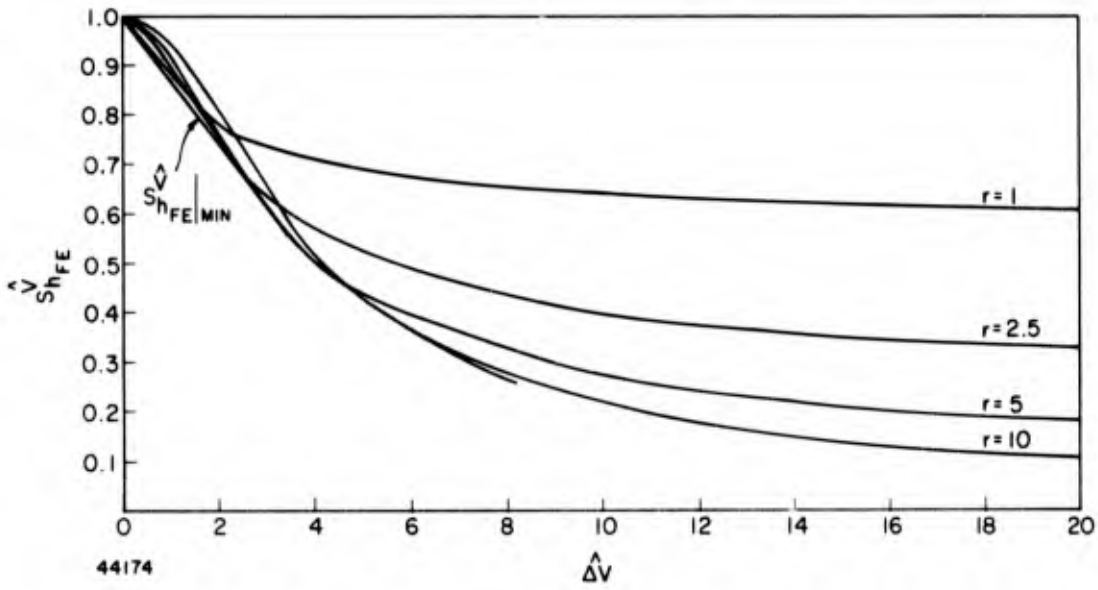


Fig. 13. h_{FE} SENSITIVITY OF PEAK OUTPUT VOLTAGE VS $\Delta\hat{V}$.

kT/q. This is shown by the scope photograph, Fig. 14, which shows the decaying sequence of output voltage pulses when illumination was cut off

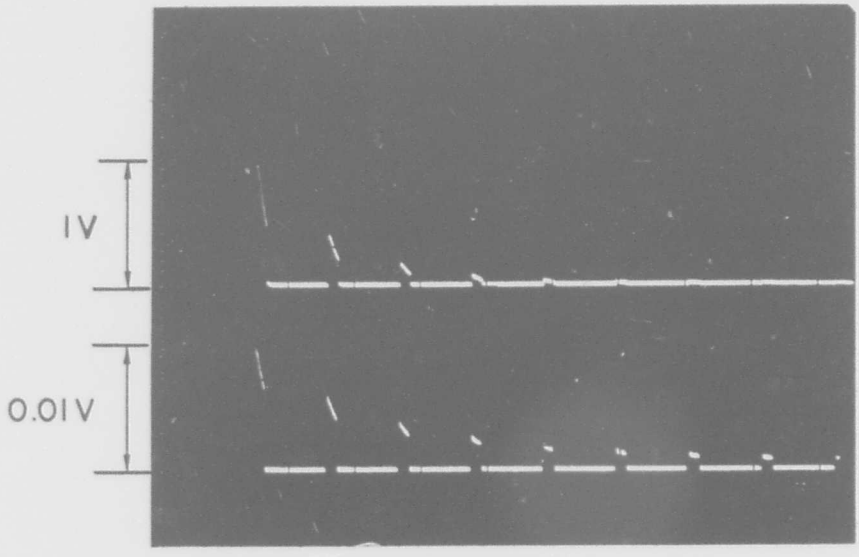


Fig. 14. COMPARISON OF HIGH AND LOW LEVEL TRANSIENT RESPONSE.

from a charge-storage phototransistor. In both traces the sample pulse was approximately equal to the circuit time constant ($r = 1$). For the upper trace, the peak value of the initial pulse was 1 V, and the succeeding pulses decay with an exponential envelope. The peak value of the first pulse was 10 mV in the lower trace, and a much-slower-than-exponential decay of succeeding pulses may be noted. This can be graphically analyzed in a simple manner by use of Eq. (3.10). If the illumination is removed (and leakage neglected) the peak output voltage at the beginning of each sample time equals the output voltage at the end of the previous sample time:

$$\hat{V}\,[(n+1)T_i] = f_n \hat{V}(nT_i) \tag{3.21}$$

where

$\hat{V}(nT_i)$ = peak voltage at beginning of n^{th} sample time

f_n = fractional memory of n^{th} pulse

and by Eq. (3.10):

$$\hat{V}(nT_i)(r + \ell n\ f_n) = \frac{1 - f_n}{f_n}$$

Thus, knowing the n^{th} output, the $(n+1)^{th}$ output can be computed using Eqs. (3.10) and (3.21). The $(n+2)^{th}$ output may then be found from the $(n+1)^{th}$ output, and so on to give the decaying sequence of output pulses. A graphical picture of this process, for the case of $r = 1$, is shown in Fig. 15 where $\hat{V}$ and $f\hat{V}$ are plotted against $\hat{V}$. The jagged dashed path constructs the output pulse sequence when illumination giving an initial value of 6 for $\hat{V}$ is cut off. The second output is found by dropping from the initial $\hat{V}$ value down to $f\hat{V}$. The third output is determined by moving to the left, back to the $\hat{V}$ line,

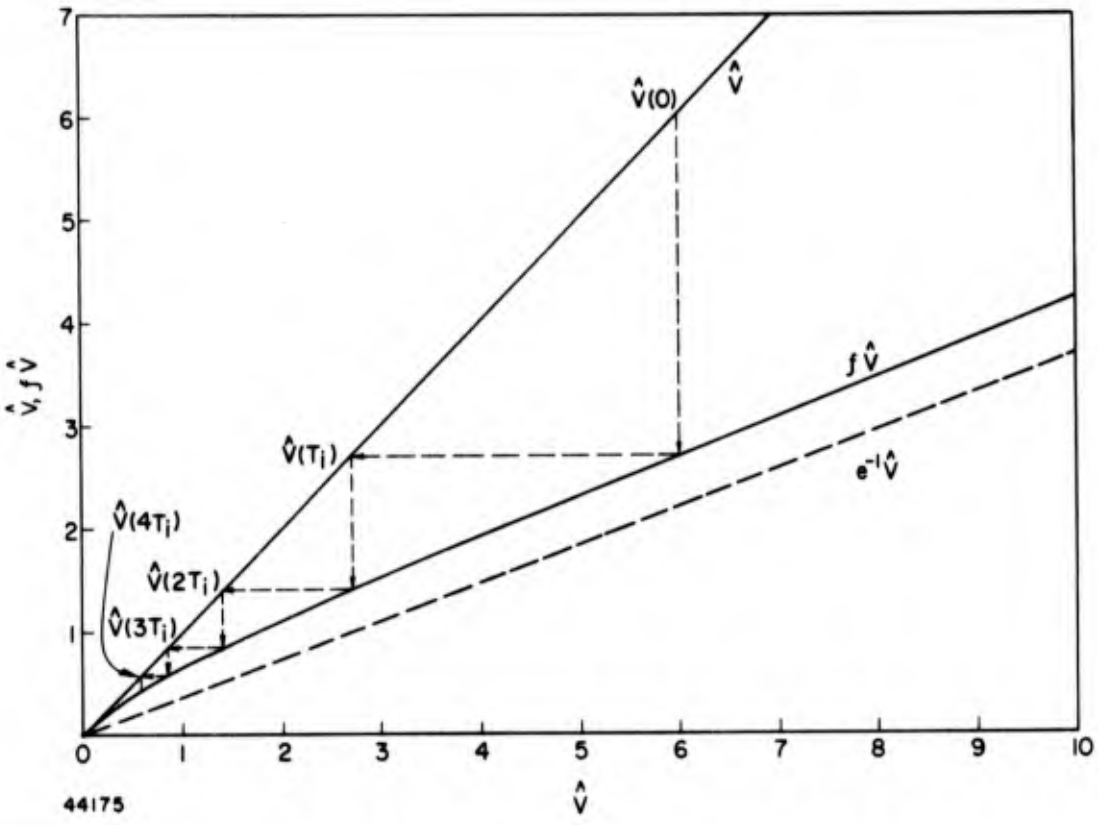


Fig. 15. CONSTRUCTION OF TRANSIENT DECAY, $r = 1$.

and then down once again to the $f\hat{V}$ curve. By repeating this procedure the output sequence is easily found. Also shown in Fig. 15 is the straight line representing $e^{-r}\hat{V}$. In the absence of low-level emitter-base junction effects, the exponential output sequence could be found by using this line for the $\hat{V}$ curve in the construction, since $f = e^{-r}$. Comparison of the $e^{-r}\hat{V}$ line with the $f\hat{V}$ curve shows how the emitter-base diode slows the transient decay, and becomes increasingly important as the output voltage level decreases.

The above scheme is basically a graphical solution of the difference equation found when f_n is eliminated from Eqs. (3.10) and (3.21). When the output becomes very much less than kT/q, this equation can be solved analytically. At these low outputs, f_n approaches unity, and the logarithmic term may be neglected in Eq. (3.10), leading to

$$f_n = \frac{1}{1 + r\hat{V}(nT_i)} \tag{3.22}$$

The difference equation is, using Eq. (3.21),

$$\hat{V}[(n+1)T_i] = \frac{\hat{V}(nT_i)}{1 + r\hat{V}(nT_i)} \tag{3.23}$$

This equation has the solution

$$\hat{V}(nT_i) = \frac{\hat{V}(0)}{1 + nT_i r\hat{V}(0)} \tag{3.24}$$

Equation (3.24) is an explicit solution for the decaying sequence of peak output voltages. It is shown to be a harmonic sequence, which decreases very slowly, in contrast to the rapidly decaying geometric sequence (exponential) observed when $\hat{V} \gg 1$. The transition between these two modes is well shown by the lower trace of Fig. 14.

E. Figure of Merit

In the preceding analysis, it was shown that the diode switch scheme may have problems of transfer characteristic nonlinearity, sluggish transient response, and sensitivity to phototransistor current gain if the input parameter $\Delta\hat{V} = (I_p T_i/C_p)/(kT/q)$ is too small. As long an integration time as possible should therefore be used, consistent with system bandwidth requirements. Since under uniform illumination both photocurrent and junction capacitance are directly related to junction area, the I_p/C_p ratio is constant for a given type of device. It may therefore be considered as a device figure of merit when a diode switch is used. Under the constraints of present integrated circuit technology, this photocurrent to capacitance ratio can be optimized to a limited degree [3]. The tradeoff is that lower capacitance per unit area implies wider depletion layer width, which, in turn, increases the dark current.

F. Validity of Assumptions

1. Photocurrent during Sample Time

A key assumption in the analysis was that the photocurrent during the sample time could be disregarded. A quantitative condition to represent this requirement is that i_B at the end of the sample time must be greater than ten times I_p. This is equivalent to the inequality

$$\beta I_K \geq 10\ I_p \tag{3.25}$$

where I_K is the peak current. This requirement can be put in a form that defines a boundary in the $\hat{V} - \Delta\hat{V}$ plane. This is shown by the dashed curves in Fig. 9 for two values of the parameter T_i/T_s, which is defined as N, the number of scanned elements. Condition (3.25) holds to the left of the boundary. The boundary intercepts the $\Delta\hat{V}$ axis at approximately

$$\Delta\hat{V} = \frac{N}{10} \tag{3.26}$$

Thus if the input $\Delta\hat{V}$ is less than N/10, we are sure that the analysis is valid, regardless of the value of r. This also implies the inverse, that when $\Delta\hat{V} \leq N/10$, an analysis that assumes complete charging of C_p at the end of the sampling period [3] is not valid.

2. Dark Current

Generation current, as well as photocurrent, will contribute to $\Delta\hat{V}$. The generation component will be independent of area, and directly proportional to integration time:

$$\Delta\hat{V}\Big|_{gen} = \frac{I_G T_i}{C_p} \Big/ \frac{kT}{q}$$

It is instructive to substitute some numbers:

$$I_G = \Gamma A_p \qquad \Gamma = 10^{-9} \text{ A/cm}^2 \text{ (see Chapter II)}$$

$$C_p = C_{pa} A_p \qquad C_{pa} = 10^{-8} \text{ F/cm}^2\dagger$$

$$T_i = 1/60 \text{ sec}$$

$$\frac{kT}{q} = 0.026 \text{ V}$$

to get

$$\Delta\hat{V}\Big|_{gen} = 0.065 \ll 1$$

This points out that dark current alone does not integrate up to a large enough $\Delta\hat{V}$ to move the operating point out of the region of low-level difficulties. Hence, unless the integration time is very long (sampling frequency of a few hertz), dark current will not be a limiting factor. In phototransistor array applications having bandwidth and uniformity constraints, low-level switching problems will dominate. This means that

† Capacitance per unit area based on 2μ diffused junction depth, 5 V bias, background concentration 10^{16}, surface concentration 10^{18} [38].

low-light-level operation of diode-switched circuits will be much worse than the ideal switch case discussed in Chapter II.

3. Switching Diode Capacitance

Another factor neglected in the analysis was the capacitance associated with the switching diode. This brings out an important distinction between the photodiode and phototransistor cases. In the photodiode situation, the only justification for disregarding the switching diode capacitance is the premise that the photodiode area is much greater than the switch diode area. A much more significant distinction happens with the phototransistor. As shown in Fig. 7b, the basic circuit model time constant is $h_{FE}R_iC_p$. If an emitter capacitance, C_e, is included, another natural mode arises with a time constant of approximately R_iC_e. This natural mode does not include the current gain factor, since current through the emitter capacitance bypasses the base. For this reason, spurious feedthrough signals due to emitter capacitance are easily filtered from the photogenerated signal. Hence, the value of the gain provided by the phototransistor is not to increase the peak output voltage, but to separate the time constant associated with the signal I_p from the spurious time constant due to switching transients. Because of this feature, the phototransistor circuit of Fig. 7a is much more useful than the photodiode circuit.

G. Summary

In this chapter the nonlinear situation resulting when a junction diode switch is used in conjunction with a charge-storage photodiode was analyzed on the basis of a simple model. The conductance of the switching diode was shown to dominate the response when the change in photodiode voltage over the sampling time, ΔV_p, is on the order of a few kT/q. This results in sluggish transient response and a nonlinear transfer characteristic. The analysis was also shown to be valid for the charge-storage phototransistor. The independence of peak output voltage from phototransistor current gain that is possible when $\Delta V_p \gg kT/q$ [3] was shown to vanish at lower input levels. For these reasons, low-light-level performance of the diode switch circuit does not match that of the ideal switch case studied in Chapter II.

Chapter IV

THE CHARGE-STORAGE PHOTODIODE AT LOW LEVELS--MOS SWITCH CASE

The most nearly ideal switching element available in integrated form is the MOS transistor. It has zero offset potential when conducting, and is capable of very high ratios of "off" to "on" resistance. It therefore seems a good candidate for the switching element of a charge-storage circuit. This possibility is considered in this chapter. Capacitive transients are shown to be a problem that can be evaded. Another spurious signal source was discovered, caused by a hitherto unreported "charge pumping" effect. A large portion of the chapter is devoted to this phenomenon.

A. Basic Properties of the Circuit

Weckler [39] has shown that all the necessary elements for a charge-storage circuit are conveniently available in a conventional MOS transistor structure. This is shown in Fig. 16, which depicts a p-channel enhancement device operating with a floating source junction. The source junction constitutes the photodiode, and the drain junction is shielded from light. When a negative gate pulse is applied, a conducting channel is induced between source and drain, and the source junction is reverse biased to the supply voltage V_R. When the gate pulse is removed, the conducting channel disappears and the switch is opened. Photogenerated

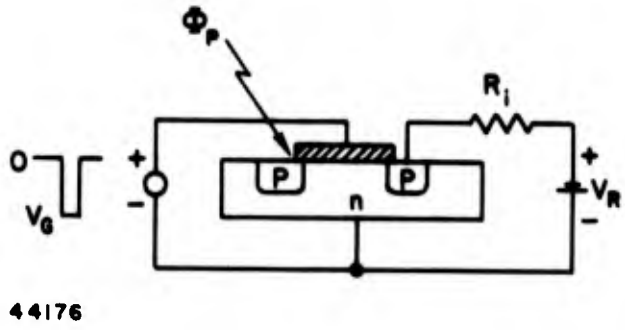


Fig. 16. MOS CHARGE-STORAGE CIRCUIT.

carriers then discharge the source capacitance. These carriers are replaced during the next gate pulse period, and the charge-storage cycle is completed. A first-order model is therefore the ideal-switch configuration of Fig. 2b. No nonlinear low-level problems are present, as in the phototransistor case. Another good feature is that arrays may be conveniently fabricated by using individual source diodes in conjunction with a common drain.

With respect to low-light-level operation, one possible difficulty might be source-to-drain leakage when the switch is nominally open. Measurements, however, show this leakage to be very low (< 1 pA) in well-made devices, so this is not a problem. The most troublesome problem is, instead, capacitively coupled transients from the MOS gate pulse. It may be recalled that the charge-storage phototransistor separates capacitive transients from the desired signal. The MOS transistor switch configuration does not accomplish this, so capacitive feedthrough and photogenerated signals cannot be distinguished during the sample time.

The magnitude of the capacitive transients may be estimated from simple MOS theory [17]. Channel conductance is given by the formula:

$$\begin{aligned} g &= 0 && |V_G| < |V_T| \\ g &= -\frac{Z}{L}\mu_p C_{oa}(V_G - V_T) && |V_G| \geq |V_T| \end{aligned} \qquad (4.1)$$

where g = channel conductance (mhos)

V_G = gate voltage (V)

V_T = threshold voltage (V)

Z = channel width (cm)

L = channel length (cm)

μ_p = hole mobility in inversion layer $\cong 200$ cm^2/V-sec

C_{oa} = oxide capacitance per unit area $\cong 4 \times 10^{-8}$ F/cm^2 for 800 Å oxide

The threshold voltage depends both on device parameters and the reverse voltage V_R applied to the junction (see Fig. 16). To a first appoximation it is true that

$$V_T = V_{TO} + V_R \tag{4.2}$$

where V_{TO} is the zero bias threshold voltage, which generally ranges from -3 to -5 V. When the gate voltage is below threshold, charge is coupled to the drain directly via gate-to-drain capacitance, which is mainly due to that portion of the gate that overlays the diffused p drain region. When the gate voltage is beyond threshold, the inversion layer beneath the gate is ohmicly connected to the drain, and the capacitive coupling from gate to drain increases. The approximate equations are:

$$\begin{aligned} Q_C &= C_{gd} V_G && |V_G| < |V_T| \\ Q_C &= (C_{gd} + C_{ox})\, V_G - C_{ox} V_T && |V_G| \geq |V_T| \end{aligned} \tag{4.3}$$

where

Q_C = capacitively coupled charge from gate to drain

C_{gd} = spurious gate-drain capacitance = $C_{oa} A_v$ (A_v = overlap area)

C_{ox} = gate oxide capacitance = $C_{oa} A_g$ (A_g = gate area)

In Fig. 17, Eqs. (4.1) and (4.3) are plotted for representative parameter values. The equations leading to Fig. 17 have been experimentally verified using discrete MOS transistors. Figure 17 shows that the higher the channel conductance, the larger the capacitive coupling will be. A channel conductance of 2×10^{-4} mho (5 kΩ), requires a -12 V gate voltage, and couples about 1.8 pC of spurious charge. In Chapter II, the most important noise source in the ideal-switch situation was the photodiode dark current. If no dc dark current compensation is employed, Fig. 6 shows I_G = 1 pA for a 10^{-3} cm^2 diode. With a 1/60 sec integration time, this corresponds to a noise charge of 0.017 pC. Comparing this to

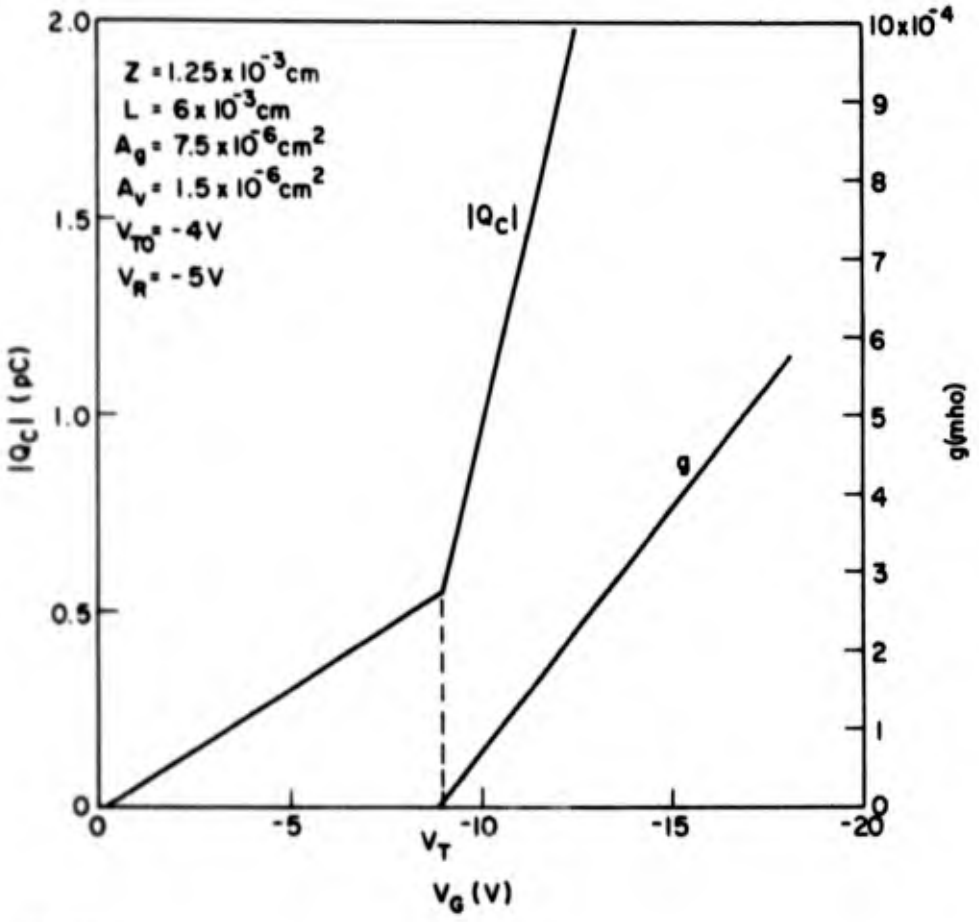


Fig. 17. CAPACITIVELY COUPLED CHARGE AND CHANNEL CONDUCTANCE VS GATE VOLTAGE.

the 1.8 pC capacitive charge, we see a two-order-of-magnitude difference between the worst-case (no compensation) charge due to generation current and a typical value of spurious capacitive charge. The capacitive charge may, of course, be compensated. However, when arrays of devices are employed, the variation in capacitive charge among devices will be large due to its geometrical (i.e., mask-alignment dependent) nature. It might be possible with fixed compensation (individual compensation of each element is clearly impractical) to reduce the variation in capacitive coupling by an order of magnitude, but this would still leave ten times the noise encountered when an ideal switch is used. For optimum low-level performance, a technique for overcoming the problem of capacitive feedthrough is required.

B. Signal Integration To Remove Capacitive Transients

A means of discriminating between capacitive feedthrough and photogenerated signal is needed. The signals are distinguished by the fact that the unwanted feedthrough contains no net dc signal component, whereas the desired photo signal is dc. Hence, discrimination may be achieved by integration of the output signal over the sample period, and not sampling the output until after the conclusion of the sampling period. The capacitive charge deposited at the leading edge of the sample pulse will then exactly be canceled by the charge removed at the trailing edge of the pulse, leaving the photogenerated charge. Figure 18 illustrates the scheme using an operational integrator. In the dark, $Q_p \cong 0$ and only the feedthrough pulse, phase-inverted and having magnitude Q_c/C_i, appears at the integrator output. The output voltage is the same before and after the sample time. When the photodiode is illuminated, all of the charge liberated during the integration time, Q_p, is also transfered to the integrator capacitor when the switch closes. The polarity of this signal is such that it subtracts from the feedthrough signal during T_s, and then, more importantly, remains at the output after the sample time. This is the desired output, and can be detected by means of a strobed comparator that samples after T_s. In a multiplexed application, this integrator will clearly have to be reset before the next element is read out. The feedback switch is provided for this task. The

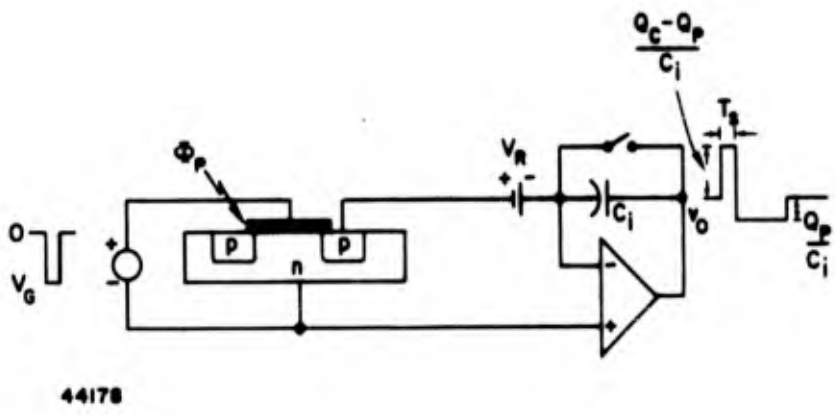


Fig. 18. INTEGRATOR FOR SUPPRESSION OF CAPACITIVE FEEDTHROUGH.

scope photograph, Fig. 19, depicts the waveform sketched in Fig. 18 (phase inverted). The photodiode was in the dark for the upper trace and illuminated for the lower trace. The properties described above are apparent, except for the reset feature.

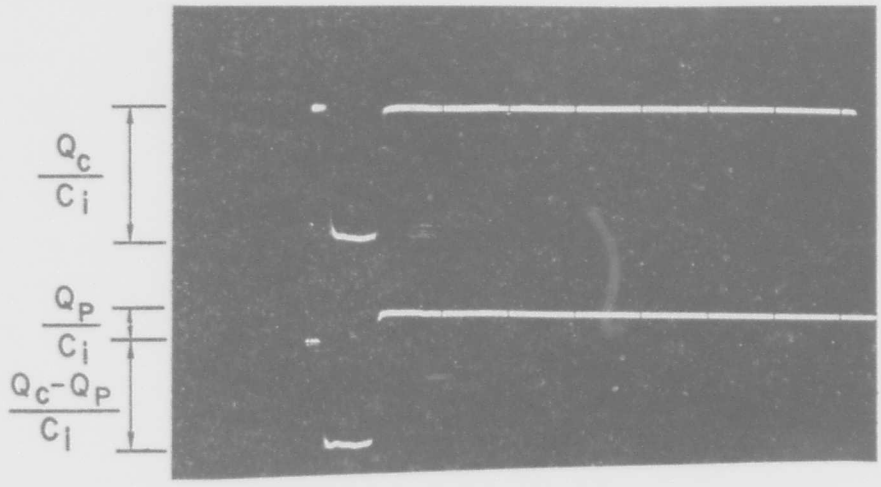


Fig. 19. WAVEFORMS ILLUSTRATING INTEGRATOR OUTPUT.

It is not necessary to use an operational integrator. If the load resistance is high, so that $f \cong 1$, the basic circuit of Fig. 2 will serve, using C_i as the integrating capacitor. Equation (2.9) then gives the circuit gain, and Eq. (2.10) defines transient response. Techniques have been worked out that remove the necessity of the reset switch using this circuit. By proper filtering and timing of the output comparator, the capacitive feedthrough can be circumvented using relatively simple circuitry.

C. The Charge Pumping Effect

When the integration scheme described above was implemented, a small net charge, having magnitude of a few percent of the feedthrough charge, was observed to be deposited on the integrating capacitor by each gate pulse. Surprisingly, the polarity observed was the opposite of that expected from dark current flow. It appeared that each gate pulse was stimulating injection in the forward-biased direction of the source and drain junctions, even though they were reverse biased. Careful investigation of this phenomenon resulted in the discovery of a "charge pumping"

effect in MOS structures. The remainder of the chapter is devoted to this subject, since it has not been reported in the literature [40,41], and is a limiting factor to the performance of the MOS photosensing structure.

1. The Basic Experiment

The MOS experiment shown in Fig. 20 clarified the effect. Source and drain of an ordinary (not photosensing) MOS transistor were connected and reverse biased ($V_R < 0$) with respect to the substrate. The substrate current was smoothed by a capacitor and fed to a dc ammeter. In the absence of any gate pulses, this ammeter simply indicated the negative reverse leakage currents of the two junctions. However, when the substrate was periodically inverted by negative gate pulses, the dc substrate current reversed polarity and became positive.. Its magnitude increased with gate pulse frequency, becoming linearly proportional to frequency when leakage effects were swamped. The linearity of current

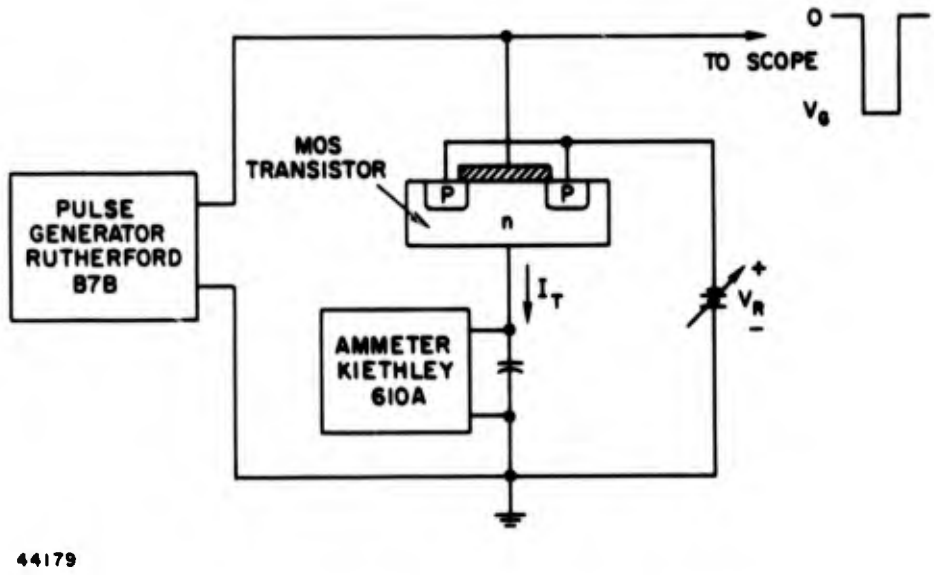


Fig. 20. BASIC MOS CHARGE PUMPING EXPERIMENT.

with frequency is shown in Fig. 21. It is clearly indicative of a charge pumping action whereby a fixed charge is measured at each gate pulse. Since no dc component of the measured magnitude can flow through the oxide, this charge must be injected across the junctions. It is

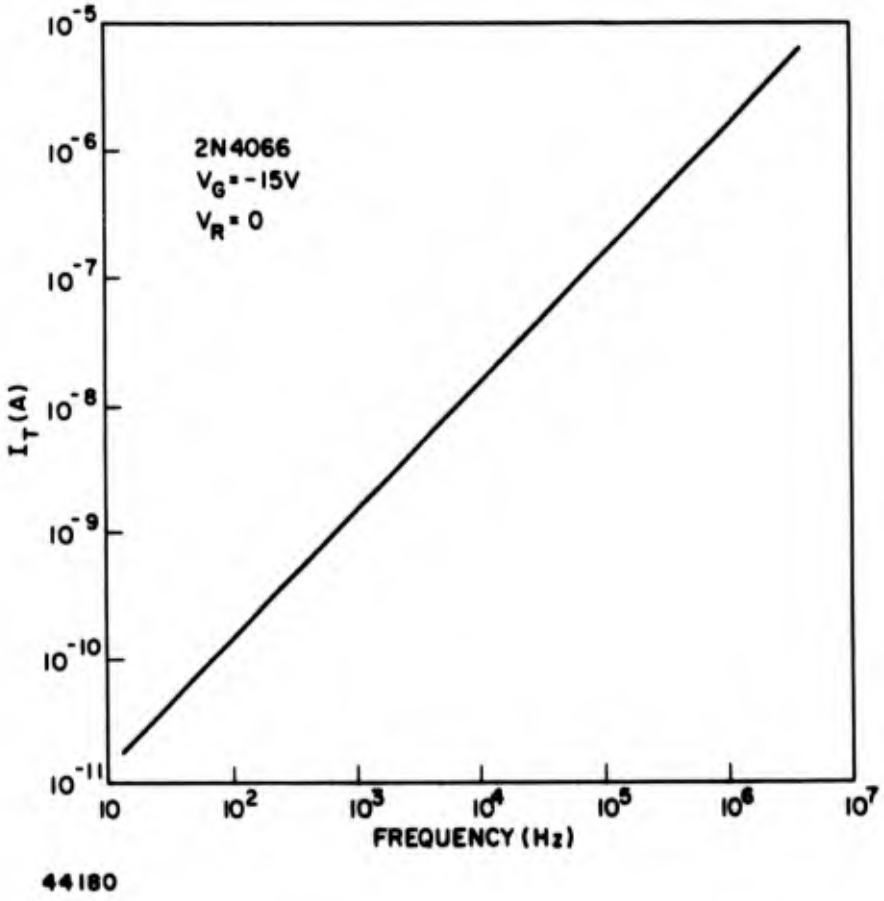


Fig. 21. DC SUBSTRATE CURRENT VS GATE PULSE FREQUENCY.

interesting to note that this results in a power flow into the battery from the pulse source.

A dc current measurement was employed since quantitative measurement of instantaneous currents and voltages was not profitable inasmuch as the pumped charge was overwhelmed by capacitively coupled charge. The basic experiment of Fig. 20 was performed with a number of MOS transistors having different geometries and made by different manufacturers, including some fabricated at Stanford.† The charge pumping effect was observed without exception in all of the units tested. One important

† By M. Barron.

geometrical effect noted is that the magnitude of the current was approximately proportional to the transistor gate area. An independent measurement at Fairchild Semiconductor also verified these observations. Another interesting verification was obtained by open-circuiting the battery connection in Fig. 20, and observing (with an electrometer voltmeter) that a dc reverse bias was built up across the source/drain junction when gate pulses were applied. This clearly indicated a buildup of electrostatic charge due to the pumping effect.

The magnitude of the substrate current at a fixed frequency is plotted vs gate pulse amplitude in Fig. 22 for three values of junction reverse bias. A threshold gate voltage is seen, below which no current is measured. As the gate pulse amplitude is increased, a sharp rise in current is observed, followed by saturation. The current remains saturated

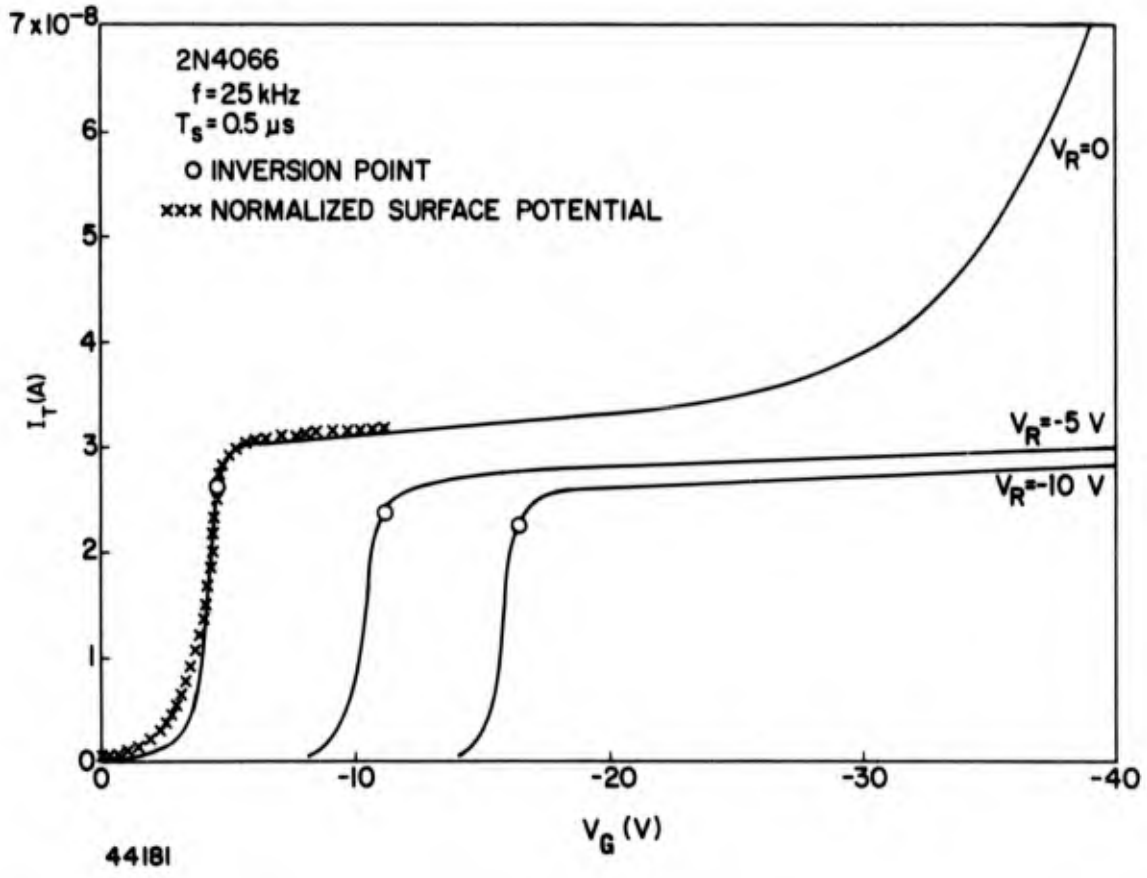


Fig. 22. DC SUBSTRATE CURRENT VS GATE VOLTAGE.

up to the device gate voltage limits, except when $V_R = 0$, in which case the current plot curves upward at higher gate voltages. If either source or drain alone was connected, the $V_R = 0$ curve was modified, so that the current rise after saturation occurred at a lower value of gate voltage.

The onset of substrate inversion could be measured by applying a small (0.25 V) drain-to-source potential and noting the gate voltage necessary for the onset of channel current. The measured gate threshold voltage is marked on the three curves. The threshold voltage increases with junction reverse bias, as predicted by Eq. (4.2). Current saturation is seen to occur approximately at the gate threshold points.

Two mechanisms have been identified as contributing to the "pumped" current. One component originates from the presence of surface states at the gate $Si\text{-}SiO_2$ interface and the other from free charge in the inversion layer under the oxide.

It is a well-understood effect that inversion layer and surface state charging is limited by thermal generation of minority carriers in MOS capacitor structures [42], and that if an opposite conductivity region is provided adjacent to the inverted region, this limitation is removed [17,43]. This is because the minority carriers necessary to maintain equilibrium conditions in the inversion region are readily obtained via minority carrier injection. This circumstance applies to the p-channel transistor under investigation; when the n-type substrate is inverted, minority carriers (holes) are supplied to the channel by the p-type source and drain regions. This results in a transient pulse of substrate current. If all of this injected charge cannot return to the p regions at the trailing edge of the gate pulse, but recombines into the substrate either via surface states or in the bulk, then a net current flow results. We therefore write the following expressions for the "trapped" charge density:

$$Q_{TA} = \beta Q_{IA} + qN_{ST} \tag{4.4}$$

and current;

$$I_T = fA_g Q_{TA} \tag{4.5}$$

where

Q_{TA} = net injected charge density per gate pulse (coul cm^{-2})

Q_{IA} = free charge (hole) density in inversion layer under gate (coul cm^{-2})

β = fraction of free holes under gate that recombine into substrate

N_{ST} = total fast surface-state density contributing to effect (cm^{-2})

I_T = average substrate current

f = gate pulse frequency

The first term of the right side of Eq. (4.4) is designated the "geometrical component," and the second the "surface-state component." These two terms are considered in more detail in the following two sections.

2. Geometrical Component of Trapped Gate Charge

The charge density in a conducting channel follows from Eq. (4.1):

$$Q_{IA} = 0 \qquad |V_G| < |V_T|$$

$$Q_{IA} = C_{oa}(V_G - V_T) \qquad |V_G| \geq |V_T| \tag{4.6}$$

Equation (4.6), when substituted into Eq. (4.4), indicates that the pumped charge should increase linearly with gate voltage above threshold. This is not true for the transistor of Fig. 22, which exhibits a saturating characteristic beyond threshold. The characteristic of an MOS gate-controlled diode structure,† Fig. 23, does show this behavior. The gate-controlled diode consisted of a small circular p-n junction surrounded by a much larger area annular MOS gate. It seems intuitively clear that this geometrical configuration is much more favorable to the trapping of channel charge than is an ordinary MOS transistor structure, since the p region perimeter is small and the gate area large.

† Kindly supplied, along with MOS transistor data, by L. J. Kabell of Fairchild Semiconductor.

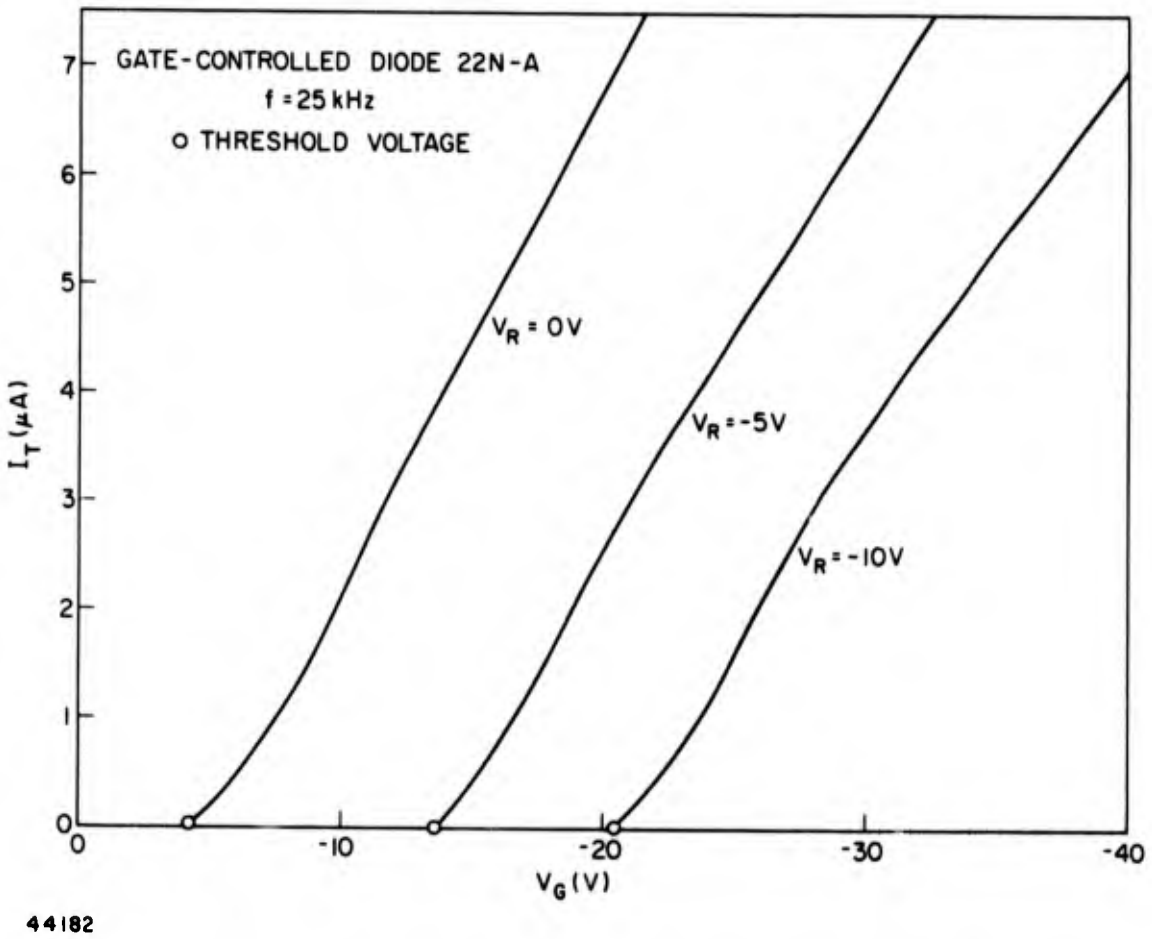


Fig. 23. SUBSTRATE CURRENT VS GATE VOLTAGE-GATE CONTROLLED DIODE.

This idea is clarified by inspection of the characteristics of three Stanford-fabricated transistors, Fig. 24. The three transistors were on the same chip, but had different gate geometries. Transistors 2 and 3 had conventional gate geometries, with a high width-to-length ratio for high channel conductance [see Eq. (4.1)] and device transconductance. The substrate current characteristic of these two transistors resembles that of Fig. 22. Since the gate area of transistor 3 was double the gate area of No. 2, its saturated current is about twice as big. The gate area of transistor 1 was approximately the same as No. 2, but its geometry was quite unconventional, having a width-to-length ratio less than one. Its characteristic did not exhibit current saturation. The qualitative explanation for this is simply that its narrow, long channel configuration is not favorable to free channel charge removal, relative to

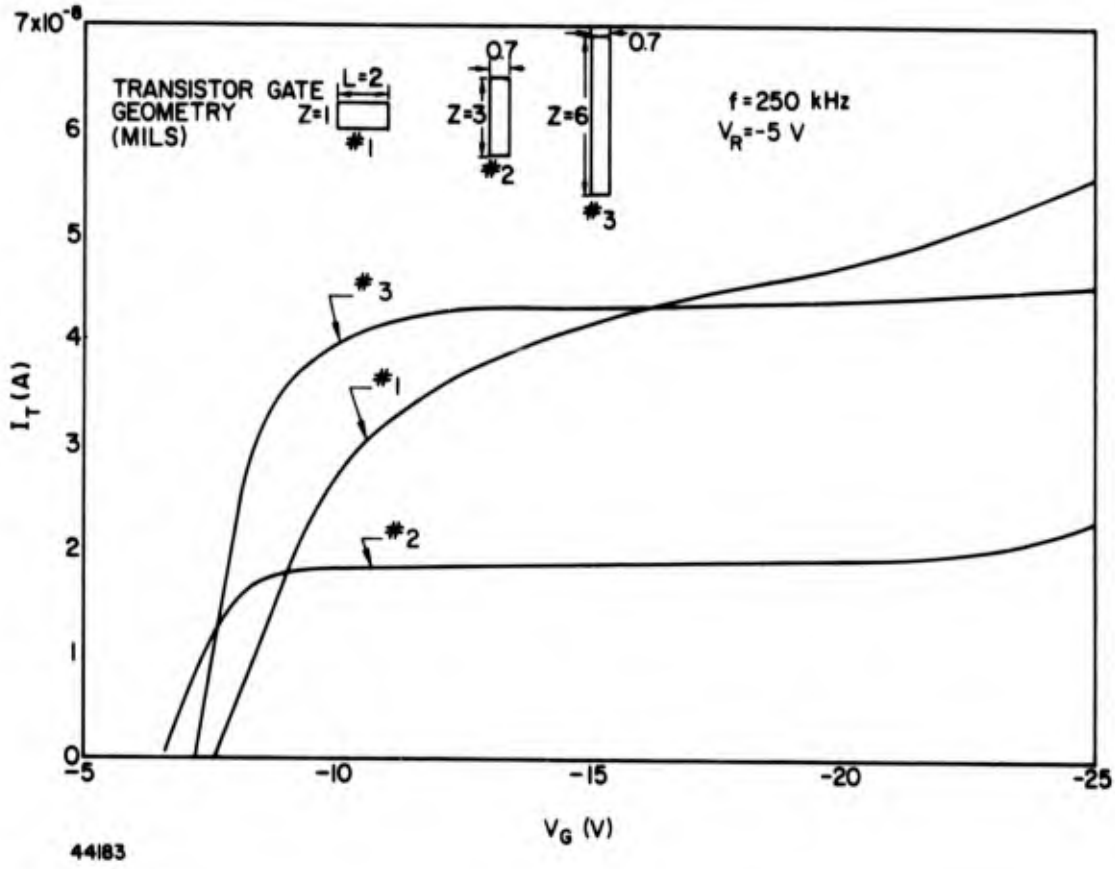


Fig. 24. SUBSTRATE CURRENT VS GATE POTENTIAL OF THREE STANFORD TRANSISTORS.

the conventional high Z/L geometries of transistors 2 and 3. Hence, the first term of the right side of Eq. (4.4) is much more significant with transistor 1. This geometrical dependency of β is the reason for the term "geometrical component" for the component of trapped charge due to free carriers that recombine into the substrate.

As long as the gate voltage is beyond threshold, a conducting contact in effect exists from inversion layer to source and drain, through which charge can readily flow in and out of the channel. One would therefore expect that, if long rise time gate pulses are applied rather than the fast rise time (20 ns) pulses used above, the "geometrical" trapping of free charges due to transport delay effects would diminish. This is strikingly shown by Figs. 25 and 26, which compare substrate current characteristics using square and sawtooth gate waveforms.

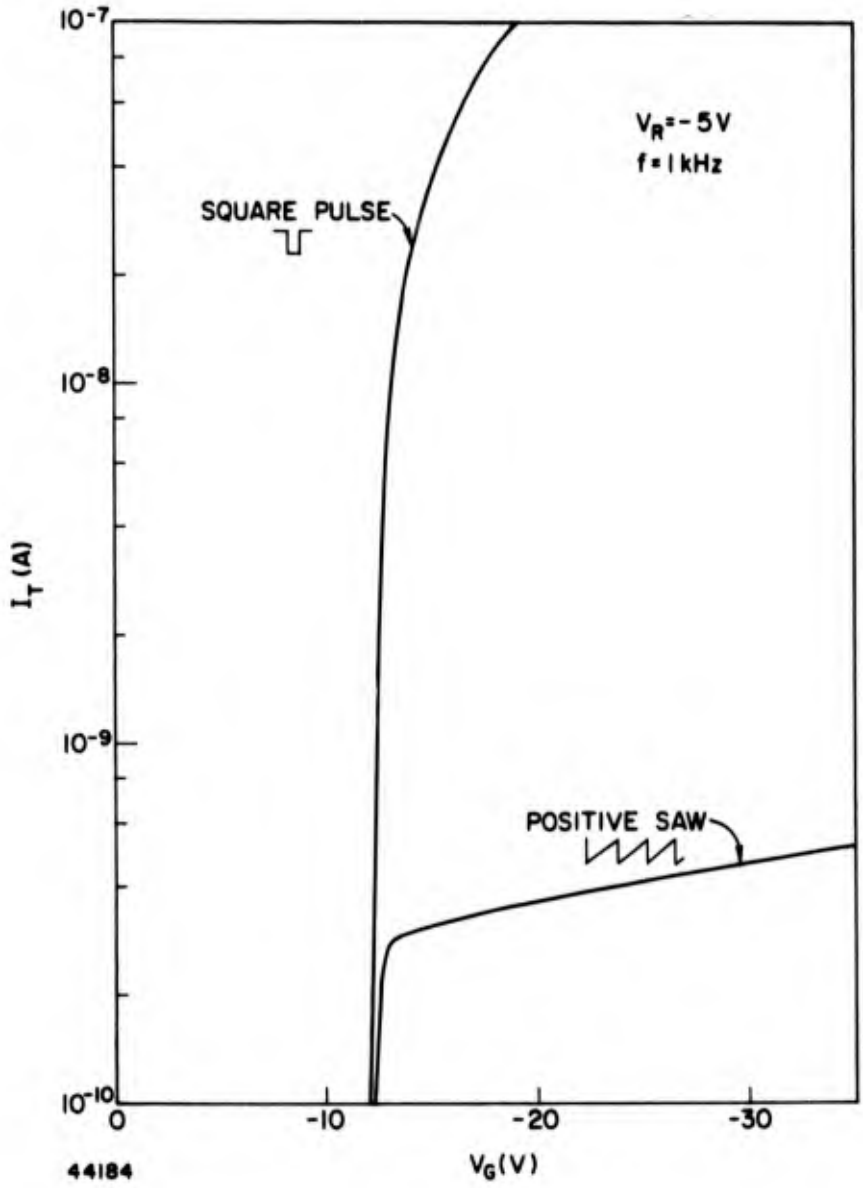


Fig. 25. COMPARISON OF SQUARE AND SAWTOOTH GATE WAVEFORMS--GATE CONTROLLED DIODE.

The gate-controlled diode current dropped about two orders of magnitude when a sawtooth was applied, as depicted in Fig. 25. Figure 26 compares transistors 1 and 2 of Fig. 24, showing how the geometrical term present in the characteristic of No. 1 vanishes when a sawtooth is applied, and the saturated currents of the two transistors become nearly identical.

The factor β in Eq. (4.4) is thus a function of gate pulse amplitude and waveform, and device geometry. A quantitative theory is

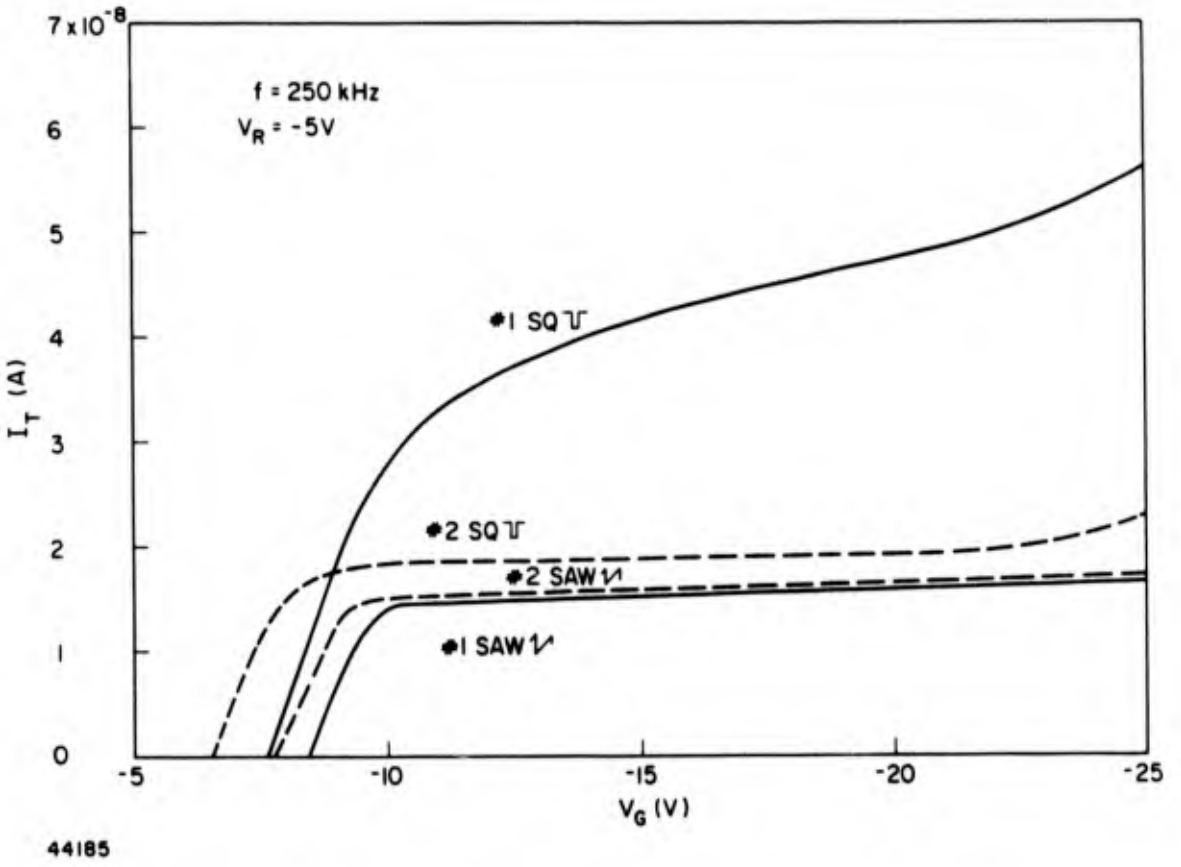


Fig. 26. COMPARISON OF SQUARE AND SAWTOOTH GATE WAVEFORMS, TRANSISTORS 1 AND 2.

difficult due to the three-dimensional distributed nature of the problem. Such a theory will not be attempted, since this component of current is not predominant in the conventional geometry MOS switches envisioned for the photosensing application. Even should it be present, it could be eliminated by use of nonsharp gate pulses.

3. Surface-State Component of Trapped Gate Charge

The current flow in Fig. 26 with a sawtooth gate pulse is attributed to charge coupling via "fast" surface states at the $Si-SiO_2$ interface. Experimental confirmation of this hypothesis was attained from a heat-treat experiment. According to Deal et al [44], fast surface states can be induced at the $Si-SiO_2$ interface by application of fields between 50 and 75 V/μ across the oxide at temperatures of 300-450°C for a few minutes. Lower fields or temperatures, with properly made devices,

will not alter the surface states. Since no other electrical properties of the transistors should be significantly altered by the heat treatment, this experiment offered a way to determine whether surface states play a role in the charge-pump phenomenon.

Data will be presented for a 2N4066, which is dual device containing two transistors for chopper applications. The transistors have very high Z/L (116), so the geometrical component of current is negligible. Before the heat treatment, both transistors had identical characteristics, as shown by the dashed curve in Fig. 27. The device was then placed for 5 min at 400°C, with the gate of one transistor biased at -30 V while the other was shorted. After heating, the transistor with no applied field showed a nearly unchanged characteristic. The characteristic of the other transistor changed markedly, giving about four times the saturated current, and a considerably shifted threshold. Similar results were found using different transistors. MOS capacitance measurements were also taken before and after heat treatment. The capacitance measurements clearly showed the increase in surface-state density caused by the heat treatment, as well as the correlation between this increase and the rise in pumped current.

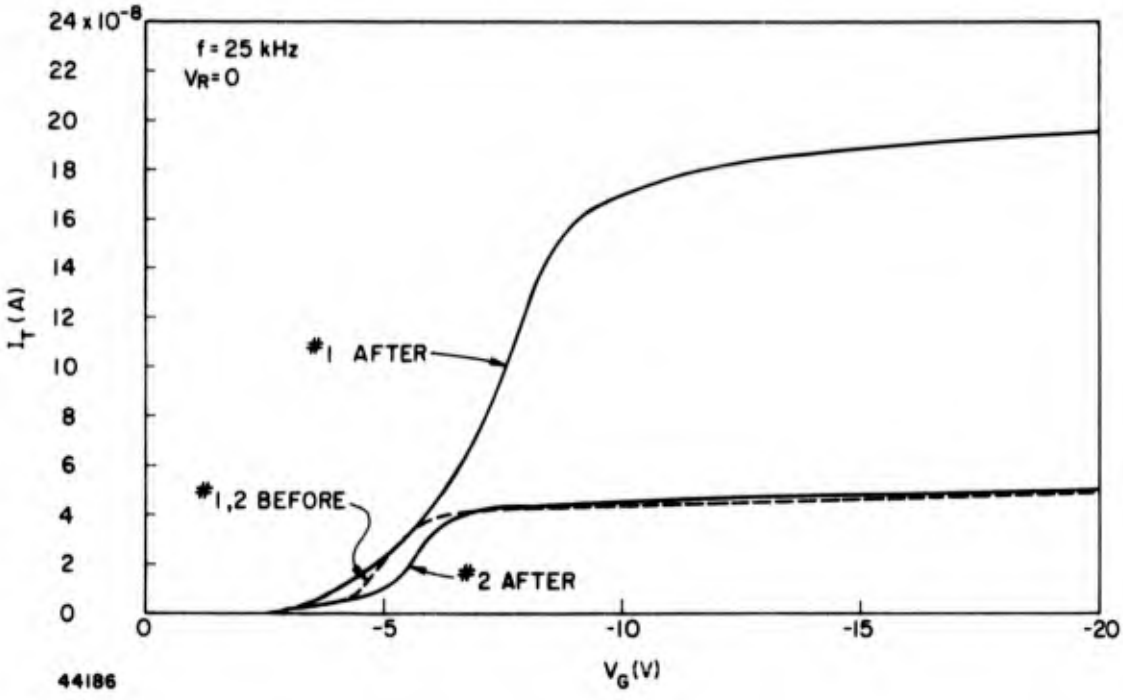


Fig. 27. 2N4066 BEFORE AND AFTER HEAT TREATMENT.

Clearly, only the "fast" surface states can contribute to the effect, and not those that result in a fixed charge independent of substrate surface potential [44]. It is worthwhile to consider numerical values applying to the 2N4066, which has a gate area of 1.16×10^{-4} cm^2. Figure 21 shows that a saturated substrate current of 1.4 nA flows at a gate pulse frequency of 1 kHz, so the charge delivered per pulse is 1.4 pC. Assuming that each surface state couples one unit of charge, the required surface state density is

$$\frac{1.3 \times 10^{-12}}{(1.6 \times 10^{-19})(1.16 \times 10^{-4})} = 7 \times 10^{10} \text{ cm}^{-2}$$

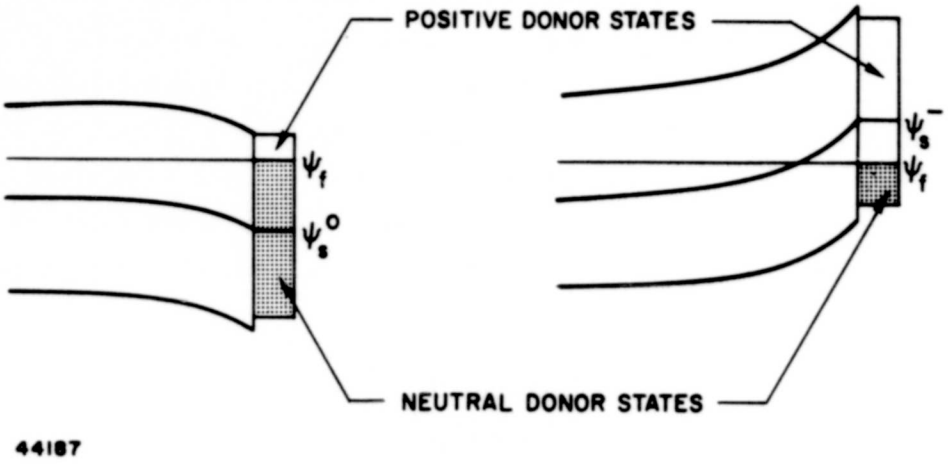
This figure agrees well with reported [45] values for thermally oxidized silicon. Results of this surface-state density computation varied between 4×10^{10} and 8×10^{10} cm^{-2} for other transistors.

A simple interpretation of how surface states are able to act as a charge-coupling medium is presented in Fig. 28. A uniform trap distribution, N_T traps/cm^2 V, is assumed through the band gap. When zero gate voltage is applied, most of the traps (considered to be donors) are below the Fermi level and neutral. When the gate voltage goes negative, the energy bands are bent upward, and most of the traps move above the Fermi level, becoming positive. We consider that holes are drawn in from the p-type source and drain to fill the traps. When the gate voltage returns to zero, electrons from the substrate bulk neutralize the injected holes, and the starting point of the cycle is reached. The net injected charge is therefore proportional to the trap density times the peak-to-peak bending of the bands:

$$Q_T = qN_T(\psi_s^o - \psi_s^-) = qN_T \ \Delta\psi_s \tag{4.7}$$

so that, from Eq. (4.4),

$$N_{ST} = N_T \Delta\psi_s \tag{4.8}$$



a. Zero gate voltage b. V_G applied

ψ_f = Fermi potential

ψ_s = surface potential

Fig. 28. ILLUSTRATING SURFACE-STATE MECHANISM.

The current is, using Eq. (4.5),

$$I_T = fA_g \, qN_T \, \triangle\psi_s \tag{4.9}$$

Equation (4.9) predicts that, as the gate pulse amplitude changes, the pumped current should be proportional to surface potential. The calculated† ideal surface potential corresponding to V_G is plotted vs V_G in Fig. 22. This surface potential plot has been normalized to match the pumped current plot at the inversion point. Quite good match of the two curves is apparent. The sharp rise of the current plot occurs when the bands swing through their largest excursion (the depletion region) and saturation is due to the "pinning" of the surface potential that occurs after the surface is inverted [17]. Of course, the trap distribution

† Computed by M. Barron.

within the band is generally not uniform, and the surface potential calculation should account for the presence of the traps, but first-order theory leading to Eq. (4.9) seems remarkably well verified by Fig. 22. These ideas may be extended to suggest that the phenomenon may prove useful for quantitative measurement of surface-state distribution within the band gap. At any rate, "global" measurement of the total state density is achieved.

Other experiments have been performed that support the above theory, such as varying the positive gate voltage excursion rather than keeping it at zero. The dynamics have also been investigated, and surface-state time constants calculated which are compatible with experimental observations.

In most MOS transistor applications, source and substrate are shorted, and the pumped current will unnoticeably circulate in this loop. In applications where this is not the case, such as choppers, this effect can limit ultimate performance. In the MOS charge-storage circuit (Figs. 16 and 18), pumped charge cannot be distinguished from photogenerated charge. If a switch gate area $A_g = 2\ \text{mil}^2 = 1.25 \times 10^{-5}\ \text{cm}^2$, and $N_{ST} = 7 \times 10^{10}\ \text{cm}^{-2}$ are assumed, then the pumped charge per cycle is $(1.6 \times 10^{-19})(1.25 \times 10^{-5})(7 \times 10^{10}) = 0.14$ pC. This charge is roughly an order of magnitude lower than the capacitive feedthrough charge calculated previously, and an order of magnitude higher than the charge due to generation current. Thus, when capacitive feedthrough is removed by integration, the pumped charge is the biggest remaining noise source. Cancellation of pumped charge is of course possible, and the ultimate limiting factor in array applications will be its spatial variation from element to element. This subject is treated quantitatively in the next chapter.

D. Summary

The MOS transistor was shown to provide a convenient structure that combines a photodiode and switch for charge-storage use. The significant

departures from ideal switching were found to be capacitive feedthrough of switching transients, and an unusual charge pumping effect. Using a signal integration scheme to eliminate the feedthrough problem, the charge pumping effect was found to limit ultimate performance more seriously than photodiode dark current.

Chapter V

LOW-LIGHT-LEVEL COMPARISON OF PHOTOTRANSISTOR AND MOS ARRAYS FOR A READING AID

The charge-storage phototransistor described in Chapter III is here compared vis-à-vis the photodiode-MOS switch combination of Chapter IV with respect to low-light-level capability. The comparison is directed toward the blind reading aid system outlined in Chapter I, for which an integrated array of 100 to 200 elements is envisaged. Electrical non-uniformities from element to element in the array are found to be the major performance-limiting factor. Conventional optics are assumed for the system, and the effects of varying the photodiode area are investigated. Optimum areas were found to exist for both of the two schemes, with the MOS switch providing the best optimized performance. If a photodiode area constraint is imposed, the relative advantage of the MOS scheme is shown to diminish with decreasing area.

A. System Configuration

An optical block diagram of the reading aid system appears in Fig. 29. The reading material is illuminated by flux Φ_I. The reflected light from

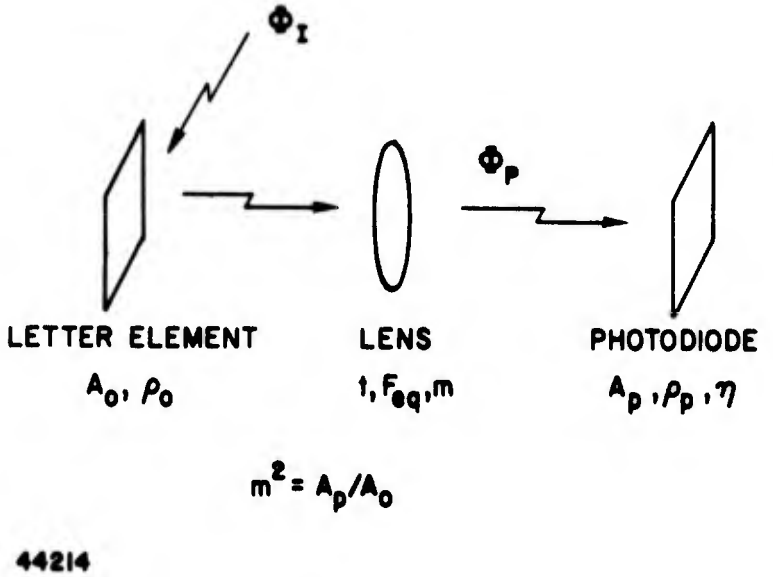


Fig. 29. SYSTEM OPTICAL CONFIGURATION.

each letter element is focused by a lens system onto a charge-storage photodiode. This photodiode may be the collector-base diode of a phototransistor or the source diode of an MOS transistor, and is considered to be one element of a multiplexed integrated array. The size of each letter element is fixed from system requirements dictated by the size of typical printed characters and the number of elements to be used. Current thinking indicates a rectangular 5 by 10 mil area to be satisfactory. Within this constraint, the photodiode area may be varied (within practical limits) to optimize performance. A more convenient alternative point of view is that the lens linear magnification $m = \sqrt{A_p/A_o}$ may be optimized.

A formula is needed that governs the passage of flux through the optical system. If the page is assumed perfectly diffusing, i.e., obeys Lambert's cosine law, the following formula applies [46]:

$$\frac{\Phi_P}{\Phi_I} = \frac{\rho_o t}{4F_{eff}^2} \tag{5.1}$$

where

ρ_o = page reflectance

t = lens transmission

F_{eff} = "effective F-number" = image distance/aperture diameter

The effective F-number can be written

$$F_{eff} = F_{eq}(1 + m) \tag{5.2}$$

where

F_{eq} = "eqivalent F-number" (the F-number of an equivalent thin lens)

m = lens magnification = $\sqrt{A_p/A_o}$

As described in Ref. 46, F-number as ordinarily defined may be meaningless in the case of a compound lens, which necessitates the use of effective and equivalent F-numbers. The factors ρ_o and t account respectively for absorption by the page and lens losses. Since ρ_o and t are less than unity, and F_{eff} may be shown to be always greater than 1/2, Eq. (5.1) indicates that $\Phi_p \leq \Phi_I$. The photodiode flux density thus cannot exceed the flux density falling upon the page. In general, Φ, ρ_o, t, and η are functions of radiation wavelength. Monochromatic illumination will be assumed throughout this discussion for simplicity.

Qualitative justification for the existence of an optimum photodiode area follows from the solution of Eq. (5.1) for photocurrent:

$$I_p = q\eta(1 - \rho_p)\, A_p \Phi_p = \frac{q\eta\rho_o(1-\rho_p)t}{4F_{eq}^2} \frac{A_p}{\left(1 + \sqrt{A_p/A_o}\right)^2} \Phi_I \qquad (5.3)$$

The factor $1 - \rho_p$ accounts for reflection from the surface of the photodiode. The photocurrent is seen to approach a constant for $A_p \gg A_o$. This occurs because flux density decreases at the same rate that A_p increases. Photocurrent becomes constant with increasing A_p, but photodiode capacitance and leakage increase linearly with A_p, so signal-to-noise ratio must diminish at large photodiode areas. Conversely, I_p goes to zero as A_p vanishes, so the signal-to-noise ratio must go down if the photodiode area becomes too small. Hence, an optimum photodiode area will be found. It remains to be seen how sharp the optimum is and whether it leads to physically reasonable values of lens magnification.

B. Optimum Phototransistor Area

It was explained in Chapter III how low-level problems were encountered when the change in voltage across the transistor collector-base photodiode during the integration time became comparable to kT/q (26 mV). This limited low-level performance at a higher level than set by generation current, unless the operating frequency was very low. A high

enough sampling frequency will be assumed in this analysis for low-level performance to be constrained by ΔV_p considerations. Specifically we require

$$\Delta\hat{V} \geq \alpha \tag{5.4}$$

or

$$\Delta V_p \geq \alpha \frac{kT}{q} \tag{5.5}$$

for useful operation of our array of charge-storage phototransistors to be possible. Equation (5.5) may be written

$$\frac{I_p T_i}{C_{pa} A_p + C_{ea} A_e} \geq \alpha \frac{kT}{q} \tag{5.6}$$

where

C_{pa} = photodiode capacitance per cm^2

C_{ea} = emitter capacitance per cm^2

A_e = emitter area, cm^2

Alpha is chosen from system considerations of bandwidth and parameter sensitivity. Its choice is discussed in more detail subsequently. As pointed out in Chapter III, the ratio of photocurrent to capacitance is the figure of merit to be optimized. In this case, a term accounting for the capacitance of the reverse-biased emitter junction, which is in parallel with the collector-base junction during storage (see Fig. 7a), is included in Eq. (5.6). Because of the order of impurity diffusion, C_{ea} will be larger than C_{pa} by approximately a factor of 10. The existence of an optimum photodiode area is implicit in Eq. (5.6). When A_p goes to zero, I_p does likewise, and the left side of Eq. (5.6) vanishes. As

A_p approaches infinity, I_p becomes constant, but the denominator increases with A_p, so the left side of Eq. (5.6) again vanishes. An optimum occurs at intermediate values of A_p, and is evaluated by combining Eqs. (5.3) and (5.6):

$$\frac{q\eta\rho_o(1-\rho_p)tT_i}{4F_{eq}^2}\,\frac{A_p}{\left(1+\sqrt{A_p/A_o}\right)^2\left(C_{pa}A_p+C_{ea}A_e\right)}\,\Phi_I \geq \alpha\,\frac{kT}{q} \qquad (5.7)$$

Substituting $A_p = m^2 A_o$,

$$\frac{q\eta\rho_o(1-\rho_p)tT_i}{4F_{eq}^2\,C_{pa}}\left[\frac{m^2}{(m+1)^2\left(m^2+\dfrac{C_{ea}A_e}{C_{pa}A_o}\right)}\right]\Phi_I \geq \alpha\,\frac{kT}{q} \qquad (5.8)$$

Defining $\Phi_I = \Phi_I\big|_{minpt}$ when equality obtains in Eq. (5.8) and $\gamma_{pt} = C_{ea}A_e/C_{pa}A_o$ = ratio of emitter capacitance to collector (photodiode) capacitance if photodiode area equals letter element area ($m = 1$), gives

$$\frac{q\eta\rho_o(1-\rho_p)tT_i}{4F_{eq}^2C_{pa}}\left[\frac{m^2}{(m+1)^2\,(m^2+\gamma_{pt})}\right]\Phi_I\big|_{minpt} = \alpha\,\frac{kT}{q} \qquad (5.9)$$

$\Phi_I\big|_{minpt}$ is the minimum usable flux density incident on the reading matter. All other quantities being constant, it is clearly minimized by choice of the value of m which maximizes the bracketed function in Eq. (5.9). The optimum m is easily found by differentiation to be

$$m_{opt} = \gamma_{pt}^{1/3} \qquad (5.10)$$

Substituting Eq. (5.10) into Eq. (5.9), the minimum usable flux density at the optimum magnification is expressed:

$$\Phi_I\Big|_{minpt} = \frac{4F_{eq}^2 \alpha \frac{kT}{q} C_{pa}}{q\eta\rho_o(1 - \rho_p)tT_i}\left(1 + \gamma_{pt}^{1/3}\right)^3 \qquad (5.11)$$

The optimum magnification given by Eq. (5.10) is a function of the ratio of emitter capacitance to collector capacitance at unity magnification:

$$m_{opt} = \left(\frac{C_{ea}A_e}{C_{pa}A_o}\right)^{1/3} \qquad (5.10)$$

Using $C_{ea}/C_{pa} = 10$, and $A_e/A_o = 0.02$ gives $\gamma_{pt} = 0.2$ and $m_{opt} = 0.6$. If $A_o = 50$ mil^2, then $A_p\Big|_{opt} = m_{opt}^2 A_o = 18$ mil^2, which is a physically reasonable figure. A plot of the left side of Eq. (5.9) vs m for these numbers is given in Fig. 30 to illustrate the effects of a nonoptimum choice of m. The plot is normalized to a peak value of unity. The optimum is not too sharply peaked; positive deviations of m from the optimum exhibit less penalty than negative deviations of the same magnitude.

In order to compute the minimum usable flux density from Eq. (5.11), a value for alpha must be assumed. The limiting factor is system transient response (Fig. 11) and/or sensitivity to phototransistor current gain (Fig. 13) at small $\Delta\hat{V}$. Transient response is probably not a difficulty as long as $\Delta\hat{V}$ is greater than 1. Current gain sensitivity is greater than 0.5 if $\Delta\hat{V}$ is less than 4, and will be troublesome unless very uniform arrays are fabricated. The required degree of array uniformity for the reading aid is a systems question not easily answered. It depends upon such factors as the uniformity of the page illumination and optical system, the page contrast, and the method of setting the threshold. For the present purpose, we will require h_{FE} sensitivity to be less than 0.5, hence $\Delta\hat{V}$ must exceed 4. Taking this value for α, and other representative values:

$\eta = 0.6$ $\qquad$ $T_i = 1/60$ sec

$\rho_o = 0.9$ (white paper) $\qquad$ $F_{eq} = 1$

$\rho_p = 0.4$ $\qquad$ $C_{pa} = 10^{-8}$ F/cm^2

$t = 0.9$ $\qquad$ $\gamma_{pt} = 0.2$

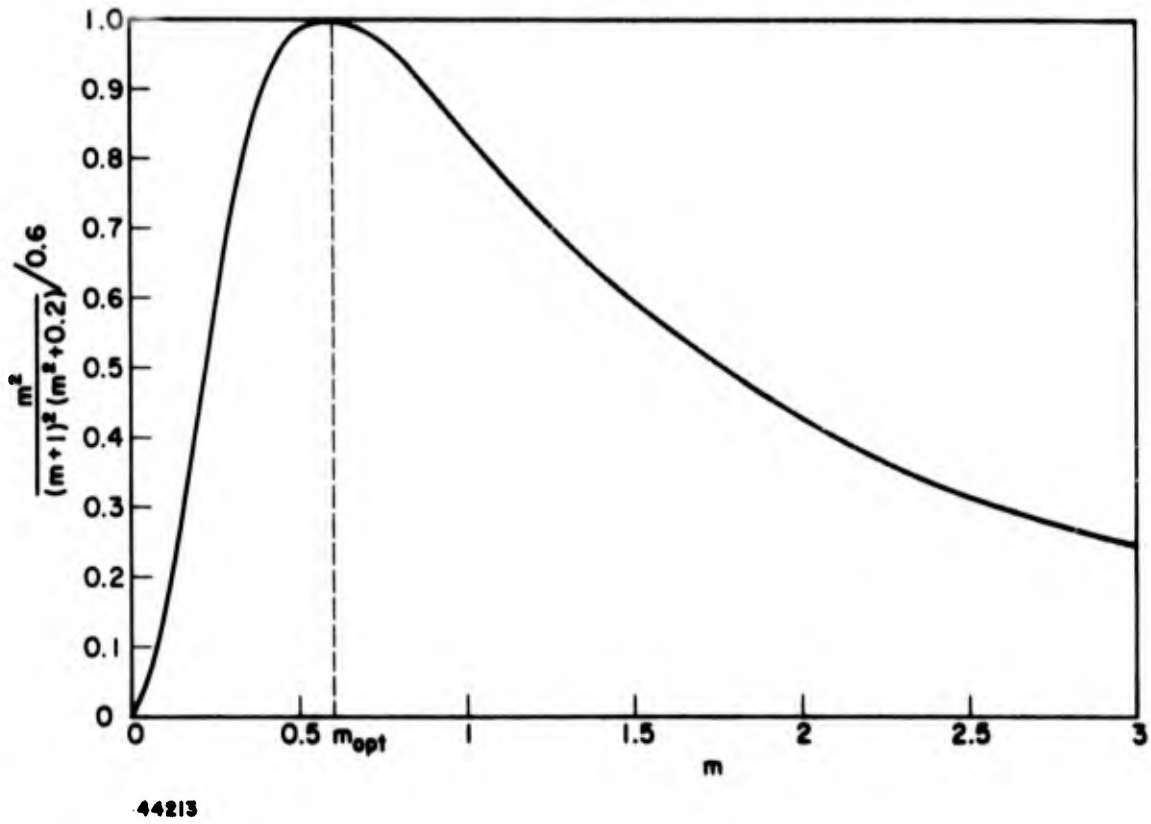


Fig. 30. ILLUSTRATING OPTIMUM CHOICE OF LENS MAGNIFICATION.

gives $\Phi_I\big|_{minpt} = 2.2 \times 10^{13}$ photons/cm^2 sec. At $\lambda = 0.55\mu$, this corresponds to an incident illuminance of 0.5 ft-candle. These figures are seen to be more than four orders of magnitude higher than those calculated in Chapter III using direct illumination upon an ideal charge-storage photodiode. The difference is due to attenuation by the lens and paper, and the nonideal low-level capability of the phototransistor.

A number of second-order effects, such as junction sidewall capacitance, were neglected in this analysis. An important consideration when the base-collector junction is comparable in area to the emitter junction is that the emitter metallization "shadow" effectively reduces the photodiode area. This causes the curve of Fig. 30 to drop off more rapidly as m is reduced, but does not affect the optimum point as long as the letter element area is much larger than the emitter area.

To summarize: The presence of the emitter capacitance was determined to limit phototransistor performance if the collector-base photodiode is too small. Because of the presence of a lens, the photocurrent

approaches a constant value at large photodiode areas, while the photodiode capacitance is directly proportional to area. Therefore, reduced photocurrent-to-capacitance ratio bounds large area phototransistor performance. The optimum lens magnification was calculated and found to be equal to the cube root of the ratio of emitter capacitance to photodiode capacitance at unity magnification. For the reading aid, this ratio (and therefore the optimum m) will be less than unity. The optimum is fairly broad, as illustrated by Fig. 30.

C. Optimum MOS Source Photodiode Area

The source photodiode-MOS switch combination can also be optimized with respect to photosensing area, the analysis being quite similar to that presented above for the phototransistor. The configuration shown in Fig. 18 will be considered. Following the results of Chapter IV, it is supposed that capacitive gate-pulse feedthrough has been suppressed by an integrator so that the most important sources of uncertainty arise from the charge pumping effect and dc generation current. As in the case of phototransistor current gain, variation of these quantities among elements of the array is the major concern, since average spatial noise is readily canceled and compensation of individual elements is not feasible.

In performing a worst-case analysis, the required condition for determining whether an element is lighted or dark is best expressed in terms of charge. The lowest possible signal from a lighted element is its photogenerated charge minus the peak noise charge. This must exceed the highest signal from a dark ($\rho_o \cong 0$) element, which is simply the peak noise charge. If the photogenerated charge exceeds the worst-case peak-to-peak variation in spatial noise charge, then this condition is true, and unambiguous thresholding is always possible. The condition is written:

$$Q_P\Big|_{min} = \epsilon Q_G + \mu Q_T \tag{5.12}$$

where

$Q_P\Big|_{min}$ = minimum usable photogenerated charge

Q_G = thermally generated charge

Q_T = trapped charge from pumping effect

ϵQ_G = worst-case peak-to-peak variation in generated charge

μQ_T = worst-case peak-to-peak variation in trapped charge

Using Eqs. (2.2), (4.7), (4.8), and (5.3), Eq. (5.12) becomes

$$\frac{q\eta\rho_o(1-\rho_p)tT_i}{4F_{eq}^2}\frac{A_p}{\left(1+\sqrt{A_p/A_o}\right)^2}\Phi_I\Big|_{minmos} = \epsilon\Gamma A_p T_i + \mu q N_{ST} A_g$$

or

$$\frac{q\eta\rho_o(1-\rho_p)tT_i}{4F_{eq}^2}\frac{A_p}{\left(1+\sqrt{A_p/A_o}\right)^2\left(\epsilon\Gamma T_i A_p + \mu q N_{ST} A_g\right)}\Phi_I\Big|_{minmos} = 1 \qquad (5.13)$$

Substituting $A_p = m^2 A_o$,

$$\frac{q\eta\rho_o(1-\rho_p)t}{4F_{eq}^2\epsilon\Gamma}\left[\frac{m^2}{(m+1)^2\left(m^2+\frac{\mu q N_{ST} A_g}{\epsilon\Gamma T_i A_o}\right)}\right]\Phi_I\Big|_{minmos} = 1 \qquad (5.14)$$

Defining $\gamma_{mos} = \mu q N_{ST} A_g / \epsilon\Gamma T_i A_o$ = ratio of variation in trapped charge to variation of dark leakage charge at unity magnification, gives

$$\frac{q\eta\rho_o(1-\rho_p)t}{4F_{eq}^2\epsilon\Gamma}\left[\frac{m^2}{(m+1)^2(m^2+\gamma_{mos})}\right]\Phi_I\Big|_{minmos} = 1 \qquad (5.15)$$

Equation (5.15) is nearly identical to Eq. (5.9), and clearly has the same optimum magnification:

$$m_{opt} = \gamma_{mos}^{1/3} \qquad (5.16)$$

which gives the minimum usable flux density

$$\Phi_I\Big|_{minmos} = \frac{4F_{eq}^2 \epsilon \Gamma}{q n \rho_o (1 - \rho_p) t} \left(1 + \gamma_{mos}^{1/3}\right) \qquad m = m_{opt} \tag{5.17}$$

The physical basis for the optimum is that if photodiode area is too small, photogenerated charge becomes small relative to pumped charge, since pumped charge is independent of photodiode area. This causes the signal-to-noise ratio to vanish as A_p goes to zero. On the other hand, as A_p becomes large, the photogenerated charge becomes constant [Eq. (5.3)], but charge due to dark leakage current increases linearly with area. Therefore SNR also vanishes as A_p goes to infinity. An optimum A_p (and m) therefore exists, the limiting factors being variation in pumped charge at small photodiode areas, and variation of leakage current charge with large photodiode areas.

In order to compute the optimum m and A_p, the values for worst-case peak-to-peak leakage and pumped charge variation must be assumed. These are process-dependent quantities that need to be minimized during device fabrication. Since no integrated arrays for the reading aid are yet available, values for ϵ and μ must be taken based on educated guesswork. Measurements on discrete units indicate that the percent leakage variation will be much greater than the percent variation in pumped charge. A spread in dark current of at least two to one is typically encountered, even in integrated arrays [47], so ϵ will be assumed equal to unity. The pumped charge variation will be taken to be 20 percent of this: $\mu = 0.2$. The MOS gate geometry will be chosen as short as possible, and wide enough for sufficiently high switch "on" conductance. A 0.5 by 4 mil gate will be taken, giving $A_g = 1.25 \times 10^{-5}$ cm^2. Thus the following numbers:

$\epsilon = 1$ $\qquad$ $A_g = 1.25 \times 10^{-5}$ cm^2

$\mu = 0.2$ $\qquad$ $A_o = 3.1 \times 10^{-4}$ cm^2

$N_{ST} = 7 \times 10^{10}$ cm^{-2} $\qquad$ $\Gamma = 10^{-9}$ Acm^{-2}

plus those taken for the phototransistor computation above are used to give

$$\gamma_{mos} = 5.4$$

$$m_{opt} = 1.75$$

$$\Phi_I\Big|_{minmos} = 1.8 \times 10^{12} \text{ photons/sec cm}^2$$

The best magnification is seen to be greater than unity. The minimum usable flux density is about an order of magnitude lower than that computed for the phototransistor at its optimum magnification.

Thus an optimum MOS transistor source diode geometry for most favorable low-light-level performance was found, for reasons analogous to the phototransistor treated in the preceding section. Performance is limited by spatial noise due to variation in dark current and MOS pumped charge from element to element. The optimum lens magnification was found to be equal to the cube root of the ratio of the peak-to-peak variation in pumped charge to the charge liberated by dark current when the photodiode area and letter area imaged are equal. This ratio, and thus m_{opt}, are usually greater than unity. The optimum is fairly broad, being governed by the same equation giving the curve of Fig. 30. A computation with representative numbers gave the low-light-level performance edge to the MOS structure by approximately a factor of 10.

D. Comparison of Bipolar and MOS Switch Circuits

The computations of the previous two sections showed that the optimized MOS array is able to operate at about an order of magnitude lower level of illumination than the optimized phototransistor array. The two schemes can be compared directly by taking the ratio of Eq. (5.11) to Eq. (5.17):

$$\frac{\Phi_I\Big|_{minpt}}{\Phi_I\Big|_{minmos}} = \frac{\alpha \frac{kT}{q} C_{pa}}{\epsilon \Gamma T_i} \left(\frac{1 + \gamma_{pt}^{1/3}}{1 + \gamma_{mos}^{1/3}} \right)^3 \qquad (5.18)$$

where

$$\gamma_{pt} = C_{ea}A_e/C_{pa}A_o = \frac{\text{emitter capacitance}}{\text{photodiode capacitance at } m = 1}$$

$$\gamma_{mos} = \frac{\mu q N_{ST} A_g}{\epsilon \Gamma T_i A_o} = \frac{\text{p-p variation in pumped charge}}{\text{p-p variation in leakage charge at } m = 1}$$

Substitution of the numbers assumed previously gives a value of 12.4 for the ratio of Eq. (5.18). This equation, as described in Section B, is only valid if the phototransistor is not limited by leakage at low levels. This means that the photodiode voltage developed by the dark leakage during the integration time must be much less than $\alpha(kT/q)$:

$$\frac{\Gamma T_i A_p}{C_{pa} A_p} \ll \alpha \frac{kT}{q} \tag{5.19}$$

or

$$\alpha \frac{\frac{kT}{q} C_{pa}}{\Gamma T_i} \gg 1$$

Equation (5.19) points out that the coefficient of Eq. (5.18) is much greater than unity. The gamma factor for the phototransistor is typically less than the MOS gamma, but not enough to make Eq. (5.18) less than unity. Thus, when the two schemes are compared, with each using its optimum magnification, the MOS switch scheme exhibits a lower minimum usable level of illumination.

It is instructive to consider the MOS and bipolar schemes on the basis of a lens magnification constraint. This means that the comparison is taken with equal photodiode areas, rather than the respective optimum areas as above. When this is true, Eqs. (5.9) and (5.15) give:

$$\frac{\Phi_I \big|_{minpt}}{\Phi_I \big|_{minmos}} = \frac{\alpha \frac{kT}{q} C_{pa}}{\epsilon \Gamma T_i} \left(\frac{m^2 + \gamma_{pt}}{m^2 + \gamma_{mos}} \right) \tag{5.20}$$

This relationship is plotted in Fig. 31, using the same parameter values presumed above. The ratio is seen to be always greater then unity, and to increase with increasing m. The relative advantage of the MOS structure is much less at low values of m than at larger magnifications.

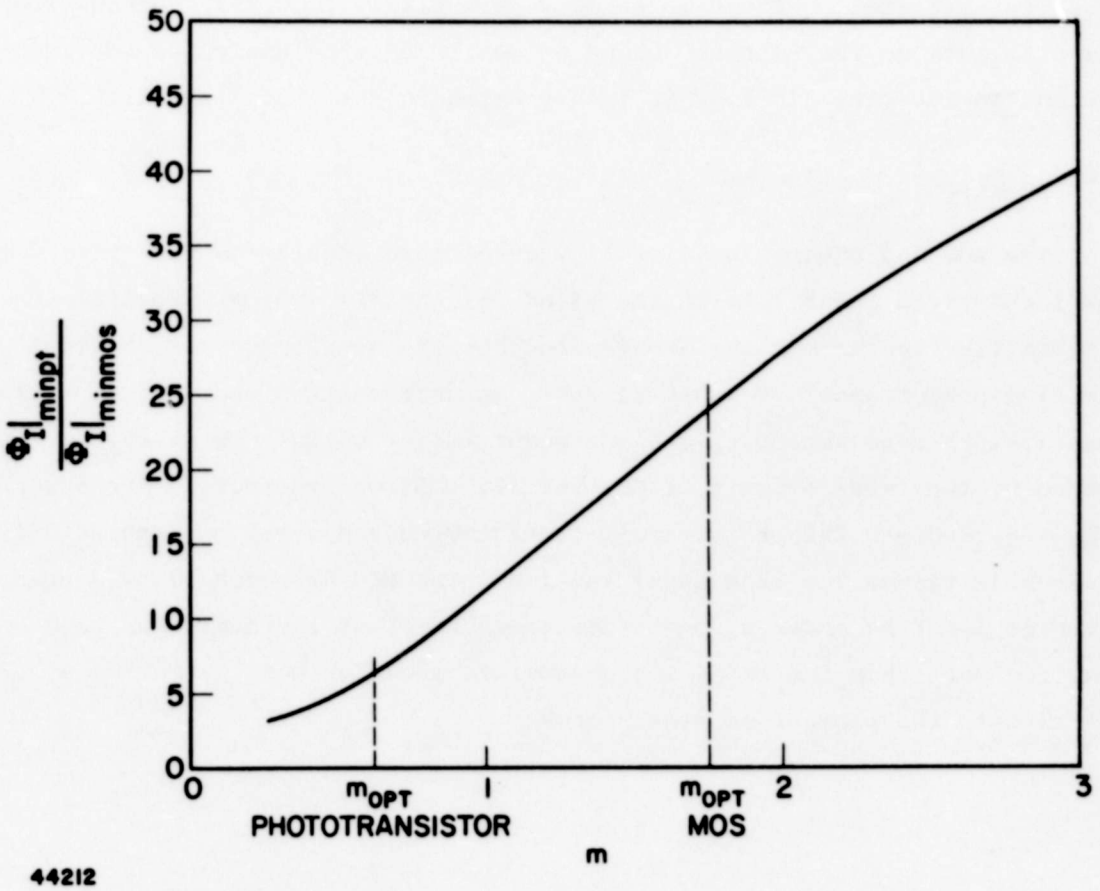


Fig. 31. RATIO OF MINIMUM PHOTOTRANSISTOR TO MINIMUM MOS FLUX DENSITY VS LENS MAGNIFICATION.

This result is not unreasonable, since the optimum phototransistor magnification (0.6) is less than the optimum MOS magnification (1.75). The underlying physical explanation comes from the different figures of merit for the two schemes. Delivered charge [Eq. (5.12)] is most important for

the MOS switch, whereas ΔV_p [Eq. (5.5)] is the crucial figure of merit for the phototransistor. Since ΔV_p depends on the ratio of charge to capacitance rather than magnitude of charge, it can be achieved at much lower photodiode area. This is why the phototransistor array is nearly as good as the MOS array as regards low-level performance when photodiode area (m) is small. When m becomes very small (< 0.25), second-order effects, such as the emitter shadowing mentioned previously, become important so the curve in Fig. 31 is not extended into this region.

E. Summary

The MOS and phototransistor structures were considered with regard to low-light-level capability in the blind reading aid system. Spatial nonuniformities in the sensing array were shown to be the most significant in limiting performance. Because of these nonuniformities and optical system losses, much more ambient light was required for useful operation than was needed by the ideal circuit of Chapter II. Optimum photodiode areas were computed for both the phototransistor and MOS cases which gave physically reasonable values for lens magnification. The MOS approach allowed operation at about an order of magnitude lower level of incident flux, and required more than ten times the photodiode area for best performance, relative to the phototransistor scheme.

Chapter VI

CONCLUSION

The requirement of an opto-mechanical transducer for a blind reading aid may be conveniently satisfied using all-solid-state techniques. A mosaic of junction photodetectors is able to perform the requisite imaging function. The charge-storage technique is universally employed as the electrical mode of operation of such scanned image arrays. The low-light level properties of photodiode charge-storage circuits suitable for array applications were the subject of this study. The discussion was limited to bipolar and MOS silicon monolithic technologies. These device technologies are presently by far the most advanced and thus are, a fortiori, best suited for fabrication of photodiode arrays.

The properties of the basic photodiode charge-storage circuit were considered in Chapter II. An ideal switching element was assumed, and attention was particularly directed toward the noise transmission properties of the circuit and the relative magnitudes of the various sources of noise. Because of the lowpass nature of the circuit, the major contaminating signals were found to be dc dark current and $1/f$ noise. The charge-storage circuit therefore operates within an unfavorable portion of the frequency spectrum with respect to ultimate noise performance, since bandpass filtering would remove the low-frequency noise sources so that only shot noise remained. Nevertheless, the ideal photodiode charge-storage circuit is difficult to realize in practice because of imperfections in the switching element.

The analysis was extended to include a nonideal switching element in Chapters III and IV. Chapter III considers the low-level limitations encountered where signal readout is taken through a junction diode, and Chapter IV deals with the MOS switch case. Chapter V compares the practical phototransistor and MOS structures described in the two preceding chapters with regard to the reading aid system application. Monolithic photodetector arrays are envisioned for this application, although the analysis is also applicable to arrays of discrete devices.

The salient results of this work are:

1. The phototransistor charge-storage circuit at low light levels is analyzed using a simple model. The emitter-base diode is shown to govern the charge readout at low levels, causing very nonlinear circuit behavior. Sluggish transient response, increased sensitivity of output to transistor current gain, and nonlinear transfer characteristic are all demonstrated to upset the phototransistor low-light-level behavior. These factors are found to degrade performance more severely than junction dark current. The parameters are all treated quantitatively, with the results presented in graphical form. Good experimental agreement with the analytical results is shown.

2. The low-level performance-limiting factors relevant to the photodiode-MOS structure in the charge-storage mode are identified. They are shown to be capacitive feedthrough of the gate pulse and an unusual charge pumping effect. A charge integration technique is proposed in order to eliminate the effect of the feedthrough charge. A first-order theory is presented to explain the charge pumping phenomenon, and is supported by experimental data.

3. Phototransistor and MOS arrays are compared with respect to low-light-level performance for the blind reading aid application. Spatial nonuniformities in the array are found to limit performance most severely. Variations in current gain among elements is most troublesome in the phototransistor array, while variations in pumped charge and leakage charge limit the MOS array. When the effect of a lens is included, optimum areas are found for the photosensing elements. Design formulas for these optima are given. The MOS array is found to provide the best low-light-level performance of the two schemes, although requiring a relatively larger photosensing area to do so.

The above results presuppose the availability of photosensing arrays of junction photodiodes having quite low leakage currents and good element-to-element uniformity. These arrays are possible using selected discrete devices, which is the technique used heretofore in the reading aid. A monolithic array is much more desirable, and a program has been

initiated to fabricate such arrays at Stanford University. Their availability will greatly improve the present reading aid hardware, and in addition firming up the various assumptions of this work. Other suggestions for further work are:

1. A systems comparison of bipolar and MOS technology for the reading aid array is desirable. Although the MOS array appears to promise better low-light-level performance, it requires more-complicated processing and scanning circuitry because of the necessity for charge integration. On the other hand, scan generation is easily accomplished using MOS technology. This leads to the possibility of integrating the scanning circuitry on the chip with the photosensing array [8]. Other systems tradeoffs as well as mosaic fabrication questions could be enumerated. The optimum technology (or perhaps a hybrid of the two) to be used for the reading aid system is thus not at all clear at the present time.

2. A better understanding of the basic physics of the charge pumping phenomenon described in Chapter IV is clearly of interest. More-quantitative experimental correlation of surface-state density and pumped current is needed. The implications of the phenomenon both as a possible technique for studying the physics of semiconductor surfaces and with respect to its importance in practical (nonphotosensing) circuitry are worthy of further study.

3. Measurements of the fundamental low-frequency noise properties of planar photodiodes to back up the analysis in Chapter II are of interest. The magnitude of the $1/f$ noise component in particular needs to be determined. Use of charge storage as a noise measurement technique is an interesting possibility. Determination of the fundamental properties of the photodiode as a detector of radiation [23] also requires these noise measurements.

4. The use of the basic charge-storage circuit (Fig. 2a), with no reverse bias on the photodiode, to achieve a logarithmic response to light is feasible. This would enable wide dynamic response without the necessity of automatic gain control in the reading aid. The circuit and systems consequences of this idea warrant further study.

REFERENCES

1. J. G. Linvill and J. C. Bliss, "A direct-translation reading aid for the blind," Proc. IEEE, 54, pp. 40-51; Jan 1966.

2. J. G. Linvill, "Generation of tactile facsimiles for blind reading," presented at the 1967 National Telemetering Conference, May 1967, San Francisco, Calif.

3. R. C. Joy, "Charge storage mode operation of phototransistors in a reading aid," Rept. SEL-68-019 TR No. 4825-1, Stanford Electronics Laboratories, Stanford, Calif.; Mar 1968.

4. V. K. Zworykin, "The iconoscope - a modern version of the electric eye," Proc. IRE, 22, pp. 16-32; Jan 1934.

5. G. P. Weckler and R. H. Dyck, "Integrated arrays of silicon photodetectors for image sensing," presented at WESCON, paper 13/2, San Francisco, Calif.; Aug 1967.

6. M. A. Schuster and G. Strull, "A monolithic mosaic of photosensors for solid-state imaging applications," IEEE Trans. on Electron Devices, ED-13, pp. 907-912; Dec 1966.

7. P. K. Weimer et al, "A self-scanned solid-state image sensor," Proc. IEEE, 55, pp. 1591-1602; Sep 1967.

8. P. J. W. Noble, "Light sensitive arrays based upon photodiodes combined with MOS devices," IEEE Integrated Circuits Conference, Eastbourne, England; 2-4 May 1967.

9. W. H. Crowell et al, "An electron beam-accessed, image-sensing, silicon-diode array with visible response," 1967 Intern. Solid-State Circuits Conference Digest of Technical Papers, 10, pp. 128-129; Feb 1967.

10. G. P. Weckler, "Operation of p-n junction photodetectors in a photon flux integrating mode," IEEE J. Solid-State Circuits, SC-2, pp. 65-73; Sep 1967.

11. G. P. Weckler, "Charge storage lights the way for solid-state image sensors," Electronics, 40, pp. 75-78; 1 May 1967.

12. A. Rapoport, Operational Philosophy, John Wiley & Sons, Inc., New York, 1965; p. 76.

13. A. Rose, P. K. Weimer, and H. B. Law, "The image orthicon - a sensitive television pickup tube," Proc. IRE, 34, pp. 424-432; Jul 1946.

14. P. K. Weimer, S. V. Forgue, and R. R. Goodrich, "The vidicon - a photoconductive television camera tube," RCA Review, 12, pp. 306-313; Sep 1951.

15. F. W. Reynolds, "Solid-state light sensitive storage device," U.S. Patent #3,011,089; 28 Nov 1961.

16. P. H. Wendland, "A charge storage vidicon camera tube," IEEE Trans. on Electron Devices, ED-14, pp. 285-291; Jun 1967.

17. A. S. Grove, Physics and Technology of Semiconductor Devices, John Wiley & Sons, Inc., New York, 1967.

18. I. Wunderman, "Characteristics of photon-coupled systems," Rept. SU-SEL-64-016 TR No. 4814-1, Stanford Electronics Laboratories, Stanford, Calif.; Apr 1964.

19. H. W. Ruegg, "Avalanche multiplication as a gain mechanism in photodiodes," Rept. SU-SEL-66-008 Tr No. 4820-2, Stanford Electronics Laboratories, Stanford, Calif.; Mar 1966.

20. R. Clark Jones, "Quantum efficiency of detectors for visible and infrared radiation," Advances in Electronics and Electron Physics, 11, pp. 87-183; 1959.

21. P. A. Gary, "Modeling and optimization of a silicon photosensor for a reading aid," Rept. SU-SEL-67-040 TR No. 4822-1, Stanford Electronics Laboratories, Stanford, Calif.; May 1967.

22. P. A. Gary and J. G. Linvill, "A planar silicon photosensor with an optimal spectral response for detecting printed material," IEEE Trans. on Electron Devices, ED-15, pp. 30-39; Jan 1968.

23. R. Clark Jones, "Phenomenological description of the response and detecting ability of radiation detectors," Proc. IRE, 47, pp. 1495-1502; Sep 1959.

24. M. J. O. Strutt, Semiconductor Devices, vol. 1, Academic Press, New York, 1966; p. 275.

25. C. T. Sah, R. N. Noyce, and W. Shockley, "Carrier generation and recombination in p-n junctions and p-n junction characteristics," Proc. IRE, 45, pp. 1228-1243; Sep 1957.

26. L. Scott and M. J. O. Strutt, "Spontaneous fluctuations in the leakage current due to charge generation and recombination in semiconductor diodes," Solid State Electronics, 9, pp. 1067-1073; Nov-Dec 1966.

27. U. F. Gianola, "Photovoltaic noise in silicon broad area p-n junctions," J. Appl. Phys., 27, pp. 51-54; Jan 1956.

28. T. E. Firle and H. Winston, "Noise measurements in semiconductors at very low frequencies," J. Appl. Phys., 26, pp. 716-725; Jun 1955.

29. G. T. Daughters II, "Noise behavior of the 1N3734 photodiode, and 2N986 and 2N2452 phototransistors," Fairchild Semiconductor Application Note APP-46; 1962.

30. N. Abramson and J. Farison, "On statistical communication theory," Rept. SEL-62-078 TR No. 2005-1, Stanford Electronics Laboratories, Stanford, Calif.; Aug 1962; p. 23.

31. J. R. Ragazzini and G. F. Franklin, Sampled-Data Control Systems, McGraw-Hill Book Company, 1958, New York.

32. K. W. Gardiner, Stanford Research Institute, personal communication.

33. M. Schwartz, Information Transmission, Modulation, and Noise, McGraw-Hill Book Company, New York, 1959; p. 274.

34. J. M. Pettit and M. M. McWhorter, Electronic Amplifier Circuits, McGraw-Hill Book Company, New York, 1961; p. 288.

35. H. E. Murphy and L. J. Kabell, "An integrating digital light-meter," IEEE J. Solid-State Circuits, SC-1, pp. 4-7; Sep 1966.

36. IES Lighting Handbook, 3rd Ed., Illuminating Engineering Society, New York, 1959; pp. 3-6.

37. H. A. Sommers, Jr., "Response of photoconducting imaging devices with floating electrodes," J. Appl. Phys., 34, pp. 2923-2934; Oct 1963.

38. R. M. Warner, Jr. and I. N. Fordemwalt, eds. Integrated Circuits, McGraw-Hill Book Company, New York, 1965; p. 90.

39. G. P. Weckler, "A silicon photodevice to operate in a photon flux integration mode," presented at the Intern. Electron Devices Meeting, Washington, D.C.; Oct 1965.

40. H. F. Storm, "Field-effect transistor (FET) bibliography," IEEE Trans. on Electron Devices, ED-14, pp. 710-717; Oct 1967.

41. E. S. Schlegel, "A bibliography of metal-insulator-semiconductor studies," IEEE Trans. on Electron Devices, ED-14, pp. 728-749; Nov 1967.

42. F. P. Heiman, "On the determination of minority carrier lifetime from the transient response of an MOS capacitor," IEEE Trans. on Electron Devices, ED-14, pp. 781-784; Nov 1967.

43. L. L. Rosier, "Surface state and surface recombination velocity characteristics of S_i-S_iO_2 interfaces," IEEE Trans. on Electron Devices, ED-13, pp. 260-267; Feb 1966.

44. B. E. Deal et al "Characteristics of the surface-state charge (Q_{ss}) of thermally oxidized silicon," J. Electrochem. Society, 114, pp. 266-274; Mar 1967.

45. A. S. Grove et al, "Investigation of thermally oxidized silicon surfaces using metal-oxide-semiconductor structures," Solid-State Electronics, 8, pp. 145-163; Feb 1965.

46. R. Kingslake, ed. Applied Optics and Optical Engineering, Academic Press, 1965, vol. II; Chapter 5.

47. G. P. Weckler, Fairchild Semiconductor, personal communication.

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13. ABSTRACT

The properties of silicon junction photodetectors have been investigated with the goal of improving low-light-level performance of a reading aid for the blind. This application requires an image-forming mosaic of photodetectors, which may be conveniently fabricated by use of integrated circuit technology. Solid-state imaging is particularly attractive because of the low resolution (100 to 200 elements) needed for the reading-aid system.

Attention is focused upon photodetector operation utilizing the charge-storage technique, because of the usefulness of this method in increasing the signal level in scanned image applications. The signal and noise transmission properties of the basic charge-storage circuit are analyzed, with the assumption of an ideal switching element. The primary contributors to output uncertainty are found to be dark current and its associated 1/f noise because of the lowpass nature of the circuit.

Practical charge-storage circuits, based upon the available bipolar and metal-oxide-semiconductor (MOS) technologies, are studied. Low-light-level performance is determined to be most severely limited by switch imperfections. The low-light-level operation of the charge-storage phototransistor is analyzed in detail. Performance is shown to be increasingly degraded as the light level is reduced due to influence of the emitter-base junction. The use of an MOS switch is considered, and capacitive feedthrough found to be excessive. A charge integration scheme is proposed to circumvent the feedthrough charge, leaving the most significant noise source to be an unusual "charge pumping" effect. The charge pumping phenomenon is studied in detail in order to establish its physical basis.

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ABSTRACT (cont)

When photosensing arrays are investigated, spatial nonuniformities are found to limit low-light-level performance most severely. Optimum photosensing areas are determined for phototransistor and MOS arrays in the reading aid application. Design formulas for these optima are given. The MOS array is found to offer the best low-light-level performance of the two schemes, although requiring a relatively larger photosensing area.