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Research and Development Technical Report
ECOM-0412-F

INVESTIGATION OF HEAT REMOVAL FROM BOTH SIDES OF A TRANSISTOR CHIP EMBODYING BUMP TECHNOLOGY

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CONTRACT NO. DAAB07-67-C-0412

FINAL REPORT
SEPTEMBER 1968

HUGHES AIRCRAFT COMPANY
MICROELECTRONICS LABORATORY
NEWPORT BEACH, CALIFORNIA, 92663

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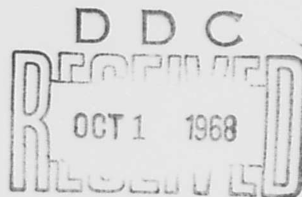

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FINAL REPORT

SEPTEMBER 1968

Contract No. DAAB 07-67-C-0412

Prepared by: H. F. Rueffer

Approved by: R. J. Belardi
Program Manager

Distribution Statement

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HUGHES AIRCRAFT COMPANY
Microelectronics Laboratory
Newport Beach, California 92663.

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H = 1 μS/Div. V = 50 mV/Div

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H = 1 μS/Div. V = 50 mV/Div.

I. PURPOSE:

The objective of this contract is to determine the feasibility of removing heat simultaneously from both the collector and emitter sides of a double diffused transistor chip. Flip chip bump technology will be employed in this investigation to improve the transistor thermal resistance and thermal response.

The basic concept for the accomplishment of this heat removal is the forming of silver contacts on the emitter and base areas and also on the back collector side. The silver contacts or bumps serve as both good electrical and good thermal conductors. The transistor chip is mounted on a header face down and a collector strap is attached to the back side.

The elements which require investigation and development are as follows:

1. Metallurgy:
   a. Silicon ohmic contacts to interconnect metal.
   b. Interconnect metal to bump.
   c. Bump formation.
2. Package:
   a. Design for face down mounting.
   b. Design for back collector contact.
3. Device structure which is sufficiently flexible to conduct experimentation on the metallurgical, electrical and thermal aspects.

II. ABSTRACT

The purpose of this work is to determine the feasibility of removing heat simultaneously from both the collector and emitter sides of a double diffused transistor chip. The work consisted of forming a large silver bump over the emitter and a small bump for base contact on the front side of a power transistor chip. This chip was mounted face down on a modified TO-60 header and a large silver strap was used to contact the collector on the back side. A non-multiple emitter structure mounted as above showed a 40% decrease in thermal resistance over a chip mounted face up in a standard manner. It is concluded that dual sided heat removal is feasible and the 40% improvement is substantial enough to warrant further attention.

III. EXPERIMENTAL:

A. Considerable effort was expended to develop a transistor design which would lend itself to investigating the advantages of heat removal from both sides of the device die.

The mask design which was chosen incorporates four separate device geometry variations which are contained on the same mask set shown in the composite drawing of Figure 1. The four design variations form a matrix as follows:

	Small Emitter Area	Large Emitter Area
Unequal Bump Areas	Geometry A (Fig. 2)	Geometry B (Fig. 3)
Equal Bump Areas	Geometry C (Fig. 4)	Geometry D (Fig. 5)

The three equal bump areas (two emitters and one base) were chosen for compatibility in the bump processing and to provide a tripod mounting to the header.

The unequal bumps were chosen so that development could be carried out on a structure which is more typical of a multiple emitter power transistor where the emitter area is larger than the base contact area.

The small and large emitter area differences were designed so that the relative effect of heat removal from the emitter area could be ascertained.

The top metal is in direct contact with silicon only in the emitter windows, so that by maintaining the base area constant and varying the emitter contact opening a measure of heat removal effectiveness can be established.

A summary of the transistor geometry data for the four design variations is tabulated in Figure 6. In addition, various ratios of interest are shown.

B. A basic outline of the dice fabrication process follows:

1. Material - N^+N (1 - 2 Ω cm 15 - 20 μ thick epi layer)
2. Oxidation
3. Base Mask
4. Base Diffusion
5. Base Enhancement Mask
6. Base Enhancement Diffusion
7. Emitter Mask
8. Emitter Diffusion and Open Emitter Oxide
9. Contact Mask
10. Sputter and Alloy Pt
11. Remove Excess Pt
12. Sputter Ti - Pt
13. Evaporate and Fuze Au - Sb on Back
14. Mask Interconnection
15. Sputter Glass
16. Open Glass
17. Evaporate Cr - Au
18. Mask for Front Bumps
19. Electroform Front Bumps
20. Dip in Sn
21. Dice Wafer
22. Mechanically & Electrically Sort Dice

C. The early lots indicated various problem areas:

1. Device Degradation.
2. Incomplete formation of the platinum silicide.
3. Improper processing sequence for the back side alloying.
4. Back bump too small.
5. Difficulty in mounting to the header.

The device degradation is one of high leakage currents which is attributed to the extra process steps required for the final bump structure. The additional metallization, glassing, and electro-forming operations require critical control of the surface chemistry and insulating layers to prevent device degradation. Although the initial lots exhibited high leakage, the later lots show improvement as better process control is achieved. A significant contribution to high leakage is believed to be the result of a thinning down of the oxide thickness prior to metallization. This was corrected by a new contact opening mask as described in the next paragraph.

The spotty formation of the platinum silicide ohmic contacts was traced to the incomplete removal of oxide prior to the sputtering process. When additional oxide etching was performed prior to sputtering a smooth uniform silicide was achieved. The oxide removal has been done in two steps, one of emitter oxide removal after diffusion, and the other a base contact opening using the base enhancement mask. The emitter oxide removal step consists of merely a dip etching process without a mask, since the emitter oxide is fairly thin and should etch fast due to phosphorus glaze. However, experience has proven the overall oxide thickness is significantly reduced during this dip etching step. Since these two

steps did not allow for controlled oxide window cleaning, a final dip etch was done just prior to placing the slices in the platinum sputtering chamber. This further reduced the overall oxide thickness, contributing to the leakage current problem after metallization over the oxide was completed. A contact mask which will open both emitter and base was fabricated and allowed for complete oxide removal and provided uniform platinum silicide.

The process step of alloying the back side of the wafer with gold-antimony was performed toward the end of the process. This step is required to provide ohmic back contact and form a metallurgical foundation for the bump structure. The approximate 400°C temperature needed to form the alloy was found to be harmful to some of the previously completed metallization processes. This step has been moved to a point directly after the sputtering of platinum.

It was found that the back bump (Figure 7) was offering difficulties in the solder dipping operation and use of a back bump was reconsidered. Upon reconsideration of the merits the back bump was removed from the process. This immediately yielded benefits in three areas, one the reduction of process steps, two the difficulties arising from working both sides of a slice led to improved yields and three the entire metallized back became available for soldering the strap. The third item improved the mechanical strength and aided the heat removal ability.

The mounting of the bumped die to the header still offers some difficulties as concerns a production worthy process. The

variability of the thermal data has been traced to the soldering operation. There are three points at which variability in the soldering step can effect the thermal resistance. They are the die attachment, the strap attachment to the post and to the back of the die. The quantity, voiding and coverage can all effect the uniformity of the solder attachment. General production type tooling techniques could be applied to this problem of uniformity but they are beyond the scope of this contract. The units supplied on this contract were built basically using hand techniques and hence the variability of the thermal data.

The bump height difference can be graphically seen in Figures 8 and 9. Figure 8 shows the equal bump heights of the "C" geometry while Figure 9 shows the unequal height of the "A" geometry. The height difference is due to the tin dipping operation wherein the amount of solder is directly proportional to the bump size. Using the tin dipping approach the bumps on the same surface must be equal size which leads to geometries which are not optimum for the transistor structure. Another method for tinning the silver bumps would be plating, the use of which would allow unequal bump sizes and hence more ideal transistor designs. The tin plating methods have been tried and it was found that the plating produced surfaces which were uniform but the tin was not adequate for soldering. All geometries were tin dipped and the attachment of unequal bumps was successfully done as described below.

Measurements on strapped and non strapped units mounted using the bent copper strap shown in Figures 28 and 29 indicated that the strap was not effective in conducting heat away from the die. Calculations then bore out the fact when the calculated thermal resistance of the strap was found to be high.

The strap was changed to a flat silver bar 80 mils wide and 8 mils thick as shown in Figure 31.

The process used for mounting the die and strap is as follows:

1. Header is placed in variable heat fixture at ≅ 150°C.
2. The die is correctly positioned face down on the header using a vacuum quill mounted in an X-Y-Z motion machine.
3. When the die is in proper position a small amount of flux is applied and the temperature raised to the melting point of the solder ≅ 215°C.
4. The strap is then placed over header pin and aligned with back of die.
5. The strap is soldered at the pin.
6. The strap is soldered at back of chip.
7. The unit is then cleaned.

Figures 26 - 29 show the header in various stages of die and strap mounting.

D. The chips have been mounted in the following configurations:

   1. Face up, collector eutectic bonded, emitter and base wires thermo compression bonded.
   2. Face down soldered, no collector strap. Wire bonded to collector.
   3. Face down soldered, with strap soldered to collector.

   This matrix should allow for the determination of the overall effects and also the contribution of each of the separate elements.

E. Figures 10 - 25 show the completed die, cross sections of the base and emitter, cross sections of base contact, and cross

sections of emitter area.

F. The various metals used in the structure and the reasons for their use follows:

1. Platinum-silicide is used to form both electrical ohmic contact and form a secure mechanical base for the additional metals. The destruction temperature of this metallizing is at least 75° C higher than aluminum.

2. Titanium-Platinum is used for the interconnections because it can be sputtered nicely and also forms a good attachment both to the oxide and the silicide. The platinum is used to protect the titanium from oxidation.

3. Gold is used for its electrical conductivity on top of the Ti - Pt interconnection base.

4. Chromium gold is used on top of the sputtered glass to form the base for the bump structure.

5. Silver is the metal from which the bump is formed and is used for its fine electrical and thermal properties.

6. Silver-tin-solder aids in reflow mounting and its ductility allows for bump height differences.

The approximate thickness of these metals are listed below.

Metal	Thickness
Pt - Si	500 Å
Ti - Pt	1500 Å
Au	3000 Å
Cr - Au	3500 Å
Ag	1 mil
Ag - Sn	1 mil

G. The use of sputtered glass offers the following advantages:

1. A high degree of mechanical and moisture protection.
2. A good insulator on which to build the large emitter bumps which overlay the many base contacts.
3. The sputtered glass is fairly rugged and offers an acceptable thermal expansion match to silicon.
4. The sputtering process offers a production-worthy method of applying controlled uniform glass layers.

H. The computation of the heat removal from both sides of the structures would be a difficult problem, but by choosing worst cases and assuming simple structures, the problem can be calculated.

The assumptions for heat removal from the top side are:

1. Heat is generated at the emitter shadow on the base junction.
2. Heat flow will transfer from this silicon area upward through a silver cube defined by each emitter area.

3. No allowance is made for spreading of the heat from each little silver cube through the large silver bump which connects all the individual cubes.

The assumption for heat removal from the back side is the heat spreading from the emitter shadow on the base junction through the silicon to the back contact.

The equations used are as follows:

$$R_T = \frac{L}{KA} \qquad\qquad R_T = \frac{1}{2\pi K}\left(\frac{1}{R_0} - \frac{1}{R_T}\right)$$

R_T	=	thermal resistance C°/watt
L	=	length mils
A	=	square mils
K	=	thermal conductivity watts/cm-C°
R_0	=	radius of source of heat
R_T	=	thickness of sample

1 cm = 3.9×10^2 mils

Silver K = 4.0 watts/cm-C° at T = 100° C
Silicon K = 1.0 watts/cm-C° at T = 100° C

R_T thru silver cube

$$R_T = \frac{1 \times 3.9 \times 10^2}{2 \times 2 \times 4.0} = 24.6 \text{ C°/watt}$$

R_T thru silicon from base junction

$$R_T = \frac{3 \times 10^{-4} (3.9 \times 10^2)^2}{(2)^2 \times 1.0} = 11.2 C°/\text{watt}$$

The total thermal resistance through top side is

Total R = 24.6 + 11.2 = 35.8 C°/watt

R_T spreading from the base to the back is as follows:

$$R_T = \frac{.159 \times 3.9 \times 10^2}{1.0} \left(\frac{1}{1.0} - \frac{1}{6.0} \right)$$

$$R_T = 52 \ C°/\text{watt}$$

This indicates that in the worst case allowing for no top side spreading in the large emitter bump and assuming a one mil thick bump, the removal from top side is nearly 130%of bottom side. Adding to this the assumption that heat can be removed from top and bottom equally efficiently it can be seen that simultaneous heat removal will result in an increase in thermal efficiency.

I. The following is an attempt to compute the potential frequency and power of the various geometries by comparison with the

2N-3375			
	F_T	=	500 MHz
	P_G	=	4.7 db at 400 MHz
	P_D	≅	10 watts

Base area	400 $(\text{mils})^2$
Emitter area	40 $(\text{mils})^2$
Emitter periphery	300 mils

Taking into account the difference in emitter area and emitter periphery the gain bandwidth products (F_T) of the geometries are:

I	130 MHz
II	13 MHz
III	130 MHz
IV	48 MHz

Using the expression for power gain

$$P_G = \frac{F_T}{8\pi f^2 rb\ Cc}$$

and assuming constant rb' and Cc dependent upon base area the following P_G's are developed

I	2 db at 100 MHz
II	2 db at 10 MHz
III	5 db at 100 MHz
IV	10 db at 10 MHz

The power dissipation should bear relationship to the base area and so the larger units should dissipate 18 watts and the smaller 10 watts in the TO-60 header.

J. Some representative electrical values have been measured on four units (Type IV) and are listed below.

hFE	BV_{CEO}	BV_{CBO}	BV_{EBO}	$V_{CE(sat)}$	$V_{BE(sat)}$
10 ma	1 ma	10 μA	10 μA	I_C = 10 ma	I_B = 1 ma
71	55 V	60 V	8.0 V	.08 V	0.7 V
62	45 V	110 V	8.5 V	.06 V	0.7 V
66	50 V	110 V	8.5 V	.07 V	0.7 V
51	50 V	60 V	8.5 V	.05 V	0.7 V

K. DATA:

1) Sixteen units of the type B variety were mounted in the three configurations described in Section "D" and pictorally shown in Figures 31, 32 and 33. The thermal data is listed in the Appendix and the means and standard deviations were as follows:

Strapped	No Strap	Face Up	
$\overline{X}$ = 7.42	$\overline{X}$ = 9.14	$\overline{X}$ = 11.7	$\overline{X}$ = 11.5
σ = 0.47	σ = 1.99	σ = 2.19	σ = 2.39

The data on the face up units were taken twice to ascertain the precision of the equipment and the reading.

2) Thermal measurements were taken on the A and B type units in the 100 transistors delivered as part of the contract. The two-sigma sports which were caused by the not well controlled soldering mentioned earlier, were removed. The mean and standard deviations are as follows. (Data in Appendix).

TYPE A

Strapped	No Strap	Face Up
$\overline{X}$ = 8.11	$\overline{X}$ = 10.16	$\overline{X}$ = 10.43
σ = 3.08	σ = 2.52	σ = 2.49

TYPE B

Strapped		No Strap	
$\overline{X}$	= 7.40	$\overline{X}$	= 9.68
σ	= 1.58	σ	= 1.15

3) Thermal response measurements were conducted on the three mounting methods. The test method used was one of displaying the collector-base voltage on an oscilloscope. The unit was turned on and then when it was turned off the oscilloscope was triggered and the scope then displayed the cooling versus time of the transistor. Pictures of the scope display are shown in Figures 34, 35, 36. At 70% of initial value the various mounting configurations show the following time values:

Strapped	9 μS
No strap	10 μS
Face-up	10^{+} μS

IV. CONCLUSIONS:

In the investigation into the feasibility of simultaneous heat removal from both sides of a transistor structure the following tasks were undertaken and completed:

1. Design of a power device vehicle.
2. Development of processes needed to exploit the use of silver bumped structures.
3. Modify the header and study the mounting techniques required for two-sided heat removal.
4. Measure and compare the thermal properties of the new structure.

1. The device design which was used as a vehicle around which to study the processes and mounting techniques served very well. The variations of emitter contact area and the two bump structures allowed for studying the thermal properties and the mounting problems. The type A & B structures which are the two bump structures were found to be mountable and since they are the closest to a practical power transistor the major effort of measurement was accomplished using them. The design included a back silver bump which as described was found not to be required, in fact, its elimination provided the benefits mentioned earlier.

2. The process development revolved around the steps required to produce a large silver bump which would make intimate thermal and electrical contact to the emitter area and which was insulated from the remainder of the device structure. The particular combination of structure used here required the mating of three processes to produce the unique device. These elements are the silver bump, the ohmic contact base and the insulating glass layer.

The choice of platinum-silicide was based on the known need for a higher temperature metallurgy. The process was successfully used to produce the required ohmic contact and form a good base for silver bump growth. The higher temperature of this metallurgical system affords additional protection against device catastrophic failure due to local hot spotting.

The use of sputtered high purity glass proved to be a production-worthy method of applying an insulator in those areas requiring this property. The glass and subsequent selective opening to allow contact of the silver bump to the emitter area and also to the base contact worked very nicely. The glass being a poor conductor of heat is considered to be an area for future work which may consider the use of materials such as BeO.

The silver bump structure presented no difficulty when formed over the emitter openings which contained the ohmic foundation of platinum-silicide. The electroforming technique used produced a solid bump with good adherence to the glass insulator while thermally and electrically tying the emitters together. The base contact bump was nicely formed simultaneously with the growth of the main emitter bump. As mentioned earlier the use of a back bump was not required, in fact, benefits of reducing processing and improved mounting accrued when the back bump was not used. Process-wise the growth of back silver bumps was shown to be feasible and though not usable on this structure, the value on future devices may make the additional work worthwhile.

3. The TO-60 type header which had its metallization pads modified to accept the bump structures and the back strap served very

nicely as a package for this study.

The mounting of the die to the header and the subsequent attachment of the back strap to the die and header post still present difficulty. A method of accomplishing this mounting was developed but as mentioned it is basically a hand operation. It was concluded that a tooling development effort could reduce the mounting problems. This effort is beyond the scope of this contract yet appears to be reasonably attainable.

4. The following ratios were formed from the thermal resistance data in Section "K".

Type B (single emitter)

(1) Face down with strap to face up $\frac{7.42}{11.7} = 63\%$

(2) Face down no strap to face up $\frac{9.14}{11.7} = 78\%$

(3) Face down strap to no strap $\frac{7.42}{9.14} = 81\%$

Type A (multiple emitters)

(4) Face down with strap to face up $\frac{8.11}{10.43} = 77\%$

(5) Face down no strap to face up $\frac{10.16}{10.43} = 97\%$

(6) Face down strap to no strap $\frac{8.11}{10.16} = 80\%$

As can be seen from ratio (1) the heat removal from both sides of a non-multiple emitter structure (Type B) is approximately 40% better than back side removal only. This alone shows that the dual sided heat removal is certainly an improvement and

substantial enough to make further work along these lines desirable. The multiple emitter structure (ratio (4)) shows about a 20% improvement which is all due to the back side removal since ratio (5) shows only a 3% improvement. This is due to the small area of silver contact and the presence of the glass layer on the front side. The difference in the available emitter contact area between the type A & B structures is about 4 to 1 (Figure 6 120 mil^2 to 425 mil^2 respectively).

The heat removal ability can be attributed to the back side removal of about 20% and the front side removal of 20% (type B) and 3% (type A). The ratio (3) & (6) of strapped to no strap for each case is 80% which again demonstrates the 20% back side strap heat removal.

Ratio (2) shows a 22% improvement due to front side heat removal and is interesting from the point of view of a completely face down mounted power device. That is a structure containing a collector bump as well as emitter and base bumps for single side mounting offers in addition to the improved attachment at least a 20% gain in thermal efficiency.

The ratio (2) of front to back removal of 78% can be compared with the computed ratio (Section H) of 35.8/52 = 69%. The comparison shows the right order of magnitude and indicates that probably additional improvement is possible.

The thermal response was measured and though the data properly indicates improvement the high thermal mass of the header probably is masking the chip thermal response casting some doubt on the measurement accuracy.

APPENDIX

DATA - °C/W

Type B.

Strap	No Strap	Face Up	
7.6	6.8	12.0	11.0
8.1	7.7	10.8	9.5
7.6	11.8	13.4	13.0
7.0	11.2	8.0	8.2
6.8	8.2	15.0	15.6
		11.0	11.8
$\bar{X}$ = 7.42	$\bar{X}$ = 9.14	$\bar{X}$ = 11.7	11.5
σ = .47	σ = 1.99	σ = 2.19	2.39
σ_{max} = .52	σ_{max} = 2.22	σ_{max} = 2.4	2.61

Type A.

Strap

6.8	5.7	8.1	6.6	6.2
7.4	6.9	7.0	8.4	6.2
6.4	5.2	7.3	10.8	19.0
6.3	7.0	6.4	8.2	16.6
9.3	5.7	11.6	6.5	
7.9	10.0	6.7	6.8	

$\bar{X}$ = 8.11

σ = 3.08

σ_{max} = 3.15

Type A. No Strap

No Strap
7.7
9.0
8.4
11.0
14.7

$\bar{X}$ = 10.16

σ = 2.52

σ_{max} = 2.82

Type A. Face Up

12.8	9.5	14.0	11.2
6.7	9.8	7.0	
10.0	9.8	16.0	
10.4	9.6	8.8	

$\bar{X}$ = 10.43

σ = 2.49

σ_{max} = 2.59

APPENDIX (continued)

DATA - °C/W

Type B.

Strap

8.4	11.6	5.8	6.8
7.0	6.4	8.4	
6.4	8.8	5.9	
6.6	6.7		

$\overline{X}$ = 7.40

σ = 1.58

σ_{max} = 1.65

Type B. No Strap

10.6
7.9
10.8
9.4

$\overline{X}$ = 9.68

σ = 1.15

σ_{max} = 1.33

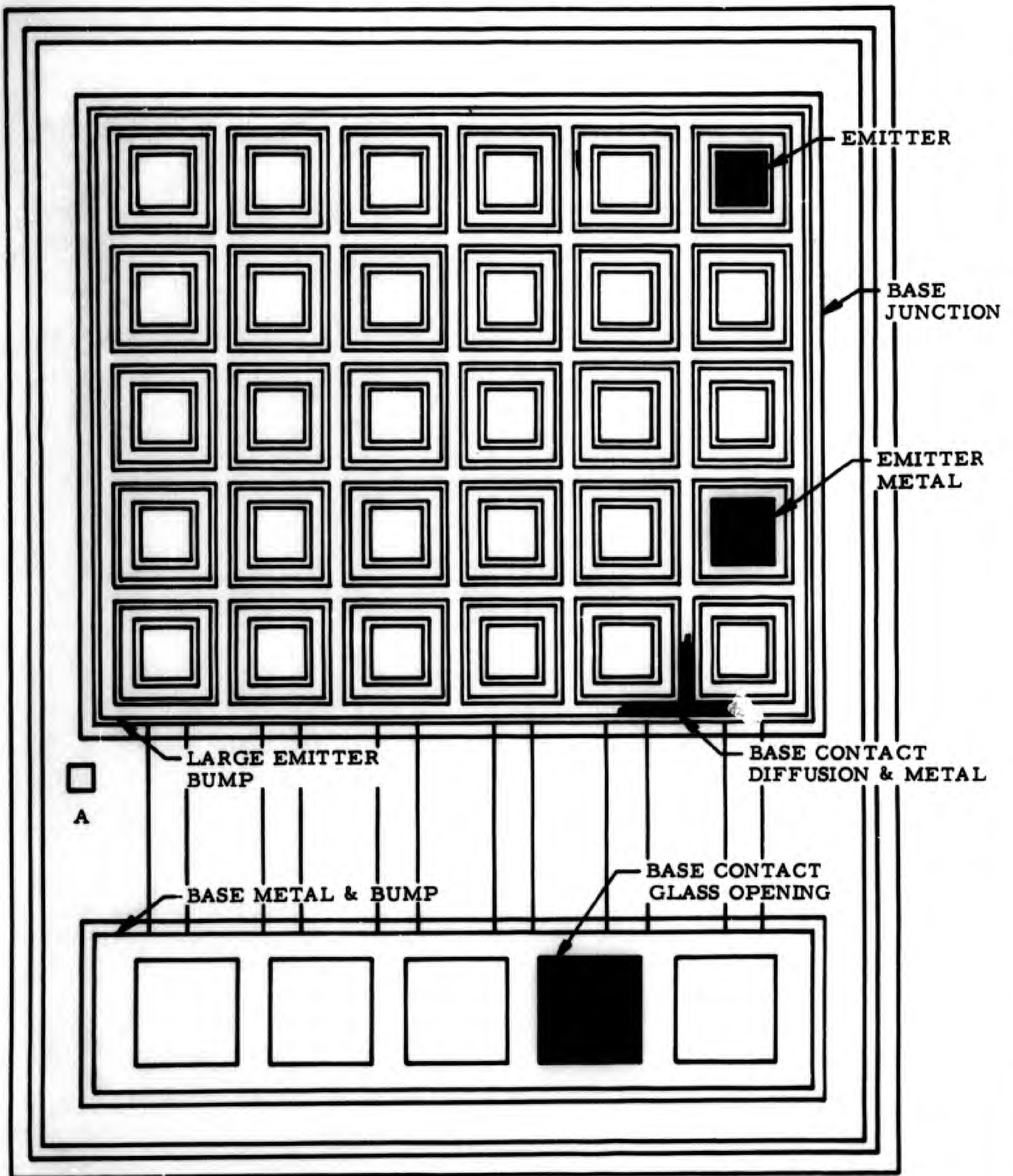
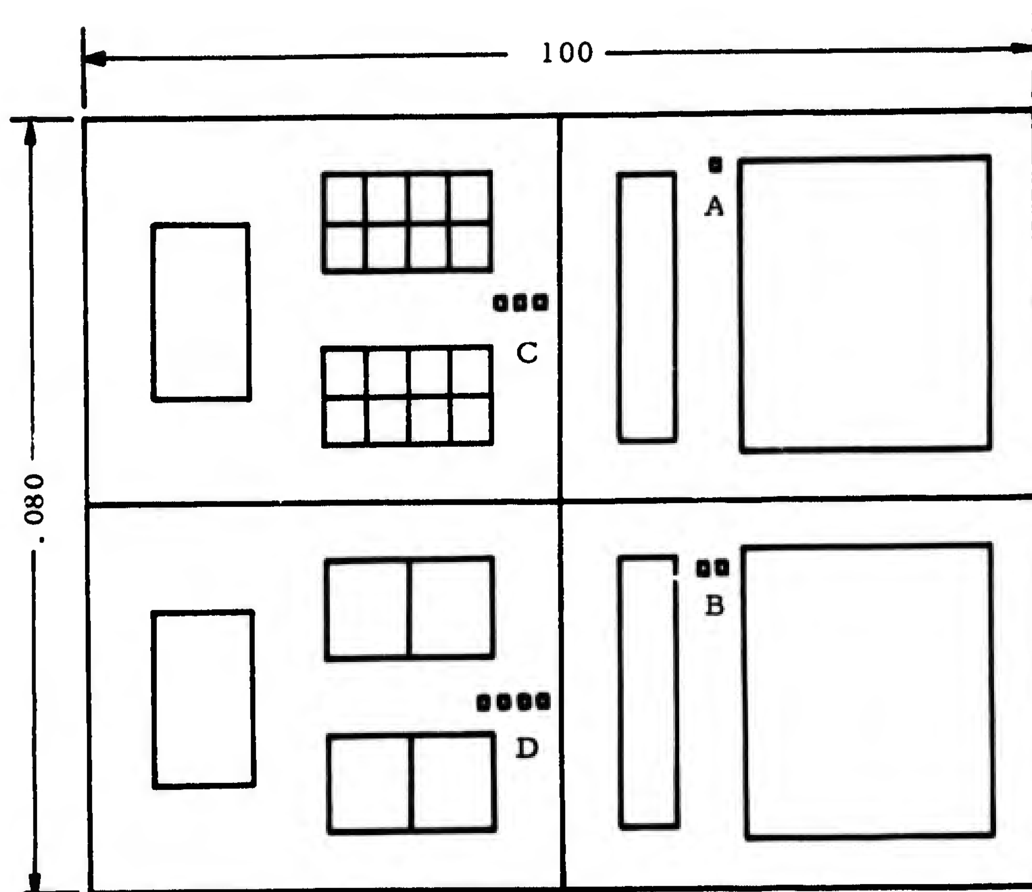


FIGURE 1.



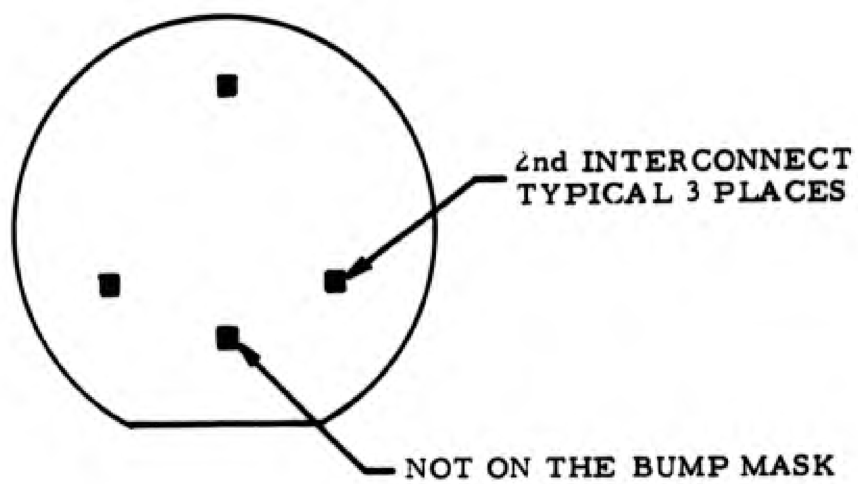


FIGURE 2.

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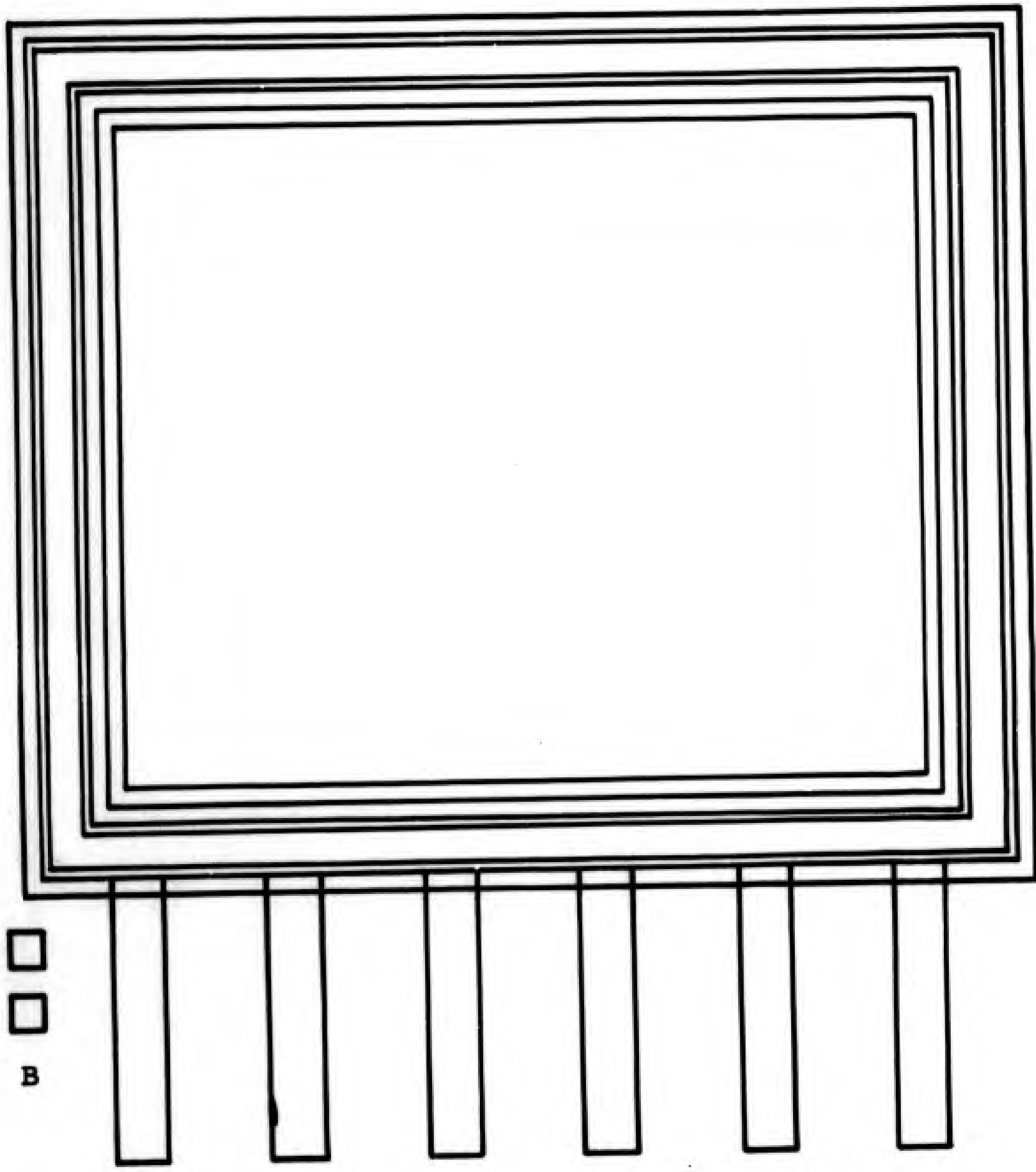
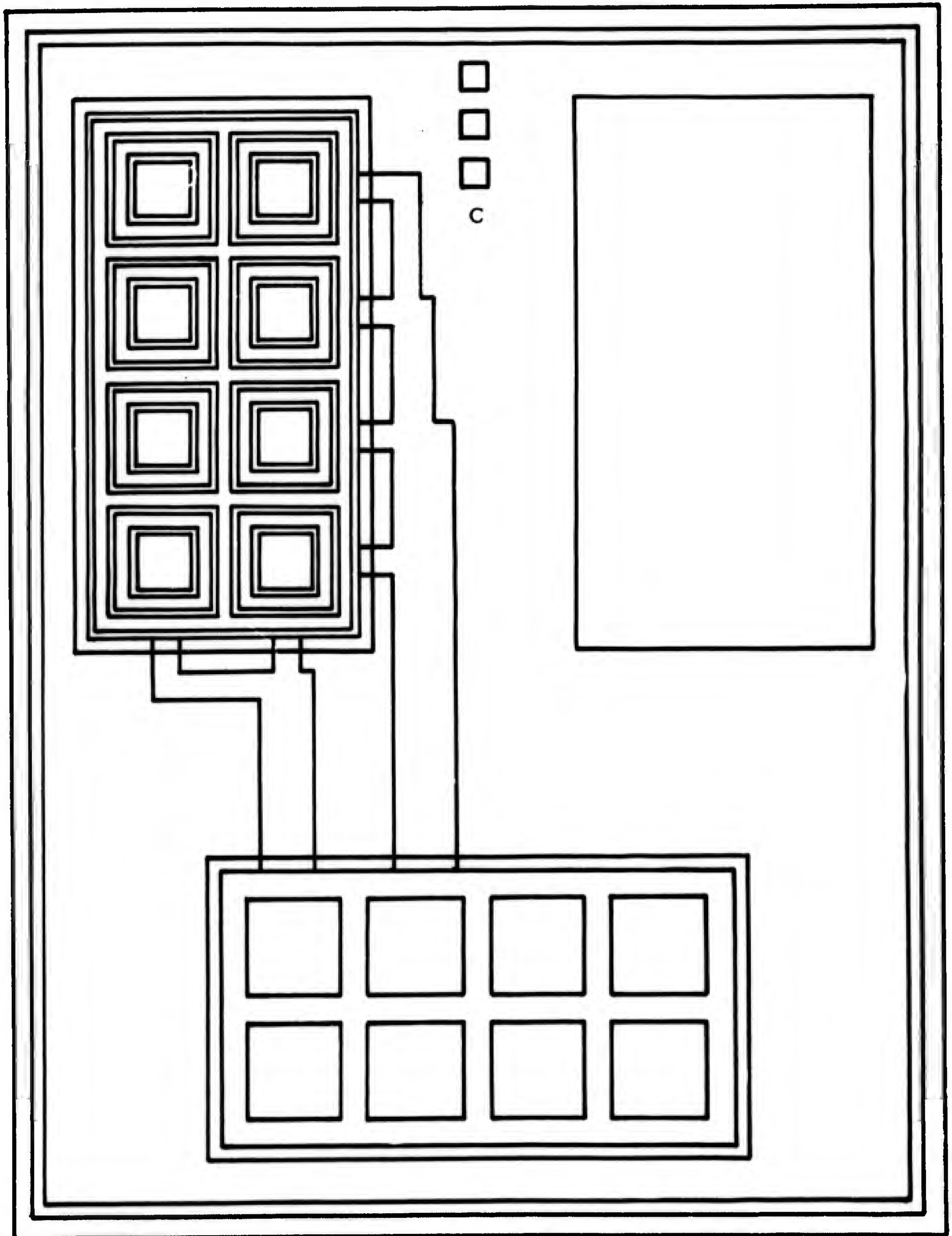


LIGHT ☐ DARK ☐

FIGURE 3.

SCALE 1 DIV. = 0.25 MIL

81247- B

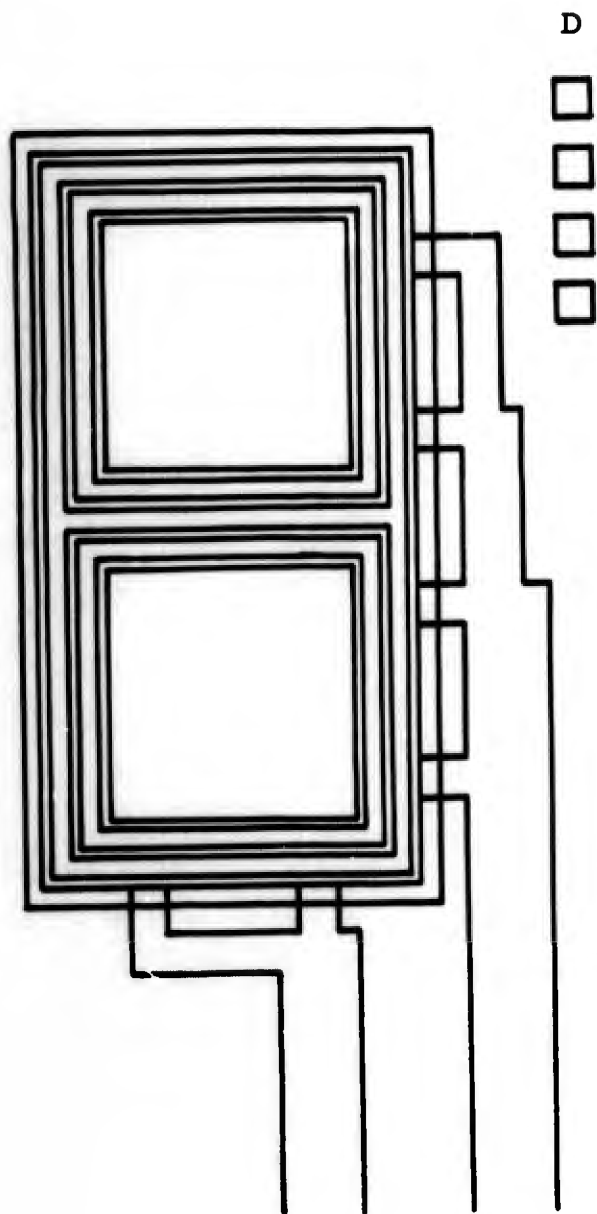


LIGHT ☐ DARK ☐

FIGURE 4.

SCALE 1 IN. = 0.25 MIL

81247- C



LIGHT ☐ DARK ☐

FIGURE 5.

SCALE 1 DIV = 0.25 MIL

81247- D

TRANSISTOR GEOMETRY DATA

	I	II	III	IV
Chip Size	40 x 50	40 x 50	40 x 50	40 x 50
Chip Area	2000	2000	2000	2000
Base Size	24.5 x 29	24.5 x 29	20 x 22	20 x 22
Base Area	710	710	440	440
Emit. Size - each cell	2 x 2	18.5 x 23	2 x 2	6.5 x 6.5
No. of Emitters	30	1	16	4
Emit. Area - per cell	4	425	4	42.25
Total Emit. Area	120	425	64	169
Emit. Periphery- per cell	8	83	8	26
Total Emit. Periphery	240	83	128	104
Emit. Contact Size - each cell	1 x 1	17.5 x 22	1 x 1	5.5 x 5.5
Emit. Contact Area -per cell	1	385	1	30.2
Total Contact Area	30	385	16	120.8
Emit. Contact / Base Area	4.23%	54.3%	3.64%	27.3%
Emit. Contact / Chip Area	1.5%	19.3%	0.8%	6.0%
Active Base Area / Chip Area	35.4%	35.4%	22%	22%
Emit. Area / Base Area	16.9%	59.8%	14.5%	38.4%
Emit. Area / Chip Area	6.0%	21.2%	3.2%	8.45%
Emit. Perip. / Emit Area	2	0.195	2	0.615

FIGURE 6

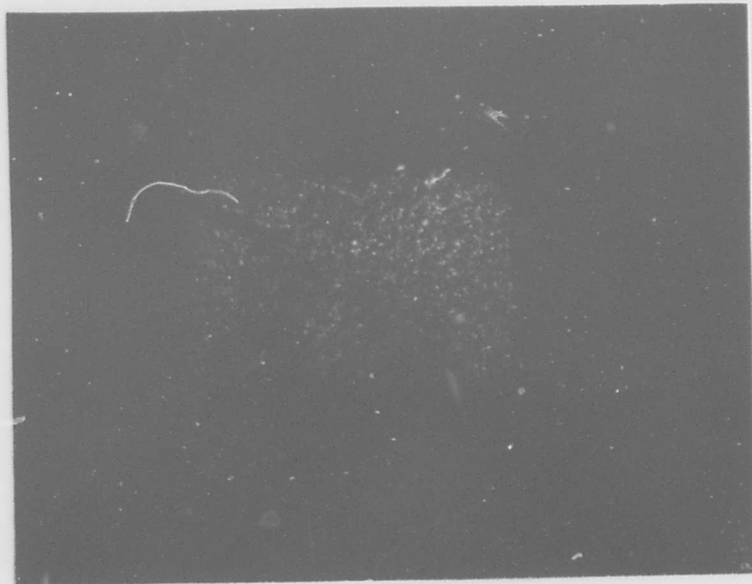


FIGURE 7. BACK BUMP-PLAN VIEW (140X)

FIGURE 8. GEOMETRY C TIN DIPPED - EQUAL BUMPS (140X)

FIGURE 9. TIN DIPPED - UNEQUAL BUMPS (140X)

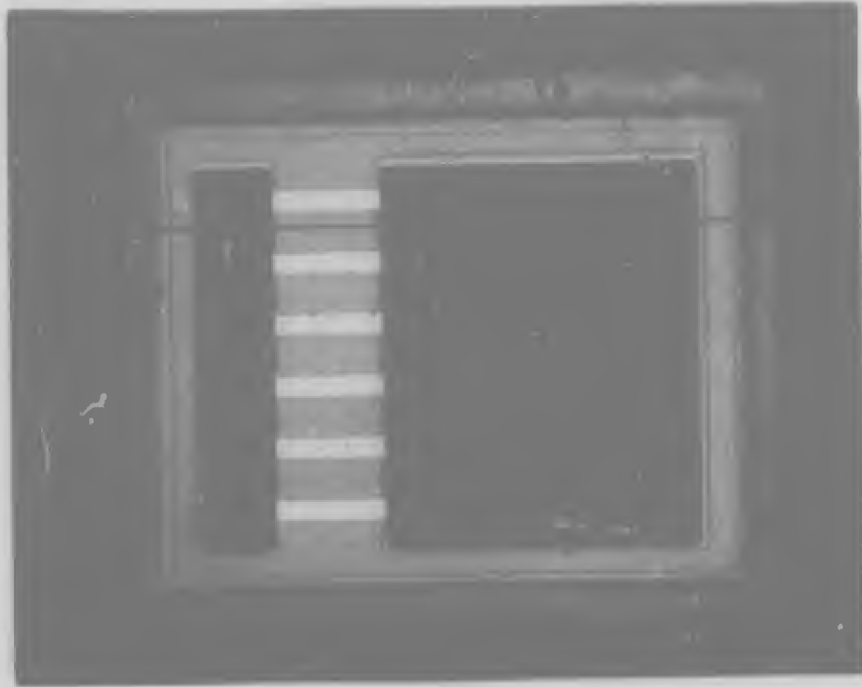


FIGURE 10. GEOMETRY A, PLAN VIEW - COMPLETED BUMPED DIE (140X)

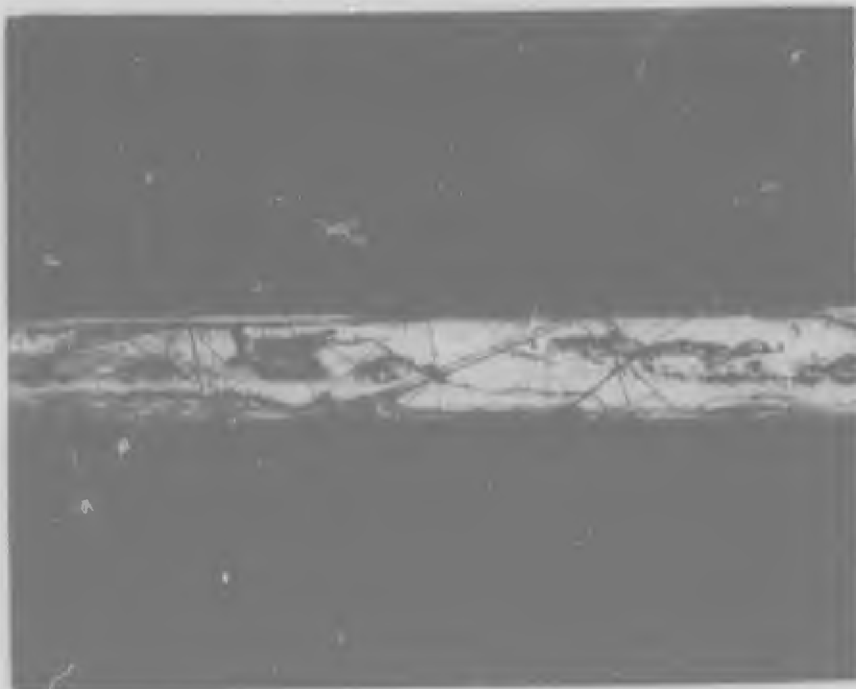
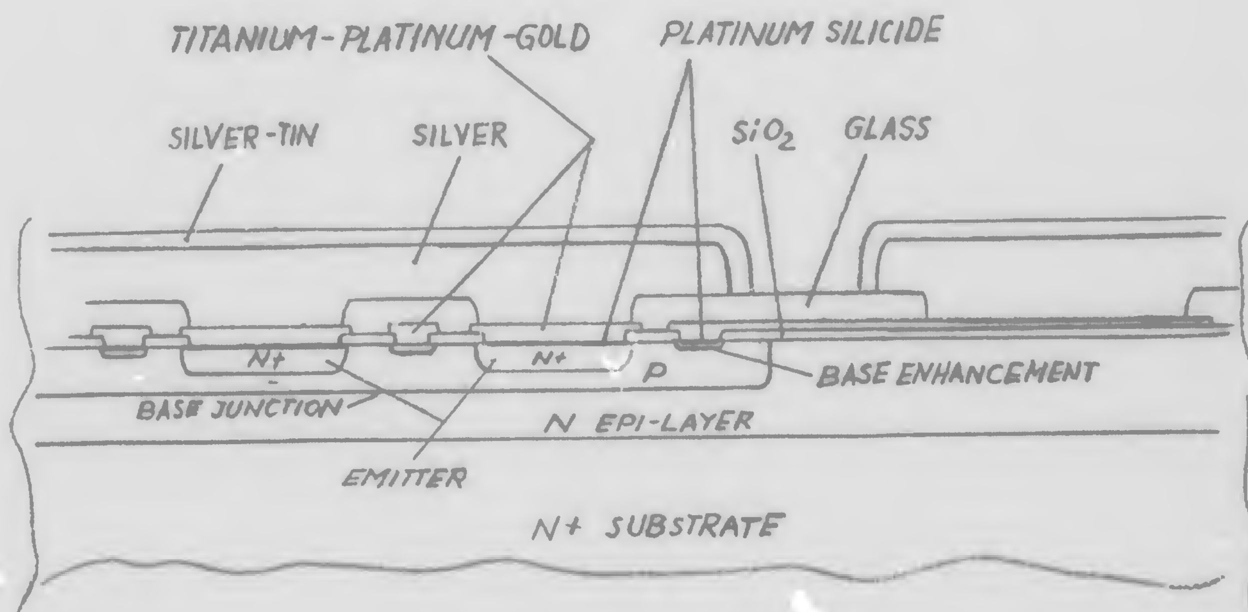
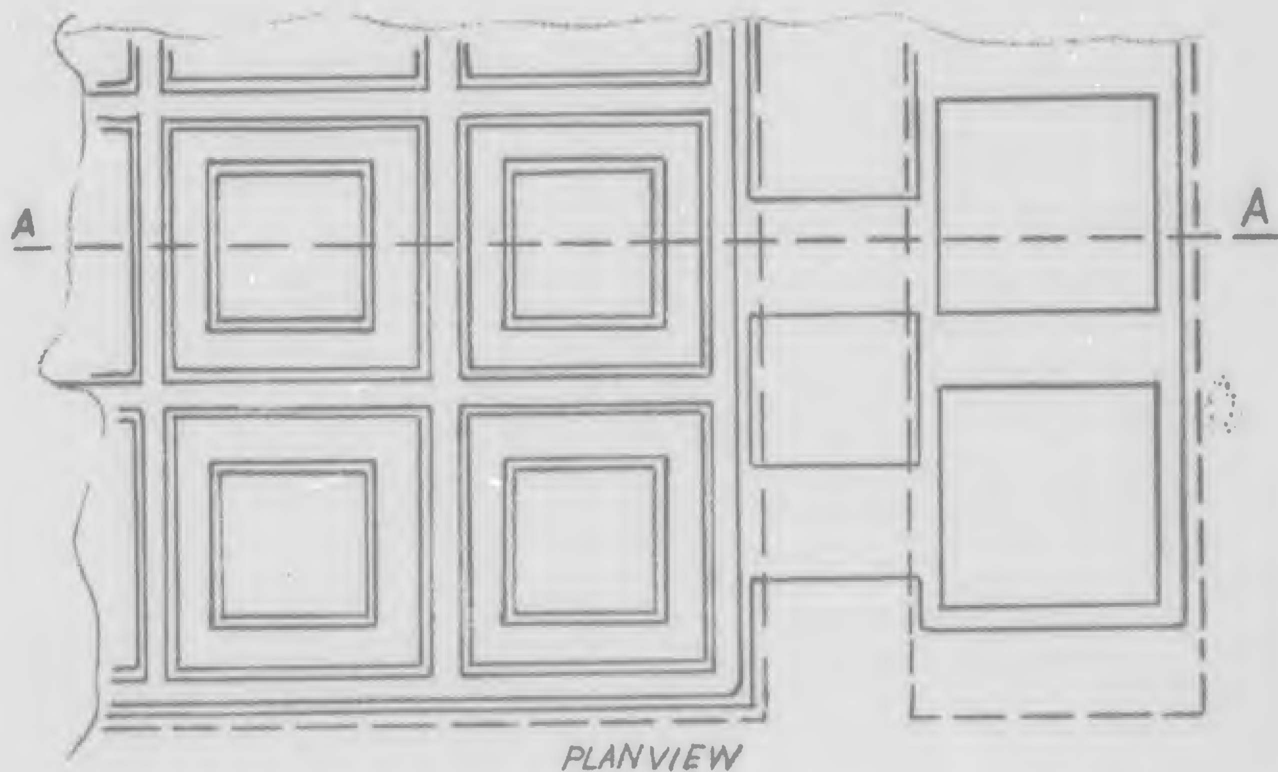


FIGURE 11. GEOMETRY A, CROSS SECTION - BASE AND EMITTER METALLIZATION (70X)



SECTION A-A



PLANVIEW

Figure 10A-Sketch of the Transistor Structure

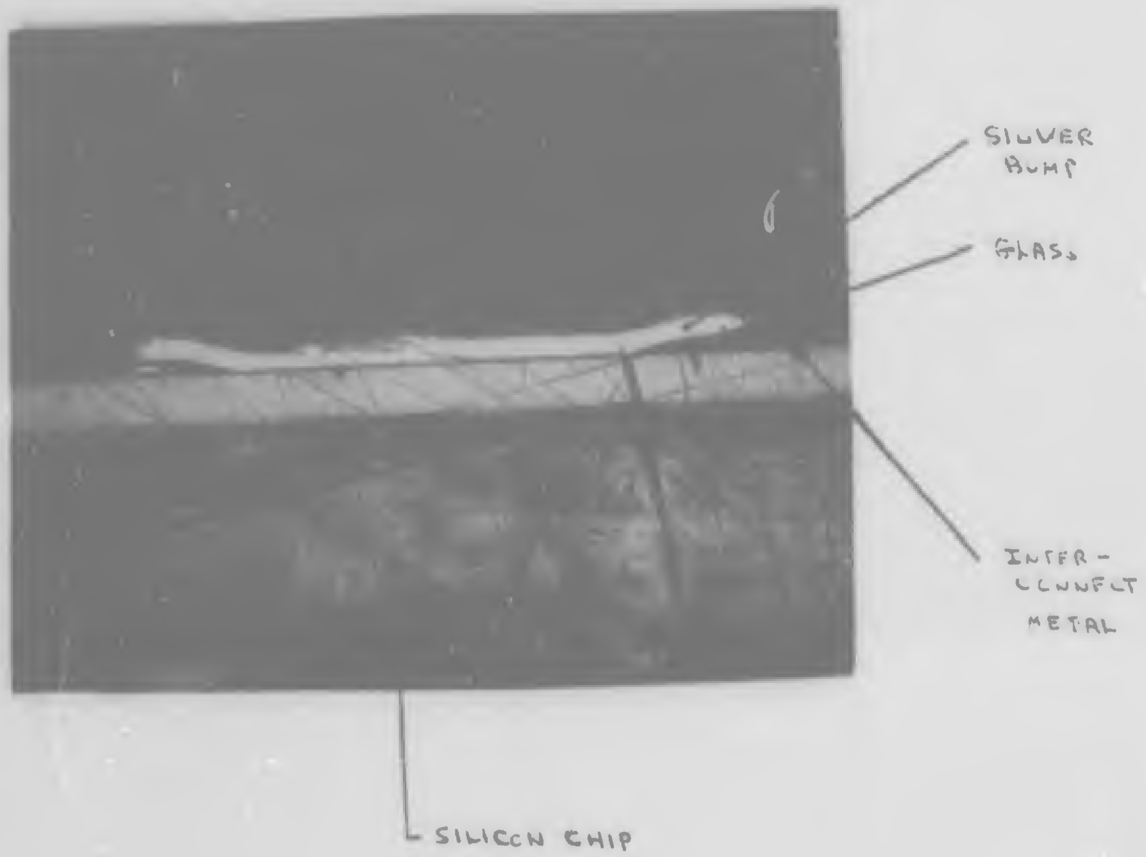


FIGURE 12. GEOMETRY A, CROSS SECTION - BASE CONTACT (410X).

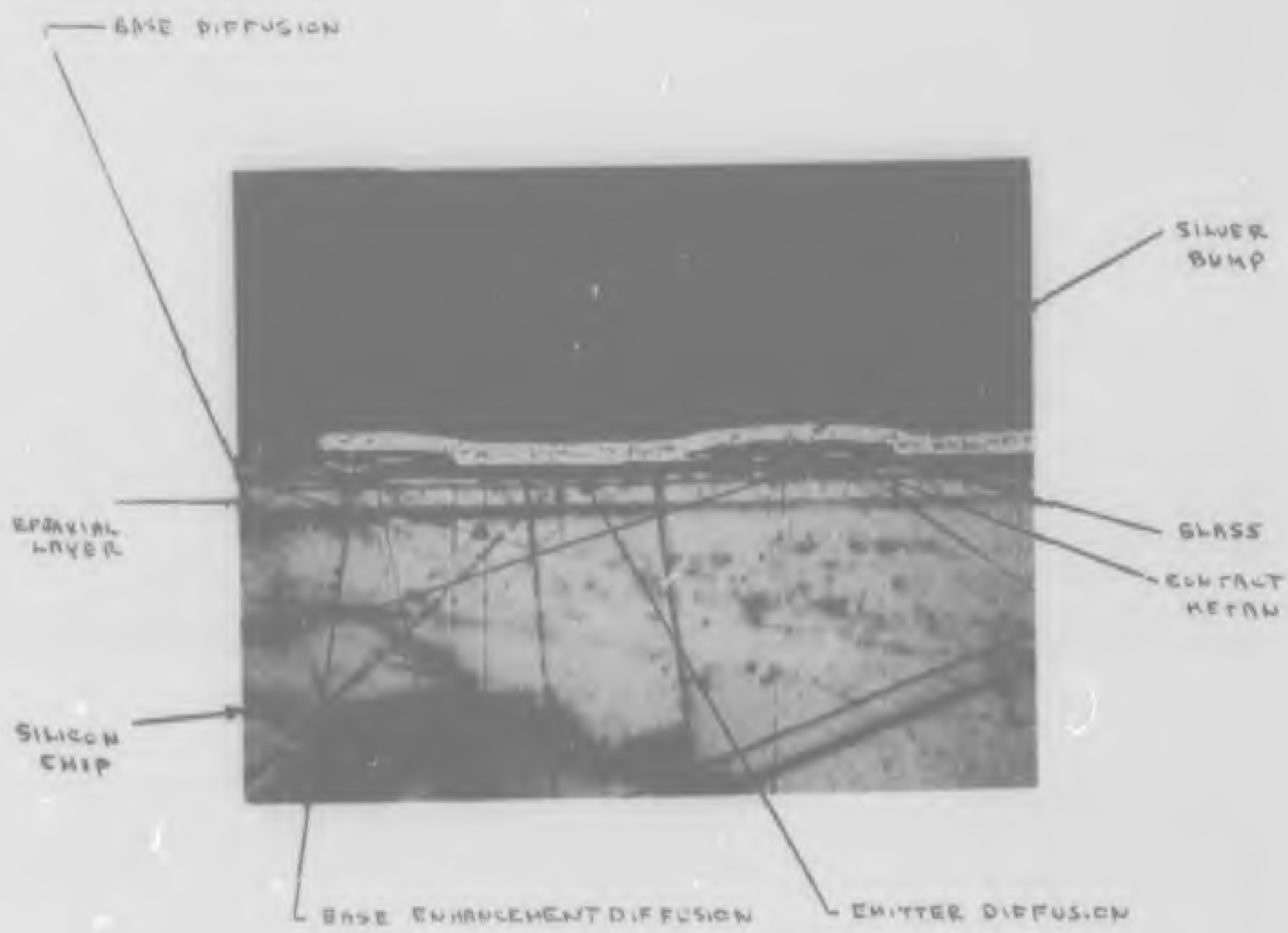


FIGURE 13. GEOMETRY A, CROSS SECTION - EMITTER CONTACT (410X).

FIGURE 14. GEOMETRY B, PLAN VIEW - COMPLETED BUMPED DIE (140X)

FIGURE 15. GEOMETRY B, CROSS SECTION - BASE AND EMITTER METALLIZATION (70X)

FIGURE 16. GEOMETRY B, CROSS SECTION - BASE CONTACT (580X)

FIGURE 17. GEOMETRY B, CROSS SECTION - EMITTER CONTACT(580X)

FIGURE 18. GEOMETRY C, PLAN VIEW - COMPLETED BUMPED DIE (140X)

FIGURE 19. GEOMETRY C, CROSS SECTION - BASE AND EMITTER METALLIZATION (110X)

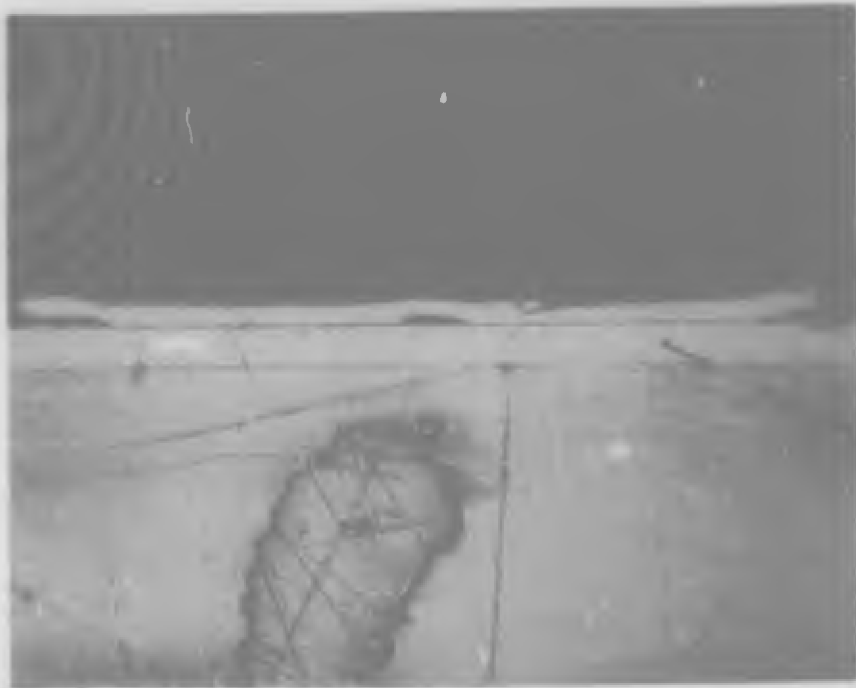


FIGURE 20. GEOMETRY C, CROSS SECTION - BASE CONTACT (410X)

FIGURE 21. GEOMETRY C, CROSS SECTION - EMITTER CONTACT (410X)

FIGURE 22. GEOMETRY D, PLAN VIEW - COMPLETED BUMPED DIE (140X)

FIGURE 23. GEOMETRY D, CROSS SECTION - BASE AND EMITTER METALLIZATION (110X)

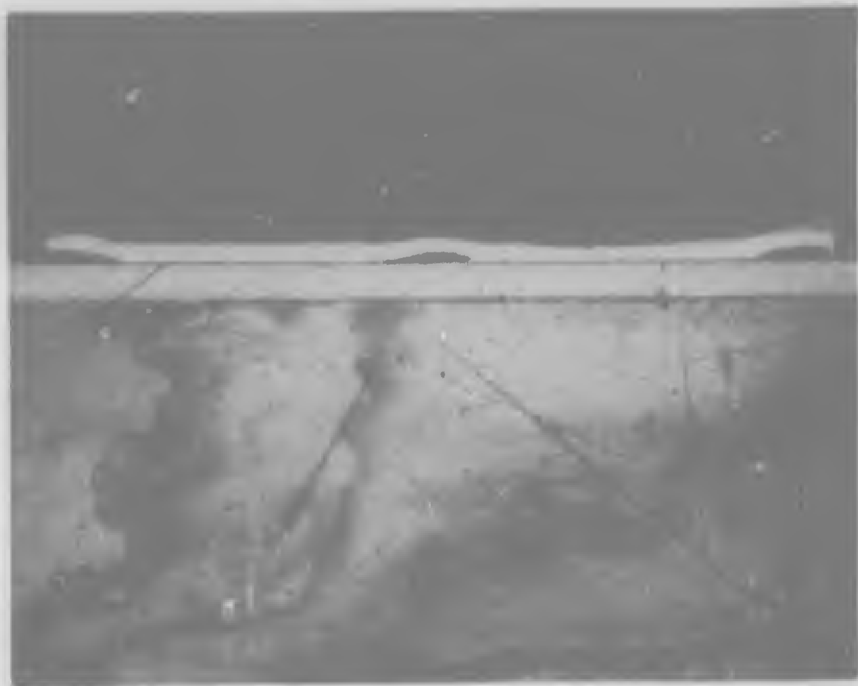


FIGURE 24. GEOMETRY D, CROSS SECTION - BASE CONTACT (410X)

FIGURE 25. GEOMETRY D, CROSS SECTION EMITTER CONTACT (410X)

FIGURE 26. DIE ULTRASONICALLY MOUNTED TO THE HEADER PRIOR TO COLLECTOR STRAP ATTACHMENT (6X).

FIGURE 27. PACKAGE HEADER WITH METALLIZATION PATTERN FOR FACE DOWN MOUNTING OF THE DIE (6X).

FIGURE 28. HEADER-DIE-STRAP-SUB-ASSEMBLY AFTER SOLDER REFLOW, PLAIN VIEW (6X)

FIGURE 29. HEADER-DIE-STRAP-SUB-ASSEMBLY AFTER SOLDER REFLOW, ANGLE VIEW (6X)

FIGURE 30. CROSS SECTION OF FACE DOWN MOUNTED TRANSISTOR DIE WITH COLLECTOR STRAP.

FIGURE 31. PACKAGE HEADER WITH FACE DOWN MOUNTED CHIP AND STRAIGHT SILVER STRAP.

FIGURE 32. PACKAGE HEADER WITH FACE DOWN MOUNTED CHIP AND ONLY SMALL WIRE TO BACK OF CHIP.

FIGURE 33. PACKAGE HEADER WITH FACE UP MOUNTED CHIP AND WIRES TO EMITTER AND BASE.

FIGURE 34. THERMAL RESPONSE STRAPPED UNIT

$H = 1\ \mu S/_{Div}$ $V = 50\ mV/_{Div}$

FIGURE 35. THERMAL RESPONSE NO STRAP

$H = 1 \mu S/_{Div}$ $V = 50\ mV/_{Div}$

FIGURE 36. THERMAL RESPONSE FACE UP UNIT

$H = 1 \mu S/_{Div}$ $V = 50\ mV/_{Div}$

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13. ABSTRACT
The purpose of this work is to determine the feasibility of removing heat simultaneously from both the collector and emitter sides of a double diffused transistor chip. The work consisted of forming a large silver bump over the emitter and a small bump for base contact on the front side of a power transistor chip. This chip was mounted face down on a modified TO-60 header and a large silver strap was used to contact the collector on the back side. A non-multiple emitter structure mounted as above showed a 40% decrease in thermal resistance over a chip mounted face up in a standard manner. It is concluded that dual sided heat removal is feasible and the 40% improvement is substantial enough to warrant further attention.

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collector and emitter						
power transistor chip						
collector and emitter						

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