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QUALIFICATION PROCEDURES FOR HYBRID CIRCUITS

General Motors Corporation
Delco Electronics Division

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13 ABSTRACT

This report summarizes the efforts expended and objectives reached in a program to establish and verify qualification procedures for hybrid microcircuits. The program was conducted in two phases. In the Study Phase, existing qualification data on hybrids were reviewed, and a series of stepped stress tests were performed on three hybrid microcircuit types. In the Verification Phase, the effectiveness of the process control and the screens established by the Study Phase were verified.

The results of the program studies and evaluation led to the establishment of an optimum set of qualification procedures for in-process screening and lot qualification, and the description of cost factors involved in each in-process screen and lot qualification test for Class A, B, and C hybrids, and for various lot sizes. Information was also compiled on vendor qualification and product qualification requirements.

Results of the program also showed hybrid microcircuit reliability to be variable by part and lot, even from the same source over brief periods. This is due principally to the diversity of hybrid part and material sources, which introduces many variables into the manufacturing cycle. The effect of these variables can be greatly minimized by exposing each hybrid to a systematic program of screening and subsequent sampling for Quality Conformance Inspection. The 100 percent screening, by itself, was shown to be not completely effective in excluding faulty and marginal units. To assess the quality of each hybrid lot, a sample must be pulled for Quality Conformance Inspection.

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George A. Hoffman
Roger L. Johnson
Robert J. Straub

General Motors Corporation
Delco Electronics Division

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FOREWORD

The effort described in this report was performed by Delco Electronics Division of General Motors Corporation, Milwaukee, Wisconsin, during the period June 1969 to January 1971, under Contract F30602-69-C-0190, Job Order Number 55190000. Delco number is Electronics Document EP0670. The program was administered under the direction of John P. Farrell (RCRM), Rome Air Development Center, Griffiss Air Force Base, New York.

Chief investigator for Delco Electronics was Robert J. Straub, Senior Project Engineer in the Semiconductor Parts Engineering Group of Parts and Materials Engineering. Engineering assistance was provided primarily by H.L. Kaiser, R.G. Krowas, and K.E. Peterson of the Semiconductor Parts Engineering Group. Publication assistance was provided by T.L. Rinehart of the Engineering Publications Department. General project supervision was rendered by George A. Hoffman, Supervisor of the Microelectronics Group in Semiconductor Parts Engineering. Overall responsibility was held by Roger L. Johnson, Group Head of Semiconductor Parts Engineering.

This technical report has been reviewed and is approved.

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ABSTRACT

This report summarizes the efforts expended and objectives reached in a program to establish and verify qualification procedures for hybrid microcircuits. The program was conducted in two phases. In the Study Phase, existing qualification data on hybrids were reviewed, and a series of stepped stress tests were performed on three hybrid microcircuit types. In the Verification Phase, the effectiveness of the process control and the screens established by the Study Phase was verified.

The results of the program studies and evaluation led to the establishment of an optimum set of qualification procedures for in-process screening and lot qualification, and the description of cost factors involved in each in-process screen and lot qualification test for Class A, B, and C hybrids, and for various lot sizes. Information was also compiled on vendor qualification and product qualification requirements.

Results of the program also showed hybrid microcircuit reliability to be variable by part and lot, even from the same source over brief periods. This is due principally to the diversity of hybrid part and material sources, which introduces many variables into the manufacturing cycle. The effect of these variables can be greatly minimized by exposing each hybrid to a systematic program of screening and subsequent sampling for Quality Conformance Inspection. The 100 percent screening, by itself, was shown to be not completely effective in excluding faulty and marginal units. To assess the quality of each hybrid lot, a sample must be pulled for Quality Conformance Inspection.

It is recommended that additional studies and testing be funded to:

1. Establish and verify qualification procedures for beam lead and flip chip hybrid microcircuits, and for complex hybrids in larger packages.
2. Assess the need for hermetic cases for packaging beam lead and flip chip microcircuits.

EVALUATION

The objective of this effort was to establish optimum procedures for assuring standard levels of quality and reliability for hybrid microcircuits. These new procedures were to provide, with a high degree of confidence, the specified classes of quality and reliability per MIL Standard 883 Method 5004. Wherever possible, maximum standardization through the use of the silicon monolithic microcircuit methods and procedures was to be attempted, with successive higher levels of quality and reliability being accomplished through more rigorous control and increased screening. Basically, the contractual requirements were to provide detailed procedures for vendor and device qualification, lot quality conformance and device screening, and also to associate with each, the cost as a function of the quality level.

The program was performed in two parts: a study phase to establish the most effective and nondestructive series of screening procedures determined by a step stress testing program on three device types; and a verification phase designed to evaluate the effectiveness of the developed procedures. During the study phase, a survey of the industry was completed that determined the types of hybrids in use today and those envisioned for the near future. Also, a comprehensive analysis of the data accumulated from the previous testing of 125,000 hybrid microcircuits was completed.

All of the screens of Method 5004 of MIL-STD-883 and several others were evaluated to optimize methods and procedures. The results of these evaluations were useful as a whole, but in the following areas, the findings were significant.

Hermeticity - Data received from the weight change technique of gross leak detection was instrumental in deciding to include this procedure in Method 1014.1 Seal of MIL-STD-883.

Bond Strength (Attached Chips) Test results indicate that a shear stress test, on attached chip components, is required on a sampling basis.

Centrifuge - It was shown that force in the Y_2 direction can push the flying lead wires toward the substrate causing potential shorts. This is true for hybrids because the internal wire leads are usually longer and tend to lie closer to the edges of chip devices than in integrated circuits. Therefore, centrifuge in the Y_2 direction is not recommended as a 100 percent screen test.

Reverse Bias Burn-In - Due to the extensive handling of semiconductor chips prior to, and during, circuit fabrication, the possibility of surface contamination is greatly increased. It was concluded that a reverse bias burn-in should be required when a circuit design readily allows the reverse biasing of a significant number of chips.

This completed hybrid effort is part of the RADC/RCRM microcircuit quality and reliability assurance studies which are designed to provide the required reliability for all forms of microcircuits the Air Force uses. However, additional work is still required to define the bonding and screening procedures applicable to attached active and passive chip components for hybrids. Also, rework in hybrids presents a different problem than rework in integrated circuits, because they are usually more expensive and fabricated in smaller quantities. These circuits, in most cases, contain various types of components which have to be mounted and interconnected to complete the circuit function which complicates the fabrication of the devices. As a result, rework is desirable from a practical and an economic point of view. Therefore, it must be decided when rework is allowable, what are acceptable limits and what criteria are necessary for control.

The overall results of this effort have been extremely useful to RCRM in revising MIL-STD-883, Test Methods and Procedures for Microcircuits. The contractor's overall performance was excellent and the program's objectives were satisfactorily completed.


JOHN P. FARRELL

Solid State Applications Section
Reliability Branch

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SECTION I

INTRODUCTION

1.1 PROGRAM OBJECTIVES

This report summarizes the efforts expended and objectives reached in a program to establish and verify qualification procedures for hybrid microcircuits, under Contract F30602-69-C-0190, issued by the Rome Air Development Center.

The functional requirements of military systems currently being developed are, to a great degree, being met through the application of hybrid microcircuit techniques. The nature of these systems is such that, in procuring these hybrid circuits, safeguards must be established to assure maintenance of specific levels of quality and reliability. Procedures for handling microelectronic devices had previously been established in MIL-STD-883, Test Methods and Procedures for Microelectronics, and in Notices 1 and 2. These procedures, however, were developed with principal emphasis on silicon monolithic circuits. This program, conversely, was concerned with hybrid microcircuits—establishing and verifying an optimum set of qualification procedures for assessing the basic capability of vendors to produce hybrid microcircuits at specified levels of quality and reliability. In doing this, the program yielded additional information necessary to incorporate hybrid microcircuit testing into the procedures of MIL-STD-883.

The overall program had two main phases:

1. The Study Phase, in which existing qualification data on hybrids were reviewed and a series of stepped stress tests was performed on three hybrid microcircuits.
2. The Verification Phase, in which the effectiveness of the process controls and screens established by the study and evaluation phase was verified.

For purposes of this investigation, the following definition of a hybrid microcircuit was adopted:

"A hybrid microcircuit is a microcircuit consisting of elements which are a combination of the film circuit type and the semiconductor type, or a combination of one or both types with discrete parts."

1.2 GENERAL APPROACH

The general approach to the goals of the program was to:

- Review the effectiveness of existing specifications already in use,
- Perform additional tests to determine the capabilities of hybrid micro-circuits which were in production,
- Perform verification and demonstration tests on a significant number of hybrids to validate the qualification procedures.

1.3 ORGANIZATION OF REPORT

This report is presented in two general parts. The first part is a general discussion of the overall program, and includes data summarizations and pertinent findings. The organization is such that major program phases are covered within major subsections. Among the major topics covered are "types of hybrids in use" (Paragraph 2.2), "experience with hybrids on production volume programs" (Paragraph 2.3), "stepped stress testing of hybrids" (Paragraph 2.4)... "screening results to obtain Class C, B, and A hybrids" (Paragraph 3.4)... and "overall conclusions" (Section IV).

The second part is appendixes containing procurement documents used in the study, and detailed information and test results, in support of the findings discussed and the conclusions set forth in the report's main body.

SECTION II

STUDY PHASE

2.1 GENERAL

The objectives of the study phase were to:

- Study, evaluate, and summarize existing data on hybrid microcircuits,
- Perform a series of tests to determine the effectiveness of specific environmental and mechanical tests in evaluating hybrid microcircuits.

Existing data were reviewed to determine the effectiveness of screens in identifying reliable hybrid microcircuits. Environmental and mechanical tests were performed, as a series of stepped stress tests, to establish what stress levels the hybrids could withstand, and to determine new and better ways of qualifying hybrids.

2.2 HYBRID TYPES AND APPLICABLE TESTING

2.2.1 HYBRID VARIABLES

A survey was performed of the industry to determine the types of hybrids currently being manufactured and the types envisioned for the near future. This was accomplished through a literature search and by calling on company experience on recent proposals on complex hybrid circuits for systems of the future.

In surveying the types of hybrids, reference was made to the Survey of Manufacturers of Film Circuitry, prepared by The Boeing Company of Seattle, Wash.* This effort resulted in definition of eight general variables in the makeup of a hybrid microcircuit. These eight variables, which affect the maximum levels of stress testing that can be applied to hybrid microcircuits without causing damage, are listed in Table I.

The variables in Table I, which in various combinations constitute the different types of hybrid microcircuits, should be carefully reviewed before selecting test levels according to the procedures of MIL-STD-883. Besides the tests described in MIL-STD-883, specific test requirements may have to be imposed for unique hybrid applications. In such cases, a good general rule is to specify electrical tests which will confirm that each hybrid pin is functioning as intended. Such tests would be performed with specific input, output, and power supply voltage and current limits at specified temperatures.

*Survey of Manufacturers of Film Circuitry. 3 Reports dated Apr. '67, Nov. '67, and June '68. Submitted by The Boeing Contract N00163-67-C-0040.

Table I (Sheet 1 of 2). Identified Variables in Hybrid Microcircuit Makeup

GENERAL VARIABLES	SUBVARIATIONS
Electrical Properties	<ul style="list-style-type: none"> • Digital • Linear • Power Dissipation • Combination (or special)
Semiconductor Components	<ul style="list-style-type: none"> • Transistors • Diodes • Zener Diodes: <ul style="list-style-type: none"> – Regulator – Precision Reference – Low Voltage (Alloy Devices with Less Than 6.5 V) • Monolithic Integrated Circuits
Interconnections Between Active Devices	<ul style="list-style-type: none"> • Chip and Wire: <ul style="list-style-type: none"> – Au Wire – Al Wire • Flip-Chip or Face Bonded Chips • Beam Lead • LID or Channel • Hermetic Package Discrete Semiconductors • Nonhermetic Package Discrete Semiconductors (Plastic Devices)
Package and Substrate	<ul style="list-style-type: none"> • Package Whose Bottom is also the Substrate (Special Bottom for Each Hybrid Circuit Type) • Ceramic Substrate Fastened to Package Bottom: <ul style="list-style-type: none"> – Alloyed to Bottom – Solder Glass or Glass Frit – Epoxyed to Bottom

Table I (Sheet 2 of 2). Identified Variables in Hybrid Microcircuit Makeup

GENERAL VARIABLES	SUBVARIATIONS
Package and Substrate (Continued)	<ul style="list-style-type: none"> ● Various Sizes of Package (1/4" × 1/8", Up Through 2" × 2") ● Various Package Materials: <ul style="list-style-type: none"> — Metal — Glass — Ceramic — Plastic or Epoxy ● Hermetic or Nonhermetically Sealed
Conductors on Substrate	<ul style="list-style-type: none"> ● Thick-Film ● Thin-Film
Resistors	<ul style="list-style-type: none"> ● Thin-Film on Substrate ● Thick-Film on Substrate ● Diffused Silicon Chips ● Thick-Film Chips ● Thin-Film Chips <ul style="list-style-type: none"> — Single Chip (All Resistors on One Common Substrate Chip) — Multi-Chip (One Resistor per Chip)
Capacitors	<ul style="list-style-type: none"> ● Ceramic Chip ● Tantalum Thin-Film ● MOS ● Small Discrete
Inductors	—

Individual conditions may require dc, ac, or pulsed dc excitation. In high power dissipation hybrids, the pulse width and duty cycle of pulsed dc tests become important factors where the hybrid is actually to be used under dc conditions. Checkout of a high power hybrid with a narrow-pulse-width, automatic, integrated circuit tester, at a specific temperature, may not assure that the hybrid will function in the actual application, because the junctions will not stabilize at the operating temperature the hybrid will experience. Electrical tests, over and above the functional tests, may have to be added to establish the quality of semiconductor junctions and passive circuit components.

The particular semiconductor components employed in the circuit have a significant bearing on what types of electrical tests should be required for the circuit and whether or not burn-in screens should be required. If discrete transistors and diodes are used, a reverse bias burn-in may prove to be more effective than a parallel excitation life. The most effective method can be determined only by testing specific hybrids using each method. If the semiconductor components used are monolithic TTL chips, however, a reverse bias burn-in would probably be ineffective.

Interconnection between active devices is another important area to consider. The low mass of 1-mil aluminum wire makes acceleration screening for weak bonds relatively ineffective at levels below 100,000 g. Data must also be obtained to determine whether beam-leaded and flip-chip hybrids are effectively screened with acceleration in the Y_1 axis.

The package and substrate are also important variables in determining stress levels applicable to a particular hybrid microcircuit. Package size, for example, is a critical feature, limiting acceleration, mechanical shock, thermal shock, and temperature cycling. Many large packages ($5/8" \times 5/8"$ and larger) are highly susceptible to environmental and mechanical damage. Conductors on the internal substrate can have limitations on their current-carrying capacity, and thin-film conductors can be subject to degradation when tested in nonhermetic packages. Hybrids having large chip resistors, capacitors, or inductors can have limited tolerance to applied stress levels due to the very mass of their chips, and also to the thermal coefficient of expansion-versus-expansion coefficient of the substrate on which they are mounted.

2.2.2 CONCLUSIONS ON SELECTION OF STRESS LEVELS

In determining the electrical, mechanical, and environmental stress levels applicable to a hybrid microcircuit, certain variables inherent in the makeup of each specific hybrid circuit must be considered, as well as the ultimate application of the device. There is, however, no general procedure applicable to all hybrid microcircuits because the maximum stress levels tolerable by each hybrid depend on all these variables (totally) and on the subvariations thereof.

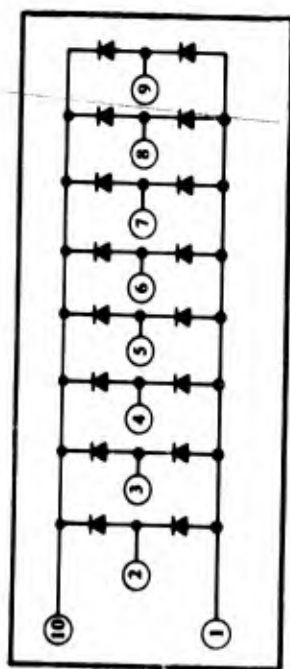
The screens applied must have stress levels low enough to not damage the hybrid, yet high enough to accelerate any latent failure mechanisms. The basic intent of screens is to stress parts sufficiently to precipitate the failure of unreliable devices during the short term screen tests. Acceptable parts are those which operate without failure for a given interval of time, at specified conditions, for each application.

2.3 VOLUME PRODUCTION EXPERIENCE WITH HYBRIDS

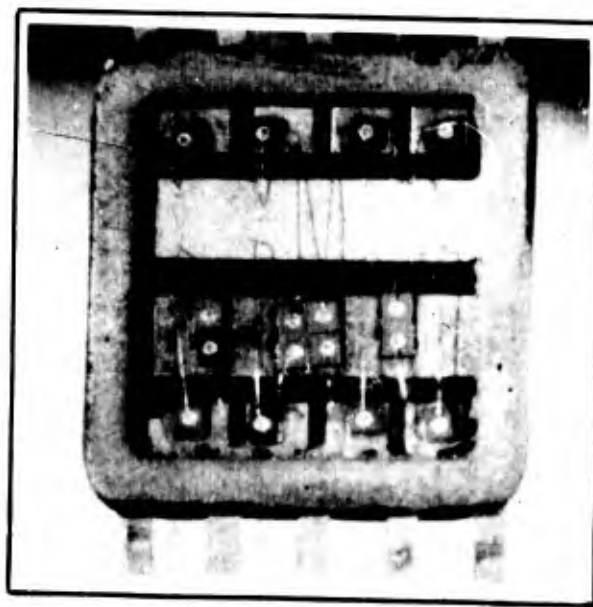
2.3.1 HYBRID CIRCUIT DESCRIPTION

Delco Electronics Division tested approximately 125,000 hybrid microcircuits from eight different manufacturers during 1967, 1968, and the first 8 months of 1969. Detailed results of this testing are presented in this section. The subject hybrids were relatively simple circuits, fabricated by the chip and wire approach, and packaged in $1/4" \times 1/8"$, $1/4" \times 1/4"$, and $1/4" \times 3/8"$, hermetically sealed flatpackages. The circuits involved were diode arrays, ladder switches, core memory switches, amplifiers, analog gates, and a dual JK flip-flop.

Figures 1 through 5 show some of the hybrid circuits used in gathering data. Figure 1 shows the schematic of a 16-diode array and the actual package of 14 chips. A ladder switch is shown in Figure 2 as two PNP transistor chips, an NPN transistor chip, and five thin-film nichrome resistors on a silicon chip. In Figure 3, two diode chips are combined with two NPN transistor chips, two PNP transistor chips, and four thin-film nichrome resistors on a silicon chip to form a memory switch. The same circuit, with thick-film resistors instead of thin-film, is shown in Figure 4. The dual-analog gate in Figure 5 consists of six FET chips, two NPN transistor chips, two PNP transistor chips, two diode chips, and two thick-film resistors in a $1/4" \times 3/8"$ flat-package. While the circuits shown do not include all the types evaluated, they are typical examples of the hybrids evaluated.

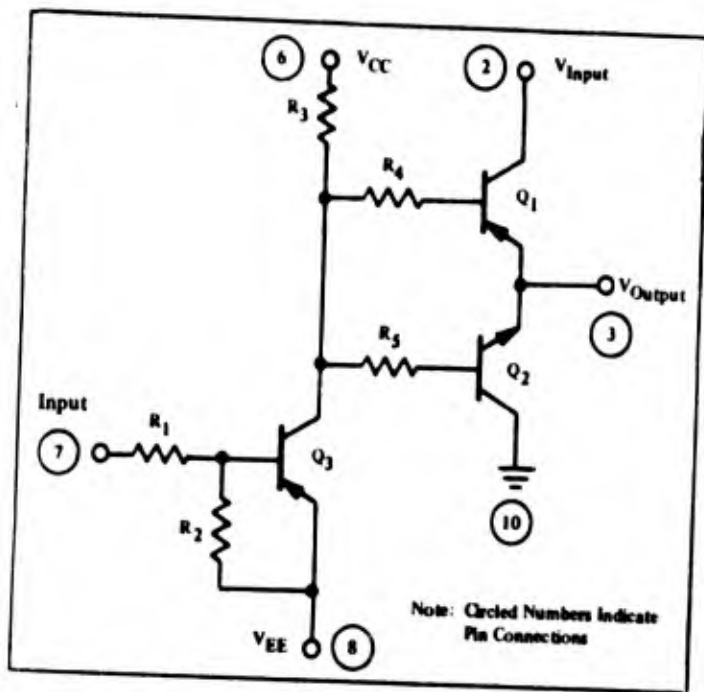


a. Schematic



b. $1/4" \times 1/4"$ Flatpack (Note the Unacceptable Crossover of Internal Conductors.)

Figure 1. Sixteen-Diode Array from Manufacturer D

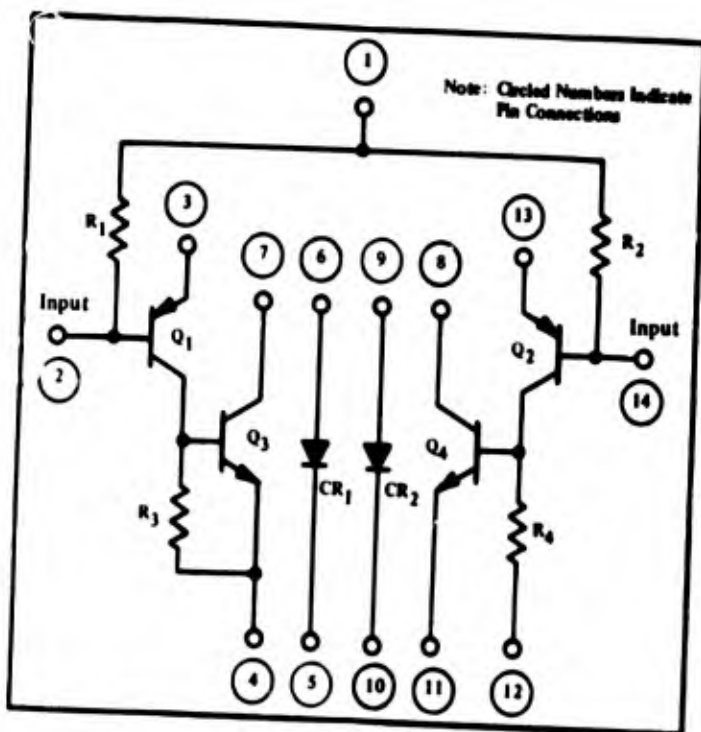


a. Schematic

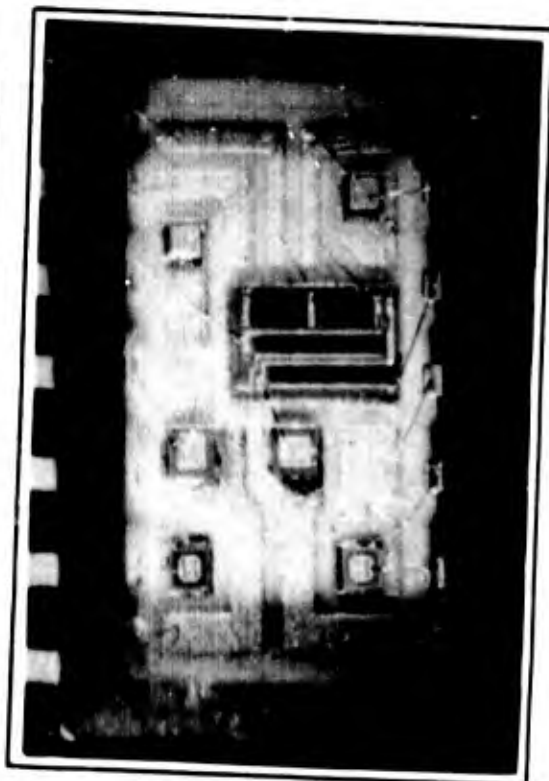


b. 1/4" x 1/8" Flatpack

Figure 2. Ladder Switch and Driver from Manufacturer B



a. Schematic

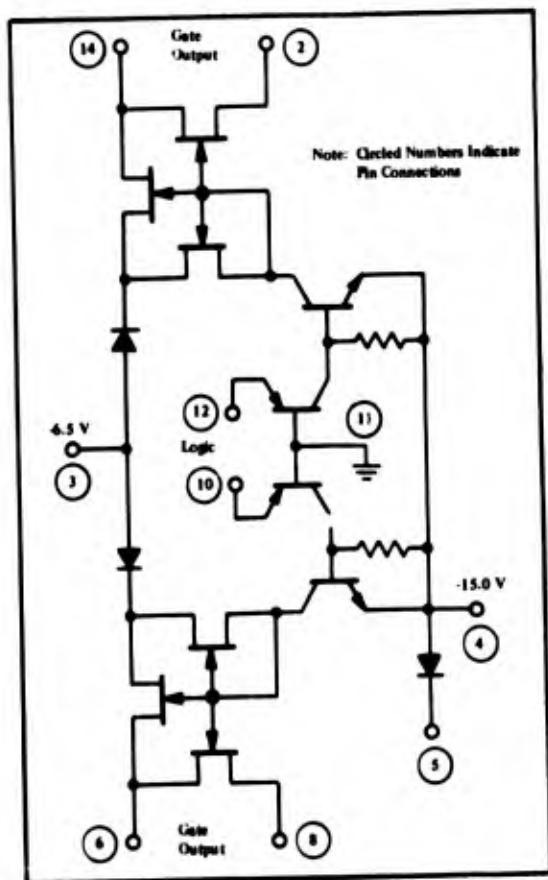


b. 1/4" x 3/8" Flatpack

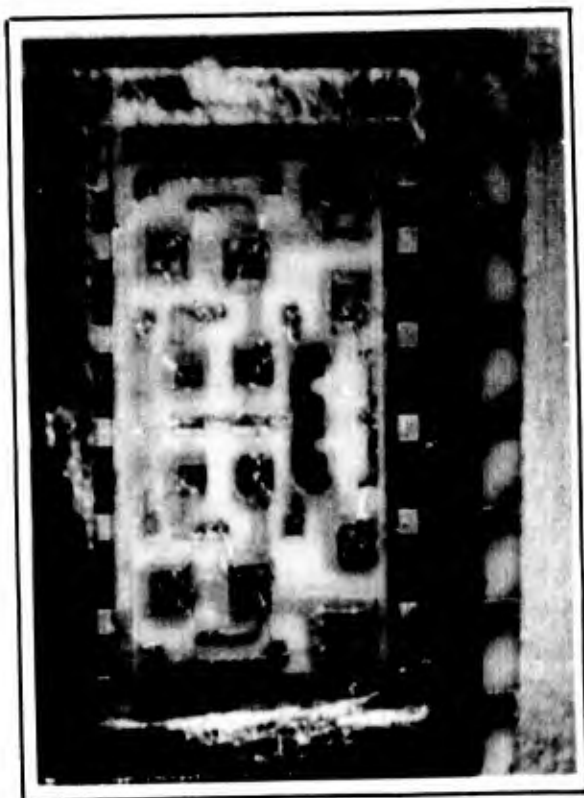
Figure 3. Memory Hybrid Switch from Manufacturer B



Figure 4. Memory Hybrid Switch from Manufacturer A



a. Schematic



b. 1/4" x 3/8" Flatpack

Figure 5. Dual Analog Gate from Manufacturer E

All of the hybrid microcircuit test results covered in this section apply to hermetically sealed flatpackages. The internal interconnects between active devices consist of flying wire leads made of either 0.7-mil or 1.0-mil gold wire, with a thermocompression gold ball bond on one end and a wedge bond on the other. The transistor, diode, and resistor chips had thin-film aluminum metalization, while the substrates used thick-film, gold interconnects. Chips were alloyed down to the substrate, and the packages were hermetically sealed with a gold plated kovar lid, soldered to a gold plated seal ring. The lead frames were gold plated kovar.

Manufacturers A and E used a ceramic substrate, which was alloyed to the package bottom. Manufacturers B and D used a package whose bottom served also as the substrate.*

2.3.2 SUPPLIER PRESHIPMENT REQUIREMENTS

All of the data presented was obtained during receiving-inspection, extended performance testing (a Delco Electronics in-house program of sample environmental testing which is discussed later), and failure analysis of parts procured from hybrid microcircuit suppliers to Delco Electronics high reliability specifications. The parts were purchased from approved suppliers on a competitive bid basis. The hybrid specifications accompanying each purchase were embodied in Specification Control Drawings (SCD's) which gave flatpackage dimensions and allowable tolerances, the circuit schematic with nominal component values, a table of absolute maximum ratings for current and voltages to all pins, and a table of detailed test conditions.

The detailed test conditions specified the voltage, current or resistance, and associated tolerances, to be applied to each pin, and the allowable limits on the measured parameter for each temperature. An inspection level was specified for each electrical parameter; that is, either 100 percent inspection, or sample inspection, to test to as a minimum, at both +25°C and the temperature extremes (-55°C, +125°C). The sample inspection was given as an LTPD**, which required a minimum size of sample to be tested to assure, with a 90 percent confidence, that a lot having percentage defective equal to the specified LTPD will not be acceptable.

The inspection levels specified were 100 percent for all dc parameters at +25°C, plus 100 percent for all critical ac values and switching times and for critical parameters at the temperature extremes. All other electrical tests were usually specified to be tested to an LTPD of 10, maximum acceptance number of 3. Also specified in the SCD was the maximum allowable thermal resistance of the flatpackage, both for junction-to-case and junction-to-ambient conditions.

*Codes used to designate manufacturers are carried through consistently in this report to enable a meaningful comparison of results presented in each section.

**Lot Tolerance Percent Defective—Reference MIL-STD-883, Method T5005, Table III.

The prescribed tests and test levels were determined by a Parts Engineer after he became familiar with each hybrid microcircuit application. He then specified the electrical parameters in such a manner that they could be programmed on an automatic integrated circuit tester. (See Appendix IA, for a copy of a typical SCD.)

For all hybrid circuits, the SCD referenced a General Specification which required the supplier to do additional 100 percent preconditioning of all hybrids. This preconditioning is shown in Figure 6, which depicts a supplier's order of procedure. This 100 percent screening is equivalent to the Class B screening of Method 5004, MIL-STD-883. The 100 percent preconditioning begins with a precap internal-visual inspection of each hybrid. The specific conditions were negotiable depending on the hybrid circuit and the supplier's manufacturing methods. (The precap visual specified was similar to the internal visual Method 2010, MIL-STD-883, Test Methods and Procedures for Microelectronics.) The next 100 percent preconditioning requirement was high temperature stabilization, either by storing at +150°C minimum for at least 24 hours, or at +200°C for at least 16 hours. After high temperature stabilization, the devices were subjected to temperature cycling for a minimum of 10 cycles from -65 to +150°C per MIL-STD-883, Method 1010, Condition C.

After temperature cycling, the parts were required to be centrifuged at 20,000 g minimum for 1 minute in the Y₁ axis to tear loose faulty internal wire bonds, semiconductor and resistor chips, and substrates. In some cases, it was also required to accelerate parts in an axis perpendicular to Y₁ (X axis) to detect lifted chips which have marginal electrical continuity. Imposition of this requirement depended on the particular design involved, as well as past experience.

On completion of preconditioning, the packaged hybrids were hermetic seal tested. Fine leak was specified per MIL-STD-883, Method 1014, Test Condition A or B, with a leak rate limit of 1×10^{-8} atm-cc/s. Gross leak, formerly performed per MIL-STD-202, Method 112, Test Condition A or B (involving part immersion in a hot fluid and check for air bubbles), is now specified per MIL-STD-883, Method 1014, Test Condition C, Step 2, specifying fluorocarbon vacuum/pressure backfill and fluorocarbon bubble testing. The superseded MIL-STD-202 methods were found to be inadequate in detecting all gross seal failures. The MIL-STD-883 methods proved to be much more effective. When questionable results were obtained, they were verified by a weight/backfill/weight increase test.

After seal testing, the parts were tested electrically to eliminate failures induced by the earlier environmental screens. Then they were subjected to an operating burn-in at +125°C for 168 hours. Operating conditions specified on the SCD were either for circuit operation at maximum allowable power dissipation with an alternating current- or pulsed-input, or for steady-state operation wherein the majority of semiconductor

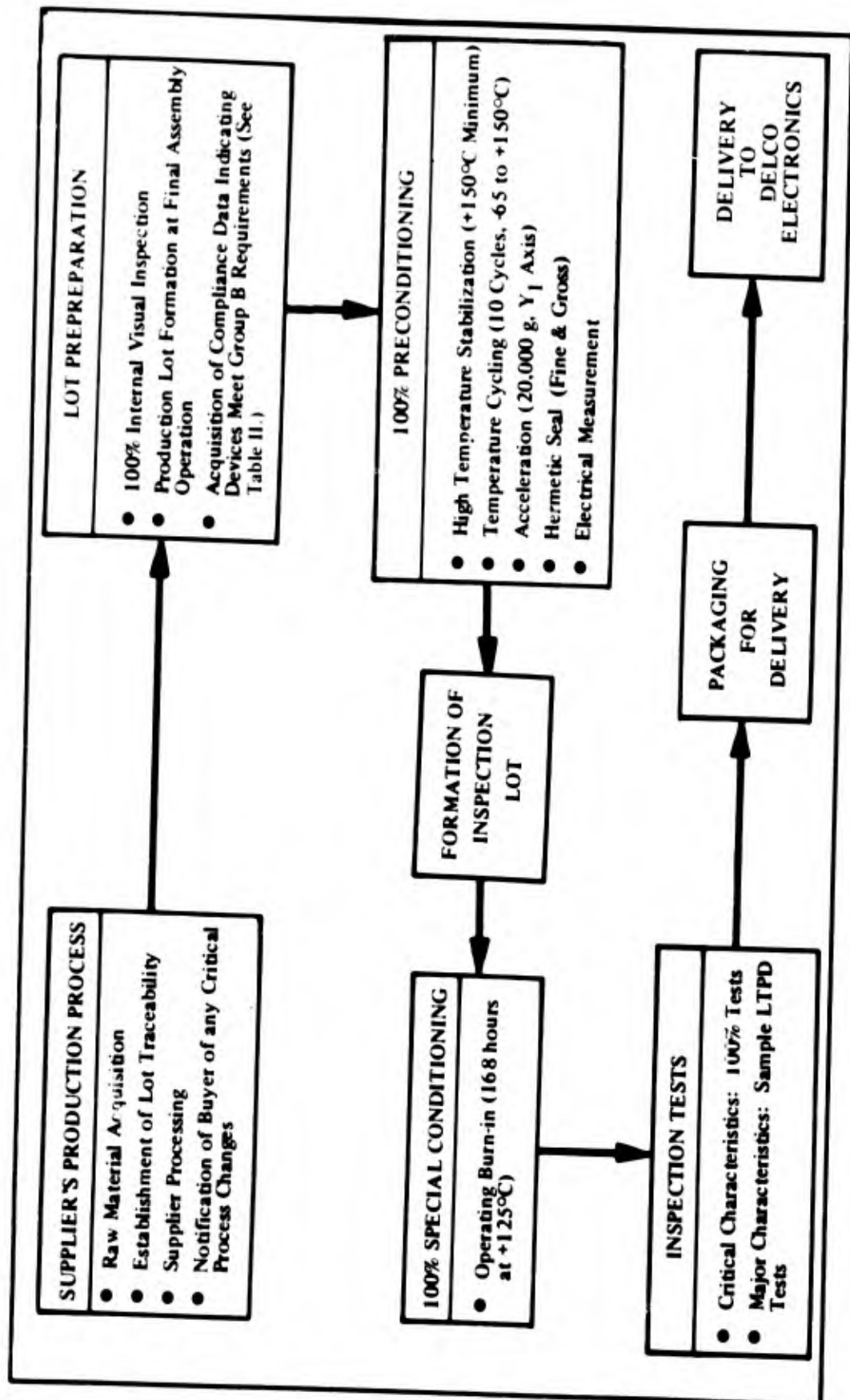


Figure 6. Supplier Processing Procedure, Prior to Shipment

junctions were reversed biased without current limiting. Caution was to be exercised under conditions of no current limiting to avoid voltage transients capable of driving devices into reverse breakdown, or latching up circuits and inadvertently destroying good units.

After the operating burn-in, the supplier was required to perform the 100 percent electrical tests specified on the SCD, and then the sampling inspection. The General Specification also required all the parts to be capable of meeting the Group B requirements of Table II. (See Appendix IC for a copy of the General Specification.)

2.3.3 EVALUATION OF DELIVERED UNITS

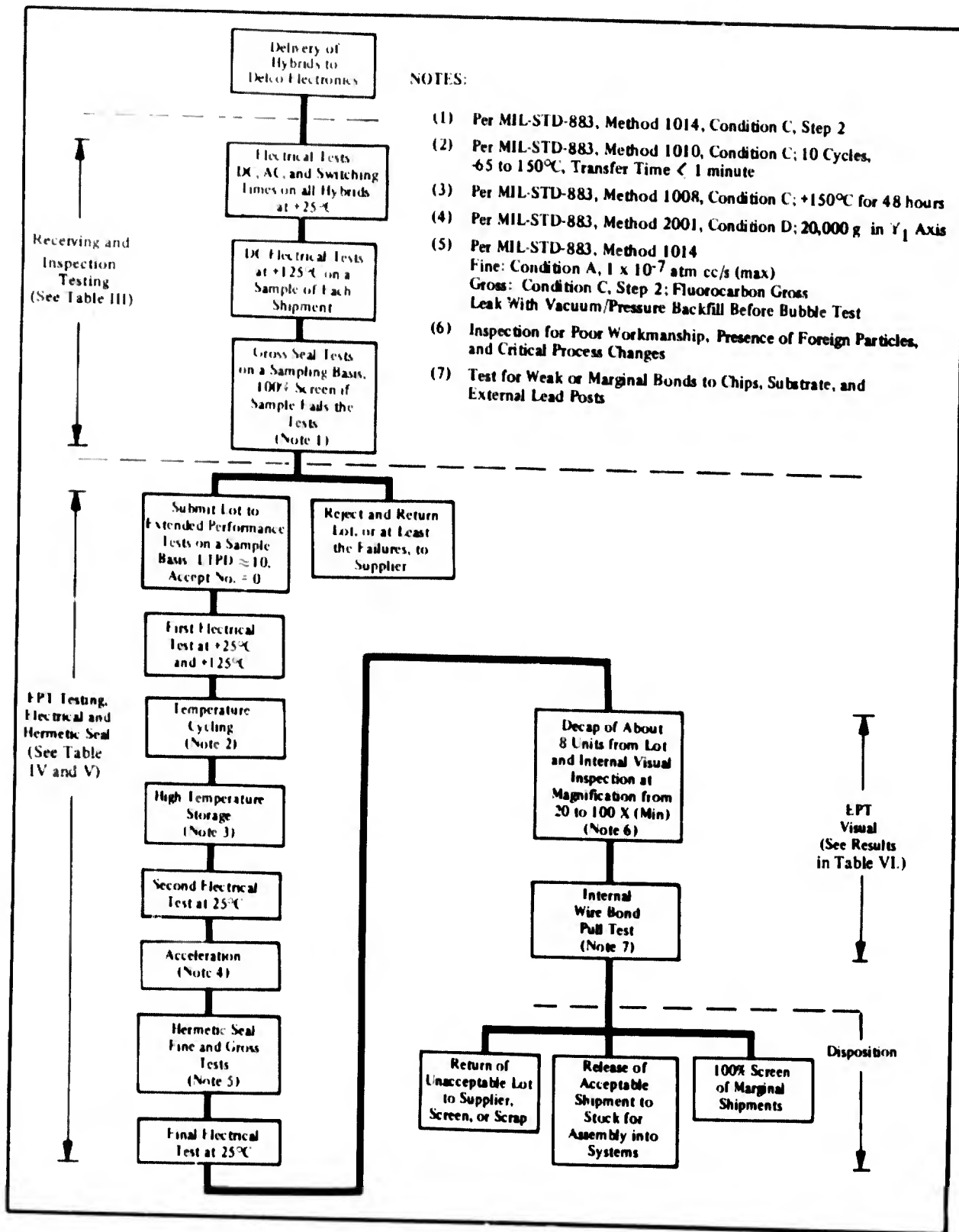
Upon receipt of supplier shipments at Delco Electronics, each unit involved in the study entered the in-plant test cycle depicted in Figure 7. Initial tests were performed in receiving-inspection; these results are summarized in Table III. Hybrid microcircuits that passed Receiving and Inspection were then exposed to Extended Performance Testing (EPT) in the laboratory by personnel trained and experienced in the processing, manufacture, test, and evaluation of semiconductor devices. Table IV summarizes the EPT sampling basis and the overall results obtained. As shown in Figure 7, the EPT portion involved two distinct phases:

1. Environmental cycling of samples, interrupted by electrical and leak tests, and terminated by a final electrical test. Results are shown in Table V.
2. Internal visual inspection for poor workmanship, presence of foreign particles, critical process changes, and bond pull tests. Results are shown in Table VI. (See Appendix II for the same test results, organized by the circuit type and manufacturer.)

Units found to be acceptable by EPT were then released to stock for use in production assemblies. Subsequent electrical testing of assemblies revealed occasional faulty hybrids. Table VII describes hybrid microcircuit failures that have undergone the processing, testing, and screening of Figures 6 and 7, but later failed during assembly or in the field. The 74 units discussed constitute all of the failures which were subjected to detailed Failure Analysis.

2.3.4 CONCLUSIONS ON PRODUCTION TEST RESULTS

The observed on-aircraft failure rate of hybrid microcircuits subjected to this controlled processing and testing through November 1969 was 0.465 failures per million hours. This failure rate, which has a 90 percent confidence interval of 0.218 to 0.874 failures per million hours, pertains to hybrid microcircuits used on aircraft. The circuits involved were exposed to mechanical shock, vibration, temperature cycling, and all of the other environments present outside of the pressurized, temperature-controlled cabin of the vehicle.



NOTES:

- (1) Per MIL-STD-883, Method 1014, Condition C, Step 2
- (2) Per MIL-STD-883, Method 1010, Condition C; 10 Cycles, -65 to 150°C, Transfer Time < 1 minute
- (3) Per MIL-STD-883, Method 1008, Condition C; +150°C for 48 hours
- (4) Per MIL-STD-883, Method 2001, Condition D; 20,000 g in Y₁ Axis
- (5) Per MIL-STD-883, Method 1014
 Fine: Condition A, 1 x 10⁻⁷ atm cc/s (max)
 Gross: Condition C, Step 2: Fluorocarbon Gross Leak With Vacuum/Pressure Backfill Before Bubble Test
- (6) Inspection for Poor Workmanship, Presence of Foreign Particles, and Critical Process Changes
- (7) Test for Weak or Marginal Bonds to Chips, Substrate, and External Lead Posts

Figure 7. Production Test Procedure After Delivery

Table II. Group B Requirements

SUB-GROUP	EXAMINATION OR TEST	CONDITIONS	
		MIL-STD-883 METHOD	SPECIFIC CONDITIONS
1	Solderability	2003	
1	Temperature Cycling	1010, Condition C	Transfer Time: 1 Minute (max)
1	Thermal Shock	1011, Condition A	0, +5, -0 to 100 to +0, -5°
1	Hermetic Seal	MIL-STD-202 Method 112, Condition C; or MIL-STD-883 Method 1014, Condition A or B and C	Procedure I, II, III, or IV for Fine Leak. Condition A or B for Gross Leak. Backfill Pressure 28 psig. Min Leakage Rate = 10 ⁻⁸ atm-cc/s (max)
1	Moisture Resistance	1004	Initial Conditioning May be Omitted
2	Shock	2002, Condition B	1,500 g, 5 Blows Nonoperating, 0.5 ms, Orientations X ₁ , Y ₁ , Z ₁ , Y ₂ , Z ₂ , 20 Blows Total
2	Vibration Fatigue	2005, Condition A	Nonoperating
2	Vibration, Variable Frequency	2007, Condition A	
2	Constant Acceleration	2001, Condition D	20,000 g, Orientation X ₁ , Y ₁ , Z ₁
3	Lead Pull (for Flat Packages only)	2004, Condition A	12 oz Axial Pull, 30 s
3	Bending Stress (for Flat Packages Only)	2004, Condition B ₂	2 Bends
4	Barometric Pressure	1001	
5	Salt Atmosphere	1009, Condition A	
6	Hi Temperature Voltage Stress	1005, Condition A	
6	Nonoperating Hi Temperature Life	1008, Condition C	
7	Operating Life	1005, Condition D	

Table III. Receiving and Inspection Testing of Incoming Hybrids

TYPE OF TEST	UNITS* TESTED	FAILURES		RANGE** OF THE FAILURES (%)
		QTY	% AVE	
Electrical Measurement: ● AC, DC, and Switching at +25°C ● DC at +125°C	103,887	2,423	2.33	0.23 to 9.02
	18,176	633	3.48	0 to 12.07
Hermetic Seal (MIL-STD-883): ● Flux [†] , Method 1014, Condition A 1 x 10 ⁻⁷ atm-cc/s (max) ● Gross, Method 1014, Condition C, Step 2	8,318	164	1.97	0 to 6.02
	37,715	1,261	3.34	1.9 to 14.3

Notes:
*124,832 Microcircuits Tested During 1967, 1968, and First 8 Months of 1969.
**Various Different Part Types and Manufacturers
†Flux Seal Test Run Only When Lot is Screened Due to EPT Failure

Table IV. Sampling Basis Used for EPT and Overall Results Obtained

EPT SAMPLING AND TEST ITEM	DATA
SAMPLING	
Total Population Subjected to EPT Sampling	67,760
No. of Lots Covered in Sampling*	296
Size Range of Lots Sampled	2 to 2,264
Total No. of Samples Selected	3,484
Size Range of Samples Taken	1 to 24
Samples Failed During EPT (See Table IV)	312 (9%)
Samples Visually Rejected After Passing Electrical and Seal Test (See Table V)	138 (4%)
Total Lots Accepted	179 (65%)
Total Lots Rejected	117 (35%)

*Represents 8 Suppliers, 19 Construction Types, and 9 Part Numbers, Spanning 1967, 1968, and 2/3 of 1969.

Table V. EPT Postelectrical and Hermetic Seal Test Failures

AFFECTED AREA	FAILURE MECHANISM	NO. OF FAILURES	MEANS OF ELIMINATING PROBLEM
Internal Wiring	Shorted after Y ₂ Axis Acceleration at 20,000 g. Due to Uninsulated Crossovers (See Figure 1)	19	String at Design Review Before Using Part
	Open Internal Bonds	15	Improve Control of Bonding Equipment. Improve Pre-cap Internal Visual Inspection. Perform 40,000 g Acceleration in Y ₁ Axis After All Screening Other Than Hermetic Seal Testing. Pull Test Bonds During Processing and During Lot Qualification Testing.
	Large Increase in Saturation Voltage (Intermetallic Formation Around Bond)	1	
	Failed Electrical Suspect Resistive Bond	1	
	Subtotal	36	11%
Chip	Failed Reverse Current & Breakdown Voltage After V-T Stress (Reverse Bias Life)	11	Require Supplier to Use Proper Shutdown Procedure After V-T Stress (Reduce Temperature to Room Ambient Before Removing Bias). Test Units Within 8 Hours After V-T Stress.
	Failed Electrical Test Unresolved	3	Cause Unknown
	Failed Leakage Current	1	Cause Unknown
	Subtotal	15	5%
Packaging	Failed Gross Seal Only	128	Require Supplier to Test Gross Seal per MIL STD-883, Method 1014, Test Condition C, Step 2. Also Specify That Supplier Use More Rugged Packaging.
	Failed Fine Seal Only	49	Require Supplier to Test Fine Seal per MIL STD-883, Method 1014, Test Condition A or B. Also Specify That Supplier Use More Rugged Packaging.
	Failed Both Fine & Gross Seal	47	Same as Above for Gross & Fine Seal Problem
	Loose Ceramic Substrate	20	Improve Bonding of Substrate and Control (Actual Solution was to Drop This Supplier.)
	Loose Chip	8	Eliminate Glass Frit or Pyroceram Bonding of Chips to Case. Accelerate Parts in Y ₁ Axis at 40,000 g to Reduce Problems. Perform Chip Bond Tests During Processing and Lot Qualification Testing
	Cover Fell Off	2	Same as for Gross Seal Problem.
	Failed Gross Seal & Electrical	1	Same as for Gross Seal Problem.
	Failed Gross Seal & Loose Ceramic Substrate	1	Same as for Gross Seal Problem.
	Cracked Chip	1	Improve Chip Mounting. Improve Internal Pre-cap Visual
	External Lead Fell Off	1	Improve External Visual Inspection of Leads, and a Sample Pull Test of Leads, by Supplier
	Failed External Lead Pull	1	Same as Above
	Subtotal	259	83%
Miscellaneous	Open Nichrome Thin Film Resistor	1	Improve Pre-cap Internal Visual Inspection.
	Failed Electrical Due to Scratched Aluminum Metallization	1	Improve Pre-cap Internal Visual Inspection
	Subtotal	2	1%

Table VI. Units Visually Rejected After Passing EPT Postelectrical and Seal Tests

AREA AFFECTED	REASON FOR REJECTION	NO. OF REJECTS	MEANS OF ELIMINATING PROBLEM
Internal Wiring	Units Have Unacceptable Design. Leads in Danger of Shorting to Common Anode and Common Cathode Side.	52	Stringent Design Review Before Using Part.
	Drooping Leads, in Danger of Shorting	10	More Stringent Design Review. Pre-cap Visual at an Angle to Note Proximity of Leads to Chips in More than One Axis. Better Control of Internal Lead Bonding System.
	Bonds Ball-Bonded Second Time, Over First Bond.	7	Study Program to Determine if Reworked Bonds Pose an Added Risk.
	Poor Bonding; Looks Unacceptable.	7	Improve Control of Bonding Equipment. Improve Pre-cap Internal Visual Inspection. Perform 40,000 g Acceleration in Y1 Axis After All Screening, Except Hermetic Seal Testing. Pull Test Bonds During Processing and During Lot Qualification Testing.
	Marginal Bond; Pulled Off at Less than 1.5 gram.	3	
	Slipped Gold Ball Bonds (Bonders Moved While Making Ball Bond).	4	
	Damaged Internal Lead.	1	Improve Pre-cap Internal Visual Inspection.
	Subtotal		94 = 61%
Chip	Scratched Metalization.	14	Improve Pre-cap Internal Visual Inspection.
	Crack in Chip Toward Junction, or into Metalization.	7	Same as Above.
	Foreign Material on Chip.	4	Same as Above.
	Corrosion of Aluminum Metalization.	2	Same as Above, Plus Seal Tests per MIL-STD-883, Method 1014, Test Condition A, or B and C.
	Diffusion Fault.	2	Improve Pre-cap Internal Visual Inspection.
	Chip Diced with an Extra Half Chip, Creating a Shorting Hazard.	1	Same as Above.
	Transistor Almost Shorted.	1	Same as Above.
	Subtotal		31 = 22%
Packaging	Chip Poorly Attached.	1	Improve Pre-cap Internal Visual.
	External Leads Damaged (Worn Down from Supplier Rework).	5	Forbid Supplier to Sand Excess Solder From Final Seal of Package, or to Try to Grind Glass Runout Off of Oversize Package.
	Misaligned Covers.	3	Improve Supplier Jig for Holding Cover in Place During Sealing.
Subtotal		9 = 7%	
Miscellaneous	Used Thick-Film Resistors, Instead of Approved Thin-Film.	6	Eliminated Supplier Because of Many Problems.
	Metal Flake(s) in Unit.	6	Improve Pre-cap Internal Visual and Precautions in Handling Prior to Capping.
	Resistor (Thin-Film) Deposition Flaw	1	Improve Pre-cap Internal Visual.
	Loose Gold Wire in Unit.	1	Same as Above.
Subtotal		14 = 10%	

Table VII. Summary of Subsequent Assembly and Field Failures Attributed to Hybrid Microcircuits

AFFECTED AREA	FAILURE MECHANISM	NO. OF FAILURES	MEANS OF ELIMINATING PROBLEM
Internal Wiring	Leads Shorting to Edge of Chip.	17	More Stringent Design Review and Pre-cap Internal Visual at an Angle to Note Proximity of Leads to Chips in More than One Axis. Better Control of Lead Bonding System.
	Lead Broke Due to Tension Caused by Varnish Coating Over Chips and Wires.	7	Eliminate Varnish Passivation
	Loose Gold Ball Bond.	8	Improve Control of Bonding Equipment. Possibly Improve Pre-cap Internal Visual Inspection. (Failure Mechanism Being Studied Because of Lack of Definition of Cause.) Perform 40,000 g Acceleration in Y ₁ Axis After All Screening Other than Hermetic Seal Testing. Pull Test Bonds During Processing and During Lot Qualification Testing.
	Loose Gold Wire Bond. (Majority of Bonds Weak on All Chips).	7	
	Wire Bond Resistive.	4	
	Loose Ultrasonic Al Bond.	2	
	Leads Touching Metal Lid. Causing Short.	2	Improve Control of Bonding Equipment. Improve Pre-cap Visual at an Angle to Note Height of Leads in More than One Axis. Improve Design of Bonding System.
	Open Wire Due to Break at Neckdown of Stitch Bond.	1	Improve Control of Bonding Equipment. and Improve Pre-cap Visual Inspection.
Subtotal		48 = 65%	
Chip	Oxide Flaw. Causing Short.	5	Increase Burn-in Temperature from +25°C to +125°C. Apply More Stringent Internal Visual Pre-cap Inspection.
	Diffusion Flaw.	2	Improve Internal Pre-cap Visual.
	Scratched Metallization. Causing Short.	2	Improve Internal Pre-cap Visual.
	Excessive F-B Leakage Current.	1	Cause Unknown.
Subtotal		10 = 14%	
Packaging	Loose Chips.	7	Eliminate Glass Frit or Pyrocera Bonding of Chips to Case. Accelerate Parts in Y ₁ Axis at 40,000 g to Reduce Problem. Perform Chip Bond Tests During Processing and Lot Qualification Testing.
	Open Thin-Film Nichrome Resistor (Suspect Nonhermetic Seal)	2	Improve Gross Seal Testing up to MIL-STD-883.
	Cracked Chip.	1	Improve Chip Mounting. Improve Internal Pre-cap Visual.
	Glass Final Sealing Material Causing Shunt Path.	1	Control Glass Final Seal Material.
	Damaged Case.	1	Use More Care in Handling.
Subtotal		12 = 16%	
Miscellaneous	Metallic Contamination.	2	Improve Internal Pre-cap Visual. Use More Care in Handling Prior to Capping.
	Short Between Thick Film Conductors on Substrate	1	Improve Internal Pre-cap Visual and Electrical Isolation Test.
	Failed Electrical Toggle Test (Flip-Flop)	1	Perform 100 Percent Toggle Tests.
Subtotal		4 = 5%	

It may be concluded, from the data in this section, that there is fallout during receiving-inspection and sample environmental testing, even with 100 percent screening requirements imposed on the suppliers. It also may be concluded that if this inspection and testing are properly utilized to assure that initial designs are sound, manufacturing and processing are properly controlled, and finished parts are adequately screened and tested, hybrid microcircuits can provide reliable, densely packed circuitry. To control this desired sequence requires a complete set of specifications, from initial procurement to final high-level testing, with rigid quality monitoring to assure full compliance.

One problem area which proved to be not easily amenable to user controls was the quality of internal wire bonds of the flatpackages. Manufacturers must clearly place more emphasis on obtaining consistently reliable wire bonding. This problem might be avoided by employing beam-leaded chips, or some other chip mounting technique which does not involve the fine interconnect wires and associated bonds.

Since this study established that the screening requirements, which are equivalent to the Class B screening of Method 5004 of MIL-STD-883, imposed on the suppliers were not 100 percent effective in eliminating all faulty hybrids, a better screening system was required. In an attempt to establish such a system, the stepped stress testing discussed in the next section was subsequently performed.

2.4 STEPPED STRESS TESTING PROGRAM

2.4.1 BACKGROUND

The test environments imposed during the supplier's processing procedure were found to be inadequate for their intended purpose; therefore, a program of stepped stress testing was undertaken to determine those test levels which, when imposed, would identify and prevent shipment of defective hybrid microcircuits. The hybrid microcircuits used for this stepped stress testing program were production program units. The overall results of this testing are shown in Figures 8, 9, and 10, for the hybrids from Manufacturers A, B, and F, respectively.

2.4.2 DESCRIPTION OF HYBRIDS SELECTED

The hybrid microcircuits selected for the stepped stress testing were of three different package sizes and from three different suppliers, each of whom employed different manufacturing techniques.

Results of stepped stress testing of a Memory Hybrid Switch from Manufacturer A are charted in Figure 8. A photomicrograph of the part is shown in Figure 4, and a schematic diagram in Figure 3. a. Transistors Q_3 and Q_4 of this circuit switch 450 milliamperes, with a maximum saturation voltage of 500 millivolts. The inputs are driven by TTL logic levels. The flatpackage is $1/4" \times 3/8"$ and has a gold plated

kovar bottom and top. The side walls are of glass, and the package is hermetically sealed by soldering the top onto a gold plated kovar window frame in a belt furnace. The chips are alloyed down to a ceramic substrate which has thick-film gold conductors on the top and thick-film gold on the bottom. The ceramic substrate is alloyed to the gold plated kovar package bottom. The four resistors are thick-film cermet. The wire interconnects are made with a combination of 0.7- and 1.0-mil gold flying wires, with thermocompression ball bonds on one end and wedge bonds on the other. The semiconductor chip metallization is thin-film aluminum, and the lead frame is gold plated kovar.

Results obtained with a Ladder Switch and Driver from Manufacturer B are shown in Figure 9. Figure 2 shows a photo and schematic of the actual hybrid. The Ladder Switch and Driver is driven by TTL logic levels at pin 7, and the output at pin 3 switches between ground and a reference voltage at pin 2. Transistors Q_1 and Q_2 operate in the inverse mode, with a 2-millivolt maximum allowable offset without a load, and 4.2 millivolts (or 30 ohms maximum "on" resistance) with a $20k\Omega$ load. Manufacturer B uses a $1/8" \times 1/4"$ flatpackage with a ceramic bottom, which also serves as the substrate, and a gold plated kovar top. The package side walls are of glass, and the unit is hermetically sealed by soldering the top to a gold plated kovar window frame in a belt furnace. The chips are alloyed down to the thick-film gold on the substrate. The five resistors are thin-film nichrome deposited on silicon dioxide on a single silicon chip. The interconnects are made with 1.0-mil gold flying wires using thermocompression ball bonds on one end and wedge bonds on the other. The chip metallization is thin-film aluminum, and the lead frame is gold plated kovar.

Test results on a Triple Operational Amplifier from Manufacturer F are shown in Figure 10. Figure 11 shows a schematic diagram and a photomicrograph of the circuit. The $1" \times 1"$ flatpackage is made of ceramic and is sealed by epoxying its cover to a gold plated sealing ring. The substrate is glazed ceramic with thin-film tantalum resistors and aluminum conductors deposited on top of it. The substrate is epoxy bonded to the package bottom. The circuit uses 6 MOS chip capacitors, which are epoxyed down to the glazed ceramic. The 9 transistor chips are alloyed to gold plated kovar tabs, which in turn are epoxy bonded to thin-film aluminum pads on the substrate. The wire interconnect is a combination of ultrasonically bonded 2.5-mil aluminum wire and thermocompression-bonded 0.7-mil gold wire, with ball bonds on one end and wedge bonds on the other. The transistor chip metallization is thin-film aluminum, and the lead frame is gold plated.

2.4.3 SUPPLIER PRESHIPMENT REQUIREMENTS

Each hybrid for this test program was procured with the requirement that it be 100 percent screened before shipment to Delco Electronics. For example, the Memory Hybrid Switch from Manufacturer A and the Ladder Switch and Driver from Manufacturer B were procured with the screening requirements described in Figure 6.

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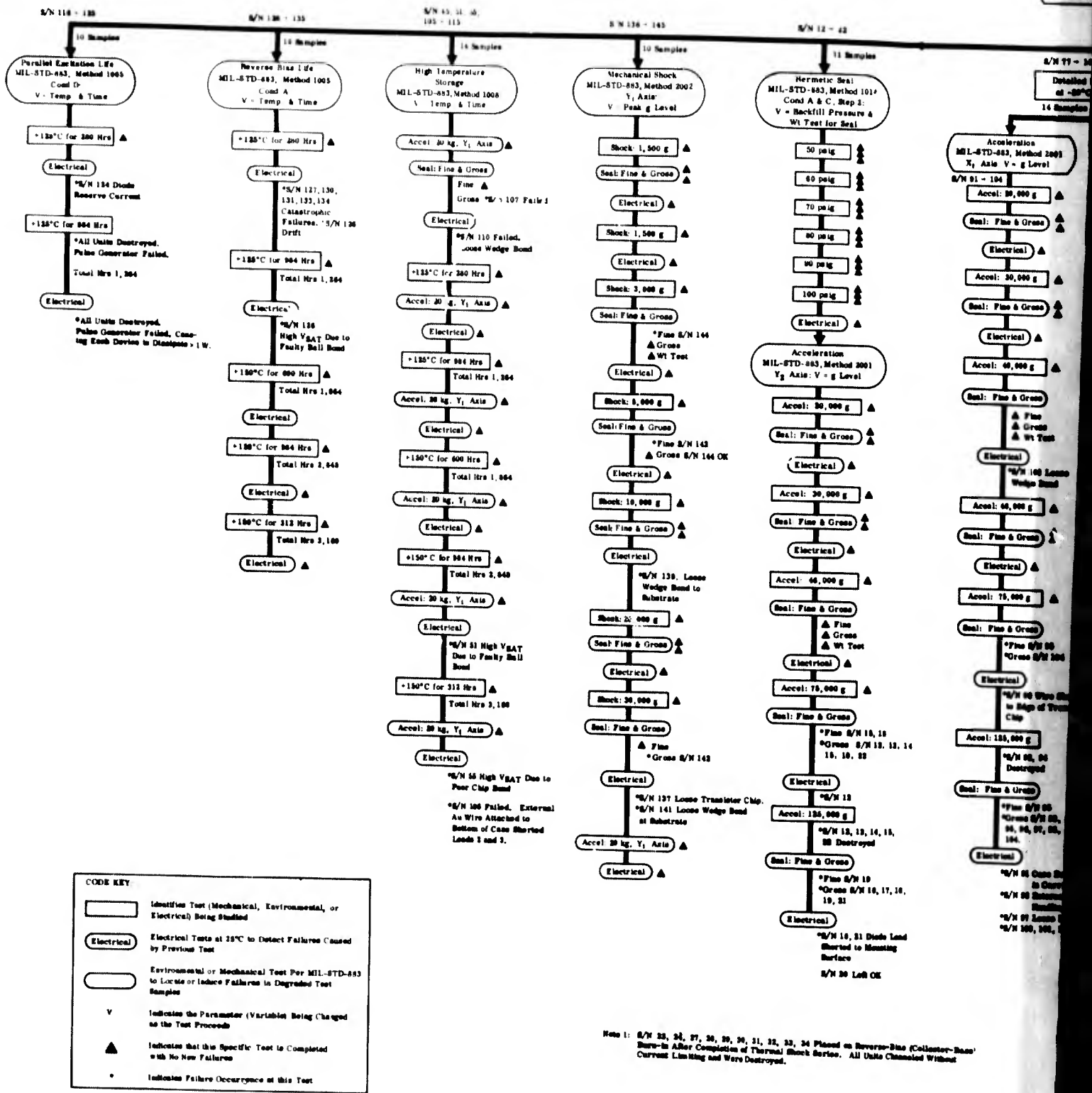


Figure 8. Stepped Stress Test Result

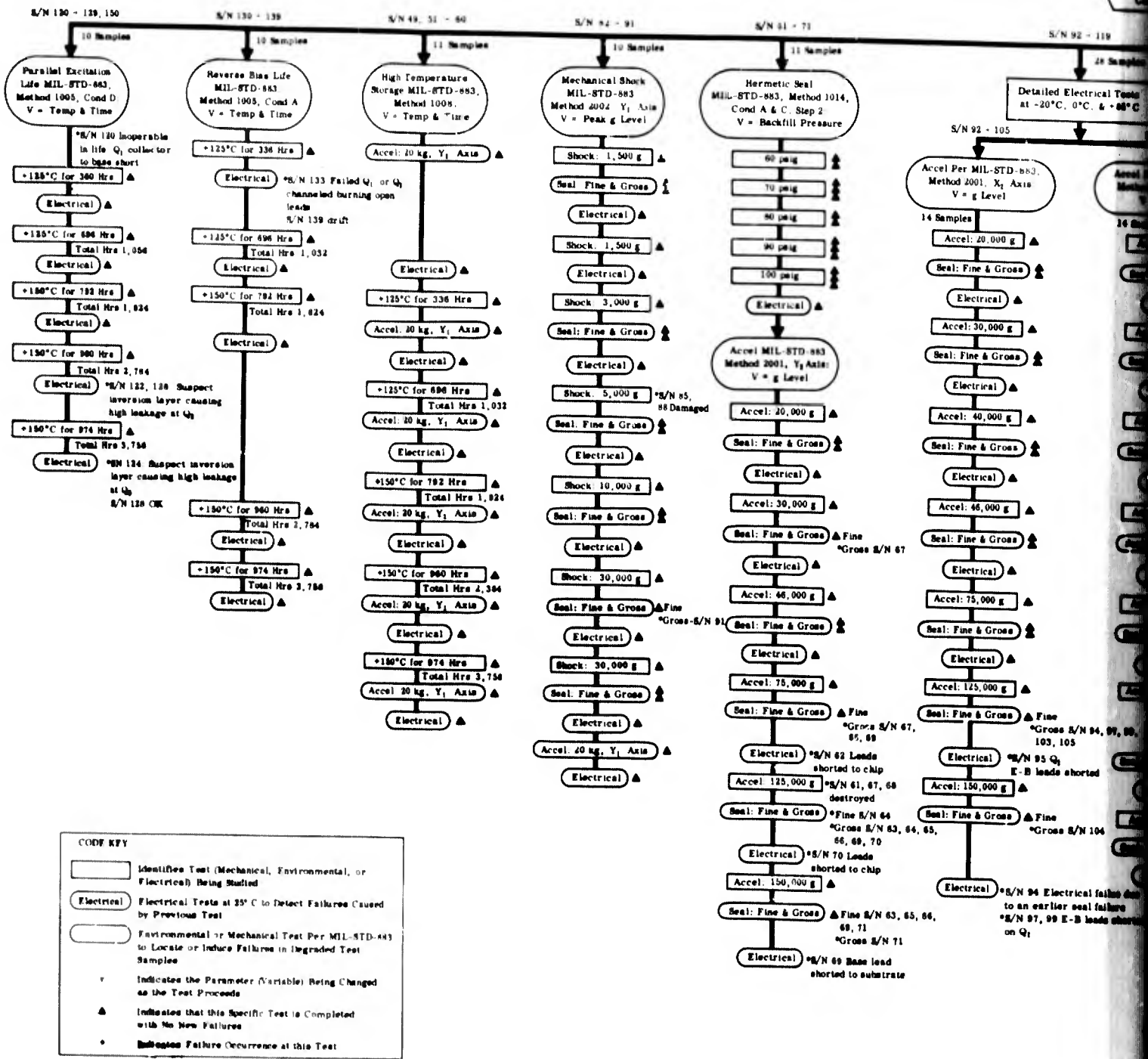
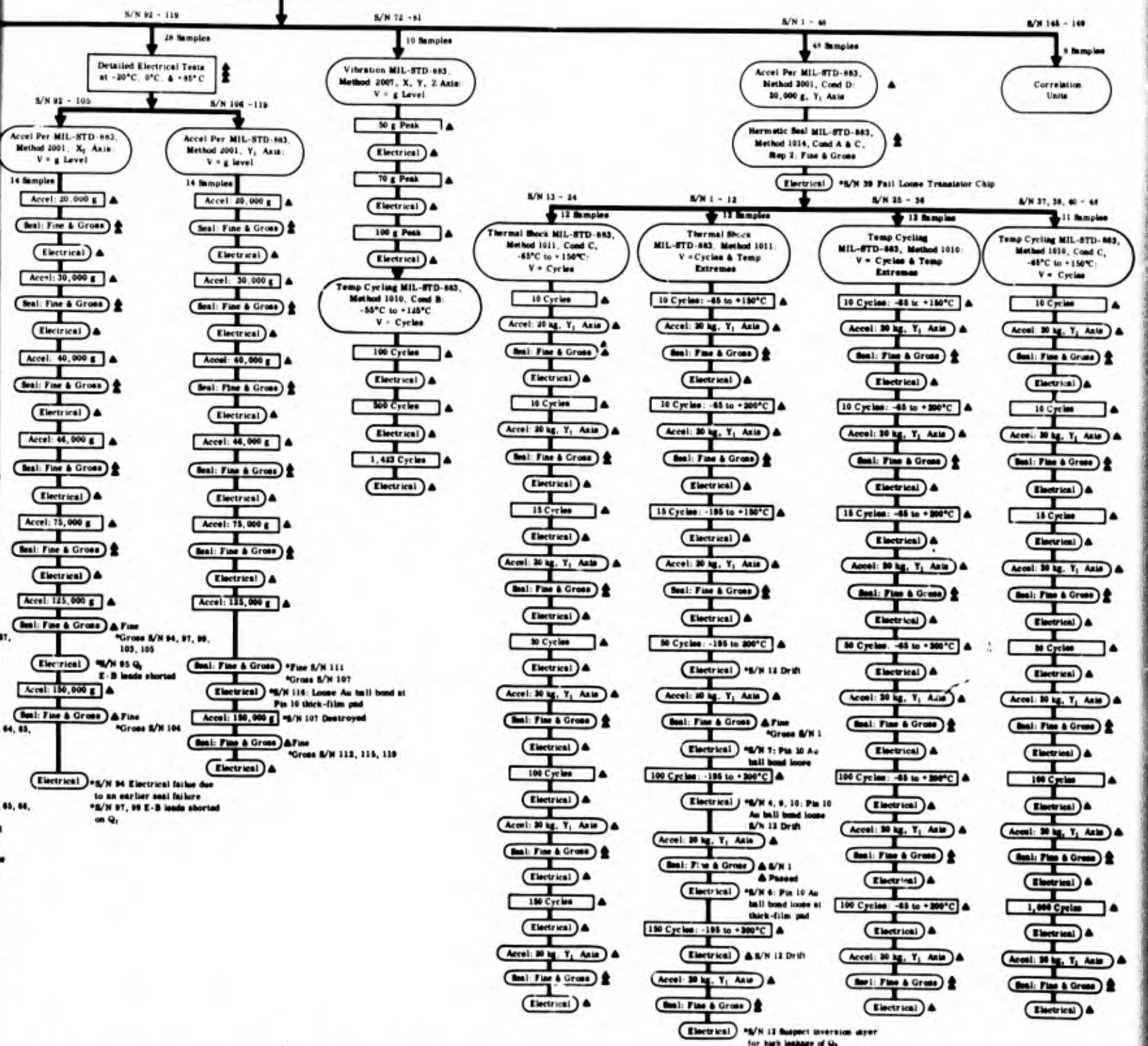


Figure 9. Stepped Stress Test Results, Ladder

Detailed Electrical Tests at +25°C, -55°C, and +125°C
 ▲ -25°C
 ▲ -55°C
 * +125°C, S/N 50 Failed: Emitter-Base Short Due to Gold Particle.

150 Samples
 Hermetic Seal Tests
 A. Fine - Per MIL-STD-883, Method 1014, Cond A
 B. Gross - Per MIL-STD-883, Method 1014, Cond C, Rep 2



Test Results, Ladder Switch and Driver from Manufacturer B

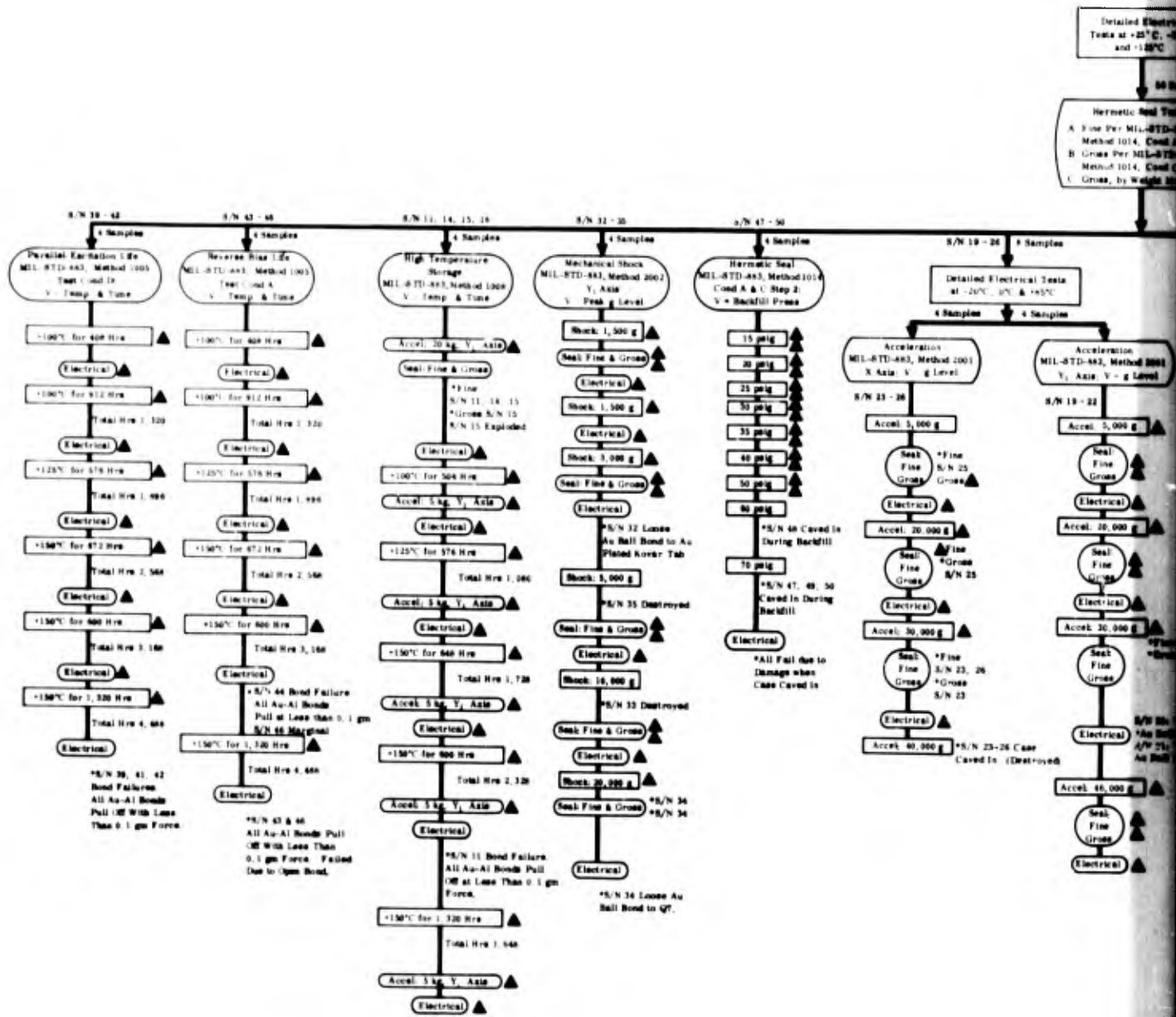
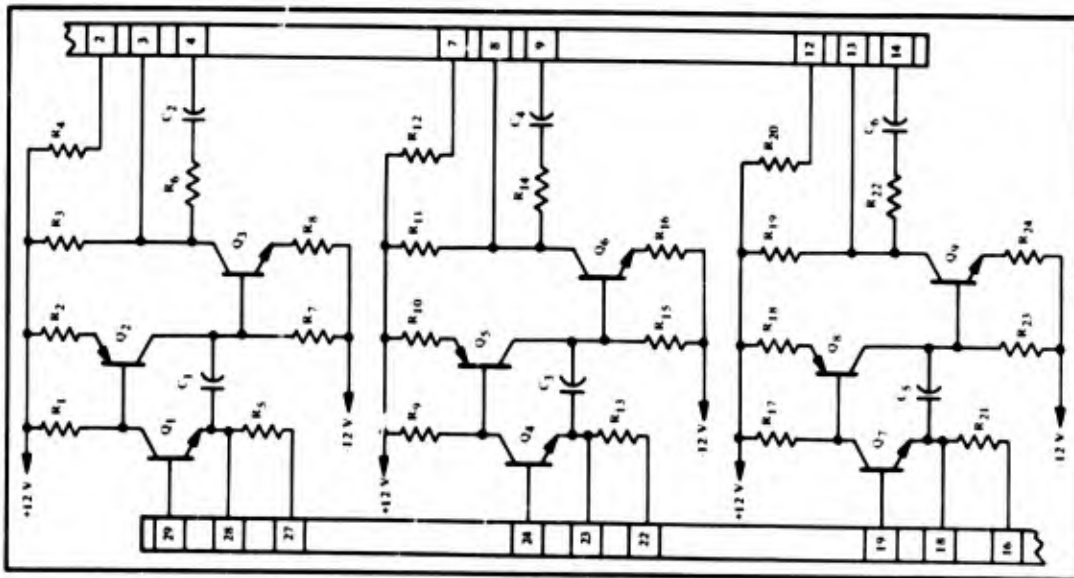


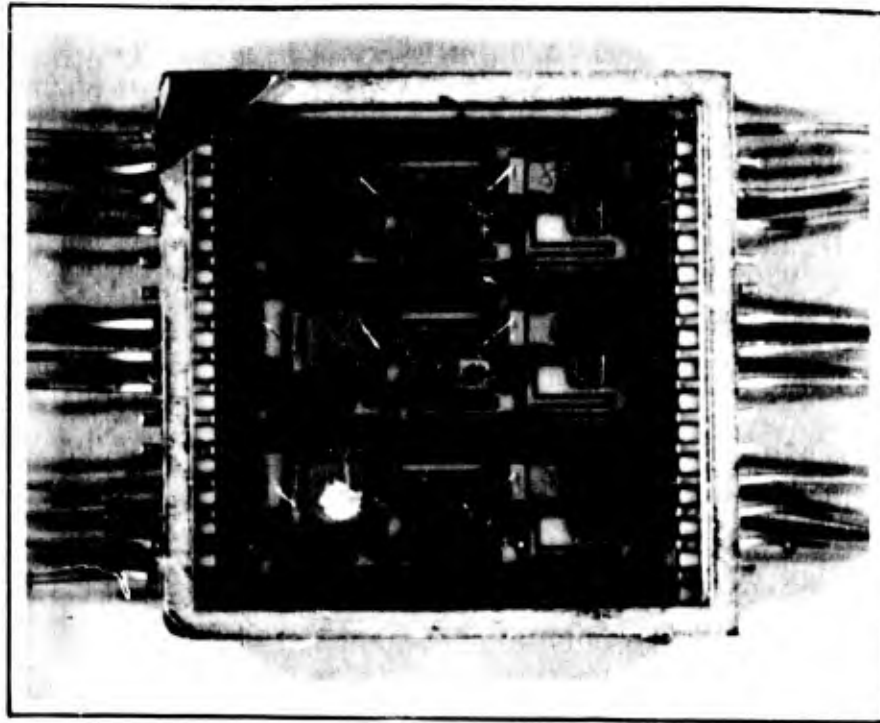
Figure 10. Stepped Stress Test Results, Th

A

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a. Schematic



b. 1" x 1" Flatpack

Figure 11. Triple Amplifier, Thin-Film from Manufacturer F

(The actual procurement documents used are in Appendix I of this book.) Manufacturers A and B are suppliers with whom Delco Electronics has had years of experience, and their hybrids received no testing at Delco Electronics prior to entering the testing sequences described in Figures 8 and 9.

The thin-film Triple Operational Amplifiers were procured off-the-shelf from Manufacturer F, a supplier with whom Delco Electronics has had no previous experience. However, the company has made many hybrid thin-film circuits. This particular hybrid contains three, identical, ac-coupled, operational amplifiers that use external feedback networks for gain control, and are suitable for providing stabilized gain from 0 to 40 dB, and for implementing active bandpass filters. The unit operates with plus and minus 12-volt power supplies. The manufacturer stated that he performs the following 100 percent screens on each of these hybrid microcircuit amplifiers:

- Operating burnin: 48 hours at 85°C,
- Temperature cycling: 15 cycles, -55°C to +95°C,
- Acceleration testing: Up to 20,000 g,
- Hermetic seal testings: fine leak at 1×10^{-7} atm cc/s (max), and a gross leak bubble test,
- Electrical testing.

2.4.4 EVALUATION OF DELIVERED HYBRIDS

2.4.4.1 Initial Testing

Upon receipt at Delco Electronics, all units to be subjected to stepped stresses were electrical tested at +25°C, -55°C, and +125°C. The Memory Hybrid Switch and Ladder Switch and Driver were electrical tested in accordance with parameters described in the SCD (listed in Appendix I). The Triple Operational Amplifier had its input impedance, output impedance, power supply drain currents, gain at 1 kHz, 6 kHz, 25 kHz, 100 kHz and 200 kHz, and noise voltage parameters measured on each unit.

In addition to the above functional parameters, each circuit received special measurements on all available resistors and transistors. Each circuit was also continuity tested to help pinpoint where failures occurred in the circuit, to expedite later failure analysis. Electrical parameters test data were logged at each electrical test point. The testing was performed on an automatic integrated circuit test system having dc, ac, and switching time capability at temperatures of -55°C to +150°C. After initial electrical testing, the parts underwent hermetic seal testing. After this, the parts were divided into subgroups preparatory to the various stepped stress tests.

The results of the initial testing are shown at the very top of Figures 8, 9, and 10. Each manufacturer's hybrids experienced some fallout during this phase. The initial tests were specifically performed to assure that the parts met all electrical specifications prior to initiating stress testing.

2.4.4.2 Temperature Cycling Evaluation

Units in the temperature cycling and thermal shock subgroups received a 20,000 g acceleration in the Y_1 axis, and another hermetic seal test prior to entering the stepped stress tests. These particular tests were performed to assure that the initial parts entering test were properly screened. As shown on the right side of Figures 8, 9, and 10, each manufacturer's product had fallout due to faulty wire bonds, poor chip bonds, weak packaging, or loose gold particles.

2.4.4.2.1 Temperature Cycling With Increasing Number of Cycles

Figure 12 shows test results for all three manufacturers' units when temperature is cycled with an increasing number of cycles. Each stress series was begun at 10 temperature cycles, from 15 minutes in low temperature air to 15 minutes in high temperature air, with a transfer time of less than one minute. The hybrids from Manufacturers A and B were cycled from -65°C to $+150^{\circ}\text{C}$, and that of Manufacturer F from -55°C to $+125^{\circ}\text{C}$. After each series of temperature cycles, additional tests were performed to determine if the parts had degraded, or failed catastrophically. After the initial 10 cycles, the parts from Manufacturers A and B were acceleration tested at 20,000 g in the Y_1 axis to destroy degraded substrate and chip and wire bonds.

After acceleration, fine and gross hermetic seal tests were performed to determine if the hermetic seal had been destroyed by the temperature cycling. Next, an electrical test was performed to detect destroyed units. The hybrids from Manufacturers A and B survived 1,185 temperature cycles with no failures due to temperature cycles, acceleration tests (6), hermetic seal tests (6), or electrical tests (10). There were 12 samples from Manufacturer A, and 11 samples from Manufacturer B.

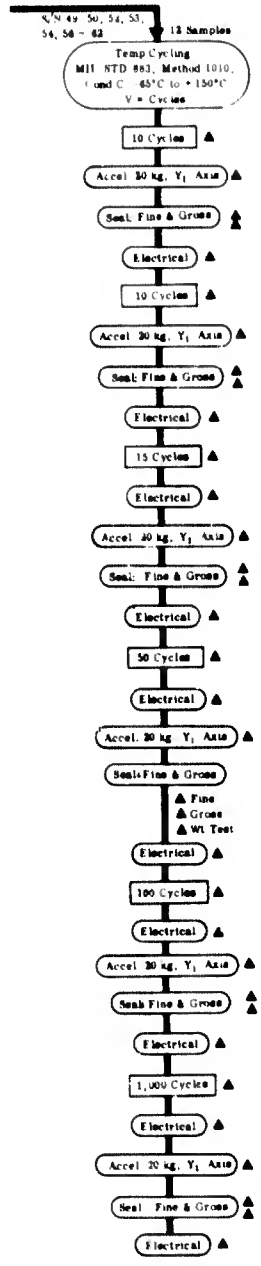
The hybrids from Manufacturer F were accelerated at 5,000 g in the Y_1 axis instead of 20,000 g, the level that appeared to damage the 1" x 1" flatpackage seal. Four of Manufacturer F's packages lost their hermeticity during 1,206 temperature cycles. No electrical failures occurred. A failure is defined as a hybrid microcircuit that exceeds any of the electrical parameter limits, or fails hermetic seal testing.

2.4.4.2.2 Temperature Cycling with Increasing Number of Cycles and Increasing Spread of Temperature Extremes

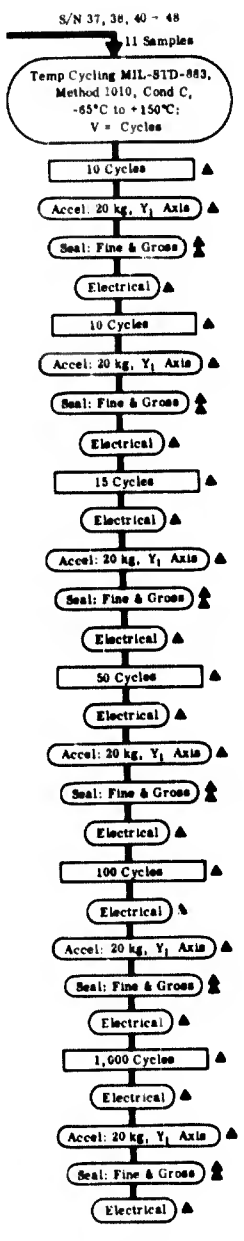
Figure 13 shows the test results for temperature cycling with an increasing spread of temperature extremes. The testing sequence is similar to that in Figure 12. Manufacturer A's parts had five failures after 285 temperature cycles, beginning at

CODE KEY:

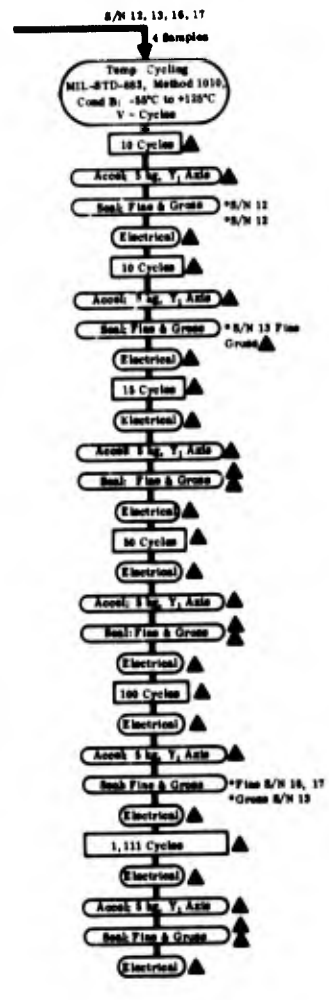
- ▭ Identifies Test (Mechanical, Environmental, or Electrical) Being Studied
- Ⓜ Electrical Tests at 25°C to Detect Failures Caused by Previous Test
- Environmental or Mechanical Test Per MIL-STD-883 to Locate or Induce Failures in Degraded Test Samples
- V Indicates the Parameter (Variable) Being Changed as the Test Proceeds
- ▲ Indicates that this Specific Test is Completed with No New Failures
- Indicates Failure Occurrence at this Test



Mfg. A






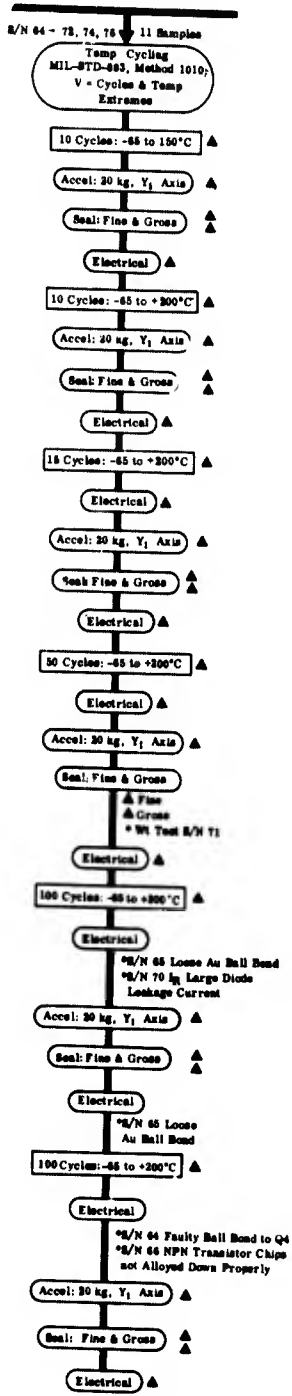
Mfg. B



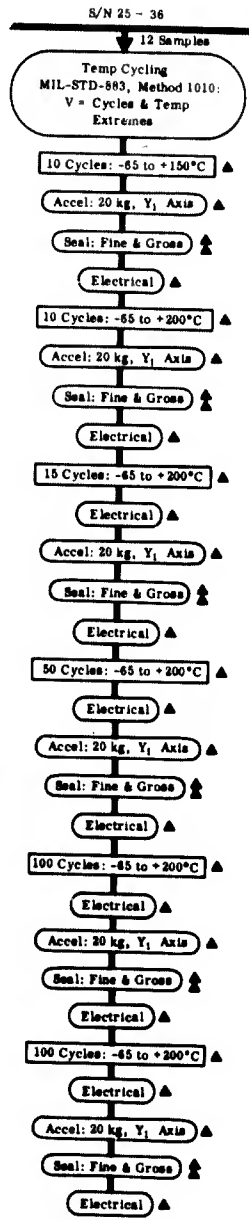
Mfg. F

Figure 12. Temperature Cycling with Increasing Number of Cycles

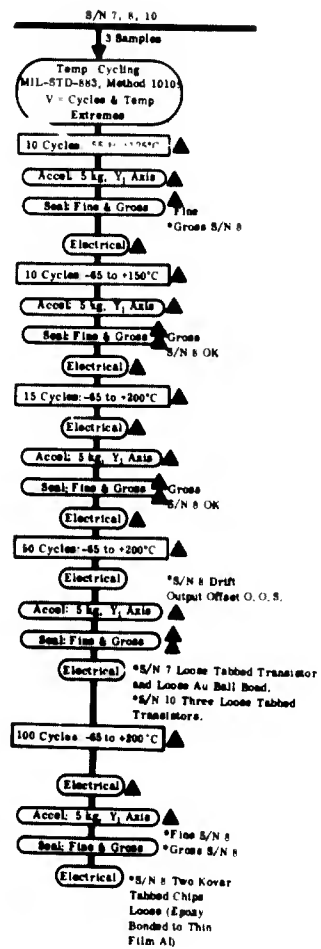
CODE KEY:	
	Identifies Test (Mechanical, Environmental, or Electrical) Being Studied
	Electrical Tests at 25° C to Detect Failures Caused by Previous Test
	Environmental or Mechanical Test Per MIL-STD-883 to Locate or Induce Failures in Degraded Test Samples
v	Indicates the Parameter (Variable) Being Changed as the Test Proceeds
▲	Indicates that this Specific Test is Completed with No New Failures
•	Indicates Failure Occurrence at this Test



Mfg. A



Mfg. B



Mfg. F

Figure 13. Temperature Cycling with Increasing Number of Cycles and Increasing Spread of Temperature Extremes

-65°C to +150°C and increasing to -65°C to +200°C. One of the failures was caused by a gross seal failure (S/N 71), two failures were due to gold ball bonds (S/N 64, 65), a fourth failure was due to a $V_{CE(SAT)}$ increase due to a poor chip bond (S/N 66), and the fifth failure was due to an increase in diode leakage current.

The gold ball bond in S/N 64 was intact when the part was decapped for failure analysis, but the suspect bond lifted away from the emitter of transistor Q4 with less than 0.1 gram force. Another ball bond to Q1 in S/N 64 lifted at less than 0.1 gram, but this weak bond did not show up as an electrical failure.

Serial Number 65 failed because of a loose gold ball bond to the emitter of Q3. This transistor $V_{CE(SAT)}$, at 450 milliamperes, was 0.347 volts during the initial electrical testing when the hybrids were received, and gradually increased up to 0.633 volts just prior to the bond opening. The chip bond was checked and considered intact. Figure 14, a photomicrograph of the chip, shows where the ball bond came off. Where the ball bond was located is shown by a black circle.

Serial Number 66 had an initial $V_{CE(SAT)}$, at 450 milliamperes, of 0.401 volts which, after undergoing 285 temperature cycles, increased to 0.607 volts. During the failure analysis, all wire bonds passed a bond pull test, with the wires breaking and the bonds remaining intact. Each transistor chip was then pushed with a fine wire. The NPN chips popped off with little applied force, while the other chips resisted and remained firmly attached.



Figure 14. Manufacturer A — Gold Ball Bond Failure

Serial Number 70 had a diode leakage current failure. The initial leakage current was 16 nanoamperes; and, as the test progressed, the value drifted up to 127 nA. During failure analysis, leakage current was again measured and this time the diode shorted, with a reverse current of 10 mA at 5 V. The high leakage, and finally the short, appeared to be related to the migration or diffusion of gold, from the gold ball bond, into the aluminum metallization on the diode.

Manufacturer B's hybrids experienced no failures during the 285 temperature cycles. Manufacturer F's hybrids, on the other hand, all failed during the 185 temperature cycles, beginning at -55°C to $+125^{\circ}\text{C}$ and increasing to -65°C to $+200^{\circ}\text{C}$. (See Figure 13.) Unit S/N 8 was failed for hermetic seal loss, plus a loosening of two of the kovar tabbed transistor chips which were epoxy bonded to the thin-film aluminum. There were also two other failures due to the epoxy bonds giving way and loosening transistors. Serial Number 7 also had a loose gold ball bond.

The stress testing described in Figure 13 served to eliminate faulty devices from Manufacturers A and B. The units from Manufacturer F failed due to the epoxy seal giving way and due to epoxy chip bonds failing. In the latter case, the epoxy bond used by this manufacturer was adjudged unable to withstand reasonable temperature cycling.

2.4.4.3 Thermal Shock

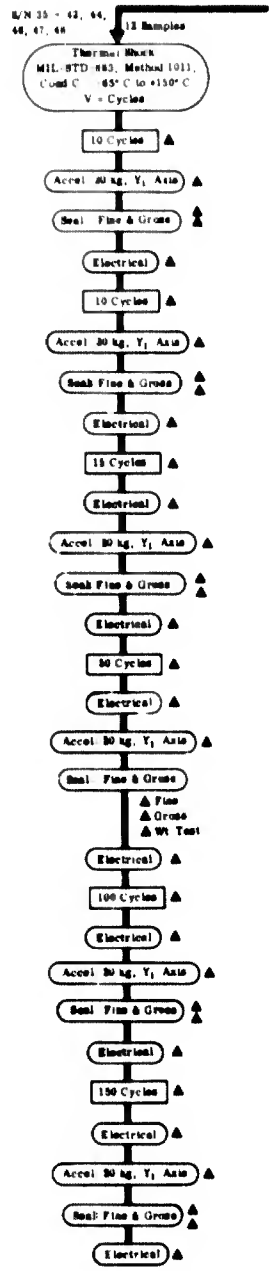
The thermal shock evaluation series was divided into two test groups (Figures 8, 9, and 10), one group for which the number of thermal shocks was the variable, and the other for which the number of thermal shocks, plus the spread of temperature extremes, was the variable. The liquids used for the shock baths were ice water for the 0°C , FC-78 for the low temperatures of -55°C and -65°C , and liquid nitrogen for the -195°C . For high temperature liquids, boiling water was used for the $+100^{\circ}\text{C}$, FC-40 for the $+125^{\circ}\text{C}$ and $+150^{\circ}\text{C}$, and high temperature silicone oil was used for the $+200^{\circ}\text{C}$.

2.4.4.3.1 Thermal Shock with Number of Cycles as the Variable

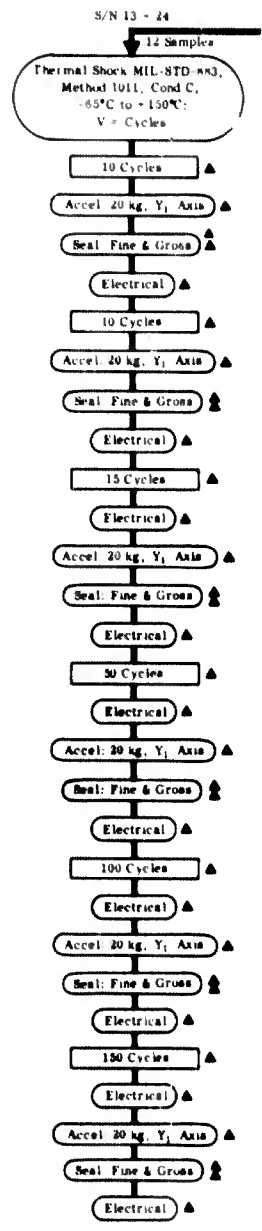
Figure 15 shows test results for thermal shock with number of temperature cycles as the variable. Hybrids from both Manufacturers A and B had no failures due to 335 cycles of thermal shock from -65°C to $+150^{\circ}\text{C}$. However, all three hybrids from Manufacturer F failed during 95 cycles of thermal shock from 0°C to $+100^{\circ}\text{C}$. The prime failure mechanism was loss of hermetic seal. Figure 16 shows photos of S/N 1 taken during failure analysis. During the failure analysis, the epoxy final seal was found to be somewhat soft, as though the water used in thermal shock had acted as a solvent and thereby contributed to the loss of hermeticity. Figure 16a shows long fiber strands in the epoxy used for the final seal. Figure 16b, c, and d show the results of the water entering the package and causing electrical failure, due to an open 2.5-mil aluminum wire (normally ultrasonically bonded to thin-film aluminum metallization).

CODE KEY:

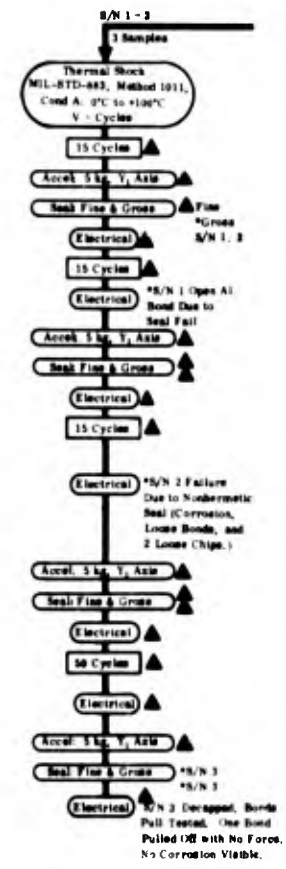
○	Identifies Test (Mechanical, Environmental, or Electrical) Being Studied
Ⓜ	Electrical Tests at 25° C to Detect Failures Caused by Previous Test
Ⓞ	Environmental or Mechanical Test Per MIL-STD-883 to Locate or Induce Failures in Degraded Test Samples
v	Indicates the Parameter (Variable) Being Changed as the Test Proceeds
▲	Indicates that this Specific Test is Completed with No New Failures
•	Indicates Failure Occurrence at this Test



Mfg. A



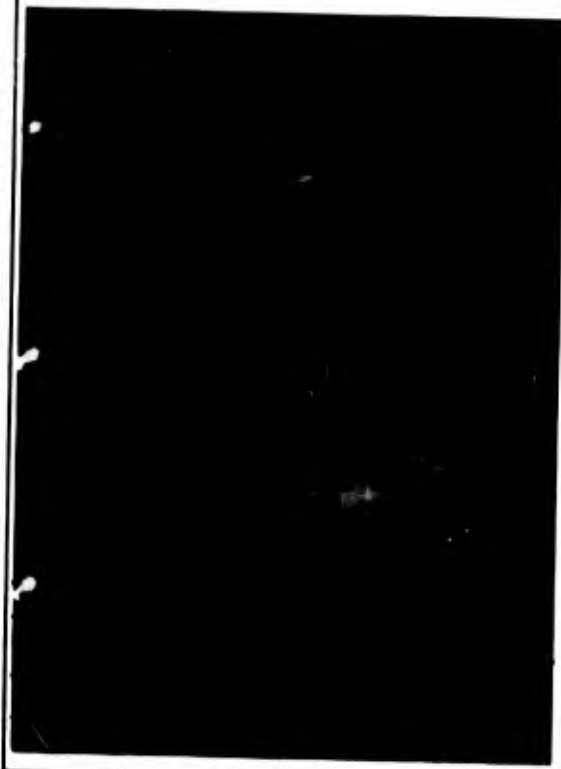
Mfg. B



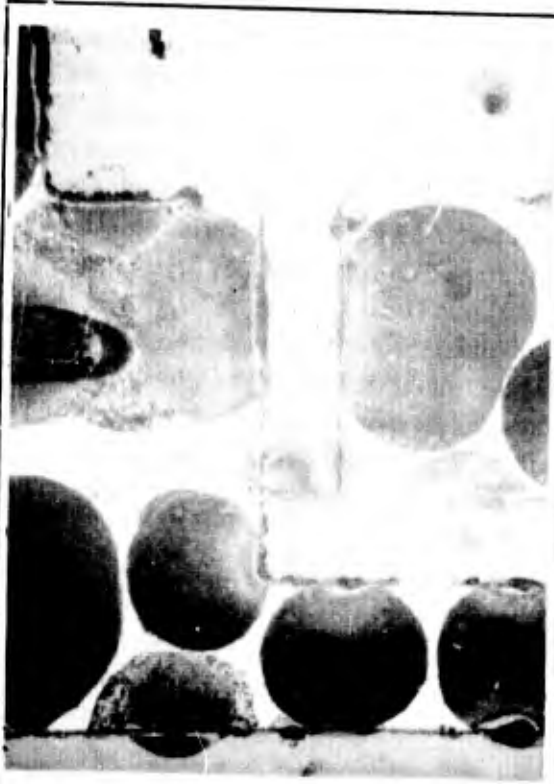
Mfg. F

Figure 15. Thermal Shock Evaluation with Number of Cycles as the Variable

a.) Strands Found in Epoxy Final Seal



b.) Corroded Thin-Film Aluminum Interconnects on Substrate, Due to Presence of Water



c.) Build-up of Material at Aluminum Bond-to-Aluminum Metallization, Due to Presence of Water



d.) Open Aluminum Wire Bond-to-Aluminum Metallization After Removal of Material Shown in (c).



Figure 16. Failed Hybrid from Manufacturer F.

2.4.4.3.2 Thermal Shock with Number of Cycles Plus the Spread of Temperature Extremes as the Variables

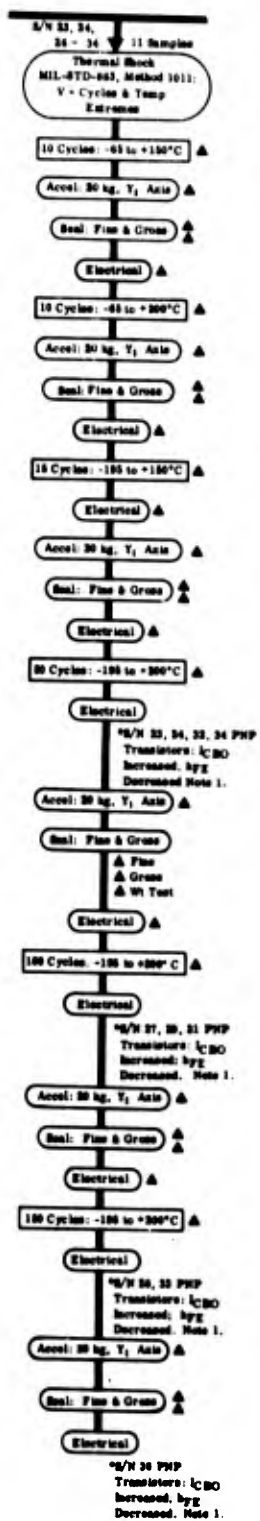
Figure 17 shows the results of thermal shocking the hybrids from Manufacturers A, B, and F with increasing numbers of cycles and with wider spreads for the temperature extremes. Manufacturer A's product had no hermetic seal failures, or acceleration failures, after 335 cycles of thermal shock beginning at -65°C to $+150^{\circ}\text{C}$ and proceeding to -195°C to $+200^{\circ}\text{C}$. Manufacturer A's hybrids did have 10 electrical failures out of the 11 hybrids tested. All ten failures were due to the PNP transistors, ICBO increasing until the hybrid exceeded the circuit leakage current limit. It was also noted that the beta of the PNP transistors decreased. Both of these parameters were unstable during the -195°C to $+200^{\circ}\text{C}$ shocks and hence were unpredictable. The parts acted as though they had channels due to an inversion layer. Because of these characteristics, the suspect parts were placed on a reverse bias (collector-base) burn-in after completion of the thermal shock series. All the suspect devices subsequently channeled and destroyed themselves in this test.*

Manufacturer B's product had 7 failures out of 12 during the 335 cycles of thermal shock. The prime failure mode was an open gold ball bond (pin 10) to the thick-film substrate. A characteristic unique to each of the gold wire ball bond failures-to-thick-film gold was that the ball bond in question was made in the area adjacent to where a transistor chip was eutectically bonded. The failed ball bonds all were in the area where the chip had been scrubbed down, whereas the ball bonds made away from the scrubbed area remained intact. This failure mechanism had also been noted in field failures, and by the manufacturer, and the problem has since been solved by bonding away from the scrubbed down areas.

Manufacturer F's product had three failures out of three samples tested. The parts underwent 95 thermal shock cycles beginning at 0° to $+100^{\circ}\text{C}$ and ending up at -65°C to $+200^{\circ}\text{C}$, before all samples failed. All three units failed hermetic seal testing. Serial Number 5 also had five loosened (epoxy-bonded) transistor chips.

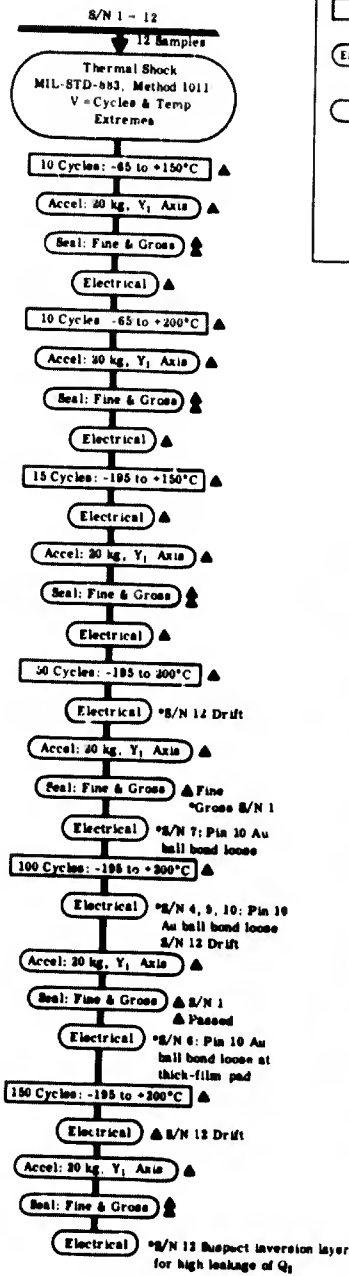
From the thermal shock testing, it was concluded that the -65°C to $+150^{\circ}\text{C}$ thermal shock did not damage the units from Manufacturers A and B, and even the -195°C to $+200^{\circ}\text{C}$ thermal shock does not itself destroy reliable hybrids (although the -195°C to $+200^{\circ}\text{C}$ extremes did cause defective hybrids to fail). It was also concluded that Manufacturer F's hybrids were unable to withstand thermal shock, even if limited to 0°C to $+100^{\circ}\text{C}$. The basic weakness is in the epoxy seal and the epoxy chip bonds used by this manufacturer.

*In a later section, Paragraph 2.4.4.8.2, it is noted that a group of Manufacturer A's parts were placed on reverse bias life and that 6 of the 10 also failed due to channeling. There is no apparent explanation for this failure mechanism occurring during -195°C to $+200^{\circ}\text{C}$ thermal shock, and further investigation was considered beyond the scope of this contract.



Mfg. A

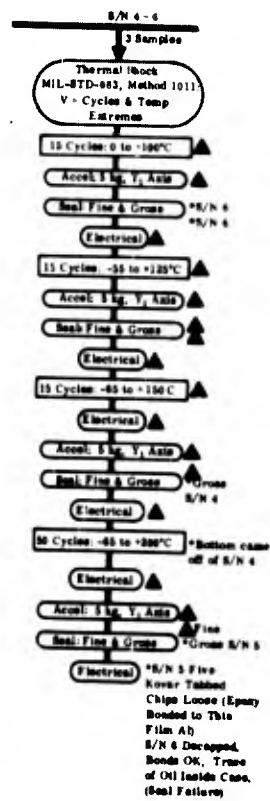
Note 1: S/N 23, 24, 27, 28, 29, 30, 31, 32, 33, 34 Placed on Reverse-Bias (Collector-Base) Burn-in After Completion of Thermal Shock Series. All Units Checked Without Current Limiting and Were Destroyed.



Mfg. B

CODE KEY

○	Identified Test (Mechanical, Environmental, or Electrical) Being Studied
⊖	Electrical Tests at 25°C to Detect Failures Caused by Previous Test
○	Environmental or Mechanical Test Per MIL-STD-883 to Locate or Induce Failures in Degraded Test Samples
V	Indicates the Parameter (Variable) Being Changed as the Test Proceeds
▲	Indicates that this Specific Test is Completed with No New Failures
*	Indicates Failure Occurrence at this Test



Mfg. F

Figure 17. Thermal Shock with Number of Cycles and Spread of Temperature Extremes as Variables

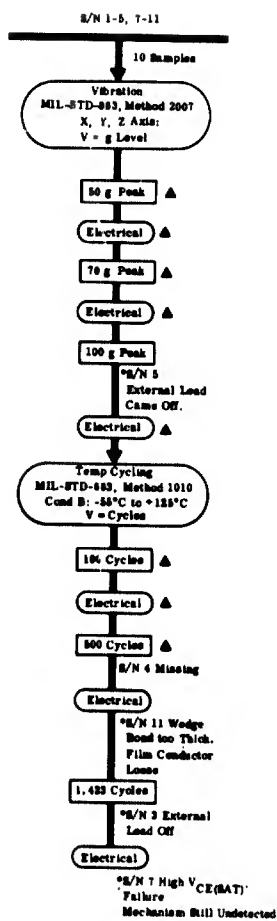
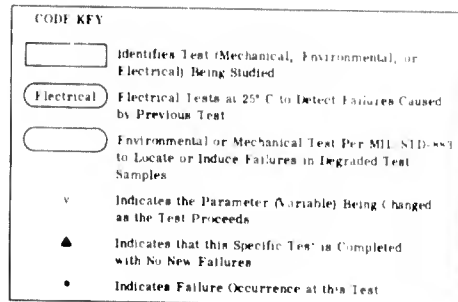
2.4.4.4 Vibration and Temperature Cycling

For this series, the hybrids (Figure 18) were first subjected to variable frequency (20 to 2,000 Hz) vibration at 50, 70, and 100 g peak, and the surviving samples were then subjected to a temperature cycling test. The temperature cycling procedure used did not conform exactly to Method 1010 of MIL-STD-883 because the cycling was performed in a single chamber, and the time duration for temperature stabilization from the low (-55°C) to the high (+125°C) was about 20 minutes, and from high to low about 10 minutes (using CO₂). These long delays were considered desirable for this test because they simulated a possible aircraft environment in which a system would be in the "off" state at a low temperature; and then turned on, causing the ambient to slowly rise to the high temperature due to the power dissipation of the overall aircraft system. While this is posed as an extreme case, it did simulate the conditions possible in real use.

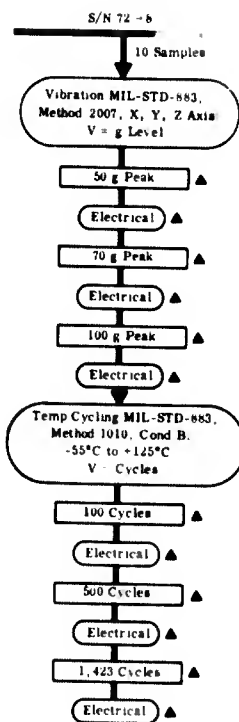
Figure 18 shows the vibration test series and its results. Manufacturer A had an external lead come off the part during vibration at 100 g. Although this failure is related to the holding fixture during vibration, Manufacturer A's hybrid does have weaker than normal external leads on the packages. Manufacturer B's unit had no failures due to the vibration at 50, 70, and 100 g peak levels in the X, Y, and Z axis. All three of the parts from Manufacturer F failed during the vibration testing. Two parts failed due to loose gold ball bonds and the third due to an external lead coming off. Serial Number 38 also had a broken gold wire wedge bond where the wire necks down at the wedge.

The bond failures on Manufacturer F's hybrids are related to the high g vibration levels only because of the very poor wire bonds. High g (100 g) vibration is not considered an effective screen for hybrid circuits, which can normally withstand 20,000 g (or more) acceleration. Introduction of variable frequency and random vibration could possibly provide a screen for large hybrids that are unable to withstand acceleration testing, but this would be expensive and still relatively ineffective.

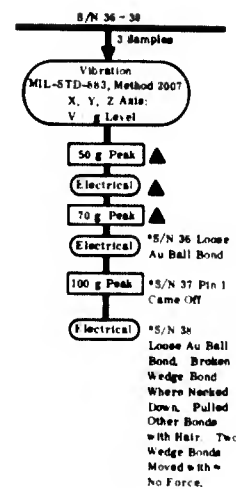
Figure 18 also shows results of the temperature cycling performed on 9 samples from Manufacturer A and 10 samples from Manufacturer B. After a total of 2,023 temperature cycles, two failures occurred on Manufacturer A's hybrids and no failures for Manufacturer B. One of the failures (S/N 11) in Manufacturer A's hybrids was due to a loose gold wire wedge bond to the gold thick-film substrate conductor. This particular device had a $V_{CE(sat)}$ of 0.470 volts (at 450 mA) at the beginning of the temperature cycling test, which increased to 0.519 volts due to the degradation of the wedge bond during temperature cycling. The second failure (S/N 7) had an initial $V_{CE(sat)}$ (at 450 mA) of 0.389 volts, which increased to 1.093 volts after 2,023 thermal cycles. The cause of this significant increase in saturation voltage was not apparent. All chip and wire bonds in this hybrid package were secure.



Mfg. A



Mfg. B



Mfg. F

Figure 18. Vibration and Temperature Cycling Evaluation

2.4.4.5 Acceleration

Constant acceleration testing was used to determine the effect of centrifugal force on the hybrid microcircuits. It was used as a high stress test to determine the mechanical limits of the package, internal lead system, die and substrate attachment, and other elements of the microelectronic devices. By establishing proper stress levels, it may be employed as an in-line screen to detect and eliminate devices having lower than nominal mechanical strengths in any of the structural elements.

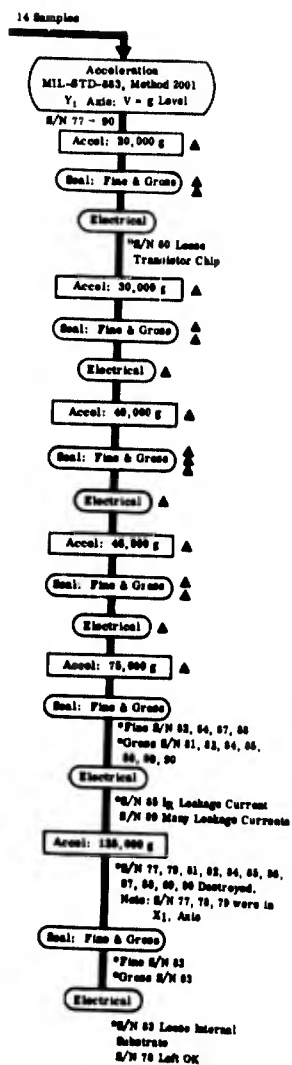
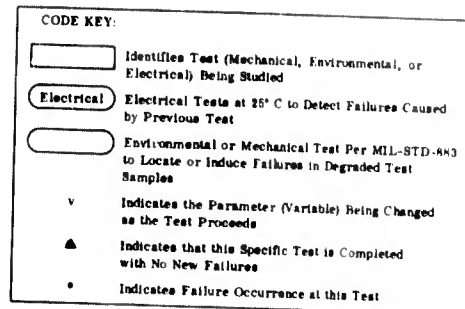
2.4.4.5.1 Acceleration in the Y_1 Axis

Stepped stress testing using acceleration in the Y_1 axis as the variable is shown in Figure 19. The Y_1 axis is defined as the axis along which centrifugal force will move substrates, chips, and wire bonds away from their bonding surface. Units from all three manufacturers failed during the acceleration testing in this axis; but, Manufacturer B had no failures prior to the 125,000 g level, and then only one legitimate failure up through 150,000 g. Manufacturer A already had a failure at the 20,000 g level, that was due to a very poor PNP transistor chip bond. The chip was improperly scrubbed into the gold pad on the substrate. With the pad very rough, the chip made contact at only three high points on the gold pad, and formed a marginal chip bond. The 13 remaining samples from Manufacturer A made it through 46,000 g with no electrical or seal failures.

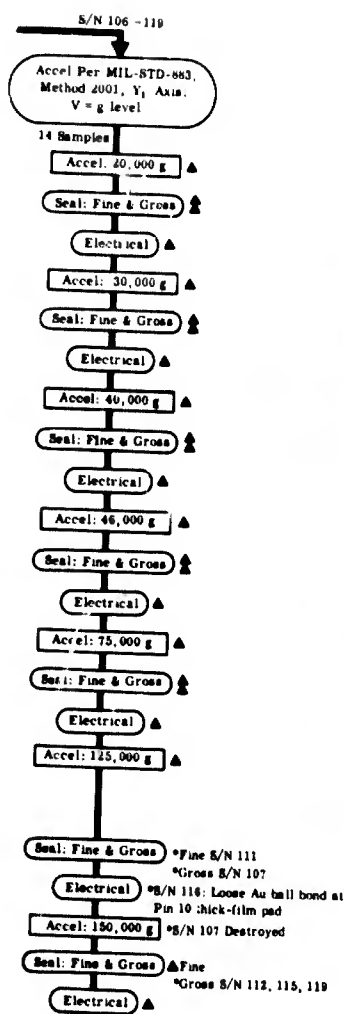
The fixturing used for acceleration below 75,000 g consisted of bowl rotors having flat surfaces machined on the inside wall of the bowl. Each of the flat surfaces had hard magnetic rubber material cemented in place. The flatpackages were centrifuged by placing them against the magnetic rubber, with plastic shim material placed under the leads to support the flat leads in the same plane they were in as they emerge from the packages. Above 46,000 g, each of the parts was potted in Carbowax* Polyethylene Glycol, a water soluble, low melting point, wax-like material. Air voids in the potting material were kept to a minimum, while the potting was hardening, by slowly cooling the holding jigs, hybrids, and potting material in a vacuum. Even with these precautions, the potting material had a tendency to "give" at very high g levels and crush the flatpackages. Because of the marginal fixturing, the fine and gross seal test failures at above 46,000 g (in Figure 19) must be considered invalid because of the possibility of seal destruction due to inadequate fixturing.

Armed with the above restrictions for interpreting data above 46,000 g, the test results showed Manufacturer A to have only one legitimate failure above 46,000 g and this failure (S/N 83) was due to a loose internal substrate after 125,000 g acceleration

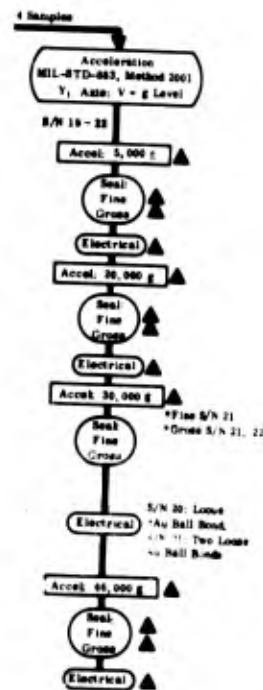
*Registered trademark of Union Carbide Corporation



Mfg. A



Mfg. B



Mfg. F

Figure 19. Acceleration Evaluation in the Y₁ Axis

in the Y_1 axis. Serial Numbers 85 and 89 failed due to the loss of hermeticity and subsequent entry of the potting material and rinse water into the flatpackages. Only one of Manufacturer B's hybrids legitimately failed acceleration testing up through 150,000 g. This was a gold ball bond failure (S/N 116) at 125,000 g acceleration. This bond had been made in the scrubbed area where a transistor chip was bonded to the thick-film pad on the substrate. (This same failure mechanism was reported in Paragraph 2.4.4.2.2, as a result of thermal shock.)

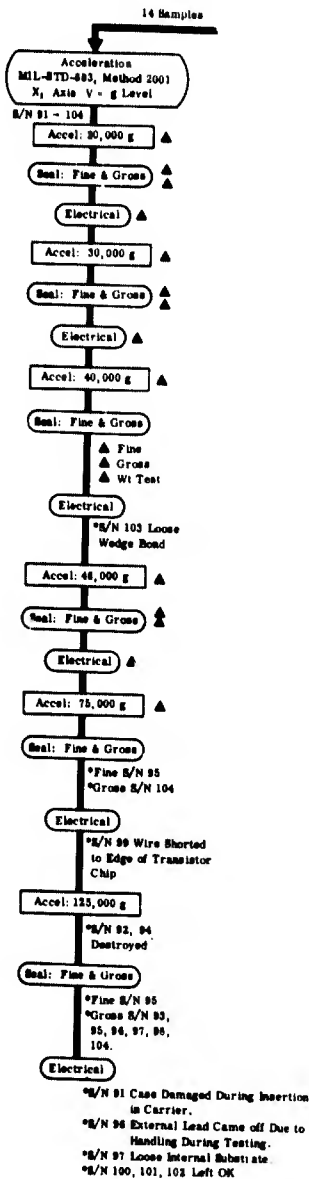
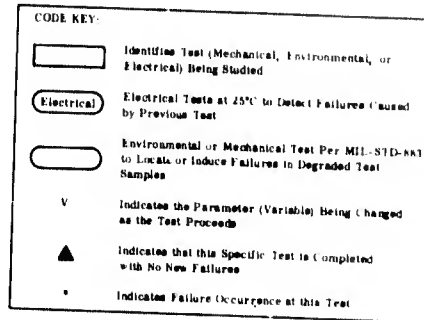
Three of the four hybrids from Manufacturer F failed prior to the 46,500 g level acceleration. Serial Number 20 had already failed the initial hermetic seal test when the parts were received from Manufacturer F (see Figure 11), and now it also failed acceleration testing because a gold ball bond lifted from the emitter of a PNP transistor. Serial Number 21 failed fine and gross seal, as well as having two loose gold ball bonds from transistor chips. Serial Number 22 failed gross seal testing. (Note that no new failures occurred on the two parts (S/N 19, 22) that were subjected to 46,000 g.)

Acceleration screening in the Y_1 axis appears to be a highly effective means of eliminating defective substrate, chip, and gold wire bonds provided that the devices can be centrifuged at high g levels. Forty thousand g is the minimum level considered to be effective for 0.7- or 1-mil gold wire systems. Aluminum wire systems, on the other hand, require at least 100,000 g. Production fixturing using magnetic rubber is available to perform screening in the Y_1 axis up to 100,000 g, but Delco Electronics has had no opportunity to evaluate these particular fixtures. Care must be taken at such high levels to assure that the holding fixtures themselves do not destroy or degrade the parts. Tooling has been fabricated at Delco to enable an evaluation of some manufacturers' monolithic integrated circuits in flatpackages up to 200,000 g without harming them. Dimensionally, these units must be held to very tight tolerances on the overall package to be suitable for consistent acceleration at 20,000 g. However, hybrid microcircuit flatpackages are not normally held to dimensions within a few thousandths of an inch.

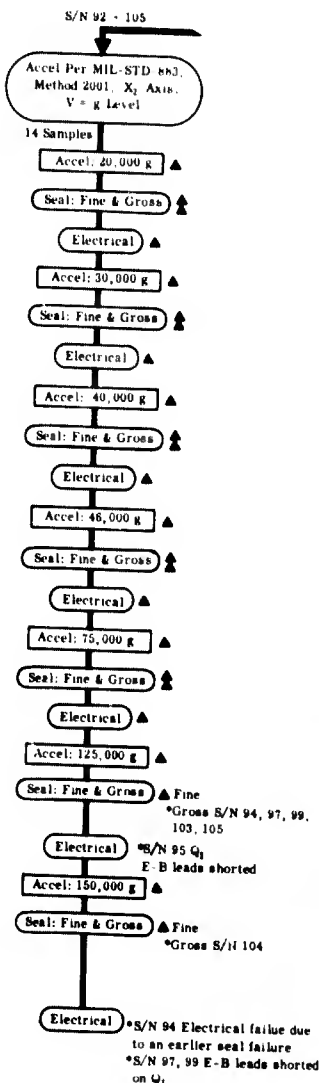
2.4.4.5.2 Acceleration in the X Axis

The X axis is defined as the axis orthogonal with both the Y axis and the axis in which the external leads emerge from the flatpackage. Acceleration in the X axis presents a shear stress on the substrate, chips, and wire bonds, and also dresses the internal wires in such a manner that they may short to one another, or to another conductive surface. All X axis acceleration was performed with the hybrids potted in Carbowax*. (Note in Figure 20 that at the higher g levels, the seals of the packages were destroyed due to the pressure of the potting material on the outside surfaces of the flatpackages.)

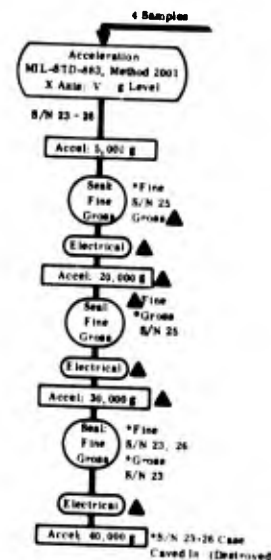
*Registered trademark of Union Carbide Corp.



Mfg. A



Mfg. B



Mfg. F

Figure 20. Acceleration Evaluation in the X Axis

Manufacturer A's hybrids all survived 20,000 and 30,000 g acceleration, but at 40,000 g, a wedge bond gave way in Serial Number 103. The wedge bond fractured at the point where the wire was indented (to a "wedge" shape) by the capillary of the bonding machine. Either too much pressure was applied in making the wedge, or else the edge of the capillary was improperly shaped, creating a weak bond. After a 75,000 g acceleration, S/N 99 had a wire shorting to the edge (collector) of a transistor chip. After 125,000 g, S/N 97 disclosed a loose ceramic substrate.

Hybrids from Manufacturer B passed all tests through 75,000 g in the X axis. After 125,000 g, the Q₁ emitter and base leads shorted on S/N 95; and, after 150,000 g, S/N 97 and 99 showed the same leads shorted as those on S/N 95. All of Manufacturer F's hybrids also survived electrical testing after acceleration, up through 30,000 g in the X axis; but then they were all crushed at 40,000 g due to the action of the potting material used. The seal on S/N 25 was already destroyed at 5,000 g, and S/N 23 and 26 each lost hermeticity at 30,000 g.

Results of the acceleration testing in the X axis clearly indicate that good substrate, chip, and wire bonds can withstand high g levels, but the fixturing used to hold the packages tends to destroy their hermeticity. Significantly high g levels are tolerated before internal leads begin to short and cause the hybrid to fail.

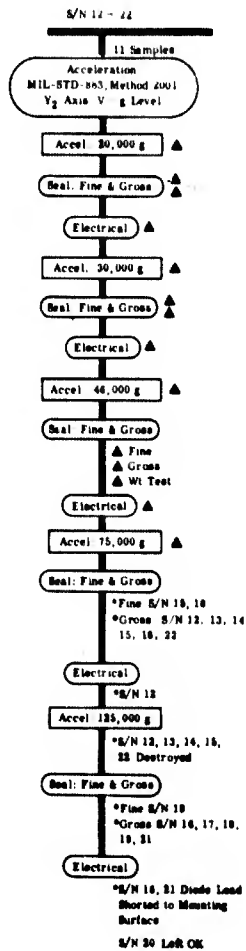
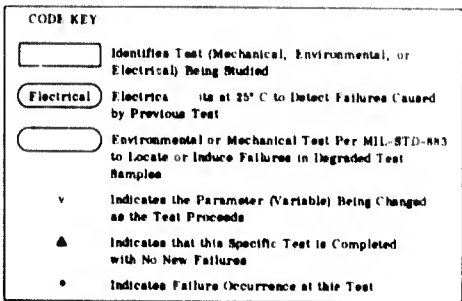
2.4.4.5.3 Acceleration in the Y₂ Axis

Figure 21 describes acceleration of Manufacturers A and B's flatpackages in the Y₂ axis. Acceleration in the Y₂ axis forces internal wires down against the chips and substrate, and ultimately causes short circuits at points where wires cross other conductors. The fixtures used were the same as those for the Y₁ axis acceleration. There were no electrical failures up to and including the 46,000 g acceleration. A unit from Manufacturer B lost its hermetic seal during the 30,000 g acceleration. However, the seal data for 75,000 g and above are not considered valid for evaluation purposes for the reasons explained earlier in the Y₁ axis discussion. Manufacturer A had 3 electrical failures. S/N 12 had a short after 75,000 g, and S/N's 18 and 21 failed after the 125,000 g acceleration. Manufacturer B also had 3 failures. S/N 62 showed a short after 75,000 g, S/N 70 after 125,000 g, and S/N 69 after 150,000 g.

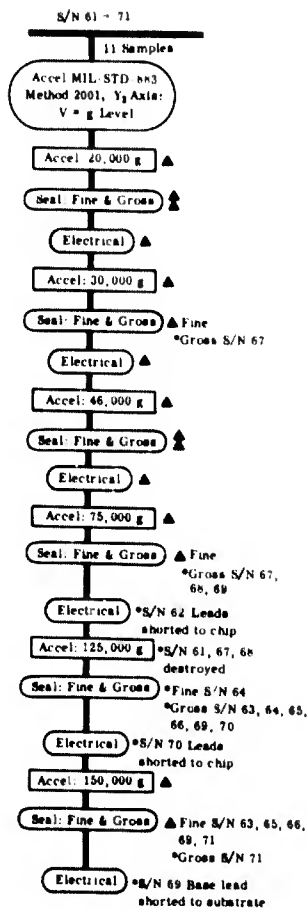
The Y₂ axis acceleration was clearly shown to be useful only as an evaluation tool, and not as a 100 percent screen. Should a hybrid short at 20,000 g acceleration or less in the Y₁ axis, this would appear to indicate a poor circuitry layout within the hybrid package. Both Manufacturers A and B have good layouts, and this is why they had no failures prior to 75,000 g.

2.4.4.6 Hermetic Seal Test

Hermetic seal testing was performed many times in the stepped stress testing to identify both initial failures and those caused by testing. (See Figures 8, 9, 10.)



Mfg. A



Mfg. B

Figure 21. Acceleration Evaluation in the Y₂ Axis

This paragraph describes the initial seal tests and those performed on one group of hybrids from each of the three suppliers. Initial results of hermetic seal testing of Manufacturers A, B, and F's hybrids are shown on the top of Figures 8, 9, and 10.

Manufacturer A had 5 hermetic seal failures out of 150 of its hybrids initially tested. The gross seal testing of Manufacturer A's hybrids per MIL-STD-883, Method 1014, Condition C, Step 2 (fluorocarbon gross leak with vacuum backfill) yielded inconclusive results during this testing because many packages emitted very fine bubbles over a wide area of the package surface. All 150 samples were then subjected to a weight hermetic seal test. The weight method for gross hermetic seal testing was performed by controlled weight measurements before and after backfill.

During the weight method hermetic seal test, all the samples were handled with great care to keep them free of any oil, or other contaminant. When handling was necessary, tweezers were used rather than bare fingers. The parts were first baked at approximately 100°C for 4 hours minimum to drive off any moisture. Shortly after baking, the parts were weighed on an electronic scale to the nearest tenth of a milligram and then backfilled with FC-78 per MIL-STD-883, Method 1014, Condition C, Step 2. After backfill, the parts were kept in FC-78 until the time they were placed back on the scale. The FC-78 evaporated so rapidly that the time it took to transfer the part from the FC-78 to the scale was sufficient to dry the external part surfaces. Failed parts were detected by a change in weight from bake to after backfill. Units whose weight changed more than 0.4 milligram were considered leakers (failures).

This weight method test was performed first with a backfill pressure of 40 psig for 3 hours, and again at 40 psig for 16 hours (because of some marginal units in the 150-piece sample). It was concluded that the 3-hour backfill at 40 psig was insufficient for this particular package at this pressure to reveal marginal units, so backfill times were increased to 5 hours for later testing of this manufacturer's part.

Table VIII provides a detailed breakdown of the hermetic seal test results for Serial Numbers 12 through 22 from Manufacturer A. Figure 22 outlines part of the hermetic seal evaluation for all three manufacturers. The same parts from Manufacturers A and B were placed on Y₂ axis acceleration testing (Figure 21) after completing the seal test. Table VIII lists these tests, along with the seal testing, with backfill pressure changes. Tables IX and X show seal test results for Manufacturers B and F, with varying backfill pressure. Manufacturer B had no initial seal failures on the 150 samples evaluated (Figure 9), and Manufacturer F (Figure 10) had two failures out of 50 samples.

The backfill pressure was varied during these evaluation tests for two reasons: first, to establish correlation of readings with backfill pressure. Second, it was increased to determine if and when packages are destroyed due to high pressure. The data in Tables VIII, IX, and X indicate that the time and pressure factors used had little effect on the fine leak rates and the overall results of the test.

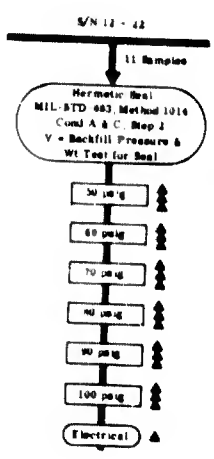
Table VIII. Hermetic Seal Test Results Using Manufacturer A's 1/4" x 3/8" Flatpackage

HYBRID NO.	SEAL TEST TYPE		SEAL TEST RESULTS FOR VARIOUS BACKGAS PRESSURES (SPARK TIMES OMITTED)										SEAL TEST 6.281 LITS PER HOUR AT 1.0 ATMOSPHERE IN THE 1/2 AND (SEE FIGURE 2)					FINE LEAK (10 ⁻⁵)	
			INITIAL SEAL TEST (SEE FIGURE 4)					HERMETIC SEAL EVALUATION (SEE FIGURE 2)					SEAL TEST 6.281 LITS PER HOUR AT 1.0 ATMOSPHERE IN THE 1/2 AND (SEE FIGURE 2)					MEAN DATA	RANGE
			40	50	60	70	80	90	100	110	120	130	140	150	160	170	180		
S/N 12	Fine Leak Rate	Alm cc/s	8.5	16.5	11.3	14.0	42.0	24.0	29.0	72.8	56.5	29.5	18.0					16.5	
		SB																	
	Gross Leak Weight (Note 2)	Before	0.4179	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	3.5-42.0	
		After	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181			
	Fine Leak Rate	Alm cc/s	25.0	23.0	17.0	15.0	15.0	22.0	30.0	30.5	3.0	10.5	23.0					19.3	
SB																			
S/N 13	Gross Leak Weight (Note 2)	Before	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	5.0-15.0	
		After	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181			
	Fine Leak Rate	Alm cc/s	8.5	15.0	10.5	11.0	21.0	16.5	21.0	8.0	11.0	8.0	15.0					14.0	
		SB																	
	S/N 14	Gross Leak Weight (Note 2)	Before	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	8.0-24.0
After			0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181			
Fine Leak Rate		Alm cc/s	8.5	14.0	11.0	15.0	19.0	24.0	28.0	8.0	10.4	8.0	13.0					20.3	
		SB																	
S/N 15		Gross Leak Weight (Note 2)	Before	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	8.0-47.0
	After		0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181			
	Fine Leak Rate	Alm cc/s	8.5	12.0	9.0	12.5	16.5	14.0	16.5	2.5	8.1	6.5	13.0					11.1	
		SB																	
	S/N 16	Gross Leak Weight (Note 2)	Before	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	5.0-16.5
After			0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181			
Fine Leak Rate		Alm cc/s	8.5	12.0	9.0	12.5	16.5	14.0	16.5	2.5	8.1	6.5	13.0					10.5	
		SB																	
S/N 17		Gross Leak Weight (Note 2)	Before	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	5.0-21.0
	After		0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181			
	Fine Leak Rate	Alm cc/s	8.5	12.0	9.0	12.5	16.5	14.0	16.5	2.5	8.1	6.5	13.0					22.3	
		SB																	
	S/N 18	Gross Leak Weight (Note 2)	Before	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	5.0-55.0
After			0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181			
Fine Leak Rate		Alm cc/s	8.5	12.0	9.0	12.5	16.5	14.0	16.5	2.5	8.1	6.5	13.0					21.5	
		SB																	
S/N 20		Gross Leak Weight (Note 2)	Before	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	5.0-55.2
	After		0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181			
	Fine Leak Rate	Alm cc/s	8.5	12.0	9.0	12.5	16.5	14.0	16.5	2.5	8.1	6.5	13.0					20.5	
		SB																	
	S/N 21	Gross Leak Weight (Note 2)	Before	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	5.0-55.2
After			0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181			
Fine Leak Rate		Alm cc/s	8.5	12.0	9.0	12.5	16.5	14.0	16.5	2.5	8.1	6.5	13.0					12.7	
		SB																	
S/N 22		Gross Leak Weight (Note 2)	Before	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	5.0-55.0
	After		0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181	0.4181			
	Fine Leak Rate	Alm cc/s	8.5	12.0	9.0	12.5	16.5	14.0	16.5	2.5	8.1	6.5	13.0					12.7	
		SB																	

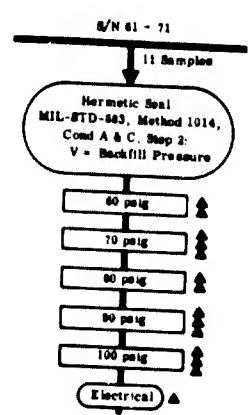
Note 1: Code: SB - No. Bubbles; FB - Fine Bubbles.
 Note 2: Gross leak test wherein the sample was baked dry, weighed, then backfilled per MIL-STD-883C, Method 1014, Cond. 1, 40 psia, and again weighed. Units are grams (1000 mg = 1 gram).

CODE KEY:

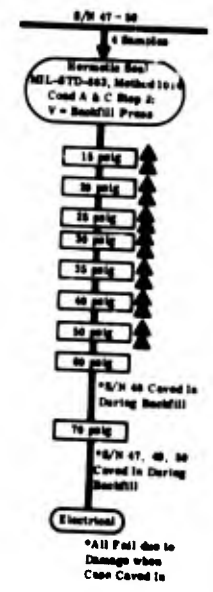
	Identifies Test (Mechanical, Environmental, or Electrical) Being Studied
	Electrical Tests at 25° C to Detect Failures Caused by Previous Test
	Environmental or Mechanical Test Per MIL-STD-883 to Locate or Induce Failures in Degraded Test Samples
v	Indicates the Parameter (Variable) Being Changed as the Test Proceeds
▲	Indicates that this Specific Test is Completed with No New Failures
•	Indicates Failure Occurrence at this Test



Mfg. A



Mfg. B



Mfg. F

Figure 22. Hermetic Seal Evaluation

Table IX. Hermetic Seal Test Results Using Manufacturer B's
1/4" x 1/8" Flatpackage

HYBRID NO.	SEAL TEST		TEST RESULTS FOR VARIOUS BACKFILL PRESSURES (psig)/TIMES (hours)						FINE LEAK ($\times 10^{-9}$)	
			40	60	70	80	90	MEAN RATE	RANGE	
	TYPE	UNITS	3	3	3	3	3			
S/N 61	Fine Leak Rate	Atm-cc/s $\times 10^{-9}$	1.7	4.2	4.2	3.0	11.0	$\bar{X} = 4.8$	1.7-11.0	
	Gross Leak	(Note 1)	FB	FB	FB	FB	FB			
	Weight (Note 2)	Before After	grams	-	-	0.1688	-			0.1687
S/N 62	Fine Leak Rate	Atm-cc/s $\times 10^{-9}$	1.4	4.2	5.5	2.1	8.3	$\bar{X} = 4.3$	1.4-8.3	
	Gross Leak	(Note 1)	FB	FB	FB	FB	FB			
	Weight (Note 2)	Before After	grams	-	-	0.1623	-			0.1622
S/N 63	Fine Leak Rate	Atm-cc/s $\times 10^{-9}$	1.7	4.2	4.4	1.4	1.4	$\bar{X} = 5.1$	1.4-14.0	
	Gross Leak	(Note 1)	FB	FB	FB	NB	FB			
	Weight (Note 2)	Before After	grams	-	-	0.1605	-			0.1604
S/N 64	Fine Leak Rate	Atm-cc/s $\times 10^{-9}$	1.5	3.5	5.5	6.6	9.6	$\bar{X} = 5.3$	1.5-9.6	
	Gross Leak	(Note 1)	FB	FB	FB	FB	FB			
	Weight (Note 2)	Before After	grams	-	-	0.1602	-			0.1601
S/N 65	Fine Leak Rate	Atm-cc/s $\times 10^{-9}$	1.4	4.2	4.6	2.5	7.6	$\bar{X} = 4.1$	1.4-7.6	
	Gross Leak	(Note 1)	FB	FB	FB	FB	FB			
	Weight (Note 2)	Before After	grams	-	-	0.1584	-			0.1584
S/N 66	Fine Leak Rate	Atm-cc/s $\times 10^{-9}$	2.1	4.2	5.5	5.0	12	$\bar{X} = 5.8$	2.1-12.0	
	Gross Leak	(Note 1)	FB	FB	B	FB	FB			
	Weight (Note 2)	Before After	grams	-	-	0.1674	-			0.1674
S/N 67	Fine Leak Rate	Atm-cc/s $\times 10^{-9}$	1.4	3.5	3.0	4.2	8.4	$\bar{X} = 4.1$	1.4-8.4	
	Gross Leak	(Note 1)	FB	FB	FB	FB	FB			
	Weight (Note 2)	Before After	grams	-	-	0.1668	-			0.1669
S/N 68	Fine Leak Rate	Atm-cc/s $\times 10^{-9}$	5.1	3.5	4.2	2.1	9.0	$\bar{X} = 4.8$	2.1-9.0	
	Gross Leak	(Note 1)	FB	FB	FB	NB	FB			
	Weight (Note 2)	Before After	grams	-	-	0.1592	-			0.1593
S/N 69	Fine Leak Rate	Atm-cc/s $\times 10^{-9}$	2.8	4.2	4.9	1.4	9.5	$\bar{X} = 4.6$	1.4-9.5	
	Gross Leak	(Note 1)	FB	FB	FB	FB	FB			
	Weight (Note 2)	Before After	grams	-	-	0.1702	-			0.1703
S/N 70	Fine Leak Rate	Atm-cc/s $\times 10^{-9}$	3.0	2.8	4.9	4.1	8.3	$\bar{X} = 4.6$	2.8-8.3	
	Gross Leak	(Note 1)	FB	FB	FB	NB	FB			
	Weight (Note 2)	Before After	grams	-	-	0.1600	-			0.1601
S/N 71	Fine Leak Rate	Atm-cc/s $\times 10^{-9}$	2.4	3.5	4.2	4.1	7.0	$\bar{X} = 4.2$	2.4-7.0	
	Gross Leak	(Note 1)	FB	FB	FB	NB	FB			
	Weight (Note 2)	Before After	grams	-	-	0.1595	-			0.1596

NOTES:

- Code: NB = No Bubbles; B = Bubbles; FB = Fine Bubbles
- Gross leak test wherein the sample was baked dry, weighed, then backfilled per MIL-STD-883, Method 1014, Cond. C, Step 2, and again weighed. Units increasing > 0.0004 grams were considered to be nonhermetic.

Table X. Hermetic Seal Test Using Manufacturer F's 1" x 1" Flatpackage

HYBRID NO.	SEAL TEST		TEST RESULTS FOR VARIOUS BACKFILL PRESSURES (psig)/TIMES (hours)												FINE LEAK	
	TYPE	UNITS	10	15	20	25	30	35	40	45	50	60	70	MEAN RATE	RANGE	
S/N 47	Fine Leak Rate	Atm-cc/s $\times 10^{-8}$	0.84	8.1	2.9	5.2	7.0	11	17	19	19	9.5	0	Cover Caved In	$\bar{X} = 8.95$	
	Gross Leak Weight (Note 2)	(Note 1) grams	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB				
	Before	3.8847														
S/N 48	Fine Leak Rate	Atm-cc/s $\times 10^{-8}$	0.70	7.0	2.5	4.2	6.1	12.5	19	18	18	8.4	0	Cover Caved In	$\bar{X} = 8.79$	
	Gross Leak Weight (Note 2)	(Note 1) grams	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB				
	Before	4.0032														
S/N 49	Fine Leak Rate	Atm-cc/s $\times 10^{-8}$	0.62	5.5	1.9	1.6	5.4	8.5	13	14	14	8.4	0	Cover Caved In	$\bar{X} = 6.77$	
	Gross Leak Weight (Note 2)	(Note 1) grams	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB				
	Before	4.0757														
S/N 50	Fine Leak Rate	Atm-cc/s $\times 10^{-8}$	0.60	9.8	3.2	6.2	8.4	1.8	25	25	25	13	0	Cover Caved In	$\bar{X} = 12.13$	
	Gross Leak Weight (Note 2)	(Note 1) grams	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB				
	Before	4.0524														
	After	4.0823														

Notes: 1

- Code: NB - No Bubbles; FB - Fine Bubbles; VFB - Very Fine Bubbles
- Gross leak test wherein the sample was weighed before and after backfill in FC-78.

The fine leak rates were measured using the tracer gas (helium) method, and the data indicates rather poor repeatability of the readings. Variables that affect the leak rate reading are the stability and calibration of the mass spectrometer, control of contamination and paint on the packages, size of packages, type of package material, and length of time out of the helium backfill before the measurements made (if the time is relatively short).

Tables VIII, IX, and X list the average leak rates and the range of readings for each sample. Also shown are the gross leak (Method 1014, Condition C, Step 2) test results and the backup gross seal data from performing the weight seal tests. The gross seal test is subjective because although some packages had very fine bubbles emerging, they are still hermetic packages. Experienced gross seal test operators can differentiate between most of the actual leakers and those merely showing background bubbles, but the capability is not 100 percent effective. Since it is poor economics to reject all the fine bubblers, this subjective method had to be backed up by the weight method to establish the actual leakers.

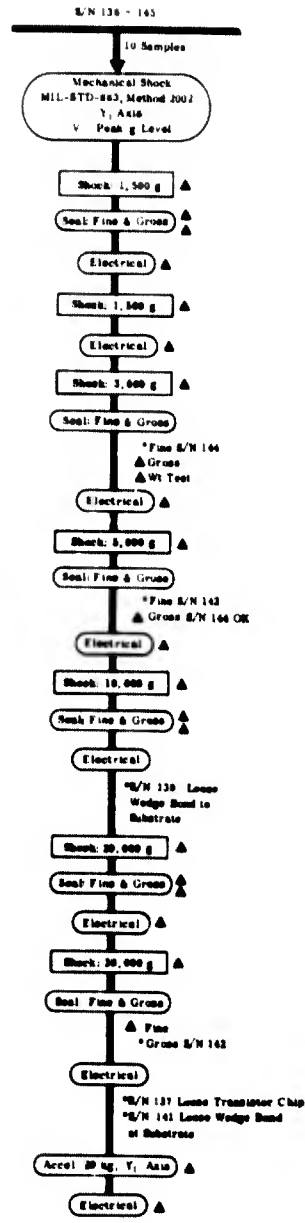
In summary, Method 1014, Condition C, Step 2 was found to be a much more effective seal test than the earlier gross seal test method (MIL-STD-750 and MIL-STD-202), but there is much room for economic improvement in the gross seal test.

2.4.4.7 Mechanical Shock

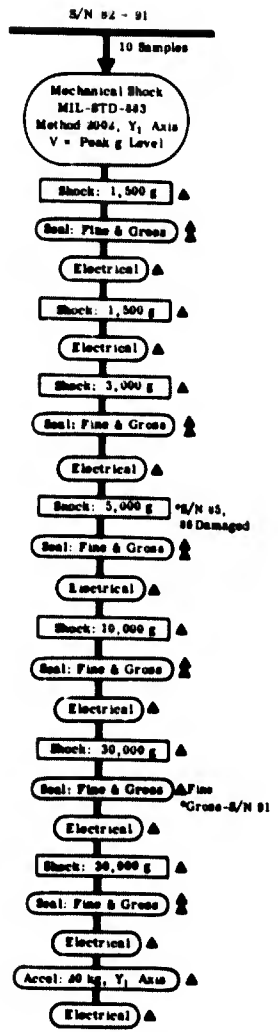
Figure 23 displays the mechanical shock test performed on a pneupactor-type, mechanical shock tester. The flatpackages were attached to a projectile and, with air flowing in the venturi section of the shock tester, a suction was created at the inlet which drew the projectile into the tube. Propelled down the tube by expanding air, the projectile left the tube and impacted on a seismically-mounted mass (called the striker plate). In this fashion, the flatpack underwent shock of a magnitude and duration that could be varied by air pressure and measured by an accelerometer. Four of the hybrids were destroyed upon impact, because the projectile and flatpack rebounded and struck part of the shock test fixture. This situation was averted through modifications to the pneupactor, where the projectile exited from the tube.

Manufacturer A's hybrids had three electrical failures due to shock testing. S/N 138 failed after 10,000 g due to a loose wedge bond to the substrate. S/N's 137 and 141 failed, after the five 30,000 g peak shock pulses, due to a loose NPN transistor chip, and a loose wedge bond to the substrate, respectively. Manufacturer B's hybrids had no electrical failures due to the five shock pulses at 1,500, 3,000, 5,000, 10,000, 20,000, and 30,000 g peak in the Y_1 axis. Only one of Manufacturer B's hybrids failed hermetic seal testing, and this was after the 20,000 g shock pulses.

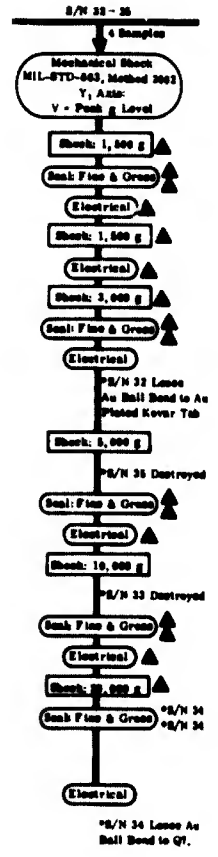
CODE KEY:	
	Identifies Test (Mechanical, Environmental, or Electrical) Being Studied
Electrical	Electrical Tests at 25° C to Detect Failures Caused by Previous Test
	Environmental or Mechanical Test Per MIL-STD-883 to Locate or Induce Failures in Degraded Test Samples
*	Indicates the Parameter (Variable) Being Changed as the Test Proceeds
▲	Indicates that this Specific Test is Completed with No New Failures
●	Indicates Failure Occurrence at this Test



Mfg. A



Mfg. B



Mfg. F

Figure 23. Mechanical Shock Evaluation

One of Manufacturer F's hybrids failed at 3,000 g due to a loose gold ball bond to the gold plated kovar transistor mounting tab, and another showed a loose ball bond to a transistor after 20,000 g. Only four of Manufacturer F's hybrids were mechanically shocked, and after the 20,000 g pulses, no samples were left for 30,000 g testing.

Mechanical shock testing at low g levels (below 10,000) appears to be ineffective in revealing part defects. Above 10,000 g, it serves to disclose poor chip bonds and wire bonds, but it is a difficult test (or screen) to employ with large quantities of parts. While special fixturing could be devised to mechanically shock on a volume basis, tight controls would have to be maintained to preclude part damage.

2.4.4.8 Life Test

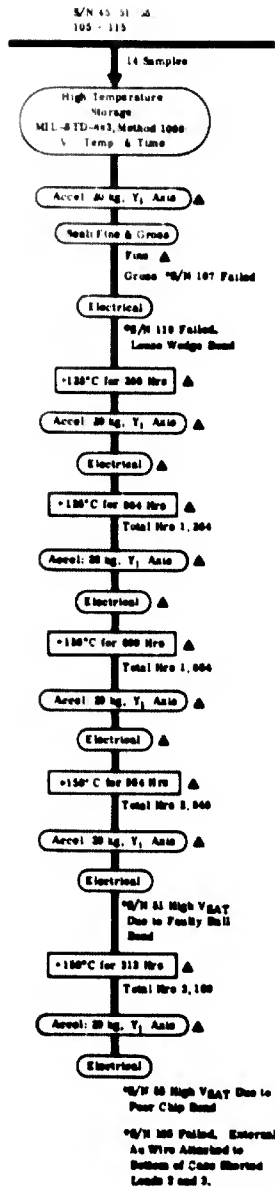
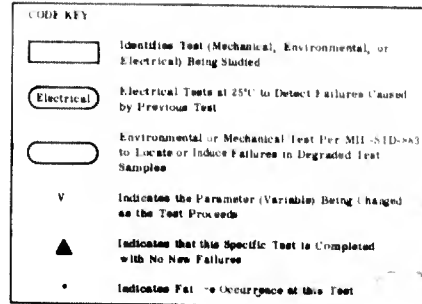
Figures 8, 9, and 10 each have three life tests listed. They are high temperature storage, reverse bias life, and parallel excitation life. The high temperature storage was performed as a reference against which to compare the other two life tests.

2.4.4.8.1 High Temperature Storage Life

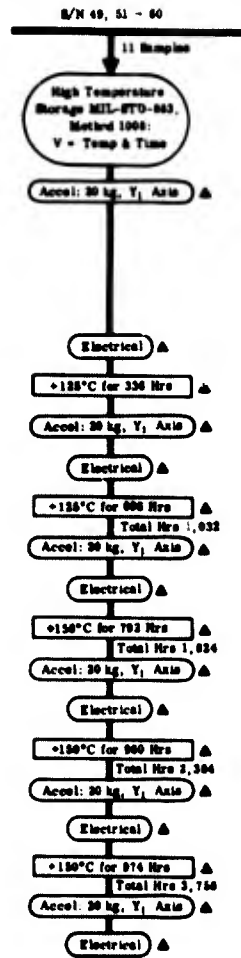
Figure 24 shows the test results for high temperature storage, beginning at +125°C and going to +150°C. The hybrids were stored, unenergized, in an oven at the specified temperature for the time duration shown in the sequence. S/N 51 from Manufacturer A failed after a total of 2,848 hours of storage (1,264 hours at +125°C and 1,584 hours at +150°C) due to a faulty ball bond. The failure mode was a high $V_{CE(sat)}$ at 450 milliamperes of collector current. At zero hour, the $V_{CE(sat)}$ measured 0.356 volt, and at the time of failure, the $V_{CE(sat)}$ had increased to 0.627 volt.

Two additional failures occurred after 3,160 hours of storage life. Serial Number 55 failed $V_{CE(sat)}$ due to a poor chip bond, and S/N 106 failed due to the loose end of a 1-mil gold wire being attached to outside the package bottom. This foreign wire contacted and shorted with leads 2 and 3. The gold wire was present since the hybrid was manufactured, and in handling the wire shifted sufficiently to cause a short circuit.

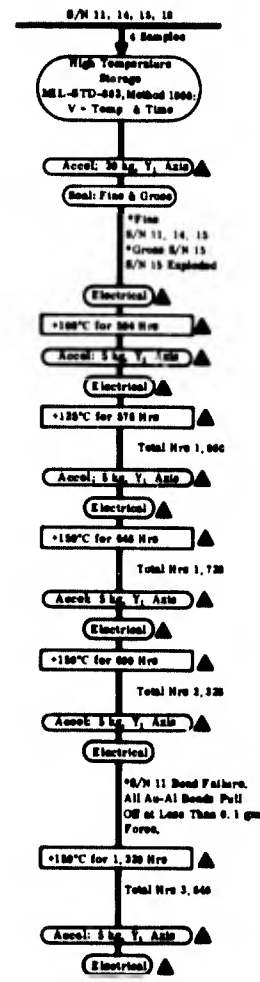
Serial Number 55 had failures on both NPN transistors due to poor chip bonds. $V_{CE(sat)}$ at 450 milliamperes was 0.360 and 0.361 volt initially, and 0.569 and 0.615 volt at failure. When the internal wire bonds were checked, during failure analysis, by pulling the wires, the wedge bonds broke at 3 grams and over. When the chip bonds were checked by gentle pushing with a fine wire, the NPN transistor chips popped off from very little force.



Mfg. A



Mfg. B



Mfg. F

Figure 24. High Temperature Storage Life Test Evaluation

Manufacturer B's hybrids had no failures during 3,758 hours of high temperature storage. Manufacturer F had one of the three samples fail after 2,328 hours of storage life (1,080 at +125°C and 1,248 hours at +150°C). Serial Number 11 failed due to a broken bond to an NPN transistor-emitter, at the point where the wire was necked down for the wedge bond. The gold wire wedge appeared to have aluminum migrating into, or over, the gold. All the other gold-to-aluminum bonds were then pull tested. All broke at less than 0.1 gram, indicating a serious bonding problem.

2.4.4.8.2 Reverse Bias Life

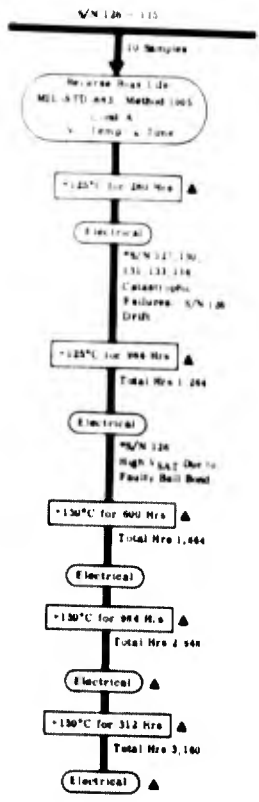
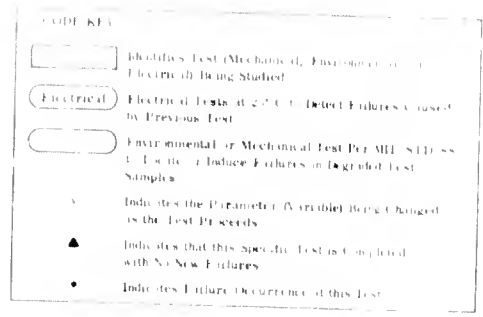
In this test, as many junctions as possible were reverse biased during the life test. Figure 25 shows the test times and temperatures. At each test point, the bias was maintained on the samples until they reached room temperature. Then, they were electrically tested within four hours after removal of the bias.

The purpose of a reverse bias life test was to determine whether semiconductor devices incur changes in electrical characteristics due to surface inversion or polarization. This was determined by monitoring critical parameters, such as h_{FE} and I_{CBO} in the case of transistors, and I_R in the case of diodes. When reverse bias life is performed with little current limiting, the poorer devices often self-destruct when their leakage currents become high enough to cause high power dissipation, or to turn on a transistor. When very little current is used, extreme caution must be used to eliminate noise or transients on the power supplies, which could inadvertently destroy good units.

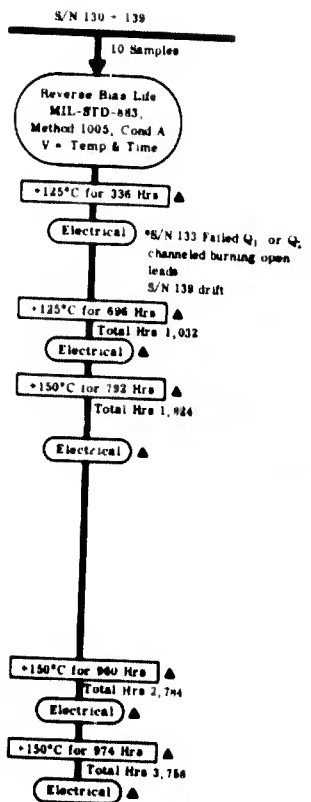
As shown in Figure 25, for Manufacturer A, six of the ten samples failed during the first 280 hours at +125°C, but then no further failures occurred due to surface inversion during the balance of the 3,758 hours of life testing. These parts supposedly had received a reverse bias burn-in by Manufacturer A. In a subsequent investigation, into why these units had passed, it was found that Manufacturer A had:

1. Introduced a high impedance in series with the power supply to limit the current in the bias circuit,
2. Removed the bias before reducing the oven temperature,
3. Not tested the parts shortly after removal of the bias.

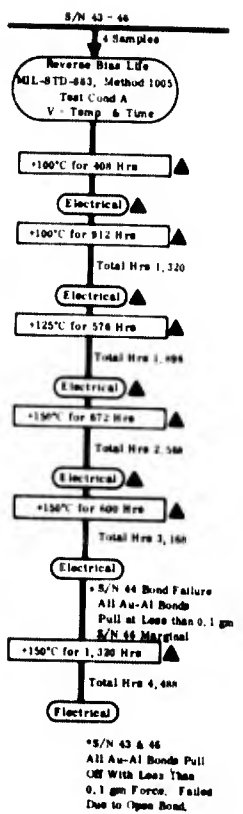
While the supplier had used no current limiting earlier, he subsequently added current limiting to increase his yield during this screen. Had the supplier introduced current limiting, lowered the oven temperature before removing the bias, and tested the parts within 8 hours, he would have exposed the faulty units.



Mfg. A



Mfg. B



Mfg. F

Figure 25. Reverse Bias Life

Manufacturer A had one other failure (S/N 126) during the reverse bias life, but this was due to a faulty ball bond. The failure mode was high V_{CE(sat)}, which was initially measured at 0.373 volt, and then at 0.678 volt at the time of failure. The ball bond was lifted away from the chip at less than 0.1 gram. The aluminum metalization had very little intermetallic formation, and very little indication of pressure in making the bond.

Manufacturer B's hybrids had two failures due to reverse bias life. This manufacturer does not perform a reverse bias burn-in on his parts, and the failures are predictable. Both failures occurred during the initial +125°C life period, and no other failures occurred during the remainder of the 3,758 hours.

Manufacturer F had no failures due to surface inversion, but there was a recurrence of the bond failures that were found during the storage life test. Manufacturer F definitely has a serious gold-to-aluminum bonding deficiency.

It was found that with reverse bias life testing, the failures occur within the first few hours of test. Experience indicates that nearly all occurred during the first 168 hours, and many are found during the 48 hours of reverse bias burn-in.

Each semiconductor manufacturer, each device type, and each lot must be evaluated to assure that the devices do not suffer surface inversion effects. These problems still predominate in discrete diode and transistor chips — even in 1970, when suppliers claim that process improvement and design changes have eliminated these failure mechanisms.

2.4.4.8.3 Parallel Excitation Life

In the parallel excitation life test condition, each circuit was driven with a signal appropriate to simulate, as closely as possible, the worst case circuit application. All circuits had a maximum load applied. Figure 26 lists the times and temperatures applied to each manufacturer's hybrids.

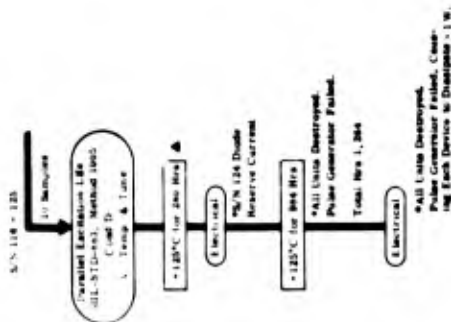
Manufacturer A's hybrids had one failure after 280 hours at +125°C. The failure mode was an increase of diode reverse current over the specification limit. During the next time period, all the samples were destroyed when a pulse generator failed, causing each hybrid to dissipate over one watt. The heat generated from the high power dissipation slowly melted the internal leads and created intermetallic formation at the gold-to-aluminum wire bonds; and the aluminum metallization on the transistor chips also showed indications of electromigration.

Manufacturer B's hybrids registered one 0-hour failure when Serial Number 120 failed to operate in the life test circuit. Failure analysis showed the collector to be shorted to the base in transistor Q₁. After 2,784 hours of life (1,056 hours at +125°C and 1,728 hours at +150°C), S/N's 122 and 128 from Manufacturer B showed a high leakage at transistor Q₃. After another 974 hours of 150°C operation, S/N 124 also failed due to high leakage. All three failures acted as though they had channels caused by an inversion, resulting in the high leakage currents. (Earlier results of the reverse bias life supported the hypothesis of channeling.)

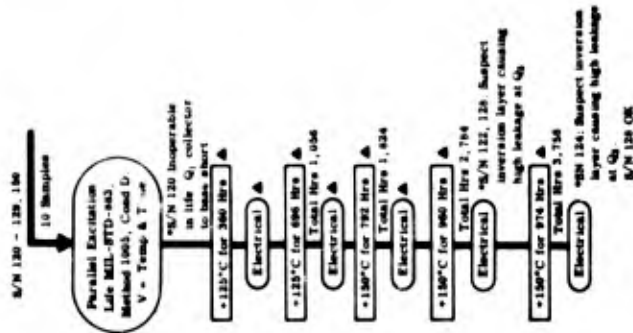
Manufacturer F's hybrids operated for 3,168 hours with no failures. But, after another 1,320 hours, three of the four hybrids failed. All three failures were caused by loose gold wire bonds. This same failure mechanism was found during high temperature storage and reverse bias life. Manufacturer F clearly has a time-dependent failure mechanism in their hybrids due to faulty wire bonds.

CODE KEY

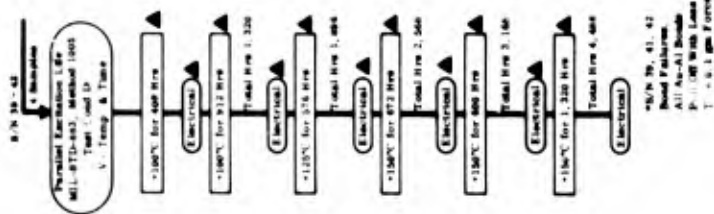
○	Identifies Test (Mechanical, Environmental, or Electrical) Being Method
□	Electrical Tests at 20° C to Detect Failures Caused by Previous Test
◇	Environmental or Mechanical Test Per MIL-STD-883 to Locate or Induce Failure in Integrated Test Sample
*	Indicates the Parameter (Variable) Being Changed at the Test Proceeds
▲	Indicates that this Specific Test is Completed with No New Failures
•	Indicates Failure Occurrence at this Test



Mfg. A



Mfg. B



Mfg. F

Figure 26. Parallel Excitation Life Evaluation

2.4.4.9 Internal Wire Bond Pull Tests

A review of Figures 8, 9, and 10 shows that, during all the stepped stress testing, 6.7 percent of Manufacturer A's 150 hybrids failed due to faulty internal wire bonds. Manufacturer B's 150 samples also had 4 percent failure due to faulty bonds; but, Manufacturer B's failure mechanism was unique in that all six failures were due to detachment of ball bonds from the thick-film conductor on the substrate. The bonds were all in the area where a transistor chip was "scrubbed in" to make a chip bond. (This bond is at the end of internal lead Number 12 in Figure 27.) Manufacturer F's hybrids did not receive stress levels as high as those of Manufacturers A and B; yet, these hybrids had 36 percent of the 50 samples fail due to faulty bonds.

Internal wire pull tests were subsequently performed on all Manufacturer B's hybrid microcircuits which survived the stepped stress tests described in Figure 28. (Note Figure 28 is Figure 9 repeated for the reader's convenience.) The pull tests were performed on these samples to determine the extent to which the gold wires bonded to gold plated kovar, gold thick-film conductors, aluminum in contact with silicon on transistor chips, and aluminum over silicon dioxide on the thin-film resistor chips were degraded due to the extreme stress levels. The wire pull tests were performed per Method 2011, Condition D of MIL-STD-883. Figures 29 through 38 portray the results of these pull tests after the stepped stress tests. Note that before the pull tests, each sample was heated by a soldering iron to remove the kovar lid (greater than 300°C).

Figure 29 depicts the overall bond pull test results for all the surviving units. Note that the gram gage used on the bond pull tester had a scale of 0 to 5 grams, and the pull tester was set to not exceed 6 grams pull to prevent damage to the gage. This precaution caused the last bar on each chart to be out of proportion to the other bars, and emphasis should therefore be placed on the wire or bond failures at and below 5 grams. Each graph portrays the distribution of force required to break the wire or bond with both a bar chart and a cumulative curve of percent fallout. Figures 30 through 35 show wire pull results for each test group in Figure 28. Note that there is very little deviation from one group to the other, indicating that the applied stresses did not significantly degrade the bonds.

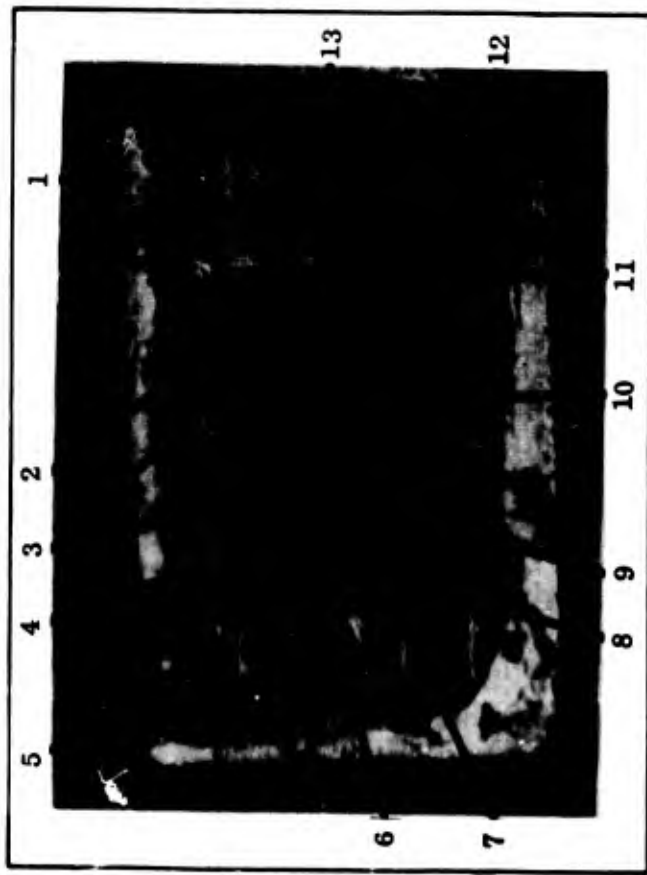


Figure 27. Internal Leads in Manufacturer B's Hybrid Microcircuit

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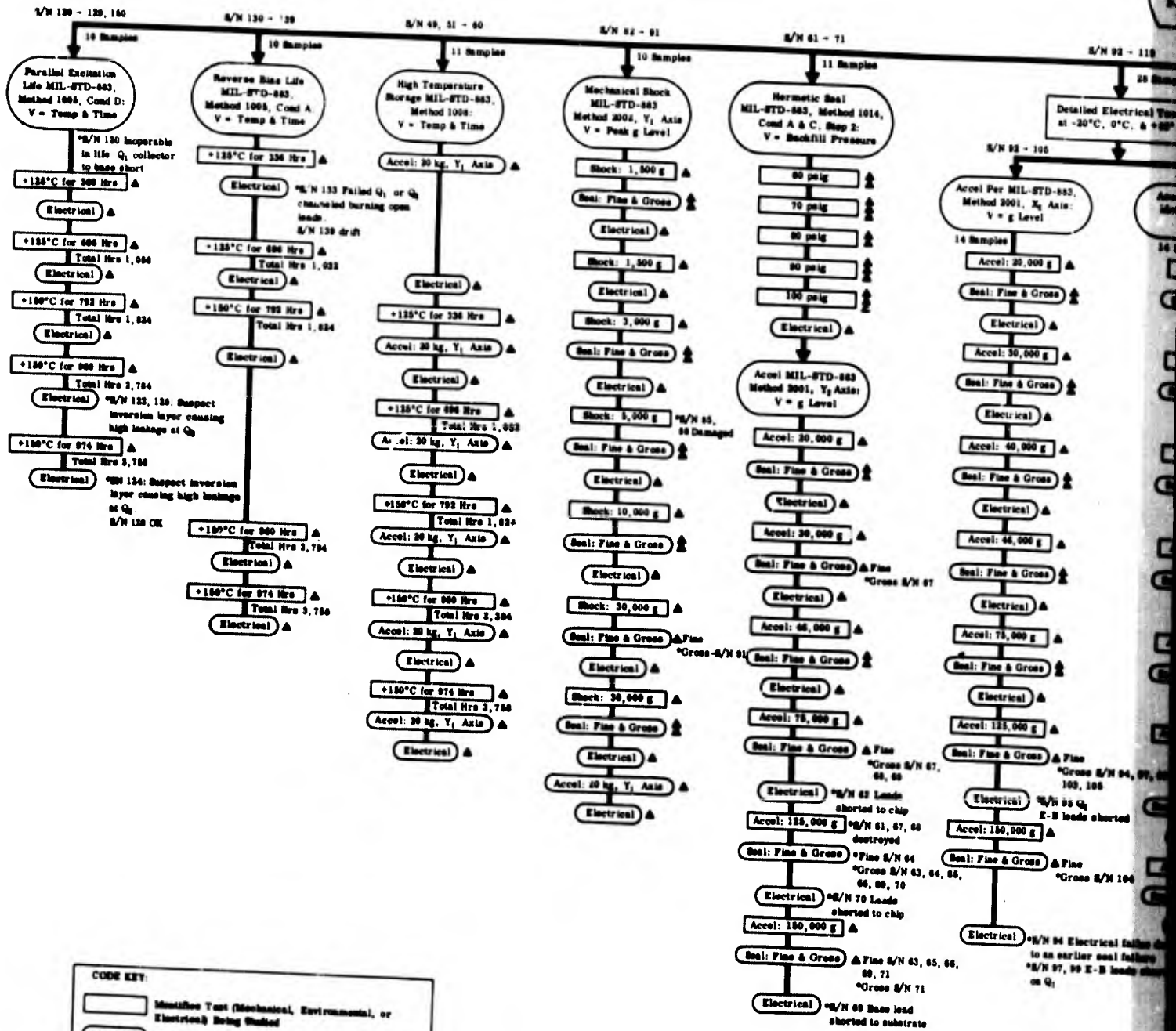
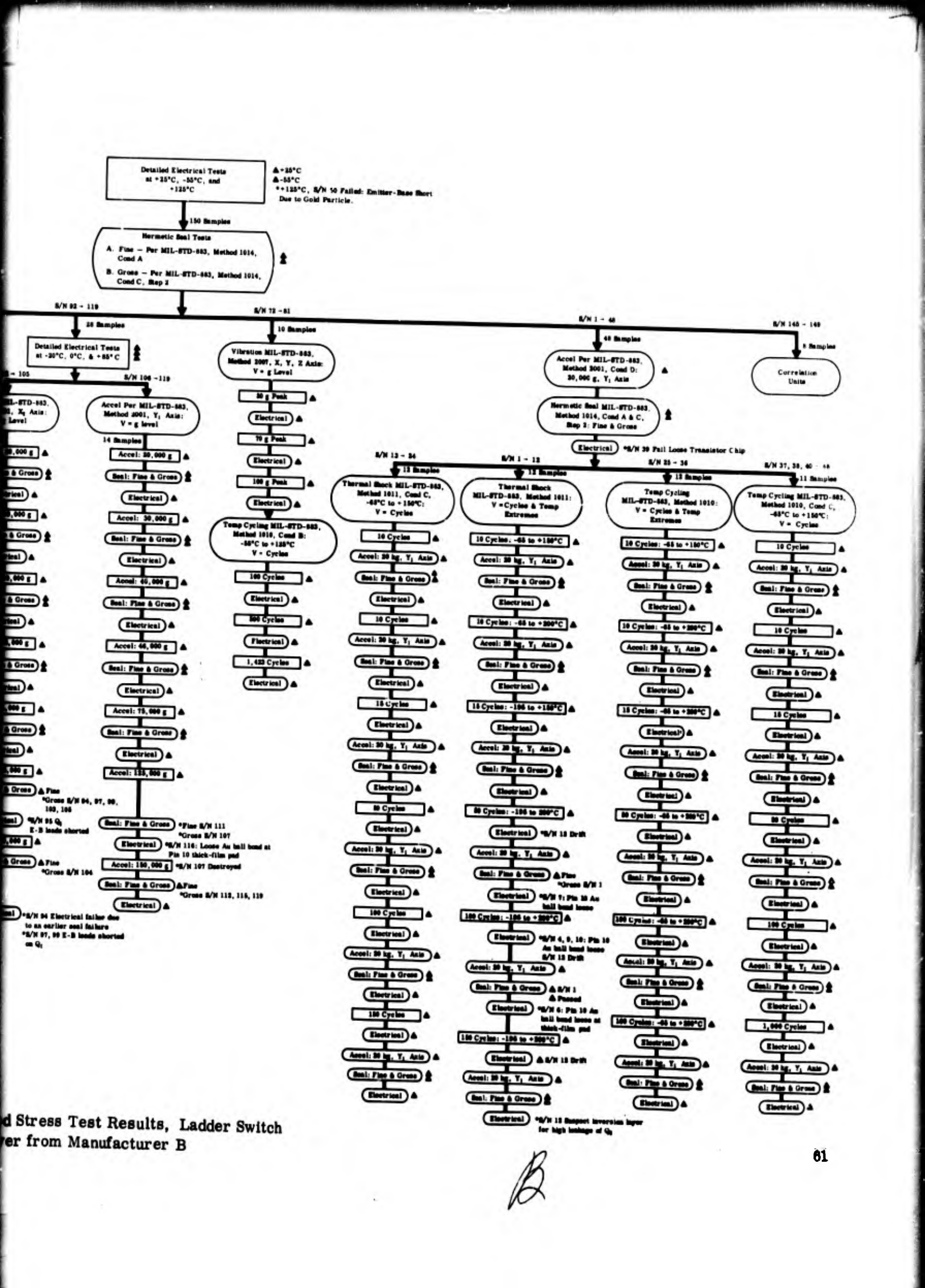


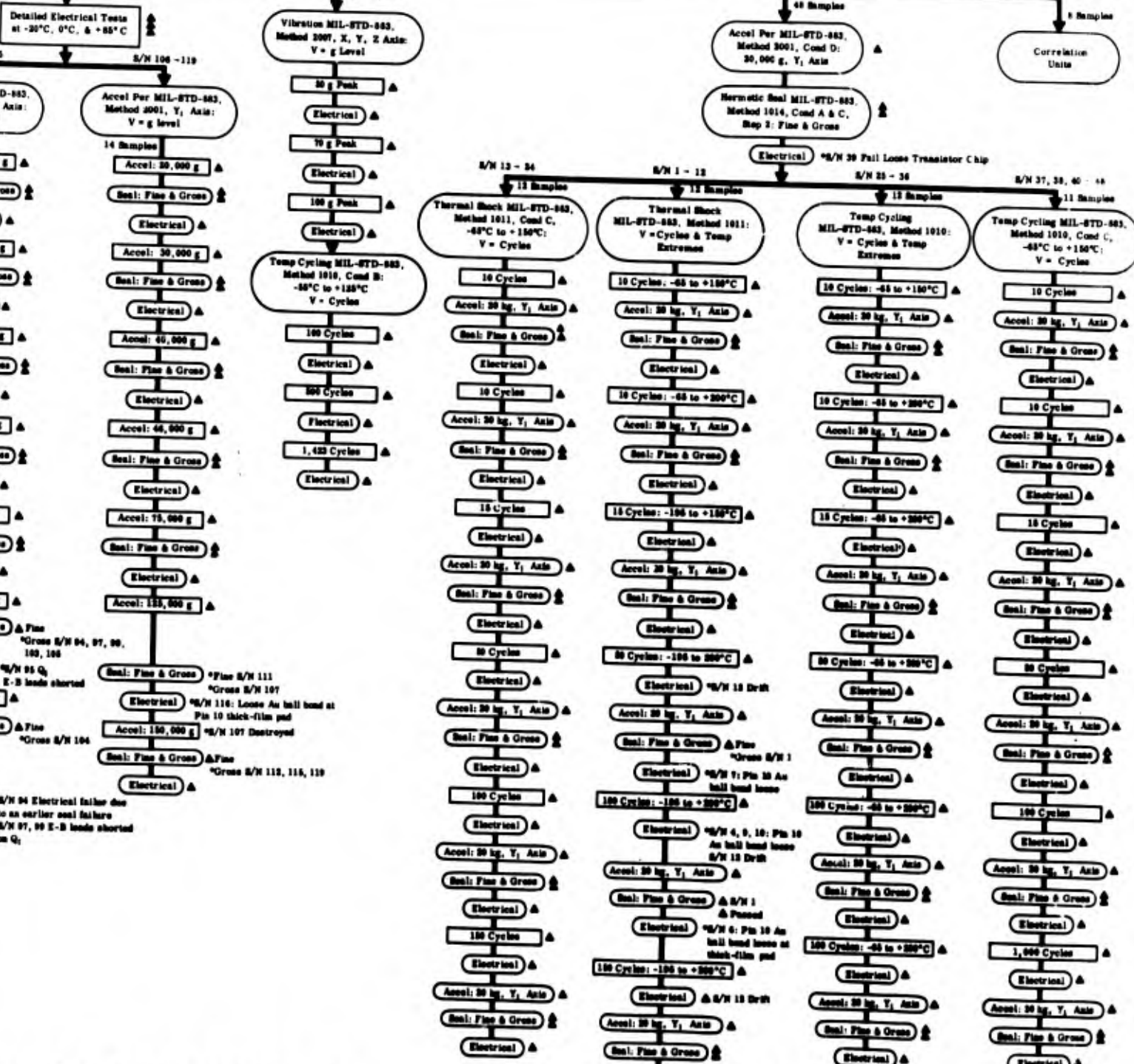
Figure 28. Stepped Stress Test and Driver from Manufacturer



Detailed Electrical Tests at +25°C, -55°C, and +125°C
 150 Samples

Hermetic Seal Tests
 A. Fine - Per MIL-STD-883, Method 1014, Cond A
 B. Gross - Per MIL-STD-883, Method 1014, Cond C, Step 2

S/N 92 - 119 S/N 72 - 81 S/N 1 - 48 S/N 145 - 148



*Gross S/N 94, 97, 99, 103, 104

*Fine S/N 111

*Gross S/N 107

*S/N 114: Loose Au ball bond at Pin 10 thick-film pad

*S/N 107 Destroyed

*Gross S/N 112, 115, 119

*S/N 94 Electrical failure due to an earlier seal failure

*S/N 97, 99 E-B leads shorted on Q1

*S/N 18 Support inversion layer for high leakage of Q1

Stress Test Results, Ladder Switch
 from Manufacturer B

B

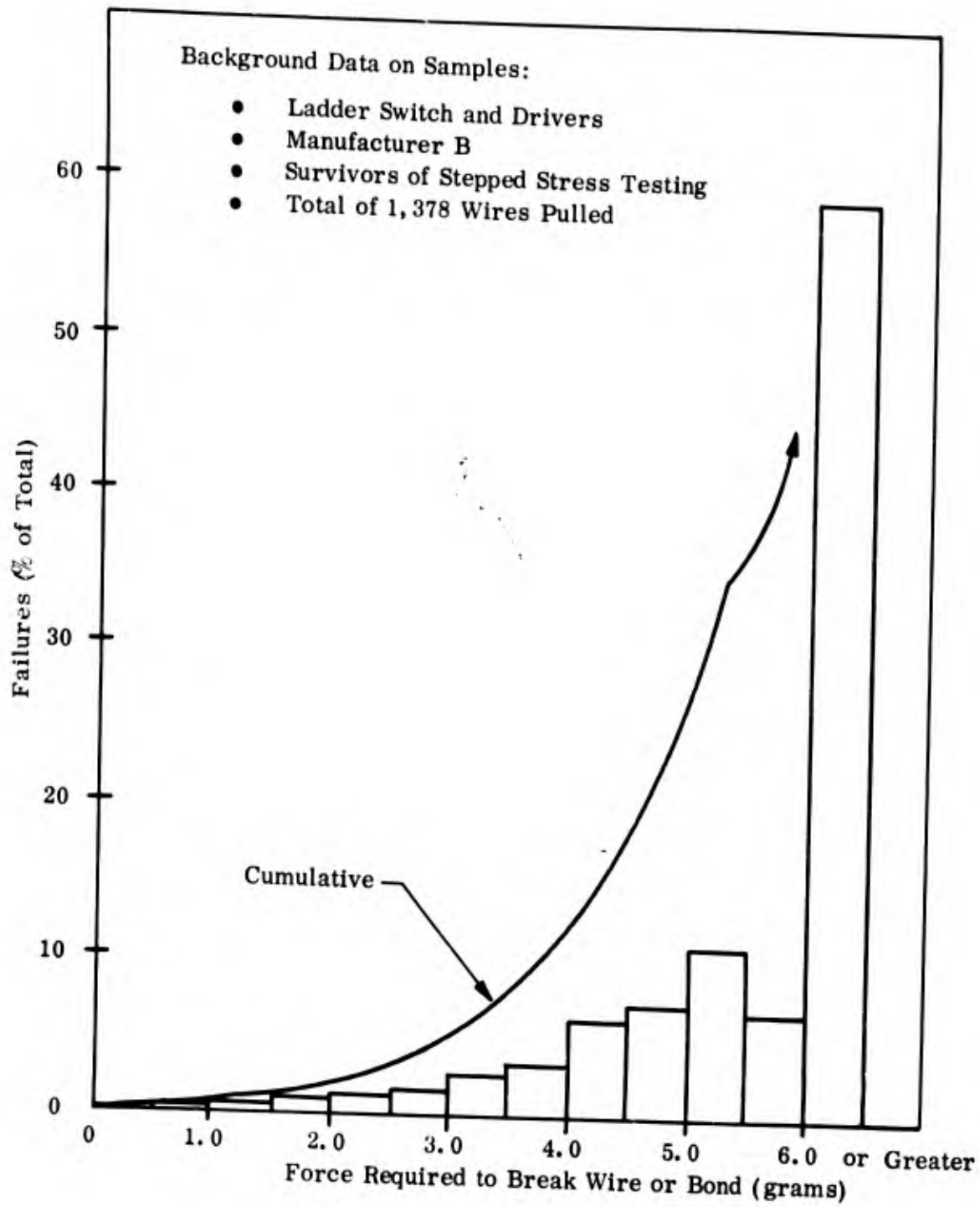
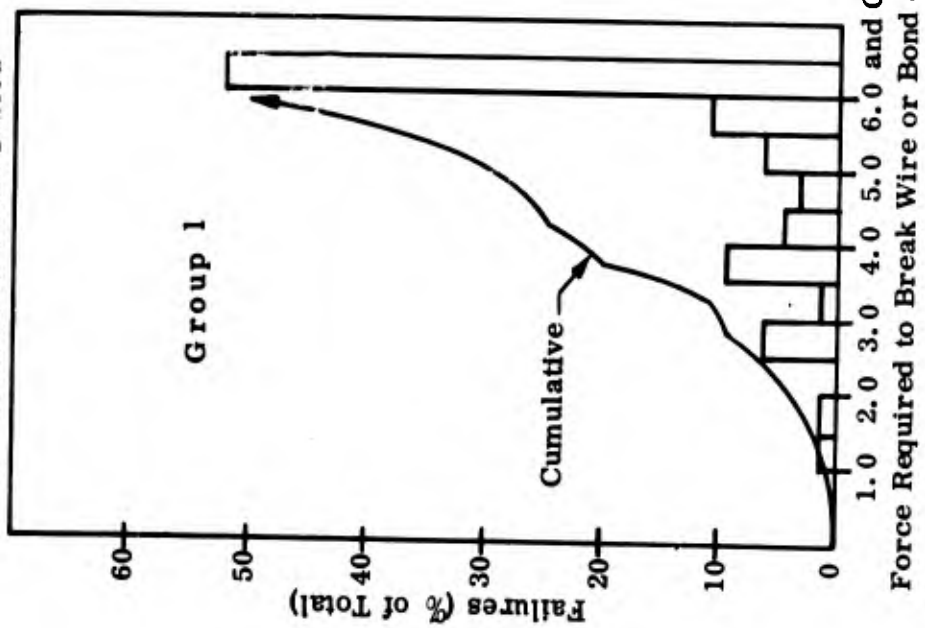


Figure 29. Overall Bond Pull Tests

Background Data:

- Tested After Passing 335 Thermal Shock Cycles: -65° to +150°C, up to -195° to +200°C
- Serial Numbers 1 - 12
- Total of 65 Wires Pulled



Background Data:

- Tested After Passing 335 Thermal Shock Cycles: -65° to 150°C
- Serial Numbers 13 - 24
- Total of 143 Wires Pulled

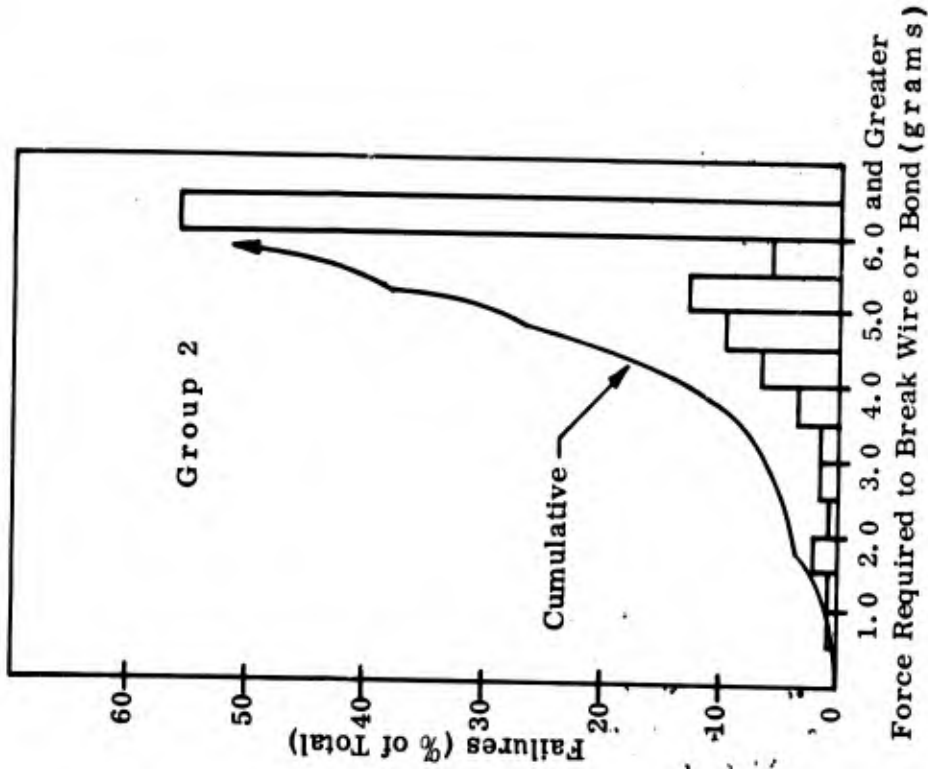
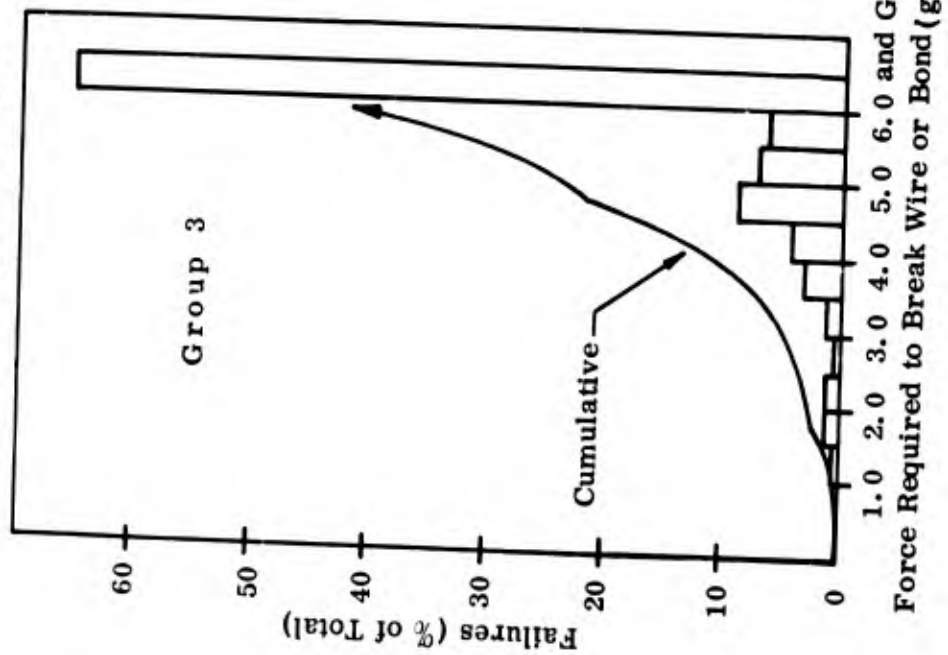


Figure 30. Wire Bond Pull Tests - Group 1 and 2

Background Data:

- Tested After Passing 1, 185
Temperature Cycles: -65°
to +150° C
- Serial Numbers 37, 38, 40 -
48
- Total of 143 Wires Pulled



Background Data:

- Tested After Passing 285
Temperature Cycles: -65°
to 150° C, up to -65° to
+200° C
- Serial Numbers 25 - 36
- Total of 143 Wires Pulled

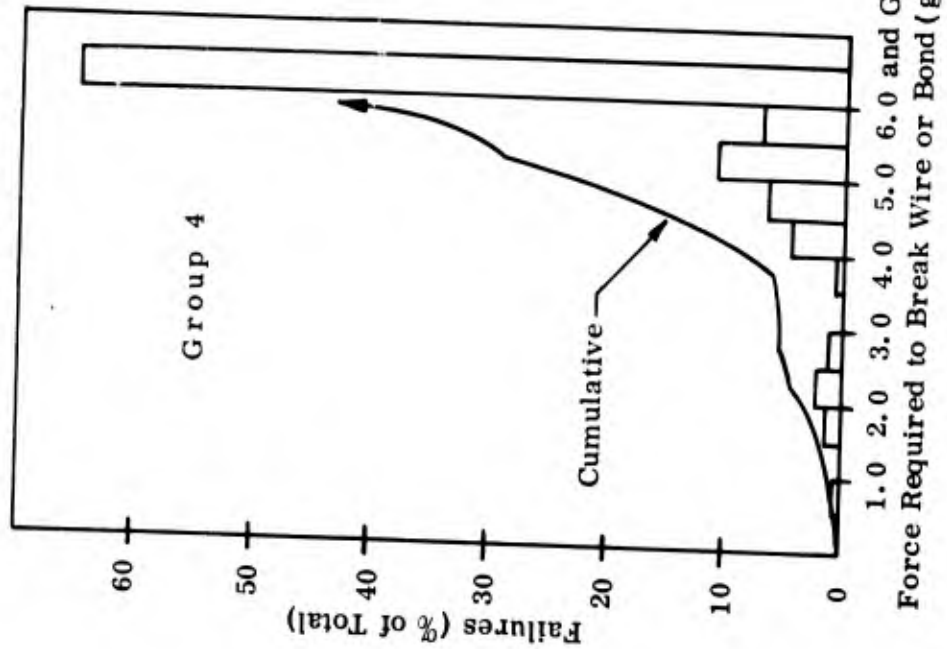
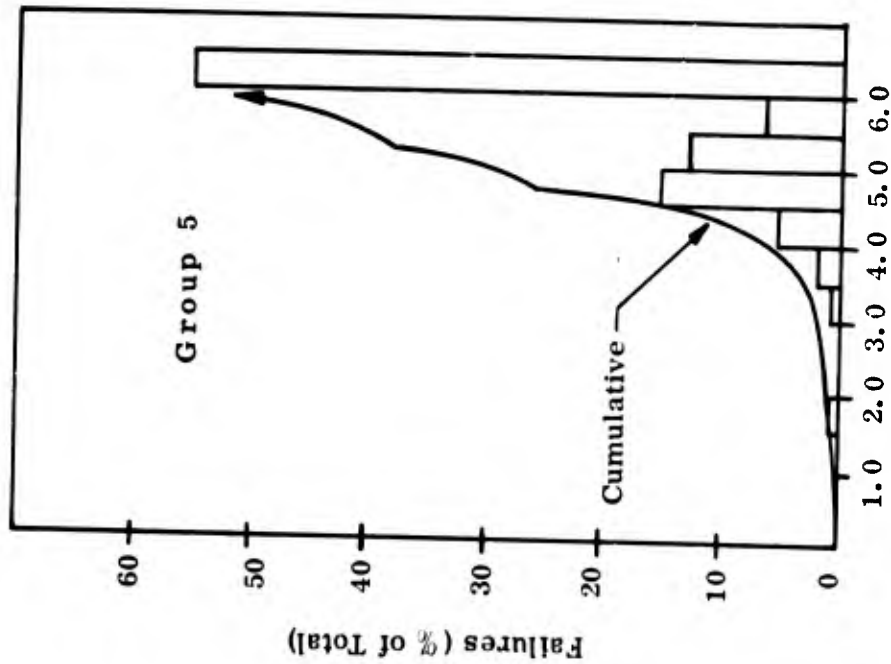


Figure 31. Wire Bond Pull Tests - Group 3 and 4

Background Data:

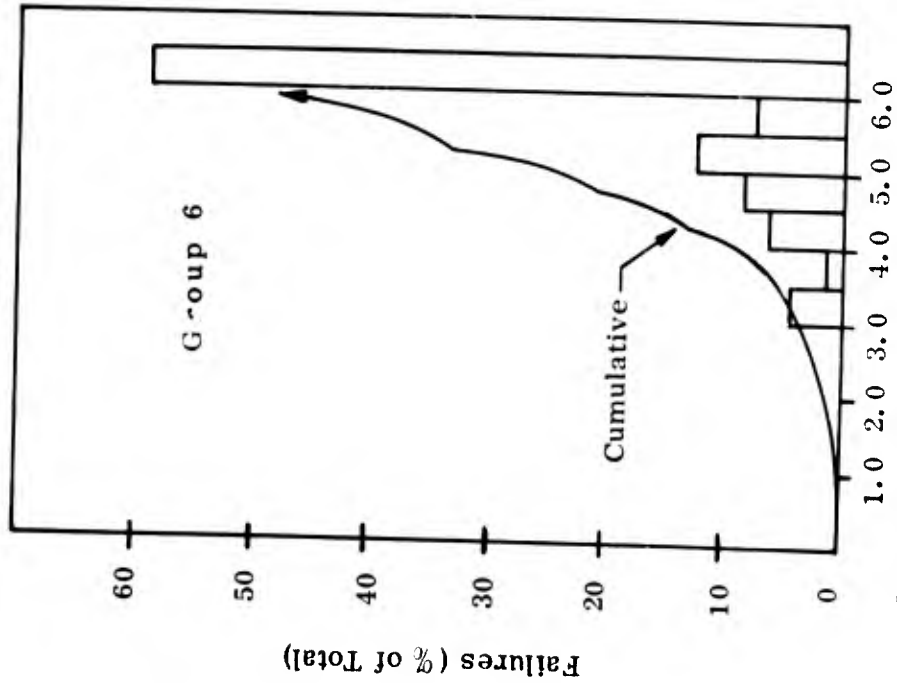
- Tested After Passing 1.5, 3, 5, 10, 20, and 30 kg Mechanical Shock, and 20 kg Acceleration in the Y₁ Axis
- Serial Numbers 82 → 91
- Total of 91 Wires Pulled



Force Required to Break Wire or Bond (grams)

Background Data:

- Tested After Passing 3, 758 Hours of High Temperature Storage: 1,032 Hours at +125°C, and 2,726 Hours at +150°C
- Serial Numbers 49, 51 → 60
- Total of 143 Wires Pulled

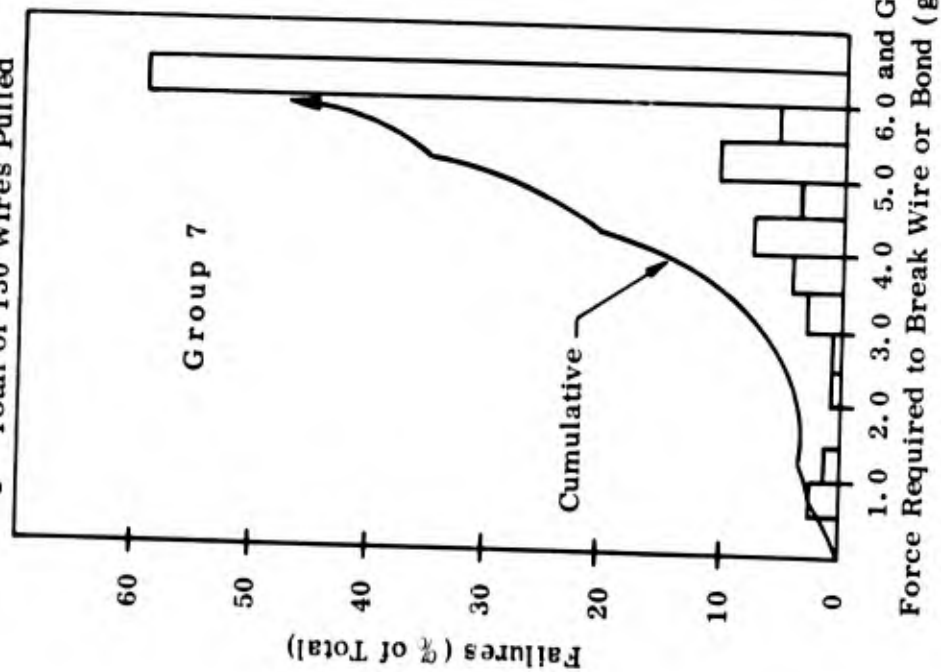


Force Required to Break Wire or Bond (grams)

Figure 32. Wire Bond Pull Tests — Group 5 and 6

Background Data:

- Tested After Passing 50, 70, and 100 g Vibration, Plus 2,023 Temperature Cycles: -55° to +125° C
- Serial Numbers 72 - 81
- Total of 130 Wires Pulled



Background Data:

- Tested After Passing 20, 30, 46, 75, 125, and 150 kg Acceleration in the Y₂ Axis
- Serial Numbers 61 - 71
- Total of 65 Wires Pulled

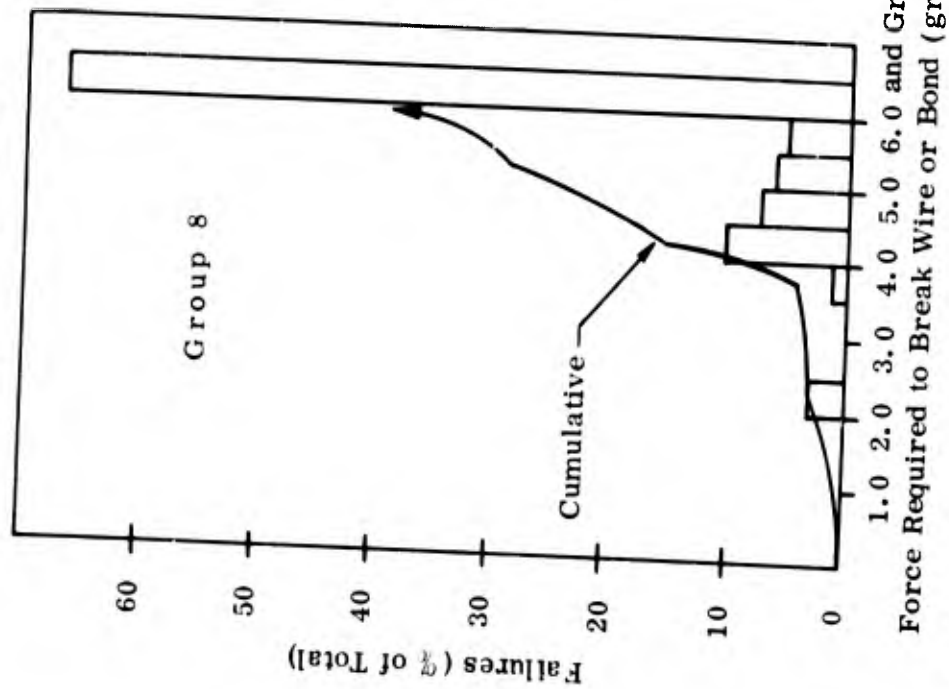
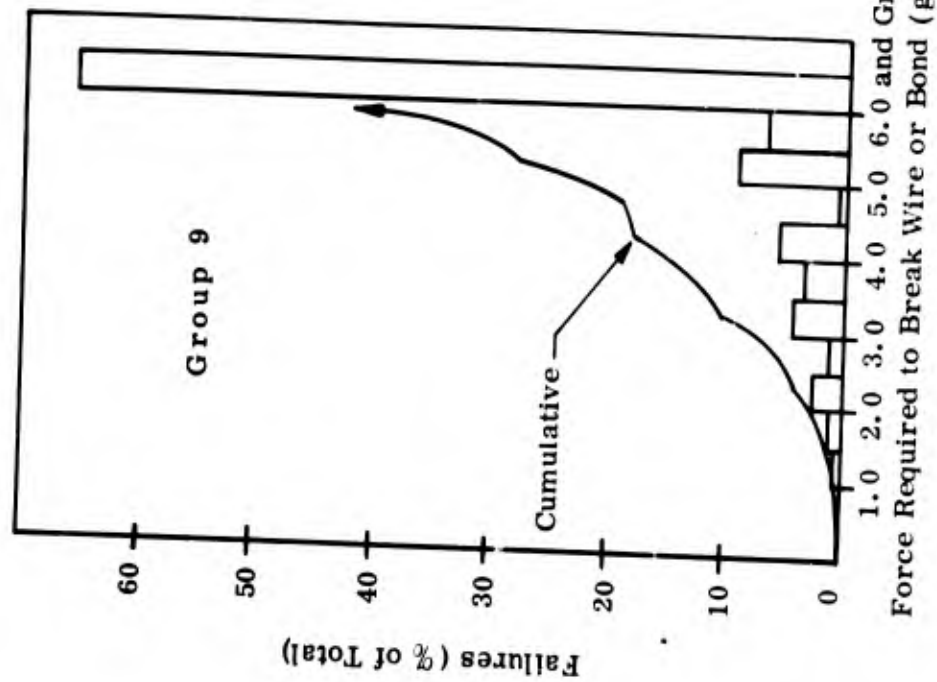


Figure 33. Wire Bond Pull Tests - Group 7 and 8

Background Data:

- Tested After Passing 20, 30, 40, 46, 75, 125, and 150 kg Acceleration in Y_1 Axis
- Serial Numbers 106 - 119
- Total of 156 Wires Pulled



Background Data:

- Tested After Passing 20, 30, 40, 46, 75, 125, and 150 kg Acceleration in the X_2 Axis
- Serial Numbers 92 - 105
- Total of 91 Wires Pulled

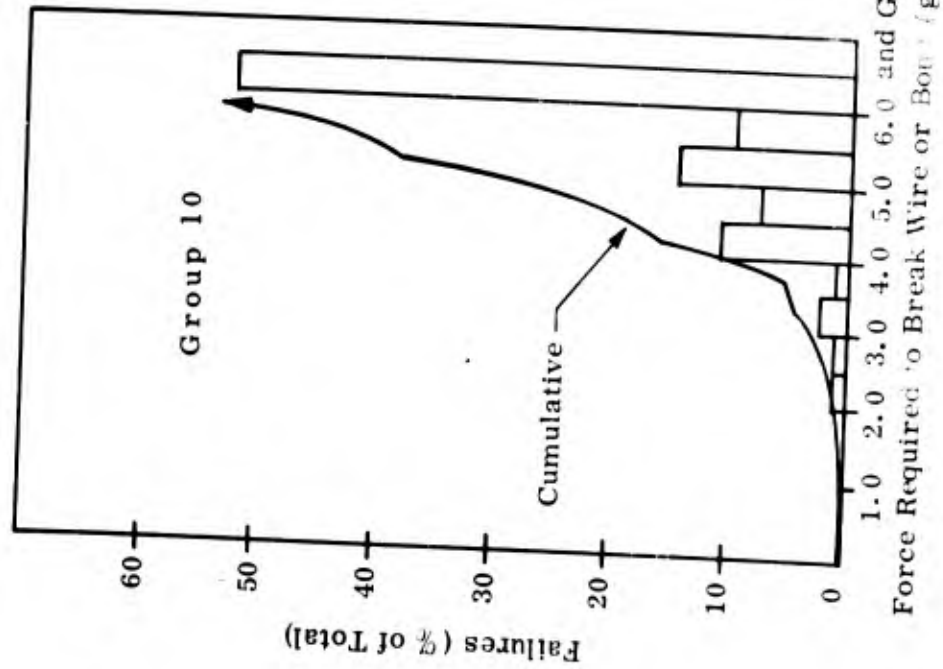
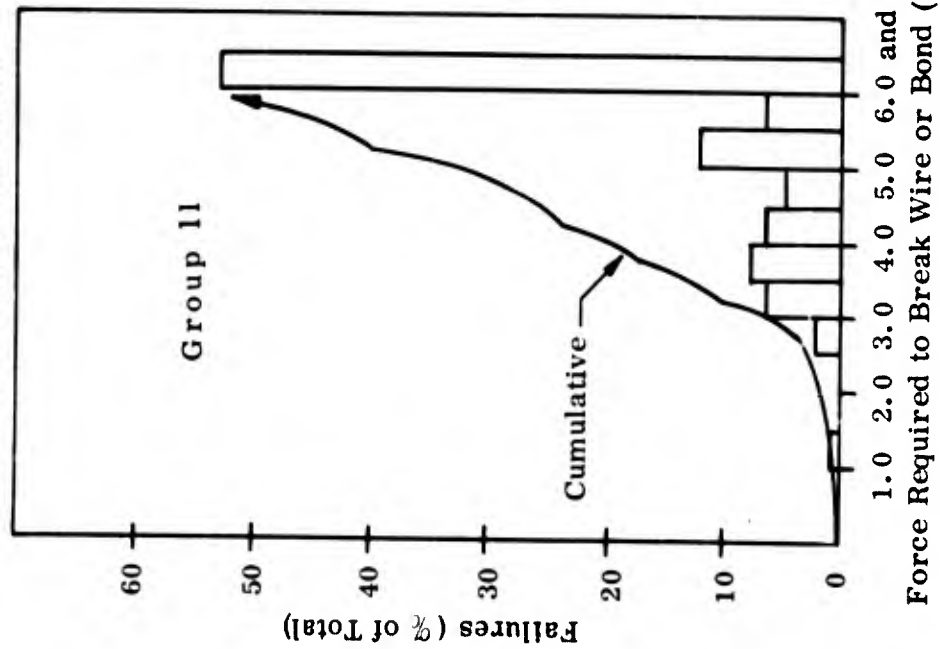


Figure 34. Wire Bond Pull Tests - Group 9 and 10

Background Data:

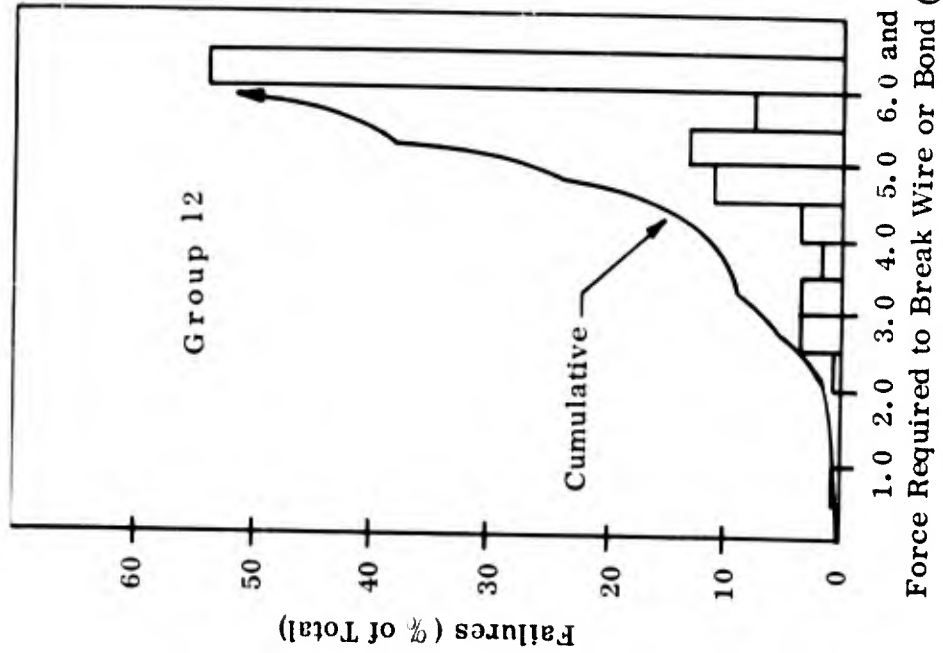
- Tested After Passing 3,758 Hours of Parallel Excitation Life: 1,056 at +125° C, and 2,702 at +150° C
- Serial Numbers 120 - 129 and 150
- Total of 91 Wires Pulled



Force Required to Break Wire or Bond (grams)

Background Data:

- Tested After Passing 3,758 Hours of Reversed Bias Life Test: 1,032 at +125° C and 2,726 Hours at +150° C
- Serial Numbers 130 - 139
- Total of 117 Wires Pulled



Force Required to Break Wire or Bond (grams)

Figure 35. Wire Bond Pull Tests - Group 11 and 12

Figures 36, 37, and 38 show wire pull results for internal leads No. 1, 2, and 10, as defined in Figure 27. Lead No. 1 has a ball bond placed on the gold thick-film conductor on the substrate, and the wedge bond to the gold plated kovar post of the lead frame. Lead No. 2 has a ball bond placed atop a gold wire wedge bond, which goes to the emitter of a PNP transistor. The other end of the lead has a wedge bond going to the aluminum metallization, on top of silicon dioxide, on the resistor chip. Lead No. 10 has the gold ball bond going to the aluminum metallization, on top of silicon dioxide, and a wedge bond going to the gold plated kovar post. Figures 37 and 38 for leads No. 2 and 10 indicate the two extremes in bond integrity for individual leads. Internal lead No. 10 has the strongest bonds, and lead No. 2 the weakest; but neither indicate a serious bond problem.

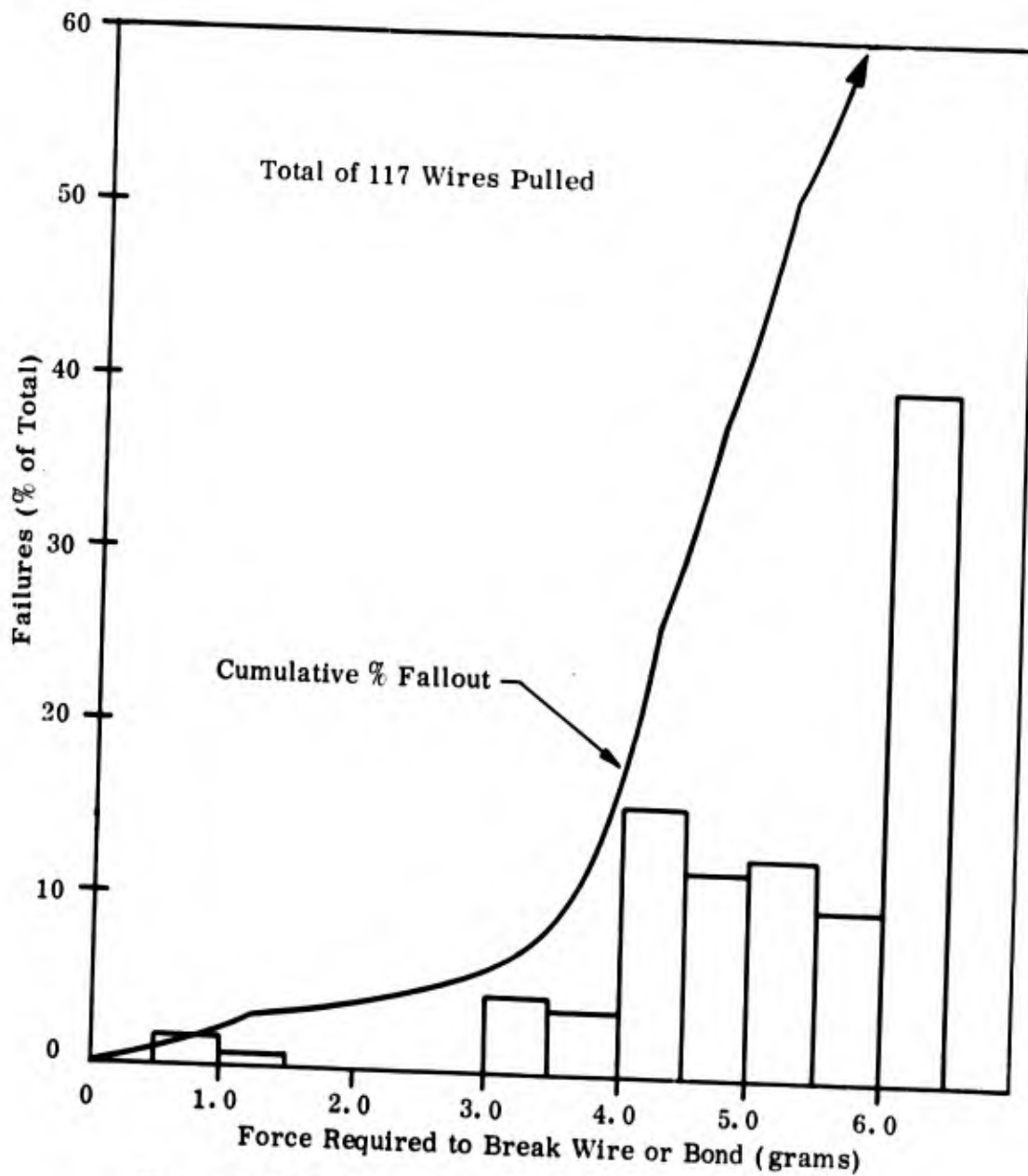


Figure 36. Wire Bond Pull Test — Internal Lead No. 1

From the wire pull data it can be concluded that good gold wire bonds do not de-
 grade significantly in environmental testing, even at very high stress levels, whereas
 poor wire bonds continue to fail all during testing, as exhibited by Manufacturer F's
 history of microcircuit failures. Also note that bonds failed at less than 1 gram pull
 on units which passed 20,000 g acceleration, and at less than 2 grams on units which
 passed 150,000 g acceleration. This indicates that even at very high g levels, accel-
 eration does not create a high force on marginal wire bonds.

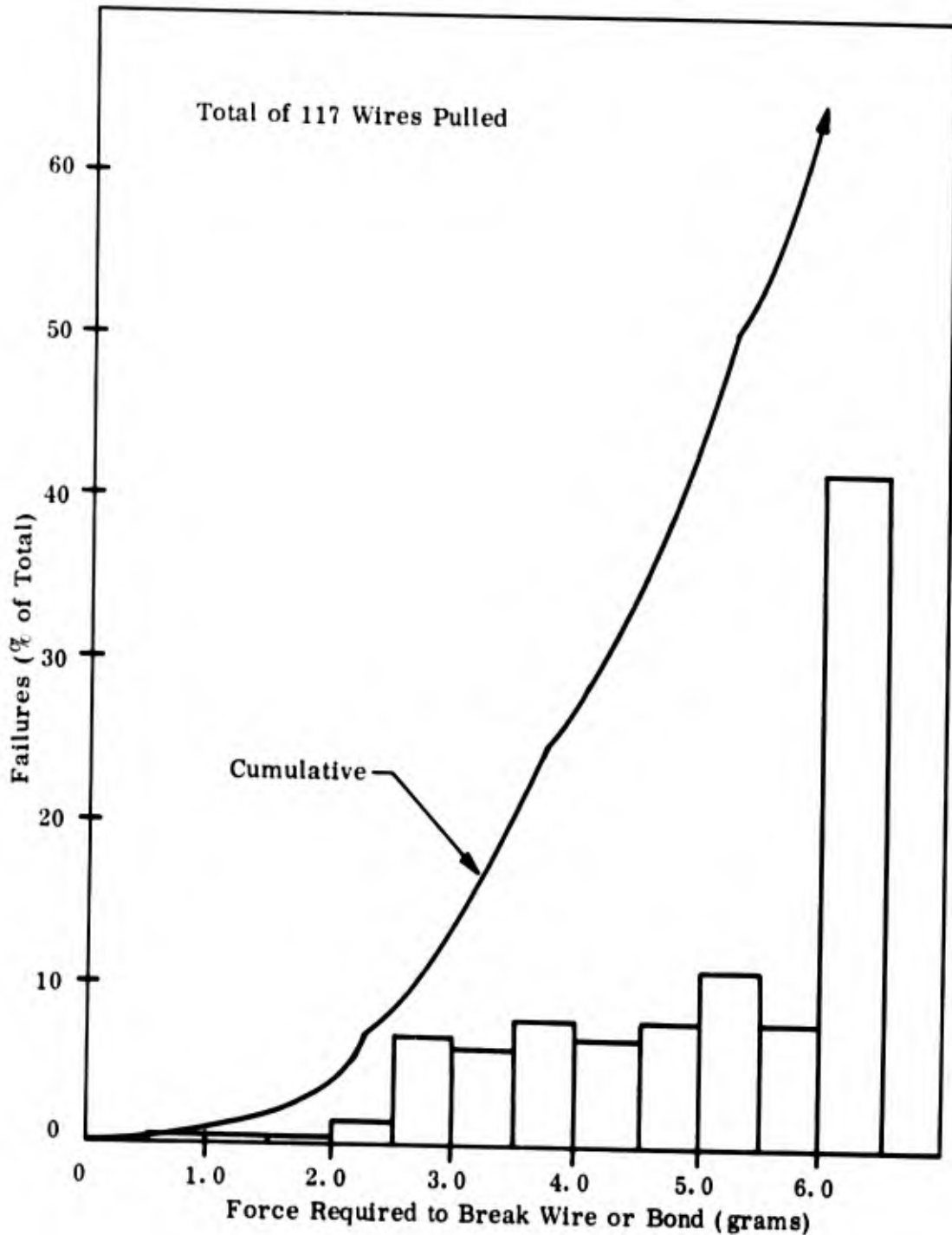


Figure 37. Wire Bond Pull Test - Internal Lead No. 2

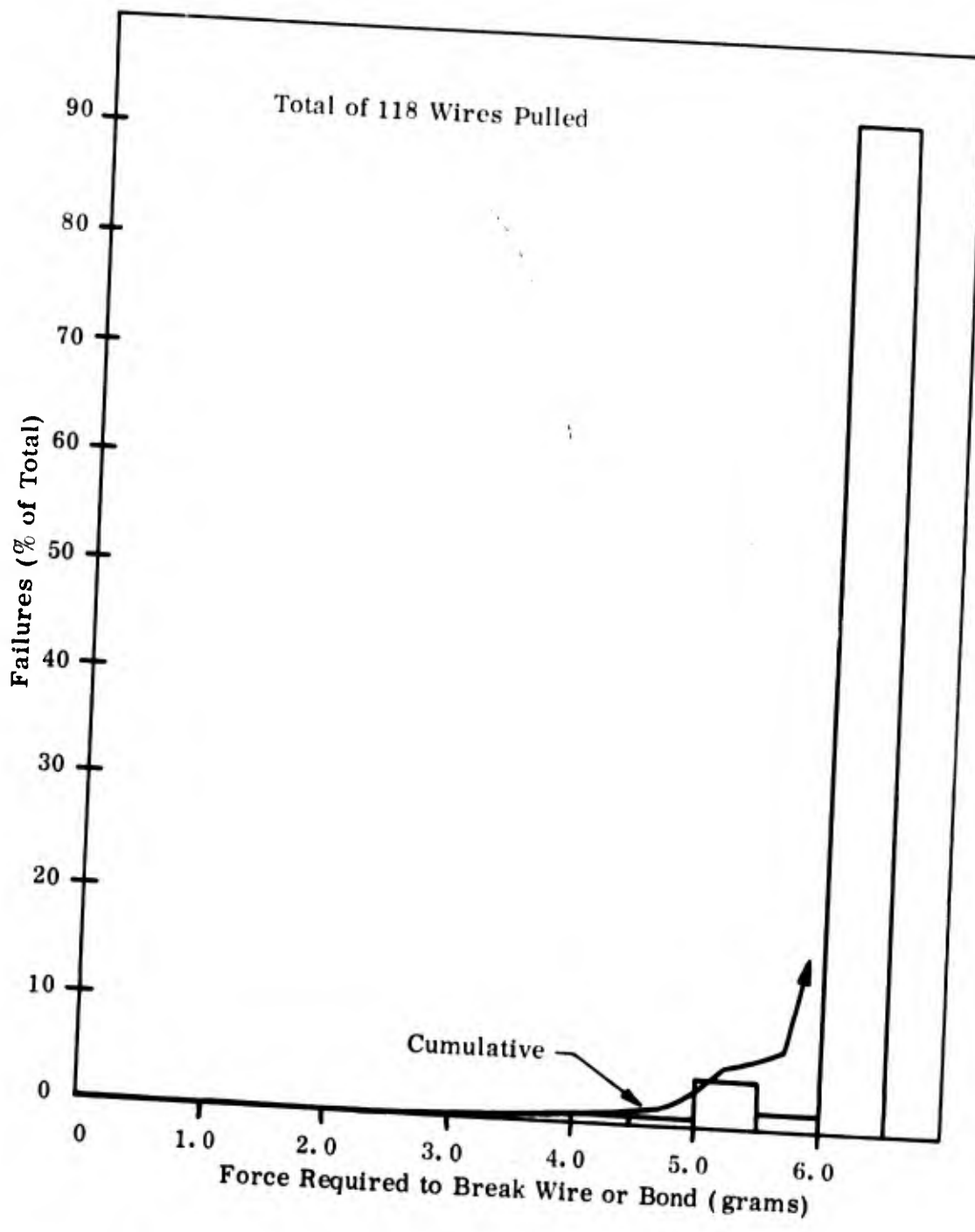


Figure 38. Wire Bond Pull Test - Internal Lead No. 10

2.4.5 CONCLUSIONS ON STEPPED STRESS TESTING

In the stepped stress testing program it was shown that a properly constructed hybrid microcircuit is able to withstand very high stress levels without degradation. During the testing, 36.6 percent of Manufacturer A's hybrids failed. This raises a question as to whether Manufacturer A's hybrids were actually subjected to the required 100 percent screens prior to shipment to Delco, considering the record of the high initial fallout for electrical testing, hermetic seal testing, reverse bias burn-in, and 20,000 g acceleration in the Y_1 axis. After the initial tests, however, Manufacturer A's hybrids performed very well.

Manufacturer B's flatpack hybrid had a 15.3 percent fallout, 26 percent of which was due to a misplaced ball bond. The bond was made in the eutectic area where a transistor chip was scrubbed during chip bonding to the substrate.

Generally, the hybrids of Manufacturers A and B withstood the high stresses and repeated cycles of stresses well, with no damage to good devices when proper fixturing was employed. At high g levels of mechanical shock and acceleration, fixturing becomes a very critical aspect of test.

Manufacturer F's hybrids had a 76 percent fallout during the stepped stress testing. However, Manufacturer F's hybrids are large package items, which cannot be considered typical high-reliability products because:

1. Large size hybrids are difficult to seal, and in many 1-inch² flatpackages it is difficult to hold a hermetic seal during environmental and electrical testing (44 percent of the failures showed hermeticity loss).
2. The manufacturer has a serious gold wire bonding problem (36 percent of the failures showed faulty bonds) with respect to these hybrids.

For these reasons, Manufacturer F's hybrid was unsuitable (in retrospect) for the stepped stress testing program. Having no previous experience with this hybrid manufacturer, Delco was unaware of the supplier's problems at the onset of this contract. The data now available on this unit indicates that it would prove to be unreliable in a high precision aircraft navigation system whose parts would be exposed to vibration, temperature extremes, mechanical shock, and long term operational requirements.

The stepped stress test results do not clearly indicate which tests provide the most effective screens to assure reliable hybrids. For example, the results of temperature cycling from -65°C to $+150^{\circ}\text{C}$, versus thermal shocks from -65°C to $+150^{\circ}\text{C}$, showed no difference in Manufacturers A and B hybrids. Thermal shock testing from -195°C to $+200^{\circ}\text{C}$ offers some potential as an effective screen, but each hybrid would have to be evaluated beforehand to assure that specimens are not degraded due to fatigue of metal from the 395°C temperature excursions. Variable frequency vibration cannot be considered an effective screen, even with levels of 100 g peak. Acceleration in the Y_1 axis

must be performed at least at 40,000 g (and preferably above this level) if realistic forces are to be applied to internal leads and chips, and the integrity of the bonds is to be realistically checked. The main limitation here is in the availability of holding fixtures to perform acceleration above 40,000 g on a production volume basis. Accelerations in the Y_2 axis and the X axis are detrimental to the hybrid's integrity and should not be used for screen testing. They can be employed as evaluation tools to obtain basic data on specific hybrid designs. Mechanical shock appears to be reasonably effective, but difficult to implement on flatpackages or dual in-line packages.

High temperature storage appears to be a useful and very economical means of precipitating poor wire bonds, chip bonds, and faulty chips. Reverse bias life is an effective screen for hybrids that have individual transistor and diode chips. Parallel excitation life is useful for screening out additional failure mechanisms due to higher power dissipation and high current concentrations, which are not revealed in storage life or reverse bias life.

All of the tests contributed to the elimination of faulty hybrids. The relative effectivity of each test can best be adjudged from the verification phase test results in Section III.

SECTION III

VERIFICATION PHASE

3.1 GENERAL

The expressed purpose of MIL-STD-883, Test Methods and Procedures for Microelectronics, was to establish uniform methods and procedures for testing microelectronic devices. Of specific interest was Method 5004, which describes a total lot screening procedure for establishing 3 standard classes (C, B, and A) of test specimen. Each higher class designation corresponds to a higher level product assurance. While Method 5004 ascribes no absolute level of quality or reliability to each standard class level, for a given application, a lesser risk could be assumed in using higher level devices. The tradeoff, of course, is higher cost in identifying the better performers. While the user himself must choose, the options remain unclear without some indication of the basic effectiveness of the screening procedures.

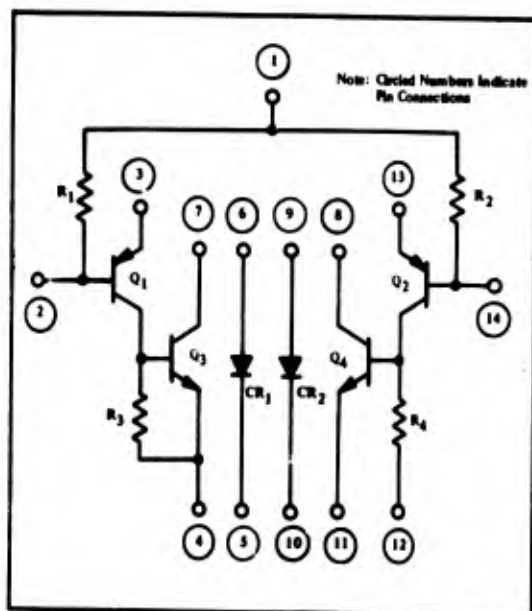
The verification phase generated fallout data from application of Method 5004 screening procedures, first for the Class C level, and then for the Class B and A levels. A Quality Conformance Inspection was also performed on identified Class A-level devices. The specimens tested were 2,249 hybrid microcircuits obtained from 3 suppliers in 2 circuit configurations. For each environmental or mechanical exposure, fallout was recorded and failure mechanism determined.

The test conditions for the data generated during the verification phase were well within the limits that any reliable hybrid microcircuit should be able to withstand. In the study phase, however, the conditions applied were more extreme. Hybrids were accelerated up to 150,000 g in the Y₁, Y₂, and X axes; thermally shocked (335 times) at extremes from -195 to +200°C; temperature cycled (2,023 times) at extremes from -65 to +200°C; vibrated up to 100 g peak; mechanically shocked up to 30,000 g in the Y₁ axis; and life tested over 3,000 hours at ambients up to +150°C. The resultant experience gained by Delco in each test phase, and from visits to Manufacturers A and B, provided considerable insight into how hybrid production uncertainties relate to performance limitations, particularly those identified by application of Method 5004.

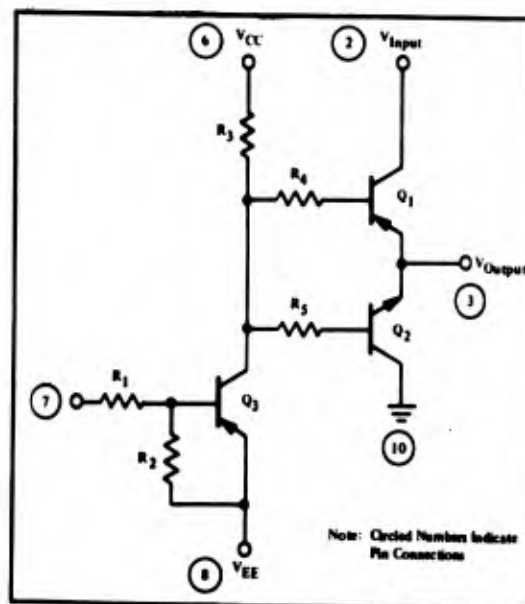
3.2 DESCRIPTION OF CIRCUITS USED

Circuit schematics and actual photomicrographs of the hybrid microcircuits tested are shown in Figures 39 and 40. Circuit X, a Dual Memory Hybrid Switch, uses Q₃ and Q₄ to switch 450 mA with a maximum saturation voltage of 500 mV. Its inputs are driven by TTL logic levels. Circuit Y, a Ladder Switch and Driver, is driven by TTL logic levels at pin 7, and its output at pin 3 switches between ground and a reference voltage at pin 2. Q₁ and Q₂ operate in the inverse mode with 2 mV maximum allowable offset without load, and 4.2 mV (or 30 Ω max. series resistance) with a 20kΩ load.

Manufacturer A's flatpack is $1/4'' \times 3/8''$ for Circuit X and $1/4'' \times 1/4''$ for Circuit Y, and has a gold plated kovar bottom and top. The sidewalls are glass and the package is hermetically sealed by soldering the top onto a gold plated kovar window frame in a belt furnace. All chips are alloyed down to a ceramic substrate having thick-film gold conductors on the top and thick-film gold on the bottom. The substrate itself is alloyed to the gold plated kovar package bottom. Resistors in Circuit X are entirely thick-film cermet. Those in Circuit Y are thick-film cermet plus 4 diffused resistors in 2 silicon chips. Interconnects are made by 0.7- or 1-mil gold flying wires having thermocompression ball bonds on one end and wedge bonds on the other. The chip metallization is thin-film aluminum, and the lead frame is gold plated kovar.



a. Circuit X - Dual Memory Hybrid Switch



b. Circuit Y - Ladder Switch and Driver

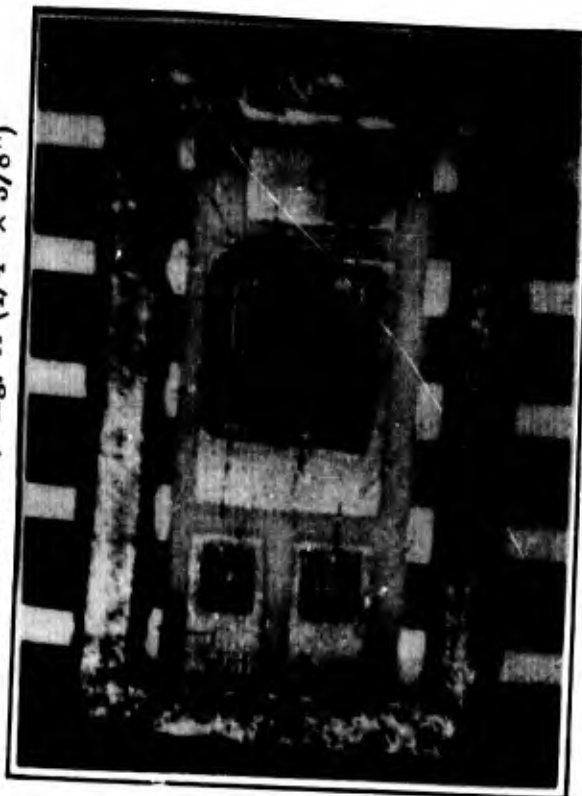
Figure 39. Circuit Types Tested



a. Circuit X/Mfg. A (1/4" x 3/8")



b. Circuit Y/Mfg. A (1/4" x 1/4")



c. Circuit Y/Mfg. B (1/4" x 1/8")



d. Circuit Y/Mfg. C (1/4" x 1/4")

Figure 40. Flatpack Types Tested

Manufacturer B's flatpack for Circuit Y is $1/4" \times 1/8"$, and has a ceramic bottom—that also serves as the substrate—and a gold plated kovar top. The sidewalls are glass, and the top is hermetically sealed to a gold plated kovar window frame by soldering in a belt furnace. The chips are alloyed down to the thick-film gold on the substrate. The 5 resistors are thin-film nichrome, deposited on silicon dioxide, on a single silicon chip. Interconnects are made by 1-mil gold flying wires having thermocompression ball bonds on one end and wedge bonds on the other. Chip metallization and the lead frame are the same as described for Manufacturer A.

Manufacturer C's flatpack for Circuit Y is $1/4" \times 1/4"$ and uses 0.7-mil gold wires for the interconnects. Otherwise, its physical description is the same as that for Manufacturer B's unit. All 3 suppliers are relatively large-scale manufacturers with extensive experience in making this type of device.

3.3 MANUFACTURER PRESHIPMENT REQUIREMENTS

The hybrids used for this phase were purchased to Specification Control Drawings (SCD's) from suppliers then producing the same devices for Delco internal programs. The actual procurement documents used are in Appendix I of this book. The procurement terms explicitly required no screening other than 100 percent precap visual and 100 percent fine and gross hermetic seal testing per MIL-STD-883, 100 percent electrical testing at $+25^{\circ}\text{C}$, and sample electrical inspection* of specified parameters at -55 and $+125^{\circ}\text{C}$. The 100 percent precap internal visual inspection was monitored at the supplier's facility by a Delco representative. The precap internal visual inspection requirements were negotiated as specific conditions which each manufacturer was to fit to his particular design and processes. The inspection conditions were similar to those in Method 2010.1, Condition B, of MIL-STD-883.

3.4 EVALUATION OF RESULTS

Fallout experienced in screening for Class C-level parts is shown in Table XI. The data are presented in 8 groupings, along with the average loss for all test groups. Where more than one grouping is shown for the same supplier, the units are grouped by data code of shipment (different production lots). Group 1 parts, for example, arrived in March, and Group 7 parts in September.

The hybrids in Group 8 were originally in Group 6. Immediately after failing the initial series resistance test, they were separated from Group 6 and regrouped for continued testing as Group 8. Except for being slightly over the 30Ω limit, they were good products. Losses shown for Group 8 are therefore those over and above the out-of-spec limit that led to the new grouping.

*For Circuit X, the specified LTPD (Lot Tolerance Percent Defective per MIL-M-38510) was 10, with a max. acceptance number of 3. For Circuit Y, the specified LTPD was 5, with a max. acceptance number of 3.

Table XI. Test Results, Screening for Class C Units

TEST AREA	TEST DESCRIPTION	MEAS UNIT	DATA BY TEST GROUP NO.								AVE. LOSS	
			1	2	3	4	5	6	7	8*		
Initial Conditions	1	Circuit Type Mfg. Code	X/A	X/A	Y/A	Y/A	Y/B	Y/C	Y/C	Y/C		
		Unit Distribution by Group (Total = 2,249 Units)	448	171	193	307	499	444	89	(87)		
Pre-Class C Screening Test	2	External Visual Inspection per MIL-STD-883, Method 2009, and Serialization	0.67	0	0	0	0	0	0	(0)	0.13	
	3	Electrical Testing	+25°C	29.2	2.34	0	0	0.40	6.08	0	(26.4)	7.52
			+125°C	2.85	0.62	1.03	0	1.00	0	0	(0)	0.80
			+55°C	0	3.59	5.18	1.63	0	12.75	2.25	(88.5)	5.15
4	Total External Visual and Electrical	31.9	6.43	5.18	1.63	1.40	18.1	2.25	(100)	12.3		
Class C Screening Test	5	Units Screened by Group (Total = 2,095 Units)	305	171	193	307	499	444	89	87		
	6	High Temperature Stabilization per MIL-STD-883, Method 1008, Cond. C., 48 Hours (min) at 150°C	0.66	0.62	0.52	0	1.40	0	0	1.15	0.57	
		Electrical +25°C										
	7	Temperature Cycling per MIL-STD-883, Method 1010, Cond. C; 10 Cycles, -65°C to +150°C; Transfer Time Less than 1 Minute	0	0	0	0	0.81	0	1.12	0	0.23	
		Electrical +25°C										
	8	Acceleration per MIL-STD-883, Method 2001, Cond. F; 30,000 g on Y ₁ Axis	2.30	0	9.90	6.85	0.80	0.23	6.82	1.15	2.82	
		Fine Seal Test per MIL-STD-883, Method 1014, Cond. A; Max Leak Rate of 1 x 10 ⁻⁷ Atm cc/s										
		Gross Seal Test per MIL-STD-883, Method 1014, Cond. C, Step 2	1.98	2.50	5.74	4.90	8.00	0.68	2.27	0	3.87	
		Electrical +25°C	1.01	2.56	0.52	0.33	0.45	0.90	0	0	0.71	
	9	Total Fallout - Including Pre-Screening Test Loss	34.4	10.5	15.5	8.15	12.4	20.0	9.00	100	18.0	
Total Fallout - Not Including Pre-Screening Test Loss		3.60	5.63	10.9	6.85	11.1	2.26	7.87	2.30	6.53		

* - Parts that originated as part of Group 6, then became Group 8 after electrical testing showed them to be marginally out of limit. Therefore, the initial Group 8 data (in parenthesis) are preliminarily contained in that of Group 6, and do not redundantly enter into the unit total and averages shown.

Most of the failures detected in the study were due to opens, shorts, or improper hermetic sealing. In Table XI, for example, the external visual test fallout was due to missing external leads. Conversely, none of the initial electrical test failures was catastrophic, but only failure to meet the electrical limits of the procurement SCD. A high percentage of failure at initial electrical inspection was not uncommon despite the procurement requirements of 100 percent electrical testing at +25°C and sample inspection at temperature extremes.

Fallout was determined by electrical testing, after each screen, to detect units out of the SCD limits. Those evidencing catastrophic failures were removed from test. Those that drifted out of limits but otherwise continued to operate were permitted to continue. Fallout was noted for a given condition only when a new failure was recognized. The specimens progressed in this manner from Class C, to B, to A screening. While this test sequence for arriving at Class A units deviates slightly from that of Method 5004, the overall result is the same.

It is apparent with this test sequence, however, that a given environmental or mechanical test could influence the data of a later test. Temperature cycling, for example, could cause loss of hermeticity before acceleration testing, with no intermediate seal test to disclose this condition. Wire bonds could similarly degrade through temperature cycling to the point of opening later at 30,000 g acceleration. This consideration makes overall fallout for each screening class the most significant data, with intermediate figures useful only as indicators of approximate fallout from each screen. Appendix III has the detailed test conditions and test results in chronological order for each test group, with a description of the failure mechanisms for each screen performed during the verification phase.

The upgrading of Class C parts to Class B and then A is depicted in Tables XII and XIII. Note, in Table XII, that Class B screening is limited to a 168-hour operating burn-in at +125°C, yielding a modest 0.63 percent average fallout. A 72-hour reverse bias burn-in would have increased the average loss to 2.02 percent, according to Table XIII, Item 10.

The Class A test results in Table XIII are complicated by acceleration introduced at various points in the screening sequence. In Test Area 4, for instance, Groups 7 and 8 were accelerated prior to mechanical shock to compare the affect of a Y_1 axis acceleration of 40,000 g with that of a Y_1 axis mechanical shock of 20,000 g. The comparison gave no clear edge to either test, but did indicate that both may be required to weed out marginal units, despite the difficulty in shocking flatpacks in production quantities. Test results for Groups 6 and 7, after initial Y_1 axis acceleration, indicated loose ball bonds, loose transistor chips, and broken wires at points where bonding tools form wedge bonds.

Table XII. Test Results, Screening for Class B Units

TEST AREA	TEST DESCRIPTION	MEAS UNIT	DATA BY TEST GROUP NO.								AVE. LOSS
			1	2	3	4	5	6	7	8	
Initial Conditions	Circuit Type/Mfg. Code		X/A	X/A	Y/A	Y/A	Y/B	Y/C	Y/C	Y/C	
	Test Sample Distribution (Total = 2,071 Units)	-	299	164	193	306	495	439	88	87	
Pre-Class B Screening Test Loss **	Class C Fallout - Including Pre-Screening Loss	% Loss	34.4	10.5	15.5	8.15	12.4	20.0	9.00	100**	18.0
	Class C Fallout - Not Including Pre-Screening Loss	% Loss	3.60	5.63	10.9	6.85	11.1	2.26	7.87	2.30	6.53
Class B Screening Test	Burn-In* per MIL-STD-883, Method 1015, Cond. D; 168 Hours at +125°C	% Loss	1.02	0.61	1.57	1.64	0.23	0	0	0	0.63
	Electrical +25°C										
4	Total Fallout - Including Class C Screening Loss and Pre-Class C Screening Loss	% Loss	35.0	11.1	16.6	9.78	12.6	20.0	9.00	100**	18.5
	Total Fallout - Not Including Pre-Class C Screening Loss	% Loss	4.60	6.25	12.0	8.47	11.4	2.26	7.87	2.30	7.07

* - Parallel Excitation Operation.

** - See Table XI.

Table XIII. Test Results, Screening for Class A Units

TEST AREA	TEST DESCRIPTION	MEAS UNIT	DATA BY TEST GROUP NO.								AVE. LOSS
			1	2	3	4	5	6	7	8	
Initial Conditions	Circuit Traps, Mfg. Code	-	X/A	X/A	Y/A	Y/A	Y/B	Y/C	Y/C	Y/C	
	Test Sample Distribution (Total Sample = 2,070 Units)		299	164	193	306	494	439	88	87	
Class A Screening Test	Thermal Shock per MIL-STD-883, Method 1011, Cond. C: 15 Cycles, -65°C to +150°C, Liquid-to-Liquid	% Loss	0	0.61	0	0	0.23	0.46	1.14	0	0.24
	Electrical +25°C										
	Mechanical Shock per MIL-STD-883, Method 2002, Cond. F: V ₁ Axis, 1 Shock, 20,000 g Peak		8.42	1.23	0	0	0.20	0	NP	NP	1.48
	Packages Damaged										
	Electrical +25°C		8.93	17.3	3.19	0.33	0.46	2.10	NP	NP	3.75
	Acceleration per MIL-STD-883 Method 2001, 40,000 g, V ₁ Axis		NP	NP	NP	NP	NP	NP	6.82	1.15	4.00
	Electrical +25°C										
	Mechanical Shock per MIL-STD-883, Method 2002, Cond. F: V ₁ Axis, 1 Shock, 20,000 g Peak		NP	NP	NP	NP	NP	NP	0	0	0
	Packages Damaged										
	Electrical +25°C		NP	NP	NP	NP	NP	NP	2.44	1.15	1.78
	Acceleration per MIL-STD-883, Method 2001, Cond. E: 30,000 g, V ₂ Axis		2.06	NP	0.55	0	0.93	30.8	NP	NP	8.98
	Electrical +25°C										
	Acceleration per MIL-STD-883, Method 2001, Cond. E: 30,000 g, V ₁ Axis		NP	7.70	NP	NP	NP	NP	NP	NP	7.70
	Electrical +25°C										
	Acceleration per MIL-STD-883, Method 2001, 40,000 g, V ₁ Axis		NP	NP	NP	NP	NP	1.63	NP	NP	1.63
Electrical +25°C											
Burn-In* per MIL-STD-883, Method 1015, Cond. D: 72 Hours at +125°C	0	0	1.10	0.33	0.23	0	1.22	0	0.28		
Electrical +25°C											
Reverse Bias Burn-In per MIL-STD-883, Method 1015, Cond. A: 72 Hours at +150°C	1.70	0	2.23	1.00	5.41	0.27	0	1.41	2.02		
Electrical +25°C											
Acceleration per MIL-STD-883, Method 2001, Cond. E: 30,000 g, V ₂ Axis	NP	14.9	NP	NP	NP	NP	NP	NP	14.9		
Electrical +25°C											
Acceleration per MIL-STD-883, Method 2001, 40,000 g, V ₂ Axis	NP	NP	0	NP	2.48	NP	NP	NP	1.82		
Fine Seal Test per MIL-STD-883, Method 1014, Cond. A: Max. Leak Rate of 1 x 10 ⁻⁷ Atm-cc/s											
Gross Seal Test per MIL-STD-883, Method 1014, Cond. C, Step 2	NP	NP	1.12	NP	4.26	NP	NP	NP	3.36		
Electrical +25°C	NP	NP	1.70	NP	7.23	NP	NP	NP	5.54		
Electrical +55°C	NP	NP	1.72	NP	0.27	NP	NP	NP	0.73		
Electrical +125°C	NP	NP	0.58	NP	4.58	NP	NP	NP	3.30		
Acceleration per MIL-STD-883, Method 2001, 40,000 g, V ₁ Axis	4.24	16.7	1.12	0.35	0.64	1.36	0	1.16	2.26		
Fine Seal Test per MIL-STD-883, Method 1014, Cond. A: Max. Leak Rate of 1 x 10 ⁻⁷ Atm-cc/s											
Gross Seal Test per MIL-STD-883, Method 1014, Cond. C, Step 2	42.4	61.5	0	3.80	1.06	1.63	1.28	1.16	10.65		
Electrical +25°C	8.60	6.30	2.28	0.67	0.56	2.17	5.13	3.49	2.93		
Electrical +55°C	2.33	0	1.75	0.68	0	0.61	3.85	0	0.97		
Electrical +125°C	3.85	0.95	0	0.68	3.70	0	2.56	2.32	1.70		
X-Ray per MIL-STD-883, Method 2012	0	0	0	0	0	0	0	0	0		
External Visual Inspection per MIL-STD-883, Method 2009	0	0	0	0	0	0	0	0	0		
Total Failout Including Class B and C Screening Losses and Pre-Screening Losses	74.5	80.0	27.0	16.0	26.5	35.4	30.4	100**	41.0		
Total Failout Including Class B and C Screening Losses but Not Including Initial Electrical Test Losses	62.3	78.7	21.8	14.3	25.4	20.5	30.4	12.6	31.4		

* - Parallel Excitation Operation
 ** - See XI, Group 8
 NP - Not Performed

The effect of acceleration after burn-in is demonstrated in Test Area 13 (Table XIII). Groups 7 and 8 show a 5.13 and 3.49 percent loss, respectively, after exposure to a second 40,000 g, Y₁ axis acceleration. Failure mechanisms here were broken wedge bonds and an open ball bond going to aluminum metallization. Acceleration levels higher than the 30,000 g specified in Method 5004 are clearly needed to properly exercise weak wire, chip, and substrate bonds. Hybrids of this size were accelerated without damage at over 100,000 g in the referenced contract's study phase. The 40,000 g limit shown in the tables was the maximum obtainable with the production fixturing available during this phase.

Method 5004 specifies acceleration in the Y₂ axis and, while this was duly performed, results indicated that this type of testing should be limited to evaluating non-production parts. For production units, it is a risky requirement since after Y₂ axis acceleration, all internal leads are not redressed by subsequent Y₁ axis acceleration. Some remain so deformed as to remain in contact with chip edges, or shorted to conductors on the substrate, even after exposure to 40,000 g acceleration in the Y₁ axis. Moreover, not all shorts were detectable with the +25°C electrical test, but were manifested only at -55°C or +125°C. Still others pass all electrical tests, only to complete shorting out in later application.

Radiographic examination in 2 axes with a TV system appeared to be ineffective as a screening tool. The typical hybrid is effectively shielded by multileveled interconnect wires and chips and relatively thick lids and substrates. Many units examined appeared to contain large foreign bodies, which were subsequently shown to be part of the firmly attached gold eutectic. In these cases, slight ridging was created outside a chip's outline during scrubbing for chip attachment, and this does not harm the hybrid's operation. In other cases, the appearance of a large foreign object was created by solder wetting the package lid inside the seal ring. On the other hand, silicon and aluminum showed poorly on X-rays, and many particles large enough to bridge conductors can still be too small to see under X-rays.

A less complicated summary of Class A screening is given in Table XIV, which consolidates Y₁ axis acceleration and mechanical shock losses to reflect overall fallout. Test Item 7 indicates the importance of final 100 percent electrical testing, at -55° and +125°C, of all parts likely to operate at such temperature extremes. In Table XI, pre-Class C electrical test losses ranged from 0 to 12.75 percent, and averaged 5.15 percent at -55°C and 0.8 percent at +125°C. In Table XIV, after all screening, additional electrical test losses ranged from 0 to 3.85 percent, and averaged 1.19 percent at -55°C and 2.7 percent at +125°C.

Test results in Table XV indicate the value of EPT* sampling for Quality Conformance Inspection. These tests were performed on a sample of each of the 8 groups after they had completed Class A screening. This lot inspection proves that 100 percent screening by itself is not completely effective in excluding faulty or marginal units. To assess the quality of each specific hybrid lot, a sample should be pulled

*-Extended Performance Test (EPT) program, used at Delco Electronics as part of the lot acceptance criteria.

for Quality Conformance Inspection. Delco routinely performs such testing on each microcircuit lot, and considers it an effective aid to quality assurance for specific applications. (The test results for EPT over a period of time were reported in Paragraph 2.3.3.2 of the study phase report.)

Table XIV. Class A Screening Test Results, Re-Presented for Clarity

TEST AREA	TEST DESCRIPTION	MEAS UNIT	DATA BY TEST GROUP NO.								AVE. LOSS	
			1	2	3	4	5	6	7	8		
Initial Conditions	1	Circuit Type/Mfg. Code	X/A	X/A	Y/A	Y/A	Y/B	Y/C	Y/C	Y/C	-	
		Test Sample Distribution (Total Sample = 2,070 Units)	299	164	193	306	494	439	88	87		
Class A Screening Test	2	Thermal Shock per MIL-STD-883, Method 1011, Cond. C; 15 Cycles -65°C to +150°C, Liquid-to-Liquid	0	0.61	0	0	0.23	0.46	1.14	0	0.24	
		Electrical +25°C										
	3	Acceleration per MIL-STD-883, Method 2001; 30,000 to 40,000 g in Y ₂ Axis	2.06	14.9	2.19	0	7.67	30.8	NP	NP	11.2	
		Electrical +25°C										
	4	Burn-In* per MIL-STD-883, Method 1015, Cond. D; 72 Hours at +125°C	0	0	1.10	0.33	0.23	0	1.22	0	0.28	
		Electrical +25°C										
	5	Reverse Bias Burn-In per MIL-STD-883, Method 1015, Cond. A; 72 Hours at +150°C	1.70	0	2.23	1.00	5.41	0.27	0	1.41	2.02	
		Electrical +25°C										
	6	Mechanical Shock per MIL-STD-883, Method 2002, Cond. F; Y ₁ Axis, 1 Shock at 20,000 g Peak, and Acceleration per MIL-STD-883, Method 2001, 40,000 g, Y ₁ Axis	23.2	29.0	5.32	1.00	1.01	5.48	13.6	5.75	8.52	
		Electrical +25°C										
	7	Fine Seal Test per MIL-STD-883, Method 1014, Cond. A; Max. Leak Rate of 1×10^{-7} Atm-cc/s	4.24	16.7	1.12	0.35	3.11	1.36	0	1.16	2.89	
		Gross Seal Test per MIL-STD-883, Method 1014, Cond. C, Step 2	42.4	61.5	1.12	3.80	5.38	1.63	1.28	1.16		
		Electrical	-55°C	2.35	0	3.44	0.68	0.27	0.81	3.85		0
			+125°C	3.85	0.95	0.58	0.68	8.09	0	2.56		2.32
8	X-Ray per MIL-STD-883, Method 2012	0	0	0	0	0	0	0	0	0		
9	External Visual Inspection per MIL-STD-883, Method 2009	0	0	0	0	0	0	0	0	0		
10	Total Fallout - Including Class B and C Screening Losses and Pre-Screening Losses	74.5	80.0	27.0	16.0	26.5	35.4	30.4	100**	41.0		
	Total Fallout - Including Class B and C Screening Losses But Not Including Initial Electrical Test Losses	62.3	78.7	21.8	14.3	25.4	20.5	30.4	12.6	31.4		

* - Parallel Excitation Operation
 ** - See Table XI, Group 8
 NP - Not Performed

Table XV. Test Results, EPT Sampling for Quality Conformance Inspection

TEST AREA	TEST DESCRIPTION	MIL-STD-883 UNIT	DATA BY TEST GROUP NO.								AVE. LOSS	
			1	2	3	4	5	6	7	8		
Initial Conditions	Circuit Type Mfg. Code		X A	X A	Y A	Y A	Y B	Y C	Y C	Y C		
	Test Sample Distribution (Total Sample = 306 Units)		38	30	38	40	45	45	34	36		
Extended Performance Test	Temperature Cycling per MIL-STD-883, Method 1010, Cond. C: 10 Cycles, -65 C to +150 C	Loss	2.6	0	0	0	0	0	0	0	0.32	
	Reverse Bias Burn-In per MIL-STD-883, Method 1015, Cond. A: 48 Hours at +125 C											
	Electrical +25 C											
	Burn-In* per MIL-STD-883, Method 1015, Cond. D: 168 Hours at +125 C	Loss	0	0	0	0	0	0	0	0	0	
	Electrical +25 C											
	Acceleration per MIL-STD-883, Method 2001, 40.000 g, Y ₁ Axis											
	Lead Pull per MIL-STD-883, Method 2004, Cond. A	Loss	5	4	4	4	5	5	4	4		
	Lead Pull Sample Distribution (Total Sample = 35 Units)											
	Loss Due to Lead Pull		0	0	0	0	0	0	0	0	0	
	Lead Bend per MIL-STD-883, Method 2004, Cond. B	Loss	5	4	4	4	5	5	4	4		
	Lead Bend Sample Distribution (Total Sample = 35 Units)											
	Loss Due to Lead Bend		20	0	0	0	0	0	0	0	2.85	
	Fine Seal Test per MIL-STD-883, Method 1014, Cond. A: Max Leak Rate of 1×10^{-7} Atm-cc-s	Loss	2.7	0	0	0	0	0	0	0	0.32	
	Gross Seal Test per MIL-STD-883, Method 1014, Cond. C, Step 2											
	Electrical +25 C		21.6	10.0	2.63	0	4.45	0	0	0	4.59	
	Internal Visual Inspection per MIL-STD-883, Method 2013	Loss	0	0	0	0	0	2.22	2.94	0	0.98	
	Inspection Sample Distribution (Total Sample = 45 Units)											
	Loss Due to Internal Visual Inspection		10	5	4	4	5	6	5	6		
Internal Bond Pull per MIL-STD-883, Method 2011, Cond. D	Loss	20	20	20	20	13	12	12	12	16		
Number of Wires Pulled per Sample												
Wires whose Thermo Compression Bond Pulled Off, or Broke at 2 gms or Less		1.50	0	1.25	1.25	1.53	8.33	18.3	15.3	4.66		
Units Lost During EPT Sampling	Loss	26	10	5	2	7	7	15	14	10		

* - Parallel Excitation Operation

Distributions of failure mechanisms for the 8 groups tested are shown in Figures 41 through 48, with a composite distribution in Figure 49. In Figures 41 through 45, Manufacturers A and B are shown to be having packaging problems as revealed by the high incidence of hermetic seal failures. Manufacturer A's package is fragile, sensitive to normal handling, and susceptible to temperature cycling and thermal shock. Manufacturer B's package, though not prone to actual breakup, is highly vulnerable to temperature cycling and thermal shock.

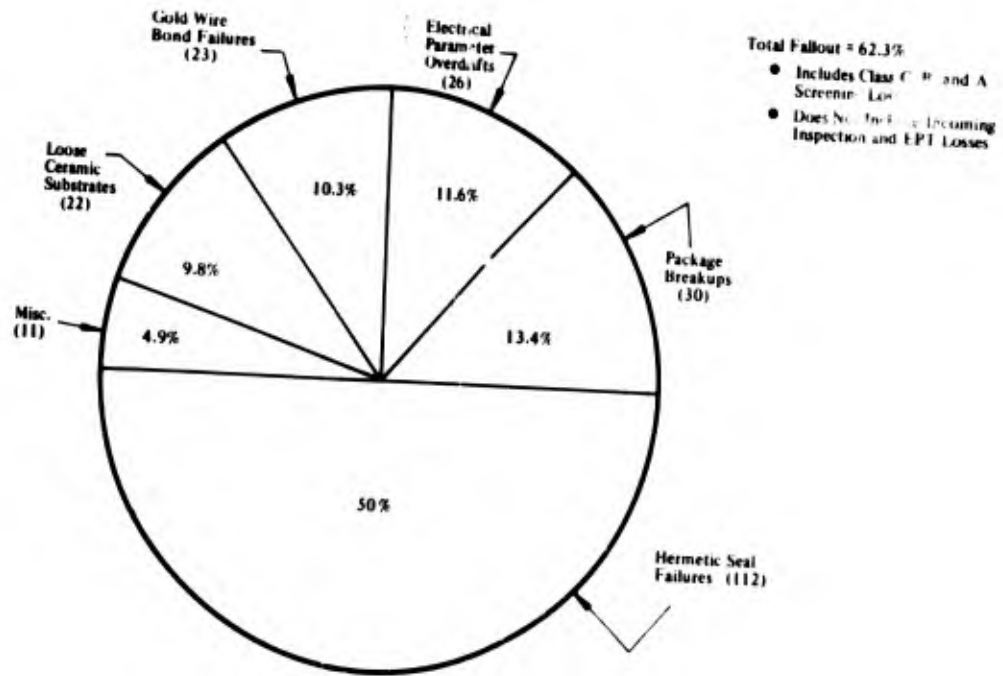


Figure 41. Distribution of Failure Mechanism for Test Group 1

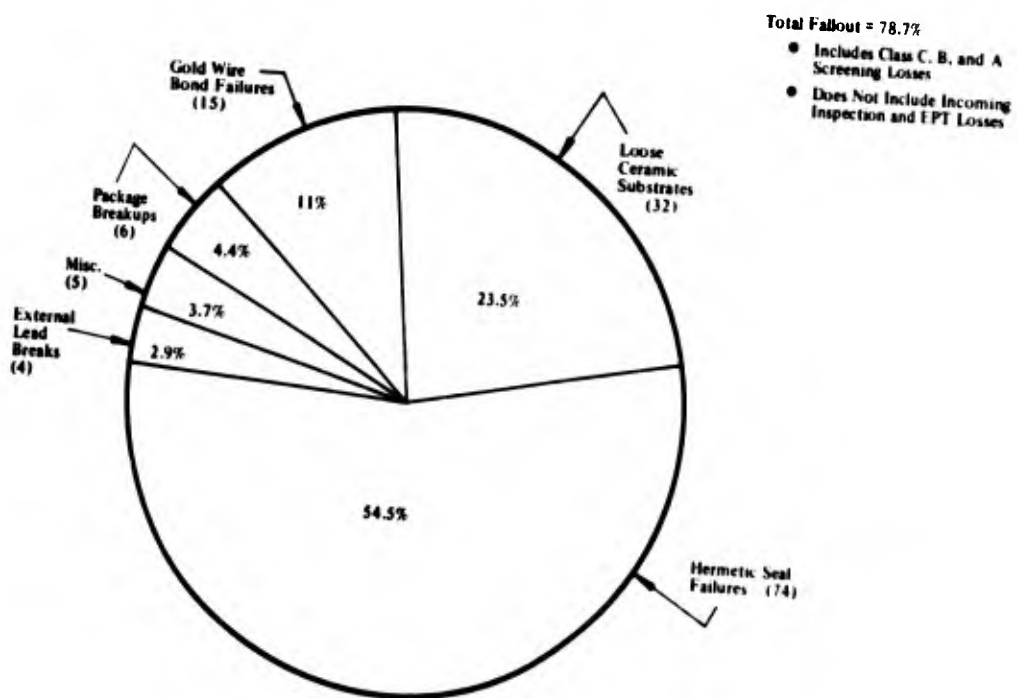


Figure 42. Distribution of Failure Mechanism for Test Group 2

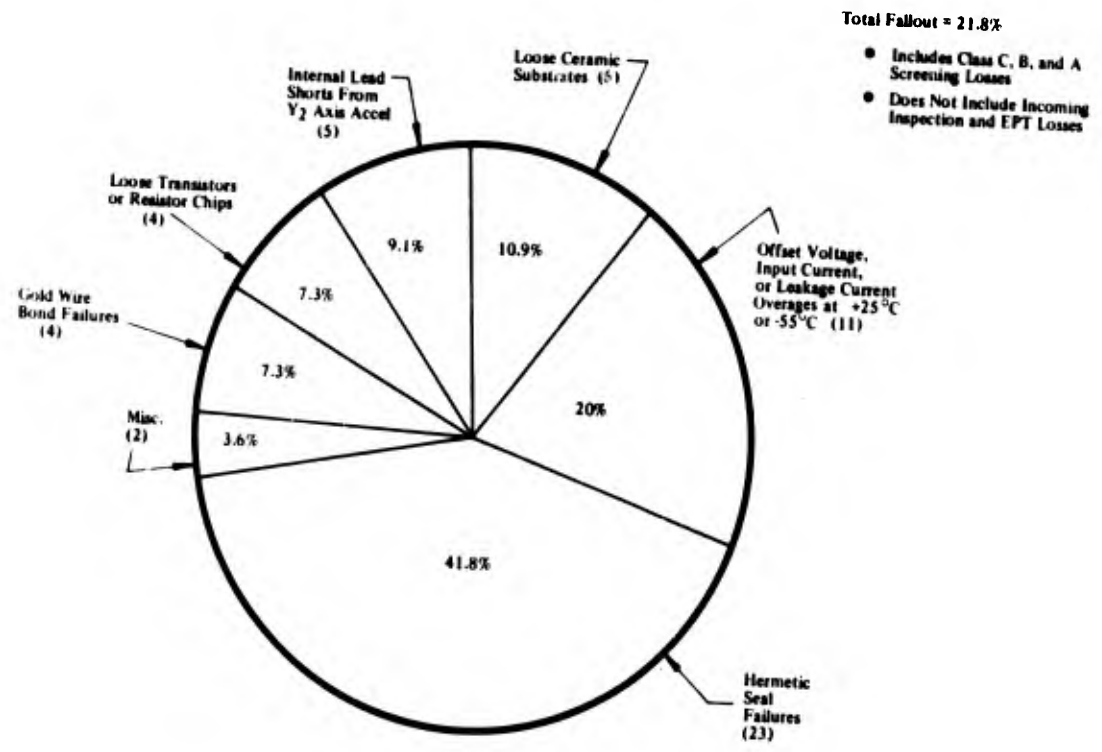


Figure 43. Distribution of Failure Mechanism for Test Group 3

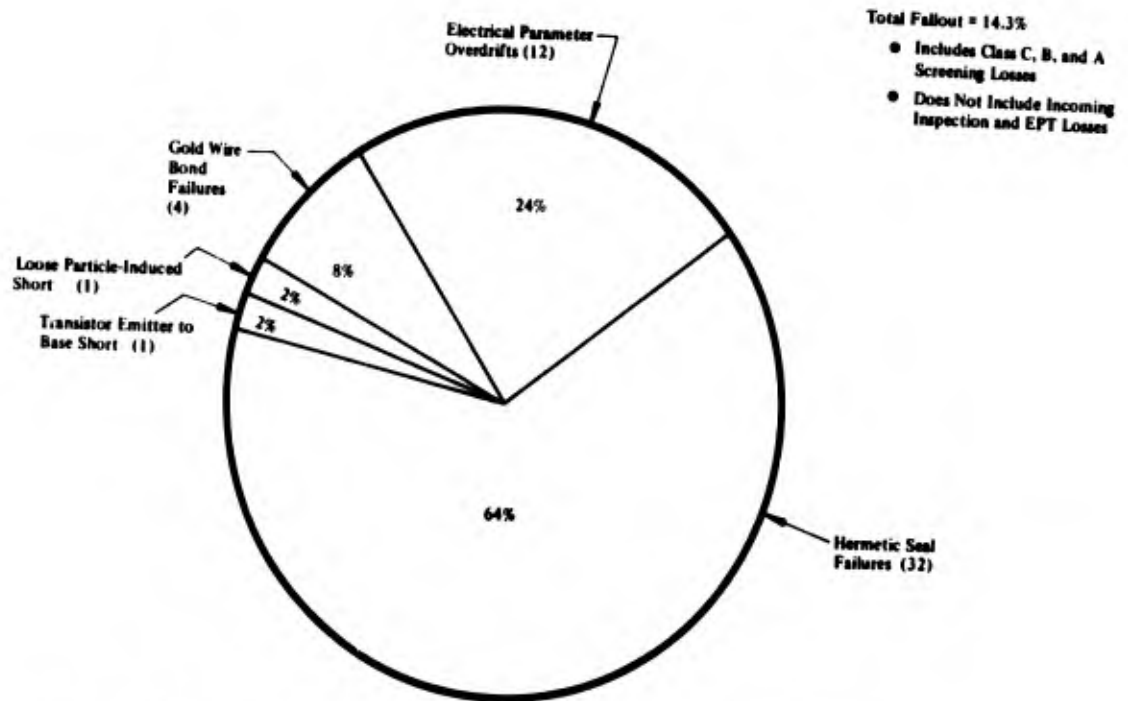


Figure 44. Distribution of Failure Mechanism for Test Group 4

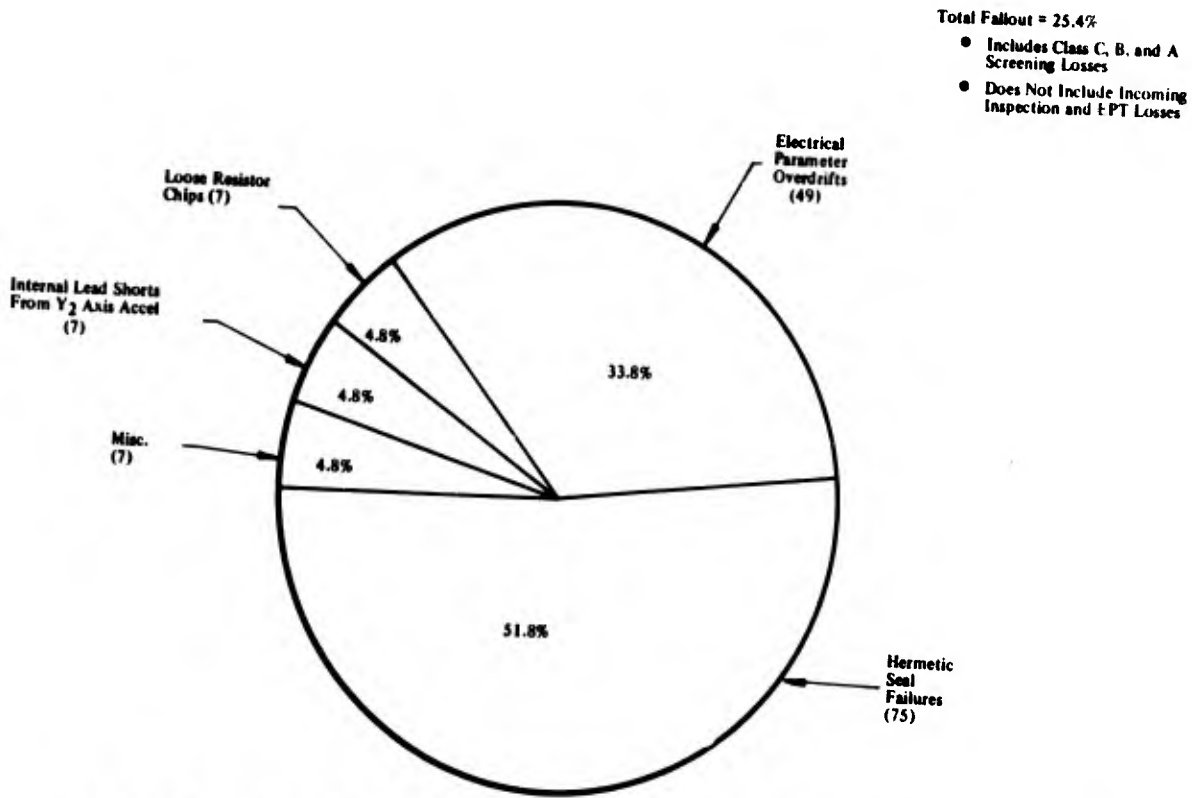


Figure 45. Distribution of Failure Mechanism for Test Group 5

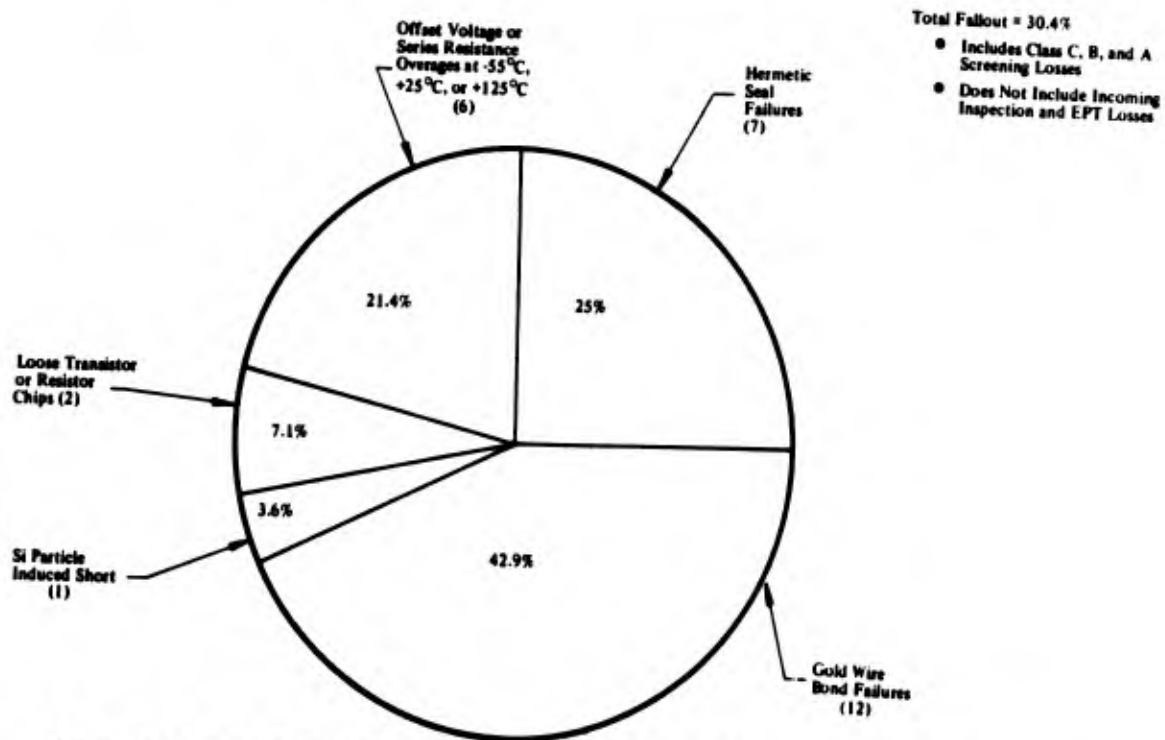
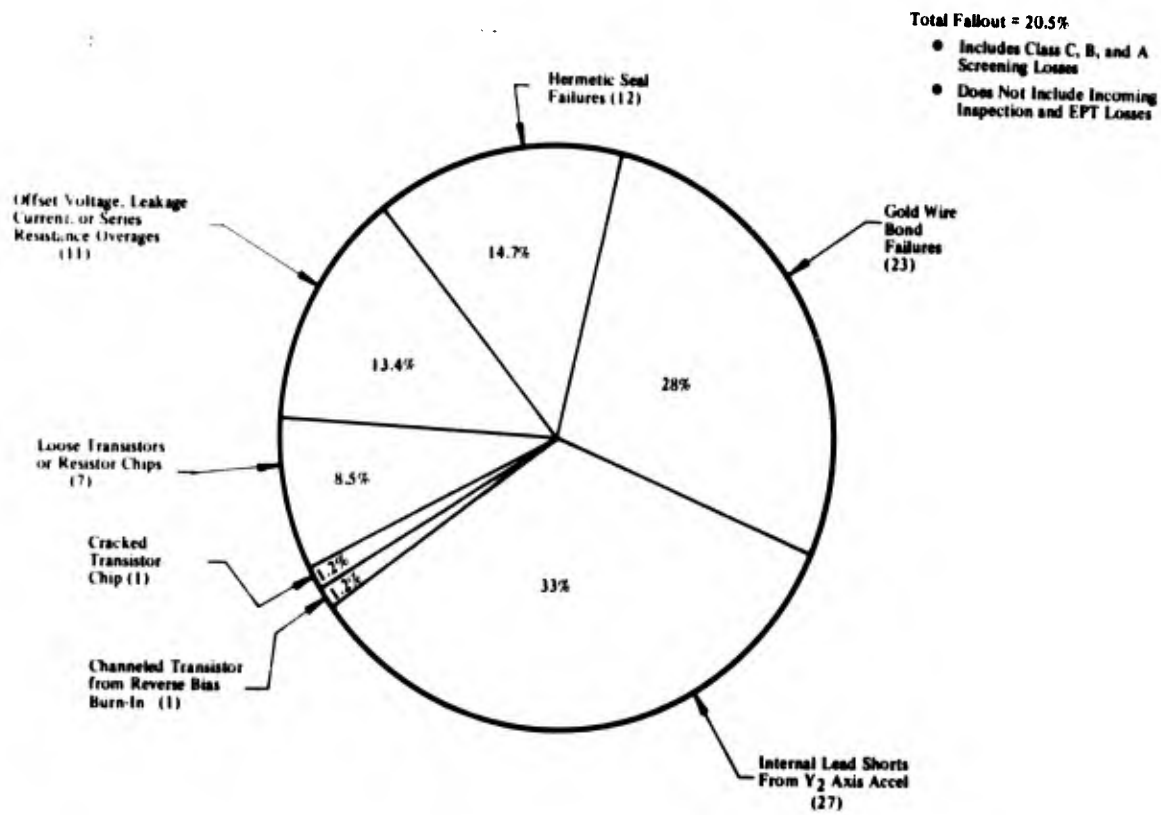
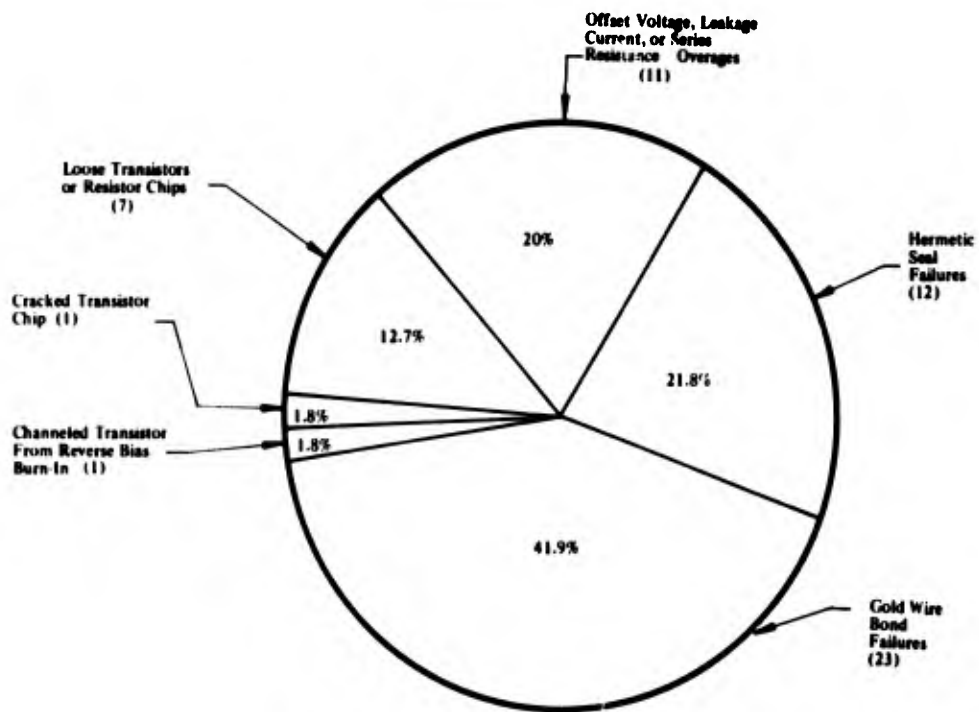


Figure 46. Distribution of Failure Mechanism for Test Group 7



(a) Distribution Including Affects of Y₂ Axis Acceleration



b. Distribution Not Including Affects of Y₂ Axis Acceleration

Figure 47. Distribution of Failure Mechanism for Test Group 6

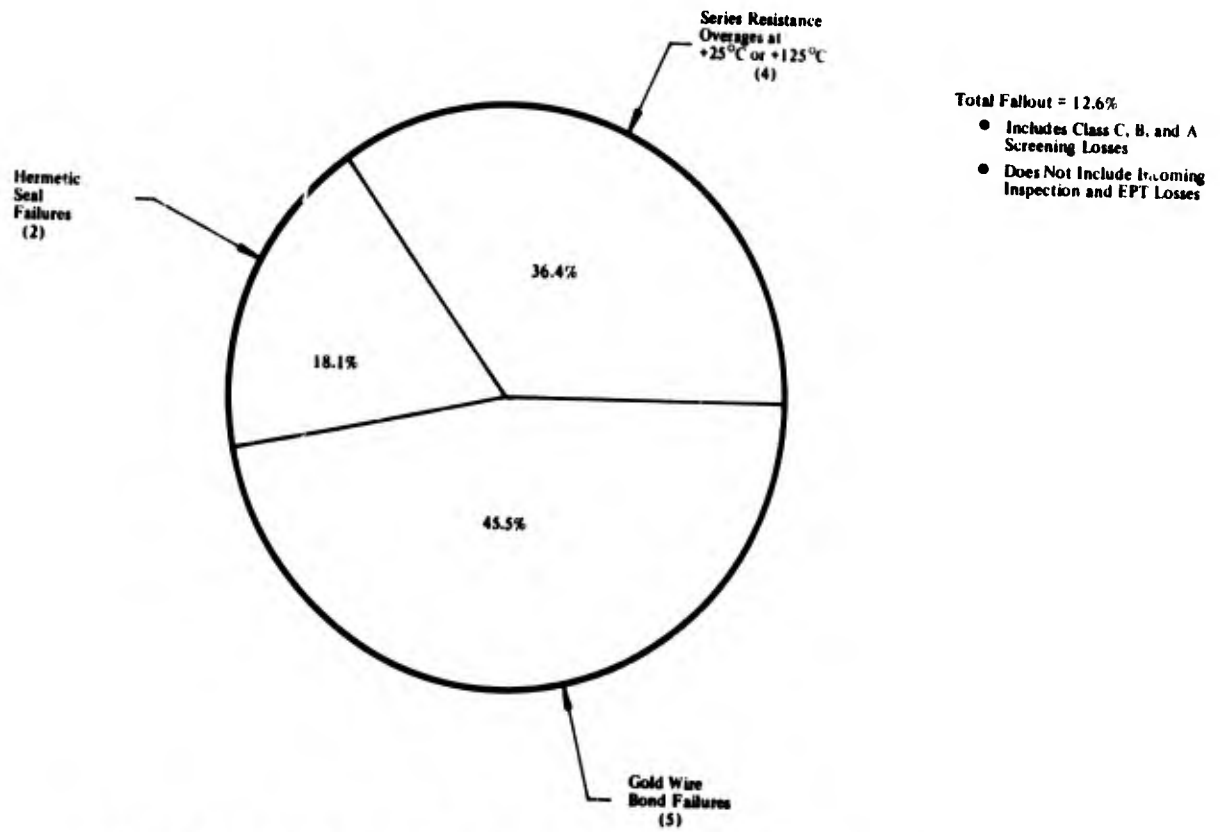


Figure 48. Distribution of Failure Mechanism for Test Group 8

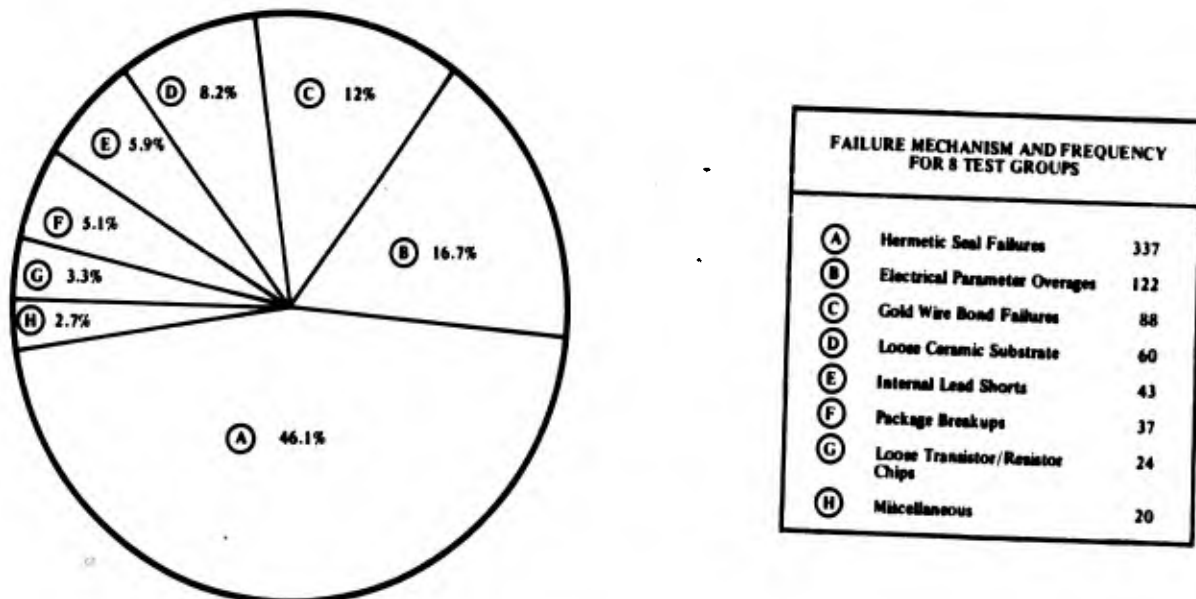


Figure 49. Overall Failure Mechanism Distribution (31.4% Average) for All Test Groups

Some perspective in these findings is provided by the results of testing packages of this same type, produced 6 months earlier by the same manufacturers, and evaluated by Delco in this contract's study phase. Results showed Manufacturer A's product to again be the more fragile, but both packages to be relatively immune to hermetic seal loss, even at high stress levels. Comparison of the packages, then and now, showed no apparent physical or mechanical differences. Both test programs were conducted by the same personnel.

Charts 46 through 48 show Manufacturer C to have wire bonding problems, primarily in his control of the thermocompression bonding cycle. Failure points were those where gold wires terminated at gold plated kovar, at thick-film gold conductors, and at thin-film aluminum. The principal failure points were the wedge bonds made at thin-film aluminum, specifically at the "wedge" shaped indentation created with the bonding tool. These occurrences cannot be eliminated with the aid of available screening techniques. Such bonds will degrade at ambients significantly above +25°C (but below +125°C), or where temperature changes are "seen" by the devices. In application, this situation represents great risk since internal wire bonding appears to be the predominant failure mechanism in both assembly and field losses. Appendix IV gives a detailed breakdown of the failure mechanisms for each test group for incoming inspection; Class C, Class B, and Class A screening; and for EPT Quality Conformance Inspection.

3.5 PRECAP INTERNAL-VISUAL INSPECTION

How precap internal-visual inspection requirements are specified is a critical aspect of obtaining reliable hybrid microcircuits. Specifying "precap internal-visual inspection per Condition A (or B) of Method 2010.1 of MIL-STD-883" is not sufficient to assure satisfactory internal materials, design, construction, and workmanship in a hybrid microcircuit because:

1. Each manufacturer tends to interpret the Method 2010 requirements in his own way,
2. Inspectors at a specific manufacturer differ among themselves on rejection criteria,
3. Many of the interpretations ignore the literal intent of MIL-STD-883, and become only goals to strive for rather than firm rejection criteria.

It has been Delco's experience that each manufacturer's interpretation of the specified precap internal-visual inspection rejection criteria had to be carefully reviewed. It was often found that although a manufacturer had excellent documentation of precap internal-visual requirements, they were not being enforced.

The purpose of the review of a manufacturer's inspection criteria must therefore be to assure that he is "literally" interpreting the requirements of Method 2010.1 of MIL-STD-883. Specific additions and exceptions must be specifically negotiated, depending on design and construction of a specific manufacturer's hybrids.

3.6 CONCLUSIONS ON SCREENING EFFECTIVENESS

Screening of hybrid microcircuits can be an effective aid to product assurance if properly administered. This study shows Method 5004 of MIL-STD-883 to be an excellent format for such screening, effecting average fallouts of 6.53 percent for Class C, 7.07 percent for Class B, and 31.4 percent for Class A. Related findings are as follows.

- **Y₁ Axis Acceleration** — A necessary procedure, best performed at the highest g level possible for each hybrid configuration, after all processing other than hermetic seal testing.
- **Y₂ Axis Acceleration** — Not recommended on a 100 percent screening basis. Some internal leads are forced close to chip edges and down to other conductors, causing potential shorts that are not necessarily corrected by Y₁ axis acceleration.
- **Reverse Bias Burn-In** — Important in screening and testing circuits that use discrete devices. The devices, however, will heal themselves before detection unless oven temperature is reduced to 25°C ambient before bias removal, and parts are electrically tested within 8 hours of bias removal.
- **Mechanical Shock vs Acceleration** — Not interchangeable as to results obtained. Acceleration exposes weak wire bonds, faulty substrate bonds, and bad chip bonds. Mechanical shock exposes additional potential failures due to improper assembly.
- **Wire Bonding** — A highly critical area of hybrid microcircuit production. Suppliers should perform stringent internal wire bond-pull tests hourly on each multichip hybrid bonder during the actual production process. Unless all of a sample's wires are pulled there is no assurance that all chips, metallizations, platings, and thick-films are bondable. Sample bond-pull tests should also be performed after hermetic sealing and all screen tests to detect any subsequent bond degradation. Good bonds do not degrade significantly.
- **Supplier Process Control** — Appears to place insufficient emphasis on obtaining consistently reliable wire bonds, chip bonds, and hermetic seals.
- **100 Percent Screening** — By itself, not completely effective in excluding faulty and marginal units. To assess the quality of each specific hybrid lot, a sample should be pulled for Quality Conformance Inspection.

- Hybrid Microcircuit Reliability — Variable by part and lot, even from the same source over brief periods. The diversity of hybrid part and material sources introduces many variables into the manufacturing cycle. The effect of these variables can be greatly minimized by exposing each hybrid to a systematic program of Method 5004 screening and subsequent sampling for Quality Conformance Inspection.
- Packaging — A chronic troublespot in hybrid microcircuit manufacturing, as evidenced by hermetic seal failures. Manufacturers should commit themselves to obtaining better packages and performing stringent incoming inspection tests of the hybrid packages before introducing them in assembly. Designers must also specify large enough packages to allow the use of reliable packages. This policy will assure the package's ability to withstand mechanical and environmental requirements, and survive through assembly into systems.
- Precap Internal-Visual Inspection — An effective screen if the rejection criteria of Method 2010.1, MIL-STD-883, is enforced. Rejection criteria must be reviewed with each manufacturer to assure a mutual understanding of what is, and is not, acceptable.

SECTION IV
CONCLUSIONS

4.1 GENERAL

In determining the electrical, mechanical, and environmental stress levels to be applied to a hybrid microcircuit, consideration must be given to the variables inherent in the production of each specific hybrid (described in Paragraph 2. 2) as well as to the hybrid's ultimate application. A general rule, applicable to all hybrid microcircuits, cannot be given because the maximum stress levels that each hybrid microcircuit can tolerate depend not only on the components used in that hybrid, but also on size and construction of the hybrid package. Thus, if a given hybrid must be highly reliable, and happens to be contained in a large package ($5/8'' \times 5/8''$ or larger), the prescription of correspondingly high applied stress levels may not assure the required level of quality assurance. Hybrids having components of large mass, and contained in large packages, may not be able to endure the required high stress levels. This situation would conflict with the intent of screens, which is to:

1. Apply stress levels high enough to accelerate failure mechanisms, and thereby fail unreliable devices during short term screen tests.
2. Confine the applied stresses to levels below those that would themselves fail a reliable device.

Parts which survive the desired screen are expected to operate without failure for a given time, at given conditions, for each application. However, if the levels required to trigger failure mechanisms in large hybrids cannot be tolerated by those units the elimination of failure mechanisms must necessarily revert back to process control in the manufacture of the hybrids. Screening to eliminate faulty hybrids is a valuable "brute force" technique which manufacturers should institute more often in the build cycle to assure consistency in producing reliable substrate, chip, and wire bonds.

The stepped stress test study showed that a properly constructed hybrid microcircuit can withstand very high stress levels without degradation. The data taken was representative of well constructed $1/4'' \times 1/8''$ and $1/4'' \times 3/8''$ hybrids. The data taken on the $1'' \times 1''$ hybrid, however, is indicative of problems that can occur with large packages which are difficult to hermetically seal and which have difficulty holding a seal, once obtained. Therefore, this study yielded no significant data to bear on high stress testing of larger hybrid microcircuits which are being designed into systems. Additional testing is required to establish the capabilities of such large hybrids for use in future systems.

The verification phase testing showed that screening of hybrid microcircuits can be an effective aid to product assurance if properly administered. By itself, 100 percent screening is not completely effective in excluding faulty and marginal units. To assess the effectiveness of the screening of each specific hybrid lot, a sample should be pulled for quality assurance inspection. Hybrid microcircuit reliability varies by part and lot, even from the same source over brief periods. The diversity of hybrid part and material sources introduces many variables into the manufacturing cycle. The effect of these variables can be greatly minimized by exposing each hybrid to a systematic program of screening and subsequent sampling for quality conformance inspection.

4.2 OPTIMUM SET OF QUALIFICATION PROCEDURES

The following procedures are recommended as a result of the study and verification phase of this contract. The hybrid microcircuits used as a basis for these recommendations were relatively simple and packaged in 1/4" x 1/8", 1/4" x 1/4", and 1/4" x 3/8" hermetically sealed flatpackages. Additional experience was obtained with a 1" x 1" flatpackage hybrid, but was of limited value because of the device's poor quality.

4.2.1 IN-PROCESS SCREENING

Table XVI is a list of screening procedures which are basically taken from Method 5004 of MIL-STD-883, but modified to incorporate information gathered during this contract. Screen Items 1 and 2, bond strength-interconnects and bond strength-chips, are very important tests for large-package hybrid microcircuits which cannot withstand extreme thermal shock and temperature cycles and high g level-mechanical shock and centrifuging. These in-process screens serve to detect weak bonds, which are primary failure mechanisms that are difficult to eliminate, by screening, during the manufacturing cycle. These two tests must be so performed as to monitor each and every bonding machine, each operator, each wire material and size, and each bond to the various chips used.

4.2.1.1 Bond Strength (Interconnects)

Bond strength testing is to be conducted, for the specified device class and LTPD, by using Conditions B, C, D, or F of Method 2011 of MIL-STD-883, as applicable to the particular device construction. The LTPD and acceptance numbers specified for the bond strength test determine the minimum sample size in terms of the minimum number of bond pulls to be accomplished, rather than the number of complete devices in the sample (except that the required number of bond pulls shall be contained in a minimum of 10 devices). All bonds pulled are to be counted and the specified sampling, acceptance, and added sample provisions observed, as applicable. Every bond in the

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Table XVI. Recommended Screen Test Procedures per MIL-STD-883

SCREEN TEST		CLASS "A"		CLASS "B"			
ITEM	TYPE	METHOD IN MIL-STD-883	REQUIREMENT	METHOD IN MIL-STD-883	REQUIREMENT	METHOD IN MIL-STD-883	
1	Bond Strength (Interconnects) Note (2)	2011 (See Paragraph 4.2.1.1)	Note (6)	2011 (See Paragraph 4.2.1.1)	Note (6)	-	
2	Bond Strength (Chips) Note (2)	(See Paragraph 4.2.1.2)	Note (6)	(See Paragraph 4.2.1.2)	Note (6)	-	
3	Internal Visual (Precap)	2010, Condition A	100%	2010, Condition B	100%	2010, Condition B	
4	Stabilization Bake	1008: 24 hrs (min), Condition C (min)	100%	1008: 24 hrs (min), Condition C (min)	100%	1008: 24 hrs (min) Condition C (min)	
5	Thermal Shock Note (7)	1011, Condition A (min)	100%	-	-	-	
6	Temperature Cycling Note (7)	1010, Condition C (min) (See Paragraph 4.2.1.3)	100%	1010, Condition C (min) (See Paragraph 4.2.1.3)	100%	1010, Condition C (min) (See Paragraph 4.2.1.3)	
7	Mechanical Shock	2002, Condition F: One Shock Pulse in Y ₁ Plane Only, or 5 Shock Pulses at Condition B in Y ₁ Plane	100%	-	-	-	
8	Interim Electrical Parameters	Note (6)	100%	Note (6)	-	-	
9	Burn-in Test	1015: 240 hrs at 125°C (min)	100%	168 hrs at 125°C (min) Note 4	100%	-	
10	Interim Electrical Parameters	Note (6)	100%	-	-	-	
11	Reverse Bias Burn-in (See Paragraph 4.2.1.4)	1015, Condition A or C, when Specified, 72 hrs at 150°C (min)	100%	-	-	-	
12	Interim Electrical Parameters Note (5)	Note (6)	100%	-	-	-	
13	Centrifuge	2001: Y ₁ Plane 40,000 g (min)	100%	2001, Condition E, Y ₁ Plane (min)	100%	2001, Condition E (min) Y ₁ Plane only	
14	Hermeticity a. Fine Note (1) b. Gross	1014	100%	1014	100%	1014	
15	Final Electrical Test (See Paragraph 4.2.1.5.2)	Static Tests: • 25°C	Note (6)	100%	Note (6)	100%	Note (6)
		• Maximum and Minimum Rated Operating Temperature		100%		100%	
		Dynamic Tests at 25°C		100%		100%	
		Functional Test at 25°C (See Paragraph 4.2.1.5.3)		100%		100%	
16	Radiographic	2012	100%	-	-	-	
17	Qualification or Quality Conformance Inspection	(See Paragraph 4.2.2)	Note (6)	(See Paragraph 4.2.2)	Note (6)	(See Paragraph 4.2.2)	
18	External Visual Note (3)	2009	100%	2009	100%	2009	

NOTES:

- (1) The radiographic (Item 16) and hermeticity (Item 14) screens may be performed in any sequence after Item 13.
- (2) All devices must be bond strength tested, the extent of which shall be a function of g level used during the centrifuge screen. (See Item 13.) Where package size restricts the g level to 40,000 or below, a tight sampling plan is recommended. Where a device is centrifuged below 20,000 g the Class A devices should be 100 percent bond strength tested, using nondestructive methods.
- (3) Unless otherwise specified, the external visual inspection need not include measurement of physical dimensions.
- (4) Burn-in conditions should be established through testing to determine the most effective such screen for each type of device. (This is necessary since some devices are best screened with reverse-bias burn-in, some are best burned-in at full-load operation, etc.)

- (5) This electrical test can be performed while the device is in operation.
- (6) Per applicable procedure.
- (7) CAUTION: In cases where load is required to be applied during the test, the load should be applied before the test is initiated.

A

Table XVIII. Recommended Group A Quality Conformance Test Procedures

ITEM	TEST TYPE	CONDITIONS	CLASS A LTPD	CLASS B LTPD	CLASS C LTPD
1	Electrical Tests at 25°C <ul style="list-style-type: none"> • Static • Dynamic • Functional 	Per Applicable Procurement Document	5 Max. Acceptance No. 5	7 Max. Acceptance No. 5	10 Max. Acceptance No. 18
2	Electrical Tests at Maximum and Minimum Rated Operating Temperature: <ul style="list-style-type: none"> • Static • Dynamic • Functional 	Per Applicable Procurement Document	5 Max. Acceptance No. 10	10 Max. Acceptance No. 18	15 Max. Acceptance No. 18

Table XIX. Recommended Group B Quality Conformance Test Procedures

ITEM	TEST	METHODS OF MIL-STD-883	CONDITIONS	CLASS A LTPD	CLASS B LTPD	CLASS C LTPD
1	Physical Dimensions	2008	Test Condition A	7 (See Para. 4.2.2.1)	10 (See Para. 4.2.2.2)	15 (See Para. 4.2.2.3)
2	Marking Permanency	2008	Test Condition B (Para. 3.2.1)			
3	Visual and Mechanical	2008	Test Condition B			
4	Temperature Cycling	1010	Test Condition C			
5	Burn-In	1015				
6	Acceleration	2001	Y ₁ Plane, 40,000 g (min.)			
7	Lead Fatigue	2004	Test Condition B ₂			
8	Electrical: <ul style="list-style-type: none"> • Static • Dynamic • Functional 					
9	Hermetic Seal: <ul style="list-style-type: none"> • Fine • Gross 	1014	Test Condition A or B Test Condition C, Step 2			
10	Internal Visual	2010	Condition A for Class A Condition B for Class B and C	(See Para. 4.2.2.1)	(See Para. 4.2.2.2)	(See Para. 4.2.2.3)
11	Bond Strength: <ul style="list-style-type: none"> • Interconnects • Chips 	2011	(See Para. 4.2.1.1.) (See Para. 4.2.1.2.)			

Item 12 after reverse bias burn-in may be eliminated if the 25°C final electrical tests (Item 15) are performed 24 hours after removal of the reverse bias (Item 11).

See procurement document.

When a large group of parts is placed in thermal shock or temperature cycling, the large thermal gradients can invalidate the test unless the equipment used has sufficient capacity to maintain the temperature extremes.

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microcircuit must be pulled. Any bond pulled which fails under an applied stress less than that indicated in Table XVII constitutes a failure. (See MIL-STD-883, Method 5005, Paragraph 3.7.)

Table XVII. Required Bond Strength for Indicated Test Conditions and Wire Type

TEST CONDITION	WIRE TYPE		REQUIRED MIN. BOND STRENGTH (grams)
	COMPOSITION	CONSTRUCTION	
B	Au or Al	Wire or Beam Lead (1-mil wire)	15
C	Al	Beam Lead	2
C	Au	Beam Lead	6
C or D	Al	Wire (1 mil)	1
C or D	Au	Wire (1 mil)	3
F	Any	Flip-Chip	5 × No. of Bonds
F	Any	Beam Lead	5 × No. of Beams

4.2.1.2 Bond Strength (Chips)

The sample used here may be the same as that used for the interconnect bond strength tests. This test is not applicable to flip-chips or beam leads; use Paragraph 4.2.1.1 for these. Chip bond strength testing must be conducted for the specified device class and LTPD of the procurement document. The chip bond test is performed as follows:

- The inspector, using a small wire or stick (toothpick), pokes the semiconductor, capacitor, and resistor chips to determine if they are securely bonded.
- Semiconductor chip bond is secure if the chip does not pop off from pushing.

A good semiconductor chip bond would result in the silicon fracturing, leaving the silicon-to-substrate bond intact.

For capacitor and resistor chips, the evaluation becomes more difficult. The definition of a failure of capacitor and resistor chip bonds must be negotiated to be some number of grams shear. This test is very similar to Condition F (bond shear for flip-chips) of Method 2011 of MIL-STD-883.

4. 2. 1. 3 Temperature Cycling

Item 6 in Table XVI, temperature cycling for Class B and C devices, may be replaced by thermal shock, Method 1011 of MIL-STD- 883, Condition B (minimum) in accordance with Item 5.

4. 2. 1. 4 Reverse Bias Burn-In

The requirement for cooldown under bias is recommended, and the parts must be tested within 8 hours after removal of bias. The reverse bias burn-in of Item 11 is required only when specified in the applicable procurement document, and is recommended only for discrete diodes; transistors and capacitors; and certain MOS, linear, or other elements in the hybrid microcircuits where surface sensitivity may be of concern.

4. 2. 1. 5 Electrical Measurements

4. 2. 1. 5. 1 Interim Electrical Parameters

Electrical testing must be performed as indicated in Items 8 and 10 , to remove defective devices prior to further testing, or to provide a basis for application of percent defective allowable (PDA) criteria when a PDA is specified. This test need not include all specified device parameters, but must include those measurements that are most sensitive to, and effective in, removing electrically defective devices. When delta limit measurements are required, they must be specified in the applicable procurement document and included as interim electrical measurements. When delta limit measurements are specified, the procedures for device traceability must be specified in the applicable procurement document.

4. 2. 1. 5. 2 Final Electrical Measurements

Final electrical testing of microcircuits assures that the microcircuits tested meet the electrical requirements of the applicable procurement document. It must include, as a minimum, tests of all parameters and limits and conditions of test which are specifically identified in the detail specification or drawing as final electrical test requirements.

4. 2. 1. 5. 3 Functional Test(s)

Functional test(s) must be performed as specified in the applicable procurement document; and, when applicable, must consist of measurement of the relationship between inputs and outputs contained in the truth table(s). Measurements and sequence of test must be specified in the applicable procurement document.

4. 2. 1. 5. 4 Data Reporting

Data must be reported as required by the applicable procurement.

4. 2. 1. 5. 5 Failure Analysis.

When required by the applicable procurement document, failure analysis of devices rejected during any test in the screening sequence must be accomplished in accordance with Method 5003 of MIL-STD-883. Requirements for such analysis should, in general, be limited to sufficient examination of devices to establish primary modes or mechanisms of failure, and provide corrective action information.

4. 2. 1. 5. 6 Defective Devices

All devices which fail to comply with the requirements of any screen, or of the applicable procurement document, must be removed from the lot. Once rejected and verified as a device failure, such devices must not be retested for acceptance.

4. 2. 2 LOT QUALIFICATION

The qualification, or quality conformance inspection, tests specified in MIL-STD-883, Method 5005, are normally performed by the microcircuit manufacturer. Delco Electronics prefers to perform these lot qualification tests in-house to assure better control of the lots. Delco negotiates the lot rejection criteria with the manufacturer and, when there is an unscreenable failure, the lot is returned to the supplier for scrapping. It is therefore recommended that the lot qualification be directed "to be performed by the user where the manufacturer obligates himself to accept return of the lots that fail."

Tables XVIII and XIX show recommended Group A and B tests for lot qualification. The recommended Group C tests are those stated in Method 5005 of MIL-STD-883.

The qualification and quality conformance inspection procedures shown are intended to assure that the device and lot quality conforms with the requirements of the applicable procurement document. The full requirements of Group A, B, and C tests and inspections are intended for use in initial device qualification, requalification in the event of product or process change, and periodic testing for retention of qualification. Group A and B tests and inspections are intended for quality conformance inspection of individual inspection lots as a condition for acceptance for delivery. In general, it is intended that the device class to which qualification or quality conformance inspection is conducted be the same device class to which screening procedures are conducted.

The Group A tests in Table XVIII are divided into two subgroups. Item 1 includes all the electrical tests at 25°C, and Item 2 includes all the electrical tests at the maximum and minimum rated operating temperatures. The static, dynamic, and functional tests are tests that can be programmed on an automatic microcircuit tester. If the lot fails the Group A LTPD test level for the respective class, the lot must be 100 percent screened to eliminate the faulty devices.

The Group B test sequence in Table XIX, which is quite different from that in Method 5005 of MIL-STD-883, has proven to be very effective in testing parts at Delco Electronics. The Group B test order should be precisely as shown in the table. The parts and initial electrical data for Group B should come from the Group A parts.

4. 2. 2. 1 Class A Lot Qualification Inspection Levels for Group B Tests

The sample size and inspection levels for the Group B tests for Class A parts should be as follows:

- For Items 1 through 9 in the table, the sample inspection should be to an LTPD of 7, with a maximum acceptance number of zero for lots of greater than 200 parts. For lots of 200 parts or less, the sample size should be at least 12 percent of the lot, with a minimum sample size of 12.
- For Items 10 and 11, the sample size should be one-half of the sample from Items 1 through 9, with one allowable failure. For example, one bond failure would allow acceptance of the lot; two bond failures would be cause for rejection; or one bond failure and one visual failure would constitute a reject.

4. 2. 2. 2 Class B Lot Qualification Inspection Levels for Group B Tests

The sample size and inspection levels for the Group B tests for Class B parts should be as follows:

- For Items 1 through 9 in the table, the sample inspection should be to an LTPD of 10, with a maximum acceptance of zero for lots of greater than 200 parts. For lots of 200 parts or less, the sample size should be at least 10 percent of the lot, with a minimum sample size of 10.
- For Items 10 and 11, the sample size should be one-half of the sample from Items 1 through 9, with one allowable failure.

4. 2. 2. 3 Class C Lot Qualification Inspection Levels for Group B Tests

The sample size and inspection levels for the Group B tests for Class C parts should be as follows:

- For Items 1 through 9 in the table, the sample inspection should be to an LTPD of 15, with a maximum acceptance number of zero for lots of greater than 200 parts. For lots of 200 parts or less, the sample size should be at least 7 percent of the lot, with a minimum sample size of 7.
- For Items 10 and 11, the sample size should be one-half of the sample from Items 1 through 9, with one allowable failure.

4.2.2.4 Disposition of Lots

Lots which pass the Group A and B tests should be considered suitable for use at the respective class parts or below. Lots which fail the Group A tests may be screened to eliminate the out-of-specification units. Lots which fail the Group B inspection should be rejected. The failures in Group P inspection should be failure analyzed to define the failure mechanism, and action should be taken to correct the problem.

On lots which pass the lot acceptance criteria of Groups A and B, the unopened samples which meet all the procurement documents could be used for production.

4.3 SOURCE INSPECTION

Delco Electronics-Milwaukee Operations dispatched engineers, experienced in microcircuits, out in the field to serve as source inspectors at the microcircuit manufacturers' facilities early in 1970. The resultant experience proved to be a great aid in obtaining the level of quality and reliability required in Delco hybrids. During this source inspection, the experienced engineers monitored the manufacturer during his processing of Delco parts, and provided the foundation of a negotiated agreement to perform precap internal visual inspection on all products to assure that they would meet the proper criteria (which was basically the precap internal visual inspection requirements of MIL-STD-883, Method 2010.1). These personnel also made available a Delco representative to assure that the specification requirements were read and correctly interpreted, and that the product was furnished in accordance with the proper requirements. Due to the relatively high turnover rate of personnel in the semiconductor industry, these resident source inspectors also provided continuity in the supplier's attention to Delco requirements, thereby creating another possible avenue for maintaining qualification of a supplier on high reliability programs.

4.4 COST FACTORS FOR SCREENING AND LOT QUALIFICATION

The costs attributable to screening and lot qualification of hybrid microcircuits are complex, interrelated, and hence difficult to establish. Prices vary substantially with business trends, competition, potential and present volume, attitude of hybrid salesmen, attitude of hybrid manufacturers, fallout of hybrids during screening, cost of hybrids, actual test costs, and other subtleties. For example, if a manufacturer's test facilities were not being fully utilized, his screening costs would be lower since it would be unnecessary to procure additional screening facilities. Similarly, if a manufacturer knew that he was the sole source of supply for a particular hybrid, his screening costs should be expected to be high.

Screening and lot acceptance costs would be high if a manufacturer knew that the user would be performing incoming inspection tests to monitor the effectiveness of the manufacturer's testing. The screening and lot acceptance costs would also be high if the manufacturer has poor process control, which would ultimately result in higher fallout in screens.

Therefore, any breakdown of screening and lot qualification costs would have little meaning or application, especially for hybrid microcircuits which vary in complexity from very simple types to very complex circuits embodying materials from many sources. Of more meaningful value would be an indication of the time it takes to test hybrid microcircuits, as reflected in the experience of Delco Electronics.

4.4.1 COST DEFINITION

It is important to realize that the costs of screening and lot qualification described herein are not necessarily costs "in addition to overall costs" of the system using hybrids. Properly controlled screening and lot qualification ultimately result in lower system costs due:

1. Decreased time in troubleshooting assemblies and replacing defective parts to get the system operating after the hybrids are installed.
2. Fewer callbacks and returns for warranty repairs.

In a program having reliability requirements (which must be achieved or the system must be repaired without charge), the use of screening and lot qualification is necessary to hold down overall system costs. Therefore, the indicated costs for screening and lot qualification should be regarded as "investment costs" which will ultimately be recouped as fewer faulty hybrids get into assemblies.

4.4.2 COST VS. LOT SIZE

Tables XX and XXI are compilations of cost factors for Screen Tests and Lot Acceptance Tests, respectively. The "cost factors" are estimates of equipment use time and the time it takes to perform the respective test. After the hybrid has been hermetically sealed, the estimates are based on performance of all the screens (other than fine and gross hermetic seal testing) with the hybrid in a carrier, which protects the leads from damage and promotes ease in handling. The estimates in Table XX were based on the screens proposed in Paragraph 4.2.1.

As expected, the unit costs of screening and lot qualification are considerably less when devices are processed in volume. The costs of screening up to 50 parts are little different than for 100 parts; whereas, the screening of thousands of parts requires equipment to handle the parts more efficiently but ultimately results in decreasing cost per part.

Highest costs in lot qualification are incurred on lots of less than 200 pieces; whereas, for lots greater than 200 pieces, increasing the lot size has no added effect on lot qualification cost (provided that the lots pass the tests). It is advantageous to strive for maximum inspection lot sizes, as defined in MIL-M-38510, to reduce the overall number of lots to be qualified. No attempt is made to incorporate added costs due to fallout in the tables. It is assumed that facilities are in existence and available to perform the lot qualification tests. As indicated in Table XXI, the lot qualification cost elements for all reliability classes are the parts which are tested and not used in production (destructive tests), the facilities used, and the man-hours expended in performing the qualification tests.

4.5 VENDOR QUALIFICATION

Procedures for establishing hybrid microcircuit vendor qualification, including specific requirements for test and analysis facilities, product traceability, error determination, and failure mode data accumulation, are the same as those for monolithic integrated circuit vendors, except that the emphasis must now be on the additional materials comprising the more complex hybrid microcircuit. That the hybrid is more complex makes it all the more important that the user assure himself that the manufacturer has a good quality control program. It is also important that the manufacturer have a well documented and controlled fabrication process.

Table XX (Sheet 1 of 3). Screen Test Cost Factors for 3 Class Levels of Part Reliability

TEST DESCRIPTION		REL CLASS LEVELS	COST ELEMENTS - BY LOT SIZE																		
			ESTIMATED HOURS TEST FACILITIES ARE IN USE					ESTIMATED MAN-HOURS REQUIRED TO PERFORM TESTS													
ITEM	TYPE		12	100	200	1000	2000	5000	12	100	200	1000	2000	5000	12	100	200	1000	2000	5000	
1	Bond Strength (Interconnects)*	C	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	
		B	0.2	0.3	0.8	0.8	0.8	0.8	0.8	0.2	0.3	0.8	0.8	0.8	0.8	0.3	0.8	0.8	0.8	0.8	0.8
		A	0.2	0.3	0.8	0.8	0.8	0.8	0.8	0.2	0.3	0.8	0.8	0.8	0.8	0.3	0.8	0.8	0.8	0.8	0.8
2	Bond Strength (Chips) *	C	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	
		B	0.2	0.2	0.3	0.3	0.3	0.3	0.3	0.2	0.3	0.3	0.3	0.3	0.3	0.2	0.3	0.3	0.3	0.3	0.3
		A	0.2	0.2	0.3	0.3	0.3	0.3	0.3	0.2	0.3	0.3	0.3	0.3	0.3	0.2	0.3	0.3	0.3	0.3	0.3
3	Internal Visual (Precap)	C	0.3	1.5	2.7	12.7	25.1	62.7	0.3	1.5	2.7	12.7	25.1	62.7	0.3	1.5	2.7	12.7	25.1	62.7	
		B	0.3	1.5	2.7	12.7	25.1	62.7	0.3	1.5	2.7	12.7	25.1	62.7	0.3	1.5	2.7	12.7	25.1	62.7	
		A	0.3	1.5	2.7	12.7	25.1	62.7	0.3	1.5	2.7	12.7	25.1	62.7	0.3	1.5	2.7	12.7	25.1	62.7	
4	Stabilization Bake	C	24.3	24.3	24.3	24.5	24.5	24.5	0.3	24.3	24.3	24.3	24.5	24.5	0.3	24.3	24.3	24.3	24.5	24.5	
		B	24.3	24.3	24.3	24.5	24.5	24.5	0.3	24.3	24.3	24.3	24.5	24.5	0.3	24.3	24.3	24.3	24.5	24.5	
		A	24.3	24.3	24.3	24.5	24.5	24.5	0.3	24.3	24.3	24.3	24.5	24.5	0.3	24.3	24.3	24.3	24.5	24.5	
5	Thermal Shock	C	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	
		B	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
		A	2.8	2.8	2.9	3.0	6.0	15.0	0.3	2.8	2.8	2.9	3.0	6.0	15.0	0.3	2.8	2.8	2.9	3.0	6.0
6	Temperature Cycling	C	3.8	3.8	3.8	3.8	3.8	3.8	0.3	3.8	3.8	3.8	3.8	3.8	0.3	3.8	3.8	3.8	3.8	3.8	
		B	3.8	3.8	3.8	3.8	3.8	3.8	0.3	3.8	3.8	3.8	3.8	3.8	0.3	3.8	3.8	3.8	3.8	3.8	
		A	3.8	3.8	3.8	3.8	3.8	3.8	0.3	3.8	3.8	3.8	3.8	3.8	0.3	3.8	3.8	3.8	3.8	3.8	
7	Mechanical Shock	C	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	
		B	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
		A	0.3	0.5	0.8	3.0	5.7	14.0	0.3	0.3	0.5	0.8	3.0	5.7	14.0	0.3	0.5	0.8	3.0	5.7	14.0

* Assuming samples sizes of 2, 5, 22, 22, 22, and 22, respectively.

Table XX (Sheet 2 of 3). Screen Test Cost Factors for 3 Class Levels of Part Reliability

TEST DESCRIPTION		REL CLASS LEVELS	COST ELEMENTS - BY LOT SIZE															
			ESTIMATED HOURS TEST FACILITIES ARE IN USE								ESTIMATED MAN-HOURS REQUIRED TO PERFORM TESTS							
			ITEM	TYPE	12	100	200	1000	200	5000	12	100	200	1000	2000	5000		
8	Interim Electrical	C	-	-	-	-	-	-	-	-	-	-	-	-	-			
		B	0.5	0.6	0.7	1.6	2.8	7.0	0.5	0.6	0.7	1.6	2.8	7.0				
		A	0.5	0.6	0.7	1.6	2.8	7.0	0.5	0.6	0.7	1.6	2.8	7.0				
9	Burn-in	C	-	-	-	-	-	-	-	-	-	-	-	-				
		B	241.0	241.0	241.0	243.3	246.7	256.7	0.3	0.3	0.7	3.3	6.7	16.7				
		A	241.0	241.0	241.0	243.3	246.7	256.7	0.3	0.3	0.7	3.3	6.7	16.7				
10	Interim Electrical	C	-	-	-	-	-	-	-	-	-	-	-	-				
		B	0.5	0.6	0.7	1.6	2.8	7.0	0.5	0.6	0.7	1.6	2.8	7.0				
		A	0.5	0.6	0.7	1.6	2.8	7.0	0.5	0.6	0.7	1.6	2.8	7.0				
11	Reverse-Bias Burn-in	C	-	-	-	-	-	-	-	-	-	-	-	-				
		B	-	-	-	-	-	-	-	-	-	-	-	-				
		A	73.0	73.0	73.0	75.3	78.7	88.7	0.3	0.3	0.7	3.3	6.7	16.7				
12	Interim Electrical	C	-	-	-	-	-	-	-	-	-	-	-	-				
		B	-	-	-	-	-	-	-	-	-	-	-	-				
		A	**	**	**	1.6	2.8	7.0	**	**	**	1.6	2.8	7.0				
13	Centrifuge	C	0.3	0.4	0.8	4.0	8.0	19.5	0.3	0.4	0.8	4.0	8.0	19.5				
		B	0.3	0.4	0.8	4.0	8.0	19.5	0.3	0.4	0.8	4.0	8.0	19.5				
		A	0.3	0.4	0.8	4.0	8.0	19.5	0.3	0.4	0.8	4.0	8.0	19.5				
14	Hermeticity, Fine	C	4.2	4.3	4.6	6.8	9.6	21.9	0.2	0.3	0.6	2.8	5.6	13.9				
		B	4.2	4.3	4.6	6.8	9.6	21.9	0.2	0.3	0.6	2.8	5.6	13.9				
		A	4.2	4.3	4.6	6.8	9.6	21.9	0.2	0.3	0.6	2.8	5.6	13.9				
	Hermeticity, Gross	C	4.2	4.3	4.5	6.3	8.5	19.2	0.2	0.3	0.5	2.3	4.5	11.2				
		B	4.2	4.3	4.5	6.3	8.5	19.2	0.2	0.3	0.5	2.3	4.5	11.2				
		A	4.2	4.3	4.5	6.3	8.5	19.2	0.2	0.3	0.5	2.3	4.5	11.2				

** Final electrical tests (Item 15) will be performed within 8 hours after removal of bias (in Item 11); therefore, this test not necessary.

Table XX (Sheet 3 of 3). Screen Test Cost Factors for 3 Class Levels of Part Reliability

TEST DESCRIPTION		REL CLASS LEVELS	COST ELEMENTS - BY LOT SIZE											
			ESTIMATED HOURS TEST FACILITIES ARE IN USE						ESTIMATED MAN-HOURS REQUIRED TO PERFORM TESTS					
ITEM	TYPE		12	100	200	1000	2000	5000	12	100	200	1000	2000	5000
15	Electrical, 25° C	C	0.5	0.6	0.7	1.6	2.8	7.0	0.5	0.6	0.7	1.6	2.8	7.0
		B	0.5	0.6	0.7	1.6	2.8	7.0	0.5	0.6	0.7	1.6	2.8	7.0
		A	0.5	0.6	0.7	1.6	2.8	7.0	0.5	0.6	0.7	1.6	2.8	7.0
15	Electrical, High Temp	C	-	-	-	-	-	-	-	-	-	-	-	-
		B	0.5	0.6	0.7	1.6	2.8	7.0	0.5	0.6	0.7	1.6	2.8	7.0
		A	0.5	0.6	0.7	1.6	2.8	7.0	0.5	0.6	0.7	1.6	2.8	7.0
15	Electrical, Low Temp	C	-	-	-	-	-	-	-	-	-	-	-	-
		B	0.5	0.6	0.7	1.6	2.8	7.0	0.5	0.6	0.7	1.6	2.8	7.0
		A	0.5	0.6	0.7	1.6	2.8	7.0	0.5	0.6	0.7	1.6	2.8	7.0
16	Radiographic	C	-	-	-	-	-	-	-	-	-	-	-	-
		B	-	-	-	-	-	-	-	-	-	-	-	-
		A	0.3	0.3	0.6	3.0	5.6	14.0	0.3	0.3	0.6	3.0	5.6	14.0
17	Lot Qualification (See Para 4.4.2)	C	182.5	182.5	184.3	184.3	184.3	184.3	4.5	4.5	6.0	6.0	6.0	6.0
		B	182.6	182.6	184.5	184.5	184.5	184.5	4.7	4.7	6.3	6.3	6.3	6.3
		A	182.9	183.2	185.6	185.6	185.6	185.6	5.0	5.3	7.4	7.4	7.4	7.4
18	External Visual	C	0.2	0.2	0.3	0.3	0.6	1.4	0.2	0.2	0.3	0.3	0.6	1.4
		B	0.2	0.2	0.3	0.3	0.6	1.4	0.2	0.2	0.3	0.3	0.6	1.4
		A	0.2	0.2	0.3	0.3	0.6	1.4	0.2	0.2	0.3	0.3	0.6	1.4
19	Serialization and Controls by S/N	C	-	-	-	-	-	-	-	-	-	-	-	-
		B	-	-	-	-	-	-	-	-	-	-	-	-
		A	0.2	2.0	4.0	10.0	20.0	50.0	0.2	2.0	4.0	10.0	20.0	50.0
Total Man-Hours	C	-	-	-	-	-	-	-	6.8	8.4	12.2	30.7	53.6	123.2
	B	-	-	-	-	-	-	-	9.7	11.8	17.1	41.8	72.9	169.3
	A	-	-	-	-	-	-	-	12.1	15.8	24.6	64.3	115.6	273.3
Man-Hours Per Part	C	-	-	-	-	-	-	-	0.567	0.084	0.061	0.031	0.027	0.025
	B	-	-	-	-	-	-	-	0.808	0.118	0.086	0.042	0.036	0.034
	A	-	-	-	-	-	-	-	1.008	0.158	0.123	0.064	0.058	0.055

Table XXI. Lot Acceptance Test Cost Factors for 3 Class Levels of Part Reliability

TEST DESCRIPTION		TYPE OF SAMPLING		RELIABILITY CLASS LEVEL TESTED FOR	COST ELEMENTS		
GROUP	TYPE	LOT SIZE	SAMPLE SIZE		PARTS NOT USABLE IN PRODUCTION	HOURS TEST EQUIP IS IN USE	MAN-HOURS REQUIRED TO PERFORM TESTS
Group A Electrical Testing	+ 25°C Tests	12	12	C	—	0.5	0.5
			12	B	—	0.5	0.5
			12	A	—	0.5	0.5
		50	16	C	—	0.5	0.5
			25	B	—	0.5	0.5
			32	A	—	0.5	0.5
		100	20	C	—	0.5	0.5
			32	B	—	0.5	0.5
			40	A	—	0.6	0.6
		200 or more	22 (Note ②)	C	—	0.5	0.5
			32 (Note ③)	B	—	0.5	0.5
			45 (Note ④)	A	—	0.6	0.6
	At Max and Min Operating Temp	12	8	C	—	1.0	1.0
			12	B	—	1.0	1.0
			12	A	—	1.0	1.0
		50	12	C	—	1.0	1.0
16			B	—	1.0	1.0	
32			A	—	1.0	1.0	
100		15	C	—	1.0	1.0	
		20	B	—	1.0	1.0	
	40	A	—	1.2	1.2		
200 or more	15 (Note ①)	C	—	1.0	1.0		
	22 (Note ②)	B	—	1.0	1.0		
	45 (Note ④)	A	—	1.2	1.2		
Group B Environmental, Mechanical, and Electrical Testing	12	7	C	4	181.0	3.0	
		10	B	5	181.1	3.2	
		12	A	6	181.4	3.5	
	50	7	C	4	181.0	3.0	
		10	B	5	181.1	3.2	
		12	A	6	181.4	3.5	
	100	7	C	4	181.0	3.0	
		10	B	5	181.1	3.2	
		12	A	6	181.4	3.5	
	200 or more	15 (Note ①)	C	8	182.8	4.5	
		22 (Note ②)	B	11	183.0	4.8	
		32 (Note ③)	A	16	183.8	5.6	
Total Cost Factors for Lot Qualification	12	7	C	4	182.5	4.5	
		10	P	5	182.6	4.7	
		12	A	6	182.9	5.0	
	50	7	C	4	182.5	4.5	
		10	B	5	182.6	4.7	
		12	A	6	182.9	5.0	
	100	7	C	4	182.5	4.5	
		10	B	5	182.6	4.7	
		12	A	6	183.2	5.3	
	200 or more	15	C	8	184.3	6.0	
		22	B	11	184.5	6.3	
		32	A	16	185.6	7.4	

NOTES:

- ① Corresponds to LTPD of 15, max acceptance number of 0
- ② Corresponds to LTPD of 10, max acceptance number of 0
- ③ Corresponds to LTPD of 7, max acceptance number of 0
- ④ Corresponds to LTPD of 5, max acceptance number of 0

The ultimate criteria of a vendor's qualification is his ability to meet the Groups A, B, and C testing, as described in the optimum procedures section (Paragraph 4. 2) for hybrid microcircuits. We recommend, as a specific document, the material reported in the Final Report, "Qualification Procedures for Integrated Devices" Volume II (Technical Report No. RADC-TR-68-315, January 1969), the section entitled "Vendor Qualification Requirements for Suppliers of Monolithic Microcircuits" prepared by Philco-Ford Corporation for Rome Air Development Center under Contract AF 30 (602) - 4282. These procedures are applicable to hybrid microcircuit manufacturers.

4. 6 PRODUCT QUALIFICATION

Detailed procedures for establishing product qualification, including specific method of test sample selection, sequence of tests, sample size, criteria for dequalification, methods for resubmission and requalifications are found in MIL-M-38510, "Military Specification - General Specification for Microcircuits" dated 20 November 1969. MIL-M-38510 is recommended for use with hybrid microcircuits, with the following changes: Where MIL-M-38510 refers to Methods 5004 and 5005 of MIL-STD-883, it is recommended that the optimum qualification procedures in Paragraph 4. 2 of this report be substituted. With reference to Paragraph 3. 1. 3. d in MIL-M-38510, defining electrically and structurally similar microcircuits, hybrids occur in so many different forms that few are classifiable as electrically and structurally similar. They have different layouts, sizes of components mounted on the substrates, sources for materials used in the hybrids, and equipment used in assembling. Since it is generally the case that hybrid microcircuits are, and will be, electrically and structurally dissimilar, as a general rule, different hybrid microcircuits cannot be qualified by similarity.

Product qualification of limited usage hybrids (less than 200 devices) becomes very costly and cannot be performed using statistically valid sample sizes to assure a certain level of quality. The minimum sample sizes that must be used for product qualification are those outlined in Section 4. 2. 2 for Group A and B testing. Using this guideline, the Group A testing will often be performed on 100 percent of the samples, using the LTPD's called out and the hypergeometric sampling plans for small lot sizes (described in Appendix B of MIL-M-38510). The recommended Group B sample size is as outlined in Paragraph 4. 2. 2. The recommended Group C sample size is the same as those for the first nine tests in Group B. Additional cost savings may be achieved by combining subgroups 1, 2, and 3, and subgroups 5 and 6 in Group C to restrict the sample size. The Group C rejection criteria should be the same as outlined in Paragraph 4. 2. 2 for the Group B tests.

APPENDIX I

HYBRID MICROCIRCUIT PROCUREMENT DOCUMENTS

APPENDIX IA
SPECIFICATION CONTROL DRAWING
FOR MEMORY HYBRID SWITCH

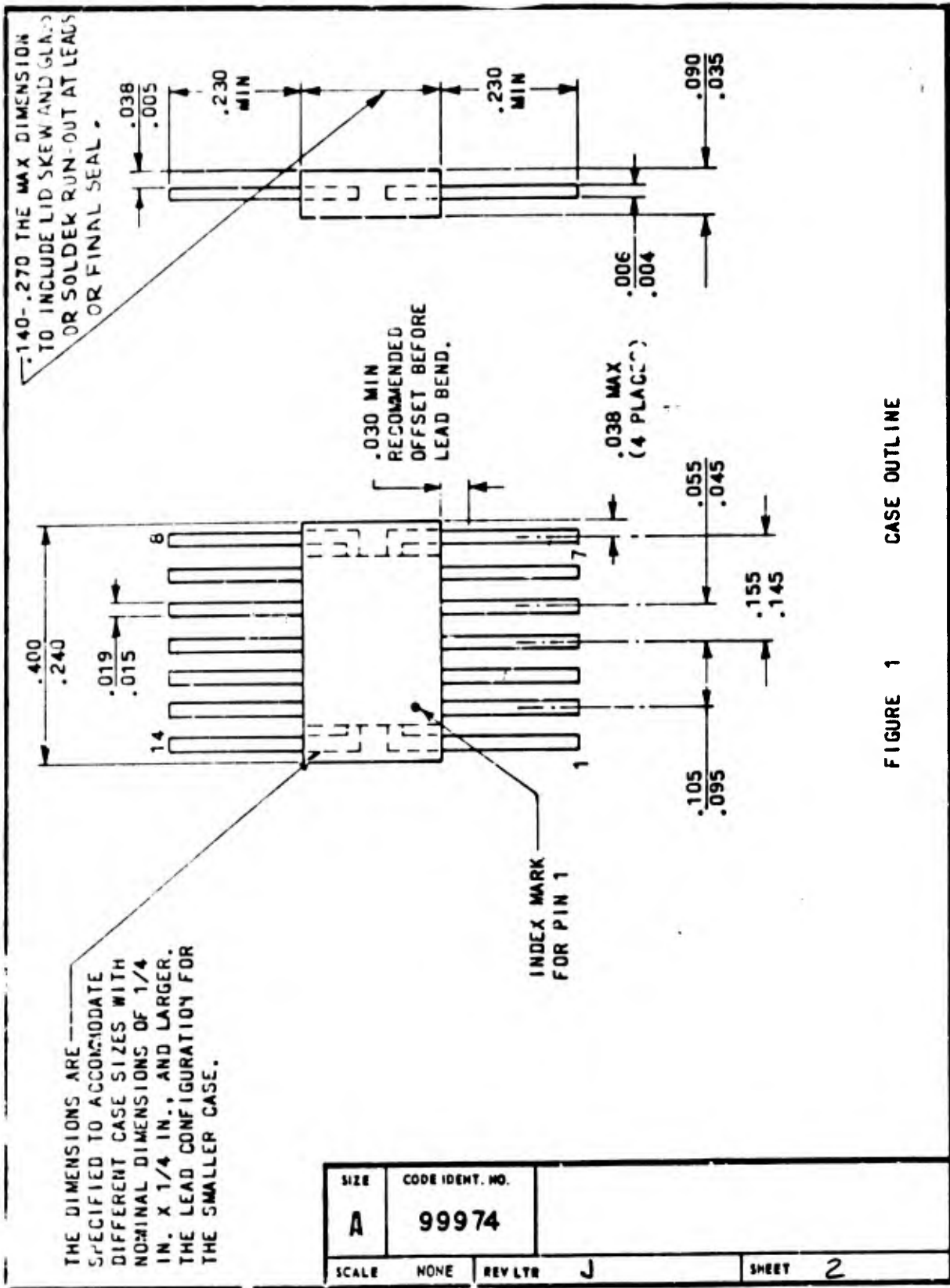
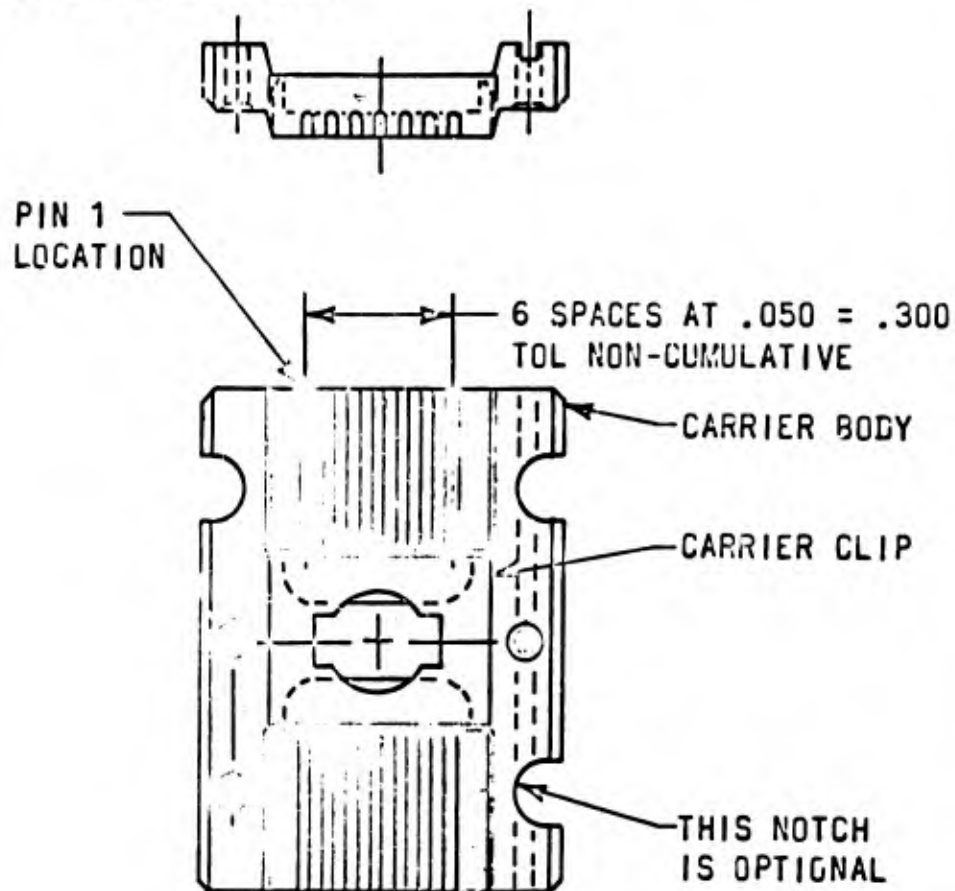


FIGURE 1 CASE OUTLINE

NOTE: CARRIER AND CLIP SHALL BE CAPABLE OF WITHSTANDING -55°C TO +150°C TEMP RANGE WITHOUT DAMAGE OR DEGRADATION.

SUGGESTED SOURCE(S) OF SUPPLY:
BARNES DEV. CORP.
LANSDOWNE, PA.



BARNES CLIP TYPE 029-504 OR 029-267-01
BARNES CARRIER TYPE 029-003

FIGURE 4

SIZE	CODE IDENT. NO.		
	99974		
SCALE	FORM	REV LTR	H
			SHEET 3

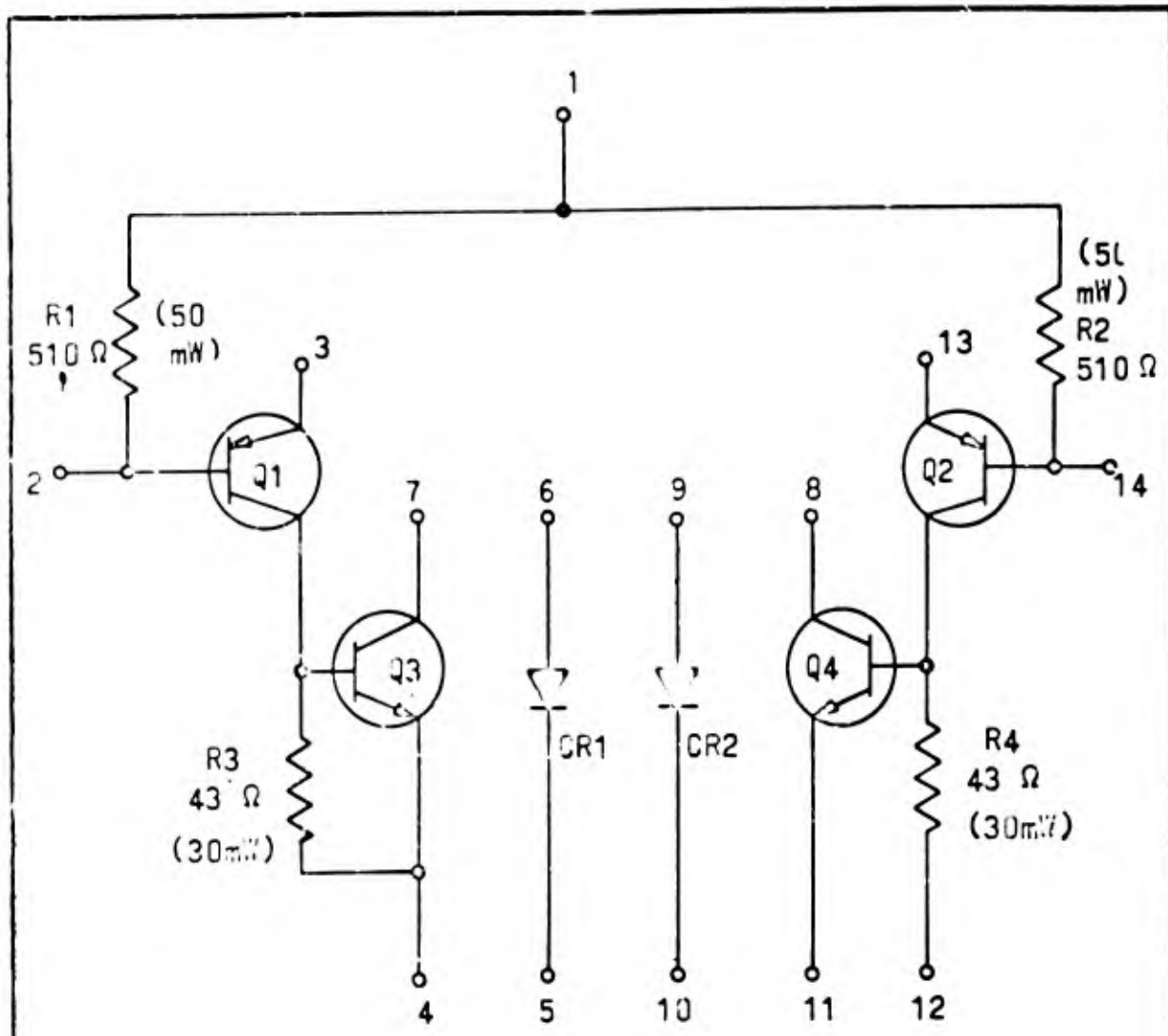


FIGURE 2
CIRCUIT SCHEMATIC

COMPONENT VALUES SHOWN
ARE NOMINAL. Q1 AND Q2
ARE SIMILAR TO 2N3505,
Q3 AND Q4 ARE SIMILAR TO
2N3725. CR1 AND CR2 ARE
SIMILAR TO 1N4610.

SIZE	CODE IDENT. NO.
1	99974
SCALE	REV LTR
100	C
SHEET	4

PULSES INTO TTL GATE SHALL HAVE A PULSE WIDTH OF $1\mu\text{SEC}$,
 A DUTY CYCLE OF 5% MAX, AND A RISE AND FALL TIME OF
 20nSEC MAX.

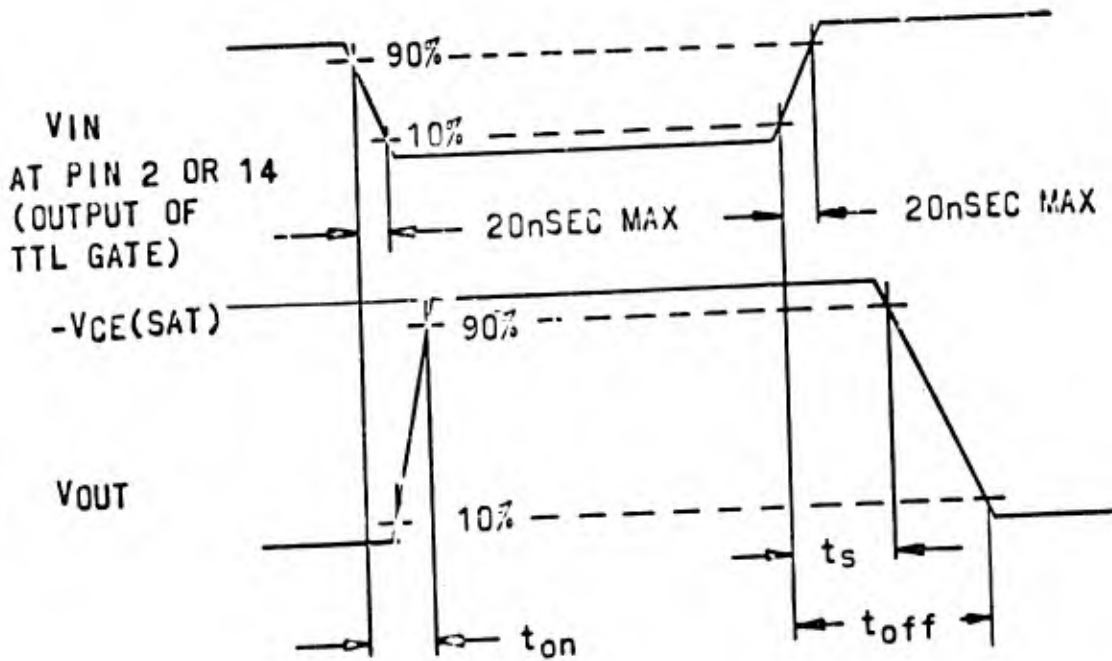
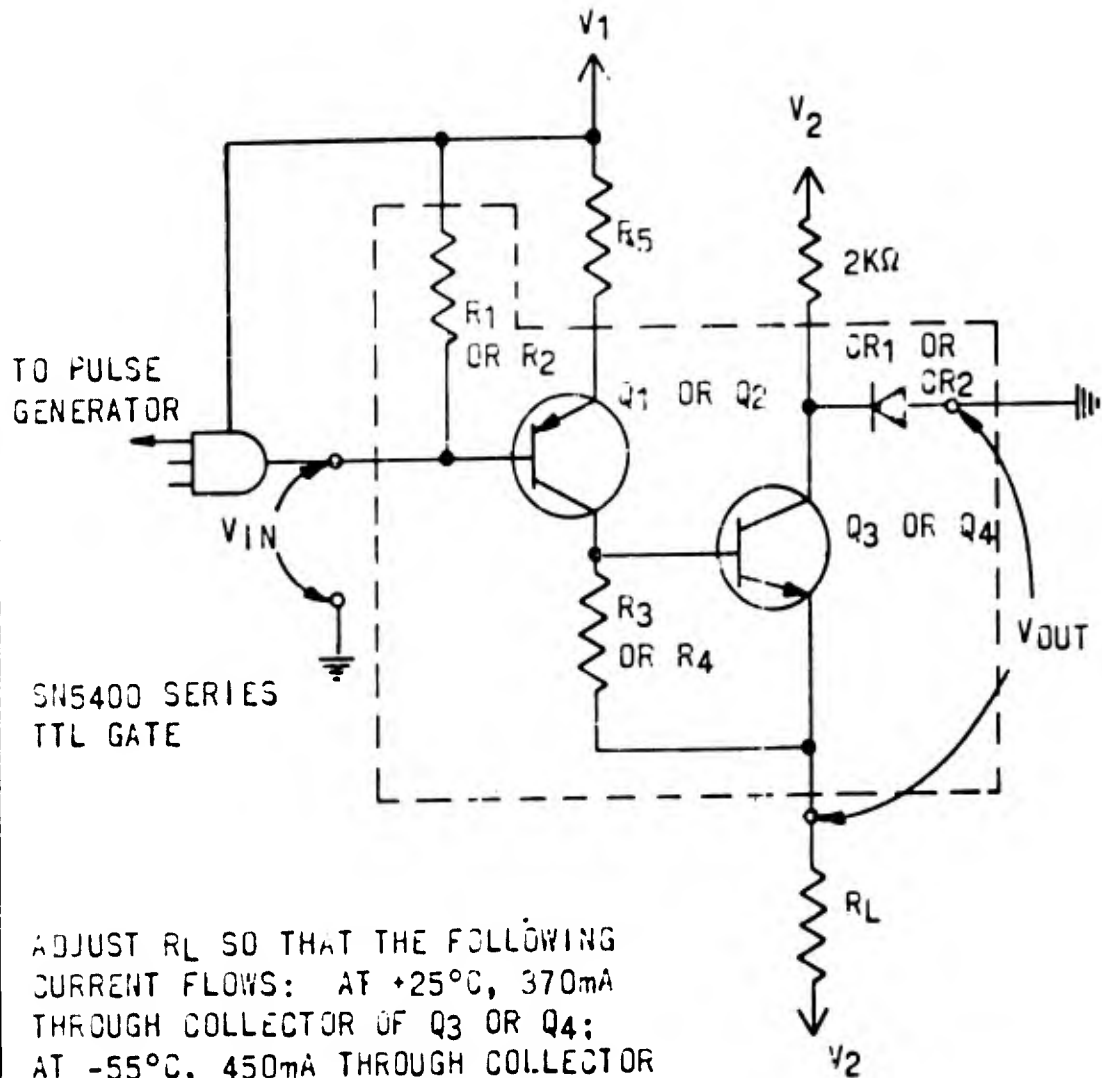


FIGURE 3 (CONT. ON SHEET 5)
 SWITCHING TIMES TEST CIRCUIT
 AND WAVEFORMS

SIZE	CODE IDENT. NO.	
	99974	
SCALE	FORME	REV LTR D
		SHEET 5

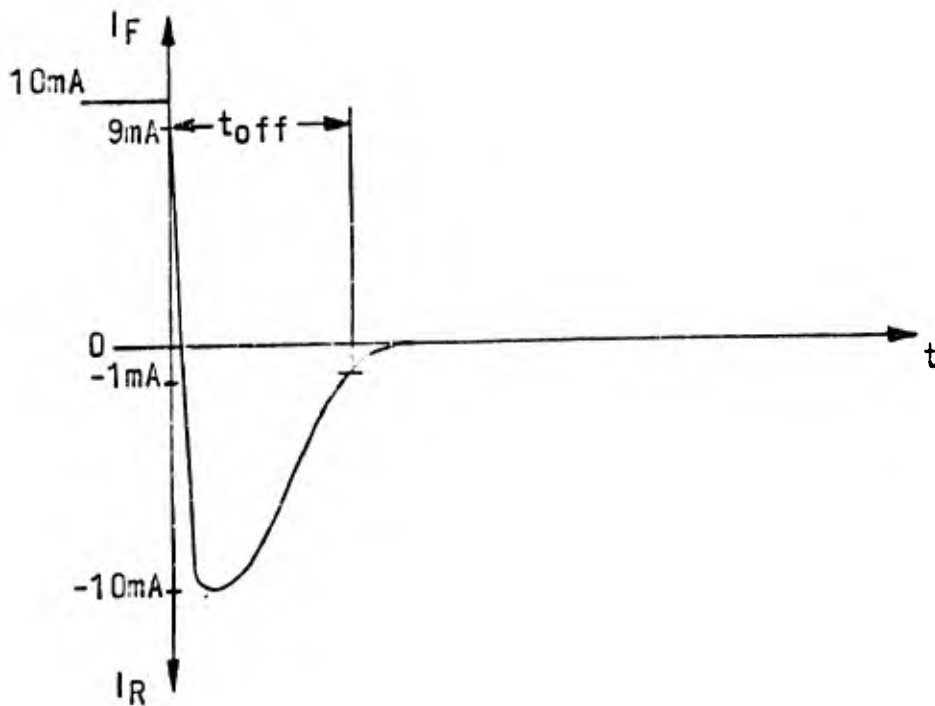
$V_1 = 5.0V$
 $V_2 = -30V$



ADJUST R_L SO THAT THE FOLLOWING
 CURRENT FLOWS: AT $+25^\circ C$, $370mA$
 THROUGH COLLECTOR OF Q_3 OR Q_4 ;
 AT $-55^\circ C$, $450mA$ THROUGH COLLECTOR
 OF Q_3 OR Q_4 ; AT $+125^\circ C$, $183mA$
 THROUGH COLLECTOR OF Q_3 OR Q_4 .
 ADJUST R_5 FOR $64 mA$
 I_E Q_1 OR Q_2

FIGURE 3 (CONTINUED)
 SWITCHING TIMES TEST CIRCUIT
 AND WAVEFORMS

SIZE	CODE IDENT. NO.	
A	99974	
SCALE	NONE	REV LTR D
		SHEET 6



MEASURED WITH DIODE SWITCHING TIME TESTER
 TEHTRONIX TYPE 291, PULSE GENERATOR HP
 MODEL 215A AND SAMPLING SCOPE TEHTRONIX
 MODEL 567

FIGURE 5

SIZE	CODE IDENT. NO.	
A	99974	
SCALE	NONE	REV LTR H
		SHEET 7

TABLE I (NOTE 1)

DASH NO.	ABSOLUTE MAXIMUM RATINGS AT TA = +25°C UNLESS OTHERWISE SPECIFIED												
	V DC	V DC	V DC	V DC	V DC	V DC	V DC	V DC	V DC	V DC	V DC	V DC	V DC
ALL	+5	+5	+4	+4	+4	+4	+4	+4	+4	+4	+4	+4	+4
	100												

TABLE I (NOTE 1) (CONTINUED)

DASH NO.	ABSOLUTE MAXIMUM RATINGS AT TA = +25°C UNLESS OTHERWISE SPECIFIED													CATEGORY NUMBER OF ST1000		
	MA DC	MA DC	MA DC	MA DC	MA DC	MA DC	MA DC	MA DC	MA DC	MA DC	MA DC	MA DC	MA DC			
-001	600	600	600	600	600	600	600	600	600	600	600	600	600	50	50	1
-003	600	600	600	600	600	600	600	600	600	600	600	600	600	50	50	2

TABLE I (NOTE 1) (CONTINUED)

DASH NO.	MANUFACTURER'S TYPE DESIGNATION
-001	
-002	
-003	
-004	

THE PART NUMBER IS THE DRAWING NUMBER PLUS THE APPLICABLE DASH NUMBER

SIZE	CODE IDENT NO	
A	99074	
SCALE	NOTE	REV LTR I
		SHEET 00

TABLE II ELECTRICAL SPECIFICATIONS

DASH NO	CHARACTERISTIC	SYMBOL	LIMITS		TEST CONDITIONS T _A = +25°C UNLESS OTHERWISE SPECIFIED (NOTE 1)			
			MIN	MAX	PIN 1	PIN 2	PIN 3	
ALL	RESISTOR TESTS	R ₁ (2)	7.35mA	9.80mA	GRD	4.5V		
		R ₂ (14)	7.35mA	9.80mA	GRD			
	DIODE REVERSE CURRENTS	I _R (8)			-100nA			
		I _R (9)			-100nA			
		I _R (6)			-12.μA			
		I _R (9)			12.μA			
	DIODE FORWARD VOLTAGE	V _F (8)			1.5V			
		V _F (9)			1.5V			
	CURRENT LEAKAGE TESTS	I _L (5,7)			2.0μA	NOTE 3	NOTE 3	
		I _L (8,13)			2.0μA	NOTE 4		
		I _L (3,7)			12.0μA	NOTE 3	NOTE 3	
		I _L (8,13)			12.0μA	NOTE 4		
	CURRENT SOURCE TESTS	I _S (4)		-63.2mA	-64.8mA		0.390V	NOTE 8
		I _S (11,12)		-63.2mA	-64.8mA			
		I _S (4)		-65.7mA	-67.7mA		0.390V	NOTE 8
		I _S (11,12)		-65.7mA	-67.7mA			
		I _S (4)		NOTE 9	NOTE 9		0.390V	NOTE 8
		I _S (11,12)		NOTE 9	NOTE 9			
	SWITCH SATURATION VOLTAGE TEST	V _{SAT} (4)			-0.5V	6.0V	0.390V	NOTE 8
		V _{SAT} (11,12)			-0.5V	6.0V		
V _{SAT} (4)				-0.6V	6.0V	0.390V	NOTE 8	
V _{SAT} (11,12)				-0.6V	6.0V			
-003 AND -004	CR1 AND CR2 SWITCHING TIME TEST	T _{OFF} (5,6)		10	-	-	-	
		T _{OFF} (9,10)		NAND SECS	-	-	-	
-003 AND -004	TRANSITION CAPACITANCE C _T FOR CR1 AND CR2	C _T (5,6)		3	-	-	-	
		C _T (9,10)		PT	-	-	-	

SIZE	COE IDENT NO	
A	99974	
SCALE	REV LTR	SHEET 9

TABLE 1 ELECTRICAL SPECIFICATIONS (CONTINUED)

SYMBOL	TEST CONDITIONS (CONTINUED)									
	T _A = +25°C UNLESS OTHERWISE SPECIFIED (NOTE 1)									
	PIN 4	PIN 5	PIN 6	PIN 7	PIN 8	PIN 9	PIN 10	PIN 11	PIN 12	
R1(2)										
R2(14)										
I _R (6)		GRD	-45V							
I _R (9)						-45V	GRD			
I _R (6)		GRD	-45V							
I _R (9)						-45V	GRD			
I _F (6)		GRD	400mA							
I _F (9)						400mA	GRD			
I _L (1,3,7)	GRD			NOTE 3						
I _L (1,8,13)					NOTE 4		GRD	GRD		
I _L (1,3,7)	GRD			NOTE 3						
I _L (1,8,13)					NOTE 4		GRD	GRD		
I _S (4)	-2.0V									
I _S (11,12)								NOTE 5	NOTE 5	
I _S (4)	-2.0V									
I _S (11,12)								NOTE 5	NOTE 5	
I _S (4)	-2.0V									
I _S (11,12)								NOTE 5	NOTE 5	
V _{SAT} (4)	NOTE 7			GRD						
V _{SAT} (11,12)					GRD			NOTE 6	NOTE 6	
V _{SAT} (4)	NOTE 7			GRD						
V _{SAT} (11,12)					GRD			NOTE 6	NOTE 6	
T _{OFF} (5,6)	-		I _F = 10 mA I _D = 10 mA RECOVERED TO 1 mA	-	-	I _F = 10 mA I _R = 10 mA RECOVERED TO 1 mA	-	-		
T _{OFF} (9,10)	-		R _L = 100 Ω SEE FIG. 5	-	-	R _L = 100 Ω SEE FIG. 5	-	-		
C _T (5,6)	-		f = 1 MEG HZ D.C. BIAS = 0V	-	-	f = 1 MEG HZ D.C. BIAS = 0V	-	-		
C _T (9,10)	-		A.C. SIGNAL = 0.25V _{pp} MAX	-	-	A.C. SIGNAL = 0.25V _{pp} MAX	-	-		

REV	CODE IDENT NO	
1.	99974	
SCALE	NONE	REV LTR H
		SHEET 10

TABLE II ELECTRICAL SPECIFICATIONS (CONTINUED)

DASH NO	TEST CONDITIONS (CONTINUED)		T _A =25°C UNLESS OTHERWISE SPECIFIED (NOTE 1)	
	SYMBOL	PIN 13	PIN 14	INSPECTION LEVELS LTPD MAX ACCEPT. NO.
ALL	R ₁ (2)			100% INSPECTION
	R ₂ (14)		4.5V	100% INSPECTION
	IR(6)			100% INSPECTION
	IR(9)			100% INSPECTION
	IR(6)			10 3
	IR(9)			10 3
	VF(6)			100% INSPECTION
	VF(9)			100% INSPECTION
	IL(1,3,7)			100% INSPECTION
	IL(1,8,13)	NOTE 4		100% INSPECTION
	IL(1,3,7)			10 3
	IL(1,8,13)	NOTE 4		10 3
	IS(4)			100% INSPECTION
	IS(11,12)	NOTE 8	0.390V	100% INSPECTION
	IS(4)			10 3
	IS(11,12)	NOTE 8	0.390V	10 3
	IS(4)			10 3
	IS(11,12)	NOTE 8	0.390V	10 3
	VSAT(4)			10 3
	VSAT(11,12)	NOTE 8	0.390V	10 3
VSAT(4)			100% INSPECTION	
VSAT(11,12)	NOTE 8	0.390V	100% INSPECTION	
-003 AND -004	T _{off} (5,6)			15 2
	T _{off} (9,10)			15 2
	C _T (5,6)			15 2
	C _T (9,10)			15 2

SIZE	CODE IDENT NO.	
A	99974	
SCALE	PONE	REV LTR H SHEET 11

TABLE IV. ELECTRICAL SPECIFICATIONS (CONTINUED)

DASH NO	CHARACTERISTICS		SYMBOL	LIMITS		TEST CONDITIONS T _A = +25°C UNLESS OTHERWISE SPECIFIED (NOTE 1)
				MIN	MAX	
ALL	SWITCHING TIME TEST	T _A = +125°C	t _{on} (4)		40rSEC	SEE FIGURE 3 FOR TEST CONDITIONS AND WAVEFORMS
			t _{on} (11,12)		40rSEC	
			t _s (4)		140rSEC	
			t _s (11,12)		140rSEC	
			t _{off} (4)		210rSEC	
			t _{off} (11,12)		210rSEC	
		T _A = -55°C	t _{on} (4)		60rSEC	
			t _{on} (11,12)		60rSEC	
			t _s (4)		60rSEC	
			t _s (11,12)		60rSEC	
			t _{off} (4)		100rSEC	
			t _{off} (11,12)		100rSEC	
		T _A = +25°C	t _{on} (4)		40rSEC	
			t _{on} (11,12)		40rSEC	
			t _s (4)		80rSEC	
			t _s (11,12)		80rSEC	
			t _{off} (4)		120rSEC	
			t _{off} (11,12)		120rSEC	

SIZE	CONFIDENT NO	
R	99974	
SCALE	NAME	REV LTR H SHEET 12

TABLE 11 ELECTRICAL SPECIFICATIONS (CONTINUED)

DASH NO	SYMBOL	TEST CONDITIONS (CONTINUED)	TA = +25°C UNLESS OTHERWISE SPECIFIED (NOTE 1)	
			INSPECTION LEVELS	
			LTPD	MAX ACCEPT. NO.
ALL	ton(4)	SEE FIGURE 3 FOR TEST CONDITIONS AND WAVEFORMS	15	2
	ton(11,12)		↑	↑
	ts(4)			
	ts(11,12)			
	toff(4)			
	toff(11,12)			
	ton(4)			
	ton(11,12)			
	ts(4)			
	ts(11,12)			
	toff(4)			
	toff(11,12)			
	ton(4)			
	ton(11,12)			100% INSPECTION
	ts(4)			↑
	ts(11,12)			
	toff(4)			
	toff(11,12)			↓
			100% INSPECTION	

SIZE	CODE IDENT. NO.	
A	999 74	
SCALE	NONE	REV LTR H SHEET 13

REQUIREMENTS:

1. GENERAL:

- A. INTERPRET DRAWING IN ACCORDANCE WITH STANDARDS PRESCRIBED BY MIL-D-1000.
- B. DEVICES SHALL BE IN ACCORDANCE WITH SPECIFICATION ST1000 WITH CATEGORY AND MANUFACTURER'S TYPE DESIGNATED IN TABLE I.
- C. DEVICES SHALL BE SHIPPED IN CARRIERS DESCRIBED IN FIGURE 4. THE DEVICE LEADS SHALL NOT EXTEND OVER THE EDGE OF THE BARNES CARRIER.
- D. DEVICES SHALL BE IN ACCORDANCE WITH THE CURRENT NEGOTIATED CRITICAL PROCESS LIST PER PARA 3.2 OF ST1000.

2. INSPECTION BY SUPPLIER:

- A. ELECTRICAL SPECIFICATIONS PER THE REQUIREMENTS OF ST1000 AND TABLE II.

3. DESIGN:

- A. STORAGE TEMPERATURE RANGE: -65°C TO $+150^{\circ}\text{C}$.
- B. OPERATING AMBIENT TEMPERATURE RANGE: -55°C TO $+125^{\circ}\text{C}$.
- C. ELECTRICAL RATINGS PER TABLE I.
- D. THERMAL RESISTANCE:
 - (1) θ_{JC} (JUNCTION TO CASE): $100^{\circ}\text{C}/\text{WATT}$ MAXIMUM.
 - (2) θ_{JA} (JUNCTION TO AMBIENT): $200^{\circ}\text{C}/\text{WATT}$ MAXIMUM.
- E. ELECTRICAL SPECIFICATIONS PER TABLE II.
- F. CASE OUTLINE AND DIMENSIONS PER FIGURE 1.
- G. SCHEMATIC DIAGRAM PER FIGURE 2.
- H. THE PNP TRANSISTORS SHALL BE ELECTRICALLY SIMILAR TO A 2N3505 TRANSISTOR.
- J. THE NPN TRANSISTORS SHALL BE ELECTRICALLY SIMILAR TO A 2N3725 TRANSISTOR.
- K. THE DIODES SHALL BE ELECTRICALLY SIMILAR TO A 1N4610 DIODE.
- L. THE RESISTORS SHALL HAVE A MAXIMUM TEMPERATURE COEFFICIENT OF $300 \text{ PPM}/^{\circ}\text{C}$.

SIZE	CODE IDENT. NO.		
A	99974		
SCALE	NOTE	REV LTR H	SHEET 4

EQUIREMENTS: (CONTINUED)

4. SPECIAL CONDITIONING BY SUPPLIER (ST1000, CATEGORY 2 PARTS ONLY)

A. UNITS SHALL BE V-T STRESSED FOR 168 HOURS MINIMUM AT +125°C AND THE FOLLOWING CONDITIONS:

(1) PINS 4, 6, 9, 11 AND 12 CONNECTED TO GROUND.

(2) CONNECT PINS 2, 5, 7, 8, 10 AND 14 TO +40V.

(3) CONNECT PIN 1 THROUGH 2000 OHMS TO GROUND.

UPON COMPLETION OF THE TEST TIME, THE VOLTAGE SHALL BE MAINTAINED UNTIL THE DEVICES HAVE REACHED ROOM AMBIENT CONDITIONS. PARAMETERS SHALL BE MEASURED WITHIN 8 HOURS AFTER REMOVAL OF THE VOLTAGE.

SUGGESTED SOURCE(S) OF SUPPLY:

SIZE	CODE IDENT. NO.	
A	99974	
SCALE	NONE	REV LTR H
		SHEET 15

NOTES:

1. POSITIVE CURRENT FLOW SHALL BE DEFINED AS CURRENT GOING INTO THE PIN. " $V_{(n)}$ " DESIGNATES A VOLTAGE MEASURED AT PIN (n). TEST CONDITION TOLERANCES SHALL BE $\pm 0.2\%$ FOR ALL VOLTAGES, AND $\pm 0.3\%$ FOR ALL CURRENTS. RESISTOR VALUES SHALL BE $\pm 0.1\%$ FOR ALL TEST CONDITIONS. ALL TESTS ARE PERFORMED USING PULSES (NOT STEADY STATE D.C.).
2. PULSED CONDITIONS (NOT STEADY STATE D.C.) 50% DUTY CYCLE AT $f = 500\text{KHZ}$.
3. PINS 1, 3, 7 TOGETHER TO +45 VOLTS.
4. PINS 1, 8, 13 TOGETHER TO +45 VOLTS.
5. PINS 11, 12 TIED TOGETHER AND TO -2 VOLTS.
6. PINS 11, 12 TIED TOGETHER TO A VARIABLE RESISTOR WHICH IS CONNECTED TO -30 VOLTS. ADJUST THE VARIABLE RESISTOR UNTIL 450 mA MINIMUM FLOWS INTO PIN 8.
7. CONNECT PIN 4 TO A VARIABLE RESISTOR WHICH IS CONNECTED TO -30 VOLTS. ADJUST THE VARIABLE RESISTOR UNTIL 450 mA MINIMUM FLOWS INTO PIN 7.
8. 75.0 OHMS TO +6.00 VOLTS.
9. TO BE SPECIFIED.

SIZE	CODE IDENT. NO.	
A	99974	
SCALE	NONE	REV LTR H
		SHEET 16

APPENDIX IB
SPECIFICATION CONTROL DRAWING
FOR LADDER SWITCH AND DRIVER

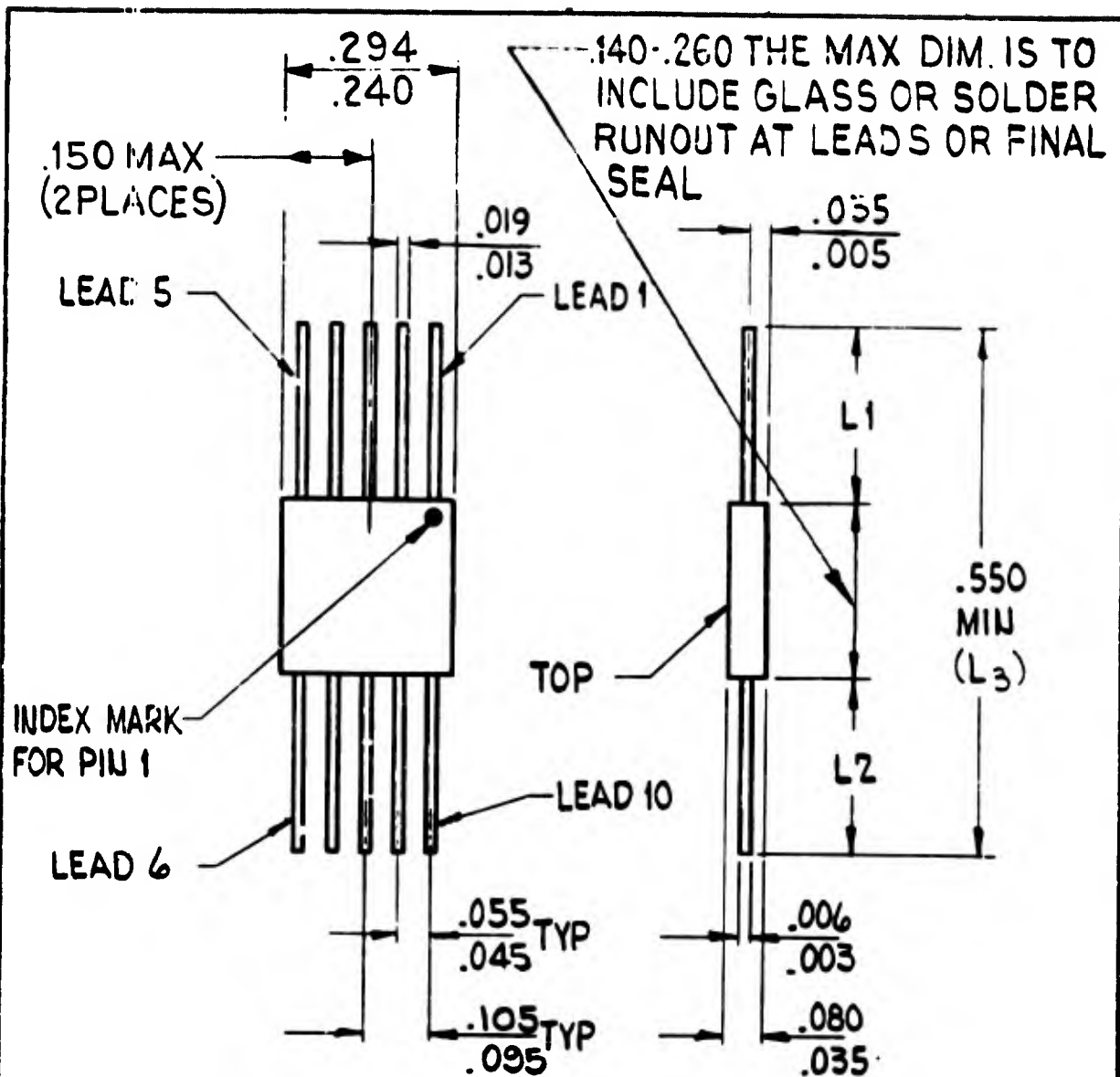


FIGURE 1. CASE OUTLINE

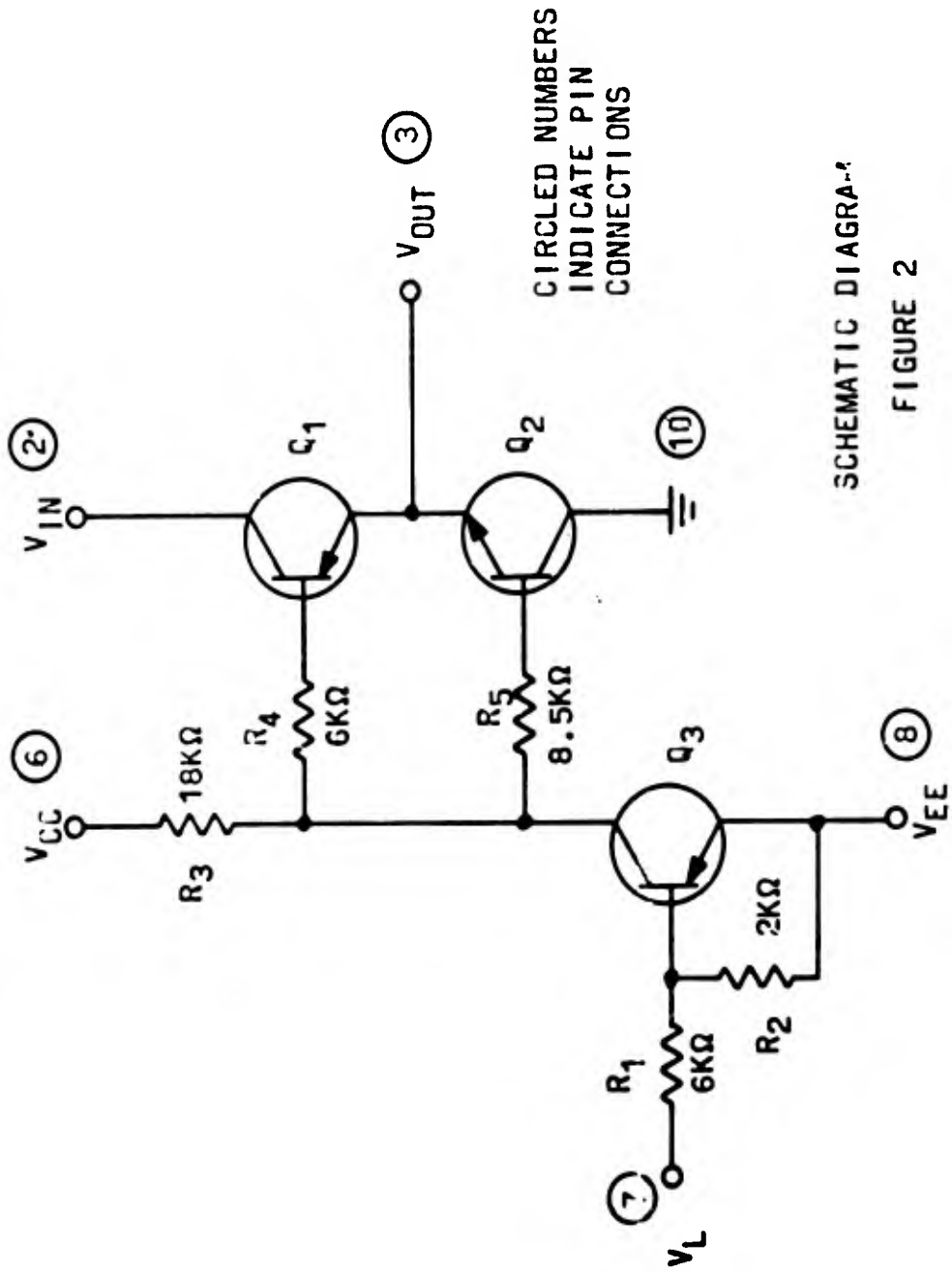
NOTES:

$L_1 = L_2 \pm 0.005$ FOR LEADS 2 THRU 10 WHEN OVERALL LENGTH (L_3) IS LESS THAN 0.560.

LEAD ① MAY BE SHORTER THAN LEADS ② THRU ⑩, BUT MINIMUM DIMENSION FROM TIP OF LEAD ① TO CENTER OF CASE IS 0.275.

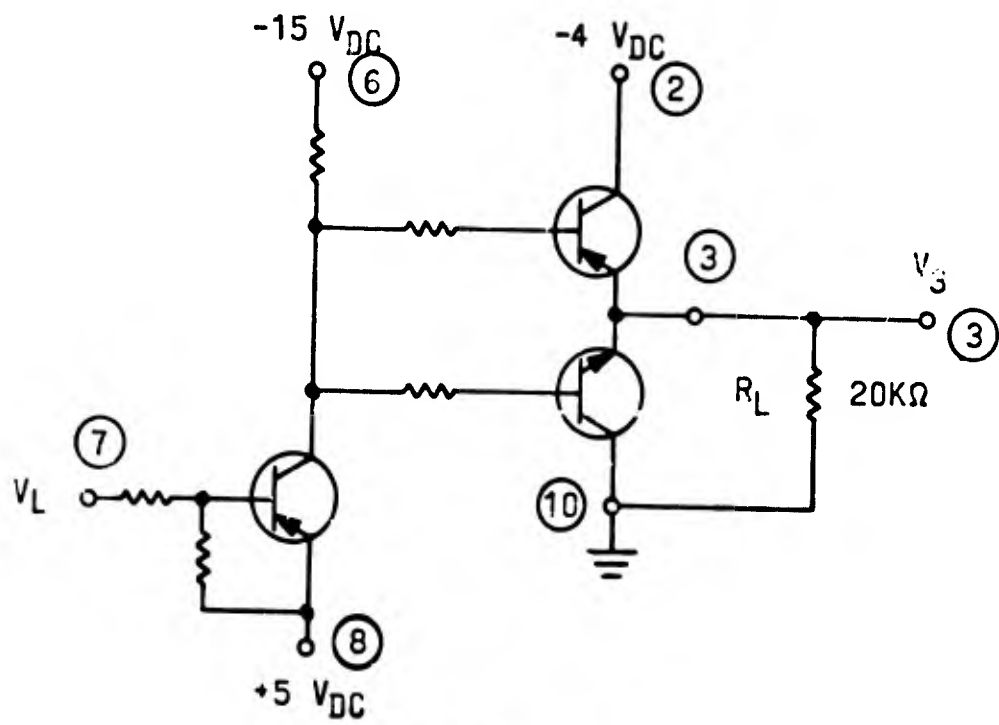
SIZE	CODE IDENT. NO.	
A	99974	
SCALE	NONE	REV LTR H SHEET 2

COMPONENT VALUES SHOWN ARE NOMINAL.
 Q1 AND Q3 ARE SIMILAR TO 2N2904.
 Q2 IS SIMILAR TO 2N2222.

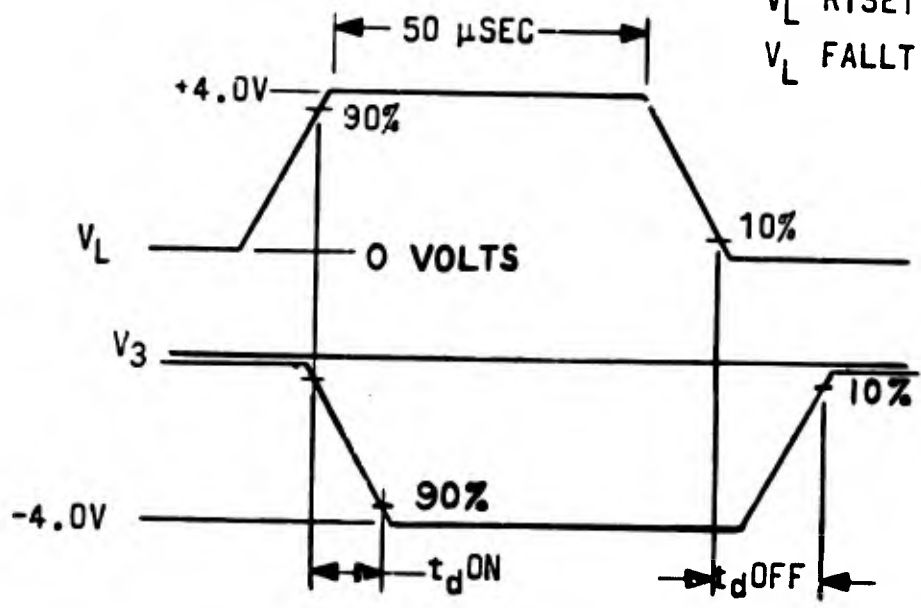


SCHEMATIC DIAGRAM
 FIGURE 2

SIZE	CODE IDENT. NO.		
A	99974		
SCALE	NONE	REV LTR	D
		SHEET	3

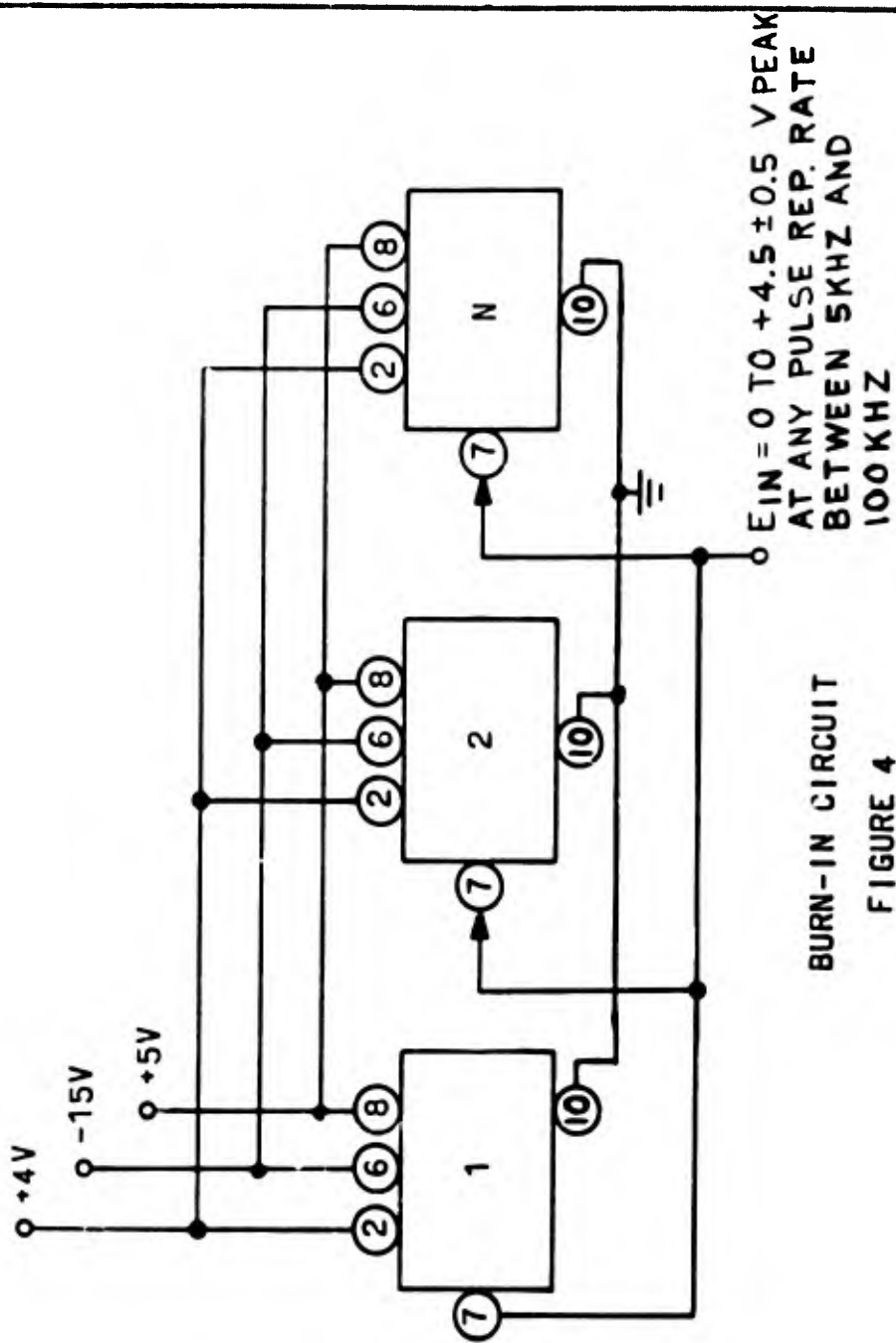


V_L RISE TIME < 20 nSEC
 V_L FALL TIME < 20 nSEC



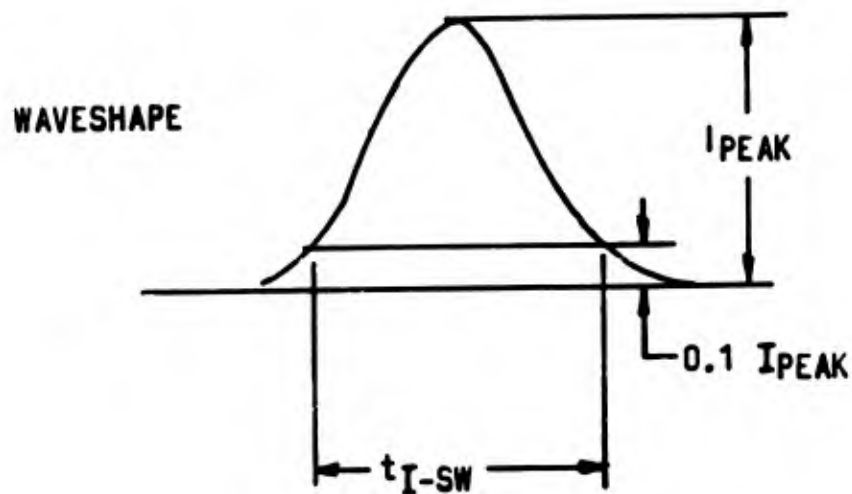
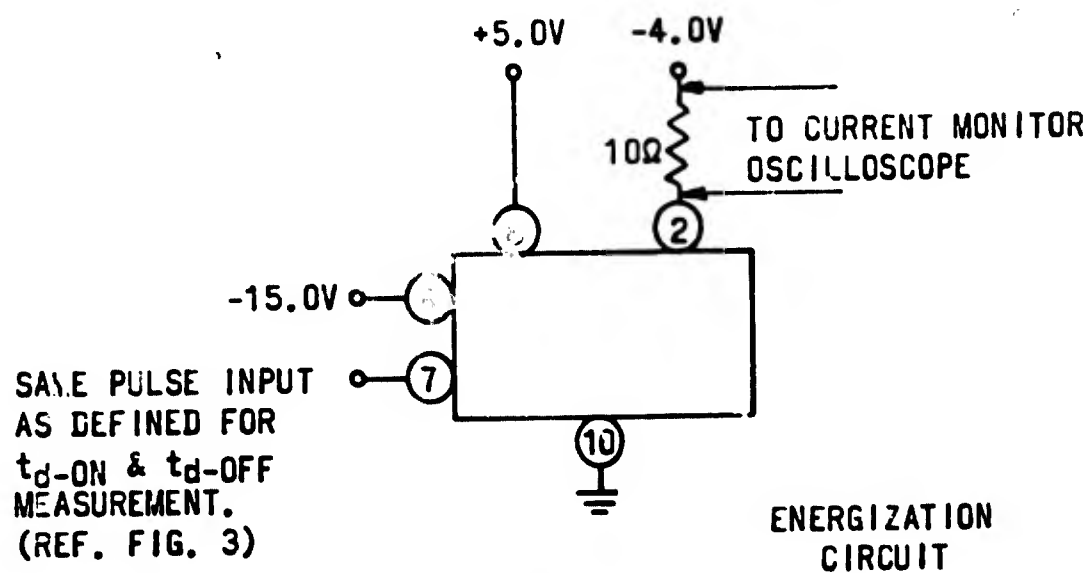
SWITCHING TIME TEST CIRCUIT
 FIGURE 3

SIZE	CODE IDENT. NO.		
A	99974		
SCALE	NONE	REV LTR	D
SHEET	4		



BURN-IN CIRCUIT
FIGURE 4

SIZE A	CODE IDENT. NO. 99974		
SCALE NONE	REV LTR	D	SHEET 5



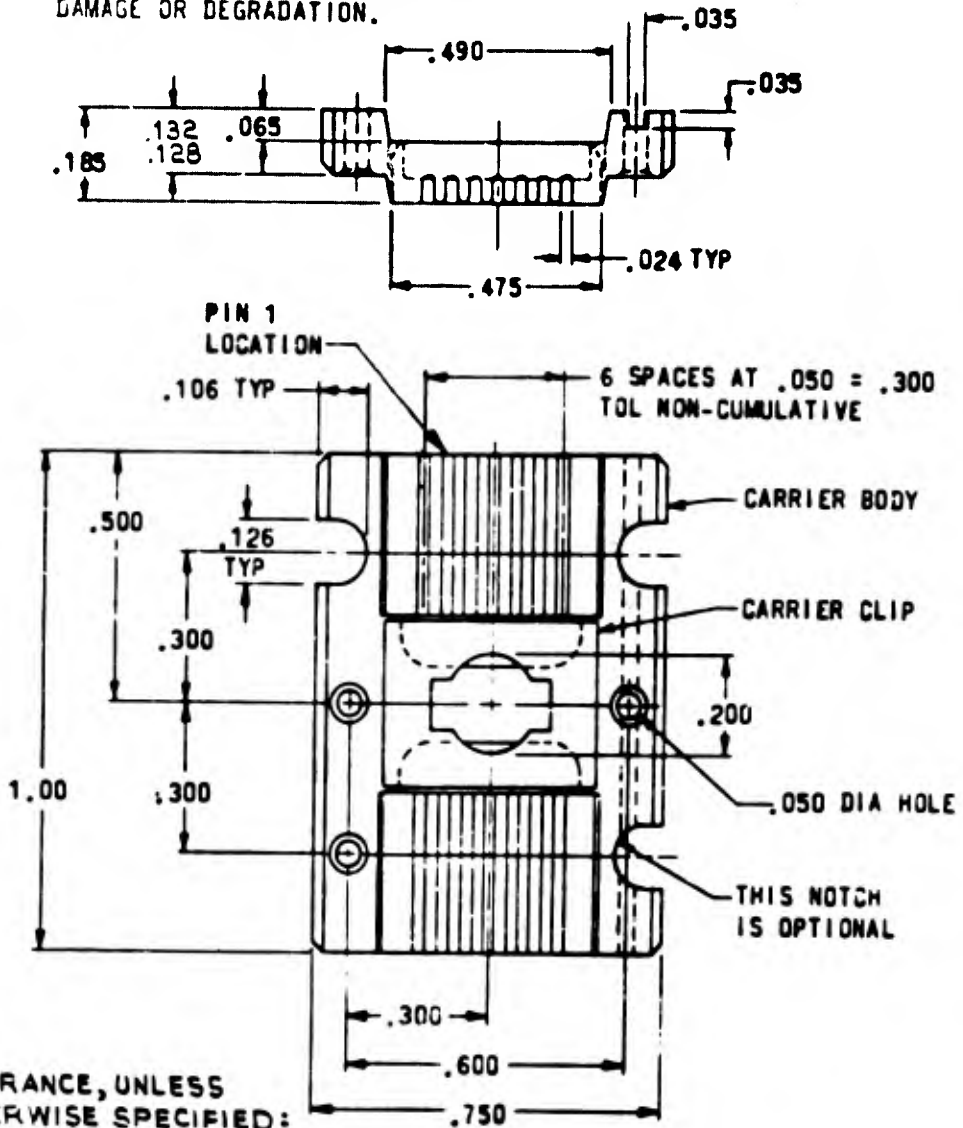
t_{I-SW} = TURN-ON OR TURN-OFF CURRENT TRANSIENT DURATION = .1.0 μ SEC MAX

FIGURE 5. TURN-ON AND TURN-OFF CURRENT TRANSIENT DURATION TEST CIRCUIT AND WAVESHAVE

SIZE	CODE IDENT. NO.	
A	99974	
SCALE	NONE	REV LTR D SHEET 6

NOTE:

CARRIER AND CLIP SHALL BE
 CAPABLE OF WITHSTANDING -55°C
 TO +150°C TEMP. RANGE WITHOUT
 DAMAGE OR DEGRADATION.



**TOLERANCE, UNLESS
 OTHERWISE SPECIFIED:**

TWO PLACE DECIMALS $\pm .02$

THREE PLACE DECIMALS $\pm .005$

BARNES CLIP TYPE 029-504 OR -267-01

BARNES CARRIER TYPE 029-003 OR -188

FIGURE 6

Q28	CODE IDENT NO	
A	99974	
SCALE	NONE	REV LTR H
		SHEET 7

TABLE I
ABSOLUTE MAXIMUM RATINGS

DASH NO.	COLLECTOR VOLTAGE VCC	EMITTER VOLTAGE VEE	DRIVER INPUT VOLTAGE VC	INPUT VOLTAGE VIN	INTERNAL POWER DISSIPATION PD
-001	-18.0 V	+6.0V	+6.0V	+5.5V	45 MW
-002					
-003					
-004					
-005					
-006	-18.0 V	+6.0V	+6.0V	+5.5V	45 MW

TABLE I (CONTINUED)
MANUFACTURER'S TYPE DESIGNATION

DASH NO.	MANUFACTURER'S TYPE DESIGNATION	ST1000 CATEGORY NUMBER
-001		1
-002		1
-003		2
-004		2
-005		NOTE 2
-006		NOTE 2

THE PART NUMBER IS THE DRAWING NUMBER PLUS THE APPLICABLE DASH NUMBER.

SIZE	CODE IDENT. NO.	
A	99974	
SCALE	NONE	REV LTR
		G
		SHEET
		8

DASH NO.	PARAMETER	SYMBOL	MEASURED AT TERMINALS	VOLTAGE APPLIED AT TERMINAL (DC UNLESS OTHERWISE NOTED)										LIMIT	UNITS
				2	3	6	7	8	10	GRD					
-001	OFFSET	V01	2-3	+4.0	—	-15.0	+4.0	+5.0	—	—	—	—	1.0 MV MAX		
	VOLTAGE	V02	3-10	+4.0	—	—	+0.4	—	—	—	—	—	1.0 MV MAX		
-003	SERIES RESISTANCE (20Ω MAX)	RS1	2-3	2.8V RMS 1KHZ SINEWAVE	20K Ω BETWEEN PINS 3 & 10	—	+4.0	—	—	—	—	—	2.8 MV RMS MAX		
		RS2	3-10	2.8V RMS 1KHZ SINEWAVE	20K Ω BETWEEN PINS 2 & 3	—	+0.4	—	—	—	—	—	2.8 MV RMS MAX		
	LEAKAGE CURRENT	IC1	2	-4.0	—	—	+0.4	—	—	—	—	—	100 NA MAX		
		IC1	2	+4.0	—	—	+0.4	—	—	—	—	—	—		
		IC2	10	-4.0	—	—	+4.0	—	—	—	—	—	—		
		IC2	10	+4.0	—	—	+4.0	—	—	—	—	—	—	100 NA MAX	
	TURN-ON DELAY	t _{d-ON}	3-10	-4.0	—	—	FIG. 3 (PULSE)	—	—	—	—	—	3μSEC MAX		
	TURN-OFF DELAY	t _{d-OFF}	3-10	-4.0	—	—	FIG. 3 (PULSE)	—	—	—	—	—	3μSEC MAX		
	OFFSET VOLTAGE AT -55°C	V01(t)	2-3	+4.0	—	—	+4.0	—	—	—	—	—	2.0 MV MAX		
	OFFSET VOLTAGE AT +125°C	V02(t)	3-10	+4.0	—	—	+0.4	—	—	—	—	—	2.0 MV MAX		
	RESISTANCE AT -55°C AND +125°C	RS1(t)	2-3	2.8V RMS 1KHZ SINEWAVE	20K Ω BETWEEN PINS 3 & 10	—	+4.0	—	—	—	—	—	2.8 MV RMS		
		RS2(t)	3-10	2.8V RMS 1KHZ SINEWAVE	20K Ω BETWEEN PINS 2 & 3	—	+0.4	—	—	—	—	—	2.8 MV RMS		
	TURN-ON AND TURN-OFF CURRENT TRANSIENT DURATION	t _{1-SW}	REF. FIG. 5	-4.0	—	—	FIG. 5 (PULSE)	—	—	—	—	—	1.0μSEC MAX		
		I _L "0"	7	+4.0	—	—	+0.4	—	—	—	—	—	-1.0 MA MAX		
	POWER SUPPLY DRAIN CURRENTS	I _{EE} "0"	8	+4.0	—	—	+0.4	—	—	—	—	—	2.92 MA MAX		
		I _{CC} "0"	6	+4.0	—	-15.0	+0.4	+5.0	GRD	—	—	—	-1.31MA MAX		

NOTE 1 ELECTRICAL CHARACTERISTICS, MEASURED AT +25 ± 3°C UNLESS OTHERWISE SPECIFIED

TABLE II

SIZE A CODE IDENT. 99974

SCALE NONE REV LTR ITT SHEET 10

DASH NO.	PARAMETER	SYMBOL	MEASURED AT TERMINALS	VOLTAGE APPLIED AT TERMINAL (DC UNLESS OTHERWISE NOTED)										LIMIT	UNITS
				2	3	6	7	8	10						
-002 & -004	OFFSET	V01	2-3	+4.0	—	-15.0	+4.0	+5.0	GRD	2.0	MV	MAX			
	VOLTAGE	V02	3-10	+4.0	—	—	+0.4	—	—	2.0	MV	MAX			
	SERIES RESISTANCE (300 MAX)	RS1	2-3	2.8V RMS	20K Ω						4.2	MV	RMS		
				1KHZ SINEWAVE	BETWEEN PINS 3 & 10								MAX		
		RS2	3-10	2.8V RMS	20K Ω						4.2	MV	RMS		
				1KHZ SINEWAVE	BETWEEN PINS 2 & 3								MAX		
	LEAKAGE CURRENT	IC1	2	-4.0	—	—	+0.4	—	—	100	NA	MAX			
		IC1	2	+4.0	—	—	+0.4	—	—	—	—	—			
		IC2	10	-4.0	—	—	+4.0	—	—	—	—	—			
		IC2	10	+4.0	—	—	+4.0	—	—	—	100	NA	MAX		
	TURN-ON DELAY	t _{d-ON}	3-10	-4.0	—	—	FIG. 3 (PULSE)	—	—	3	μSEC	MAX			
	TURN-OFF DELAY	t _{d-OFF}	3-10	-4.0	—	—	FIG. 3 (PULSE)	—	—	3	μSEC	MAX			
	OFFSET VOLTAGE AT -55°C & +125°C	V01(t)	2-3	+4.0	—	—	+4.0	—	—	4.0	MV	MAX			
		V02(t)	3-10	+4.0	—	—	+0.4	—	—	4.0	MV	MAX			
	SERIES RESISTANCE AT -55°C AND +125°C	RS1(t)	2-3	2.8V RMS	20K Ω						4.2	MV	RMS		
				1KHZ SINEWAVE	BETWEEN PINS 3 & 10										
		RS2(t)	3-10	2.8V RMS	20K Ω						4.2	MV	RMS		
				1KHZ SINEWAVE	BETWEEN PINS 2 & 3										
	TURN-ON AND TURN-OFF CURRENT TRANSIENT DURATION	t _{I-SW}	REF. FIG. 5	-4.0	—	—	FIG. 5 (PULSE)	—	—	1.0	μSEC	MAX			
				4.0	—	—	+0.4	—	—	—	—	—	—		
				4.0	—	—	+0.4	—	—	—	—	—	—		
	LOGIC "0" INPUT CURRENT	I _L "0"	7	4.0	—	—	+0.4	—	—	—	—	—			
				4.0	—	—	+0.4	—	—	—	—	—			
				4.0	—	—	+0.4	—	—	—	—	—			
	POWER SUPPLY DRAIN CURRENTS	I _{CC} "0"	6	4.0	—	-15.0	+0.4	+5.0	GRD	2.82	MA	MAX			
				4.0	—	—	+0.4	—	—	—	—	—	—		

NOTE 1 ELECTRICAL CHARACTERISTICS, MEASURED AT +25 ± 3°C UNLESS OTHERWISE SPECIFIED

TABLE II (CONTINUED)

SCALE	NONE	REV LTR	E	SHEET	10
SEE	CODE IDENT. NO.				
A	99974				

TABLE III. INSPECTION REQUIREMENTS

DASH NO.	PARAMETER	SYMBOL	LTPD	MAXIMUM ACCEPTANCE NUMBER
-001 THRU	OFFSET VOLTAGE (25°C)	V ₀₁	—	100% INSPECTION
		V ₀₂		
-004	SERIES RESISTANCE (25°C)	R _{S1}	—	100% INSPECTION
		R _{S2}		
	LEAKAGE CURRENT	I _{C1}	—	100% INSPECTION
		I _{C1}		
		I _{C2}		
		I _{C2}		
	TURN-ON DELAY	t _{d-ON}	5	3
	TURN-OFF DELAY	t _{d-OFF}	5	3
	OFFSET VOLTAGE AT -55°C AND +125°C	V ₀₁ (t)	5	3
		V ₀₂ (t)		
	SERIES RESISTANCE AT -55°C AND +125°C	R _{S1} (t)	5	3
		R _{S2} (t)		
	TURN-ON AND TURN-OFF CURRENT TRANSIENT DURATION	t _{I-SW}	5	3
	LOGIC "0" INPUT CURRENT	I _L "0"	100% INSPECTION	
	POWER SUPPLY DRAIN CURRENTS	I _{EE} "0"	100% INSPECTION	
		I _{CC} "0"	100% INSPECTION	
		I _{IN} "1"	100% INSPECTION	

SIZE	CODE IDENT. NO.	
A	99974	
SCALE	NONE	REV LTR E SHEET 11

REQUIREMENTS:

1. GENERAL:

- A. INTERPRET DRAWING IN ACCORDANCE WITH STANDARDS PRESCRIBED BY MIL-D-1000.
- B. DEVICES SHALL BE IN ACCORDANCE WITH SPECIFICATION ST1000 WITH CATEGORY AND MANUFACTURER'S TYPE DESIGNATED IN TABLE I.
- C. DEVICES SHALL BE SHIPPED IN CARRIERS DESCRIBED IN FIGURE 6. DEVICE LEADS SHALL NOT EXTEND BEYOND THE ENDS OF THE CARRIER.

2. INSPECTION BY SUPPLIER:

- A. ELECTRICAL SPECIFICATIONS PER THE REQUIREMENTS OF ST1000 AND TABLES II AND III.
- B. CATEGORY 2 DEVICES SHALL BE BURNED IN PER THE CIRCUIT OF FIGURE 4 AT $T_A = +125^\circ\text{C}$ FOR 168 HOURS MINIMUM.

3. DESIGN:

- A. OPERATING TEMPERATURE RANGE: -55°C TO $+125^\circ\text{C}$.
- B. ELECTRICAL RATINGS PER TABLES I AND II.
- C. CASE OUTLINE AND DIMENSIONS PER FIGURE 1.
- D. SCHEMATIC AND CONNECTION DIAGRAM PER FIGURE 2.
- E. LEAD ARRANGEMENT PER FIGURE 1.
- F. STORAGE TEMPERATURE RANGE: -65°C TO $+150^\circ\text{C}$.
- G. THERMAL RESISTANCE:
 - (1) θ_{JC} (JUNCTION TO CASE): TO BE SPECIFIED BY SUPPLIER
 - (2) θ_{JA} (JUNCTION TO AMBIENT): TO BE SPECIFIED BY SUPPLIER

SIZE	CODE IDENT. NO.	
A	99974	
SCALE	NONE	REV LTR H
		SHEET 12

SUGGESTED SOURCE(S) OF SUPPLY:

NOTES:

1. POSITIVE CURRENT FLOW SHALL BE DEFINED AS CURRENT GOING INTO THE PIN. TEST CONDITION TOLERANCES SHALL BE $\pm 0.2\%$ FOR ALL VOLTAGES, AND $\pm 0.3\%$ FOR ALL CURRENTS. RESISTOR VALUES SHALL BE $\pm 0.1\%$ FOR ALL EXTERNAL TEST CONDITIONS. ALL CURRENTS AND VOLTAGES ARE DIRECT CURRENT UNLESS OTHERWISE SPECIFIED. ALTERNATING CURRENTS AND VOLTAGES ARE SPECIFIED AS RMS VALUES AND FREQUENCY IS 100 HZ UNLESS OTHERWISE SPECIFIED.
2. THE -005 PART IS IDENTICAL TO THE -003 PART AND THE -006 PART IS IDENTICAL TO THE -004 PART EXCEPT THE CASE WIDTH DIMENSION IN FIGURE 1 SHALL BE .240 TO .275 INSTEAD OF .240 TO .290 INCH. NOTE: DO NOT USE THE -005 AND -006 PART IN NEW DESIGNS.

SIZE	CODE IDENT. NO.		
A	99974		
SCALE	NONE	REV LTR	G
			SHEET 13

APPENDIX IC

**GENERAL SPECIFICATION FOR SEMICONDUCTOR DEVICES
AND ADDENDUM II (CATEGORY 2)**

MIL 1188A
REV. 4-61

OUR NEW NAME
AC ELECTRONICS
DIVISION OF
GENERAL MOTORS
CORPORATION

AC SPARK PLUG DIVISION
GENERAL MOTORS CORPORATION
MILWAUKEE 1, WISCONSIN

DATE 10 March 1969

ENGINEERING DEPT.

TOTAL NO. OF SHEETS 62

KEY

SPECIFICATION

NUMBER

REV.

ST1000

D

General Specification 10
Addendum I 6
Addendum II 11
Addendum III 12
Addendum IV 14
Total 62

CODE IDENT NO. 99974
Superseding
ST1000C
Dated: 11 September
1968

REFERENCE COPY

Subject to Change without Notice
No Parts to be Fabricated to this Print

GENERAL SPECIFICATION
SEMICONDUCTOR DEVICES

REV	ECO NO.	DATE	REV	ECO NO.	DATE
A	220512	6 April 1967			
B	ECM 232139	28 Mar 1968			
C	235281	11 Sept 1968			
D	237620	10 Mar 1969			

ORIGINAL ISSUE DATE: 1 August 1966
RELEASE AUTHORITY: General Use
CONTRACT: _____

APPROVALS

[Handwritten signatures and stamps]
PROG. ENGINEERING

[Handwritten signature]
REG. ENG.

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MILWAUKEE, WISCONSIN 53201

SPECIFICATION	
NUMBER	REV.
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CODE IDENT NO. 99974

1. SCOPE

1.1 SCOPE. This specification covers the requirements for semiconductor devices.

1.2 CLASSIFICATION. Specific requirements for a particular category of semiconductor devices are classified as follows.

- a. Category 1: Category 1 devices shall meet the requirements of Addendum 1.
- b. Category 2: Category 2 devices shall meet the requirements of Addendum 2.
- c. Category 3: Category 3 devices shall meet the requirements of Addendum 3.
- d. Category 4: Category 4 devices shall meet the requirements of Addendum 4.

2. APPLICABLE DOCUMENTS

2.1 The following documents shall form a part of this specification to the extent specified herein. Reference to these documents within this specification shall be construed as meaning the issue or revision specified in this applicable document list. When an issue or revision is not specified within this specification, the latest issue or revision of the referenced document shall apply.

SPECIFICATIONS**Military**

MIL-Q-9858A

Quality Program Requirements

MIL-S-19500D
 Amend 5, Supp 1C,
 Change Notice 1

Semiconductor Devices, General Specification for

MIL-C-45662A

Calibration System Requirements

AC Electronics

ST1011

General Specification, Levels for Nuclear Environments

STANDARDS**Military**

MIL-STD-202C
 Change Notice 1, 2 & 3

Test Methods for Electronic and Electrical
 Component Parts

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MIL-STD-750A Test Methods for Semiconductor Devices
 Change Notice 1 & 2

MIL-STD-883 Test Methods and Procedures for microelectronics
 Change Notice 1
 MIL-STD-1276A Weldable Leads for Electronic Components Parts

2.2 ORDER OF PRECEDENCE. In case of conflict, the following order of precedence shall apply:

- a. Purchase Order
- b. Negotiated critical processes (when applicable)
- c. The detail Specification Control Drawing (SCD)
- d. This specification
- e. Other referenced documents

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3. REQUIREMENTS

3.1 GENERAL. Devices furnished under this specification shall be capable of (see 6.2.6) meeting the requirements of Specification MIL-S-19500 with the following additions and exceptions including those of the detail SCD (see 6.2.5).

3.1.1 Marking. As a minimum, each device shall be marked with the following information:

- a. Manufacturer's name, trademark, or symbol.
- b. Manufacturer's type designation.
- c. Date code placed on the part or identified in packaging. The date code shall identify the week the device was final sealed. It shall consist of 3 or 4 digits identifying the week and year. Example: xxyy or xyy where x would be the year and y would be the week.

d. A delta (Δ) or dot placed on the device after burn in when burn in is specified on the detail SCD. If the device already has a dot for Pin 1 location or polarity a delta (Δ) or additional dot must be used to indicate burn in.

e. Polarity marking indicating cathode end on diodes. Where a dot is used to identify diode polarity, the burn in dot shall appear either on the cathode end or in the center of the diode body.

3.1.1.1 Method. Each device shall be marked using one of the following methods. The marking method shall not degrade the functional parameters of the device:

a. Preferred. Permanent and legible etching, stamping, stenciling, or engraving on the body of the device.

b. Alternate. Pressure sensitive adhesive labels attached to the body of the device. Printing on the label shall contrast noticeably with the color of the label. Labels shall adhere firmly to the device and printing shall remain legible during and after subsection of the device to the environmental and life requirements of this specification, and after storage at room ambient conditions for four years.

c. For flat packages and dual in line packages marking is to be on the top side i.e., the side opposite the principle base (chip mounting base).

3.1.2 Failure modes. The supplier shall notify the buyer of any failure modes, potential or existing, that can compromise the reliability or performance of parts furnished under this specification. Such notification shall be given either immediately, when the failure mode(s) are identified, or prior to the first shipment of the devices.

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3.1.3 Environmental and mechanical requirements. With the specific conditions stated in Table I, the environmental and mechanical requirements shall be as specified in 4.5.3.

3.1.4 Qualification. The semiconductor devices furnished to this specification shall be capable of meeting the qualification requirements of Specification MIL-S-19500.

3.1.5 Lot traceability. The manufacturer's date code or serialization of individual devices shall provide lot traceability from the buyer to the manufacturer's production lot (see 6.2.11).

3.1.6 Shelf life. The devices shall be capable of withstanding shelf storage at room ambient conditions for four years minimum and meet the requirements of the detail SCD after this time period.

3.1.7 Contamination control. The entire volume inside the package shall be free of any material or residue, loose or attached which may be injurious to or limit in any way the performance or reliability of the device.

3.2 **PROCESS CONTROL.** Process control shall be as specified in the applicable addendum.

3.3 **COMPLIANCE DATA.** Compliance data requirements shall be as specified in the applicable addendum.

3.4 **LEAD AND TERMINAL MATERIALS.** Leads and terminals of devices processed to this specification shall be as specified in the applicable addendum. The leads and terminals shall show no evidence of twists, kinks, or other imperfections under visual examination.

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TABLE I
 GROUP B INSPECTION

SUB-GROUP	EXAMINATION OR TEST	CONDITIONS	
		MIL-STD-750 Method	Specific Conditions
1	Solderability	2026	Specified in 4.5.3.1 of ST1000
1	Temperature Cycling	MIL-STD-883 Method 1010 Cond C	Transfer time 1 minute max
1	Thermal Shock	1056 Cond A	0° +5°, -0° to 100° +0°, -5°
1	Hermetic Seal	MIL-STD-202 Method 112 Cond C or MIL-STD-883 Method 1014 Cond A or B and C or D	Procedure I, II, III or IV for fine leak. Cond A or B for gross leak. Backfill pressure 28 psig. Min. leakage rate = 10 ⁻⁸ atm-cc/sec max
1	Moisture Resistance	1021	The initial conditioning may be omitted.
2	Shock	2016	G = 1500, 5 blows nonoperating, 0.5 msec, orientations X ₁ , Y ₁ , Z ₁ , Y ₂ Total: 20 blows
2	Vibration Fatigue	2046	Nonoperating
2	Vibration, Variable Frequency	2056	-
2	Constant Acceleration	2006	G = 20,000, orientation X ₁ , Y ₁ , Y ₂ , Z ₁
3	Lead Pull (for other than flat packages)	2036 Cond A	4 lb axial pull 30 sec per 4.5.3.2 of ST1000
3	Lead Pull (for flat packages only)	2036 Cond A	12 oz axial pull 30 sec per 4.5.3.3 of ST1000
3	Bending Stress (for other than flat packages)	2036 Cond E	Per 4.5.3.4 of ST1000
3	Bending Stress (for flat packages only)	--	2 bends per 4.5.3.5 of ST1000
3	Torque	2036 Cond D	Per 4.5.3.6 of ST1000
4	Barometric Pressure	MIL-STD-202 106 Cond E	-
5	Salt Atmosphere	1041	-
6	Hi Temp Voltage Stress	-	Per 4.5.3.9 of ST1000
6	Nonoperating Hi Temp Life	1031	Per 4.5.3.7 of ST1000
7	Operating Life	1026	Per 4.5.3.8 of ST1000

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4. QUALITY ASSURANCE PROVISIONS

4.1 GENERAL. Semiconductors furnished under this specification shall be capable of meeting the Quality Assurance Provisions of Specification MIL-S-19500 with the following additions and exceptions, including those of the detail SCD.

4.1.1 Inspection system requirements. The supplier's inspection system shall conform to the requirements of Specification MIL-Q-9858.

4.1.2 Calibration system requirements. The supplier's calibration system shall conform to the requirements of Specification MIL-C-45662.

4.2 DUPLICATION OF TESTS. This specification does not require duplication of any tests which may have been conducted on applicable devices in conjunction with the supplier's internal testing program. The supplier is invited to use his own internal high reliability program to supply parts under this specification if such a program includes devices described by the applicable detail SCD.

4.3 100 PERCENT PRECONDITIONING REQUIREMENTS. Preconditioning shall be performed on all devices as specified in the applicable addendum. All devices shall meet the limits specified for the preconditioning screens, and meet the mechanical or electrical limits specified in the detail SCD after preconditioning.

4.4 100 PERCENT SPECIAL CONDITIONING REQUIREMENTS. Special conditioning shall be performed on all devices as specified in the applicable addendum and SCD. All devices shall meet the limits specified in the detail SCD after special conditioning.

4.5 QUALITY CONFORMANCE INSPECTION

4.5.1 Drawing compliance. Each device shall be examined for compliance to the detail SCD.

4.5.2 Group A inspection. The Group A inspection specified on the detail SCD shall be performed in accordance with the following requirements.

4.5.2.1 Characteristics with 100 percent inspection required (critical characteristics). Characteristics with 100 percent inspection specified on the detail SCD shall be measured on 100 percent of the lot after completion of preconditioning and special conditioning. All devices shall meet the limits specified in the detail SCD.

4.5.2.2 Characteristics with a specified LTPD (major characteristics). Characteristics with a LTPD specified in the detail SCD may be sample inspected using the sampling procedures of Specification MIL-S-19500. The supplier, at his option, may use guard bands on other parameters, or at different temperatures, to guarantee that a specific parameter meets the LTPD specified in the detail SCD without actually testing at that level or at the specified conditions.

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4.5.3 Group B inspection. Group B inspection in accordance with Table I shall be defined as the environmental requirements of Specification MIL-S-19500. The testing in any subgroup shall be performed in the sequence listed. All devices shall be capable of withstanding the environmental requirements and meeting the electrical requirements of the applicable detail SCD after being exposed to the environments.

4.5.3.1 Solderability. This test shall be performed in accordance with MIL-STD-202C, Method 208A and shall include all solid and stranded wires up to 1/8 inch thickness, ribbon leads up to 0.050 inches in width and up to 0.025 inches in thickness, and lugs, taps, hook leads, turrets, etc, which are normally joined by a solder operation.

4.5.3.2 Lead pull (other than flat packages). Each lead shall withstand an axial pull of 4 lb minimum for 30 sec. The device shall meet the hermetic seal test after this test.

4.5.3.3 Lead pull (for flat packages only). Each lead shall withstand an axial pull of 12 ounces minimum for 30 sec. The device shall meet the hermetic seal test after this test.

4.5.3.4 Bending stress test (for other than flat packages). The device shall be placed in a vertical position and an 8±0.5 ounce weight shall be attached to the lead. The device shall be slowly rotated, in approximately 5 seconds to a horizontal position and then returned to the vertical position. The two succeeding bends shall be made in the same manner. The device shall meet the hermetic seal test after this test.

4.5.3.5 Bending stress test (for flat packages). The unit shall be held in a vertical position with a 2-ounce weight suspended from the lead to be tested. Two cycles of bending shall be performed, a cycle consisting of slowly moving the body of the unit 45° from the vertical in one direction and back 45° to the original position, taking approximately 5 seconds per direction. The device shall meet the hermetic seal test after this test.

4.5.3.6 Torque. Stud-mounted units shall withstand the torque specified in the detail SCD without resulting in the loss of the ability to turn a nut onto the stud using only finger pressure.

4.5.3.7 Nonoperating high temperature life. The devices shall be stored at the maximum rated temperature specified in the detail SCD for 1000 hours.

4.5.3.8 Operating life. Operation of the device shall be at the maximum rated power for 1000 hours. The burn-in conditions in the detail SCD may be used as the operating life conditions.

4.5.3.9 High temperature voltage stress. Operation of the device shall be at:

V_{CBO} = 70 percent (minimum) of the maximum rated voltage for transistors.

V_R = 70 percent (minimum) of the maximum rated voltage for diodes.

Ambient Temperature: +150°C minimum

Operation shall be for 96 hours minimum. Upon completion of the test time, the voltage shall be maintained until the devices have reached room ambient conditions. Parameters shall be measured within 8 hours after removal of the voltage.

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4.6 TEST SURVEILLANCE. A member or designated agent of the buyer may be assigned to the supplier's plant to perform a surveillance function in connection with products subject to this specification. This representative shall have the prerogative to observe all tests and the data showing the results of all tests performed as a requirement of this specification.

4.7 EXTENDED PERFORMANCE TESTS. Semiconductor devices may be subjected to environmental tests, which are within the specification requirements, to assure the buyer that the devices continue to meet the specification requirements. This testing will be performed by AC Electronics on a limited sampling basis. When the extended performance test detects a substandard lot, the disposition of that lot will be negotiated with the supplier.

4.8 NUCLEAR HARDNESS ASSURANCE TESTS. Nuclear hardness assurance tests shall be performed on a sample of the devices from each lot as specified in the applicable addendum and SCD. All devices shall meet the limits specified in the detail SCD after the nuclear hardness assurance tests.

5. PREPARATION FOR DELIVERY

5.1 GENERAL

5.1.1 Cleaning and drying. Prior to packaging, all items shall be free from contamination. The items shall be cleaned and dried with suitable materials and methods which will not damage the items. When a specific degree of cleanliness is specified in the detail requirements, the cushioning or wrap, and the bag or container interior, used for the unit packaging of the item, shall be as clean or cleaner than the degree of cleanliness specified for the item.

5.1.2 Physical protection of item. Cushioning materials or devices shall be used to protect the item from physical damage during handling and shipment. Cushioning or partitioning shall be provided, as applicable, to prevent free movement of the item or unit packages within an intermediate or shipping container. Shredded or unbounded cushioning materials shall not be used.

5.1.3 Unit container. The size of a rigid, semi-rigid, or nonrigid container shall be such that a minimum amount of clearance is allowed between the item and the container boundaries. When the container is in contact with the item, it shall be noncorrosive (pH 6.4 to 8.3), non-abrasive, and as dry as practicable.

5.1.4 Intermediate container. Items which are unit packaged by wrapping or by placement in a nonrigid container, shall be placed in a rigid container suitably cushioned or partitioned to prevent free movement of the unit packages during handling and shipment.

5.1.5 Shipping container

5.1.5.1 Packing. Items, unit packages, or intermediate packages shall be packed in shipping containers acceptable by common carrier, and in a manner which will assure safe delivery at destination. The method of packing and the assigned mode of shipment shall be such that the items shall not be damaged. Unless otherwise specified, or when impractical because of quantities being shipped, all items shipped in the same container shall be identical. Where possible, a shipment shall consist of parts from no more than one production lot.

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5.1.5.2 Enclosures. Any applicable technical data, such as special conditioning data, reports and instructions, shall be contained within the outer packing in separate envelopes or similar enclosures and properly secured to prevent free movement within the shipping container. If the bulk data is such that inclusion within the packing is impractical or impossible, the data shall be supplied under a separate cover which is securely attached to the shipping container by means of tape, tie, or adhesive. Special data peculiar to each unit may be included within each unit container.

5.1.6 Container marking. The markings on unit, intermediate, and shipping containers shall be located where they may be easily read when the packages are stacked or stored on shelves, and where they will not be destroyed when the package is opened for inspection or until the contents have been used. The following is a list of the information that shall be marked on unit, intermediate, and shipping containers. The information for d, e, and f, is required only when the markings are applicable to the container contents:

- a. The AC Electronics part number
- b. Item description
- c. Quantity in container
- d. Precautionary information as required to assure the safety of the items during handling or opening
- e. Identification of preservative or lubricant used, when applicable.
- f. Number of the lot, date code, batch, serial or other control number.

5.2 DETAIL PACKAGING REQUIREMENTS

5.2.1 Hand carry. When hand carrying or personal delivery is used to expedite delivery of items, the protection afforded the items shall be such that the items shall be acceptable at AC Electronics, but the detail packaging requirements of this specification need not apply.

5.2.2 Item packaging. The items may be packaged individually or in small groups. The unit container shall be a transparent plastic bag, or a capped rigid or a semirigid plastic container. A special container may also be used such as one designed to hold a specific number of items and which allows for resealing the container after removal of one or more items, or a multiple compartment container which allows for removal of any compartment without breaking the seal of an adjacent compartment. Items having leads or terminals shall be packaged

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in a manner that will prevent the leads or terminals from bending, receiving shock, and being used for removal. The following components shall be packaged in the manner described:

a. Axial lead: Package by any method shown in Figure 1 regardless of quantities involved. The preferred method is body taped and wound on reels or taped to paper strips.

b. Radial lead: Package by any method shown in Figure 2 regardless of quantities involved.

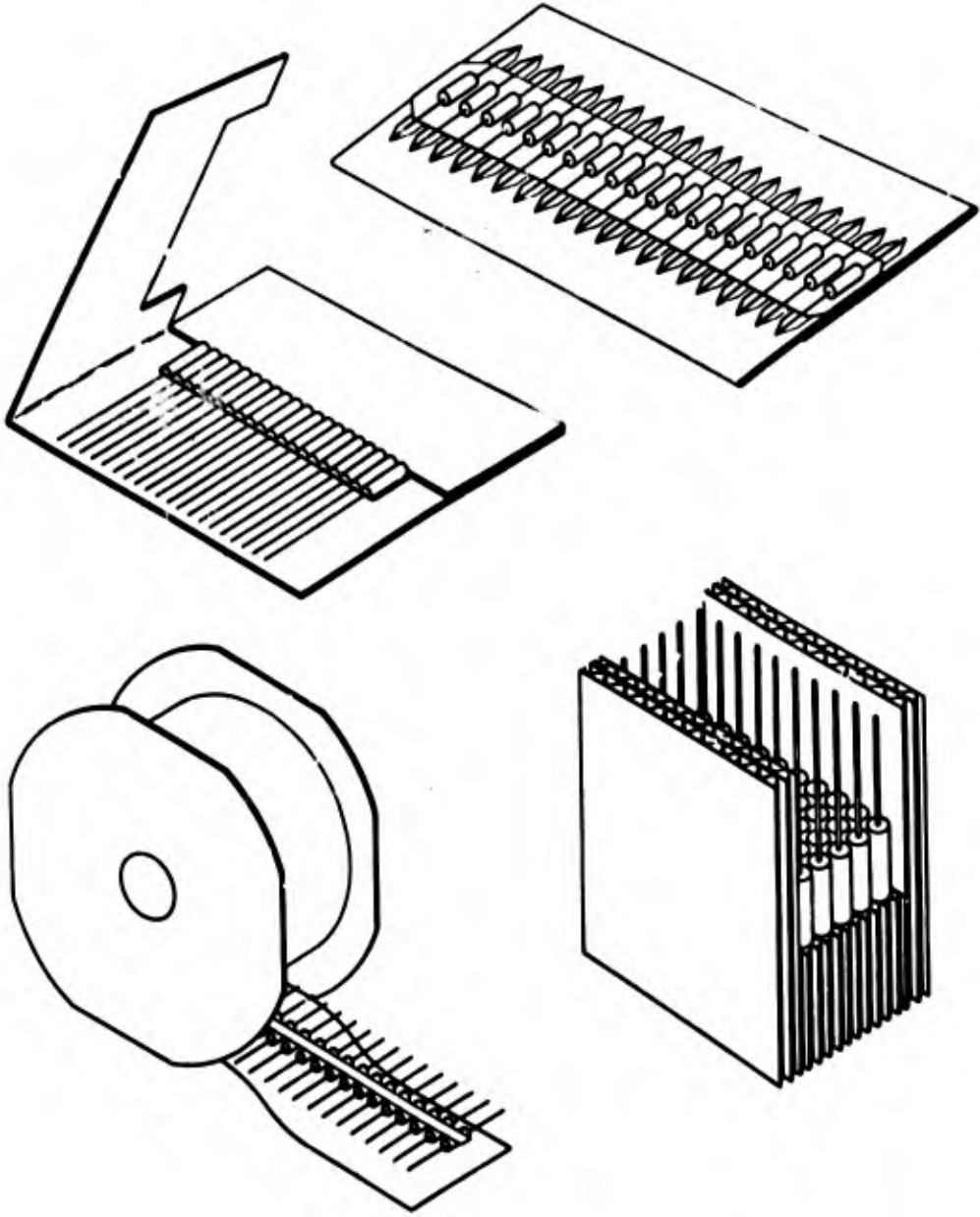
c. Integrated Circuits (Flat Packs):

(1) Less than 100: Package as shown in Figure 3 [Barnes 029 carrier (see 6.3) with chipboard or plastic container] or Figure 4 (Barnes 029 carrier with Barnes 029 magazine or Barnes 029 carrier with Motorola magazine, or equivalent magazine).

(2) 100 or more: Package as shown in Figure 4.

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PACKAGING METHODS FOR AXIAL LEAD COMPONENTS

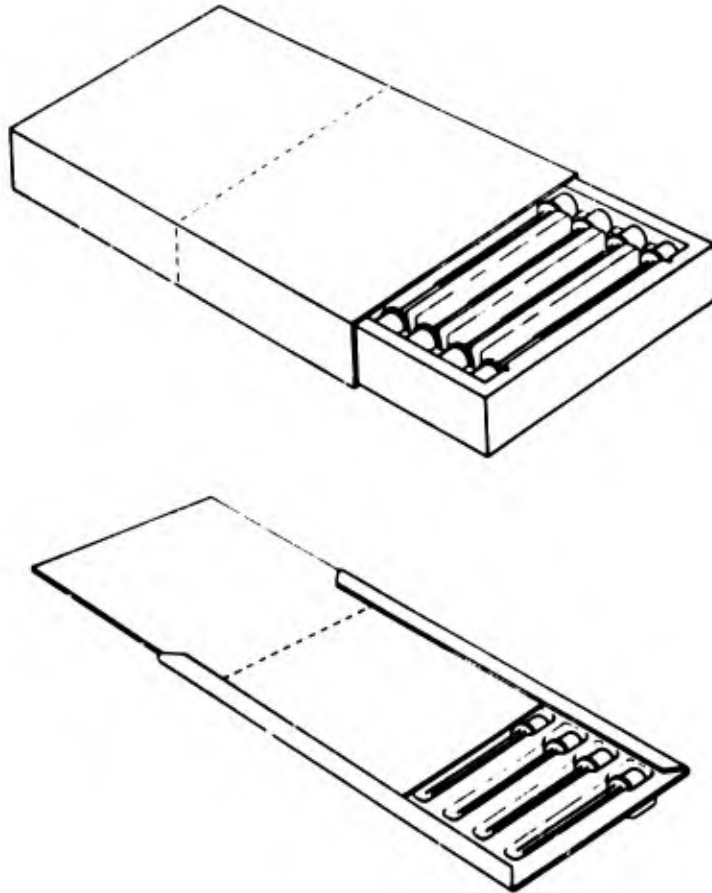
FIGURE 1

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PACKAGING METHODS FOR RADIAL LEAD COMPONENTS

FIGURE 2

AC ELECTRONICS DIVISION
GENERAL MOTORS CORPORATION
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CODE IDENT NO. 99974

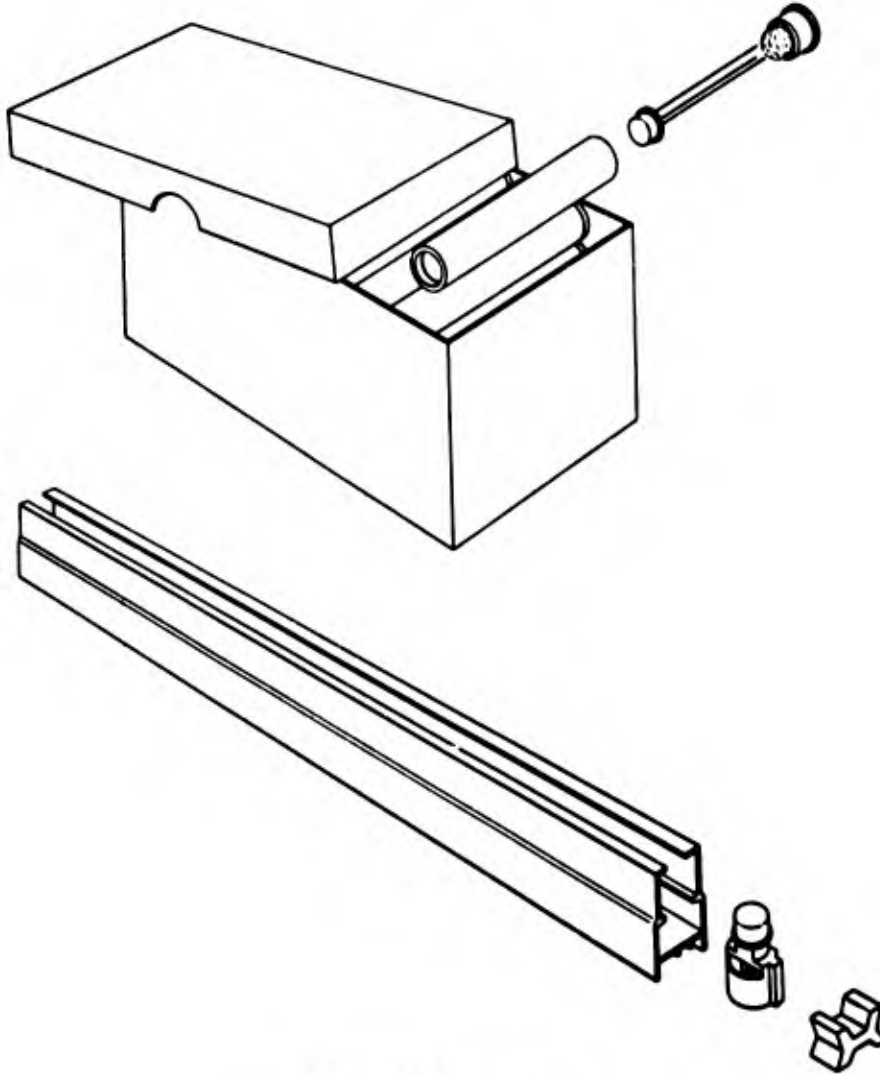


FIGURE 2 (Continued)

SPECIFICATION	
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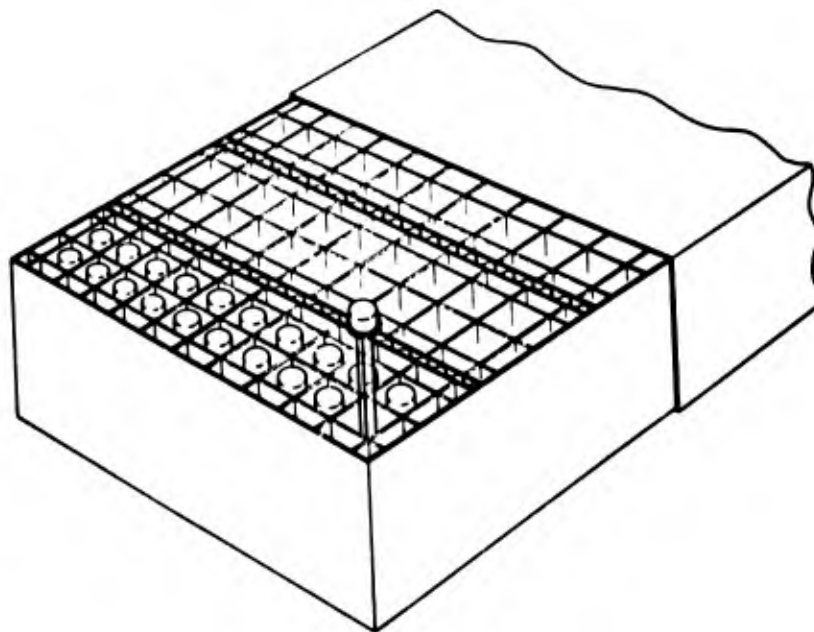
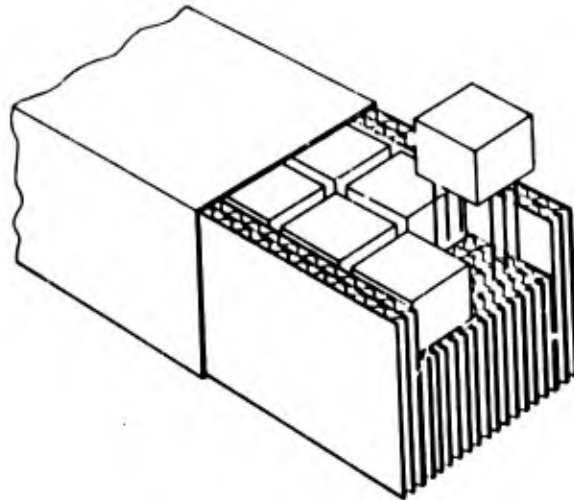
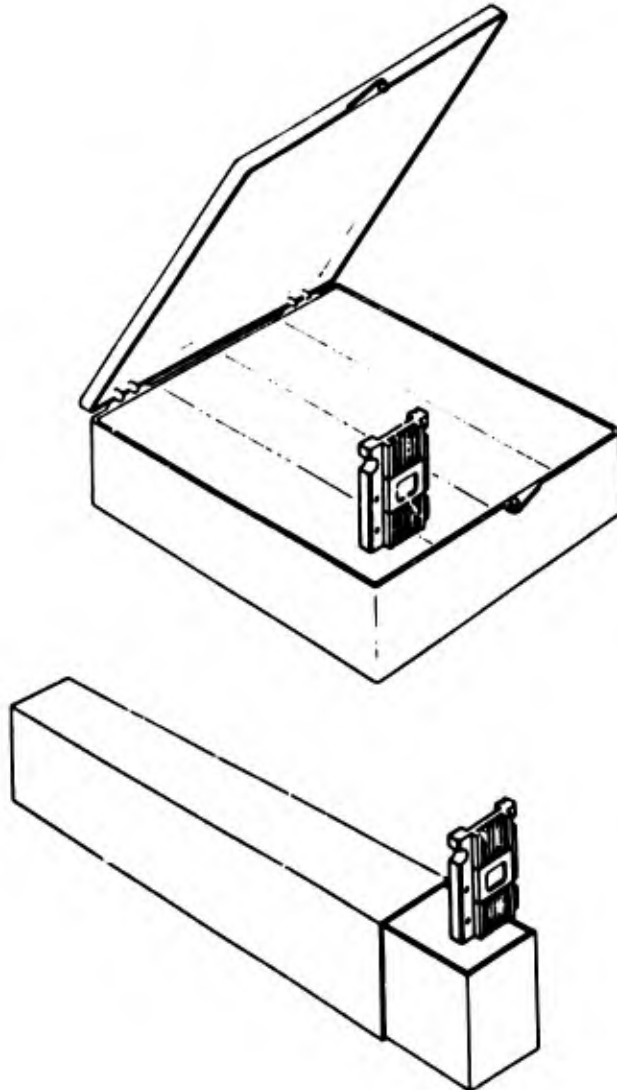


FIGURE 2 (Continued)

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CODE IDENT NO. 99974



PACKAGING METHODS FOR INTEGRATED CIRCUITS
(QUANTITIES LESS THAN 100)

FIGURE 3

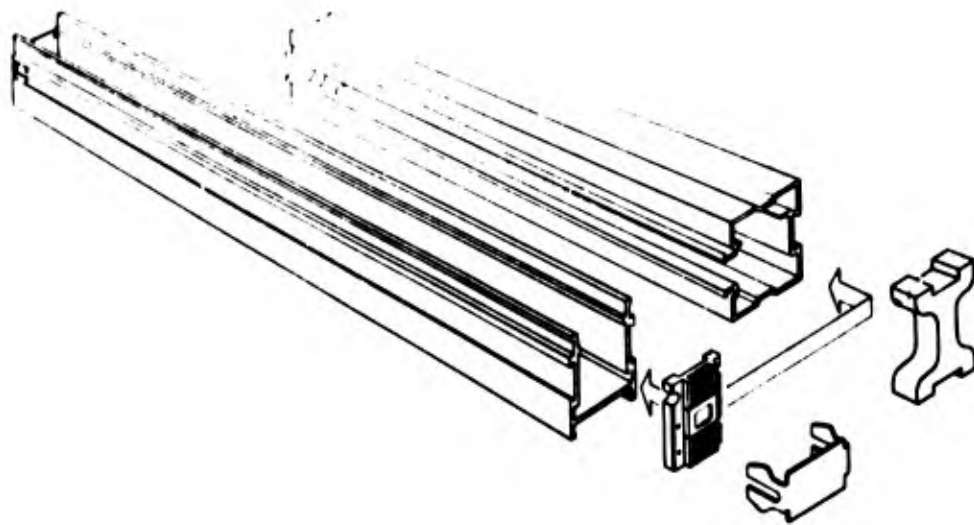
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FORM 1151

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PACKAGING METHODS FOR INTEGRATED CIRCUITS
(ANY QUANTITY)

FIGURE 4

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6. NOTES

6.1 APPROVAL OF CHANGES OR WAIVERS. The only personnel authorized to give suppliers approval of changes or waivers to any requirement of the applicable SCD or this specification are the buyer's purchasing representative.

6.2 DEFINITIONS

6.2.1 Buyer. Buyer, as used in this specification, shall mean AC Electronics Division, General Motors Corporation, Milwaukee, Wisconsin.

6.2.2 Supplier. Supplier, as used in this specification, shall mean an entity, e.g., a vendor or manufacturer, supplying a part subject to the requirements of this specification in accordance with a purchase order or contract issued by the buyer.

6.2.3 User. User, as used in this specification, shall mean an agent of the buyer that will incorporate, into an equipment, items furnished under this specification; this term does not describe a manufacturer, vendor, or supplier furnishing items in accordance with this specification.

6.2.4 Part or unit. Part or unit, as used in this specification, shall mean one piece, or two or more pieces joined together which are not normally subject to disassembly without destruction.

6.2.5 Detail Specification Control Drawing (SCD). As used in this specification, reference to a detail SCD shall mean a document or set of documents that describe an individual type of semiconductor device to be supplied in accordance with this specification.

6.2.6 "Shall be capable of". "Shall be capable of", as used in this specification, shall mean that the part must meet the applicable requirements to the LTPD of Specification MIL-S-19500, but the supplier does not have to run tests other than the preconditioning requirements and electrical measurements required by the applicable drawing or specification on each lot shipped to demonstrate they have met them. For example, the supplier may have adequate data from tests on devices from the same family which are the same generic type that demonstrate that the devices of that family do meet the applicable environmental requirements of Specification MIL-S-19500.

6.2.7 Unit package. A unit package is the first tie, wrap, or container applied to a single item or a multiple thereof, or a group of items of a single part number which involves a complete and identifiable package.

6.2.8 Intermediate package. An intermediate package is an interior container which contains two or more unit packages of identical items.

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6.2.9 Packing. Packing includes the insertion of unit or intermediate packages or un-packaged material into a shipping container and the application, when required, of bracing, blocking, cushioning, and waterproof barriers. Packing is completed with the final closure.

6.2.10 "Same generic type". "Same generic type", as used in this specification, shall mean semiconductor chips manufactured with the same manufacturing process, geometry polarity, and size. An exception, where the overall size of the chip is not applicable, is for multi-function integrated circuits, provided they have the same manufacturing process, geometries, and polarities.

6.2.11 Production lot. A production lot shall be the total quantity of units continuously produced by a manufacturing process known to be "in control" and having all manufacturing operations completed. The period of this production shall not exceed thirty calendar days. Any shipment containing more than one production lot shall be packaged and identified separately. The production lot shall be homogeneous and consist of the same process control specified in 3.2.

6.3 REQUIRED SOURCE. Required source for the integrated circuit carrier specified in 5.2.2 is Barnes Development Company, 213 W. Baltimore Pike, Landowne, Pa.

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SUMMARY SHEET

FOR
GENERAL SPECIFICATION
SEMICONDUCTOR DEVICES

TYPE OF CHANGE	PAGE NO.	PARA. NO.	CHANGE DESCRIPTION	AUTH	DATE
REV A	All	All	Specification completely revised and retyped.	ECO NO. <i>220512</i>	6 April 1967
REV B	All	All	Specification completely revised and retyped. Addendums I, II and III added for Categories 1, 2, and 3 respectively. Specification was 19 pages, is now 40 pages.	ECO NO. <i>ECM 232139</i>	28 March 1968
REV C	6	3.4	<u>BASIC SPECIFICATION</u> Revised	ECO NO. <i>235281</i>	11 Sept 1968
	3	3	<u>ADDENDUM I</u> Revised		
	8	3.4	<u>ADDENDUM II</u> Added		
	8	3.4	<u>ADDENDUM III</u> Revised		
REV D	2	1.2	<u>BASIC SPECIFICATION</u> Category 4 added	ECO NO. <i>237620</i>	10 March 1969
	2	2.1	Revised		
	4	3.1.1	Revised		
	5	3.4	Revised		
	6	Table I	Revised		
	10	5.2.2	Revised		
	12	6.2.11	Revised		
	12	6.3	Added		
	3	3.4	<u>ADDENDUM I</u> Revised		
	4	4.3.4	Revised		

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GENERAL SPECIFICATION
SEMICONDUCTOR DEVICES

TYPE OF CHANGE	PAGE NO.	PARA. NO.	CHANGE DESCRIPTION	AUTH	DATE
REV D (CONT'D)	2	1.1	<u>ADDENDUM II</u> Revised	237620	3-10 69
	7	3.2.1.12	Revised		
	8	3.8	Revised		
	9	4.3.5	Revised		
	2	1.1	<u>ADDENDUM III</u> Revised		
	7	3.2.1.12	Revised		
	8	3.4	Revised		
	9	4.3.5	Revised		
	11	4.3.7	Revised		
			<u>ADDENDUM IV</u> Added		

FORM 1152
REV. 6-61

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DATE 10 March 1960

ENGINEERING DEPT.	TOTAL NO. OF SHEETS 11	KEY	SPECIFICATION	
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ADDENDUM II
CATEGORY 2
SEMICONDUCTOR DEVICES

REFERENCE COPY

Subject to Change without Notice
No Parts to be Fabricated to this Print

Refer to General Specification, Page 1

REV*	ECO NO.*	DATE *	REV	ECO NO.	DATE

ORIGINAL ISSUE DATE: _____ *

RELEASE AUTHORITY: _____ *

CONTRACT: _____

APPROVALS	PRODUCT ENGINEERING	SPEC. ENG. <i>[Signature]</i>	1
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ADDENDUM II	SPECIFICATION	
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1. SCOPE

1.1 SCOPE. This addendum covers the requirements for semiconductor devices classified as Category 2. These semiconductor devices are to be used in high reliability systems such as aerospace, missiles and other critical applications.

2. APPLICABLE DOCUMENTS. Same as basic specification ST1000.

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3. REQUIREMENTS. The requirements for Category 2 semiconductor devices shall be as specified in basic Specification ST1000 and as specified herein.

3.1 GENERAL. Same as basic Specification ST1000.

3.2 PROCESS CONTROL. Any article furnished to this specification shall be constructed to the same design, using the same critical materials and processes as the first article supplied to this specification. Prior to fabrication of the first order, the supplier and buyer shall jointly review process, configuration, fabrication and material control documentation and agree on critical features based on the buyers application. After mutual agreement and determination of the adequacy of the supplier's control, the supplier shall make no changes or alteration in processes, design, and materials affecting these critical areas on articles to be purchased by the buyer, prior to written notification of the buyer. The supplier shall provide the buyer with the engineering reasons and sufficient details to permit evaluation of any proposed change of critical processes by submitting a supplier documentation change request shown in Figure 1. If a change is considered unacceptable by the buyer, he may cancel his order if the supplier cannot revert his production to the original configuration. Supplier change proposals, if any, are to be submitted in a timely manner while open purchase orders exist. During periods of procurement inactivity, description of changes shall be accumulated and submitted to the buyer upon placement of new purchase orders. The supplier shall assure that the design, manufacturing processes, materials, and sources of materials used by him and his lower tier suppliers are fully controlled by drawings or an equivalent system of documentation, and that articles to be furnished shall be fabricated in compliance with the documentation. The supplier shall permit the cognizant government agency, its designated representative or the purchaser to review the specified documentation without compromise of proprietary rights, and to observe the manner in which the documentation is implemented within the supplier's facilities. Process control shall be maintained so as not to compromise reliability or circuit performance. The critical materials and processes shall be defined as the information in the following paragraphs and this information shall be furnished to the buyer for each part number when applicable. The critical materials and processes shall be documented on the critical process and documentation list shown in Figure 2 and the critical process and documentation agreement shown in Figure 3. The buyers approval of critical materials and process documentation shall not constitute that the suppliers methods, procedures or design are adequate to meet the requirements of the procurement documents.

3.2.1 Critical material and processes. The following paragraphs are intended as a guide as to the type of critical materials and processes which could be included on the Critical Process and Documentation List.

3.2.1.1 Similar type designation and case size. Devices selected or screened from manufacturers basic type line. (Examples: EIA or JEDEC Type 2N930, 2N2605, 2N2945, 1N935, 1N3504A, or Manufacturers Type MHM2201, SE-124K, SN5400, μ a 709, etc.) (This information will aid qualifying similar devices manufactured on the same line.) The case type (examples: TO-18, TO-46, TO-5, TO-100, TO-89, DO-7, DO-9, 14 lead DIP, etc.)

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ADDENDUM II

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 PURCHASER'S CHANGE
 REQUEST NO.

SUPPLIER DOCUMENTATION CHANGE REQUEST
 FORM 3543 DEPT. 65-39

SUPPLIER		SUPPLIER REQUEST NO.	
PART NUMBER	REV. LETTER	DOCUMENT AFFECTED	REV. FROM TO
PERSON REQUESTING CHANGE		TELEPHONE NO.	EXT. NO. DATE OF REQUEST
DESCRIPTION OF CHANGE (NOTE: This form is not intended to be used to request changes to procurement drawings or specifications)			
THIS AREA TO BE COMPLETED BY SUPPLIER			
REASON FOR CHANGE			
EFFECT ON SELLING PRICE		EFFECT ON DELIVERY	
PROPOSED BREAK-IN POINT	LOT NO.	SERIAL NO.	DATE OTHER
<input type="checkbox"/> ACCEPTABLE	PURCHASING		DATE
<input type="checkbox"/> UNACCEPTABLE	ENGINEERING		DATE
<input type="checkbox"/> NON-INTERCHANGEABLE NEW PART NO. REQUIRED	RELIABILITY		DATE
G.A./SUPPLIER PRODUCTS			DATE
REMARKS			

SAMPLE FORM: SUPPLIER DOCUMENTATION CHANGE REQUEST

FIGURE 1

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3.2.1.2 Manufacturing process. Manufacturing processes involved. (Examples: Planar triple diffused, planar epitaxial, alloy, mesa, alloy base contact mesa, planar epitaxial double diffused with nichrome thin film resistors. Silicon dioxide dielectric isolation planar epitaxial quadruple diffused, etc.)

3.2.1.3 Overall dimensions and number of chips. For example; 1 chip 10 mils square and 5 mils thick, 1 chip 50 x 70 x 8 mils, 4 chips 20 x 30 x 5 mils connected as dual darlington, etc.

3.2.1.4 Geometry of chip. Geometry of junctions. A photomicrograph shall be furnished to indicate the geometry.

3.2.1.5 Gaseous backfill. Type of gaseous backfill used in capping devices (Examples: Dry nitrogen, dry air, helium, etc.)

3.2.1.6 Gold doped or electron bombarded. Information as to whether the devices are "Gold Doped" or "Electron Bombarded".

3.2.1.7 Metalization for contacts. Types of metalization used for contacts. (Examples: Aluminum, gold, etc.)

3.2.1.8 Die mount. The method used for mounting the chip to header (e.g. alloy bond, glass frit, etc.). The type of mounting material used if any.

3.2.1.9 Type of bond, wire diameter and wire material. Type of bond made to metalization along with the diameter and material of wire. (Examples: 5-mil gold wire ball-bonded, 10-mil aluminum wire ultrasonic bonded, spring pressure "S" whisker made of nickel, 0.5-mil aluminum wire sono-bonded, etc.)

3.2.1.10 Type of passivation. (Examples: silicon dioxide, borosilicate glass, varnish, etc.)

3.2.1.11 Basic material used. (Examples: N type silicon, P type silicon, P type germanium, etc.)

3.2.1.12 Hermetic seal test. (In-line) Type of hermetic seal tests used for gross leak and fine leak testing. (Examples: Gross leak; units backfilled with helium at 30 psi for 30 minutes, submerged in mineral oil at +100°C, examined under 40x magnification for evidence of bubbles. Fine leak: Radiflo leak test; units are backfilled with tracer gas at 100 psi for 3 hours prior to the fine leak test. Per MIL-STD-883, Method 1014, Test Conditions B and C; etc.)

3.2.1.13 Internal visual inspection. The supplier's internal visual inspection documents shall be reviewed and utilized wherever possible.

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3.2.1.14 100 percent preconditioning requirements. Description of the 100 percent preconditioning (4.3) as performed by the supplier.

3.2.1.15 100 percent special conditioning requirements. Description of the 100 percent special conditioning (4.4) as performed by the supplier.

3.3 COMPLIANCE DATA. The supplier shall keep on file for 3 years a copy of the data which was used to determine that the lot is capable of meeting the requirements of Specification MIL-S-19500. This data shall be from devices of the same generic type (see 6.2.10 of ST1000). However, the data need not be from the individual devices in the shipment.

3.4 LEAD AND TERMINAL MATERIALS. Leads and terminals of devices processed to this specification shall be solderable in accordance with the requirements of MIL-STD-750, Method 2026 and 4.5.3.1 of Basic Specification ST1000.

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4. QUALITY ASSURANCE PROVISIONS

4.1 GENERAL. Same as basic specification ST1000.

4.2 DUPLICATION OF TESTS. Same as basic specification ST1000.

4.3 100 PERCENT PRECONDITIONING REQUIREMENTS. The following preconditioning shall be performed on all devices in the order specified in Figure 4.

4.3.1 Internal visual inspection. All devices shall be subjected to internal visual inspection. The internal visual inspection procedure and acceptance criteria shall be negotiated and documented as a part of the critical process and documentation list (Reference 3.2.1 in this addendum). The supplier's internal visual inspection documents shall be reviewed and utilized whenever possible.

4.3.2 High temperature stabilization. All devices shall be stored at an ambient temperature of +150°C minimum for at least 24 hours, or +200°C for at least 16 hours.

4.3.3 Temperature cycling. All devices shall be subjected to temperature cycling in accordance with MIL-STD-750, Method 1051, Condition F, with the following exceptions and additions:

a. A minimum of ten cycles shall be performed.

b. After the device (devices less than 0.3 lbs) has stabilized to a temperature within the limits of the extreme to which it has been subjected, it shall have an additional exposure time of 10 minutes minimum.

4.3.4 Acceleration. All devices shall be subjected to a constant acceleration of 20,000g minimum in accordance with MIL-STD-883, Method 2001, Condition D. All devices other than cylindrical packaged, axial lead diodes shall be accelerated in the Y₁ direction. Cylindrical packaged axial lead diodes shall be accelerated in the X or Z direction. An alternate test is the high impact shock test of 25,000g minimum, with a pulse width of 15 to 30 microseconds.

4.3.4.1 Flat package acceleration. After the Y₁ axis acceleration all Flat Packages shall be accelerated in the X or Z axis in accordance with MIL-STD-883, Method 2001, Condition D or X-rayed in accordance with MIL-STD-883, Method 2012 in order to detect and reject all packages with loose chips. Copies of radiographs are not required.

NOTE: X or Z axis acceleration may not be advisable on some hybrid circuits due to lead dress, therefore X-ray would be required.

4.3.5 Hermetic seal. All devices other than glass cased diodes and devices with no cavity for this type leak detection, i.e., plastic or epoxy cased devices shall be subjected to the following seal tests. The maximum leakage rate shall be 10^{-8} atm-cc/sec:

a. Fine Leak - Per MIL-STD-883, Method 1014, Test Condition A or B.

b. Gross Leak - Per MIL-STD-883, Method 1014, Test Condition C.

c. Alternate Seal Tests

(1) Fine Leak - Per MIL-STD-202, Method 112, Test Condition C, Procedure I, II, III, or IV. Backfill pressure shall be 28 psig minimum.

(2) Gross Leak - Per MIL-STD-202, Method 112, Test Condition A or B

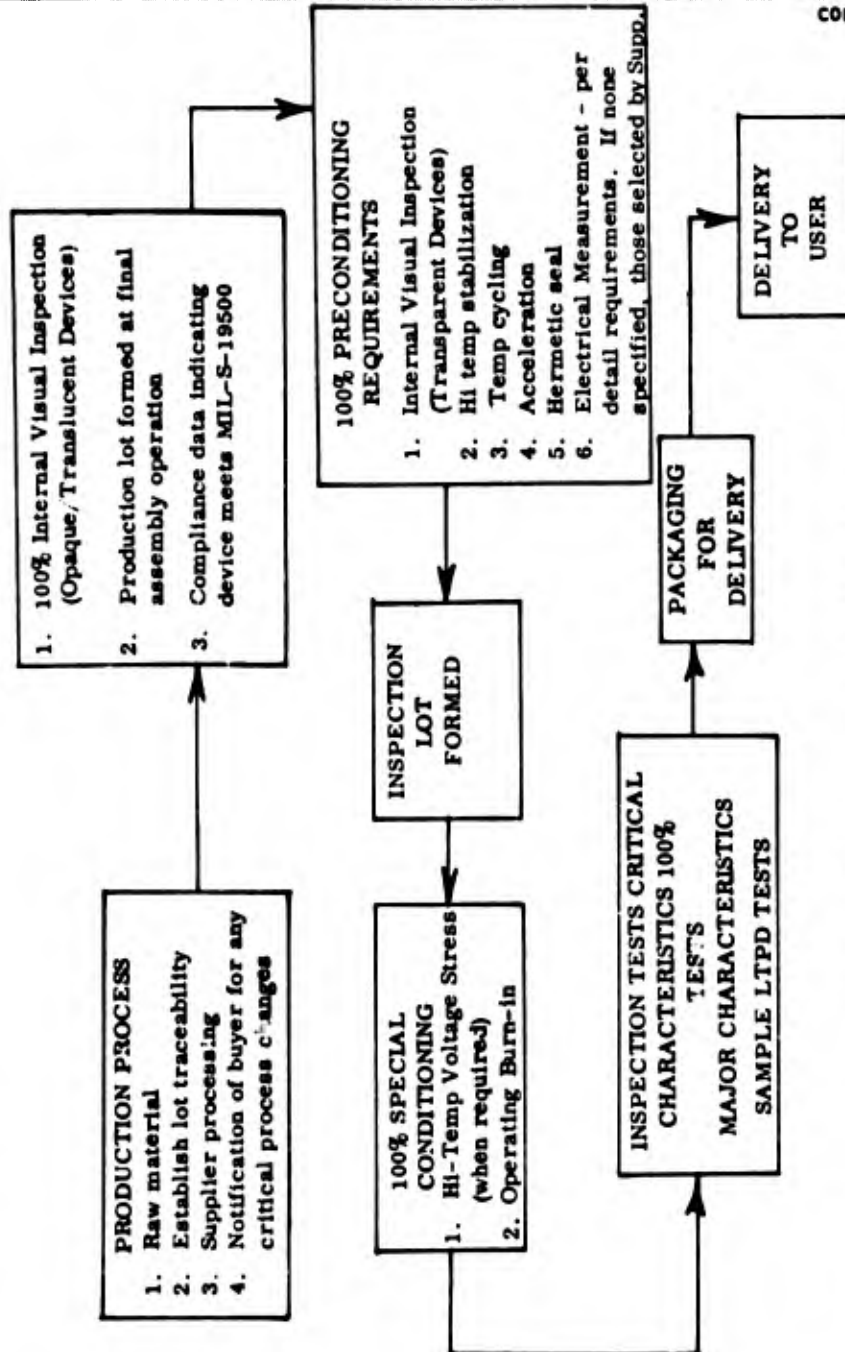
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ORDER OF PROCEDURE DIAGRAM (CATEGORY 2)
FIGURE 4

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4.3.6 Hermetic seal (glass cased diodes only). All diodes shall be subjected to a seal test to assure a leakage rate no greater than 10^{-8} atm-cc/sec. The test method shall be approved by the buyer.

4.3.7 Hermetic seal (devices with no cavity such as plastic or epoxy cased semiconductor). All devices shall be subjected to a seal test. The test method shall be approved by the buyer.

4.4 100 PERCENT SPECIAL CONDITIONING REQUIREMENTS. All devices shall be subjected to special conditioning as required on the individual SCD.

4.4.1 High temperature voltage stress. When required on the SCD, all devices shall be subjected to a high temperature, reverse voltage stress for 96 hours minimum under conditions specified on the SCD. After the devices have been subjected to the specified hours of stress, the voltage shall be maintained until devices have reached room ambient conditions. Parameters specified on the SCD shall be measured within eight hours after removal of voltage.

4.4.2 Burn-in. All devices shall be subjected to an operational burn-in for 168 hours minimum under the conditions specified on the SCD.

4.5 QUALITY CONFORMANCE INSPECTION. Same as basic specification ST1000.

4.6 TEST SURVEILLANCE. Same as basic specification ST1000.

4.7 EXTENDED PERFORMANCE TESTS. Same as basic specification ST1000.

4.8 NUCLEAR HARDNESS ASSURANCE TESTS. This paragraph not applicable.

5. PREPARATION FOR DELIVERY. Same as basic specification ST1000.

6. NOTES. Same as basic specification ST1000.

APPENDIX II
DETAILED TEST DATA
FROM
INCOMING INSPECTION AND EXTENDED PERFORMANCE TESTS

Incoming Inspection of Hybrid Microcircuits

MFG. CODE	RECEIVED/DATES	ELECTRICAL FAILURES AT +25°C (NO. FAIL/NO. TESTED)	DC ELECTRICAL FAILURES AT +125°C (NO. FAIL/NO. TESTED)	FINE SEAL FAILURES	GROSS SEAL FAILURES	EQUIVALENT YIELD %
Memory Hybrid Switch						
(A)	6700/.68	155/6487 = 2.39%	7/1553 = 0.45%	61/2589 = 2.36%	433/5406 = 8.01%	82.28
(G)	5014/.68	452/5013 = 9.02%	8/2498 = 0.32%	18/1272 = 1.42%	36/1894 = 1.90%	87.70
(H)	2857/.67	115/2857 = 4.02%	-	29/539 = 5.4%	25/539 = 4.8%	86.44
(B)	16230/.67	489/16224 = 3.01%	6/1250 = 0.48%	-	16/564 = 2.84%	93.78
Totals	30,801/.67	1211/30,581 = 3.96%	21/5301 = 0.40%	108/4400 = 2.45%	510/8403 = 6.07%	87.65
Dual Ladder Switch and Driver						
(B)	401/.67	5/401 = 1.25%	-	-	-	98.75
Sixteen-Diode Array						
(D)	478/.68	2/478 = 0.42%	7/447 = 1.57%	-	-	98.01
(I)	13,201/.68	122/12906 = 0.94%	7/6160 = 0.11%	6/1754 = 0.34%	144/6385 = 2.26%	96.30
Totals	13,679	124/13,384 = 0.93%	14/6607 = 0.22%	6/1754 = 0.34%	144/6385 = 2.26%	96.29

Incoming Inspection of Hybrid Microcircuits

MFG. CODE	NO. OF PARTS RECEIVED/DATES	ELECTRICAL FAILURES AT +25°C (NO. FAIL./NO. TESTED)	DC ELECTRICAL FAILURES AT +125°C (NO. FAIL./NO. TESTED)	FINE SEAL FAILURES NO. FAIL./NO TESTED	GROSS SEAL FAILURES NO. FAIL./NO. TESTED	EQUIVALENT YIELD %
Ladder Switch and Driver						
(D)	17035/.68	215/3481 = 6.18%	0/22 = 0%	5/269 = 1.86%	70/490 = 14.3%	78.91
(A)	445/.69	1/429 = 0.23%	1/62 = 1.61%	-	28/443 = 6.32%	91.96
(B)	53,221/.67 .68 .69	602/48,748 = 1.23%	-	30/1619 = 1.85%	371/17,593 = 2.11%	94.90
Totals	70,701/.67 .68 .69	818/52,658 = 1.55%	1/84 = 1.19%	35/1,888 = 1.85%	469/18,526 = 2.53%	93.06
Dual Analog Gate						
(E)	1697/.68 .69	55/1,464 = 3.76%	14/1,353 = 1.03%	0/27 = 0%	24/1,018 = 2.36%	93.00
(J)	7,553/.67 .68 .69	210/5,399 = 3.89%	583/4,831 = 12.07%	15/249 = 6.02%	114/3,383 = 3.37%	76.74
Totals	9,250/.67 .68 .69	265/6,863 = 3.86%	597/6,184 = 9.65%	15/276 = 5.43%	138/4,401 = 3.14%	79.56
Grand Totals	124,832/.67 .68 .69	2,423/103,887 = 2.33%	633/18176 = 3.48%	164/6,318 = 1.97%	1,261/37,715 = 3.34%	89.33

Hybrid Microcircuit EPT Summary, Lots in Which a Sample was Pulled for EPT
Dual Analog Gate

MFG. CODE	NO. OF LOTS	LOT SIZE RANGE	TOTAL POP. (Σ OF ALL LOTS)	EPT SAMPLE SIZE RANGE PER LOT	TOTAL EPT QUANTITY (Σ OF ALL LOTS)	NO. OF LOTS ACCEPTED	FAILURES
(E) Mfg. during 1968, 1969	13	7-82	425	1-9	52	5 38%	1 fails fine seal only 2 fail gross seal only 1 fail both fine & gross seal 1 fail gross seal & electrical 2 fail electrical - cause unresolved <u>7 TOTAL FAILURES 7/52 ≈ 13%</u> 2 internal visual rejects - scratched metalization and poor wire dress. Units pass electrical test 2/52 ≈ 3.8%
(J) (Old Package)	43	5-250	2731	1-22	269	36 84%	6 fail fine seal only 3 fail gross seal only 3 fail both fine & gross seal <u>12 TOTAL FAILURES 12/269 ≈ 4.5%</u> 1 visual reject - FET chip has spot on oxide and metal 1 visual reject - damaged internal lead 1 visual reject - chip diced with an extra half chip on it creating a shorting hazard 1 visual reject - scratched metalization 1 visual reject - diffusion fault 4 visual rejects - drooped lead-shorting hazard <u>9 INTERNAL VISUAL REJECTS - UNITS PASSED ELECTRICAL TESTS 9/269 ≈ 3.3%</u>
Mfg. during 1967, 1968							

Hybrid Microcircuit EPT Summary, Lots in Which a Sample was Pulled for EPT

Dual Analog Gate

MFG. CODE	NO. OF LOTS	LOT SIZE RANGE	TOTAL POP. (Σ OF ALL LOTS)	EPT SAMPLE SIZE RANGE PER LOT	TOTAL EPT QUANTITY (Σ OF ALL LOTS)	NO. OF LOTS ACCEPTED	FAILURES
(J) (New Package) MFR. during 1968, 1969	3	16-520	1710	5-20	115	4 50%	3 fail Gross seal only 1 fail both fine & gross seal 4 TOTAL FAILURES 4 / 115 ≈ 3.5% 4 VISUAL REJECTS - Drooped lead - Shorting Hazard 1 VISUAL REJECT - Chip poorly attached 2 EXTERNAL VISUAL REJECT - Misaligned Covers 2 VISUAL REJECTS - ELECTRICAL PASS 2 / 115 ≈ 1.7%

**Hybrid Microcircuit EPT Summary, Lots in Which a Sample was Pulled for EPT
Memory Hybrid Switch**

MFG. CODE	NO. OF LOTS	LOT SIZE RANGE	TOTAL POP. (Σ OF ALL LOTS)	EPT SAMPLE SIZE RANGE PER LOT	TOTAL EPT QUANTITY (Σ OF ALL LOTS)	NO. OF LOTS ACCEPTED	FAILURES
(A) Mfg. during 1968, 1969	6	186-1186	3,262	18-20	118	0 0%	5 fail fine seal only 8 fail gross seal only 11 fail both fine & gross seal <u>24 TOTAL FAILURES</u> 24 118 ≈ 20%
(G) Mfg. during 1968	18	18-524	3,377	3-22	241	7 39%	23 fail fine seal only 25 fail gross seal only 1 fail both fine & gross seal 1 fail leakage current 1 open bond <u>51 TOTAL FAILURES</u> 51 241 ≈ 21%
(H) Mfg. during 1967, 1968	18	10-354	2,158	3-24	204	2 11%	4 fail fine seal only 41 fail gross seal only 9 fail both fine & gross seal 19 loose ceramic substrate 4 loose bond 1 cover fell off 1 unit failed external lead pull 1 unit large Δ bond (Intermetallics) 1 fail gross seal & loose ceramic sub. 1 cracked chip <u>37 TOTAL FAILURES</u> 37 204 ≈ 18%
(B) Mfg. during 1967, 1968, 1969	28	3-1475	11,239	1-22	370	26 30%	6 fail gross seal only 1 fail both fine & gross seal <u>7 TOTAL FAILURES</u> 7 370 ≈ 2%

Hybrid Microcircuit EPT Summary, Lots in Which a Sample was Pulled for EPT

Ladder Switch and Driver

MFG. CODE	NO. OF LOTS	LOT SIZE RANGE	TOTAL POP. (OF ALL LOTS)	EPT SAMPLE SIZE RANGE PER LOT	TOTAL EPT QUANTITY (OF ALL LOTS)	NO. OF LOTS ACCEPTED	FAILURES
(D)	1	20-1440	3727	9-22	155	3	4 fail gross seal only 2 fail both fine and gross seal 1 external lead fell off 2 internal bond failures 17 TOTAL FAILURES 17 155 ≈ 111 4 external lead damaged (worn down from supplier rework) 2 weak gold ball bond. Pulled off at less than 1 gram 4 internal visual rejects-slipped gold ball bonds 1 internal visual reject-transistor almost shorted 6 internal visual reject thick film resistors instead of approved thin film. 17 VISUAL REJECTS (Did not fail electrical tests)
(A) Mfg. during 1968 (B)	1	29	29	3	3	1	1 Internal Visual-Loose Gold wire in package 1 3 ≈ 33%
(B) Old Package Mfg. during 1967	32	2-325	4972	1-22	371	12	1 Pails fine seal only 2 Pail gross seal only 4 Pail both fine and gross seal 2 Loose chip 1 Loose bond 1 Pail electrical-suspect resistive bond 17 TOTAL FAILURES 17 371 ≈ 4.5%

Hybrid Microcircuit EPT Summary, Lots in Which a Sample was Pulled for EPT
Ladder Switch and Driver

MFG. CODE	NO. OF LOTS	LOT SIZE RANGE	TOTAL POP. (Σ OF ALL LOTS)	EPT SAMPLE SIZE RANGE PER LOT	TOTAL EPT QUANTITY (Σ OF ALL LOTS)	NO. OF LOTS ACCEPTED	FAILURES
(B) New Package	50	4-2264	18,222	1-22	803	40 803	2 Fail fine seal only 22 fail gross seal only 1 fail both fine and gross seal 1 electrical open due to scratched al metalization 3 loose bond 1 open thin film resistor 30 FAILURES 30/803 ≈ 3.7% 5 metallic chips in package (Internal visual) 11 scratched aluminum metalization (Internal Visual) 4 Crack in chip toward junction or into metalization (Internal Visual) 1 diffusion flaw in chip (Internal Visual) 1 Resistor deposition flaw (Internal Visual) 1 Four external leads necked down (Worn) - (visual) 6 bonds ball bonded 2nd time over first bond on resistor chip. Lead pull greater than 3 grams (Internal Visual) 3 Contamination on resistor chip (Internal Visual) 2 Corrosion on aluminum metalization (Visual) 34 VISUAL REJECTS (DID not fail electrical tests) 34/803 ≈ 4.2%

Hybrid Microcircuit EPT Summary, Lots in Which a Sample was Pulled for EPT

MFG. CODE	NO. OF LOTS	LOT SIZE RANGE	TOTAL POPULATION (K-ALL LOTS)	EPT SAMPLE SIZE RANGE PER LOT	TOTAL EPT QUANTITY (K-ALL LOTS)	NO. OF LOTS ACCEPTED	FAILURES
Sixteen-Diode Array							
(I)	22	2-1496	11,264	1-22	364	13	<ul style="list-style-type: none"> 2 Fail fine seal only 4 Fail gross seal only 3 Fail both fine & gross seal 1 Internal bond off 1 Internal electrical test - Unresolved 11 Total failures 11/384 \approx 2.9%
Manufactured in 1968, 1969						0%	<ul style="list-style-type: none"> 2 Internal visual reject - drooped leads 3 Internal visual reject - chip into guard ring 1 Internal visual reject - marginal bond pulled off @ 1.5 gram 7 Internal Visual Reject - poor bonding 13 Internal visual rejects - Pass electrical tests 13/384 \approx 3.4%
Sixteen-Diode Array - Early Design							
(D)	8	16-130	500	3-13	52	2	<ul style="list-style-type: none"> 3 Fail fine seal only 2 fail gross seal only 19 shorted after Y₂ axis acceleration @ 20,000 G 1 bond open 25 Total failures 25/52 \approx 48%
Manufactured in 1967						12	<ul style="list-style-type: none"> 52 internal visual reject - Units have unacceptable design. Danger of leads shorting to common anode and common cathode side.
(I)	15	19-462	2917	3-22	331	8%	<ul style="list-style-type: none"> 11 fail reverse current & breakdown voltage after V-T stress (reverse bias life) 1 bond off 12 Total failures 12/231 \approx 5.2%
Manufactured by 1968, 1967							

Hybrid Microcircuit EPT Summary, Lots in Which a Sample was Pulled for EPT

Source Switch Gate

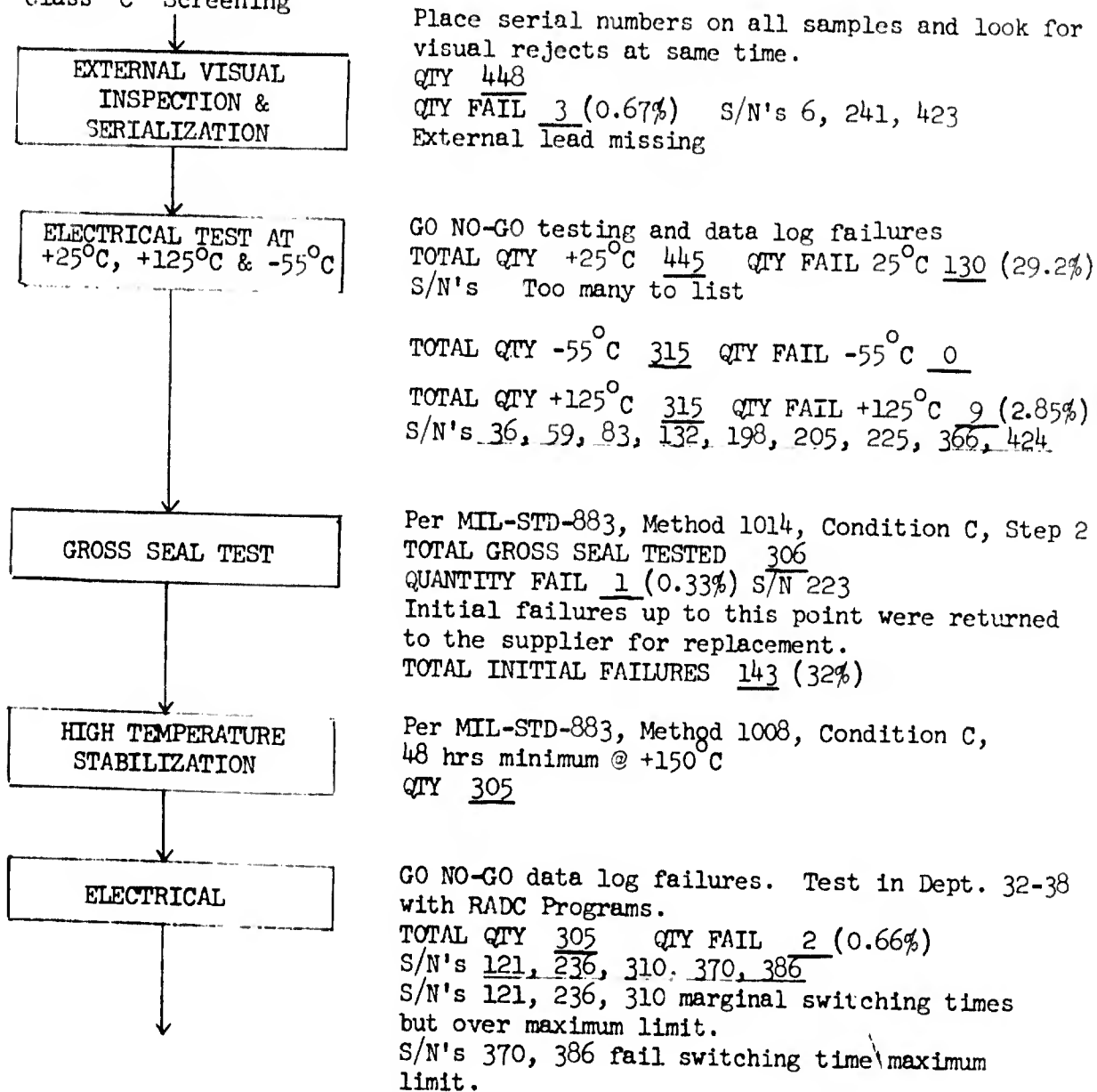
MFG. CODE	NO. OF LOTS	LOT SIZE RANGE	TOTAL POPULATION (Σ-ALL LOTS)	EPT SAMPLE SIZE RANGE PER LOT	TOTAL EPT QUANTITY (Σ-OF ALL LOTS)	NO. OF LOTS ACCEPTED	FAILURES
(D)	5	25-75	281	3-7	27	4	1 Fails fine seal only 1 Fails gross seal only 1 Fails both fine & gross seal 3 Total failures 3/27 ≈ 11%
Manufactured in 1967						80%	1 Visual reject - gold flake in unit 1 visual reject - one gold ball bond on top of another 2 Visual rejects 2/27 ≈ 7.4%
(H)	5	5-80	237	1-8	23	4	1 Ceramic substrate loose 1/23 ≈ 4.3%
Manufactured in 1967, 1968						80%	
Dual Ladder Switch and Driver							
(B)	10	17-58	326	3-6	39	7	3 Fail gross seal only 2 Fail both fine & gross seal 5 Total 5/39 ≈ 13%
Manufactured during 1967, 1968						70%	
Eight-Diode Array							
(D)	2	50-64	114	5-6	11	2	
Manufactured during 1967						100%	
Eight-Diode Array							
(D)	3	18-101	149	3-10	16	1	1 Fails fine seal only 2 Fail Gross seal only 1 Cover fell off 4 Total failures 4/16 ≈ 25%
Manufactured during 1967						33%	

APPENDIX III
DETAILED TEST DATA
FROM
VERIFICATION PHASE SCREENING TESTS

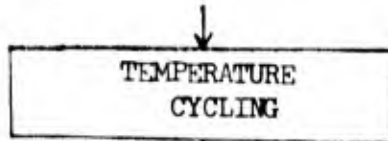
VERIFICATION PHASE TESTING
 FOR HYBRID CIRCUITS CONTRACT
 WITH RADC PER MIL-STD-883, METHOD 5004

TEST GROUP NUMBER: 1 PART TYPE: MEMORY HYBRID SWITCH
 SUPPLIER: A
 QUANTITY: 448 S/N: 1 → 448
 RECEIVED: MARCH 1970 DATE CODE: 7008

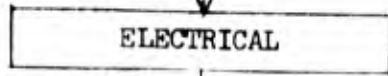
Class "C" Screening



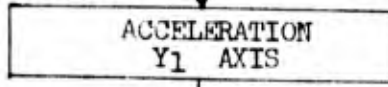
TEST GROUP NO. 1



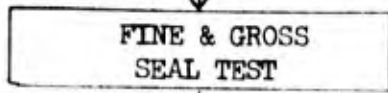
Per MIL-STD-883, Method 1010, Condition C,
10 cycles, -65°C to +150°C.
Transfer time less than 1 minute.
QTY 305



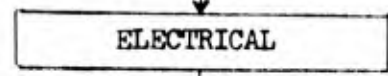
GO NO-GO data log failures
TOTAL QTY 305 TOTAL QTY FAIL 2
QTY NEW FAIL 0
S/N's 370*, 386*



Per MIL-STD-883, Method 2001, 30,000 G
QTY 305



Per MIL-STD-883, Method 1014, Condition A and
Condition C, Step 2. GO NO-GO fine leak rate
limit 1×10^{-7} ATM cc/sec.
TOTAL QTY SEAL TESTED 305
QTY FAIL FINE 7 (2.3%)
S/N's 38, 45, 46, 110, 278, 281, 313
QTY FAIL GROSS 6 (1.98%)
S/N's 38, 45, 46, 110, 281, 313
S/N 110 removed from test. Exploded in Gross Seal.



Data log all units.
TOTAL QTY 304 TOTAL QTY FAIL 8
QTY NEW FAILURES 3 (1.01%)
S/N's 38, 121*, 175, 236*, 310*, 319, 370*, 386*
S/N's 38, 133, 175, 319 removed from test.
S/N 38 loose ceramic substrate
S/N 133 could not confirm failure. Part OK.
S/N 175 external lead off. Another lead badly
twisted.
S/N 319 loose gold ball bond to aluminum metal-
ization on transistor

End of Class "C" screening procedures per MIL-STD-883, Method 5004.

$$\text{Total fallout } \frac{154}{448} = 34.4\%$$

$$\text{Fallout without initial failures } = \frac{11}{305} = 3.6\%$$

*Failed earlier test.

TEST GROUP NO. 1

Beginning of Class "B" Screening per MIL-STD-883, Method 5004

BURN-IN
 $T_A = +125^\circ C$
 168 HRS

Per MIL-STD-883, Method 1015, Condition D
 QTY 300

ELECTRICAL

Data log all units. TOTAL QTY 299
 TOTAL QTY FAIL 8 QTY NEW FAILURES 3 (1.02%)
 S/N's 121*, 201, 236*, 255, 310*, 349, 370*, 386*
 S/N 349 removed from test.
 S/N 201 diode reverse current increased over maximum limit.
 S/N 255 circuit leakage current increased over maximum limit.
 S/N 349 transistor Q_2 collector-emitter short.

End of Class "B" Processing

Total fallout to obtain Class B processed parts $\frac{157}{448} = 35\%$

Total fallout excluding initial failures $\frac{14}{305} = 4.6\%$

Beginning of Class "A" Processing per MIL-STD-883, Method 5004

THERMAL SHOCK

Liquid to liquid TOTAL QTY 299
 Per MIL-STD-883, Method 1011, Cond. C,
 15 cycles, $-65^\circ C$ to $+150^\circ C$
 S/N 310* Pin 8 missing
 386* Pin 14 missing

ELECTRICAL

GO NO - GO data log fails
 TOTAL QTY 299
 QTY FAIL 2
 S/N's 201*, 370*

MECHANICAL SHOCK

Per MIL-STD-883, Method 2002, Cond. F,
 Y₁ Axis, One Shock, 20,000 G Peak
 TOTAL QTY 297
 QTY DAMAGED 25 (8.42%)
 S/N's 9, 35, 43, 74, 95, 113, 119, 156, 214, 218,
240, 254, 285, 303, 314, 317, 336, 343, 348, 351,
364, 388, 408, 439, 446
 Failures removed from test.

TEST GROUP NO. 1

ELECTRICAL

GO NO-GO Data Log Fails
TOTAL QTY 272 TOTAL QTY FAIL 27
QTY NEW FAILURES 24 (8.93%)
S/N's 55, 78, 96, 108, 121*, 126, 154, 176, 201*,
217, 222, 230, 231, 232, 245, 252, 258, 267, 279,
291, 293, 323, 338, 355, 370*, 426, 432
S/N's 55, 78, 96, 108, 126, 154, 176, 217, 222,
230, 231, 245, 252, 258, 267, 279, 291, 293, 323,
338, 355, 426, 432 removed from test.
S/N's 55, 231, 291, 338 ceramic substrate broke in
two and one piece loose.
S/N's 96, 323 loose ceramic substrate.
S/N's 78, 108, 154, 267, 279, 432 loose Au wedge
bond to thick film conductor on substrate.
S/N's 126, 252 loose transistor chip.
S/N's 176, 217, 222, 230, 245, 252, 258, 293, 355,
426 loose Au ball bond to semiconductor chip.
S/N 232 switching time over maximum limit.

ACCELERATION
Y₂ AXIS

Per MIL-STD-883, Method 2001, 30,000 G Y₂ Axis,
Cond. E
TOTAL QTY 249
S/N's 138, 237 cover off when removed from carrier
S/N 49 cover off after acceleration. Parts re-
moved from test.

ELECTRICAL

GO NO-GO Data Log Fails
TOTAL QTY 246 TOTAL QTY FAIL 6
QTY NEW FAILURES 5 (2.06%)
S/N's 142, 210, 249, 327, 370*, 448
S/N's 142, 210, 249, 327, 448 removed from test
S/N's 142, 210, 448 lead from Pin 12 drooping
down and shorting to thick film conductor going
to Base of Q₂.
S/N 249 Pin 13 lead wire bonded in wrong place to
thick film conductor causing lead to short to
Pin 12.
S/N 327 loose ceramic substrate.

BURN-IN
T_A = +125°C
72 HOURS

Operating Life with Loads per MIL-STD-883,
Method 1015, Cond. D
TOTAL QTY 241

TEST GROUP NO. 1

ELECTRICAL

Data Log

TOTAL QTY 239 TOTAL QTY FAIL 4
QTY NEW FAILURES 0
S/N's 201*, 236*, 292*, 370*
* S/N 292 has a broken package

REVERSE BIAS
BURN-IN

72 Hours @ +125°C per MIL-STD-883, Method 1015,
Condition A
TOTAL QTY 238

ELECTRICAL

Data Log @ 25°C
TOTAL QTY +25°C 238 TOTAL QTY FAIL 6
QTY NEW FAIL 4 (1.7%)
S/N's 88, 121*, 131, 283, 363, 370*
S/N's 88, 283 circuit leakage current over the
maximum limit.
S/N's 121, 370 switching time over the maximum
limit.
S/N's 131, 363 diode reverse current over
maximum limit.

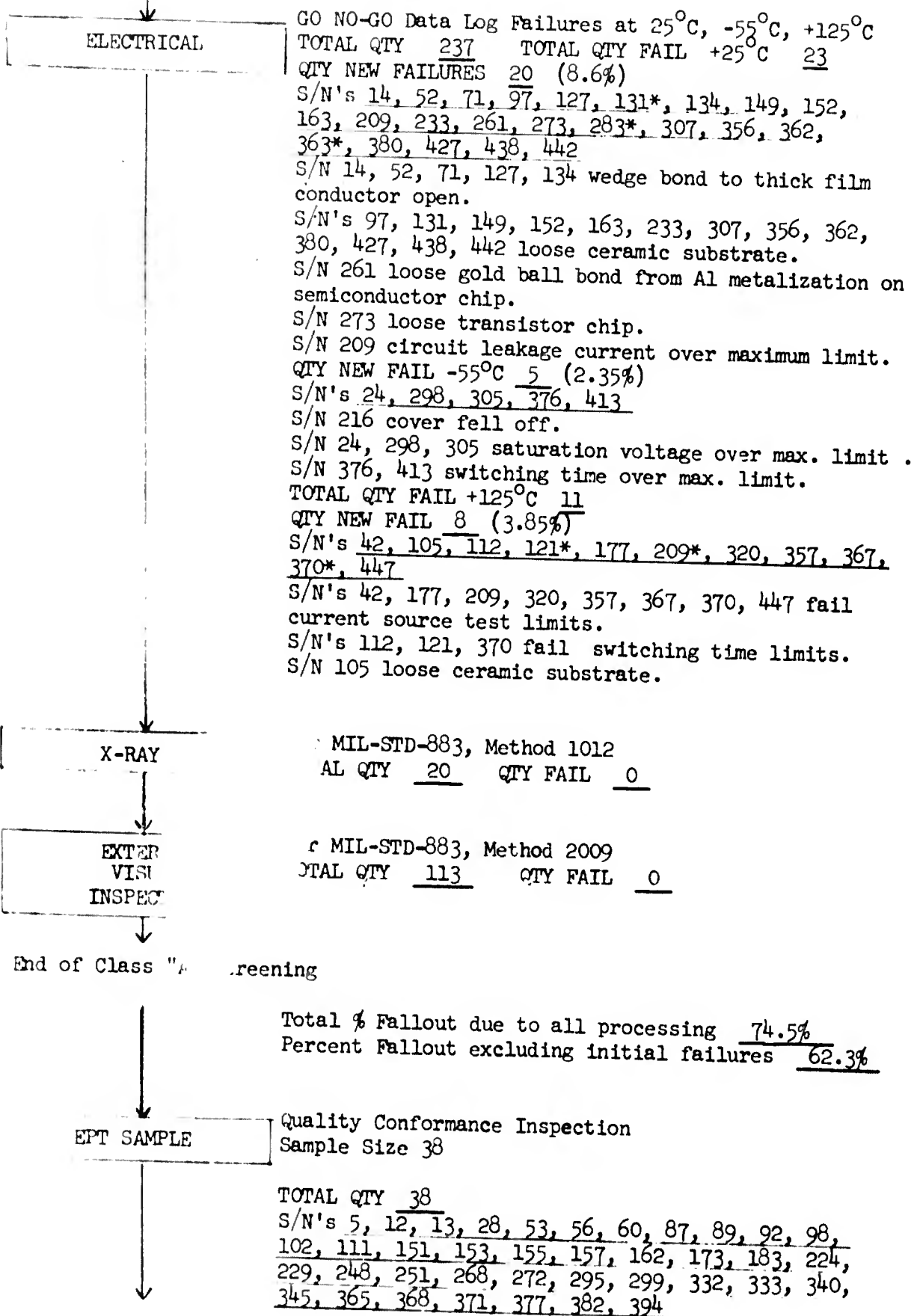
ACCELERATION
Y1 AXIS

Per MIL-STD-883, Method 2001, 40,000 G, Y₁ Axis
TOTAL QTY 237
S/N 346 cover off when removed from carrier.

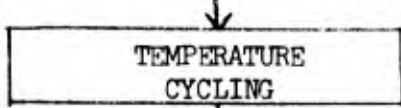
FINE & GROSS
SEAL TEST

Per MIL-STD-883, Method 1014, Cond. A and
Cond. C, Step 2
TOTAL QTY FINE 237 TOTAL QTY FAIL 11
QTY NEW FAILURES 10 (4.24%)
S/N's 46*, 62, 120, 127, 220, 244, 255, 273, 326,
335, 367
TOTAL QTY GROSS 237 TOTAL QTY FAIL 104
QTY NEW FAILURES 100 (42.4%)
S/N's 17, 20, 22, 24, 25, 27, 30, 42, 45*, 46*,
57, 58, 62, 66, 75
S/N's 76, 78, 91, 97, 109, 112, 120, 121, 123, 127,
128, 131, 144, 148, 152, 165, 169, 171, 172, 174,
179, 180, 182, 186, 191, 201, 209, 211, 213, 215,
216, 220, 233, 236, 238, 243, 244, 250, 253, 257,
259, 262, 266, 273, 278, 281*, 284, 286, 287,
288, 297, 298, 302, 305, 306, 312, 313*, 315, 316,
320, 321, 322, 324, 326, 328, 331, 335, 339, 344,
357, 367, 376, 378, 380, 383, 391, 392, 393, 395,
397, 411, 412, 414, 427, 429, 438, 442, 443, 444

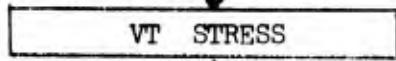
TEST GROUP NO. 1



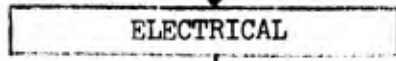
TEST GROUP NO. 1



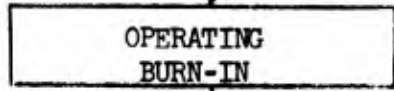
Per MIL-STD-883, method 1010, Cond. C,
 10 Cycles -65°C to $+150^{\circ}\text{C}$.
 TOTAL QTY 38



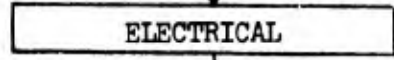
48 hours @ $+125^{\circ}\text{C}$ per MIL-STD-883, Method 1015,
 Cond. A
 TOTAL QTY 38



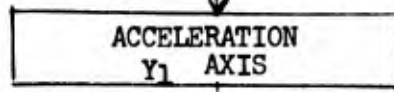
Data Log
 TOTAL QTY 38
 QTY FAIL 1
 S/N 60 transistor Q₂ shorted causing base lead
 to burn open.



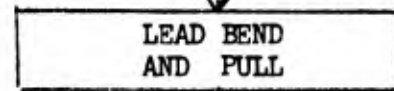
168 hours @ $+125^{\circ}\text{C}$ per MIL-STD-883, Method 1015,
 Cond. D.
 TOTAL QTY 37



Data Log
 TOTAL QTY 37
 QTY FAIL 0
 S/N's -



Per MIL-STD-883, Method 2001, 40,000 G, Y₁ Axis
 TOTAL QTY 37



Pull per MIL-STD-883, Method 2004, Cond. A
 (5 parts)
 Lead No. 1, 3, 5, 11, 13
 S/N's of Parts 12, 28, 251, 340, 382
 QTY FAIL 0

Bend per EPT-800 on 5 parts
 Lead No. 2, 4, 6, 8, 10
 S/N's of Parts 12, 28, 251, 340, 382
 QTY FAIL 1
 S/N 28 lead 8 came off

TEST GROUP NO. 1

FINE & GROSS
SEAL TEST

Per MIL-STD-883, Method 1014, Condition A and
Step 2 of C

TOTAL QTY FINE 37 QTY FAIL 1
S/N 162

TOTAL QTY GROSS 37 QTY FAIL 8
S/N;s 12^x, 28^x, 98, 183, 248, 251^x, 332, 368

S/N 28 lead 6 also fell off

X S/N's 12, 28, 251 were subjected to lead bend &
pull.

ELECTRICAL

Data Log

TOTAL QTY 37
QTY FAIL 1

S/N's 28* leads 6 & 8 off from previous testing

INTERNAL
VISUAL

Decap 10 parts 20 wires pulled/device.

Visual inspection and bond pull tests.

S/N's 12, 28, 251, 340, 382, 98, 183, 248, 332,
368

TOTAL QTY 10 QTY FAIL 2

S/N's 98, 332

S/N 98 wedge bond pulled at 1.6 gram

S/N 332 two ball bonds pulled at 0.7 gm.

DISPOSITION OF
LOT

Unopened EPT Samples sold to production.

QTY SOLD TO PRODUCTION 25

TO STOCK

Qty released to Stock 102

APPENDIX IIB
DATA FROM TEST GROUP NO. 2

VERIFICATION PHASE TESTING
FOR HYBRID CIRCUITS CONTRACT
WITH RADC PER MIL-STD-883, METHOD 5004

TEST GROUP NUMBER 2

PART TYPE - MEMORY HYBRID SWITCH

RECEIVED MARCH & MAY 1970

DATE CODES 7008, 7009, 7011 Qty 171 S/N 449-619

Class "C" Screening

EXTERNAL VISUAL
INSPECTION &
SERIALIZATION

Place serial numbers on all samples and look for visual rejects at same time.
Qty. 171

ELECTRICAL TEST AT
25°C, +125°C & -55°C

GO NO-GO testing and data log failures.

Total Qty. 25°C 171 Qty. Fail 25°C 4 (2.34%)
S/N's 476, 485, 490, 551 fail maximum limit for switching times.

Total Qty. -55°C 171 Qty. Fail -55°C 6 (3.59%)
S/N's 454, 537, 541, 542, 610, 612

S/N 454, 537, 541, 542, 610 fails saturation voltage maximum limit.

S/N 454, 537, 612 fails switching time maximum limits.

Total Qty. +125°C 171 Qty. Fail +125°C 1 (0.62%)
S/N 518 fails current source minimum limit.

HIGH TEMPERATURE
STABILIZATION

Per MIL-STD-883, Method 1008, Condition C, 48 hrs minimum @ +150°C.

Qty. 171

ELECTRICAL

GO NO-GO data log failures. Test in Dept. 32-38 with RADC Programs.

Total Qty. 171 Qty Fail 1 (0.625%)
S/N 612 fails circuit leakage current max. limit.

S/N 612 Q₁ collector to emitter short. Collector base breakdown voltage is 9 Volts.

TEST GROUP NUMBER 2

TEMPERATURE CYCLING

Per MIL-STD-883, Method 1010, Condition C, 10 cycles, -65°C to +150°C.

ELECTRICAL

GO NO-GO data log failures
Total Qty. 171 Total Qty. Fail 1
Qty. New Fails 0
S/N 612*

ACCELERATION Y₁ AXIS

Per MIL-STD-883, Method 2001, 30,000 G
Qty. 171

FINE & GROSS SEAL TEST

Per MIL-STD-883, Method 1014, Condition A and Condition C, Step 2. GO NO-GO fine leak rate limit 1×10^{-7} ATM cc/sec.

Total Qty. Fine Seal Tested 171
Total Qty. Gross Seal Tested 171
Qty. Fail Fine 0
Qty Fail Gross 4 (2.5%)
S/N's 452, 491, 537, 567

S/N's 537 & 567 removed from test.

ELECTRICAL

Data log all units.
Total Qty. 169
Total Qty. Fail 5 Qty. New Failures 4 (2.56%)
S/N's 498, 554, 565, 606, 612*

S/N's 498, 554, 565, 606, 612 removed from test.

S/N 498 loose ball bond to aluminum metalization of diode.

S/N's 554, 606 external lead missing.

S/N 565 loose ceramic substrate.

End of Class "C" screening procedures per MIL-STD-883, Method 5004.

Total Fallout $\frac{18}{171} = 10.5\%$,

Fallout excluding initial failures $\frac{9}{160} = 5.63\%$

*Failed earlier test.

TEST GROUP NUMBER 2

Beginning of Class "B" Screening per MIL-STD-883, Method 5004

BURN-IN
T_A = +125°C
168 HRS

Per MIL-STD-883, Method 1015, Condition D
Qty. 164

ELECTRICAL

Data log all units. Total Qty. 164

Qty. Fail 1 (0.61%)

S/N 575 circuit leakage current over max.limit.

End of Class "B" Processing

Total Fallout to obtain Class B Processed Parts $\frac{19}{171} = 11.1\%$

Fallout excluding initial failures $\frac{10}{160} = 6.25\%$

Beginning of Class "A" Processing per MIL-STD-883, Method 5004

THERMAL SHOCK

Liquid to liquid Total Qty. 164

Per MIL-STD-883, Method 1011, Condition C,
15 Cycles, -65°C to +150°C.

ELECTRICAL

GO NO-GO Data Log Fails

Total Qty. 164 Qty. New Failures 1 (0.614%)

Total Qty. Fail 2

S/N's 575*, 578

S/N 578 removed from test. External pin 8 missing.

MECHANICAL SHOCK

Per MIL-STD-883, Method 2002, Condition F,
Y₁ Axis, One Shock, 20,000 G Peak

Total Qty. 163

Qty. Damaged 2 (1.23%)

S/N's 450, 607

S/N's 450, 607 case damaged due to it being too fragile.

TEST GROUP NUMBER 2

ELECTRICAL

GO NO-GO Data Log Fails

Total Qty. 162

Total Qty. Fail 30

Qty. New Failures 28 (17.3%)

S/N's 449, 457, 463, 466, 473, 475, 477, 478, 483, 489, 492, 493, 495, 500, 549, 551*, 560, 563, 566, 569, 575, * 577, 586, 590, 591, 595, 597, 600, 605, 609

S/N's 449, 466, 473, 475, 500, 569, 600 ceramic substrate broke in two with one section loose and the other firmly attached.

S/N's 457, 464, 551, 566, 577, 586, 591, 595, 605, 609 loose gold ball bond to aluminum metalization on semiconductor chip.

S/N's 477, 478, 489, 492, 493, 495, 549, 560 loose ceramic substrate.

S/N 483 fails diode leakage current maximum limit.

S/N's 563, 590, 597 loose wedge bond to thick film conductor on substrate.

ACCELERATION
Y₁ AXIS

Per MIL-STD-883, Method 2001, 30,000 G, Y₁ Axis, Cond. E

Total Qty. 130

S/N 526 came apart during removal from carrier.

ELECTRICAL

GO NO-GO Data Log Fails

Total Qty. 130

Total Qty. Fail 13 Qty. New Failures 10 (7.7%)

S/N's 455, 485*, 496, 540, 553, 558, 570, 572, 575*, 592, 595*, 601, 613

S/N's 455, 496, 540, 553, 558, 570, 572, 592, 601, 613 removed from test.

S/N's 455, 496, 540, 570, 572, 592, 601, 613 loose ceramic substrate.

S/N's 553, 558 ceramic substrate broke in two with one piece loose and the other firmly attached.

BURN-IN
T_A = +125°C
72 HRS

Operating Life with Loads per MIL-STD-883, Method 1015, Cond. D.

Total Qty. 116

S/N 559 would not operate. Part removed and cover & substrate fell off.

TEST GROUP NUMBER 2

ELECTRICAL

Data Log

Total Qty. 116 Total Qty. Fail 2
Qty. New Failures 0
S/N's 575*, 595*

REVERSE BIAS
BURN-IN

72 Hrs @ +125°C per MIL-STD-883, Method 1015,
Condition A
Total Qty. 116

ELECTRICAL

Data Log @ 25°C
Total Qty. 116 Total Qty. Fail 2
Qty. New Fail 0
S/N's 575*, 595*
S/N 595 removed from test.

ACCELERATION
Y₂ AXIS

Per MIL-STD-883, Method 2001, 30,000 G, Y₂ Axis,
Cond. E
Total Qty. 115
S/N 589 cover fell off.

ELECTRICAL

GO NO-GO Data Log Fails
Total Qty. 115 Total Qty. Fail 18
Qt. New Failures 17 (14.9%)
S/N's 470, 480, 503, 512, 517, 519, 534, 541, 544,
547, 552, 575*, 599, 602, 603, 604, 608

ACCELERATION
Y₁ AXIS

Per MIL-STD-883, Method 2001, 40,000 G, Y₁ Axis
Total Qty. 114
S/N 582 package fell apart.

TEST GROUP NUMBER 2

FINE & GROSS SEAL TEST

Per MIL-STD-883, Method 1014, Condition A and Condition C, Step 2

Total Qty. Fine 114 Qty. New Fail 19 (16.7%)
S/N's 456, 470, 476, 480, 491, 501, 508, 513, 514, 528, 535, 536, 544, 547, 573, 574, 610, 617, 619

Total Qty. Gross 114 Qty. New Fail 70 (61.5%)
S/N's 456, 459, 460, 464, 467, 468, 470, 471, 472, 474, 476, 479, 480, 485, 487, 488, 490, 491, 494, 497, 501, 505, 507, 508, 509, 511, 513, 514, 515, 517, 518, 520, 521, 522, 524, 527, 528, 533, 535, 536, 538, 539, 543, 544, 545, 547, 552, 555, 556, 557, 562, 564, 568, 573, 574, 576, 580, 583, 585, 588, 593, 596, 599, 602, 608, 610, 614, 617, 618, 619

ELECTRICAL

GO-NO-GO Data Log Failures At +25°C, -55°C, +125°C

Total Qty. 113 Total Qty. Fail +25°C 9
Qty. New Failures 7 (6.3%)
S/N's 467, 468, 499, 507, 561, 568, 575*, 588, 599*
S/N's 467, 468, 499, 507, 561, 568, 588, 599 re-
moved from test.

S/N 467 loose wedge bond to the external lead post.
S/N 468, 561, 568, 588 loose ceramic substrate.
S/N 499, 507 cermaic substrate broke in two with one piece loose and other firmly attached.
S/N 588 external lead missing.
S/N 599 loose diode chip.

Qty. Fail -55°C 1 Qty. New Failures 0
S/N 541*

Qty. New Fail +125°C 1 (.952%) S/N 461
S/N 461 fails circuit leakage over maximum limit.

X-RAY

Per MIL-STD-883, Method 1012, Total Qt. 34
Qty. Fail 0

EXTERNAL VISUAL INSPECTION

Per MIL-STD-883, Method 2009
Total Qty. 34 Qty. Fail 0

End of Class "A" Screening

Total % Fallout due to all Processing 80.0%
Percent Fallout excluding initial Failures 78.7%

EPT SAMPLE

Quality Conformance Inspection
Sample Size 30

Total Qty. 30 S/N's 458, 462, 465, 481, 482, 484, 486, 502, 504, 506, 510, 516, 519, 523, 525, 529, 531, 532, 534, 546, 548, 571, 579, 587, 594, 598, 603, 604, 611, 615

TEST GROUP NUMBER 2

TEMPERATURE CYCLING

Per MIL-STD-883, Method 1010, Cond. C,
10 Cycles -65°C to $+150^{\circ}\text{C}$.
Total Qty. 30

VT STRESS

48 Hrs @ $+125^{\circ}\text{C}$ per MIL-STD-883, Method 1015,
Condition A
Total Qty. 30

ELECTRICAL

Data Log
Total Qty. 30
Qty. Fail 0

OPERATING
BURN-IN

168 Hrs @ $+125^{\circ}\text{C}$ per MIL-STD-883, Method 1015,
Condition D
Total Qty. 30

ELECTRICAL

Data Log
Total Qty. 30
Qty. Fail 0

ACCELERATION
Y₁ AXIS

Per MIL-STD-883, Method 2001, 40,000 G, Y₁ Axis
Total Qty. 30

LEAD BEND
AND PULL

Pull per MIL-STD-883, Method 2004, Cond. A
(4 Parts)
Pull Lead No's 1, 3, 5, 7, 9
S/N's of Parts 481, 484, 502, 532
Qty. Fail 0

Bend per EPT-800 on 4 parts
Bend Lead No's 2, 4, 6, 8, 10
S/N's of Parts 481, 484, 502, 532
Qty Fail 0

TEST GROUP NUMBER 2

Per MIL-STD-883, Method 1014,
Condition A and Step 2 of C

FINE & GROSS
SEAL TEST

Total Qty. Fine 30 Qty. Fail 0

Total Qty. Gross 30 Qty. Fail 3 (10.0%)

S/N's 484, 502, 587

S/N's 484, 502 were on lead bend and pull test.

ELECTRICAL

Data Log

Total Qty. 30
Qty. Fail 0

INTERNAL VISUAL

Decap 5 parts

Visual inspection and Bond Pull Tests

S/N 481, 484, 502, 532, 587

Total Qty. 5 Qty. Fail 0

DISPOSITION OF
LOT

The unopened EPT Samples to be sold to production.

Qty. Sold to Production 25

TO STOCK

Qty. released to Stock 29

APPENDIX IIIC
DATA FROM TEST GROUP NO. 3

VERIFICATION PHASE TESTING
 FOR HYBRID CIRCUITS CONTRACT
 WITH RADC PER MIL-STD-883, METHOD 5004

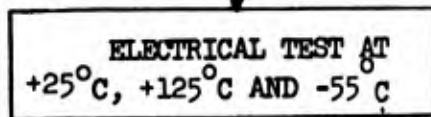
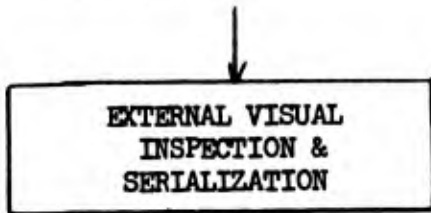
TEST GROUP NUMBER: 3
 SUPPLIER: B
 QUANTITY: 193
 RECEIVED: MARCH 1970

PART TYPE: LADDER SWITCH AND DRIVER
 S/N's: 1 thru 193
 DATE CODES: 7004, 7005, 7006, 7008

Class "C" Screening

Place serial numbers on all samples and look for visual rejects at same time.

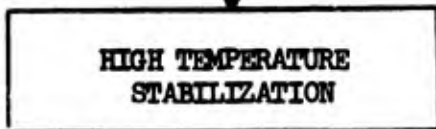
QTY: 193



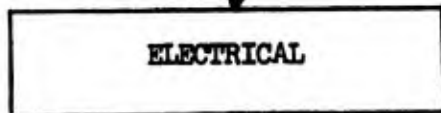
GO NO-GO testing and data log failures.
 TOTAL QTY 25°C 193 QTY FAIL 25 C 0

TOTAL QTY -55°C 193 QTY FAIL -55°C 10 (5.18%)
 SN's: 9, 11, 16, 18, 67, 116, 141, 178, 184, 193
 S/N's: 16, 67, 116, 141, 178, 184 fail maximum series resistance limit at -55°C.
 S/N's: 9, 11, 16, 18, 116, 141, 193 fail maximum offset limit at -55°C.

TOTAL QTY +125°C 193 QTY FAIL +125°C 2* (1.03%)
 S/N's: 178*, 184*
 S/N's 178, 184 fail maximum series resistance limit at +125°C.



Per MIL-STD-883, Method 1008, Condition C, 48 hrs. minimum @ +150°C.
 QTY: 193

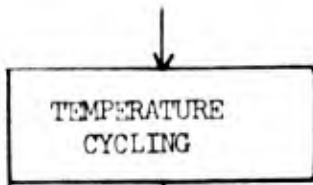


GO NO-GO data log failures. Test in Dept. 32-38 with RADC Programs.

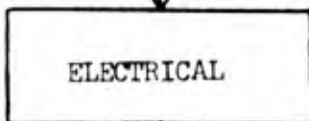
TOTAL QTY: 193 QTY FAIL: 1 (0.52%)
 S/N: 178

*Failed earlier test

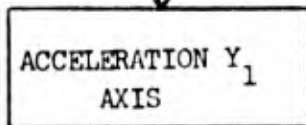
TEST GROUP NUMBER: 3



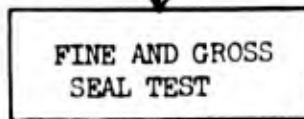
Per MIL-STD-883, Method 1010, Condition C,
10 cycles, -65°C to $+150^{\circ}\text{C}$.
Transfer time less than 1 minute.
QTY: 193



GO NO-GO data log failures.
TOTAL QTY: 193 QTY FAIL: 1*
QTY NEW FAIL: 0
S/N: 178*

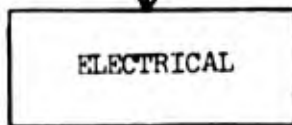


Per MIL-STD-883, Method 2001, 30,000G
QTY: 193



Per MIL-STD-883, Method 1014, Condition A and
Condition C, Step 2. GO NO-GO fine leak rate
limit 1×10^{-7} ATM cc/sec.

TOTAL QTY Fine Seal Tested: 193
TOTAL QTY Gross Seal Tested: 193
QTY FAIL Fine: 19 (9.90%)
S/N's: 33, 44, 46, 57, 79, 84, 87, 108, 112,
123, 134, 139, 147, 158, 166, 169, 172,
173, 193
QTY FAIL Gross: 11 (5.73%)
S/N's: 38, 44, 46, 87, 108, 112, 123, 134, 147
166, 193



Data log all units.
TOTAL QTY: 193
TOTAL QTY FAIL: 2
QTY. NEW FAILURES: 1 (0.52%)
S/N's: 178*, 181
S/N 181 failed because both diffused resistor
chips are loose.

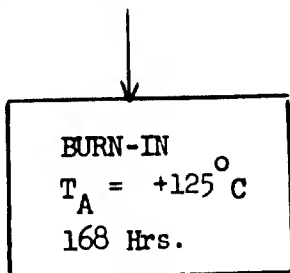
End of Class "C" screening procedures per MIL-STD-883, Method 5004,

TOTAL FALLOUT: $30/193 = 15.5\%$
FALLOUT WITHOUT INITIAL FAILS: $20/183 = 10.9\%$

*Failed earlier test

TEST GROUP NUMBER: 3

Beginning of Class "B" Screening per MIL-STD-883, Method 5004



Per MIL-STD-883, Method 1015, Condition D
Qty: 193
Data log all units. Total Qty: 193

Total Qty. Fail: 5
Qty. New Failures: 3 (1.57%)
S/N's: 10, 30, 38, 178*, 181*

S/N 10: Offset voltage increased over the maximum limit. Part left on test and it passed later tests until it was placed on burn-in again.

S/N 30: Input current increased over the maximum limit. Part left on test and it passed later tests. Part was lost prior to the next burn-in.

S/N 38: Circuit leakage current increased over the maximum limit. Part left on test and it passed later tests until it was placed back on burn-in again.

End of Class "B" Processing

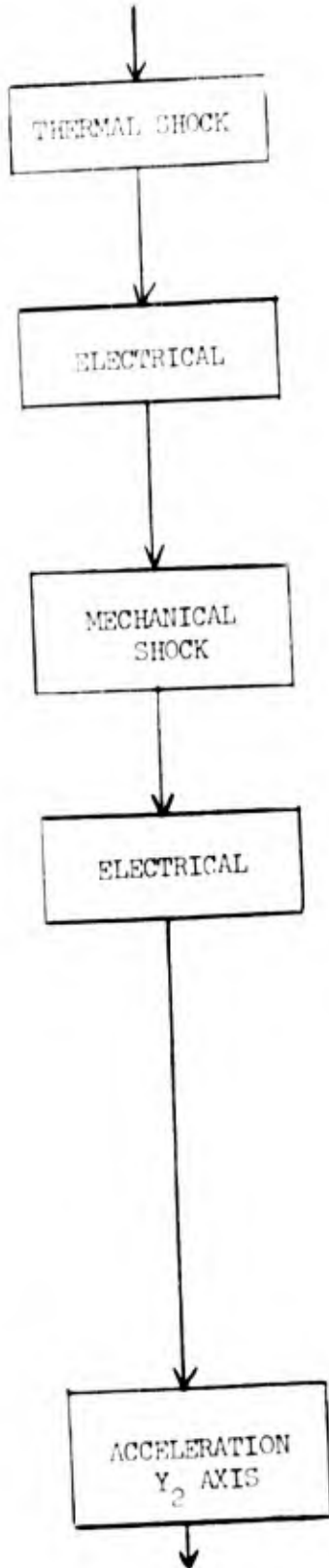
Total Fallout to Obtain Class B Processed
Parts: $\frac{32}{193} = 16.6\%$

Total Fallout Excluding Initial Failures=

$$\frac{22}{183} = 12\%$$

Beginning of Class "A" Processing per MIL-STD-883, Method 5004

TEST GROUP NUMBER: 2



Liquid to Liquid Total Qty: 193

Per MIL-STD-883, Method 1011, Cond. C.
15 Cycles, -65°C to $+150^{\circ}\text{C}$

GO NO-GO Data Log Fails

TOTAL QTY: 193

TOTAL QTY FAIL: 2

QTY. NEW FAILURES: 0

S/N's: 178*, 181*

Per MIL-STD-883, Method 2002, Cond. F
 Y_1 Axis, One Shock, 20,000G Peak

TOTAL QTY: 193

Qty. Damaged: 0

GO NO-GO Data Log Fails

TOTAL QTY: 193

TOTAL QTY FAIL: 8

QTY. NEW FAILURES: 6 (3.19%)

S/N's: 16, 82, 115, 127, 145, 147, 178*,
181*

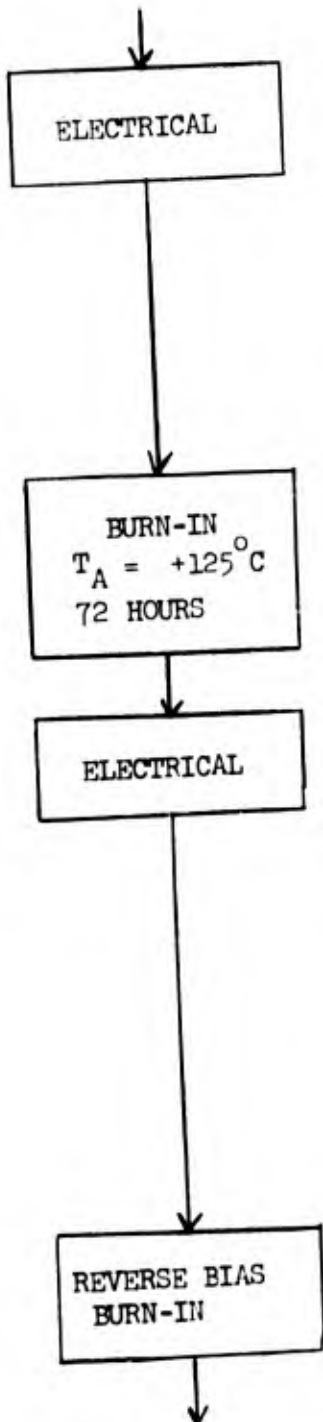
S/N's: 16, 82, 115, 127, 145, 147, 181
removed from test

S/N's: 115, 127, 145 loose ceramic substrate
S/N 16 Loose resistor chip
S/N 82 Loose transistor chip
S/N 147 Loose wedge bond to thick-film conductor on substrate.

Per MIL-STD-883, Method 2001
30,000G Y_2 Axis, Condition E

TOTAL QTY: 186

TEST GROUP NUMBER: 3



GO NO-GO Data Log Fails
TOTAL QTY: 186
TOTAL QTY. FAIL: 2
QTY. NEW FAILURES: 1 (0.55%)
S/N's: 60, 178*

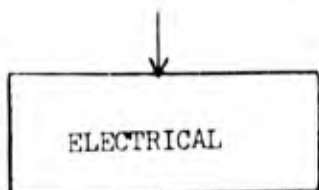
S/N 60 Removed from Test - Loose wedge bond going to thick-film conductor on substrate.

Operating life with loads per MIL-STD-383, Method 1015, Condition D
TOTAL QTY: 185
S/N 30 missing from test.

Data Log
TOTAL QTY: 184
TOTAL QTY FAIL: 5
QTY. NEW FAILURES: 2 (1.10%)
S/N's: 8, 10*, 28, 38*, 178*
S/N 8 Input zero current over the maximum limit.
S/N 28: Circuit leakage current over the maximum limit.
(Both parts left on test and they passed later tests.)

72 Hrs. @ +150°C per MIL-STD-383, Method 1015, Condition A
TOTAL QTY: 134

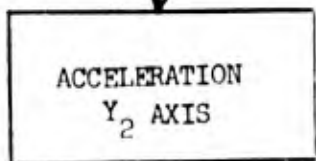
TEST GROUP NUMBER: 3



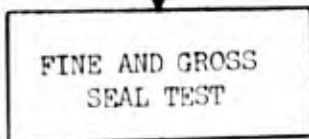
Data Log @ 25 °C

TOTAL QTY. +25 °C 184
TOTAL QTY. FAIL: 5
QTY. NEW FAIL: 4 (2.23%)
S/N's: 73, 141, 166, 178*, 184

S/N 73 Part has solid material inside of package as if liquid was in package and it became a solid.
S/N's 141, 166: Circuit leakage current increased over the maximum limit.
S/N 184 Series resistance increased over the maximum limit.



Per MIL-STD-883, Method 2001
40,000G, Y₂ Axis (Note: Y₂ Axis done in error)
TOTAL QTY: 184
S/N 152 Pin 1 (external lead) came off.



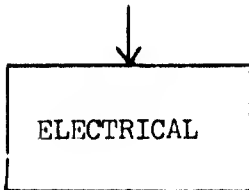
Per MIL-STD-883, Method 1014,
Condition A and Condition C, Step 2
TOTAL QTY. FINE: 183
TOTAL QTY. FAIL: 14
QTY. NEW FAILURES: 0

S/N's: 33*, 44*, 46*, 84*, 87*, 112*,
123*, 134*, 139*, 158*, 166*, 172*,
173*, 193*

TOTAL QTY. GROSS: 183
TOTAL QTY. FAIL: 0
QTY. NEW FAILURES: 2 (1.12%)

S/N's: 38*, 46*, 63, 73, 87*, 112*

TEST GROUP NUMBER: 3



GO NO-GO Data Log Failures at 25^o C,
-55^o C, +125^o C
TOTAL QTY: 183
TOTAL QTY. FAIL 25 C: 7
QTY. NEW FAILURES: 3 (1.70%)

S/N's: 11, 22, 141*, 166*, 170, 178*, 184*

S/N's 11, 22, 170 - Internal leads drooped down and shorting to edge of semiconductor chips and thick-film conductors on substrate.

TOTAL QTY. FAIL -55^o C: 12
QTY. NEW FAILURES: 3 (1.72%)

S/N's: 4, 9*, 11*, 14, 18*, 22*, 32, 67*, 116*, 141*, 178*, 184*

S/N's 4, 14 - Series resistance marginally over the maximum limit at -55 C.

S/N 32 - Internal leads drooped down and shorting at -55 C and +125 C only.

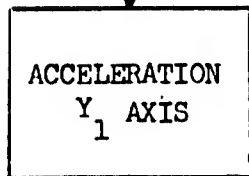
TOTAL FAIL +125^o C: 7
QTY. NEW FAILURES: 1 (0.57%)

S/N's: 11*, 22*, 32*, 125, 170*, 178*, 184*

S/N's 11, 22, 170: Removed from test for failure analysis.

S/N 125 leads drooped down and shorting at +125^o C only.

S/N 16 accidentally put back on test.



Per MIL-STD-383, Method 2001
40,000 G, Y₁ Axis
TOTAL QTY: 180

TEST GROUP NUMBER: 3

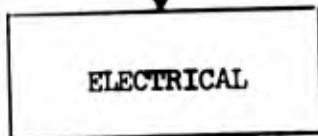


Per MIL-STD-883, Method 1014
Condition A and Condition C, Step 2
TOTAL QTY. FINE: $\frac{180}{4}$
TOTAL QTY. FAIL: $\frac{4}{2}$
QTY. NEW FAILURES: $\frac{2}{2}$ (1.12%)

S/N's: 38, 57*, 63, 112*

TOTAL QTY. GROSS: $\frac{180}{6}$
TOTAL QTY. FAIL: $\frac{6}{0}$
QTY. NEW FAILURES: $\frac{0}{0}$

S/N's: 38*, 44*, 46*, 63*, 87*, 112*



GO NO-GO Data Log Failures at +25^o C,
-55^o C and +125^o C
TOTAL QTY: $\frac{180}{9}$
TOTAL QTY. FAIL +25^o C: $\frac{9}{4}$
QTY. NEW FAILURES: $\frac{4}{4}$ (2.28%)

S/N's: 16*, 54, 69, 94, 112, 141*, 166*,
178*, 184*

S/N 54 - Loose wedge bond to thick-film
gold conductor on substrate and loose gold
ball bond to pin 2 gold plated post.

S/N's: 69, 94, 112: Loose ceramic substrate.

TOTAL QTY. FAIL -55^o C: $\frac{17}{4}$
QTY. NEW FAILURES: $\frac{4}{4}$ (2.28%)

S/N's: 4*, 9*, 14*, 15, 16*, 18*, 54*, 67*,
69*, 94*, 106, 112*, 116*, 141*,
178*, 184*, 185

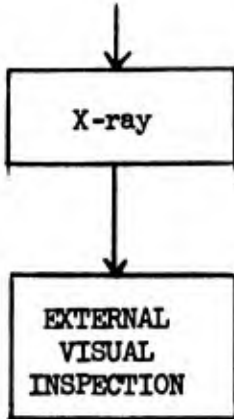
S/N 15 - Marginal over maximum -55^o C limit
for series resistance.

S/N's 106, 185: Unresolved, All internal
bonds pass 1.5 gm bond pull. Devices also
pass internal visual inspection. Lead dress
O.K.

TOTAL QTY: FAIL + 125^o C. $\frac{8}{0}$
QTY. NEW FAILURES: $\frac{0}{0}$

S/N's: 4*, 16*, 54*, 69*, 94*, 112*, 178*,
184*

TEST GROUP NUMBER: 3

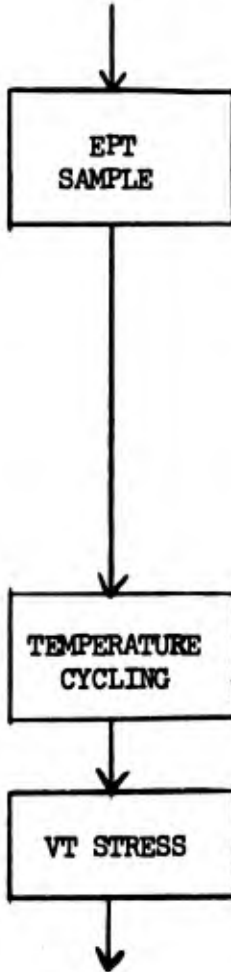


Per MIL-STD-883, Method 1012
TOTAL QTY: 20
QTY. FAIL: 0

Per MIL-STD-883, Method 2009
TOTAL QTY: 141
QTY. FAIL: 0

End of Class "A" Screening

TOTAL PERCENT FALLOUT DUE TO ALL
PROCESSING: 27.0%
PERCENT FALLOUT EXCLUDING INITIAL
FAILURES : 21.8%



Quality Conformance Inspection
Sample Size 38.

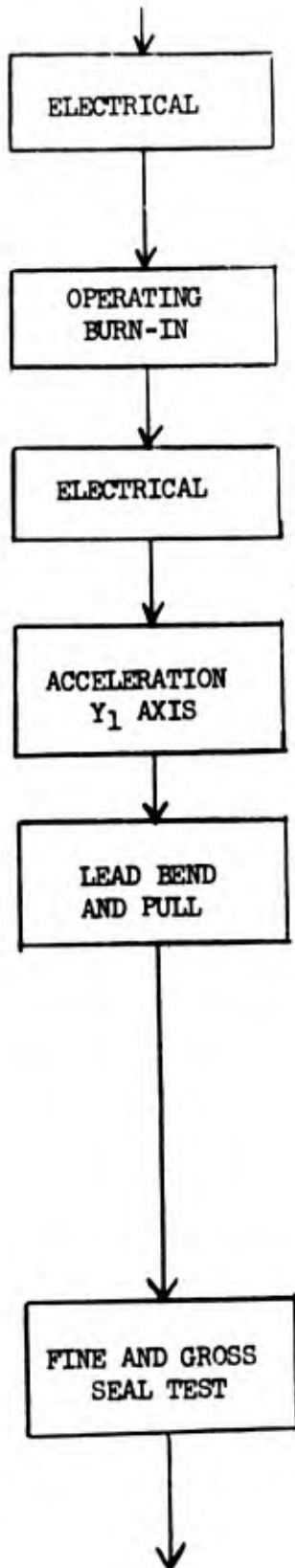
TOTAL QTY: 38

S/N's: 5, 13, 17, 21, 23, 37, 43, 47,
52, 62, 65, 66, 71, 74, 75, 78,
80, 83, 86, 97, 99, 102, 103,
109, 111, 113, 118, 120, 129,
130, 133, 137, 140, 154, 167,
168, 182, 188

Per MIL-STD-883, Method 1010, Cond. C
10 Cycles -65 C to +150 C
TOTAL QTY: 38

48 hours @ +125^o C per MIL-STD-883,
Method 1015, Condition A
TOTAL QTY: 38

TEST GROUP NUMBER: 3



Data Log
TOTAL QTY: 38
QTY. FAIL: 0

168 hours @ +125° C per MIL-STD-883
Method 1015, Condition D
TOTAL QTY: 38

Data Log
TOTAL QTY: 38
QTY. FAIL: 0

Per MIL-STD-883, Method 2001
40,000 G, Y₁ Axis
TOTAL QTY: 38

Pull per MIL-STD-883, Method 2004,
Condition A (4 parts)
Lead N's 1, 3, 5, 7, 9

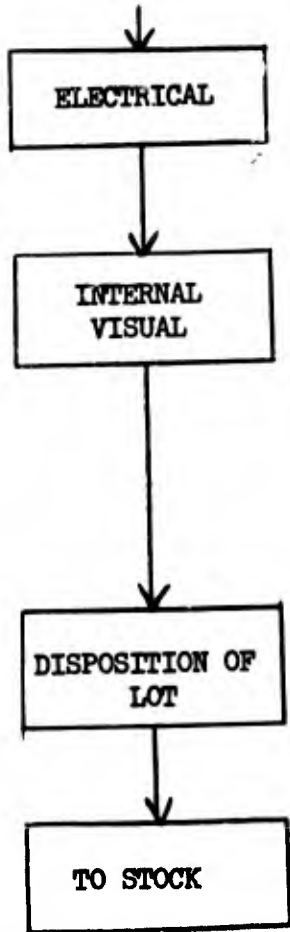
S/N's of Parts: 17, 71, 97, 113
QTY. FAIL: 0

Bend per EPT-800 on 4 parts
Lead N's 2, 4, 6, 8, 10

S/N's of parts: 17, 71, 97, 113
QTY. FAILED: 0

Per MIL-STD-883, Method 1014
Conditions A and Step 2 of C
TOTAL QTY. FINE: 38
QTY. FAIL: 0
TOTAL QTY. GROSS: 38 QTY. FAIL: 1 (2.63%)
S/N 71 was subjected to lead bend and pull testing.

TEST GROUP NUMBER: 3



Data Log
TOTAL QTY: 38
QTY. FAIL: 0

Decap 4 parts.
Visual inspection and bond
pull tests (40X, 100X)
S/N's: 17, 71, 97, 113

TOTAL QTY: 4 QTY. FAIL: 1
S/N 97 - One ball bond pulled off at 0.2 gm
from aluminum metalization of PNP transistor.

Unopened EPT samples to be sold to production.
QTY. SOLD TO PRODUCTION: 34

QTY. RELEASED TO STOCK: 137

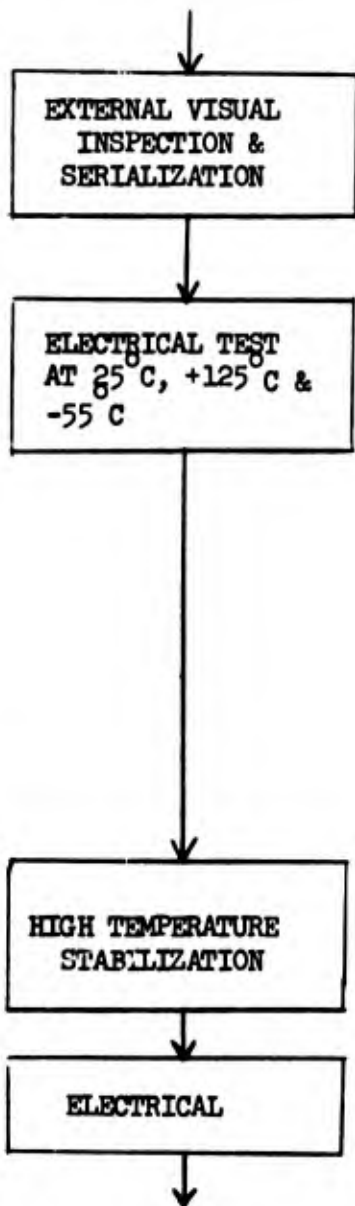
APPENDIX III
DATA FROM TEST GROUP NO. 4

VERIFICATION PHASE TESTING
FOR HYBRID CIRCUITS CONTRACT
WITH RADC PER MIL-STD-883, METHOD 5004

TEST GROUP NUMBER: 4
SUPPLIER: A
QUANTITY: 307
RECEIVED: APRIL 1970

PART TYPE: LADDER SWITCH AND DRIVER
S/N's: 194 thru 500
DATE CODE: 7011

Class "C" Screening



Place serial numbers on all samples and look for visual rejects at same time.

QTY: 307

GO NO-GO testing and data log failures.

TOTAL QTY: 25 C = 307

QTY. FAIL: 25 C = 0

TOTAL QTY. -55 C = 307

QTY. FAIL -55 C = 5 (1.63%)

S/N's: 226, 261, 264, 299, 443

S/N's 226, 264, 299 - fail maximum limit for offset voltage at -55 C.

S/N's 261, 264, 443 - fail maximum limit for series resistance at -55 C.

TOTAL QTY. +125 C: 307

QTY. FAIL +125 C: 0

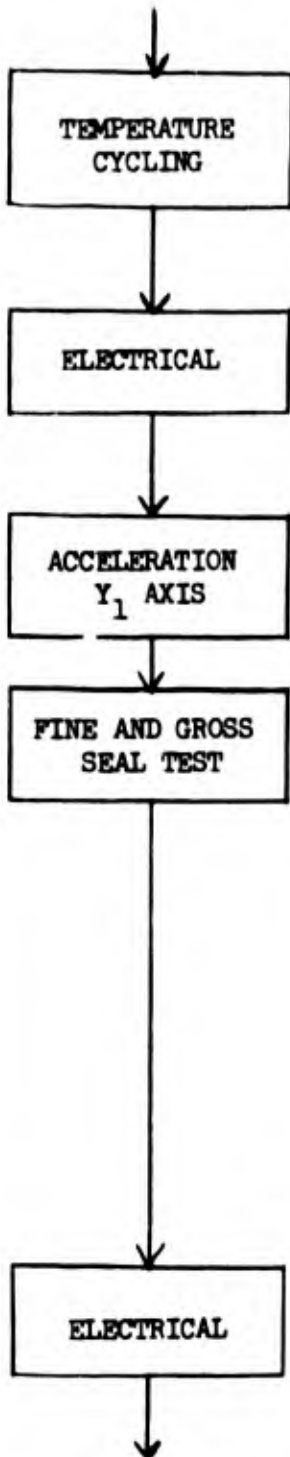
Per MIL-STD-883, Method 1008, Condition C
48 Hrs. minimum @ +150 C.

QTY: 307

GO NO-GO data log failures. Test in Dept. 32-38 with RADC Programs.

TOTAL QTY: 307 QTY. FAIL: 0

TEST GROUP NUMBER: 4



Per MIL-STD-883, Method 1010, Cond. C
10 Cycles, -65°C to +150°C
Transfer time less than 1 minute.
QTY: 307

GO NO-GO data log failures
TOTAL QTY: 307
QTY. FAIL: 0

Per MIL-STD-883, Method 2001, 30,000G
QTY: 307

Per MIL-STD-883, Method 1014,
Condition A and C, Step 2.
GO NO-GO fine leak rate limit 1×10^{-7}
ATM cc/sec.

TOTAL QTY. SEAL TESTED: 307
QTY. FAIL FINE: 21 (6.85%)
S/N's: 194, 195, 200, 205, 218, 227,
228, 230, 240, 255, 262, 263,
264, 265, 268, 326, 349, 360,
380, 456, 498

QTY. FAIL GROSS: 15 (4.90%)
S/N's: 194, 195, 205, 227, 230, 240,
255, 264, 265, 268, 349, 360,
380, 456, 498

Data log all units.
TOTAL QTY. 306 QTY. NEW FAIL: 1 (0.33%)
S/N 360 - Offset voltage increased over
maximum limit.

End of Class "C" screening procedures per MIL-STD-883, Method 5004

TEST GROUP NUMBER: 4

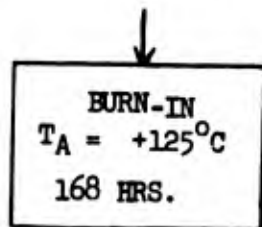
TOTAL FALLOUT TO OBTAIN CLASS "C"

PARTS: $\frac{25}{307} = \underline{8.15\%}$

TOTAL FALLOUT EXCLUDING INITIAL

FAILURES: $\frac{21}{307} = \underline{6.85\%}$

Beginning of Class "B" Screening per MIL-STD-883, Method 5004



Per MIL-STD-883, Method 1015, Cond. D
QTY: 306

Data log all units. TOTAL QTY: 306
TOTAL QTY. FAIL: 6
QTY. NEW FAILURES: 5 (1.64%)

S/N's: 219, 267, 329, 360*, 409, 414

S/N 219 - Offset voltage, series resistance and circuit leakage current increased over maximum limit. Device left on test and it continued to fail until after reverse-bias burn-in. After R-B burn-in, the part was O.K.

S/N 267 - Circuit leakage current increased over the maximum limit as if part shorted. Part had a loose metallic particle inside case.

S/N 329 - Input currents increased due to burn-in but were O.K. later. They increased again during the second burn-in. Cause of failure unresolved.

S/N 409 - Emitter-base leads of Q₃ look as if they are shorted together. Input offset voltage and circuit leakage current over maximum limit, later it was O.K. but went bad again during second burn-in.

S/N 414 - Input offset voltage drifted over the maximum limit.

TEST GROUP NUMBER: 4

End of Class "B" Processing

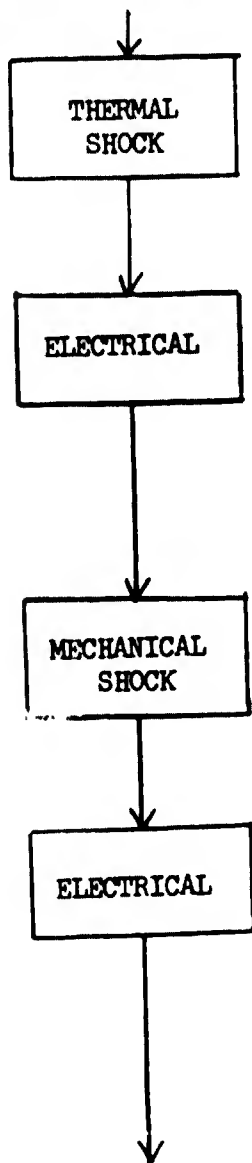
TOTAL FALLOUT TO OBTAIN CLASS B
PROCESSED PARTS:

$$\frac{30}{307} = \underline{9.78\%}$$

TOTAL FALLOUT EXCLUDING INITIAL
FAILURES:

$$\frac{26}{307} = \underline{8.47\%}$$

Beginning of Class "A" Processing per MIL-STD-883, Method 5004



Liquid to liquid TOTAL QTY: 306
Per MIL-STD-883, Method 1011, Cond C
15 Cycles, -65°C to +150°C

GO NO-GO Data Log Fails
TOTAL QTY: 306
TOTAL QTY. FAIL: 3
QTY. NEW FAILURES: 0

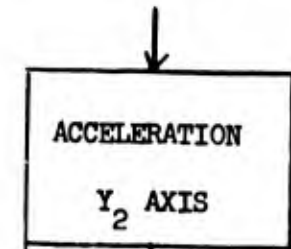
S/N's: 219*, 360*, 414*

Per MIL-STD-883, Method 2002, Cond F
Y₁ Axis, One Shock, 20,000 G Peak
TOTAL QTY: 306
QTY. DAMAGED: 0

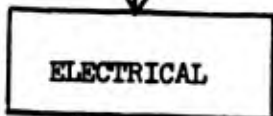
GO NO-GO Data Log Fails
TOTAL QTY: 306
TOTAL QTY FAIL: 4
QTY. NEW FAILURES: 1 (0.33%)

S/N's: 219*, 360*, 414*, 472
S/N 472 removed from test.
S/N 472 loose wedge bond to thick-film
conductor on substrate.

TEST GROUP NUMBER: 4

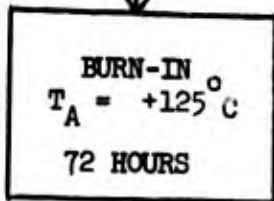


Per MIL-STD-883, Method 2001
30,000 G Y₂ Axis, Condition E
TOTAL QTY: 305

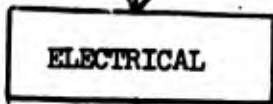


GO NO-GO Data Log Fails
TOTAL QTY: 305
TOTAL QTY. FAIL: 3
QTY. NEW FAILURES: 0

S/N's: 219*, 360*, 414*

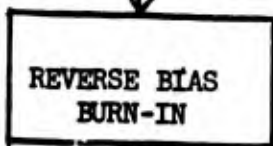


Operating Life with loads per
MIL-STD-883, Method 1015, Cond. D
TOTAL QTY: 306



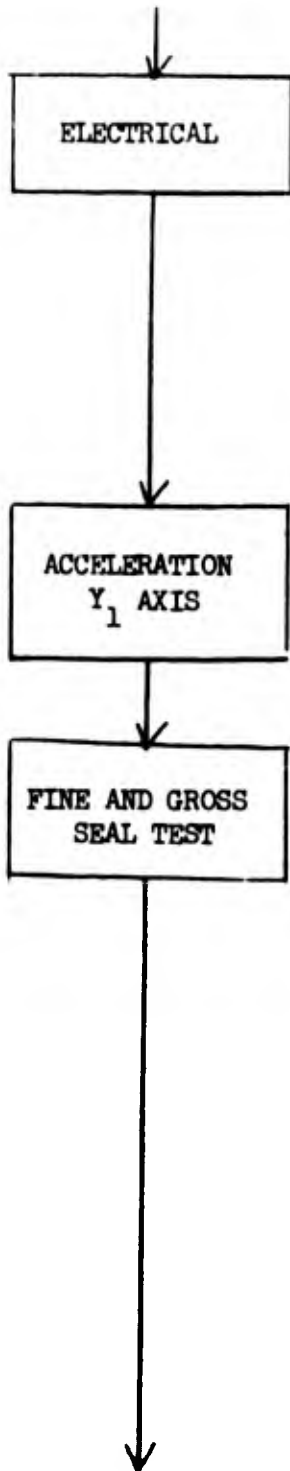
Data Log
TOTAL QTY: 306
TOTAL QTY. FAIL: 6
QTY. NEW FAILURES: 1 (0.33%)

S/N's: 219*, 329*, 337, 360*, 409*, 414*
S/N 337 - Circuit leakage current
increased over maximum limit. High leak-
age current went away during reverse bias
burn-in.



72 Hrs. @ +150° C per MIL-STD-883,
Method 1015, Condition A
TOTAL QTY: 305

TEST GROUP NUMBER: 4



Data Log @ 25°C
TOTAL QTY +25°C: 305
TOTAL QTY. FAIL: 5
QTY. NEW FAILURES: 3 (0.99%)

S/N's: 217, 228, 345, 360*, 414*
S/N's 217, 228 - Series resistance
drifted over the maximum limit.
S/N 345 - Offset voltage drifted over
the maximum limit.

Per MIL-STD-883, Method 2001
40,000 G, Y₁ Axis
TOTAL QTY: 305

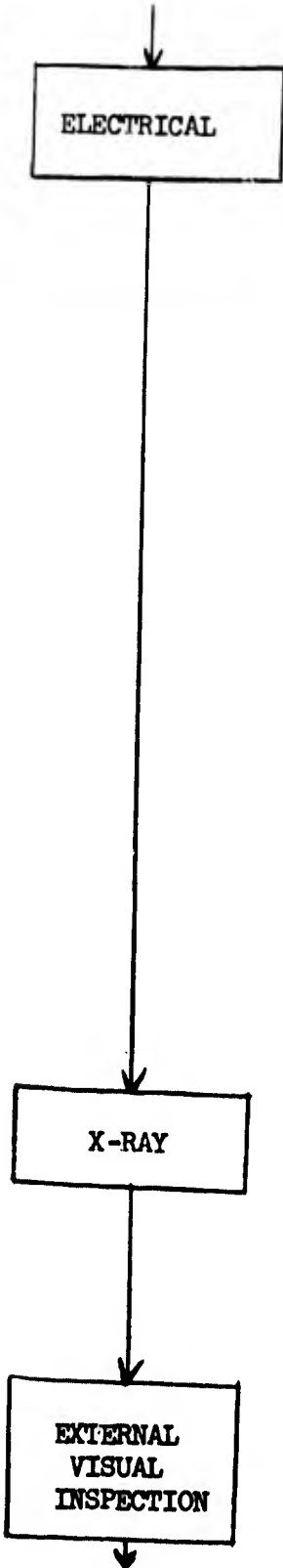
Per MIL-STD-883, Method 1014
Conditions A and C, Step 2
TOTAL QTY: FINE: 305
TOTAL QTY. FAIL: 19
QTY. NEW FAILURES: 1 (0.35%)

S/N's: 194*, 200*, 205*, 218*, 227*,
228*, 240*, 255*, 263*, 264*,
265*, 268*, 326*, 349*, 360*,
380*, 434, 456*, 498*

TOTAL QTY. GROSS: 305
TOTAL QTY. FAIL: 26
QTY. NEW FAILURES: 11 (3.8%)

S/N's: 194*, 195*, 200, 205*, 218,
227*, 228, 230*, 240*, 255*,
263, 264*, 265*, 268*, 319,
325, 326, 349*, 360*, 380*,
405, 434, 448, 450, 456*, 498*

TEST GROUP NUMBER: 4



GO NO-GO Data Log Failures At +25° C,
-55° C, +125° C.

TOTAL QTY: 305
TOTAL QTY. FAIL: +25° C: 6
QTY. NEW FAILURES: 2 (0.67%)

S/N's: 228*, 345*, 360*, 414*, 459, 482
S/N 345 - Open ball bond to aluminum
metalization on transistor chip.
S/N's 459, 482 - Open wedge bond to thick
film conductor on substrate.

TOTAL QTY. FAIL -55° C: 13
QTY. NEW FAIL: 2 (0.68%)

S/N's: 194*, 217*, 228*, 261*, 264*,
299*, 339, 345*, 360*, 399,
443*, 459*, 482*

S/N's 339, 399 - Offset voltage and series
resistance over the maximum limit.

TOTAL QTY. FAIL +125° C: 2
QTY. NEW FAIL: 2 (0.68%)

S/N's: 217*, 219*, 228*, 345*, 409*, 437,
449, 459*, 482*

S/N's 437, 449 - Offset voltage and series
resistance over the maximum limit.

Per MIL-STD-883, Method 1012

TOTAL QTY: 20
QTY. FAIL: 0

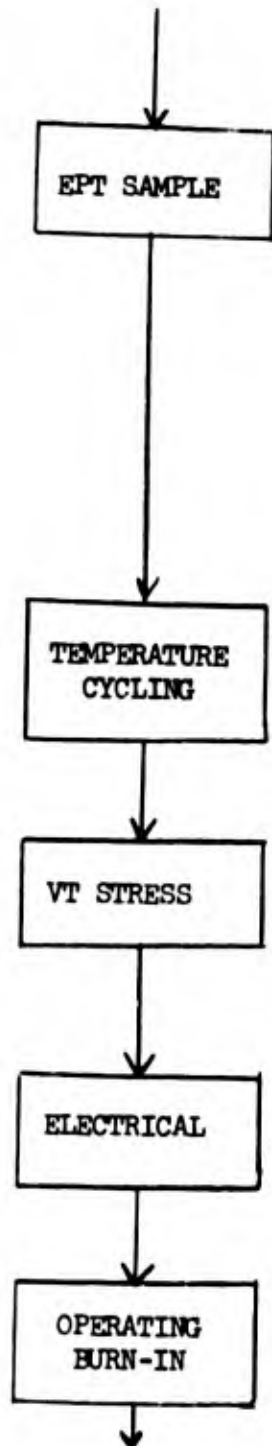
S/N's: 332, 373 - Opened for internal
inspection.

Per MIL-STD-883, Method 2009

TOTAL QTY: 258
QTY. FAIL: 0

TEST GROUP NUMBER: 4

End of Class "A" Screening



TOTAL PERCENT FALLOUT DUE TO ALL
PROCESSING: 16.0%
PERCENT FALLOUT EXCLUDING INITIAL
FAILURES: 14.3%

Quality Conformance Inspection
Sample Size 40
TOTAL QTY: 40

S/N's: 201, 202, 206, 209, 215, 224,
225, 239, 246, 269, 277, 281,
285, 289, 292, 293, 300, 306,
309, 312, 315, 335, 336, 351,
367, 379, 383, 398, 411, 412,
415, 419, 435, 452, 469, 479,
484, 492, 495

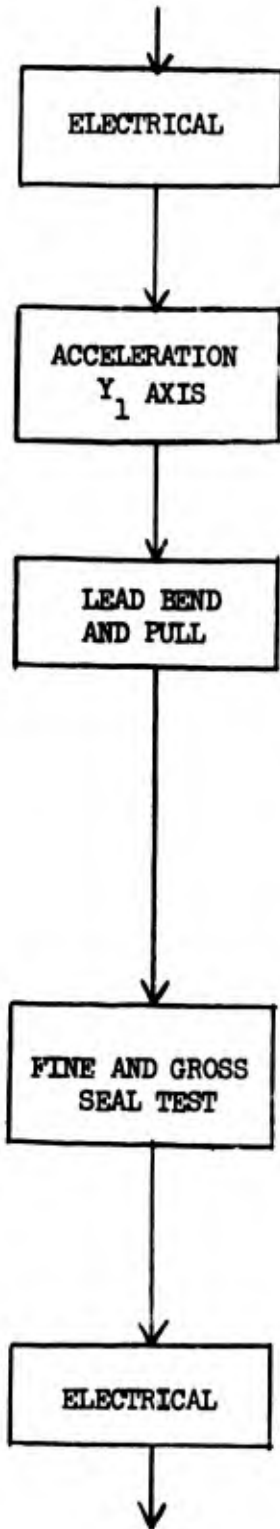
Per MIL-STD-883, Method 1010, Cond. C
10 Cycles -65 C to +150 C
TOTAL QTY: 40

48 Hours @ +125^o C per MIL-STD-883
Method 1015, Cond. A
TOTAL QTY: 40

Data Log
TOTAL QTY: 40
QTY. FAIL: 0

168 Hours @ +125^o C per MIL-STD-883
Method 1015, Condition D
TOTAL QTY: 40

TEST GROUP NUMBER: 4



Data Log
TOTAL QTY: 40
QTY. FAIL: 0

Per MIL-STD-883, Method 2001
40,000 G Y₁ Axis
TOTAL QTY: 40

Pull per MIL-STD-883, Method 2004
Condition A (4 Parts)
Leads: 1, 3, 5, 7, 9
S/N's of Parts: 206, 224, 285, 452
QTY. FAIL: 0

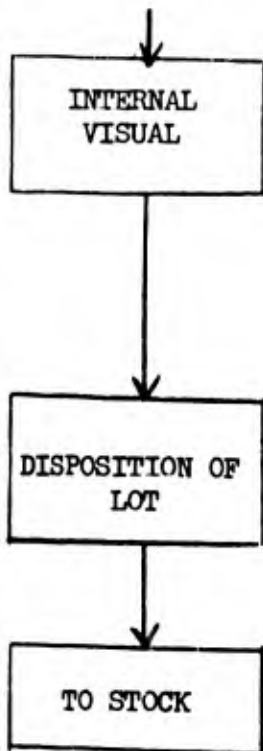
Bend per EPT-800 on 4 parts
Leads: 2, 4, 6, 8, 10
S/N's of Parts: 206, 224, 285, 452
QTY. FAIL: 0

Per MIL-STD-883, Method 1014
Conditions A and Step 2 of C
TOTAL QTY. FINE: 40
QTY. FAIL: 0

TOTAL QTY. GROSS: 40
QTY. FAIL: 0

Data Log
TOTAL QTY: 40
QTY. FAIL: 0

TEST GROUP NUMBER: 4



Decap 4 parts
Visual inspection and bond pull tests (20 wires/unit)
S/N's: 206, 224, 285, 452

TOTAL QTY: 4 QTY. FAIL: 1
S/N's: 285 Wire pulled at 2 gms. All others pass 2 gm pull test.

Unopened EPT samples to be sold to production.

QTY. SOLD TO PRODUCTION: 36

QTY. RELEASED TO STOCK: 254

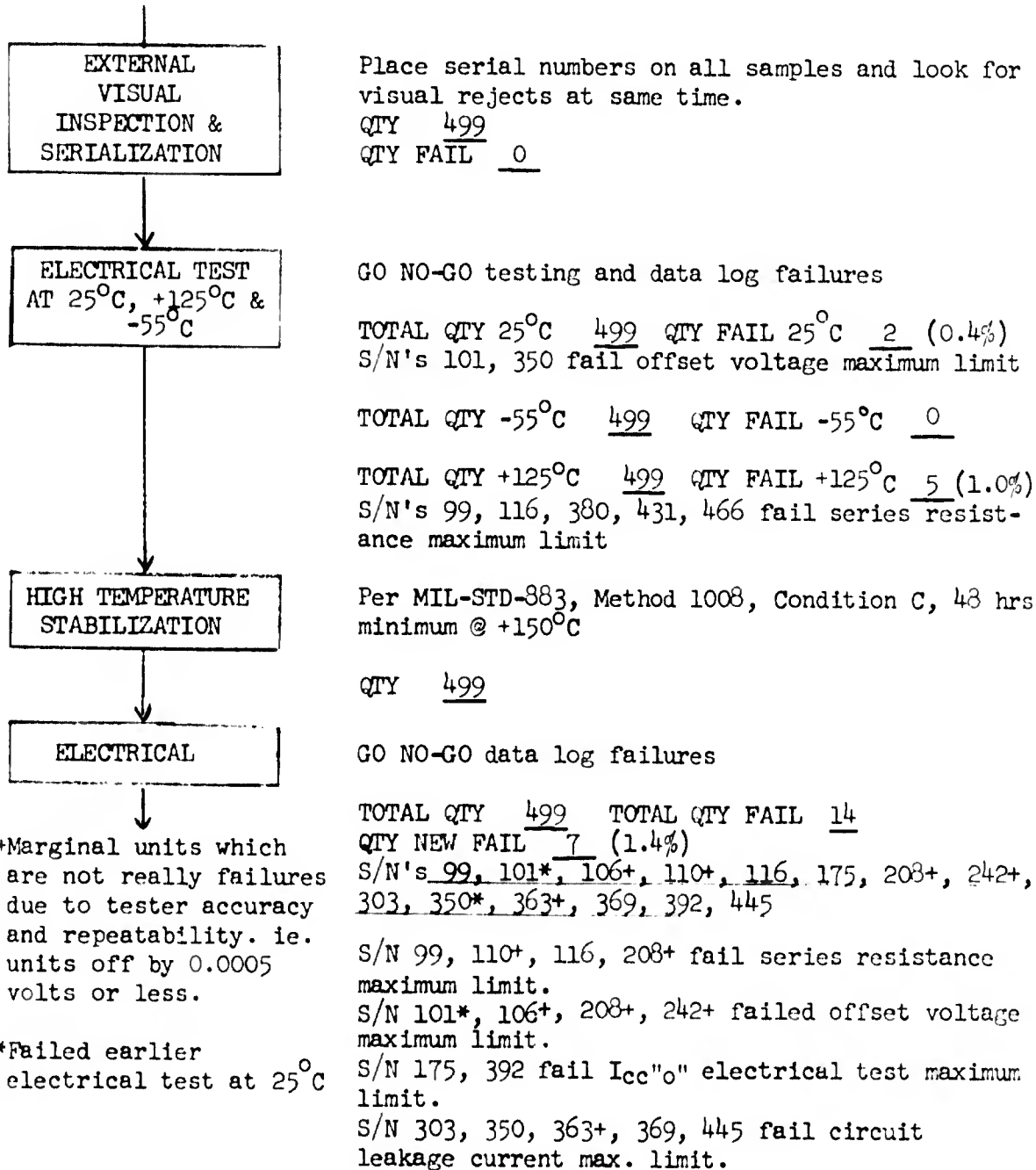
APPENDIX III E

DATA FROM TEST GROUP NO. 5

VERIFICATION PHASE TESTING
FOR HYBRID CIRCUITS CONTRACT
WITH RADC PER MIL-STD-883, METHOD 5004

TEST GROUP NUMBER 5 PART TYPE LADDER SWITCH AND DRIVER
 SUPPLIER B
 QUANTITY 499 S/N 1 - 499 RECEIVED FEB 1970
 DATE CODE 7002

CLASS "C" SCREENING



+Marginal units which are not really failures due to tester accuracy and repeatability. ie. units off by 0.0005 volts or less.

*Failed earlier electrical test at 25°C

TEST GROUP NO. 5

TEMPERATURE
CYCLING

Per MIL-STD-883, Method 1010, Condition C,
10 cycles, -65°C to +150°C.
Transfer time less than 1 minute.
QTY 499

GO NO-GO data log failures.

TOTAL QTY 499 TOTAL QTY FAIL 16
QTY NEW FAIL 4 (0.81%)

S/N's 101*, 116*, 175*, 185, 203, 208*, 238,
301, 303*, 350*, 369*, 392*, 445*, 106*, 242*,
281+

S/N 445 removed from testing.

S/N 185, 238 circuit leakage current over maximum limit.
S/N 203 looked like a collector-base short on Q₃ but cleared
up during confirmation of failure on manual tester. Part
decapped after all testing through Class "A" processing, and
could not find cause of failure.

S/N 301 switching time over maximum limit.

S/N 445 scratched aluminum metalization shorting collector-
base of transistor Q₃.

ACCELERATION
Y₁ AXIS

Per MIL-STD-883, Method 2001, 30,000 G
QTY 498

FINE & GROSS
SEAL TEST

Per MIL-STD-883, Method 1014, Condition A and
Condition C, Step 2. GO NO-GO fine leak rate
limit 1 x 10⁻⁷ ATM cc/sec.

TOTAL QTY SEAL TESTED 498
QTY FAIL FINE 4 (0.80%) S/N's 66, 94, 97,
212
QTY FAIL GROSS 40 (8.04%) S/N's 17, 29, 31, 80,
88, 89, 111, 121, 150, 157, 159, 181, 183, 205,
209, 212, 222, 230, 233, 243, 254, 266, 317,
327, 334, 343, 367, 370, 377, 391, 395, 397,
408, 422, 423, 439, 476, 487, 494, 499

ELECTRICAL

Data log all units.
TOTAL QTY 498 TOTAL QTY FAIL 18
QTY NEW FAILURES 2 (0.45%)

S/N's 116*, 175*, 185*, 238*, 264, 301*, 303*, 350*, 369*, 392*, 432,
99*, 101*, 106*, 208*, 242*, 281*, 466*

S/N's 264 & 432 removed from testing.

S/N's 264 & 432 loose resistor chip.

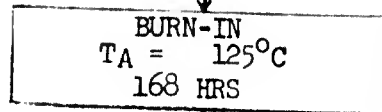
*Failed earlier test .

End of Class "C" screening procedures per MIL-STD-883, Method 5004.

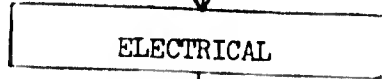
Total fallout $\frac{62}{499} = 12.4\%$ Total fallout excluding
initial failures $= \frac{55}{492} = 11.1\%$

TEST GROUP NUMBER 5

BEGINNING OF CLASS "B" SCREENING PER MIL-STD-883, METHOD 5004



Per MIL-STD-883, Method 1015, Condition D
QTY 495



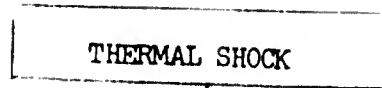
Data log all units TOTAL QTY 495
QTY NEW FAILURES 1 (0.23%)
TOTAL QTY FAIL 11
S/N's 99*, 101*, 107, 116*, 175*, 185*, 238*,
301*, 350*, 369*, 392*
S/N 107 removed from test. S/N 107 failure caused by holes in silicon oxide under aluminum termination for the nichrome resistors R1 & R3 causing them to short through the silicon substrate.

END OF CLASS "B" PROCESSING

Total fallout to obtain Class B parts $\frac{63}{499} = 12.6\%$

Total fallout excluding initial failures to obtain Class B parts $\frac{56}{492} = 11.4\%$

BEGINNING OF CLASS "A" PROCESSING PER MIL-STD-883, METHOD 5004

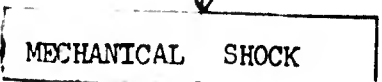


Liquid to liquid TOTAL QTY 494

Per MIL-STD-883, Method 1011, Cond. C, 15 cycles, -65°C to +150°C

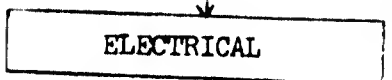


GO NO-GO Data Log Fails
TOTAL QTY 494 TOTAL QTY FAIL 16
QTY NEW FAILURES 1 (0.23%)
S/N's 29, 99*, 101*, 106*, 116*, 175*, 185*,
208*, 238*, 242*, 301*, 303*, 350*, 363*, 369*,
392*
S/N 29 fails circuit leakage current max. limit.



Per MIL-STD-883, Method 2002, Cond. F, Y₁ Axis, One Shock, 20,000 G Peak

TOTAL QTY 494
QTY DAMAGED 1 (0.20%)
S/N's 494



GO NO-GO DATA LOG FAILS
TOTAL QTY 494
QTY FAIL 15 QTY NEW FAILURES 2 (0.46%)
S/N's 29*, 99*, 101*, 116*, 175*, 185*, 225,
238*, 259, 301*, 303*, 350*, 369*, 392*, 494*
S/N's 225, 259, 494 removed from test.
S/N's 225, 259 loose resistor chip. Chip broke in two with part still attached to the substrate.

TEST GROUP NUMBER 5

ACCELERATION
Y₂ AXIS

Per MIL-STD-883, Method 2001, 30,000 G, Y₂ Axis,
Cond. E

TOTAL QTY 491

ELECTRICAL

GO NO-GO Data Log Fails

TOTAL QTY 491

TOTAL QTY FAIL 15 QTY NEW FAILURES 4 (0.93%)

S/N's 29*, 61, 99*, 116*, 175*, 185*, 238*, 267, 272, 301*,
303*, 350*, 355, 369*, 392*

S/N's 267, 272 & 355 removed from test for failure analysis.

S/N 61 Loose gold ball bond to base of Q₂.

S/N 267 Lead shorting to edge of transistor chip.

S/N 272 Emitter-base leads of Q₁ shorted together.

S/N 355 Base lead of Q₂ drooping down and shorting to thick
film pad on substrate.

BURN-IN
T_A = +125°C
72 HOURS

Operating Life with Loads per MIL-STD-883,
Method 1015, Cond. D.

TOTAL QTY 487

ELECTRICAL

Data Log

TOTAL QTY 487

TOTAL QTY FAIL 13 QTY NEW FAILURES 1 (0.23%)

S/N's 24, 29*, 61*, 99*, 116*, 175*, 185*, 238*, 301*, 303*,
350*, 369*, 392*

S/N 24 removed from test.

S/N 24 cause of failure unresolved.

REVERSE BIAS
BURN-IN

72 Hours @ +150°C per MIL-STD-883, Method 1015,
Cond. A

TOTAL QTY 486

ELECTRICAL

Data Log @ 25°C

TOTAL QTY +25°C 486 TOTAL QTY FAIL 37

QTY NEW FAILURES 23 (5.41%)

S/N's 28, 29*, 47, 61*, 90, 99*, 110*, 112, 116*, 119, 124,
137, 175*, 185*, 208*, 214, 268, 269, 301*, 303*, 331, 334,
350*, 359, 362, 363*, 365, 369*, 380, 383, 392*, 431, 433,
435, 443, 466, 498

S/N 119 & 433 removed from test.

S/N 28, 47, 90, 110, 112, 124, 137, 208, 214, 268, 269, 331,
334, 359, 362, 365, 380, 431, 435, 443, 466, 498 series

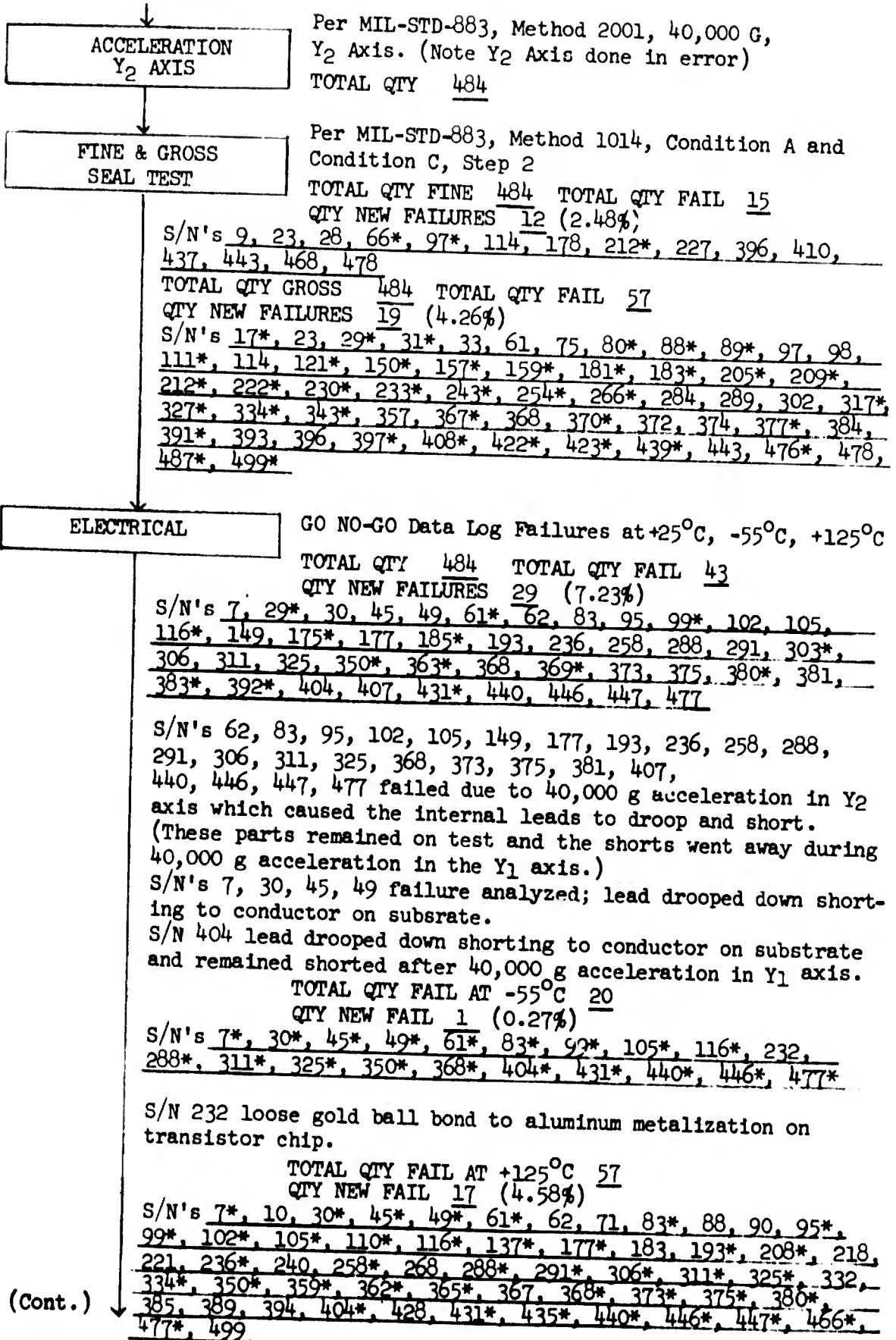
resistance increased over the maximum limit.

S/N 119, 433 device channeled and destroyed internal leads from high leak-
age current.

S/N 363 circuit leakage current increased significantly over the max. limit.

S/N 383 power supply drain current increased over the maximum limit.

TEST GROUP NUMBER 5



(Cont.)

TEST GROUP NUMBER 5

ELECTRICAL
(CONT.)

S/N's 10, 62, 71, 88, 183, 218, 221, 240, 268, 332, 367, 385, 389, 394, 428, 499 failed due to 40,000 g acceleration in Y₂ axis which caused the internal leads to droop and short at +125°C but not at +25°C or -55°C. (These parts remained on test and the shorts went away during 40,000 g acceleration in the Y₁ axis.)

S/N 90 series resistance over maximum limit at +125°C.
S/N 268 shorts went away after Y₁ axis acceleration but series resistance remained over maximum limit at +125°C.

ACCELERATION
Y₁ AXIS

Per MIL-STD-883, Method 2001, 40,000 g, Y₁ Axis
TOTAL QTY 480

FINE & GROSS
SEAL TEST

Per MIL-STD-883, Method 1014, Condition A and Condition C, Step 2

TOTAL QTY FINE 480 TOTAL QTY FAIL 13
QTY NEW FAIL 3 (0.64%)

S/N's 9*, 23*, 28*, 61, 100, 114*, 178*, 183*, 212*, 374, 437*, 443*, 478*

TOTAL QTY GROSS 480 TOTAL QTY FAIL 61
QTY NEW FAIL 5 (1.06%)

S/N's 9, 17*, 23*, 28, 29*, 31*, 33*, 61*, 80*, 89*, 97*, 98*, 111*, 114*, 121*, 150*, 157*, 159*, 178, 181*, 183*, 205*, 209*, 212*, 222*, 230*, 233*, 243*, 254*, 266*, 284*, 289*, 302*, 317*, 327*, 334*, 343*, 357*, 367*, 368*, 370*, 372*, 374*, 377*, 384*, 391*, 395*, 396*, 397*, 408*, 422*, 423*, 437, 439*, 443*, 453, 476*, 478*, 487*, 499*

ELECTRICAL

GO NO-GO Data Log Failures at +25°C, -55°C, +125°C

TOTAL QTY 480 TOTAL QTY FAIL AT +25°C 16
QTY NEW FAIL 2 (0.565%)

S/N's 29*, 61*, 99*, 116*, 143, 175*, 185*, 208*, 263, 288*, 303*, 350*, 363*, 369*, 392*, 404*

S/N's 143, 208, 263 removed from test.

S/N's 143, 208, 263 failed due to loose resistor chip.

TOTAL QTY FAIL at -55°C 7
S/N's 61*, 99*, 116*, 185*, 232*, 288*, 404*

QTY NEW FAILURES AT -55°C 0

TOTAL QTY FAIL AT +125°C 33

QTY NEW FAILS AT +125°C 13 (3.7%)

S/N's 25, 28, 61*, 90*, 99*, 110*, 112, 116*, 124, 137*, 185*, 198, 214, 268*, 269, 288*, 331, 334*, 337, 350*, 359*, 362*, 365*, 373*, 380*, 404*, 416, 431*, 435*, 437, 443, 466*, 498

S/N's 25, 28, 112, 124, 198, 214, 269, 331, 337, 416, 437, 443, 498 series resistance slightly over max. limit (Marginal units)

X-RAY

Per MIL-STD-883, Method 1012

TOTAL QTY 20 QTY FAIL 0

TEST GROUP NUMBER 5

EXTERNAL VISUAL INSPECTION

Per MIL-STD-883, Method 2009

TOTAL QTY 367 QTY FAIL 0

Total % Fallout Due to All Processing 26.5%

Percent Fallout Excluding Initial Failures 25.4%

END OF CLASS "A" SCREENING

EPT SAMPLE

Quality Conformance Inspection

Sample Size 45

TOTAL QTY 45

S/N's 15, 22, 34, 39, 68, 72, 77, 84, 86, 96, 113, 133, 138, 165, 193, 215, 226, 235, 240, 245, 256, 260, 261, 277, 278, 291, 304, 307, 310, 314, 330, 349, 376, 381, 385, 386, 388, 414, 415, 426, 428, 446, 448, 485, 493

TEMPERATURE CYCLING

Per MIL-STD-883, Method 1010, Cond. C, 10 Cycles -65°C to +150°C

TOTAL QTY 45

V-T STRESS

48 hours @ +125°C per MIL-STD-883 Method 1015, Cond. A

TOTAL QTY 45

ELECTRICAL

Data Log

TOTAL QTY 45
QTY FAIL 0

OPERATING BURN-IN

168 hours @ +125°C per MIL-STD-883, Method 1015, Cond. D

TOTAL QTY 45

TEST GROUP NUMBER 5

ELECTRICAL

Data Log

TOTAL QTY 45
QTY FAIL 0

ACCELERATION Y₁ AXIS

Per MIL-STD-883, Method 2001,
40,000 G, Y₁ Axis

TOTAL QTY 45

LEAD BEND
AND PULL

Pull per MIL-STD-883, Method 2004,
Cond. A (5 parts)
Leads 1, 3, 5, 7, 9 pulled

S/N's of parts 34, 165, 381, 388, 485
QTY FAIL 0

Bend per EPT-800 on 5 parts
Leads 2, 4, 6, 8, 10 bent

S/N's of parts 34, 165, 381, 388, 485
QTY FAIL 0

FINE & GROSS
SEAL TEST

Per MIL-STD-883, Method 1014,
Conditions A and Step 2 of C

TOTAL QTY FINE 45 QTY FAIL 0

TOTAL QTY GROSS 45 QTY FAIL 2
S/N's 381, 485

S/N's 381, 485 were used for lead bend & pull testing.

TEST GROUP NUMBER 5

ELECTRICAL

Data Log

TOTAL QTY 45
QTY FAIL 0

INTERNAL
VISUAL

Decap 5 parts
Visual inspection and bond pull tests
S/N's 34, 165, 381, 388, 485

TOTAL QTY 5 QTY FAIL 1
S/N 388 wedge bond to substrate pulled at 0.8 gm.

DISPOSITION OF
LOT

Unopened EPT samples to be sold to production.

Qty sold to Production 40

TO STOCK

Qty released to Stock 362

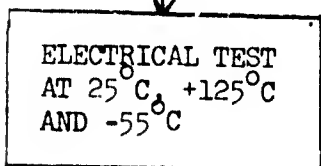
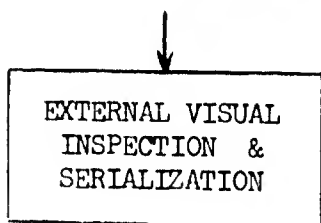
APPENDIX III F
DATA FROM TEST GROUP NO. 6

VERIFICATION PHASE TESTING
 FOR HYBRID CIRCUITS CONTRACT
 WITH RADC PER MIL-STD-883, METHOD 5004

TEST GROUP NUMBER: 6
 SUPPLIER: C
 QUANTITY: 542
 RECEIVED: JULY 1970

PART TYPE: LADDER SWITCH & DRIVER
 S/N's: 1 thru 542
 DATE CODE: 7028, 260

Class "C" Screening



Place serial numbers on all samples and look for visual rejects at same time.

QTY: 542

GO NO-GO testing and data log failures.

TOTAL QTY. 25°C: 542

QTY. FAIL 25°C: 33 (6.08%)

S/N's: 4, 43, 51, 54, 65, 73, 93, 96,
137, 139, 185, 188, 190, 195,
233, 237, 260, 329, 338, 343,
363, 410, 413, 433, 435, 450,
451, 455, 490, 497, 510, 535,
536

Above units fail the series resistance maximum limit.

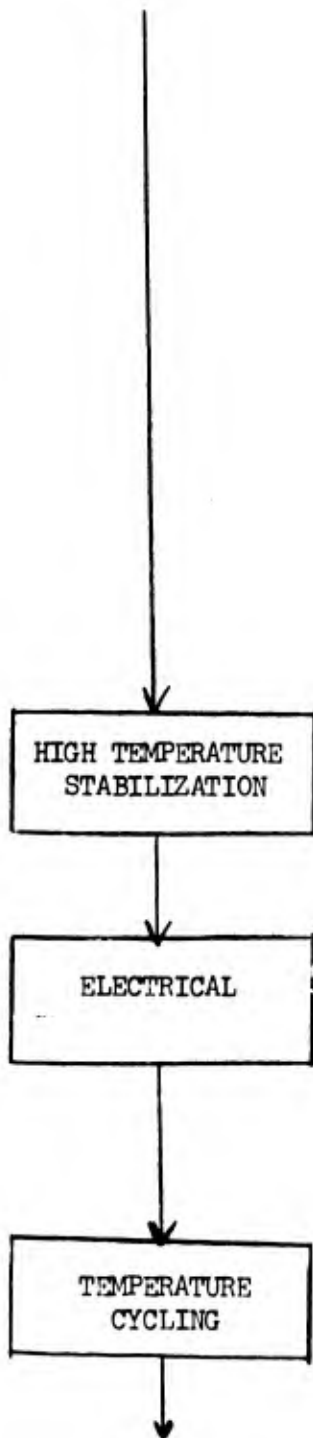
TOTAL QTY. -55°C: 542

TOTAL QTY. FAIL -55°C: 86

QTY. NEW FAIL: 65 (12.75%)

S/N's: 8, 15, 24, 43*, 46, 51*, 54*,
58, 60, 62, 65*, 73*, 77, 85,
86, 96*, 101, 115, 117, 123,
124, 130, 133, 135, 137*, 139*,
141, 143, 147, 152, 153, 156,
158, 163, 165, 174, 177, 183,
185*, 188*, 190*, 195*, 197,
220, 220, 222, 227, 230, 231,
233*, 234, 237*, 242, 252, 260*,
 (Continued next page)

TEST GROUP NUMBER: 6



S/N's (Continued): 270, 287, 290,
291, 300, 302, 309, 313, 325,
393, 396, 413*, 422, 433*,
447, 464, 474, 475, 486, 490*,
495, 509, 510*, 514, 521, 525,
527, 531, 532, 534, 535*, 536*

All the above failures, except S/N 396,
fail the series resistance maximum limit.
S/N's: 73, 115, 123, 143, 174, 177, 183,
396, 474 also fail to meet the
maximum limit for offset voltage.

TOTAL QTY. +125° C: 542
QTY. FAIL +125° C: 0

INITIAL FALLOUT REMOVED FROM TEST:

$$\frac{98}{542} = \underline{18.1\%}$$

Per MIL-STD-883, Method 1008, Cond. C
48 Hrs. minimum @ +150° C.
QTY: 444

GO NO-GO data log failures. Test in
Dept. 32-38 with RADC programs.
TOTAL QTY: 443
QTY. FAIL: 2

S/N's: 331, 354 - Marginal series
resistance.

Per MIL-STD-883, Method 1010, Cond. C
10 Cycles, -65° C to +150° C
Transfer time less than 1 minute.
QTY: 443

TEST GROUP NUMBER: 6



GO NO-GO data log failures.

TOTAL QTY: 443

QTY. FAIL: 0

Per MIL-STD-883, Method 2001, 30,000G

QTY: 443

Per MIL-STD-883, Method 1014, Cond. A
And Condition C, Step 2. GO NO-GO
fine leak rate limit 1×10^{-7} ATM
cc/sec.

Total Qty. Fine Seal Tested: 443

Total Qty. Gross Seal Tested: 443

Qty. Fail Fine: 1 (0.23%) S/N 315

Qty. Fail Gross: 3 (0.677%)

S/N's: 112, 203, 289

S/N 112 - Had many fine bubbles.

Data log all units.

TOTAL QTY: 443

QTY. FAIL: 4 (0.90%)

S/N's: 92, 159, 184, 513

S/N's: 92, 159, 184, 513 - removed
from test.

S/N's: 92, 159 - Transistor chip
loose from substrate.

S/N's: 184, 513 - Resistor chip loose
from substrate.

End of Class "C" Screening Procedures per MIL-STD-883, Method 5004.

TOTAL FALLOUT FOR CLASS C

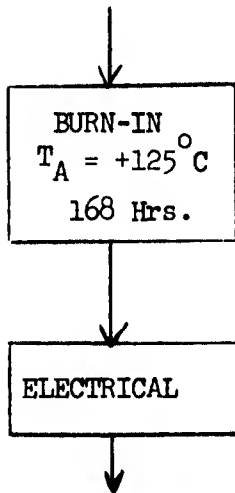
PARTS: $\frac{108}{542} = \underline{20\%}$

TOTAL FALLOUT EXCLUDING INITIAL

FAILURES: $\frac{10}{444} = \underline{2.26\%}$

TEST GROUP NUMBER: 6

Beginning of Class "B" Screening per MIL-STD-883, Method 5004



Per MIL-STD-883, Method 1015, Cond. D.
Data log all units.

TOTAL QTY: $\frac{439}{}$
QTY. FAIL: $\frac{0}{}$

End of Class "B" Processing

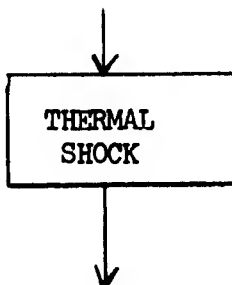
TOTAL FALLOUT FOR CLASS B PARTS:

$$\frac{108}{542} = \underline{20\%}$$

TOTAL FALLOUT EXCLUDING INITIAL FAILURES:

$$\frac{10}{444} = \underline{2.26\%}$$

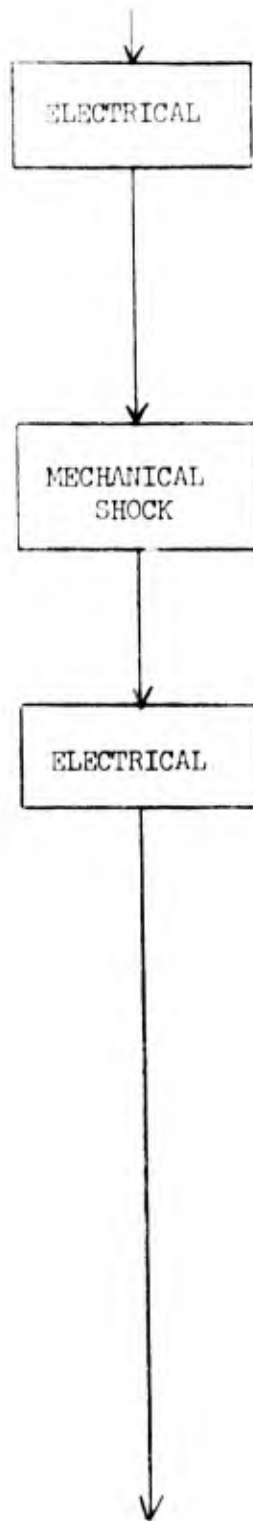
Beginning of Class "A" Processing per MIL-STD-883, Method 5004



Liquid to Liquid
TOTAL QTY: $\frac{439}{}$

Per MIL-STD-883, Method 1011, Cond. C
15 Cycles, -65°C to +150°C

TEST GROUP NUMBER: 6



GO NO-GO Data Log Fails
TOTAL QTY: 439
QTY. NEW FAIL: 2 (0.455%)
S/N's: 136, 443

S/N 443 removed from test.
S/N 443 failed due to a loose resistor chip.

Per MIL-STD-883, Method 2002, Cond F
Y₁ Axis, One Shock, 20,000 G Peak
TOTAL QTY: 438
QTY. DAMAGED: 0

GO NO-GO Data Log Fails
TOTAL QTY: 438
QTY. NEW FAIL: 9 (2.1%)
S/N's: 11, 57, 76, 90, 166, 218, 328, 337, 403
S/N's: 11, 57, 76, 90, 166, 218 -
Removed from test.

S/N 11 - Open gold ball bond to aluminum metalization on resistor chip and open wedge bond to aluminum metalization on transistor.

S/N's: 57, 76 - Open gold ball bond to aluminum metalization on transistor-emitter.

S/N 90 - Loose transistor chip.

S/N 166 - Loose transistor chip.

S/N 218 - Open gold ball bond to thick-film gold on substrate. (Lead was not bonded to scrubbed area near chip.)

S/N's: 328, 337, 403 - Series resistance drifted over maximum limit. S/N 328 also had circuit leakage drift over maximum limit.

TEST GROUP NUMBER: 6

ACCELERATION
Y₂ AXIS

ELECTRICAL

Per MIL-STD-883, Method 2001
30,000 G Y₂ Axis, Cond. E.
TOTAL QTY: 432

GO NO-GO Data Log, Fails
TOTAL QTY: 432
QTY. NEW FAIL: 133 (30.8%)

S/N's: 1, 3, 5, 14, 18, 22, 23, 25,
27, 28, 31, 32, 36, 37, 45,
47, 48, 53, 52, 64, 68, 69,
71, 79, 89, 97, 100, 102, 104,
106, 107, 112, 113, 121, 140, 157,
161, 169, 191, 198, 201, 202, 203,
206, 210, 223, 225, 226, 229,
232, 239, 243, 245, 248, 251,
256, 259, 265, 266, 272, 276,
282, 288, 296, 303, 304, 306,
321, 322, 328, 330, 331, 340,
342, 345, 346, 348, 350, 353,
356, 360, 361, 362, 366, 368,
371, 372, 374, 375, 376, 380,
385, 386, 391, 392, 400, 403,
406, 408, 414, 420, 421, 429,
430, 433, 434, 437, 441, 442,
446, 449, 458, 459, 460, 465,
466, 470, 473, 476, 477, 484,
485, 493, 494, 502, 504, 506,
516, 520, 522, 530, 538, 542

Failure analysis performed on S/N's 1, 3, 5 at this time. The rest of the failures were left in until after Y₁ axis acceleration.

NOTE: Actual catastrophic fallout due to Y₂ axis acceleration (i.e., Y₁ axis acceleration at 40,000G did not make parts O.K. again).

$$\frac{47}{432} = \underline{10.9\%}$$

TEST GROUP NUMBER: 6

Failures due to Y_2 axis acceleration at 30,000 G:

S/N's: 22, 23, 27, 31, 36, 37, 45, 48, 50, 52, 64, 68, 79, 97, 102, 106, 112, 121, 140, 157, 169, 191, 201, 202, 203, 210, 223, 225, 226, 229, 232, 239, 243, 248, 251, 256, 259, 266, 272, 276, 296, 303, 304, 322, 330, 331, 340, 342, 345, 346, 348, 350, 356, 360, 368, 372, 374, 376, 385, 391, 400, 403, 406, 408, 421, 429, 437, 441, 446, 459, 460, 465, 466, 470, 476, 477, 484, 485, 493, 494, 504, 516, 520, 522, 538, 542 (86 parts) failed due to drooped leads causing shorts but passed after 40,000G acceleration in the Y_1 axis.

S/N's: 18, 28, 47, 69, 71, 89, 100, 104, 161, 198, 206, 306, 321, 353, 371, 375, 392, 420, 434, 449 (20 parts). Part destroyed due to overstress caused by automatic microcircuit tester malfunction.

S/N's: 25, 107, 282, 366, 414, 458, 502, 533 (8 parts). Emitter-base leads of transistor Q_2 shorted and remained shorted after acceleration at 40,000 G in Y_1 axis.

S/N's: 32, 265, 288, 361, 362, 430, 473 (7 parts). Internal wire drooped down and touching conductor on substrate and edge of chip. Parts remained shorted after 40,000G acceleration in Y_1 axis.

S/N's: 1, 3 - Leads shorting to edge of chip.

S/N's: 14, 245 - Internal wire drooped down and touching conductor on substrate. Parts remained shorted after 40,000G acceleration in the Y_1 axis.

S/N's: 113, 380 - Failed due to leads drooping down and shorting. After Y_1 axis acceleration a wedge bond also became loose.

S/N 506 - Leads drooped down and shorting, but leads to Q_2 not shorted. After Y_1 axis acceleration emitter-base³ leads to Q_3 shorted.

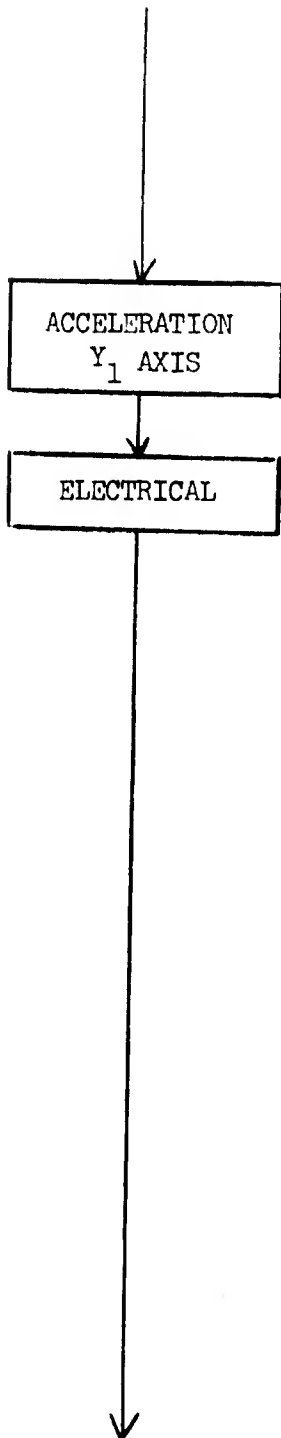
S/N 5 - Leads shorting to edge of chip and to conductor on substrate.

S/N 328 - Transistor chip Q_1 cracked.

S/N 530 - Loose internal gold wire wedge bond to aluminum metallization on resistor chip.

S/N 442 - Offset voltage drifted over maximum limit.

TEST GROUP NUMBER: 6



S/N 336 - Leads drooped down and shorted which cleared up after Y₁ axis acceleration at 40,000G but offset voltage remained over maximum drawing limit.

Per MIL-STD-883, Method 2001
40,000G Y₁ Axis, Cond. E
TOTAL QTY: 429

GO NO/GO Data Log Fails
TOTAL QTY: 429
TOTAL QTY. FAIL: 51
QTY. NEW FAILURES: 7 (1.63%)

S/N's: 14*, 18*, 25*, 28*, 32*, 42, 47*, 55,
69*, 71*, 89*, 100*, 104*, 107*,
113*, 127, 161*, 198*, 206*, 245*,
265*, 280, 282*, 306*, 321*, 328*,
339, 353*, 361*, 362*, 366*, 371*,
375*, 380*, 386*, 392*, 401, 414*,
420*, 430*, 434*, 442*, 445, 449*,
458*, 473*, 502*, 506*, 530*, 533*

S/N 386 - Left on test - other failures removed from test.

S/N's: 42, 55, 280, 506 - Emitter-base leads of transistor Q₃ shorted due to Y₁ axis acceleration moving leads after Y₂¹ axis acceleration.

S/N's: 380, 445 - Loose gold wire wedge bond to aluminum metalization on resistor chip.

S/N's: 113, 127 - Open wedge bond at neck down of gold wire.

S/N 339 - Open gold ball bond to gold conductor on substrate.

S/N 401 - Open gold ball bond to aluminum metalization on emitter of Q₁.

TEST GROUP NUMBER: 6

↓
FINE AND GROSS
SEAL TEST

Per MIL-STD-883, Method 1014
Condition A and C, Step 2
TOTAL QTY. FINE: 369
TOTAL QTY. FAIL: 6
QTY. NEW FAILURES: 5 (1.36%)

S/N's: 6, 249, 251, 315*, 365, 452

TOTAL QTY. GROSS: 369
TOTAL QTY. FAIL: 7
QTY. NEW FAILURES: 6 (1.63%)

S/N's: 6, 249, 273, 278, 289*, 452
505

↓
ELECTRICAL

GO NO-GO Data Log Failures At 25^o C,
-55 C, +125^o C.
TOTAL QTY: 369
TOTAL QTY. NEW FAIL at +25^o C: 8 (2.17%)

S/N's: 10, 63, 72, 84, 182, 312, 381,
503

S/N's: 10, 63, 312, 381 - Open gold
wire wedge bond going to aluminum
metalization on resistor chip.
S/N 72 - Two open gold wire wedge bonds
going to aluminum metalization on resistor
chip. Also, lead from pin 6 touching edge
of resistor chip.
S/N's: 84, 182, 503 - Open gold wire wedge
bond going to aluminum metalization of trans-
istor Q₂ emitter.

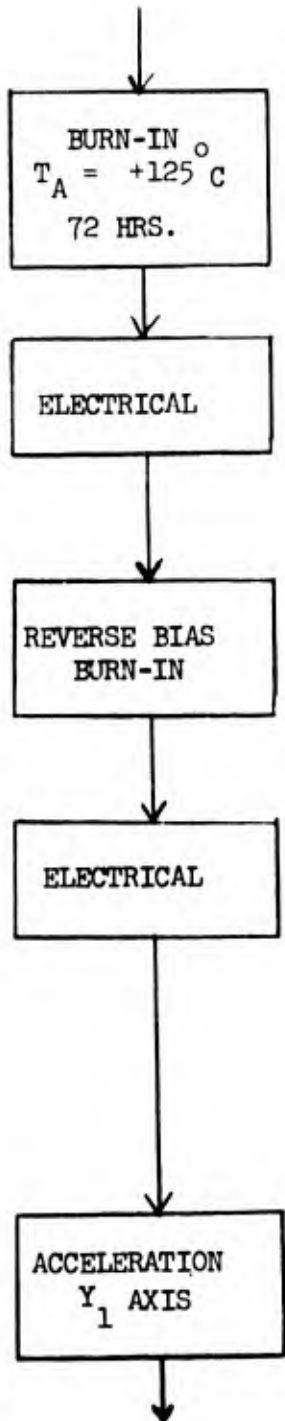
TOTAL QTY. FAIL AT -55^o C: 13
QTY. NEW FAILS: 3 (0.81%)

S/N's: 10*, 45, 63*, 72*, 84*, 182*, 187
312*, 381*, 386*, 403*, 503*, 538

S/N's: 45, 187, 538 - Series resistance
measures over maximum limit at -55 C

TOTAL QTY. FAIL AT +125^o C: 19
QTY. NEW FAILS: 10

TEST GROUP NUMBER: 6



Operating Life with Loads per
MIL-STD-883, Method 1015, Cond. D.
TOTAL QTY: 379

GO NO-GO Data Log Fails
TOTAL QTY: 376
QTY. FAIL: 0

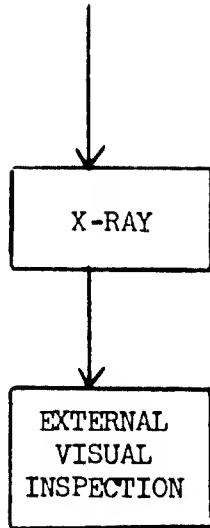
72 Hrs. @ +150 °C per MIL-STD-883,
Method 1015, Condition A
TOTAL QTY: 370

GO NO-GO Data Log Fails @ 25 °C

TOTAL QTY: +25 °C: 370
QTY. NEW FAIL: 1 (0.27%)
S/N 463 - Transistor Q₁ or Q₂ channeled

Per MIL-STD-883, Method 2001
40,000G, Y₁ Axis
TOTAL QTY: 369

TEST GROUP NUMBER: 6



S/N's: 10*, 63*, 72*, 84*, 182*,
312*, 381*, 403*, 503*

Per MIL-STD-883, Method 1012

TOTAL QTY: 20
QTY. FAIL: 0

Per MIL-STD-883, Method 2009

TOTAL QTY: 340
QTY. FAIL: 0

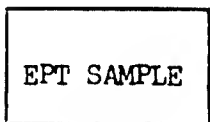
End of Class "A" Screening

TOTAL FALLOUT TO OBTAIN CLASS "A"
PARTS:

$$\frac{192}{542} = \underline{35.4\%}$$

TOTAL FALLOUT EXCLUDING INITIAL
ELECTRICAL TO OBTAIN CLASS "A" PARTS:

$$\frac{94}{444} = \underline{20.5\%}$$

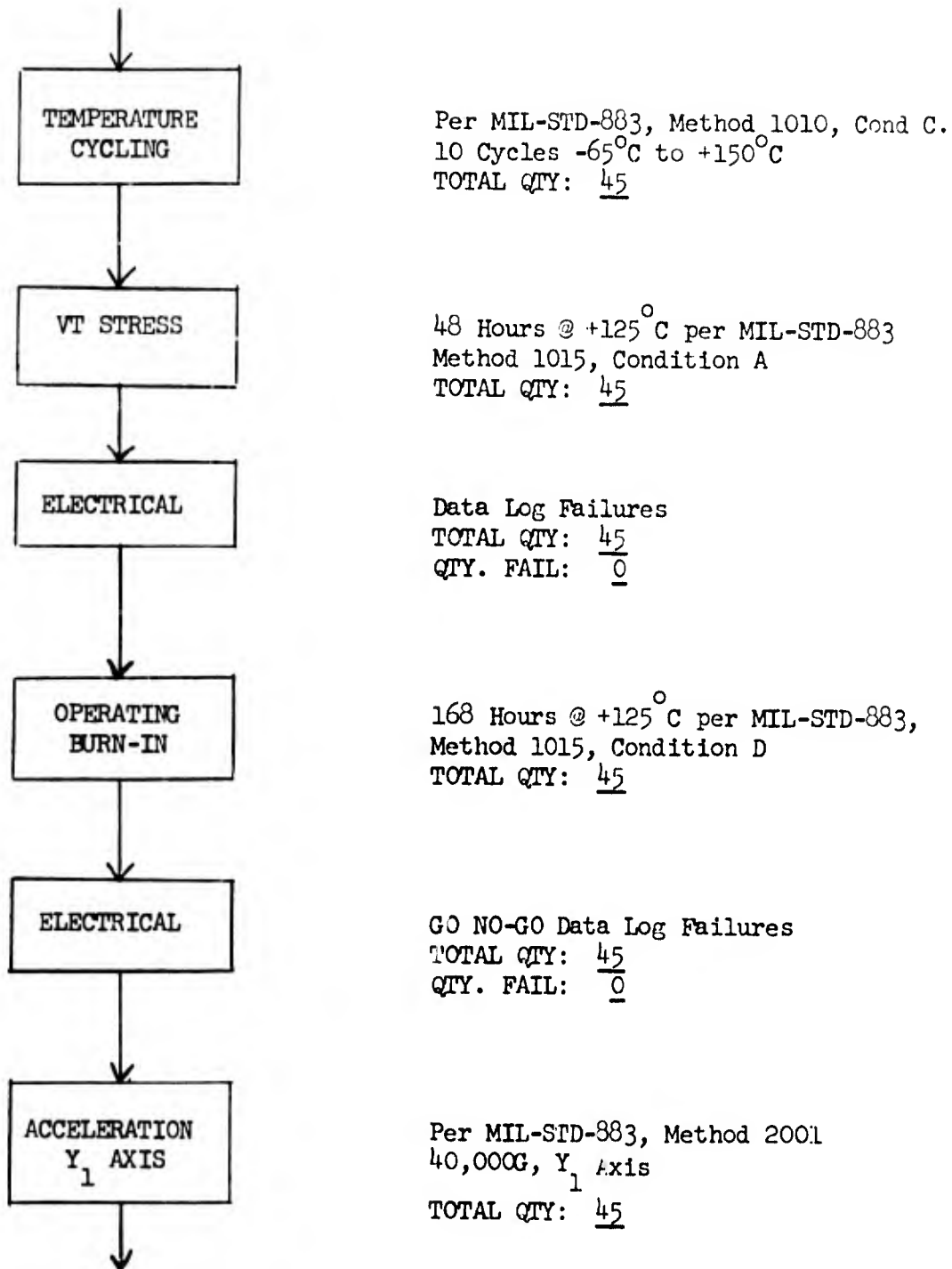


Quality Conformance Inspection
Sample Size 45,

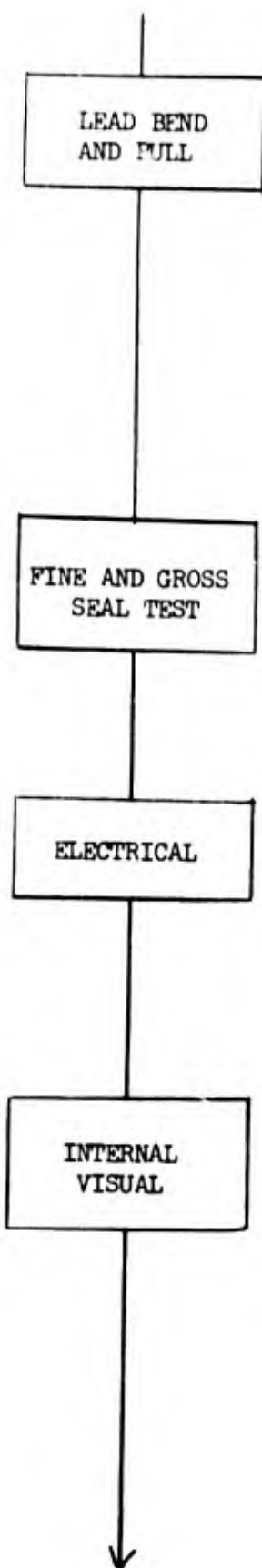
TOTAL QTY: 45

S/N's: 13, 27, 40, 49, 52, 59, 64, 75,
79, 91, 118, 121, 155, 164, 167,
194, 213, 207, 208, 219, 221, 240,
261, 268, 283, 303, 359, 367, 372,
374, 379, 384, 387, 395, 416, 419,
432, 440, 443, 488, 498, 515, 520,
529, 538

TEST GROUP NUMBER: 6



TEST GROUP NUMBER: 6



Pull per MIL-STD-883, Method 2004
Condition A (5 parts)
Pin Numbers: 1, 3, 5, 7, 9

S/N's: 13, 164, 167, 207, 384
QTY. FAIL: 0

Bend per EPT-800 on 5 parts
Pin Numbers: 2, 4, 6, 8, 10

S/N's: 13, 164, 167, 207, 384
QTY. FAIL: 0

FINE AND GROSS
SEAL TEST

Per MIL-STD-883, Method 1014
Conditions A and Step 2 of C
TOTAL QTY. FINE: $\frac{45}{0}$
QTY. FAIL: $\frac{0}{0}$
TOTAL QTY. GROSS: $\frac{45}{0}$
QTY. FAIL: $\frac{0}{0}$

ELECTRICAL

Data Log
TOTAL QTY: $\frac{45}{1}$ (2.22%)
QTY. FAIL: $\frac{1}{1}$ (2.22%)
S/N: 27

S/N 27 - Open gold wire wedge bond going to gold thick-film conductor on substrate.

INTERNAL
VISUAL

Decap six (6) parts
Visual inspection and bond pull tests
(12 wires pulled per S/N)
S/N's: 13, 27, 164, 167, 207, 384

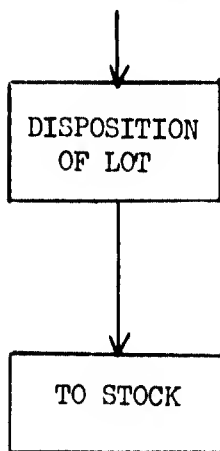
TOTAL QTY: $\frac{6}{3}$ QTY. FAIL: $\frac{3}{3}$
S/N's: 13, 27, 167

S/N 13 - Ball bond pulled at 1.0 gram; one wedge bond pulled at 0.7 gram, another pulled off at 1.2 grams.

S/N 27 - One wedge bond pulled off at 0.7 gram; another pulled off at 1.7 grams.

S/N 167 - One wedge bond pulled off at 1.6 grams.

TEST GROUP NUMBER: 6



Unopened EPT samples to be sold to production,

QTY. SOLD TO PRODUCTION: 38

QTY. RELEASED TO STOCK: 333

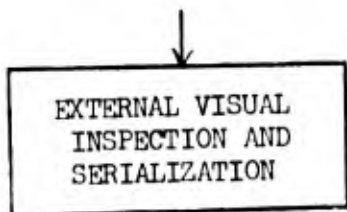
APPENDIX III G
DATA FROM TEST GROUP NO. 7

VERIFICATION PHASE TESTING
 FOR HYBRID CIRCUITS CONTRACT
 WITH RADC PER MIL-STD-883, METHOD 5004

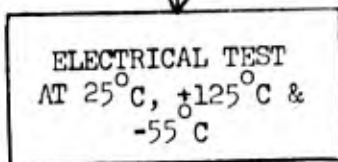
TEST GROUP NUMBER: 7
 SUPPLIER: C
 QUANTITY: 89
 RECEIVED: SEPT 1970

PART TYPE: LADDER SWITCH & DRIVER
 SERIAL NO's: 543 through 631
 DATE CODES: 7032, 7034

Class "C" Screening



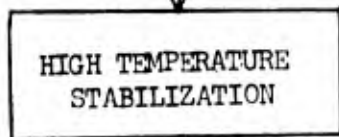
Place serial numbers on all samples and look for visual rejects at same time.
 QTY: 89



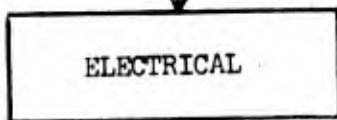
GO NO-GO testing and data log failures.
 TOTAL QTY. 25°C: 89
 QTY. FAIL 25°C: 0

TOTAL QTY. -55°C: 89
 QTY. FAIL -55°C: 2 (2.25%)

S/N's: 575, 614
 S/N's: 575, 614 - Fail maximum limit for series resistance at -55°C.
 TOTAL QTY. +125°C: 89
 QTY. FAIL +125°C: 0

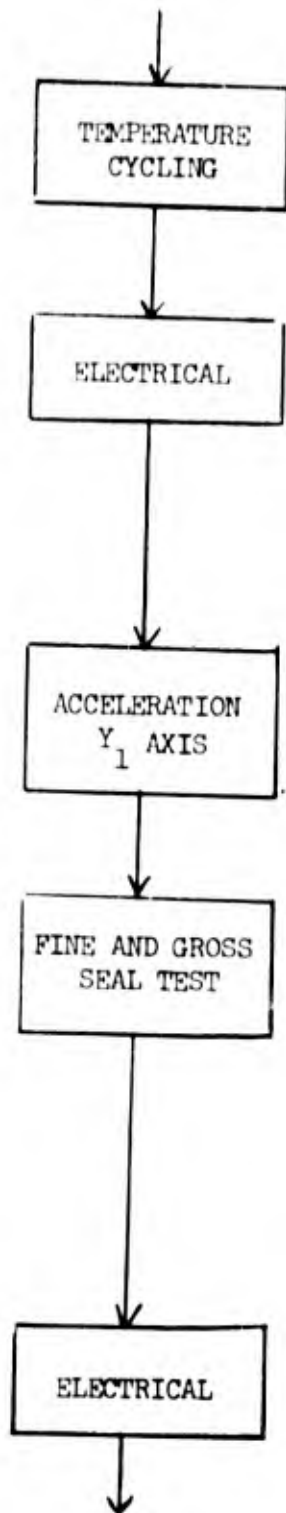


Per MIL-STD-883, Method 1003, Cond. C
 48 hours minimum @ +150°C
 QTY: 89



GO NO-GO data log failures
 TOTAL QTY: 89
 QTY. FAIL: 0

TEST GROUP NUMBER: 7



Per MIL-STD-883, Method 1010, Cond. C
10 Cycles, -65°C to +150°C
Transfer time less than 1 minute.
QTY: 89

GO NO-GO data log failures
TOTAL QTY: 89
QTY. FAIL: 1 (1.12%)

S/N's: 614 - Removed from test.
S/N 614 loose gold ball bond to
aluminum metalization on transistor.

Per MIL-STD-883, Method 2001; 30,000G
QTY: 88

Per MIL-STD-883, Method 1014, Conditions
A and C, Step 2. GO NO-GO fine leak
rate limit 1×10^{-7} ATM cc/sec.
TOTAL QTY: 88 (Seal Tested)
QTY. FAIL FINE: 6 (6.82%)

S/N's: 544, 555, 567, 569, 579, 601

QTY. FAIL GROSS: 2 (2.27%)
S/N's: 544, 567

Data log all failed units.
TOTAL QTY: 88
QTY. FAIL: 0

End of Class "C" screening procedures per MIL-STD-883, Method 5004.

TEST GROUP NUMBER: 7

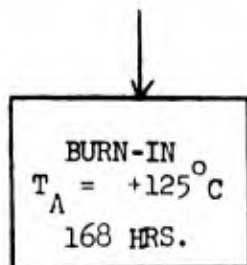
TOTAL CLASS "C" SCREENING FALLOUT:

$$\frac{8}{89} = \underline{9\%}$$

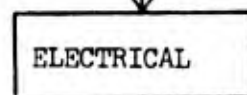
CLASS "C" FALLOUT EXCLUDING INITIAL ELECTRICAL FAILURES:

$$\frac{7}{89} = \underline{7.87\%}$$

Beginning of Class "B" Screening per MIL-STD-883, Method 5004



Per MIL-STD-883, Method 1015, Cond. D
QTY: 88



Data log all failed units.
TOTAL QTY: 88
QTY. FAIL: 0

End of Class "B" Processing

TOTAL FALLOUT TO GET CLASS "B" PARTS:

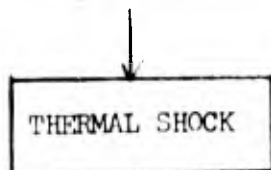
$$\frac{8}{89} = \underline{9\%}$$

FALLOUT TO GET CLASS "B" PARTS EXCLUDING INITIAL ELECTRICAL FAILURES:

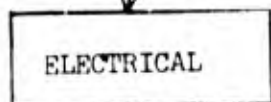
$$\frac{7}{89} = \underline{7.8\%}$$

TEST GROUP NUMBER: 7

Beginning of Class "A" Processing per MIL-STD-883, Method 5004

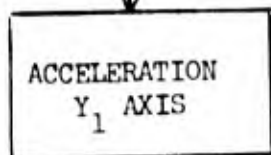


Liquid to liquid
TOTAL QTY: 88
Per MIL-STD-~~883~~⁸⁸³, Method ~~1011~~¹⁰¹¹, Cond C
15 Cycles, -65 C to +150 C

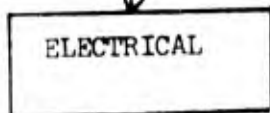


GO NO-GO Data Log Fails
TOTAL QTY: 88
QTY. NEW FAIL: 1 (1.14%)

S/N 572 - Series resistance drifted
over maximum limit.



Per MIL-STD-883, Method 2001
40,000 G, Y₁ Axis
TOTAL QTY: 1 88



GO NO-GO Data Log Fails
TOTAL QTY: 88
QTY. NEW FAIL: 6 (6.82%)

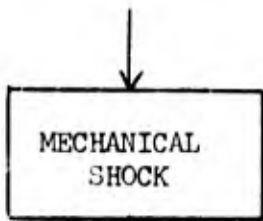
S/N's: 551, 566, 572, 587, 595, 602

S/N 551, 595 - Loose gold ball bond to
aluminum metalization on emitter of
transistor.

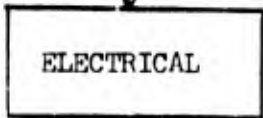
S/N's 566, 572 - Loose gold wedge bond
to aluminum metalization on emitter of
transistor Q₂.

S/N's 587, 602 - Loose transistor (Q₂) chip.

TEST GROUP NUMBER: 7



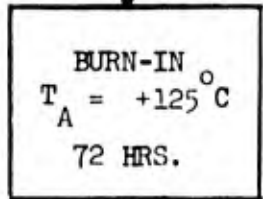
Per MIL-STD-883, Method 2002, Cond F
Y₁ Axis, One Shock; 20,000G Peak
TOTAL QTY: 82
QTY. DAMAGED: 0



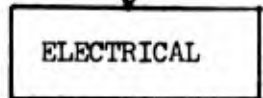
GO NO-GO Data Log Fails
TOTAL QTY: 82
QTY. NEW FAIL: 2 (2.44%)

S/N's: 568, 586

S/N's 568, 586 - Gold wire wedge bond
to aluminum metalization of emitter on
Q₂ open.

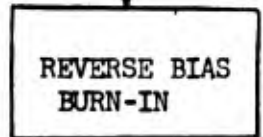


Operating life with loads per
MIL-STD-883, Method, 1015, Cond. D
TOTAL QTY: 79

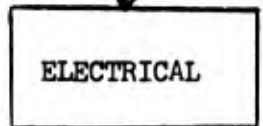


GO NO-GO Data Log Failures
TOTAL QTY: 79
QTY. NEW FAIL: 1 (1.22%)
S/N 588 - (Removed from test)

S/N 588 - Silicon particle shorting base
metalization to collector metalization
on transistor Q₃.

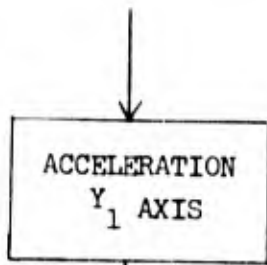


72 Hours @ +150° C per MIL-STD-883,
Method 1015, Cond. A
TOTAL QTY: 78

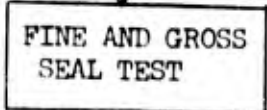


GO NO-GO
TOTAL QTY. +25° C: 78
QTY. FAIL: 0

TEST GROUP NUMBER: 7

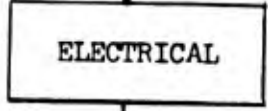


Per MIL-STD-883, Method 2001
40,000G; Y₁ Axis
TOTAL QTY: 78



Per MIL-STD-883, Method 1014
Conditions A and C, Step 2
TOTAL QTY. FINE: 78
TOTAL QTY. FAIL: 2
TOTAL NEW FAIL: 0
S/N's: 544*, 567*

TOTAL QTY. GROSS: 78
QTY. NEW FAIL: 1 (1.28%)
S/N 598



Data Log Failures
TOTAL QTY. +25°C: 78
QTY. NEW FAIL: 4 (5.13%)

S/N's: 565, 573, 584, 600

S/N's: 565, 584 - Open gold wire wedge bond to aluminum metalization on resistor chip.

S/N's: 573, 584, 600 - Open gold wire wedge bond to aluminum metalization at the emitter of Q₂.

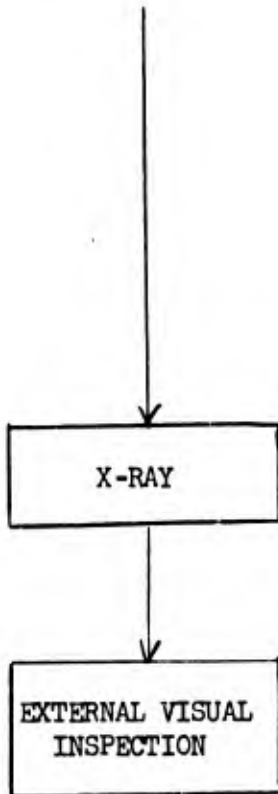
TOTAL QTY. -55°C: 78
QTY. FAIL: 8
QTY. NEW FAIL: 3 (3.85%)

S/N's: 565*, 573*, 576*, 577, 583, 584*, 592, 600*

S/N 577 - Offset voltage drifted over the maximum limit at -55°C.

S/N's 583, 592 - Series resistance drifted over the maximum limit at -55°C.

TEST GROUP NUMBER: 7



TOTAL QTY. +125^o C: 78
QTY. FAIL: 6
QTY. NEW FAIL: 2 (2.56%)

S/N's: 565*, 573*, 575, 584*, 600*, 628

S/N's: 575, 628 - Series resistance o
drifted over the maximum limit at +125 C.

Per MIL-STD-883, Method 1012
TOTAL QTY: 20
QTY. FAIL: 0

Per MIL-STD-883, Method 2009
TOTAL QTY: 63
QTY. FAIL: 0

End of Class "A" Screening

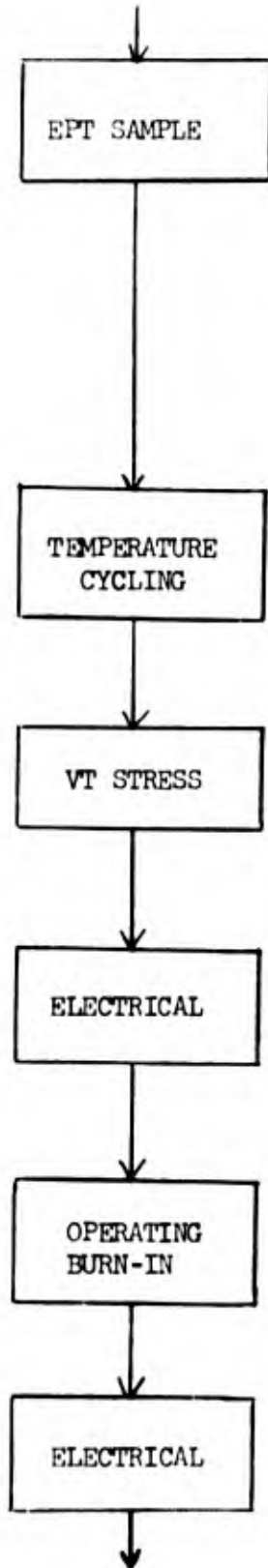
PERCENT FALLOUT TO OBTAIN CLASS "A"
PARTS:

$$\frac{27}{89} = \underline{30.4\%}$$

PERCENT FALLOUT EXCLUDING INITIAL
FAILURES:

$$\frac{27}{89} = \underline{30.4\%}$$

TEST GROUP NUMBER: 7



Quality Conformance Inspection

Sample size 34

TOTAL QTY: 34

S/N's: 546, 550, 553, 557, 560, 562,
563, 564, 570, 571, 581, 585,
589, 593, 594, 596, 597, 599,
603, 604, 605, 606, 607, 608,
610, 615, 616, 617, 618, 619,
620, 621, 625, 631

Per MIL-STD-883, Method 1010, Cond. C

10 Cycles -65°C to $+150^{\circ}\text{C}$

TOTAL QTY: 34

48 Hours @ $+125^{\circ}\text{C}$ per MIL-STD-883

Method 1015, Condition A

TOTAL QTY: 34

Data Log

TOTAL QTY: 34

QTY. FAIL: 0

168 Hours @ $+125^{\circ}\text{C}$ per MIL-STD-883

Method 1015, Condition D

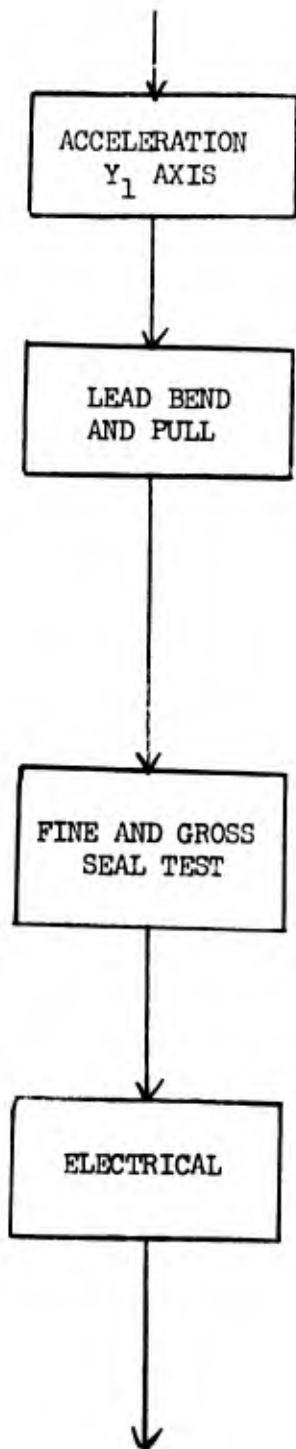
TOTAL QTY: 34

Data Log Failures

TOTAL QTY: 34

QTY. FAIL: 0

TEST GROUP NUMBER: 7



Per MIL-STD-883, Method 2001
40,000G; Y₁ Axis

TOTAL QTY: 34

Pull per MIL-STD-883, Method 2004
Condition A (4 parts)

Pull Lead No's: 1, 3, 5, 7, 9
S/N's of Parts: 581, 605, 620, 631
QTY. FAIL: 0

Bend per EPT-800 on 4 parts

Bend Lead No's: 2, 4, 6, 8, 10
S/N's of Parts: 581, 605, 620, 631
QTY. FAIL: 0

Per MIL-STD-883, Method 1014
Conditions A and Step 2 of C

TOTAL QTY. FINE: 34
QTY. FAIL: 0
TOTAL QTY. GROSS: 34
QTY. FAIL: 0

Data Log

TOTAL QTY: 34
QTY. FAIL: 1 (2.94%)
S/N 606

S/N 606 - Series resistance drifted
over the maximum limit due to a loose
gold wire wedge bond to the aluminum
metalization at the emitter of Q₂.

TEST GROUP NUMBER: 7

INTERNAL
VISUAL

Decap 5 parts
Visual inspection and bond pull
tests (12 wires per part pulled)

S/N's: 581, 605, 606, 620, 631

TOTAL QTY: 5 QTY. FAIL: 5
S/N's: 581, 605, 606, 620, 631

S/N 581 - Three gold wire wedge
bonds to aluminum metalization on
resistor chip broke at 0.6, 1.0
and 1.1 gms, respectively.

S/N 605 - Gold wire wedge bond to
aluminum metalization at emitter of
 Q_2 broke with no force. Gold wire
ball bond to aluminum metalization at
emitter of Q_1 pulled off at 1.7 gms.

S/N 606 - Gold wire wedge bond to
aluminum metalization at emitter of
 Q_2 open. Gold wire wedge bond to
aluminum metalization on resistor chip
broke at 1.7 gram. Gold wire ball
bond to emitter of Q_1 pulled off at 0.8
gram.

S/N 620 - Gold wire ball bond to base
of Q_1 pulled off at 0.9 gram. Gold
wire wedge bond to emitter of Q_2 broke
at 1.4 grams.

S/N 631 - Gold wire ball bond pulled
from emitter of Q_1 at 0.7 gram.

Unopened EPT samples to be sold to
production.

QTY. RELEASED TO STOCK: 58

DISPOSITION
OF LOT

TO STOCK

APPENDIX IIIH
DATA FROM TEST GROUP NO. 8

VERIFICATION PHASE TESTING
 FOR HYBRID CIRCUITS CONTRACT
 WITH RADC PER MIL-STD-883, METHOD 5004

TEST GROUP NUMBER: 8
 SUPPLIER: C
 QUANTITY: 87

PART TYPE: LADDER SWITCH & DRIVER
 SERIAL NOS: 1 through 542

NOTE: These parts were originally in Group No. 6 but were removed after the initial electrical tests, because they were marginally out-of-limit for an electrical parameter. Later they were put on test as test group number 8.

Class "C" Screening

EXTERNAL VISUAL
 INSPECTION AND
 SERIALIZATION

Place serial numbers on all samples and look for visual rejects at same time.

QTY: 87

ELECTRICAL TEST
 AT 25°C, +125°C
 AND -55°C

GO NO-GO testing and data log failures.

TOTAL QTY. 25°C: 87

QTY. FAIL 25°C: 23 (26.4%)

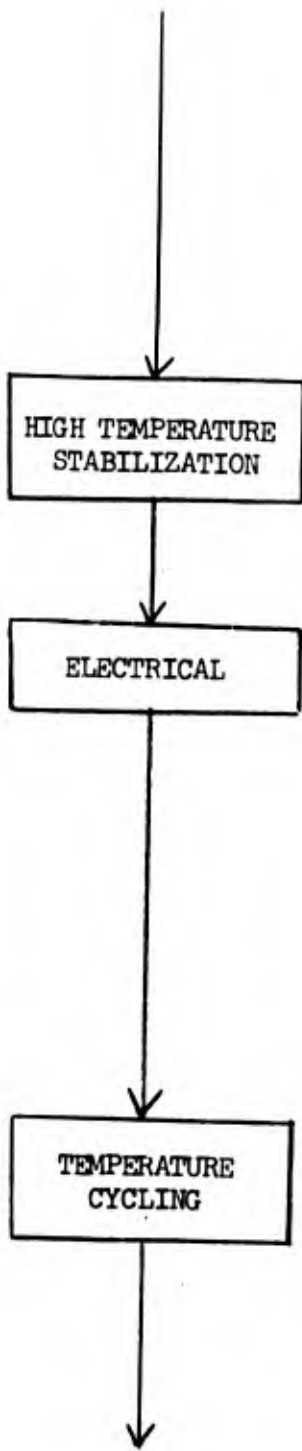
S/N's: 43, 51, 54, 93, 139, 185, 188,
190, 233, 237, 260, 329, 338,
343, 363, 413, 433, 435, 450,
451, 455, 490, 535

TOTAL QTY. -55°C: 87

TOTAL QTY. FAIL -55°C: 77 (88.5%)

S/N's: 8, 15, 24, 43*, 46, 51*, 54*, 58
60, 62, 77, 86, 101, 115, 117,
124, 130, 133, 135, 139*, 141,
143, 147, 152, 153, 156, 158,
163, 165, 174, 177, 183, 185*,
188*, 190*, 197, 220, 222, 227,
230, 231, 233*, 234, 237*, 242,
252, 260*, 270, 287, 290, 291, 300,
302, 309, 313, 325, 393, 396,
 (Continued next page)

TEST GROUP NUMBER: 8



S/N's: (Continued)

413*, 422, 433*, 447, 464,
474, 475, 486, 490*, 495, 509
514, 521, 525, 527, 531, 532,
534, 535*

TOTAL QTY. +125^o C: 87
QTY. FAIL +125 C: 0

Per MIL-STD-883, Method 1008, Cond. C
48 Hrs. minimum @ +150^o C.

QTY: 87

GO NO-GO data log failures.

TOTAL QTY: 87
TOTAL QTY. FAIL: 14
QTY. NEW FAIL: 1 (1.15%)

S/N's: 8, 51*, 93*, 233*, 260*, 338*,
343*, 363*, 433*, 435*, 450*,
451*, 455*, 490*

S/N 8 - Series resistance drifted over
maximum limit.

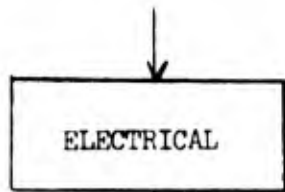
Per MIL-STD-883, Method 1010, Cond. C
10 Cycles, -65 C to +150 C

Transfer time less than one minute.

QTY: 87

*Indicates part failed earlier test

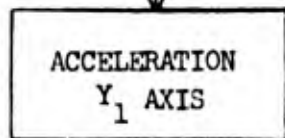
TEST GROUP NUMBER: 8



GO NO-GO data log failures

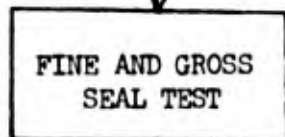
TOTAL QTY: 87
TOTAL QTY. FAIL: 17
QTY. NEW FAIL: 0

S/N's: 8*, 51*, 93*, 139*, 185*,
233*, 237*, 260*, 329*, 338*,
363*, 433*, 435*, 450*, 455*,
490*, 535*



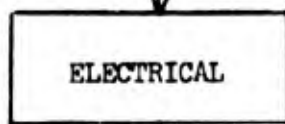
Per MIL-STD-883, Method 2001; 30,000 G

QTY: 87



Per MIL-STD-883, Method 1014, Cond. A and Condition C, Step 2. GO NO-GO fine leak rate limit 1×10^{-7} ATM cc/sec.

TOTAL QTY. SEAL TESTED: 87
QTY. FAIL FINE: 1 (1.15%)
S/N: 507 (4.7×10^{-7} atm cc/sec)
QTY. FAIL GROSS: 0



Data log all failed units.

TOTAL QTY: 87
TOTAL QTY. FAIL: 15
QTY. NEW FAILURES: 0

S/N's: 8*, 51*, 93*, 139*, 185*, 233*,
260*, 343*, 363*, 433*, 450*,
451*, 455*, 490*, 535*

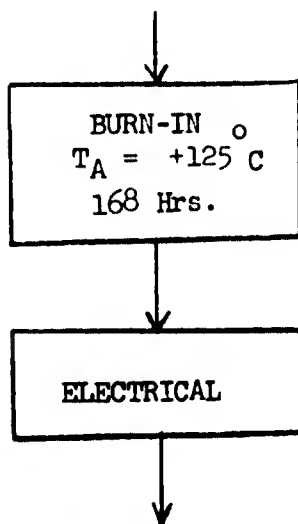
End of Class "C" Screening Procedures per MIL-STD-883, Method 5004

TOTAL FALLOUT INCLUDING INITIAL: 100%

TOTAL FALLOUT EXCLUDING INITIAL FAILURES: $2/87 =$ 2.3%

TEST GROUP NUMBER: 8

Beginning of Class "B" Screening per MIL-STD-883, Method 5004



Per MIL-STD-883, Method 1015, Cond D
QTY: 87

Data log all failed units.
TOTAL QTY: 87
QTY. FAIL: 0

End of Class "B" Processing

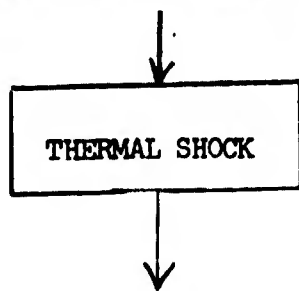
PERCENT FALLOUT TO GET CLASS "B"
PARTS:

$$\frac{87}{87} = \underline{100\%}$$

PERCENT FALLOUT EXCLUDING INITIAL
FAILURES TO GET CLASS "B" PARTS:

$$\frac{2}{87} = \underline{2.3\%}$$

Beginning of Class "A" Processing per MIL-STD-883, Method 5004



Liquid to Liquid
TOTAL QTY: 87
Per MIL-STD-883, Method 1011, Cond C
15 Cycles, -65 C to +150 C

TEST GROUP NUMBER: 8

ELECTRICAL

GO NO-GO Data Log Fails
TOTAL QTY: 87
TOTAL QTY. FAIL: 1
QTY. NEW FAILURES: 0
S/N: 490*

ACCELERATION
Y₁ AXIS

Per MIL-STD-883, Method 2001
40,000 G; Y₁ Axis
TOTAL QTY: 87

ELECTRICAL

GO NO-GO Data Log Fails
TOTAL QTY: 87
QTY. NEW FAIL: 1 (1.15%)
S/N: 435

S/N 435 - Open gold wire ball bond to aluminum metalization of transistor Q₁ emitter.

MECHANICAL SHOCK

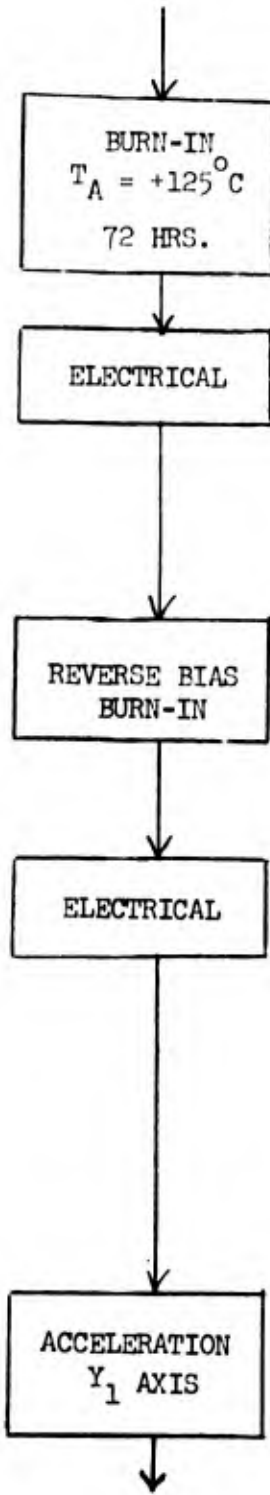
Per MIL-STD-883, Method 2002, Cond F
Y₁ Axis, One Shock; 20,000 G Peak
TOTAL QTY: 87
QTY. DAMAGED: 0

ELECTRICAL

GO NO-GO Data Log Fails
TOTAL QTY: 87
QTY. NEW FAIL: 1 (1.15%)
S/N: 514

S/N 514 - Gold wire wedge bond to aluminum metalization of emitter of Q₂ open.

TEST GROUP NUMBER: 8



Operating life with loads per
MIL-STD-883, Method 1015, Cond D
TOTAL QTY: 86

GO NO-GO Data Log Failures
TOTAL QTY: 86
QTY. FAIL: 3
QTY. NEW FAIL: 0

S/N's: 139*, 490*, 535*

72 Hours @ +150°C per MIL-STD-883,
Cond. A, Method 1015
TOTAL QTY: 86

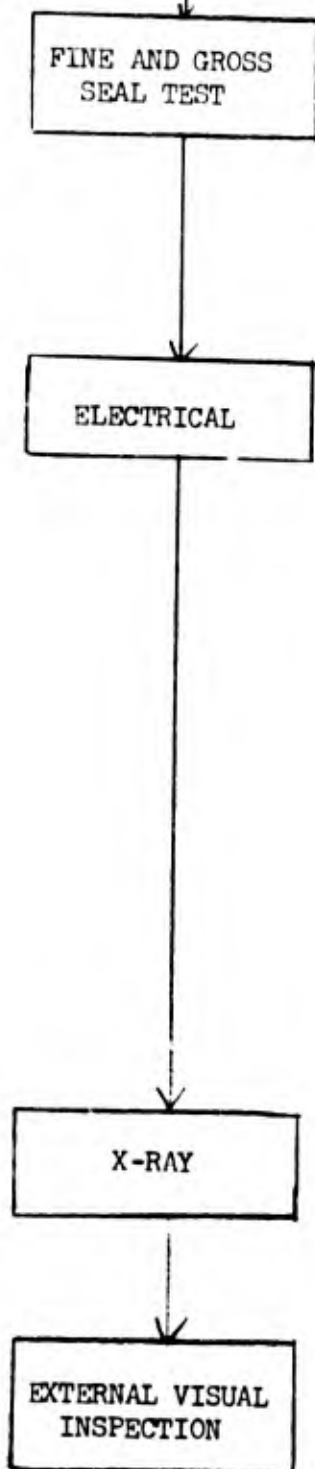
GO NO-GO
TOTAL QTY. +25C: 86
TOTAL QTY. FAIL: 16
QTY. NEW FAIL: 1 (1.41%)

S/N's: 8*, 51*, 54*, 93*, 139*, 158,
185*, 188*, 190*, 233*, 237*,
260*, 433*, 455*, 490*, 535*

S/N 158 - Series resistance drifted
over the maximum limit at 25°C.

Per MIL-STD-883, Method 2001
40,000 G; Y₁ Axis
TOTAL QTY: 86

TEST GROUP NUMBER: 8



Per MIL-STD-883, Method 1014
Conditions A and C, Step 2
TOTAL QTY. FINE: 86
QTY. NEW FAIL: 1 (1.16%)
S/N 338

TOTAL QTY. GROSS: 86
QTY. NEW FAIL: 1 (1.16%)
S/N 338

Data Log Failures
TOTAL QTY. +25°C: 86
QTY. NEW FAIL: 3 (3.49%)
S/N's: 234, 363, 413

S/N's 234, 363 - Open gold wire wedge bond to aluminum metalization on resistor chip.

S/N 413 - Open gold wire ball bond to aluminum metalization on resistor chip.

TOTAL QTY. -55°C = 86
TOTAL QTY. FAIL: 71
QTY. NEW FAIL: 0
S/N's: Too many to list

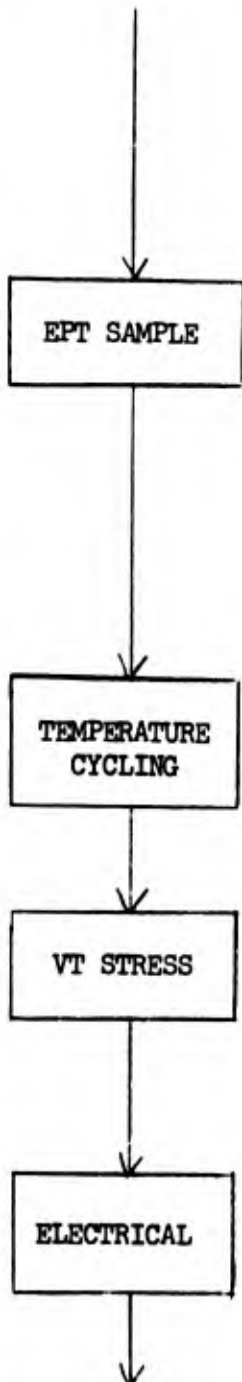
TOTAL QTY. +125°C: 86
TOTAL QTY. FAIL: 5
QTY. NEW FAIL: 2 (2.56%)
S/N's: 234*, 290, 363*, 413*, 447
S/N's 290, 447 - Series resistance_o drifted over maximum limit at +125 C.

Per MIL-STD-883, Method 1012
TOTAL QTY. 20
QTY. FAIL: 0

Per MIL-STD-883, Method 2009
TOTAL QTY: 83
QTY. FAIL: 0

TEST GROUP NUMBER: 8

End of Class "A" Screening



TOTAL FALLOUT TO GET CLASS "A" PARTS:

$$\frac{87}{87} = \underline{100\%}$$

PERCENT FALLOUT EXCLUDING INITIAL FAILURES TO OBTAIN CLASS A PARTS:

$$\frac{11}{87} = \underline{12.65\%}$$

Quality Conformance Inspection

Sample Size: 36
TOTAL QTY: 36

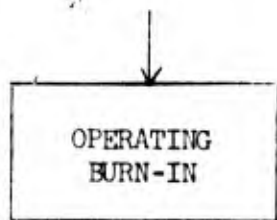
S/N's: 51, 147, 152, 153, 156, 163,
165, 177, 183, 197, 220, 222,
233, 237, 242, 252, 260, 270,
287, 291, 309, 313, 325, 393,
422, 433, 450, 486, 495, 509,
514, 521, 525, 527, 531, 534

Per MIL-STD-883, Method 1010, Cond.C
10 Cycles -65°C to +150°C
TOTAL QTY: 36

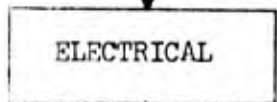
48 Hrs. @ +125°C per MIL-STD-883
Method 1015, Condition A
TOTAL QTY: 36

Data Log
TOTAL QTY: 36
QTY. FAIL: 1
QTY. NEW FAILURES: 0
S/N: 450*

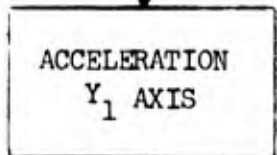
TEST GROUP NUMBER: 8



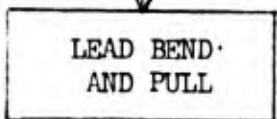
168 Hours @ +125°C per MIL-STD-883
Method 1015, Condition D
TOTAL QTY: 36



Data Log
TOTAL QTY: 36
QTY. FAIL: 0



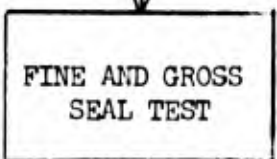
Per MIL-STD-883, Method 2001
40,000G; Y₁ Axis
TOTAL QTY: 36



Pull per MIL-STD-883, Method 2004
Condition A (4 parts)
Pull Lead No's: 1, 3, 5, 7, 9
S/N's Of Parts: 152, 163, 220, 525
QTY. FAIL: 0

Bend per EPT-300 on 4 Parts
Bend Lead No's: 2, 4, 6, 8, 10
S/N's Of Parts: 152, 163, 220, 525

QTY. FAIL: 0



PER MIL-STD-883, Method 1014,
Conditions A and Step 2 of C
TOTAL QTY. FINE: 36
QTY. FAIL: 0
TOTAL QTY. GROSS: 36
QTY. FAIL: 0

TEST GROUP NUMBER: 8

ELECTRICAL

INTERNAL
VISUAL

Data Log
TOTAL QTY: $\frac{36}{0}$
QTY. FAIL: $\frac{0}{0}$

Decap parts
Visual inspection and bond pull
tests (12 wires pulled per part)

S/N's: 152, 163, 220, 514, 525, 534

TOTAL QTY: $\frac{6}{5}$
QTY. FAIL: $\frac{5}{5}$

S/N's: 152, 163, 220, 525, 534

S/N 152 - Two gold wire wedge bonds going to aluminum metalization on resistor chip broke at neckdown at 0.5 and 1.6 grams, respectively.

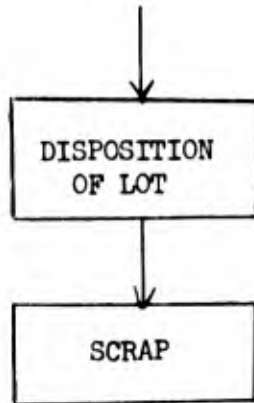
S/N 163 - Two gold wire wedge bonds going to aluminum metalization on resistor chip broke at neckdown at 1.8 and 2.0 grams, respectively.

S/N 220 - Gold wire ball bond to aluminum metalization on resistor chip pulled off with no force. Three gold wire wedge bonds going to aluminum metalization on resistor chip broke at neckdown at 1.3, 1.5 and 2.0 grams, respectively.

S/N 525 - Gold wire wedge bond to aluminum metalization on resistor chip broke at neckdown at 0.8 gram.

S/N 534 - Two gold wire wedge bonds to aluminum metalization on resistor chip broke at neckdown at 0.9 and 1.9 grams, respectively.

TEST GROUP NUMBER: 8



QTY. SOLD TO PRODUCTION: 0

All units failed initial electrical tests at 25 C and/or -55 C.

QTY. RELEASED TO STOCK: 0

APPENDIX IV

**FAILURE MECHANISM DETERMINATIONS BY TEST GROUP
RESULTING FROM
INCOMING INSPECTION, SCREENING TESTS, AND EPT TESTS**

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VERIFICATION PHASE TEST RESULTS - TEST GROUP NO. 1
(FAILURE MECHANISMS)

<p>Ⓘ Incoming Inspection - 32% (143) Fallout</p> <ul style="list-style-type: none"> 3 External leads missing 130 Fail electrical at 25°C 9 Fail electrical at +125°C 1 Fail gross seal <p>Ⓢ Class C Screening - 3.6% (11) Fallout</p> <ul style="list-style-type: none"> 7 Fail seal testing 2 Fail switching time maximum limit 1 Loose ceramic substrate 1 External lead fell off 1 Loose gold ball bond <p>Ⓣ Class B Screening (Operating Burn-In) - 1.00% (3) Fallout</p> <ul style="list-style-type: none"> 1 Diode reverse current increased over the maximum limit. 1 Circuit leakage current increased over the maximum limit. 1 Transistor collector-emitter shorted. <p>Ⓤ Class A Screening - 60.5% (176) Fallout</p> <ul style="list-style-type: none"> 105 Fail hermetic seal test 30 Package case apart 21 Loose ceramic substrate 	<p>Ⓡ Class A Screening (Cont.)</p> <ul style="list-style-type: none"> 11 Loose gold wedge bond to thick film conductor on substrate 11 Loose gold ball bond to aluminum metallization on semiconductor chip 8 Fail current source test limits 6 Switching time over maximum limit 3 Internal lead drooping down and shorting 3 Saturation voltage over the maximum limit 3 Loose transistor chip 3 Circuit leakage current over maximum limit 2 External lead fell off 2 Diode reverse current over the maximum limit 1 Internal lead wire bonded in wrong place causing lead to short <p>Total fallout including initial incoming tests - 74.33% (333)</p> <p>Ⓡ EFT Test Results (38 parts tested) - 6.3% (10) failed</p> <ul style="list-style-type: none"> 1 Transistor shorted 1 Fail lead bend test 9 Fail hermetic seal test 3 Bonds pulled at less than 2.0 grams (200 wires pulled)
--	--

VERIFICATION PHASE TEST RESULTS - TEST GROUP NO. 2

(FAILURE MECHANISMS)

I. Incoming Inspection - 6.44% (11) fallout

- 4 fail electrical at 25°C
- 6 fail electrical at -55°C
- 1 fail electrical at +125°C

II. Class C Screening - 5.63% (9) fallout

- 4 Fail gross hermetic seal test
- 2 External lead missing
- 1 Transistor collector to emitter short
- 1 Loose gold ball bond to aluminum metalization on semiconductor chip
- 1 Loose ceramic substrate

III. Class B Screening (Operating Burn-In) 0.61% (1) fallout

- 1 Circuit leakage current increased over the maximum limit

IV. Class A Screening - 77.5% (116) fallout

- 70 Fail hermetic seal test
- 31 Loose ceramic substrate
- 17 Leads drooped down due to Y₂ axis acceleration and shorted temporarily. Units passed after Y₁ axis acceleration redressed the leads.
- 10 Loose gold ball bond to aluminum metalization on semiconductor chip.
- 6 Package came apart
- 3 Loose gold wedge bond to thick film conductor on substrate
- 2 External lead missing
- 1 Fail diode leakage current maximum limit
- 1 Loose wedge bond to the external lead post
- 1 Loose diode chip
- 1 Fail circuit leakage current maximum limit at +125°C

Total Fallout including initial incoming tests - 80% (137)

V. EPT Test Results (30 parts tested) - 10% (3) failed

- 3 Fail gross hermetic seal test.

**VERIFICATION PHASE TEST RESULTS - TEST GROUP NO. 3
(FAILURE MECHANISMS)**

I.

- Incoming Inspection - 5.18% (10) Fallout
 - 10 Failed electrical at -55°C
 - 2 Failed electrical at +125°C

II.

- Class "C" Screening - 10.9% (20) Fallout
 - 20 Failed seal testing
 - 1 Two diffused resistor chips are loose

III.

- Class "B" Screening (Operating Burn-in) - 1.57% (3) Fallout
 - 1 Offset voltage increased over maximum limit
 - 1 Input current increased over maximum limit
 - 1 Circuit leakage current increased over the maximum limit

IV.

- Class "A" Screening 15.0% (29) Fallout
 - 6 Loose ceramic substrate
 - 3 Circuit leakage current increased over the maximum limit at 25°C.
 - 3 Internal leads drooped down and shorting to the edge of the semiconductor chips and also to the thick-film conductors on the substrate.
 - 3 Series resistance over the maximum limit at -55°C.
 - 3 Failed hermetic seal test

V.

- EFT Test Results (38 parts tested) - 5.26% (2) Fallout
 - 1 Gross hermetic seal failure
 - 1 Gold wire ball bond pulled off at 0.2 gram from aluminum metallization of transistor.

- 2 Loose gold wire wedge bond to gold thick-film conductor on substrate.
 - 1 Loose resistor chip
 - 1 Loose transistor chip
 - 1 Input zero current increased over the maximum limit.
 - 1 Part has solid material inside of package as if liquid was in package and it became a solid.
 - 1 Series resistance increased over the maximum limit at 25°C.
 - 1 Internal leads drooped down and shorting at -55°C and +125°C only.
 - 1 Leads drooped down and shorting at +125°C only.
 - 1 Loose wedge bond to thick-film gold conductor on substrate and loose gold ball bond to pin 2 gold-plated post.
 - 1 External lead fell off.

VERIFICATION PHASE TEST RESULTS - TEST GROUP NO. 4

(FAILURE MECHANISMS)

- I. Incoming Inspection - 1.63% (5) Fallout
5 Fail electrical tests at -55°C .
- II. Class C Screening - 6.85% (21) Fallout
21 Fail hermetic seal test.
1 Offset voltage increased over maximum limit.
- III. Class B Screening (Operating Burn-In) 1.64% (5) Fallout
1 Offset voltage, series resistance and circuit leakage current increased over the maximum limit.
1 Input offset voltage drifted over the maximum limit.
1 Input currents increased over maximum limit.
1 Emitter-base leads of transistor shorted.
1 Part shorted due to loose metallic particle.
- IV. Class A Screening - 7.5% (23) Fallout
11 Fail hermetic seal test.
3 Loose wedge bond to thick film conductor on substrate.
2 Series resistance increased over the maximum limit at 25°C .
2 Offset voltage and series resistance increased over the maximum limit at -55°C .
2 Offset voltage and series resistance increased over the maximum limit at $+125^{\circ}\text{C}$.
1 Circuit leakage current increased over the maximum limit at 25°C .
1 Offset voltage increased over the maximum limit at 25°C .
1 Open gold ball bond to aluminum metallization on transistor chip.
- V. EPT Test Results (40 parts tested) - 2.5% (1) failed
1 Bond pulled at 2.0 grams (80 wires pulled and all other wires passed 2 grams pull).

VERIFICATION PHASE TEST RESULTS - TEST GROUP NO. 5 (FAILURE MECHANISMS)

I. Incoming Inspection - 1.4% (7) Fallout

- 2 fail electrical at 25°C
- 5 fail electrical at +125°C

II. Class C Screening - 11.1% (55) Fallout

- 43 fail hermetic seal test
- 5 circuit leakage current increased over max. limit
- 2 loose resistor chip
- 2 series resistance increased over max. limit
- 2 power supply current I_{CC}"0" increased over maximum limit
- 1 switching time increased over maximum limit
- 1 scratched aluminum metalization shorting collector-base of transistor

III. Class B Screening (Operating Burn-In) - 0.23% (1) Fallout

- 1 failure caused by holes in silicon oxide under aluminum termination for the nichrome resistors causing them to short through the silicon substrate.

IV. Class A Screening - 15.8% (69) Fallout

- 32 fail hermetic seal test
- 24 fail at 25°C due to 40,000 g acceleration in Y₂ axis which caused the internal leads to droop and short. (These parts remained on test and the shorts went away during 40,000 g acceleration in the Y₁ axis.
- 23 series resistance increased over the maximum limit (25°C)
- 16 fail at +125°C due to 40,000 g acceleration in Y₂ axis which caused the internal leads to droop and short at +125°C but not at 25°C or -55°C. (These parts remained on test and the shorts went away during 40,000 g acceleration, in the Y₁ axis).
- 13 series resistance slightly over maximum limit at +125°C (marginal units)
- 5 loose resistor chip
- 5 lead drooping down and shorting to thick film conductor on substrate
- 2 circuit leakage current increased over the maximum limit
- 2 loose gold ball bond to aluminum metalization on semiconductor chip
- 2 device channeled and destroyed internal leads from high leakage current
- 1 power supply drain current increased over the maximum limit
- 1 package broke in mechanical shock
- 1 lead shorting to edge of transistor chip
- 1 internal leads shorting together

Total Fallout including Initial Tests - 26.5% (132)

V. EPT Test Results (45 parts tested) - 6.67% (3) failed

- 2 fail gross hermetic seal test
- 1 internal wedge bond pulled off at 0.8 gram (65 wires pulled)

**VERIFICATION PHASE TEST RESULTS - TEST GROUP NO. 6
(FAILURE MECHANISMS)**

<p>I. Incoming Inspection - 16.1% (90) Failout</p> <p>33 Failed electrical test at 25°C.</p> <p>96 Failed electrical test at -55°C.</p> <p>II. Class "C" Screening - 2.26% (10) Failout</p> <p>4 Failed hermetic seal test</p> <p>2 Transistor chip loose from substrate</p> <p>2 Resistor chip loose from substrate</p> <p>2 Series resistance marginally over the maximum limit at 25°C.</p> <p>III. Class "B" Screening (Operating Burn-in) - 0 Failout</p> <p>IV. Class "A" Screening - 14.8% (65) Failout</p> <p>11 Loose gold wire because wedge bond broke at neckdown where wire went to aluminum metallization.</p> <p>8 Failed hermetic seal test</p> <p>4 Emitter-base leads of transistor T_3 shorted due to Y_1 axis acceleration moving leads after Y_2 axis acceleration.</p> <p>3 Open gold ball bond to aluminum metallization on transistor emitter.</p> <p>3 Series resistance drifted over the maximum 25°C limit.</p> <p>3 Series resistance drifted over the maximum -55°C limit.</p> <p>2 Resistor chip loose from substrate.</p> <p>2 Open gold wire ball bond to thick-film gold on substrate.</p> <p>1 Open gold wire ball bond to aluminum metallization on resistor chip and open wedge bond and neckdown of gold wire to aluminum metallization on transistor.</p> <p>1 Transistor chip loose from substrate.</p> <p>1 Offset voltage drifted over maximum limit.</p> <p>1 Leads drooped down and shorted which cleared up after Y_1 axis acceleration at 40,000 G, but offset voltage remained over maximum drawing limit.</p> <p>1 Circuit leakage drifted over maximum 25°C limit.</p>	<p>1 Transistor channeled (high leakage current) due to reverse bias burn-in.</p> <p>1 Two open gold wire wedge bonds at neckdown where wire goes to aluminum metallization. Also, lead from pin 6 touching edge of resistor chip.</p> <p>Failures due to Y_2 axis acceleration at 3,000 G:</p> <p>4 Failed due to drooped leads causing shorts but passed after 40,000 G acceleration in the Y_1 axis. (Note: These were not counted as part of the failout.)</p> <p>20 Part destroyed due to overstress caused by automatic micro-circuit tester malfunction. (Notes: These were not counted as part of the failout.)</p> <p>6 Emitter-base leads of transistor T_3 shorted and remained shorted after acceleration at 40,000 G in Y_1 axis.</p> <p>7 Internal wire drooped down and touching conductor on substrate and edge of chip. Parts remained shorted after 40,000 G acceleration in Y_1 axis.</p> <p>2 Leads shorting to edge of chip.</p> <p>2 Internal wire drooped down and touching conductor on substrate. Parts remained shorted after 40,000 G acceleration in the Y_1 axis.</p> <p>2 Failed due to leads drooping down and shorting. After Y_1 axis acceleration a wedge bond also became loose.</p> <p>1 Leads drooped down and shorting, but leads to T_3 not shorted. After Y_1 axis acceleration emitter-base leads to T_3 shorted.</p> <p>1 Leads shorting to edge of chip and to conductor on substrate.</p> <p>1 Transistor chip T_1 cracked.</p> <p>1 Loose internal gold wire wedge bond to aluminum metallization on resistor chip.</p>
	<p>V. EPR Test Results (45 parts tested) - 6.67% (3) Failout</p> <p>1 Open gold wire wedge bond at neckdown of wire going to gold thick-film conductor on substrate.</p> <p>1 Gold wire ball bond pulled off at 1.0 gram.</p> <p>5 Gold wire wedge bonds broke at neckdown of wire at 1.7 grams and less.</p>

VERIFICATION PHASE TEST RESULTS - TEST GROUP NO. 7

(FAILURE MECHANISMS)

<p>I. Incoming Inspection - 2.25% (2) Fallout 2 Failed electrical test limit at -55°C.</p> <p>II. Class "C" Screening - 7.87% (7) Fallout 6 Failed hermetic seal test 1 Loose gold wire ball bond to aluminum metallization on transistor.</p> <p>III. Class "B" Screening (Operating Burn-in) - 0 Fallout</p> <p>IV. Class "A" Screening 22.8% (20) Fallout 7 Loose gold wire due to wedge bond breaking at neckdown going to aluminum metallization of emitter on transistor Q_2. 2 Loose gold ball bond to aluminum metallization on emitter of transistor. 2 Loose gold wire due to wedge bond breaking at neckdown going to aluminum metallization on resistor chip. 2 Loose transistor chip. 2 Series resistance drifted over the -55°C maximum limit. 2 Series resistance drifted over the +125°C maximum limit. 1 Series resistance drifted over the +25°C maximum limit. 1 Silicon particle shorting base metallization to collector metallization on transistor Q_3. 1 Fail gross hermetic seal test. 1 Offset voltage drifted over the -55°C maximum limit.</p>	<p>V. EFT Test Results (34 parts tested) 14.7% (5) Fallout 1 Loose gold wire due to wedge bond breaking at neckdown going to aluminum metallization of emitter. 1 Three gold wire wedge bonds to aluminum metallization on resistor chip broke at 0.6, 1.0 and 1.1 gms, respectively. 1 Gold wire wedge bond to aluminum metallization at emitter of Q_2 broke with no force. Gold wire ball bond to aluminum metallization at emitter of Q_1 pulled off at 1.7 gms. 1 Gold wire wedge bond to aluminum metallization at emitter of Q_2 open. Gold wire wedge bond to aluminum metallization on resistor chip broke at 1.7 gms. Gold wire ball bond to emitter of Q_1 pulled off at 0.8 gram. 1 Gold wire ball bond to base of Q_1 pulled off at 0.9 gram. 1 Gold wire wedge bond to emitter Q_2 broke at 1.4 grams. 1 Gold wire ball bond pulled from emitter of Q_1 at 0.7 gram.</p>
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**VERIFICATION PHASE TEST RESULTS - TEST GROUP NO. 8
(FAILURE MECHANISMS)**

<p>I. Incoming Inspection - 100% (87) Failout</p> <p><u>Note:</u> These parts were originally in Group No. 6 but were removed after the initial electrical tests, because they were marginally out-of-limit for an electrical parameter. Later they were put on test as test group number 3.</p> <p>77 Failed electrical test at -55°C.</p> <p>23 Failed electrical test at $+25^{\circ}\text{C}$.</p> <p>II. Class "C" Screening - 2.3% (2) Failout</p> <p>1 Series resistance drifted over the maximum limit at 25°C.</p> <p>1 Fail fine hermetic seal test</p> <p>III. Class "B" Screening (Operating Burn-in) - 0 Failout</p> <p>IV. Class "A" Screening - 10.3% (9) Failout</p> <p>2 Gold wire wedge bond broken at neckdown where it goes to the aluminum metalization on the resistor chip.</p> <p>2 Series resistance drifted over the $+125^{\circ}\text{C}$ maximum limit.</p> <p>1 Open gold wire ball bond to aluminum metalization on transistor Q_1 emitter.</p> <p>1 Gold wire wedge bond broken at neckdown where it goes to the aluminum metalization on the emitter of transistor Q_2.</p> <p>1 Series resistance drifted over the maximum limit at $+25^{\circ}\text{C}$.</p> <p>1 Fail hermetic seal test</p> <p>1 Open gold wire ball bond to aluminum metalization on resistor chip.</p>	<p>V. EPT Test Results (36 parts tested) 17.7% (5) Failout</p> <p>1 Two Gold wire wedge bonds going to aluminum metalization on resistor chip broke at neckdown at 0.3 and 1.6 grams, respectively.</p> <p>1 Two gold wire wedge bonds going to aluminum metalization on resistor chip broke at neckdown at 1.3 and 2.0 grams, respectively.</p> <p>1 Gold wire ball bond to aluminum metalization on resistor chip pulled off with no force. Three Gold wire wedge bonds going to aluminum metalization on resistor chip broke at neckdown at 1.3, 1.5 and 2.0g respectively.</p> <p>1 Gold wire wedge bond to aluminum metalization on resistor on resistor chip broke at neckdown at 0.3 gram.</p> <p>1 Two Gold wire wedge bonds to aluminum metalization on resistor chip broke at neckdown at 0.9 and 1.9 grams, respectively.</p>
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