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SAMSO-TR-72-213

SYSTEM 621B USER EQUIPMENT DEFINITION AND EXPERIMENTS PROGRAM

TASK VI - PHASE II ALTERNATE RECEIVER FINAL REPORT

Leonard J. Jacobson

Magnavox Research Laboratories

TECHNICAL REPORT SAMSO-TR-72-213

December 1972

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Final Report

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F.P. Paterno
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SAMSO-TR-72-213

SYSTEM 621B USER EQUIPMENT DEFINITION AND EXPERIMENTS PROGRAM

TASK VI - PHASE II ALTERNATE RECEIVER FINAL REPORT

Leonard J. Jacobson

FOREWORD

This report, dated December 1972, contains the results of a program titled "System 621B User Equipment Definition and Experiments Program, Task VI - Phase II Alternate Receiver." The work was accomplished by the Magnavox Research Laboratories, Torrance, California, at Torrance, and at the White Sands Missile Test Range, Holloman AFB, New Mexico, and complies with all requirements of Contract Number F04701-71-C-0318.

The report is published in one volume under Magnavox Report Number R-4490. The USAF Report Number is SAMSO-TR-72-213. Capt Donald Wilson, SAMSO Code XRLO, was the program monitor. The period of performance covered by this report is from 71 May 1 to 72 Nov 30.

Significant assistance was received from Messrs. D. Cnossen, L. Seidl, F. Charles, B. Glazer and M. Taylor, all of whom contributed to this report.

Publication of this report does not constitute Air Force approval of the report's findings or conclusions. It is published only for the exchange and stimulation of ideas.

VALENTINE L DENNINGER, Maj, USAF
NAV SAT Development Engineer
Orbital Division

ABSTRACT

System 621B is a concept for a highly accurate, satellite-navigation system which enables any number of users anywhere on the globe to determine in real time, their position and velocity in three dimensions. The most important performance parameter of this system is the degree of navigational accuracy which is provided the users. This accuracy and other pertinent performance characteristics depend to a large extent upon the chosen orbit configuration and the resulting geometry between the user and the satellites. However, it has been necessary to evolve user navigation receiver designs capable of performing within the system constraints and which contribute negligibly to the overall system accuracy degradation. It is the purpose of this report to document one such receiver design, designated to the MX-450 Navigation Receiver, which was developed to further refine and verify the predicted performance of System 621B.

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INTRODUCTION

1.1 GENERAL

There were two major objectives to be achieved in order to successfully complete the airborne receiver development phase of the Task VI - Phase II Field Test Program. First, it was necessary to verify in the laboratory that the receiver could meet the performance requirements associated with a highly dynamic user, such as an F4 high performance jet aircraft, operating in a low-signal-power, high-jamming environment. The second objective, and one which was of central importance to the System 621B program, was to demonstrate in a field environment simulating an operational satellite configuration that the receiver could in fact measure pseudo-range and range rate within the allocated error budget.

The first objective was successfully achieved prior to the shipment of the receiver to Grumman Aerospace Corp., Bethpage, Long Island, to support their System Integration Test which commenced the last week of November, 1971. In fact, the results of simulated testing in the laboratory at MRL during the latter part of 1971 showed that the receiver's performance met or exceeded performance requirements specified by the Government. (See Receiver General Requirements - appendix C. This performance was officially verified and accepted on behalf of the Government by SAMSO/Aerospace Corp. personnel on 11 November 1971. Since that time, the receiver has operated both in the laboratory and during the flight tests.

The second objective was achieved by participating with the Grumman Aerospace Corp., in the flight test program conducted at Holloman Air Force Base, New Mexico, and at nearby White Sands Missile Range.

1.2 OVERVIEW OF THE RECEIVER FUNCTIONAL DESIGN

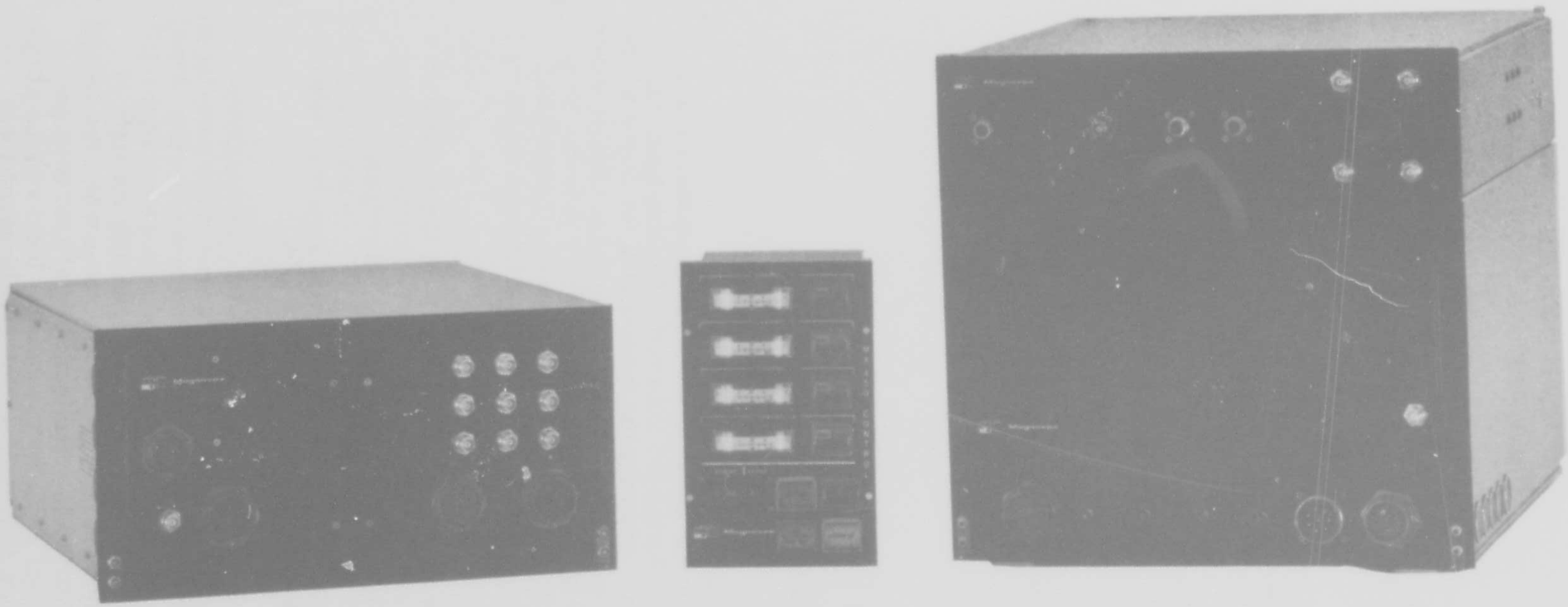
The MX-450 Navigation Receiver was designed to acquire, track, and process a composite signal consisting of four unique pseudonoise (PN) modulated, L-Band-carrier signals for the purpose of deriving very accurate estimates of signal arrival times and doppler frequencies relative to a local frequency-time standard. These pseudo-range and range-rate measurements are combined with various receiver status indicators (such as automatic gain control levels) and formatted in a manner suitable for transfer to an incremental digital tape recorder for subsequent off-line data reduction and processing. It is worthy of note that while the receiver/tape recorder interface is a custom design and implemented in a modular sense to be an integral part of the signal processor package, it can readily be adapted and/or changed to satisfy a wide variety of interface requirements with no particular impact on the receiver design.

The receiver was designed and fabricated to withstand the environmental rigors associated with actual flight testing in the field. Figure 1 illustrates the physical appearance and dimensions of the various units which comprise the receiver and associated peripheral equipments. During the development phase it was not considered essential to optimize the packaging concept. However, if it were necessary and/or desirable, a significant reduction in the volume required for the receiver could be achieved by the use of custom designed power supplies and an integrated microwave package.

As an alternate receiver, it was necessary to constrain some of the receiver design electives in order to accommodate the transmitter design implemented by the field test contractor. In particular, it was necessary to conform to his choice of pseudonoise code design and at least partially conform to the method selected at the transmitter for accomplishing initial signal acquisition at the receiver. A typical transmitter signal consists of an L-Band carrier biphase modulated at a 10-Mbps rate with a pseudorandom code sequence. This code sequence has a period of 2^{25} bits so that it repeats approximately every 3.36 seconds. The initial signal acquisition technique chosen by the field test contractor is implemented at his transmitter by inserting a special 255-bit sequence at the beginning of the transmit period and transmitting at a boosted power level for the duration of this special short sequence in order to allow him to perform matched filter detection upon reception. Immediately following this short sequence, the last 2^{25} -255 bits of a long code generated by a 25-stage, maximal-length, linear-code generator is transmitted at nominal power level. Since the initial acquisition procedure was selected on the basis of contractor convenience in accordance with the ground rules established by SAMSO, the Magnavox Research Laboratories elected to implement at their receiver a rather inexpensive but very effective radiometric type detection technique to detect the increase in receiver power during the 25-microsecond period of power boosted initial sync signal. The relatively small amount of initial time uncertainty remaining after the detection of power boost is resolved by means of a short reacquisition search. Finally, each of the transmitter long codes are generated by a sequence generator with different feedback arrangements which uniquely identifies each individual emitter and which in turn, permits each of the four signal processors in the airborne receiver to track only the intended transmitter signal.

Figure 2 illustrates the essential functions performed by the L-band microwave receiver. The incoming 1575-MHz composite signal is first bandpass filtered by the fixed-tuned preselector prior to radio-frequency amplification. The preselector's frequency response is less than 1 dB down within 10 MHz, 3 dB down within 15 MHz and 80 dB down within 60 MHz of the center frequency. The preamplifier has a noise figure of approximately 3.5 dB and provides a signal gain of 30 dB. The down-converter generates the 135-MHz, intermediate-frequency signal by mixing the received 1575-MHz signal with the 1440-MHz, local-oscillator signal. This 1440-MHz signal is derived from a fixed-reference frequency by means of a phase-lock multiplier which helps to ensure the generation of a local-oscillator signal characterized by a high degree of spectral purity.

The 135-MHz, intermediate-frequency module performs three essential functions within the receiver. Two of these functions satisfy the need to provide a controlled intermediate-frequency gain prior to correlation; namely noncoherent (or total power) agc and what will be referred to as max-channel coherent agc. Since noncoherent agc is required in any case, it is a relatively simple extension to detect the increase in total receiver power level during the 25-microsecond power boost



SIGNAL PROCESSOR

DIAM.	15" X 18" X 8"
VOL.	1.25 CU. FT.
WT.	36 LBS.

CONTROL DISPLAY PANEL

DIAM.	5-3/4" X 4-1/2" X 9"
VOL.	.135 CU. FT.
WT.	4-1/2 LBS.

MICROWAVE RECEIVER

DIAM.	15" X 18" X 4"
VOL.	0.625 CU. FT.
WT.	16-1/4 LBS.

POWER SUPPLIES

DIAM.	15" X 8" X 9"
VOL.	1.4 CU. FT.
WT.	88 LBS

Figure 1. MX-450 Navigation Receiver.

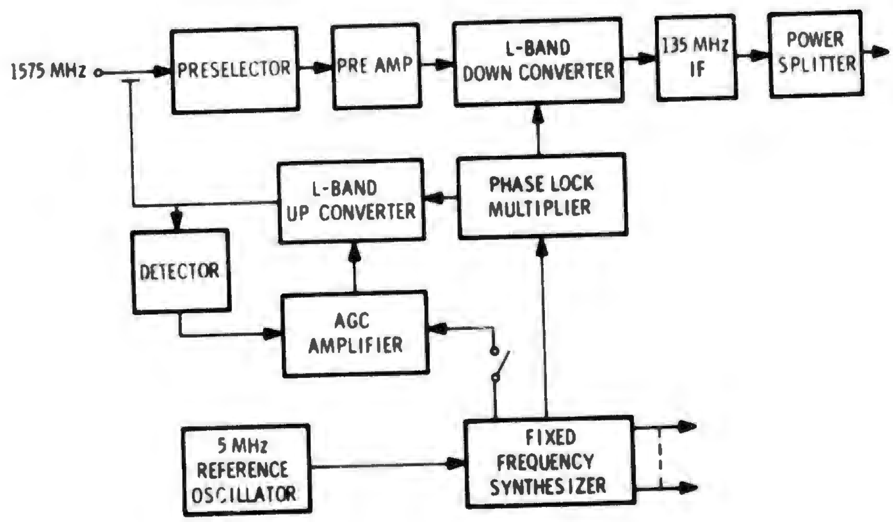


Figure 2. L-Band Microwave Receiver

period by ac coupling the output of the square-law detector in the noncoherent agc loop to a threshold device. For example, during the long-code, transmit period, the agc square-law detector will effectively see only the front-end noise power at -96 dBm since the received signal level will be at the nominal level of -123 dBm or lower. When the power-boost signal is received at -100 dBm the square-law detector sees an apparent increase of approximately 33 percent in the total receiver power level for 25 microseconds which is more than adequate for the threshold device to detect signal presence reliably.

The remaining functions shown in figure 2 have to do with the calibration and self-test of the receiver. In either of these modes the switch closure provides either a modulated or unmodulated 135-MHz signal as desired. This signal is up converted to 1575 MHz and applied to the preselector input through a coupler as a method of simulating a transmitter signal. The purpose of the agc loop is to control the calibrate-signal, power level to something on the order of 1 dBm.

At this point in the signal flow, the composite 135-MHz, intermediate-frequency signal is separated into its constituent elements by means of the correlation process in order to perform the necessary parameter estimation tasks on each of the unique pseudonoise signals. If we now consider a typical signal processing channel as depicted functionally in figure 3, we see that each channel basically consists of two loops; one is a carrier-tracking, third-order, phase-locked loop while the second is a delay-lock, code-tracking, third-order loop. The fundamental operation performed by the carrier loop is the generation of a phase-coherent, local replica of the received carrier signal while the code loop generates a time synchronized local replica of the received-code signal.

It should be noted that the block diagram shown in figure 3 is merely functionally representative of the essential elements of the delay-lock receiver and does not reflect the many novel techniques incorporated in the receiver design. In subsequent sections specific details regarding these techniques will be presented from a functional and circuit design viewpoint. In this introductory section, figure 3 will suffice as the vehicle for conveying the general principles upon which the receiver was developed.

Assuming, for the moment, that the particular channel of interest has acquired frequency, phase, and time synchronization with respect to the received signal, the local reference at the pseudonoise correlator will consist of a biphase modulated carrier whose frequency, except for an offset equal to the intermediate-frequency, is identical to the received carrier frequency including doppler and doppler rate and whose modulating code is aligned exactly in time with the received code. The correlation properties of pseudonoise codes are such that once the local code is time aligned with the corresponding received code, a continuous-wave signal appears at the correlator output and all other received codes will be discriminated against and appear as wideband noise at the relatively narrowband, intermediate-frequency input. The cw signal is then amplified, down converted and filtered before being applied to the baseband processor which, among other things, derives the tracking-loop-error signal by synchronously demodulating the cw signal at its input. This error signal is then operated upon by the loop filter before it is applied to the vco to maintain phase coherence with the received carrier. Biphase modulating this regenerated carrier with the synchronized code from the code-tracking loop and applying it to the correlator closes the carrier-tracking loop.

The functional operation of the code-tracking loop is not very different from that described for the carrier-tracking loop. The major difference is the way the correlation function is implemented to derive the appropriate code-loop-error function. The delay-lock technique which has been implemented for tracking the pseudonoise signals is theoretically far superior to the more traditional approaches such as tau-jitter although it is somewhat more complex to mechanize. The operation of the delay-lock loop can be readily visualized by means of the baseband model as shown in figure 4(a). There are some serious problems associated with the practical implementation of the baseband, delay-lock loop. For example, it does require an excessive amount of circuitry and power and considerable care must be exercised to match the two correlation channels. The particular implementation incorporated in the MX-450 design produces the desired results while avoiding the problems just cited by delaying the local code separately by a full-code chip and by a half-code chip. If this latter code (i.e., one-half chip delayed) is now applied as the local code replica to the carrier channel, then once code correlation is achieved in the carrier channel we see that the undelayed local code is one-half of a chip early while the full chip delayed local code is one-half of a chip late. Performing a differencing operation on these local early and late codes gives rise to a three-level waveform which, when correlated with the incoming received code, produces exactly the same error characteristic curve as obtained for the baseband model. These functional operations are illustrated in figure 5.

Since each channel generates a local replica of the received carrier and code signals, it only remains to derive estimates of the pseudorange and pseudo-doppler frequency for the receiver to complete its primary function. In order to describe the method used to accomplish this task, consider the receiver as being in the calibrate mode. In this mode, each of the four channels simultaneously tracks a

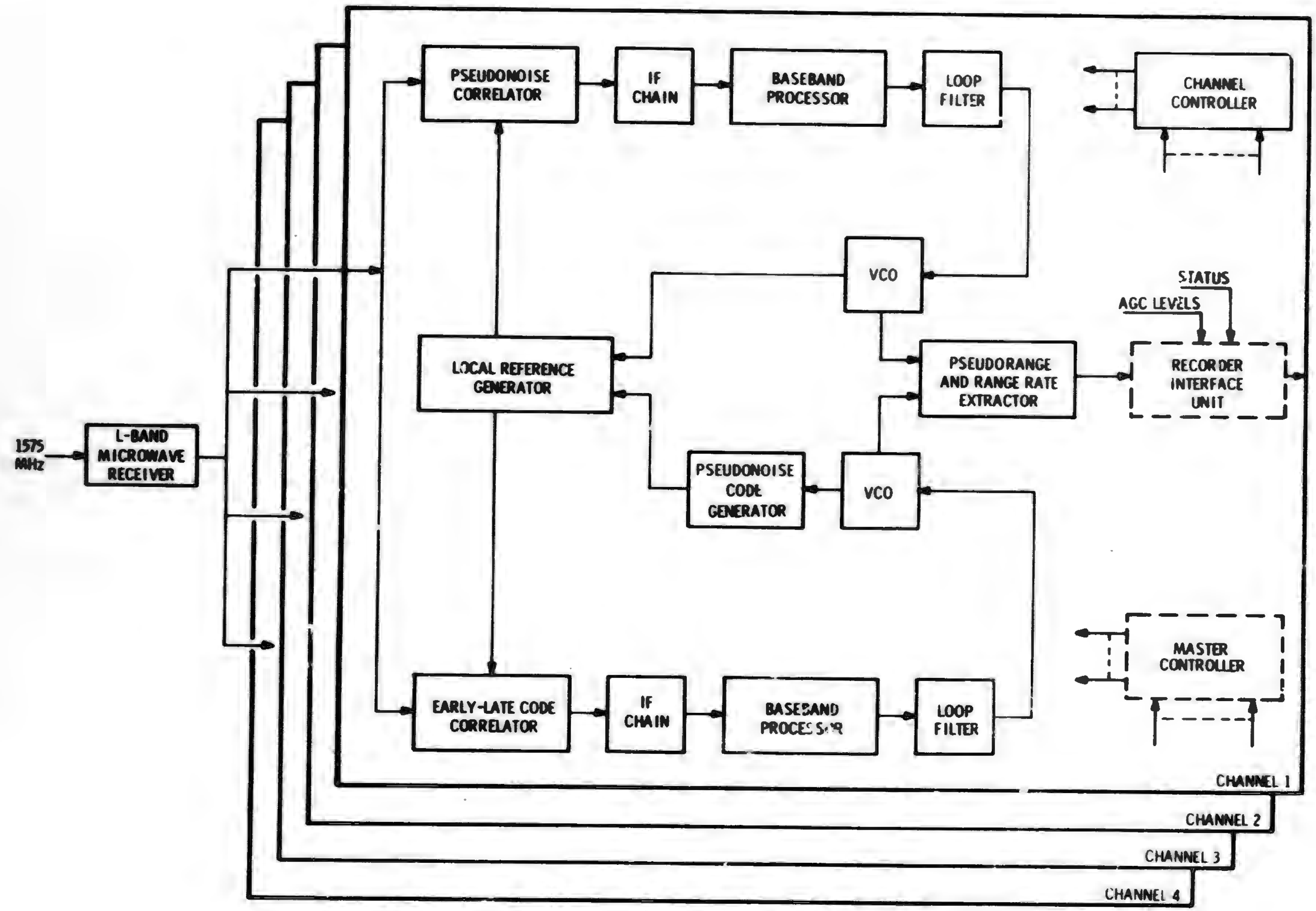


Figure 3. Functional Block Diagram of Delay Lock Correlation Receiver

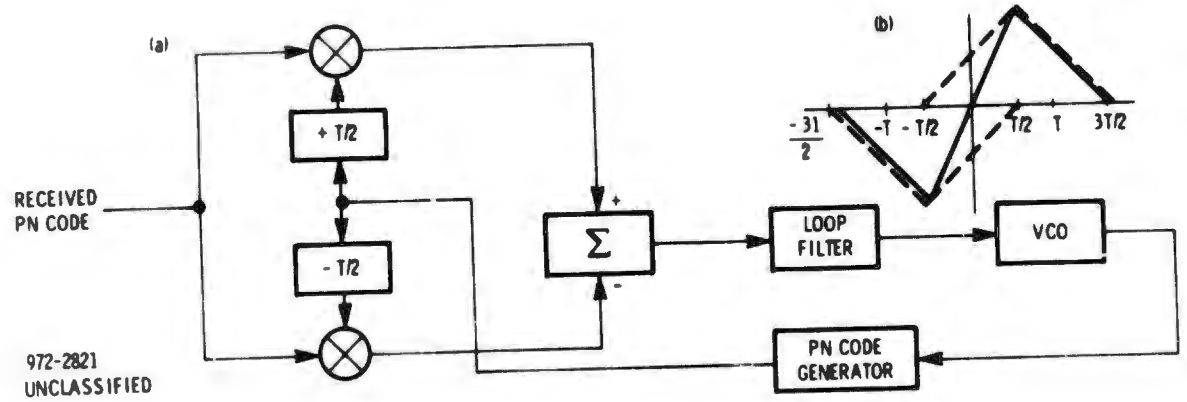


Figure 4. Baseband Delay Lock Model

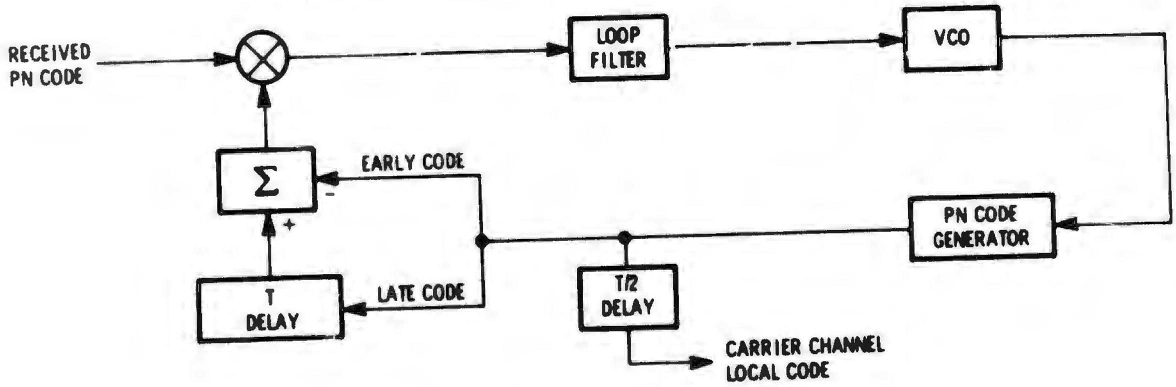


Figure 5. IF Delay-Lock Correlator

common code and a carrier frequency derived from the local frequency reference. During this process the receiver measures the relative delays between the locally simulated transmitter code and the individual channel codes induced as a result of the different electrical paths traversed by the simulated transmitter code. These delays are accumulated in what will be referred to as range registers until the end of the calibrate mode at which point in time the range registers are reset to zero and thereby compensate for the static differential delay among the four channels. Postponing the fine grain detail for subsequent sections, the receiver can now be considered to be in a coast mode until a power-boost signal is detected. In this coast mode, the local carrier frequency and coder clock are effectively derived from the local frequency reference and both the carrier and code voltage-controlled oscillator, which are essentially digital implementations, are inhibited from responding to their respective control signals until the initial acquisition mode begins upon detection of the power boost. At the end of the calibrate mode (which also happens to be the start of the coast mode), the pseudonoise code generators are reset to their initial-state conditions and at the same time, a time-of-day counter is reset to zero. For the remainder of the coast mode both the pseudonoise generators and the time-of-day counter are stepped forward by a 10-MHz clock derived from the 5-MHz frequency standard. Once the power-boost, sync signal (which marks the beginning of the received sequence) is detected for the channel under consideration, the contents of the tod counter represents the number of pseudonoise chips by which the origin of the received pseudonoise sequence and the origin of the local pseudonoise sequence are separated in time. Since all four pseudonoise codes in the receiver have a common time origin (i.e., end of calibrate) and at least in principle, since all four transmitted sequences also share a common time origin, the four time-of-day numbers derived at the receiver could be utilized to generate a coarse estimate of the differential slant ranges between the transmitter grid and the airborne platform. As soon as the power-boost event is detected the local pseudonoise code generator is reset to its initial condition and a small aperture atuosearch is begun to achieve code synchronization. As digital devices, the vco's (or as they more properly will be referred to later, incremental phase modulators) respond to digital control signals such that the carrier vco advances or retards its phase by 3 degrees per pulse and the code vco advances or retards its phase by 1/256th of a code bit per pulse in accordance with their respective sign information. Accumulating the algebraic sum of the code-loop, control pulses during the autosearch routine in the fine range register provides the pseudonoise chip fractional count to the time-of-day count which, after suitable scaling, provides readings of signal arrival times relative to the local on-board clock. In a similar manner, the algebraic sum of the carrier-loop, control pulses is accumulated in the doppler register to provide readings of doppler measurements relative to the local frequency standard.

The contents of the pseudorange registers are sampled every 0.2 seconds and stored in a 4096-bit, buffer memory. The doppler registers are also sampled every 0.2 seconds for their contents accumulated over the previous 0.1 seconds. Finally, the contents of the buffer memory are transferred every second to an incremental digital tape recorder for postflight data reduction and processing.

It is perhaps instructive to complete this overview discussion of the receiver functional design with a summary description of the acquisition (or reacquisition) mode peculiar to a particular channel. When in this mode a channel attempts to verify the presence of a cw carrier signal in the 6-KHz bandwidth of its final 1.25-MHz, intermediate-frequency stage. The decision as to whether signal is present or not is based on a time-variable, sequential-decision strategy where the decision "signal not present" is manifested by a pulse. This pulse increments the phase of the local code by one-half a pseudonoise chip and a signal-present decision is reviewed again. The sequential detector continues to generate pulses indicating the absence of signal as long as the received and local pseudonoise codes are misaligned in time by a pseudonoise chip or more. Sooner or later, by stepping the local code in half-chip increments, the two-code sequences become time aligned and a burst of cw energy appears at the intermediate-frequency amplifier output. The sequential detector finally decides that the signal is indeed present and advertises this decision by not creating a pulse. As a result, the local code hovers without any additional half-chip phase stepping so as to maintain the correlation which resulted in the appearance of cw at the intermediate-frequency. In the meantime, the inphase and quadrature channels of the synchronous demodulator are monitored by a digital frequency discriminator to estimate the initial frequency uncertainty of the cw signal. This estimate, in turn, is applied to the digital-loop filter to aid the third-order-tracking loops' frequency pull in until the point is reached where the loop automatically phase locks. At this point the code loop is closed and the time alignment of the received and local codes is further refined. On the occurrance of this event, the acquisition mode is terminated and the channel enters the tracking mode.

SECTION II

RECEIVER FUNCTIONAL DESCRIPTION

The functional details of the MX-450 receiver design are presented in this section. The receiver consists of four major assemblies which are identified as the microwave receiver assembly, the signal processor assembly, the power supply assembly and the control-display panel assembly.

The most significant functional elements of the receiver are shown in the system level block diagram of figure 6. The microwave receiver input interfaces to the aircraft antenna subsystem to receive the four transmitted pseudonoise (pn) modulated carrier signals at 1575 MHz. The output of the microwave receiver consists of the received composite pseudonoise signal which has been frequency down converted to 135 MHz and appropriately filtered and amplified. The microwave receiver contains its own fixed frequency synthesizer which is excited by the 5-MHz frequency standard located, for convenience, in the power supply assembly. For the purpose of receiver calibration and self-test, a pseudonoise calibrate/test sequence and a 20-MHz, local carrier, both of which are derived in the signal processor, is supplied to the microwave receiver. The signal processor also supplies to the microwave receiver the four individual channel coherent automatic-gain-control (agc) signals in order to allow the weakest received signal to control the gain of the 135-MHz, intermediate-frequency amplifier which is common to all four received signals. In conjunction with the noncoherent agc, an event pulse marking the occurrence of received-signal power boost, is generated in the microwave receiver which performs a control function in the signal processor during the initial acquisition mode. In the calibrate mode, this event pulse is generated in the signal processor and used in the microwave receiver to control the attenuation of the simulated transmitter signal prior to its injection in the front end at 1575 MHz.

The first operation performed in the signal processor is to separate, by correlation, the four components of the 135-MHz, composite pseudonoise signal received from the microwave receiver. Each of these individual pseudonoise signals correlates with its local reference to provide two relatively narrowband signals at 21.25 MHz for the purpose of carrier and code tracking. As shown in figure 6, each member of this narrowband pair is amplified, filtered, and frequency down converted to 1.25 MHz in identical intermediate-frequency sections prior to synchronous demodulation which results in the baseband tracking error signals for the carrier and code loops. The inphase and quadrature components of the demodulated carrier signal is also used to develop an estimate of the initial doppler frequency uncertainty as an aid to carrier loop lock during the acquisition mode. A sequential detector, operating on the output of the 1.25-MHz-carrier, intermediate-frequency amplifier to determine the presence of carrier signal, controls the process of code search and synchronization.

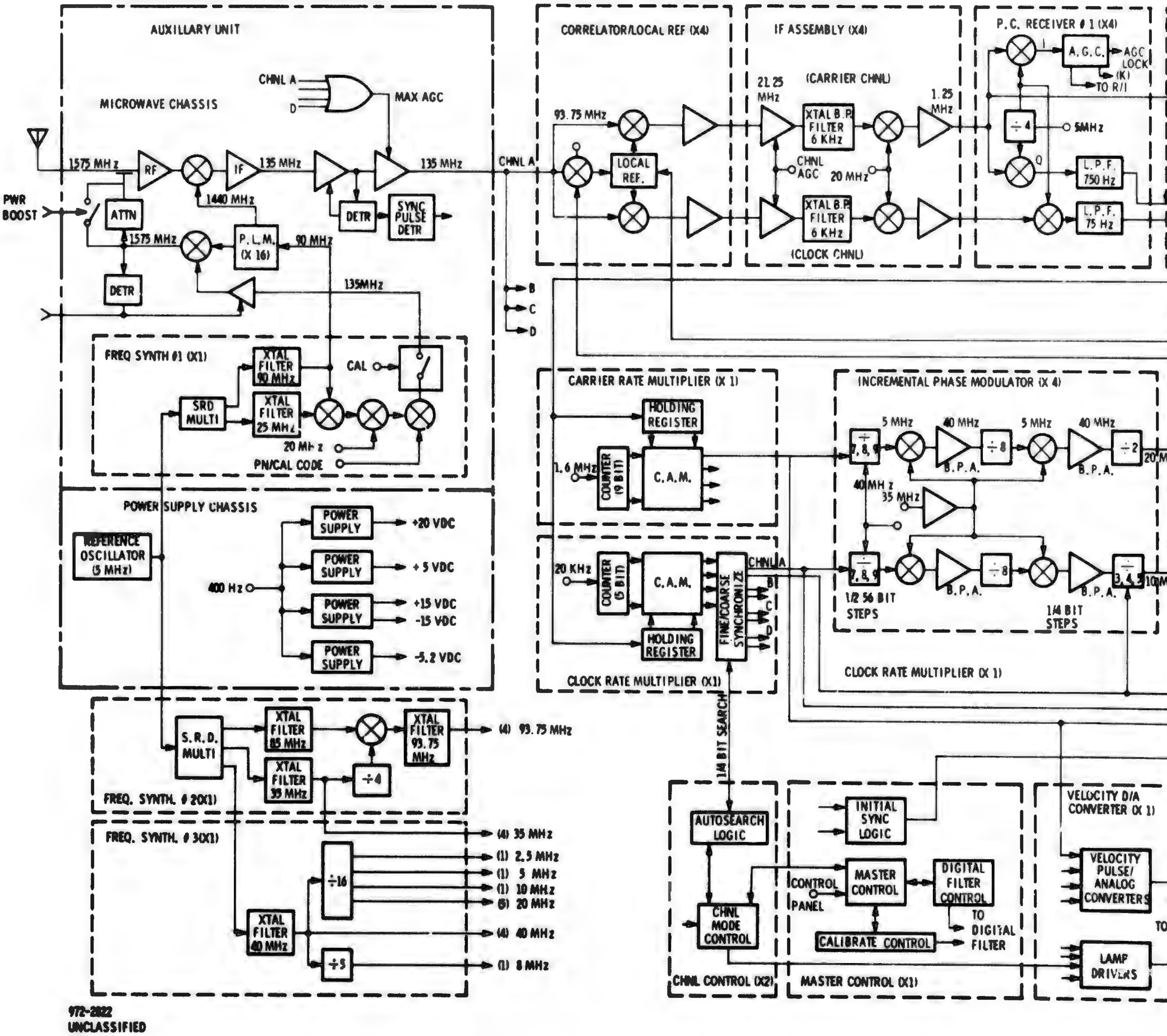
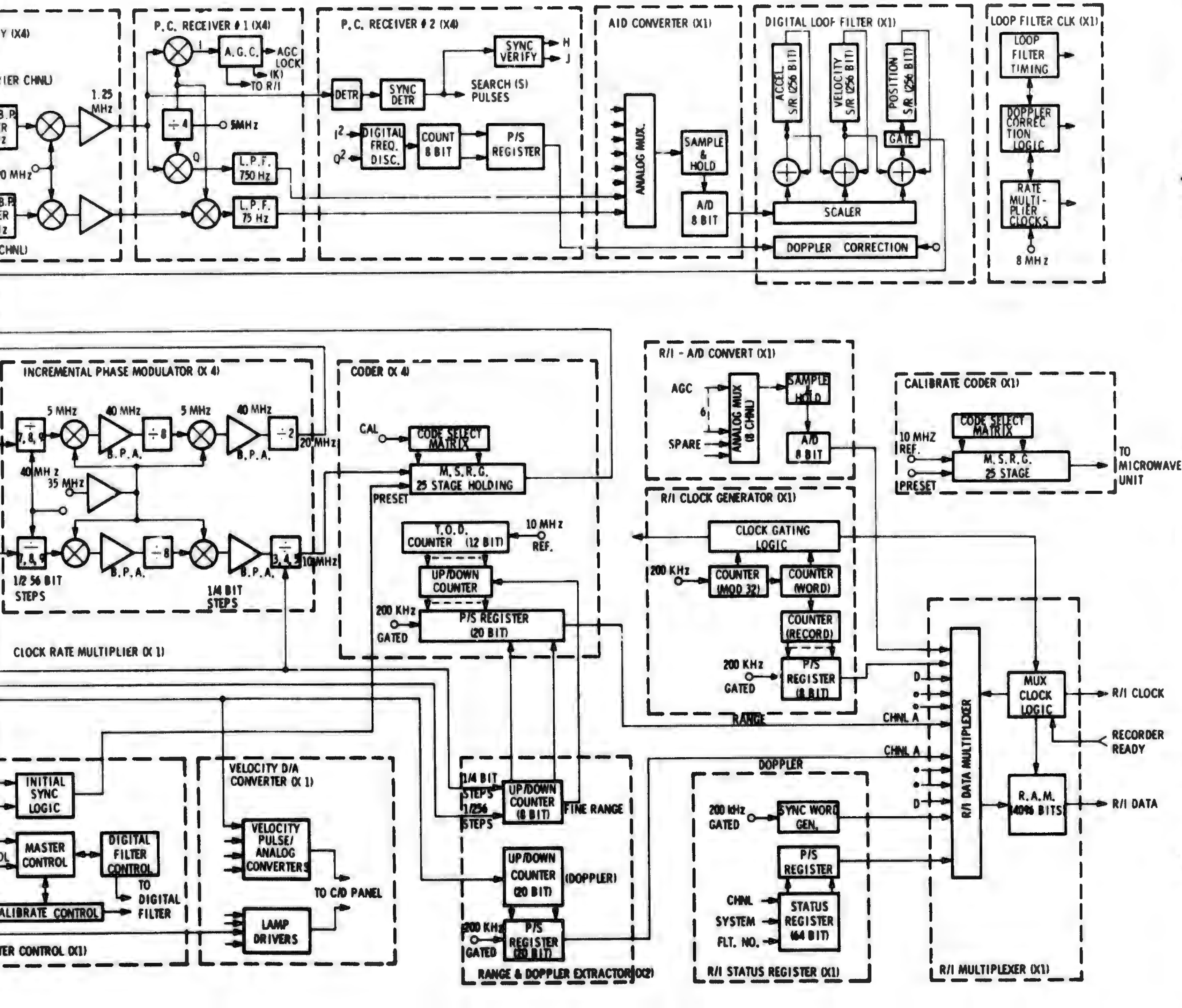


Figure 6. MX-450 Navigation Receiver, Block Diagram


P.C. RECEIVER # 1 (X4)
A.G.C.
AGC LOCK (K)
TO R/I
1.25 MHz
5MHz
L.P.F. 750 Hz
L.P.F. 75 Hz
P.C. RECEIVER # 2 (X4)
SYNC VERIFY
H
J
DETR
SYNC DETR
SEARCH (S) PULSES
DIGITAL FREQ. DISC.
COUNT 8 BIT
P/S REGISTER
A/D CONVERTER (X1)
ANALOG MUX.
SAMPLE & HOLD
A/D 8 BIT
DIGITAL LOOP FILTER (X1)
ACCEL. S/R (256 BIT)
VELOCITY S/R (256 BIT)
POSITION S/R (256 BIT)
GATE
SCALER
DOPPLER CORRECTION
LOOP FILTER CLK (X1)
LOOP FILTER TIMING
DOPPLER CORRECTION LOGIC
RATE MULTI-PLIER CLOCKS
8 MHz
INCREMENTAL PHASE MODULATOR (X 4)
5 MHz
40 MHz
B.P.A.
20 MHz
35 MHz
10 MHz
1/2 56 BIT STEPS
1/4 BIT STEPS
CLOCK RATE MULTIPLIER (X 1)
CODER (X 4)
CAL
CODE SELECT MATRIX
M.S.R.G. 25 STAGE HOLDING
PRESET
T.O.D. COUNTER (12 BIT)
10 MHz REF.
UP/DOWN COUNTER
200 KHz GATED
P/S REGISTER (20 BIT)
R/I - A/D CONVERT (X1)
AGC
SPARE
ANALOG MUX (8 CHNL)
SAMPLE HOLD
A/D 8 BIT
CALIBRATE CODER (X1)
10 MHZ REF.
CODE SELECT MATRIX
M.S.R.G. 25 STAGE
TO MICROWAVE UNIT
R/I CLOCK GENERATOR (X1)
CLOCK GATING LOGIC
200 KHz
COUNTER (MOD 32)
COUNTER (WORD)
COUNTER (RECORD)
200 KHz GATED
P/S REGISTER (8 BIT)
RANGE
CHNL A
R/I DATA MULTIPLEXER
MUX CLOCK LOGIC
R/I CLOCK
RECORDER READY
R.A.M. 4096 BITS
R/I DATA
R/I MULTIPLEXER (X1)
INITIAL SYNC LOGIC
MASTER CONTROL
DIGITAL FILTER CONTROL
TO DIGITAL FILTER
CALIBRATE CONTROL
VELOCITY D/A CONVERTER (X 1)
VELOCITY PULSE/ ANALOG CONVERTERS
TO C/D PANEL
LAMP DRIVERS
1/4 BIT STEPS
1/256 STEPS
UP/DOWN COUNTER (8 BIT)
FINE RANGE
UP/DOWN COUNTER (20 BIT)
(DOPPLER)
200 KHz GATED
P/S REGISTER (20 BIT)
RANGE & DOPPLER EXTRACTOR (X2)
DOPPLER
200 kHz GATED
SYNC WORD GEN.
P/S REGISTER
CHNL
SYSTEM
FLT. NO.
STATUS REGISTER (64 BIT)
R/I STATUS REGISTER (X1)

2

At this point the signal processor services the four carrier and four code-loop-error signals with a single time-shared, third-order, loop filter. To accomplish this feat, an eight-channel, analog multiplexer is used to sample the loop-error signals sequentially in time. Each code loop error signal is sampled 625 times a second while each carrier-loop-error signal is sampled at five times that rate or 3125 times per second. Each analog sample is converted to a digital word and applied to the digital loop filter. As shown in figure 6, a simplified representation of the loop filter algorithm consists of a set of 256 bit recirculating shift registers which effectively performs the integration of the error signal as dictated by the mathematical model of the filter. Each register contains a set of eight 32-bit words; each word corresponding to a particular loop out of the eight loops being time shared by the filter. At any instant in time a particular word in one of the registers and the corresponding pair or words in the two other registers represents, in engineering units, the appropriate loops present estimate of acceleration, velocity, and position. Needless to say, the recirculation rate of the registers is synchronous with the multiplexing of the loop-error signals.

At this point the system demultiplexes and applies the most significant part of the contents of the position register to the carrier or code content addressable memory (cam) depending on which loop is being sampled. The least significant bit of the position word corresponds to 2^{-7} Hz for the carrier loop and 2^{-8} chips for the code loop. The cam accepts this digital word from the filter, regards it as an integer and applies that number of pulses at an almost uniform rate to an incremental phase modulator (ipm). Depending on the sign bit associated with the integer, the ipm advances or retards its output phase by 2^{-7} cycle in the case of the carrier ipm or 2^{-8} chips in the case of the code ipm in response to each pulse received from the cam.

The implementation of the ipm is relatively straightforward. For example, the carrier ipm in its quiescent state divides a 40-MHz reference frequency by 128 and frequency translates back up to 20-MHz. For a positive-sign bit the divide-by-eight counter is forced for one time to count short or reset after seven periods rather than the normal eight periods of the 40-MHz input. The effect on the 20-MHz output appears as a discrete phase advance of approximately 3 degrees. In a similar manner a negative sign bit causes the ipm output phase to retard by 3 degrees. Analogously, the code ipm which provides code clock can be advanced or retarded by 1/256 of a chip or approximately 0.4 feet. The carrier loop is now closed directly through the correlator/local reference module and the code loop closes through the pseudonoise code generator and the correlator/local reference module.

The range and doppler extractors are implemented in the form of counters which accumulate, with due regard for sign, the pulses which are applied to the code and carrier ipms respectively. The fine-range counter accumulates the net count of quarter chip steps of the local code which occur in pairs during the acquisition mode and the 1/256 chip steps which occur in the tracking mode. When the fine-range counter accumulates a net count corresponding to a complete one chip code displacement, the counter, containing the time-of-day count marking the time of occurrence of power boost, is incremented by one count in the appropriate direction. The integer chip time-of-day count and the fractional chip count in the fine-range register are combined every 0.2 seconds and transferred to the recorder interface module. Similarly, every 0.2 seconds the contents of the doppler register, accumulated over the previous 0.1 seconds, are also transferred to the recorder interface module.

The recorder interface module performs the functions of strobing each processor channel for range, doppler, and channel status information in addition to formatting and storing the data for subsequent transfer to the airborne data acquisition system on a once-per-second basis.

The executive control of the receiver is performed by the master controller module. This module provides the command and control functions required by the individual processor channels for the purpose of initialization and acquisition. Each individual channel has its own controller which effectively operates as a hard-wired programmer to cycle the channel through its various operating states from standby through acquisition to the tracking mode.

The remaining functional element is the fixed frequency synthesizer which is excited by the 5-MHz, frequency standard to provide the various clocks and reference frequencies required throughout the signal processor.

2.1 MICROWAVE RECEIVER DETAILED DESCRIPTION

A detailed functional block diagram of the microwave receiver is shown in figure 7. The input from the antenna subsystem is first filtered by a fixed tuned preselector with a measured 3-dB bandwidth of 47 MHz centered at 1575 MHz. The 75-dB-rejection points for this preselector occur at approximately 80 MHz on either side of the center frequency which is an indication of the excellent image rejection characteristics of the filter. To maintain a relatively low system noise figure, the preselector has a measured insertion loss of 0.5 dB.

The preselector is followed by a signal limiter which protects the L-band preamplifier from permanent damage as a result of high-powered, in-band interference. The limiter is a Hewlett-Packard back-to-back, pin-diode device rated at 0.8 watt of cw power or a peak power of 75 watts for 1 microsecond. The output of the limiter is attenuated by 0.3 dB at input levels of up to -30 dBm. For much higher signal levels, the limiter output stays relatively constant at about +10 dBm.

The output of the limiter is routed through the direct leg of a 30-dB, directional coupler with an insertion loss of 0.2 dB. The purpose of the coupler is to permit introduction of a test signal simulating a transmitter signal. The sidearm attenuator is normally set at 30 dB to establish the proper power level of the test signal. This attenuator also serves to increase by 30 dB, the 25 dB of isolation inherent in the coupler design.

The output of the directional coupler is applied to a low-noise preamplifier with a gain of 31 dB and a noise figure of 3.3 dB. This device effectively establishes the system noise figure which is less than 5 dB.

The frequency down converter was implemented as a broadband balanced mixer. By means of the 1440-MHz local oscillator, it translates the received 1575-MHz signal to the first intermediate-frequency amplifier centered at 135 MHz. The image frequency at 1305 MHz is suppressed by at least 80 dB by the preselector and the largest in-band intermodulation product at 270 MHz is suppressed by the balanced mixer by at least 50 dB.

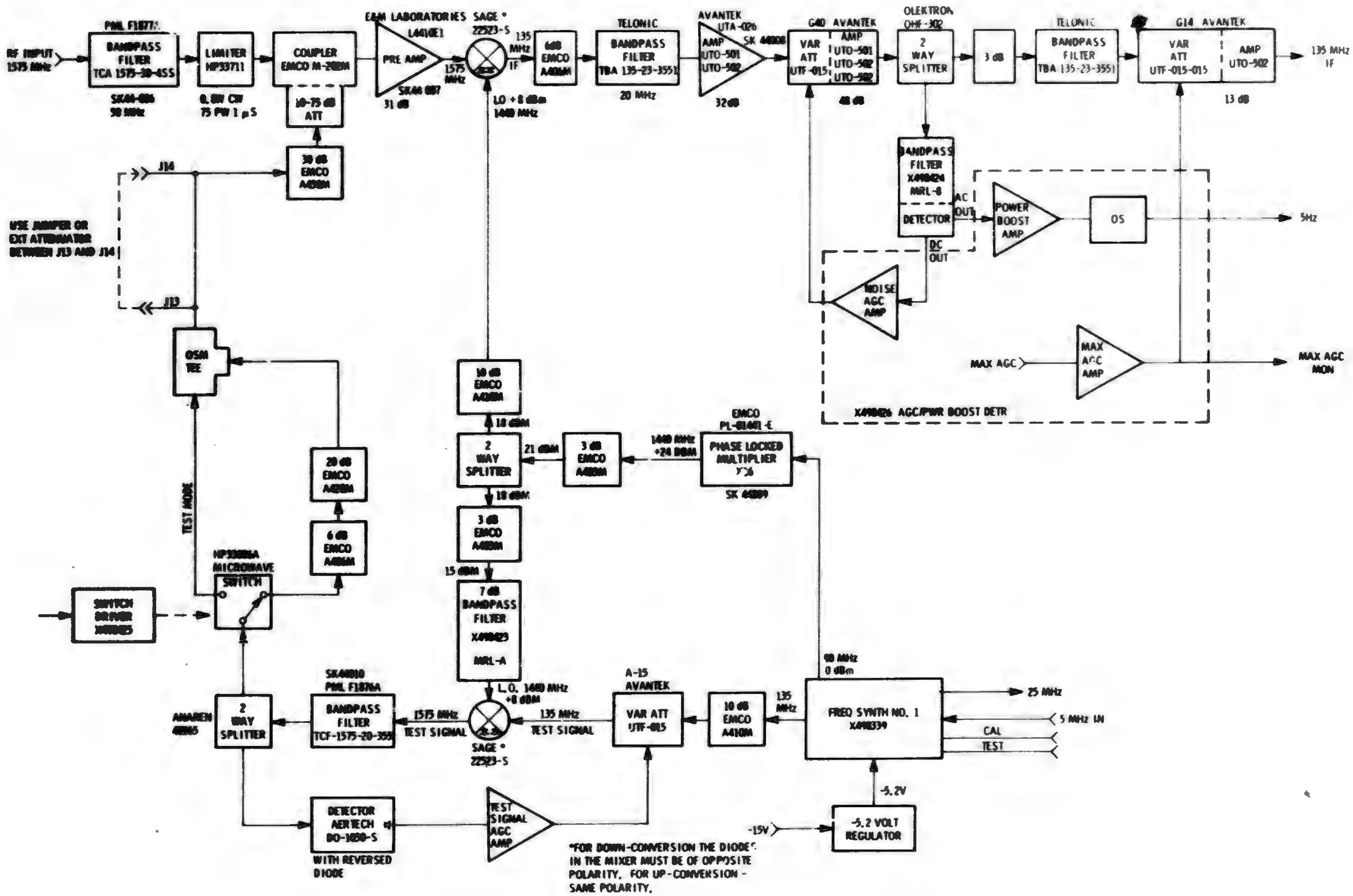


Figure 7. Microwave Receiver - Block Diagram

Before proceeding with a description of the 135-MHz, intermediate-frequency section, we consider the frequency synthesis required to generate the local oscillator signal and that which is required to simulate a transmitter signal. The synthesizer in the microwave receiver is excited by a high-Q, low-distortion, 5-MHz standard. This frequency standard is applied to a snap-recovery diode which generates a wideband line spectrum with spectral components occurring every 5 MHz. Two custom-designed, narrowband, crystal, bandpass filters are utilized to extract two of these line components: one at 90 MHz and a second at 25 MHz. The filtered 90-MHz reference frequency is then applied to the phase-lock multiplier for multiplication by 16 to 1440 MHz. The 90-MHz and 25-MHz, crystal filter outputs are also mixed to obtain a 115-MHz reference for up converting to 135 MHz for a local 20-MHz replica of the received carrier derived in the signal processor. Provision is also made to biphase modulate this 135-MHz carrier with a pseudonoise calibrate code for calibration and self-test purposes. This 135-MHz, calibrate signal is up converted to 1575 MHz in a balanced mixer similar to that used for down converting the received signal. The reference frequency used to perform the up conversion is the 1440 MHz generated by the phase-lock multiplier. The purpose of the bandpass filter in the calibrate signal local oscillator path is to increase by at least 60 dB the isolation between the received-signal and the calibrate-signal modulation. The 1575-MHz, calibrate signal is filtered and its power is equally split between two paths. In one path a measure of the calibrate-signal, power level is made and is applied as a control signal to a solid-state, variable attenuator in order to maintain the calibrate-signal level within 1 dB of nominal. In the second path the calibrate signal is connected to a solid-state, microwave switch which simulates the signal power-boost condition of the transmitted signal. In one mode, which corresponds to the long code transmission, the fixed attenuators are connected to the calibrate signal path which establishes a calibrate signal level of -123 dBm at the preamplifier input. In the other mode, the calibrate signal is connected to the path without the attenuators so that a calibrate-signal level of -100 dBm is established for 25 microseconds at the preamplifier input. The signal which controls the switching is developed in conjunction with the calibrate code at the signal processor.

Returning to the received signal flow we see from figure 7 that, after frequency down conversion, the 135-MHz, intermediate-frequency signal is bandpass filtered in a 20-MHz filter and amplified by 32 dB prior to the noise agc circuit. The noise agc loop consists of a variable attenuator/intermediate-frequency amplifier, a two-way power splitter, a bandpass filter/power detector and a noise agc amplifier. The bandpass filter, prior to the agc detector, has a gain of 10 dB at 135 MHz and a bandwidth of 10 MHz. The square-law detector output is dc coupled to the noise agc amplifier which develops the required control signal for the solid-state variable attenuator to maintain the loop intermediate-frequency amplifier gain essentially constant at 48 dB. The square-law detector output is also ac coupled to the power-boost amplifier and filter. The power-boost filter was designed such that the 3 dB points occur at 0.35 and 10 kHz. This filter is followed by a threshold device which indicates the occurrence of power-boost. An analytical derivation which influenced the selection of this relatively simple method for initial synchronization is presented in appendix A.

The second output of the two-way power splitter in the agc loop is again bandpass filtered before it is applied to the final 135-MHz amplifier whose gain is controlled by the largest of the four-channel agc voltages.

2.2 SIGNAL PROCESSOR FUNCTIONAL DESCRIPTION

Functionally, the signal processor accepts the composite signal at 135 MHz from the microwave receiver and by means of the correlation technique separates the four unique pseudonoise-modulated signals for subsequent processing by four independent processing channels. Each of these processing channels consists of a carrier and code tracking loop which maintains a phase-coherent local replica of the appropriate transmitted carrier and modulating code signal. Since each of the four processing channels are functionally identical the remainder of this discussion will be focused on the operation of just one channel unless it is otherwise noted.

2.2.1 CORRELATOR AND IF SECTION

In figure 6 the correlator-local reference module has three basic inputs. One is the 135-MHz received signal and the remaining two consist of a 20 MHz version of the locally generated carrier and the 10-MHz, local-code sequence. The purpose of this functional element is to construct two local signal replicas at 113.75 MHz which correlate with the desired incoming signal at 135 MHz to provide two narrowband signals at 21.25 MHz for carrier and code tracking. A more detailed block diagram illustrating the operations necessary to achieve the objective is shown in figure 8. First consider the operations required to derive the pseudonoise-modulated local-reference signal for the carrier loop. The 20-MHz replica of the carrier signal is up converted to 113.25 MHz by the 93.75-MHz reference from the fixed-frequency synthesizer. This signal is then power split to provide the local carrier reference for both the carrier loop and code loop. For the carrier loop the next operation consists of biphase modulating the local carrier reference with the local 10-MHz pseudonoise sequence in order to accomplish correlation with the 135-MHz received signal. The biphase modulation is implemented by means of a two-stage process to achieve maximum carrier suppression in the modulated reference signal. The output of this process results in a cw signal at 21.25 MHz.

A two-stage biphase modulation process is also implemented in the code loop to achieve the desired degree of carrier suppression in the modulated local reference as shown in figure 8.

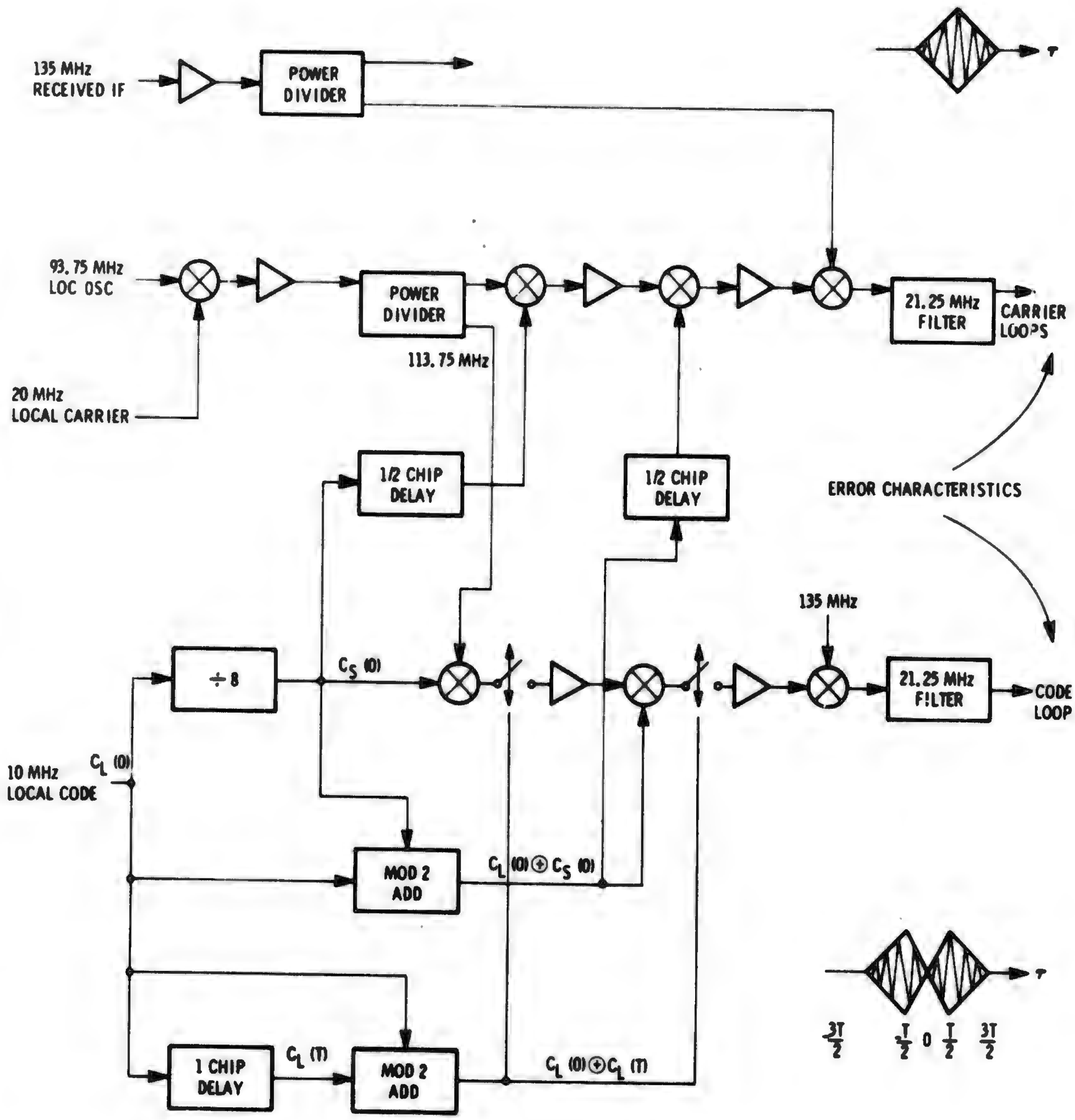


Figure 8. Functional Block Diagram of Correlator/Local Reference Generator

Both the carrier and code loop contain identical intermediate-frequency sections which provide the necessary signal gain and filtering for the decorrelated signals supplied by the correlator/local-reference generator module. The first intermediate-frequency amplifier has a center frequency of 21.25 MHz and a bandwidth on the order of 1 MHz. The amplifier which was designed to provide a nominal gain of 28 dB is followed by a current controlled variable attenuator which operates to maintain the intermediate-frequency signal level constant over a 25 dB range of input signal level variability. The agc signal which is derived from the carrier loop is utilized to control the intermediate-frequency gain in both the carrier and code loops.

Between the 21.25 MHz and 1.25 MHz intermediate-frequency amplifiers a three-pole Butterworth crystal filter was inserted in each intermediate-frequency section. The crystal filter has a center frequency of 21.25 MHz and a 3 dB bandwidth of 6 kHz which limits the noise power at the input of the synchronous demodulator.

The final intermediate-frequency amplifier in the chain is centered at 1.25 MHz and has a nominal bandwidth of 500 kHz.

The characteristics and specifications for the intermediate-frequency section are tabulated in table I.

Table I. Intermediate-Frequency Section Specifications

Characteristics	Specifications
21.25 MHz IF	
Bandwidth	1 MHz (3 dB)
Input Signal Level	-40 dBm Max. -60 dBm Min.
Input Noise Level	-21 dBm Max.
AGC Range	25 dB
AGC Gain	15 dB/volt
Output Signal Level	-30 dBm Nominal
Output Noise Level	-15 dBm Max.
21.25 MHz Crystal Filter	
Type	3-pole Butterworth
Frequency	21.25 MHz
Bandwidth	6 kHz (3 dB) 40 kHz (40 dB)
Temperature Coefficient	20 ppm (0 to 70° C)
1.25 MHz IF	
Bandwidth	500 kHz Nominal
Output Signal Level	-7 dBm Nominal
Output Noise Level	+8 dBm Max.
Aperture	4 v p-p Min.

2.2.2 POSTCORRELATION RECEIVER

The postcorrelation receiver module is perhaps the most active element of the receiver in terms of the variety of functions it is required to perform. Referring to the blocks identified in figure 6 as PC Receiver No. 1 and No. 2, we see the major functions which were implemented in this module. During the tracking mode the essential function performed relates to the coherent demodulation of the 1.25 MHz intermediate-frequency signal in order to generate carrier and code-loop error signals. Incidential to this process several indicators such as carrier loop phase lock are developed as well as the control signals required to activate the agc circuits. In the acquisition mode it is necessary to estimate the initial carrier frequency uncertainty in order to aid the narrowband tracking loop to acquire carrier frequency. To accomplish this objective, a digital frequency discriminator was implemented which operates on the inphase (I) and quadrature (Q) channels of the carrier loop synchronous demodulator to provide an initial velocity correction and subsequent updates to the tracking loop filter. A variable time sequential detector was also implemented in this module to detect the occurrence of code synchronization by sensing the presence of cw signal in the 1.25-MHz intermediate-frequency of the carrier tracking loop. A related function entitled code-sync verification was incorporated into the design to perform as a local event controller during the acquisition/reacquisition modes. A detailed block diagram illustrating these various functions and their interrelationships is shown in figure 9.

The synchronous demodulators required to develop the loop error signals are essentially generically equivalent for both the carrier and code tracking loops. The major difference is that in the code loop the inphase component of the 1.25 MHz demodulator reference is utilized to coherently amplitude demodulate the code-loop error signal. In the tracking mode, the effective low-pass filters operating on the loop error signals is 75 Hz and 750 Hz for the code loop and carrier loop respectively.

The block diagram of figure 9 shows that the low-pass filtered output of the synchronous demodulator I channel is utilized to develop an indication of the occurrence of carrier tracking loop phase lock and an estimate of received signal level for the purpose of generating channel agc. These measurements are made at this point since the parameter available at the I-channel output is directly proportional to the product of the carrier amplitude and the cosine of the phase error. The signal agc estimate developed for a particular channel is applied at the corresponding 21.25 MHz intermediate-frequency amplifier. This same signal agc estimate is filtered further at each channel as indicated in figure 9. The largest agc signal among the four channels is selected to control the gain of the 135-MHz amplifier contained in the microwave receiver and which is common to all four received signals. A high-pass filter on the I-channel output with a low-frequency corner at 200 Hz, allows an envelope detector to derive an estimate of the noise power contained

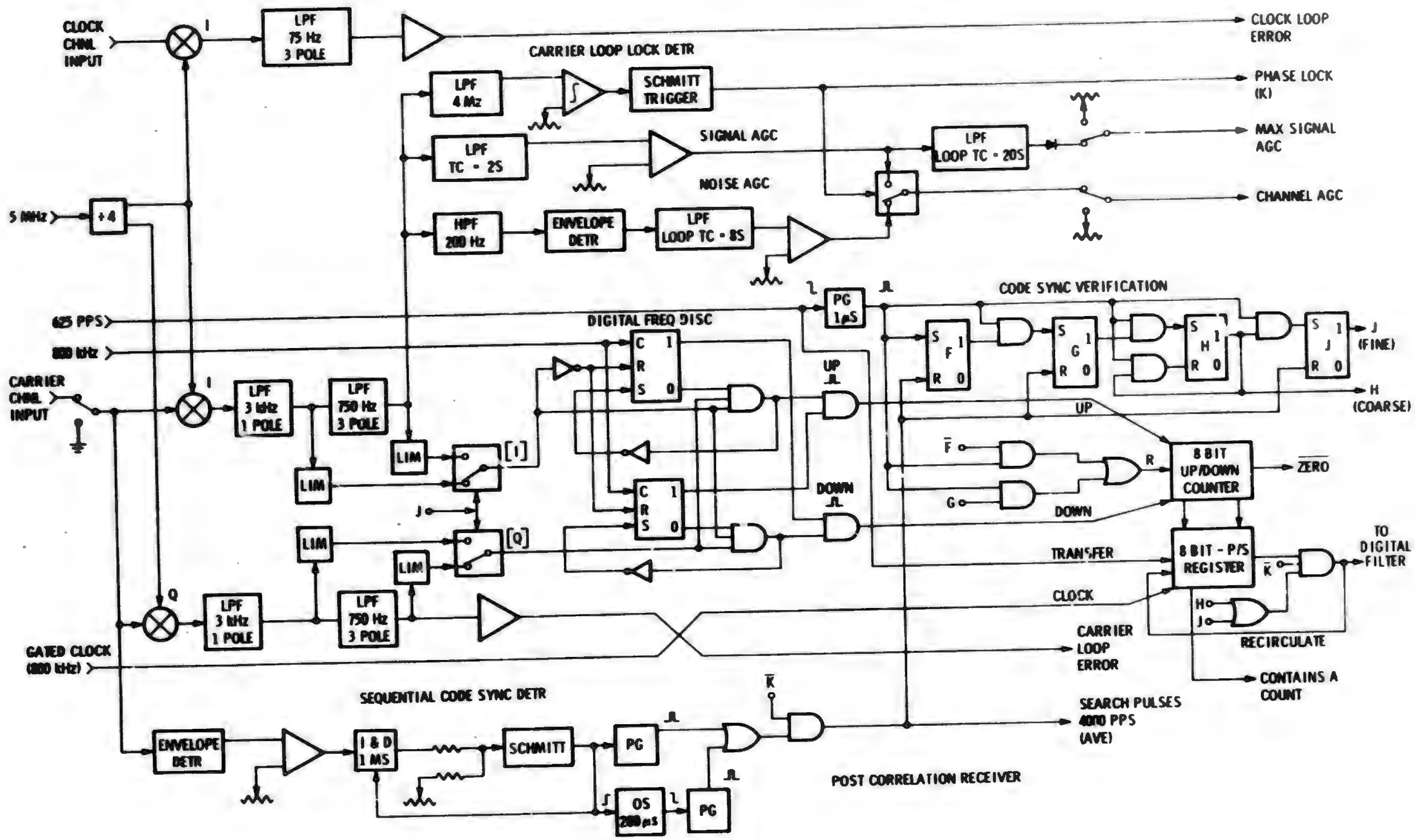


Figure 9. Postcorrelation Receiver

in the intermediate-frequency bandwidth. This noise power estimate is filtered, as indicated in figure 9, and used prior to carrier loop lock to establish the appropriate intermediate-frequency amplifier gain for the subsequent arrival of signal which occurs with the alignment in time of the local and received codes. Once the indication of carrier phase lock appears (denoted by a true K state) the channel automatically switches from noise agc to signal agc.

Referring to figure 9, we note that the spectral occupancy of the demodulated signals in the I and Q channels are first restricted by a 3-kHz, low-pass filter. Each signal thus filtered is simultaneously applied to a parallel combination consisting of a limiter and a 750-Hz, low-pass filter/limiter pair. Depending on the state J, which marks a particular point in the acquisition process, the digital frequency discriminator operates on either the wideband or narrowband I and Q outputs. Consider the occurrence of the true state J as partitioning the process of estimating the initial carrier frequency offset into two segments. The first segment occurs when code sync has been conditionally accepted for approximately 3 milliseconds. During this period of time the initial carrier frequency uncertainty can be as much as 3 kHz in magnitude which in turn gives rise to a beat frequency in the I and Q channels of the demodulator of the same magnitude. To estimate this initial frequency offset, the digital frequency discriminator operates on the 3-kHz low-pass filtered output to determine the average beat frequency over the 3-millisecond period. Since the signal-to-noise ratio is relatively low in the 3-kHz bandwidth, the frequency offset estimate developed by the discriminator is relatively coarse with a deviation from true value amounting to as much as 200 Hz. This coarse estimate of initial frequency offset is applied as a doppler correction to the carrier tracking loop filter which has the effect of pulling the local carrier frequency to somewhere within 200 Hz of the actual received carrier frequency. Assuming the conditional code-sync state has not changed, the discriminator inputs are next switched to operate on the 750 Hz filtered I and Q channels. This results in a significant improvement in signal-to-noise ratio and a corresponding reduction in the variance of the frequency estimates developed by the discriminator. These high-quality estimates of the residual frequency offset are applied as velocity updates to the loop filter at each sampling time until the frequency error has been reduced to the point where the loop automatically phase locks.

It was alluded to in the previous paragraphs that a digital frequency discriminator was implemented as part of the postcorrelation receiver design to estimate carrier doppler frequencies in order to significantly reduce the time required by the narrowband tracking loop to achieve a phase locked condition. The concept upon which the discriminator design is based is relatively simple and relies on the $\pi/2$ phase displacement between the synchronous demodulator's inphase and quadrature channel outputs. For example, in the absence of noise, the inphase output is proportional to $\cos 2\pi\Delta ft$ while the quadrature output is proportional to $\sin 2\pi\Delta ft$ where Δf is the difference between the received carrier and local oscillator frequencies, f_c and f_0 respectively. We note that this difference frequency, Δf, can be either positive or negative depending on whether f_c is greater or less than f_0 and will be reflected in the sign of the quadrature output. Perhaps, the simplest method of illustrating the discriminator concept is to consider a phasor representation of the inphase and quadrature sinusoidal outputs of the demodulator. For a positive frequency offset, the phasors will rotate in the frequency plane in counter-clockwise fashion so that a positive going inphase zero crossing is represented in the phasor diagram by the inphase vector crossing from the third into the fourth quadrant to be followed subsequently by the quadrature vector. An alternate situation occurs when the offset frequency is negative. In this case, the phasors rotate in a clockwise manner and a positive going inphase zero crossing is represented by the inphase vector crossing from the second to the first quadrant after the quadrature vector has already made its transfer to the right half of the plane. Conceptually, then, the strategy for estimating the frequency offset is to simply count, on a per unit time basis, the number of times the inphase vector crosses from the left hand side to the right hand side of the frequency plane given that the conditions placed on the quadrature vector in the preceeding discussion are satisfied. The polarity of the frequency offset is determined by the polarity of the quadrature zero crossing. The comparative performance of three types of digital discriminators with respect to that of a theoretical discriminator, is presented in appendix B.

A functional element of major importance which was incorporated as part of the postcorrelation receiver design is the sequential sync detector. A block diagram of this function is shown in figure 10.

The full-wave rectifier and low-pass filter develops a measure of the total power (noise or signal plus noise) in the 6 kHz bandwidth of the carrier loop intermediate-frequency. Before code synchronization is achieved the output voltage, $-V_i$, from the low-pass filter is proportional to the measured noise power and its magnitude is less than the bias voltage $-V_b$. This causes the output of the integrator to ramp downward in the negative direction from zero until its magnitude exceeds that of the threshold voltage $+V_D$. The threshold detector output voltage which is normally at zero volts, now changes to +5 volts indicating a dismissal of code sync. The positive change in the detector's output-voltage level initiates a sequence of events by means of mode control logic which maintains an average search pulse rate of 2 kpps.

When code correlation is finally achieved, a cw signal appears in the intermediate-frequency increasing the total power to the full-wave rectifier by 6 dB. The magnitude of the voltage, $-V_i$, becomes larger than the bias voltage so that the integrator output now grows positive. The threshold detector remains dormant and no search pulse is generated.

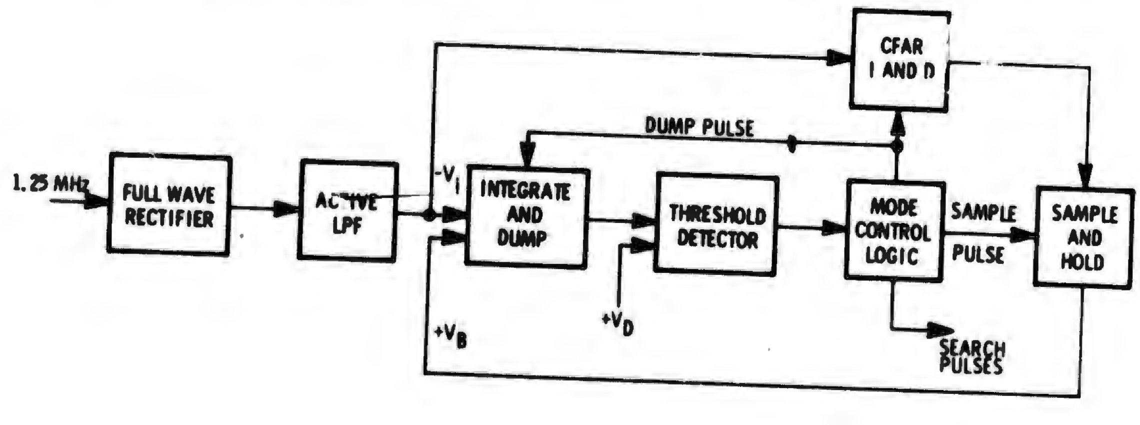


Figure 10. Sequential Sync Detector Block Diagram

The mode control logic in the detector is also used to make the conditional sync decision. After 3.2 milliseconds if no search pulse is generated, the mode logic moves to a state H. This causes the current frequency offset estimate to be dumped into the digital frequency discriminator filter. At the next 625 pps clock (assuming no search pulse), a state J occurs which declares code sync. Simultaneously, the carrier loop filter is being slowly updated from the initial coarse offset estimate made in state H. These updates every 1.6 milliseconds continue until the carrier loop locks completing the synchronization procedure (state K). This is achieved on the order of 10 seconds.

2.2.3 ANALOG/DIGITAL CONVERTER

After sequentially sampling the carrier and code loop error signals from each channel, an analog/digital converter applies the resulting digital word to the loop filter as shown in figure 11.

The multiplexer is an eight-channel, high-speed MOSFET device that samples each code loop error signal every 1.6 milliseconds and each carrier loop error signal every 320 microseconds. The samples are each tracked for 20 microseconds and then held for 20 microseconds and applied sequentially to the A/D converter. A convert command to the A/D converter module starts an internal 750 kHz square-wave and resets the previous output word to zero. Bit decisions are made on successive positive edges of each clock cycle of the square-wave. After eight clock times the parallel output data is valid. The parallel to serial conversion is performed by a comparator circuit. Each outputted eight bit word is a bipolar 2's complement representation of the error signals which is provided to the loop filter.

2.2.4 DIGITAL LOOP FILTER

The digital loop filter uses a time sharing technique and functions as a third order filter for: (1) four independent carrier tracking loops and, (2) four independent code clock tracking loops. The key components are shown in figure 12 and consist of a shift register for scaling, arithmetic adders, shift registers which function as accumulators and switching logic for time sharing purposes.

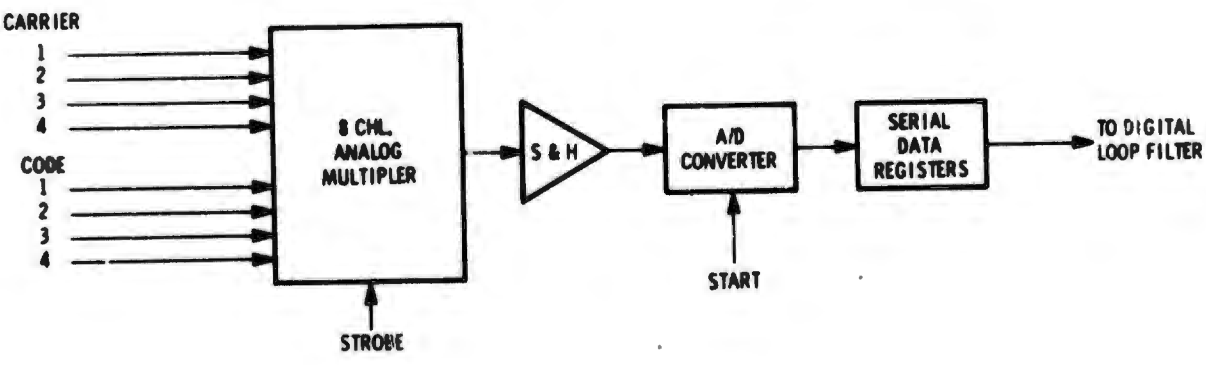
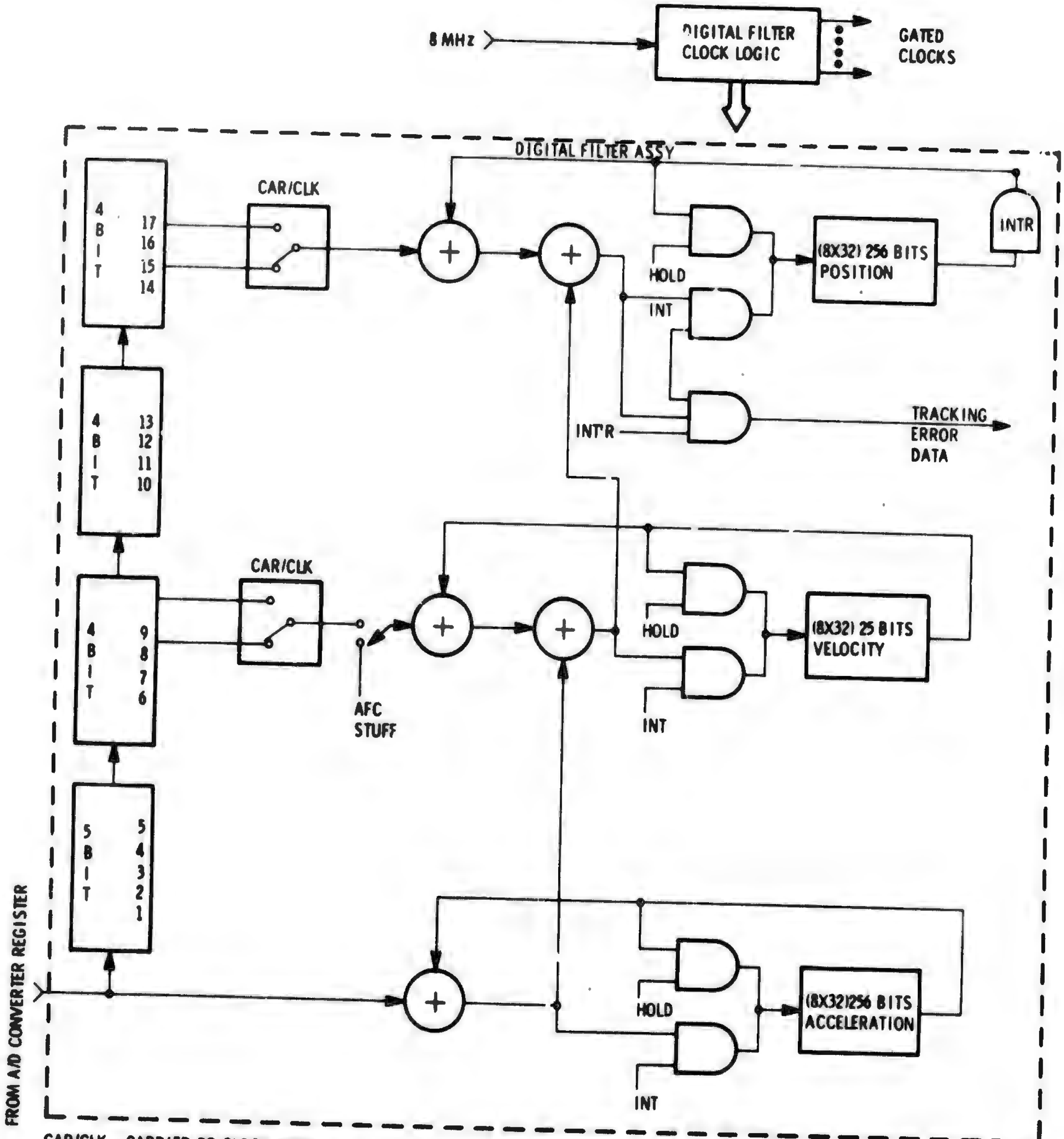


Figure 11. Multiplexer-A/D Converter



CAR/CLK - CARRIER OR CLOCK MODE
HOLD - RECIRCULATE CLOCK DATA 4 OUT OF 5
INT - INTERROGATE OR CIRCULATE REGISTER
ZERO - HOLD · INT OR LOAD ALL ZEROS
INT R - INTERROGATE OR READ RANGE
CP32 - SAVE THE SIGN

Figure 12. Digital Loop Filter - Logic Diagram

Each shift register contains eight independent signals in series. Each register and adder combination forms a digital integrator. One of the registers contains the acceleration components of the tracking error signal for all eight loops. A second and third register contains the velocity and position error signals for all eight loops respectively.

The input shift register functions as a scaler by shifting the digital error signal from the analog-to-digital converter with respect to the word position in each register. The scaler in effect provides the coefficient terms in the third order equation.

For time sharing, a particular channel can be placed in a "hold mode" by recirculating the error-signal words in each register without adding an error signal. Provision for injecting initial conditions into the velocity register is also provided to implement doppler correction.

During each integration interval (1/3125 second for the carrier loops, 1/625 second for the code loops), tracking error data is sent out to the appropriate rate multipliers. This data consists of the most-significant-bit position of the word errors from the position register. Since the tracking error data is used within the phase locked loop, the extracted data is replaced with zeros, thus the position registers actually contain only the residual position error to prevent truncation errors.

The implementation of the carrier- and clock-loop scaling is shown in figures 13 and 14.

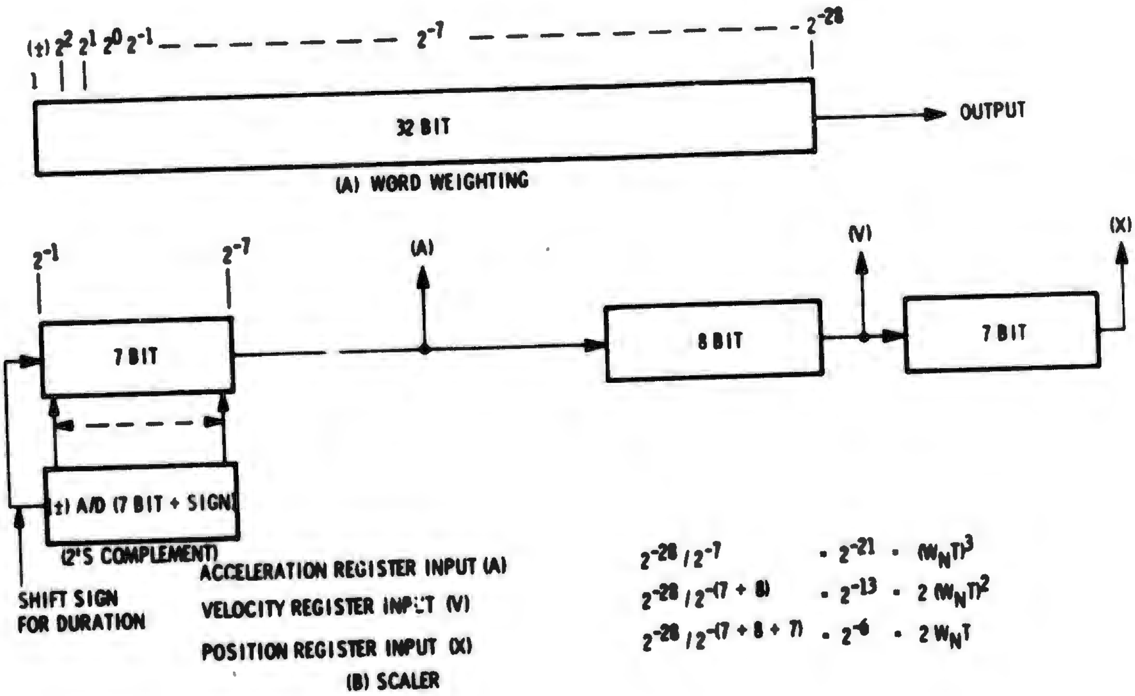


Figure 13. Carrier Loop Scaling

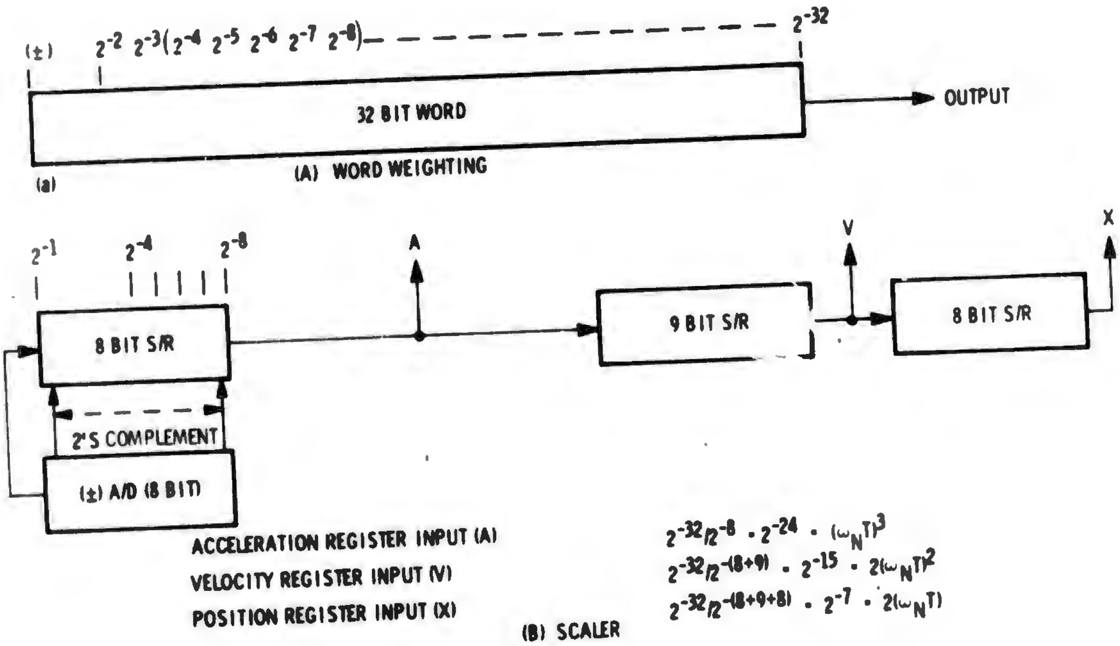


Figure 14. Clock Loop Scaling

2.2.5 LOOP FILTER CLOCK

The function of the loop filter clock is to provide all of the timing signals in proper phase relationship for the operation of the digital filter, rate multipliers, channel controllers, and master controller. A block diagram of the filter timer is shown in figure 15.

The prime concern of the filter timer is to keep track of address locations within the recirculating dynamic shift register memory which is on the digital filter card. This digital filter time sharing sequence is shown in figure 16. All bit addressing, word selection, channel addressing, and iteration cycle counting originates on this printed circuit assembly.

2.2.6 RATE MULTIPLIERS

2.2.6.1 Clock Rate Multiplier

The function of the clock-rate multiplier card is to interface the digital loop filter with four incremental clock phase modulators by means of translating a binary 6-bit word into an evenly distributed rate taken over a fixed period of time. The design is completely modular in construction and rate multiplication for all four channels is accomplished on a single point-to-point assembly. All unique timing signals are taken from the filter timer. A block diagram of the rate multiplier is shown in figure 17.

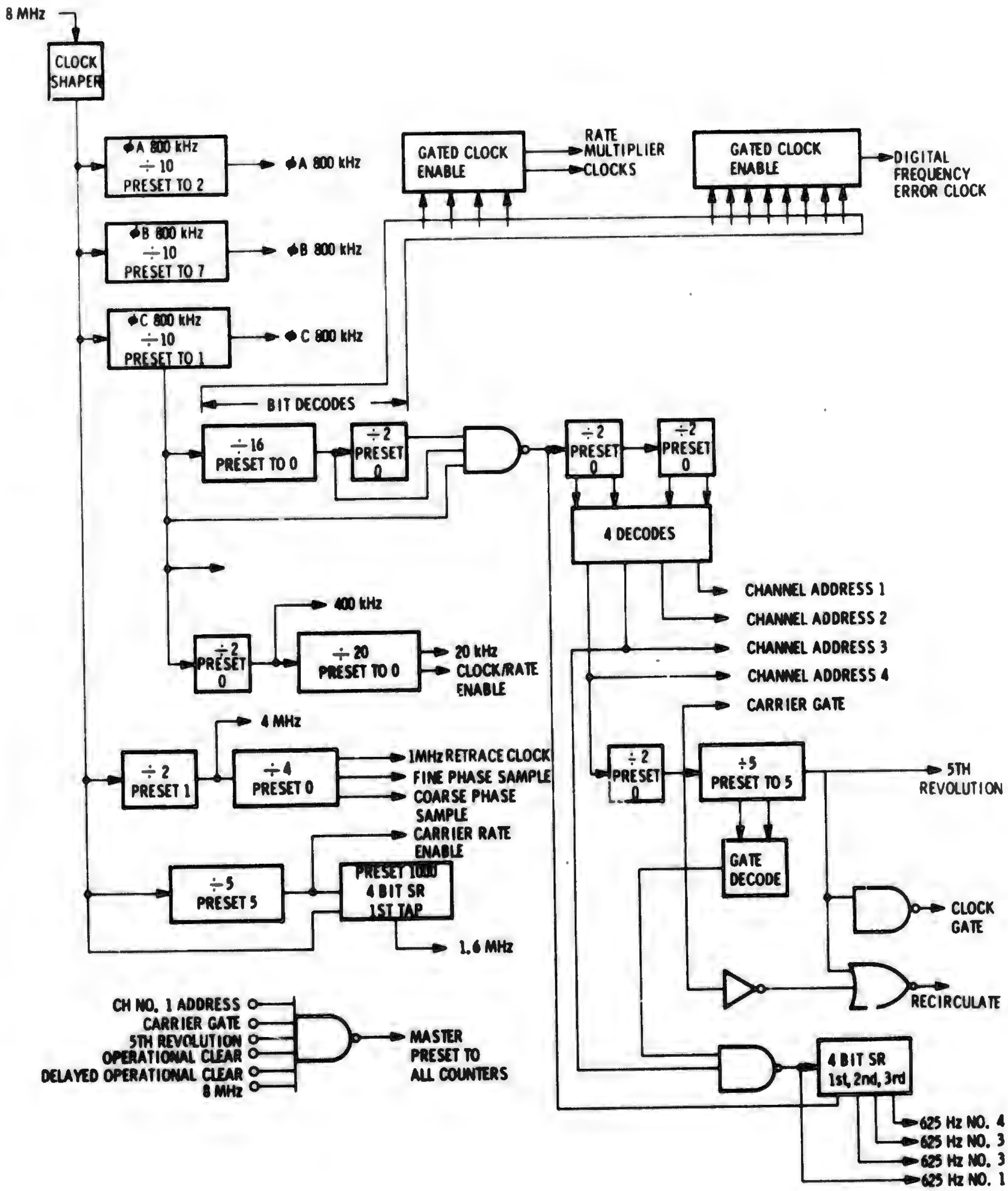


Figure 15. Loop Filter Clock

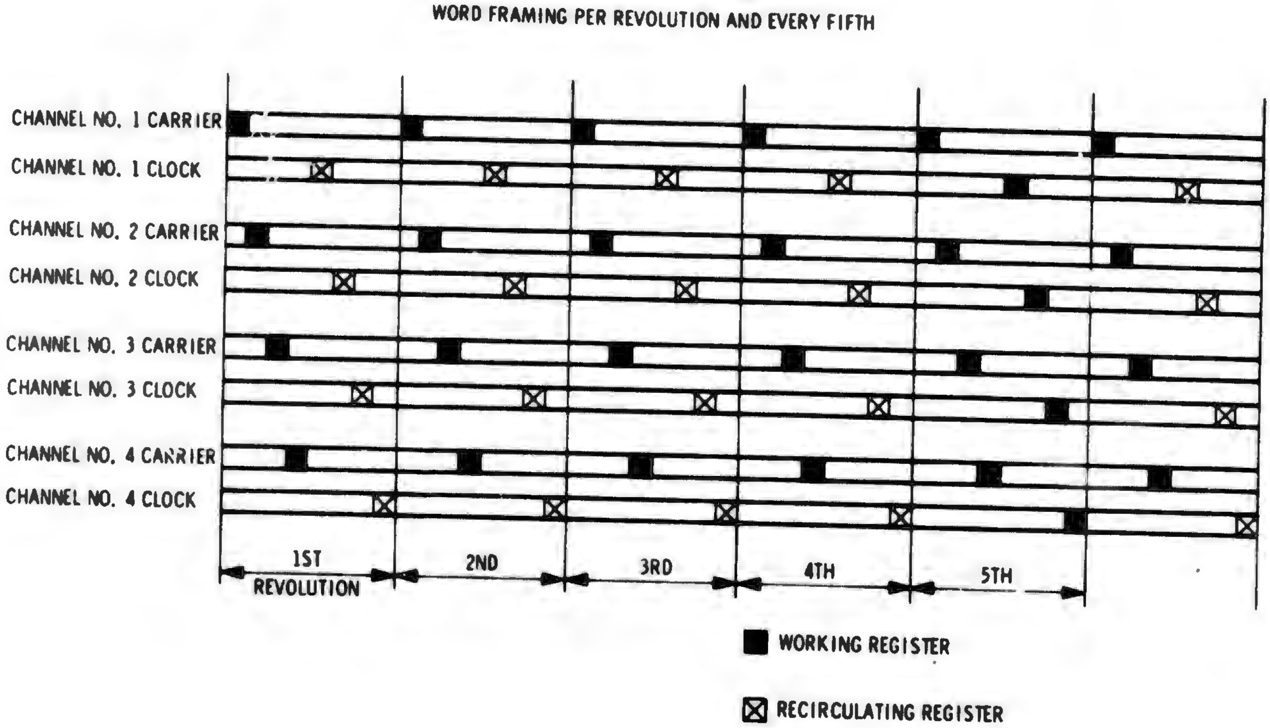


Figure 16. Digital Filter Time Sharing Sequence

There are three basic operations performed in the rate multiplier:

- Four 6-bit input data words are channel addressed and stored during each iteration interval.
- Counter decoders are associated with the stored data.
- Each data word is converted to twos complement and translated to a serial pulse stream which is proportional to offset frequency.

Operations 1 and 2 are combined in a single device called a Content Addressable Memory (cam). The cam device provides for four randomly accessed 2-bit words of read/write/associate storage.

As data arrives serially from the digital loop filter, timing signals are used to enter clock data into a six-stage, serial-shift register. Channel address timing signals are then used to address the cam and, at the end of each iteration interval, the shift register contents are transferred to the cam. Two cam devices are used to process the four least-significant bits for each of the four channels. Separate latch storage is provided for the fifth bit and the sign bit.

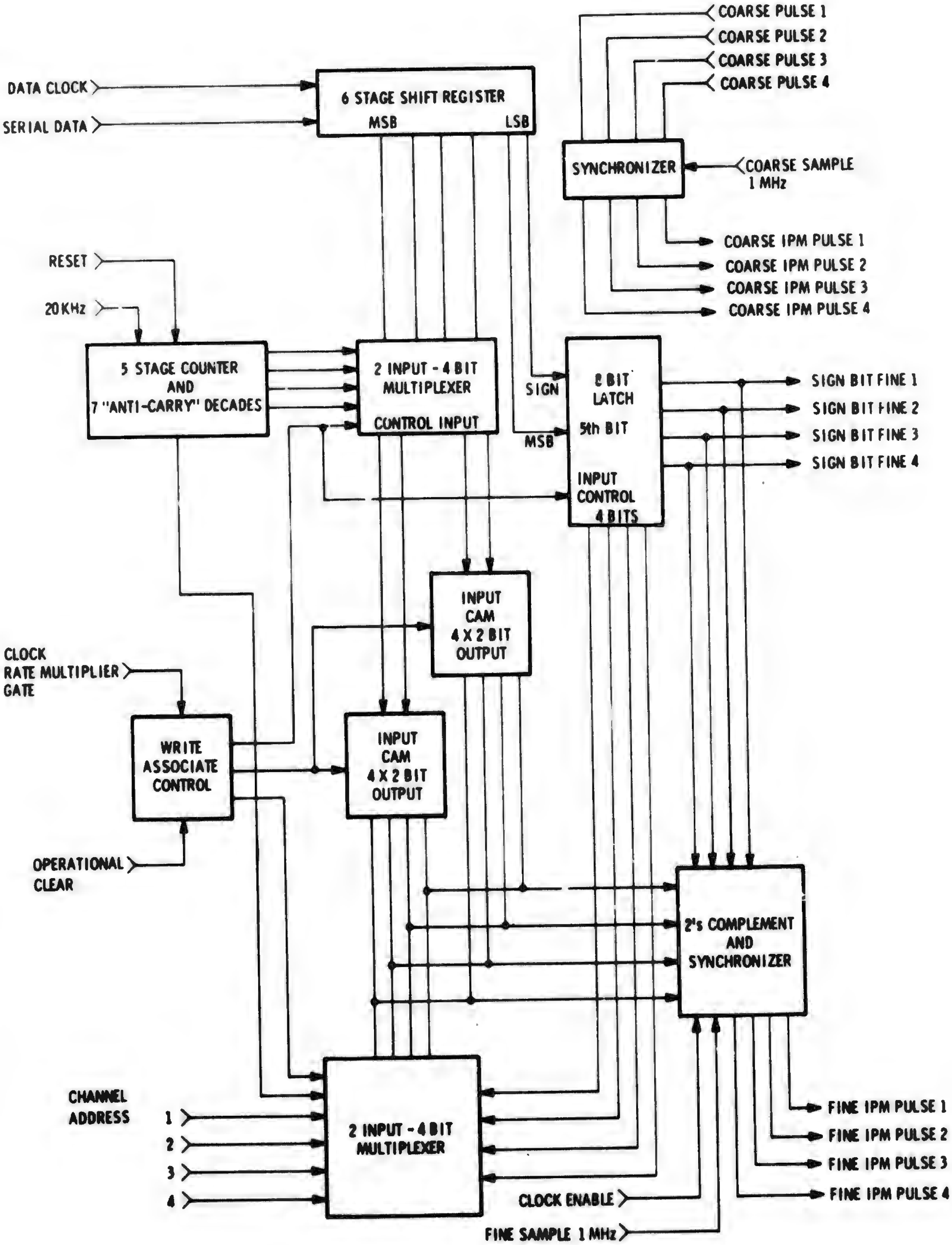


Figure 17. Clock Rate Multiplier - Block Diagram

In the next operation, one of 32 different pulse rates are selected by gating the appropriate outputs of a five-stage counter. Each stage of the counter provides a nonoverlapping sequence.

This card also synchronizes the fine increment output with the coarse increment output to prevent them from being applied simultaneously to the IPM. All increment pulses are synchronized to a 1-MHz clock. Finally, the fine sign bit is supplied as a static "1" for advance, "0" for retard.

2.2.6.2 Carrier Rate Multiplier

The function of the carrier rate multiplier card is to interface the digital loop filter with four carrier incremental phase modulators by means of translating a binary 10-bit word into an evenly distributed rate taken over a fixed iteration interval of 1/624 seconds. This printed-circuit card is the same as the clock rate multiplier with the addition of devices to operate on 10-bit words instead of 6-bit words. Nine stages of ripple binary count, instead of five, provide counter decodes.

The counter is incremented at a 1.6-MHz clock rate. Up to 512 evenly distributed pulses occur every 320 microseconds or at a 3125-Hz rate. The block diagram in figure 18 illustrates the carrier rate multiplier.

2.2.7 INCREMENTAL PHASE MODULATOR

A pair of incremental phase modulators (ipms) are used in each of the four channel processors as shown in figure 19. In the code clock tracking loop an ipm is used to advance or retard the phase of the coder clock in discrete increments of either 1/256 bits or 1/4 bits. In the carrier tracking loop, an ipm is used to advance or retard the phase of the carrier in increments of ±128 Hz.

The two ipms for each processor channel have been conveniently implemented on a common printed circuit assembly shown in figure 20. The mixer and bandpass amplifier circuits are contained on shielded subassemblies on one side of a mother board while the logic circuits are contained on additional assemblies on the other side of the mother board. In addition to holding the subassemblies, the mother board distributes and collects the signals to and from the individual circuits.

Delay variations in the ipm were minimized as they directly effect ultimate range accuracy. Long-term variations in delay are zeroed out during the range calibration mode. However, careful consideration was given in the ipm circuit design to minimize the delay variations as a function of temperature. Tests on the completed ipm design over a temperature range of 0 degrees to 40 degrees centigrade revealed an absolute time drift of 1.3 nanoseconds. In addition, the worst-case tracking difference between two ipm assemblies over the same temperature range was 0.2 nanoseconds.

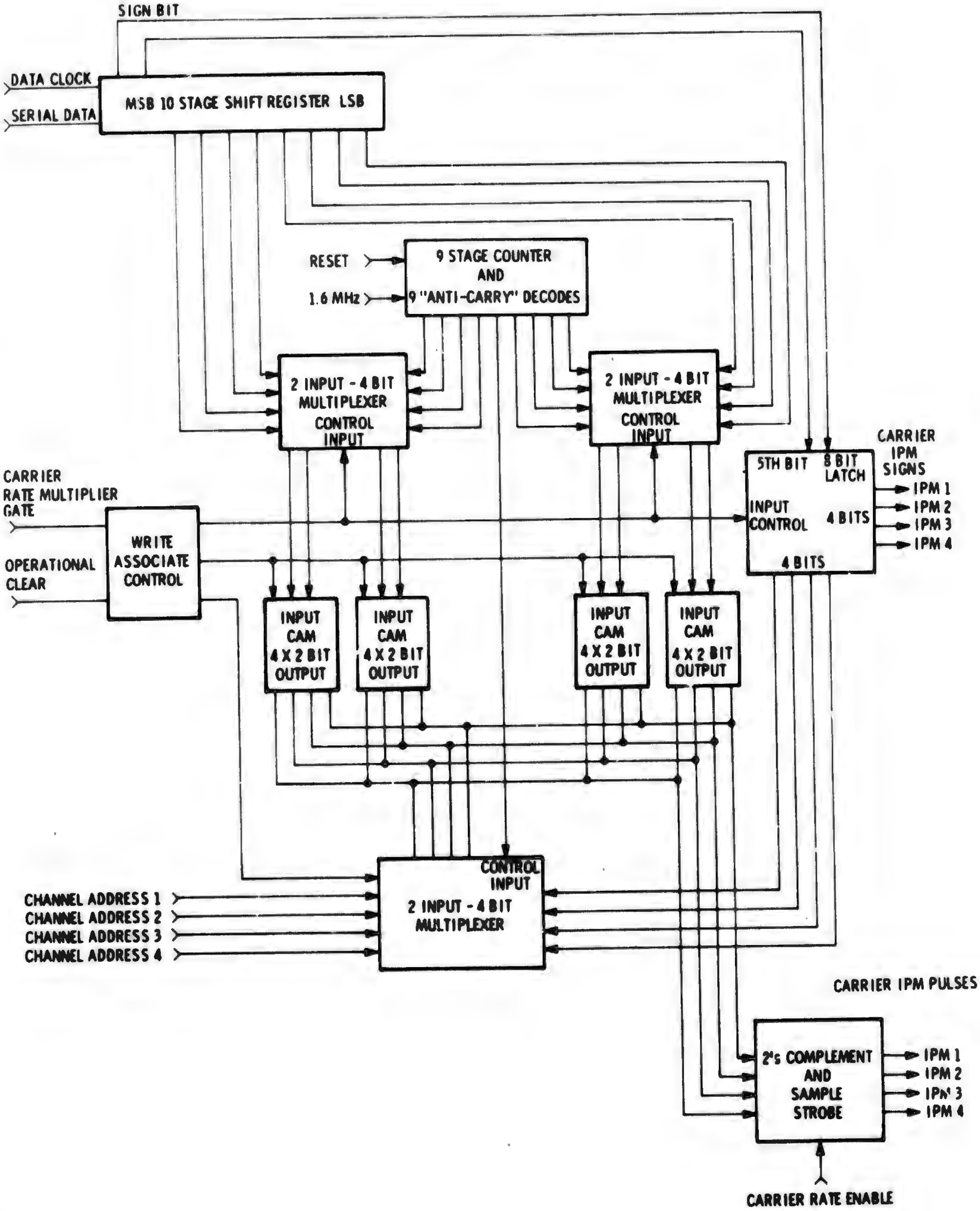


Figure 18. Carrier Rate Multiplier - Block Diagram

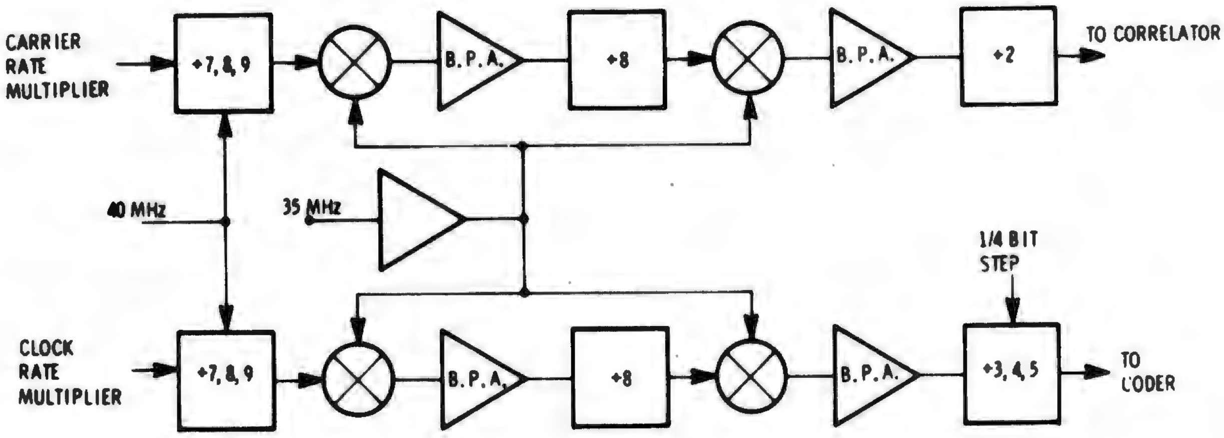


Figure 19. Incremental Phase Modulator Functional Block Diagram

The pertinent specifications of the ipm are as follows:

40 MHz Input

Waveform:	Sinewave
Level:	+7 dBm $\pm$1 dB
Load:	50 ohms
Spurious Response:	-30 dBm maximum

35 MHz Input

Waveform:	Sinewave
Level:	0 dBm $\pm$1 dB
Load:	50 ohms
Spurious Response:	-35 dBm maximum

Fine Step Command

Increment Rate	$\leq 3.3 \times 10^6$ PPS
Level	TTL
Condition for Step	1 step per 0 to 1 transition
1 duration	$\geq 0.15\ \mu s$

Fine Direction Command

Level	TTL "1" Advance "0" Retard
Transition Time	$\geq$25 ns before rise of "step"
Duration till Change	$\geq 0.15\ \mu s$ after step rise

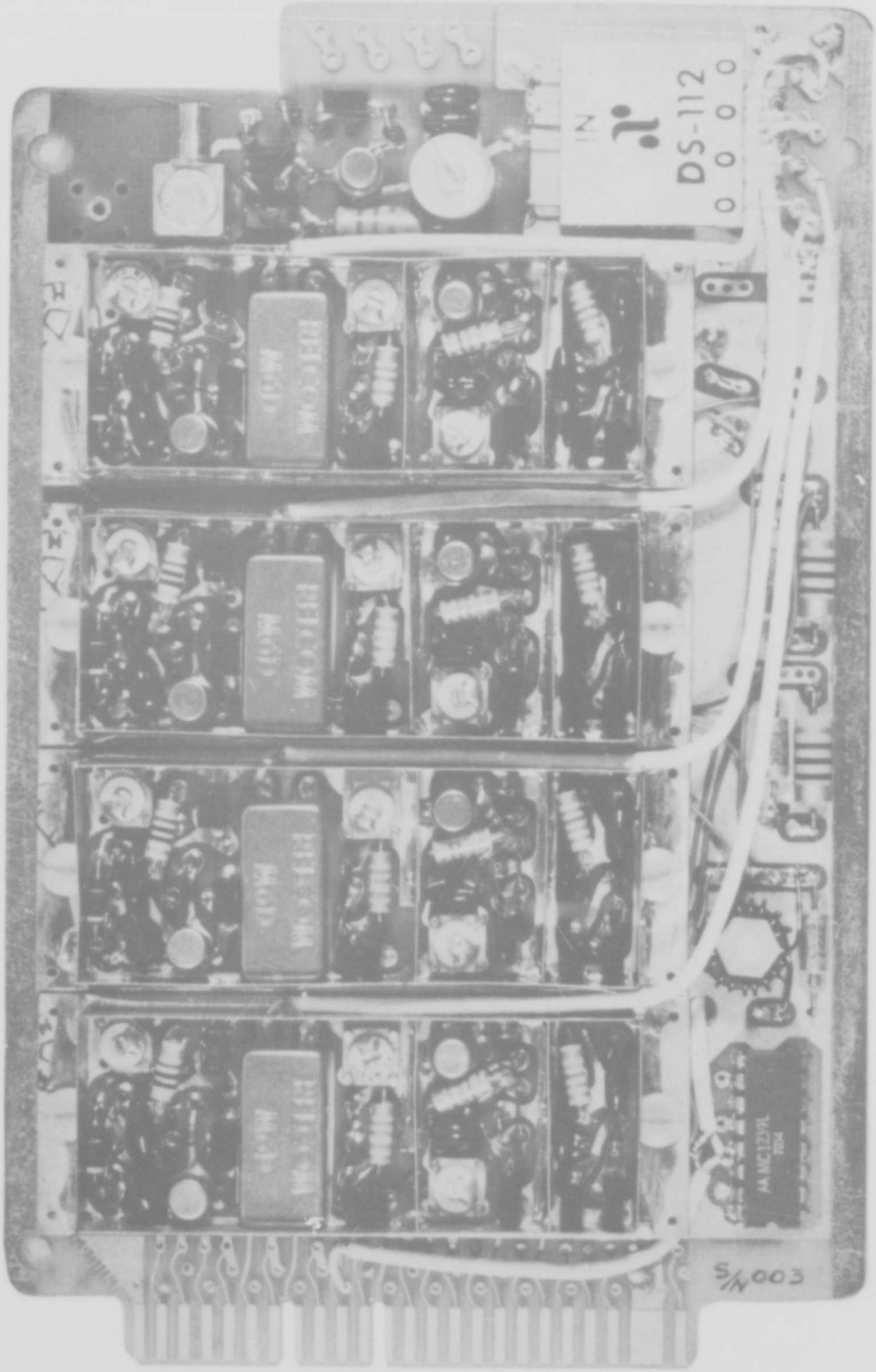


Figure 20. Incremental Phase Modulation Board

Course Step Command

Increment Rate	≤3.3 x 10^6 PPS
Level	TTL
Condition for Step	1 step per 0 to 1 transition
Pulse Duration	>0.15 μs

Course Direction Command

Level	TTL "1" Advance "0" Retard
Transition Time	≥25 ns before rise of course step
Duration till Change	≥0.15 μs after rise of step

Outputs

Frequency	10 MHz ±2.5 MHz 20 MHz ±78 kHz
Load	50 ohms
Level	MECL levels
Waveform	Symmetrical Square Wave

The digital portion of the ipm utilizes extremely high speed MECL III logic. The choice of this logic family was dictated by the requirement that the ipm have absolute minimum propagation delay variation. The MECL III logic provides a typical propagation delay of 1.8 nanoseconds per gate.

The analog circuitry in this ipm consists of a double balanced mixer whose inputs are 5 MHz and 35 MHz driving a 40-MHz bandpass amplifier. This circuitry is used twice in this ipm, since two mixing and filtering operations are required.

The bandpass amplifier stage uses a high F_T transistor (2N918), with a single tuned circuit in the collector circuit. It operates in a Class A mode and is implemented as a common emitter stage and provides the required selectivity to eliminate unwanted mixer products. The nominal output frequency of this stage is 40 MHz and unwanted mixer products can occur ±5 MHz from center frequency. By virtue of the balanced mixer these products are down 20 dB from the desired signal. The lower sideband mixer product at 30 MHz, however, is equal in strength to the desired 40-MHz upper sideband. It is required that all undesired frequencies be down at least 30 dB from the 40-MHz signal level.

2.2.8 CODERS

The experience of Magnavox in the design and use of shift register generators has demonstrated that long maximal linear sequences possess all of the properties required for adequate protection against most jamming strategies. The word "long" used in conjunction with pseudonoise sequences denotes that the period of repetition of the sequence substantially exceeds the receiver integration time. It is also desirable that the sequence be longer than the time uncertainty to be resolved to gain protection against repetitive or spoof jamming. In fact, the pseudonoise sequence should be sufficiently long to prevent a jammer from recording and later rebroadcasting the signal in time sync with a subsequent repetition of the sequence. A register of 25 stages will generate a sequence with a length of about 3×10^7 which will run for about 3 seconds without repetition of that sequence using a 10 MHz clock.

The bit duration of a typical voltage-waveform generated by a linear shift register is inversely proportional to the clock frequency, f_c. Figure 21 is the power spectrum of the sequence; the first zero crossing of the power spectrum envelope occurs at the frequency of the code generator. After translation to the desired rf frequency, the first zero crossings of the power spectrum envelope occur at $f_{RF} \pm f_c$. It can be shown that an rf channel with a 3-dB bandwidth of $1.4\ f_c$ will incur approximately 1 dB of signal power loss. Therefore, a 25-MHz rf bandwidth is well suited for a wideband signal generated from a 10-MHz clock.

When a correlation receiver must extract a signal from an environment which includes other signals modulated with binary sequences which may be maximal linear sequences but which are generated by a shift register having different or related tap connections, then the performance of the system will depend on the cross-correlation function of the binary sequences involved. In such a case, the false alarm rate will be somewhat affected during a reacquisition mode of operation at times when the cross-correlation function of two pseudonoise sequences have high values for particular phase positions. Experience and statistical studies have shown that selected 25-stage maximal shift register generators will meet the minimal correlation properties.

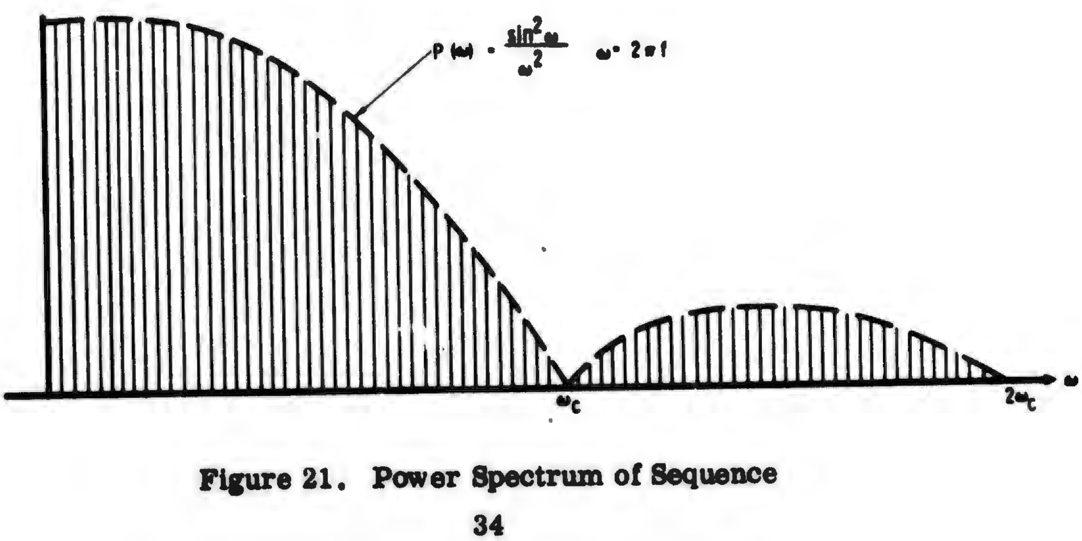


Figure 21. Power Spectrum of Sequence

The coder assembly is a multilayer printed circuit card implemented with integrated circuits. The circuits on the coder card are divided into two relatively independent functions; a pseudorandom code generator operating at a nominal 10-MHz clock rate, and the pseudorange logic for accumulating the 12-most-significant bits of pseudorange data.

The signal processor coder was designed to be compatible with a transmit coder with the format given in figure 22. The long code length is 2^{25} chips, and the coder operates at a nominal 10 MHz. The four-channel code tap selections using a simple shift register generator (ssrg) implementation are as follows:

Channel	Mod-2 Feedback Taps
1	22, 25
2	3, 25
3	13, 21, 22, 25
4	22, 23, 24, 25

The coder actually implemented is a modular shift register generator (msrg). It produces long code sequences identical to the ssrg described above, except for the absence of the 255 bit short code interval immediately following the "all ones" vector of each long code interval. Since the short code interval is not needed for initial acquisition in this receiver, this implementation represents a substantial savings in hardware and power dissipation.

The coder shown in figure 23 can produce different code streams when programmed with one of four code tap connectors. A control signal will logically select the calibrate code stream regardless of which code tap connector is used. Additional features of this coder are the following:

- Injection of "all ones" vector with sync power boost (xspb)
- Detection of all ones vector

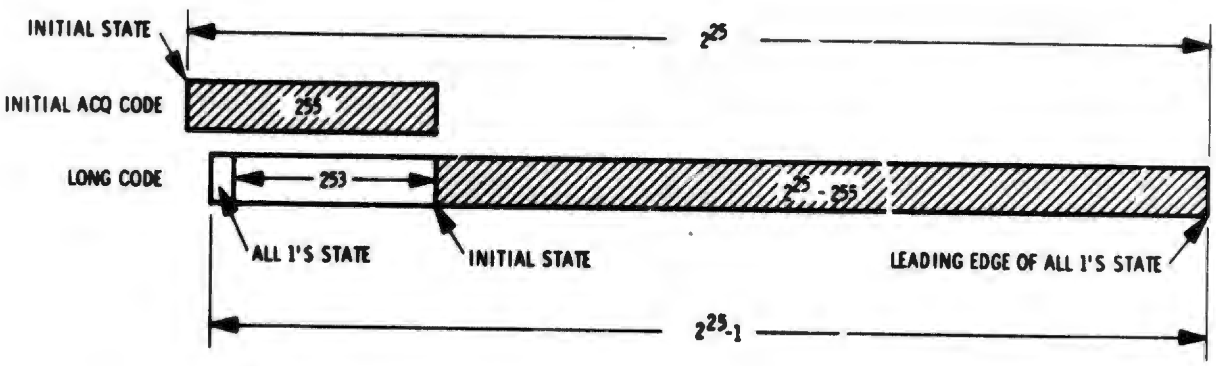


Figure 22. Transmit Coder Format

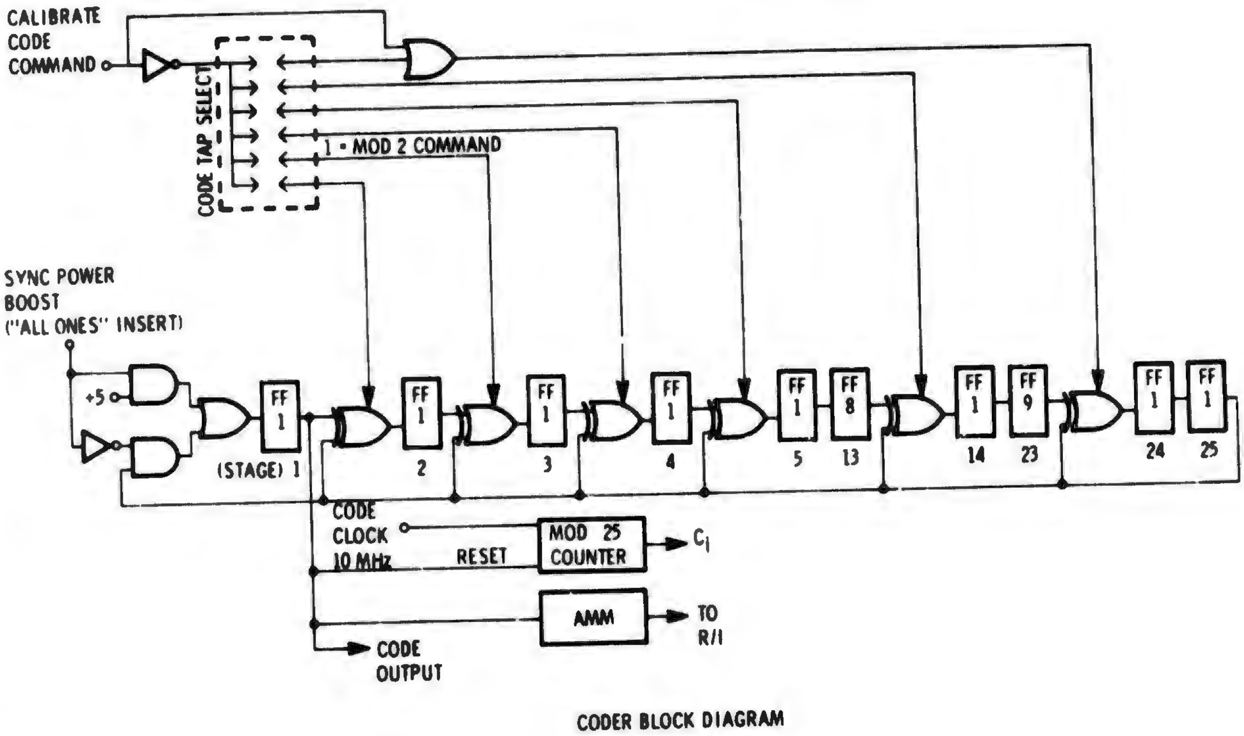


Figure 23. Coder Block Diagram

- Synchronization of code start command
- Detection of sequence generation (automatic malfunction monitoring)

The injection of all ones vector occurs when sync power boost falls. The input to the first flip-flop in the coder shift register chain is held in a "one" state for at least 25 bit times. The coder thus fills up with all ones. Each time 25 ones are counted in a string 25-bits long, a counter outputs a coder incidence (C_i) pulse. Any zeroes in the string reset the counter. After sync power boost rises, the synchronizations circuitry supplies a start pulse of one 10-MHz period to the range circuitry. The edge of the next clock transition enables code start. Automatic malfunction monitoring simply indicates whether or not the coder is generating a sequence.

Implementation of the pseudorange logic is shown in figure 24. Pseudorange data is the accumulation of code phase displacement from some arbitrary but well defined time-of-day vector. The time-of-day vector is generated by a 12-bit counter driven with a common 10-MHz clock reference. This counter is zeroed with a master reset pulse at end of calibration. The counter vector is transferred into an up/down counter upon receiving an end of sync power boost from the coder. All 1-chip displacements of the time-of-day vector from that time on are entered into the up/down counter after fractional bit accumulation by the range extractor circuit card.

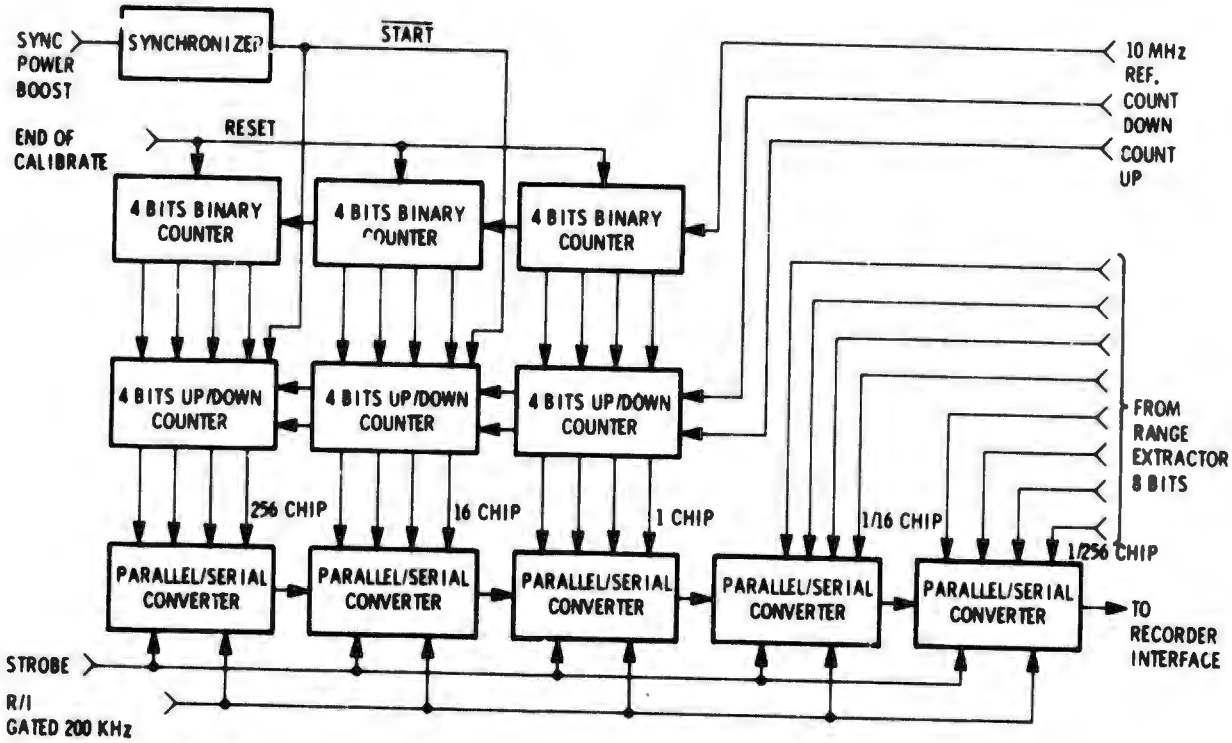


Figure 24. Pseudorange Logic Diagram

Range readouts are only valid if the processor channel is tracking. All four pseudorange counters are simultaneously sampled and pseudorange data entered into a 20-bit parallel to serial converter. The eight least significant bits are brought over with parallel wires from the range extractor card. The serial data is then formatted in the recorder interface buffer memory.

2.2.9 CONTROLLERS

2.2.9.1 Master Controller

The master controller provides a set of control functions for the initialization and acquisition phases of the individual channels. A block diagram of the master controller is shown in figure 25. The frequency estimate status bit (x nonzero) is multiplexed and channel addressed and sent directly to the digital filter from the master controller. Seven system test set switches interface through the master controller by introducing an overriding set of functions which include:

- Standby Enable 1, 2, 3, 4
- Test Sync Power Boost Enable

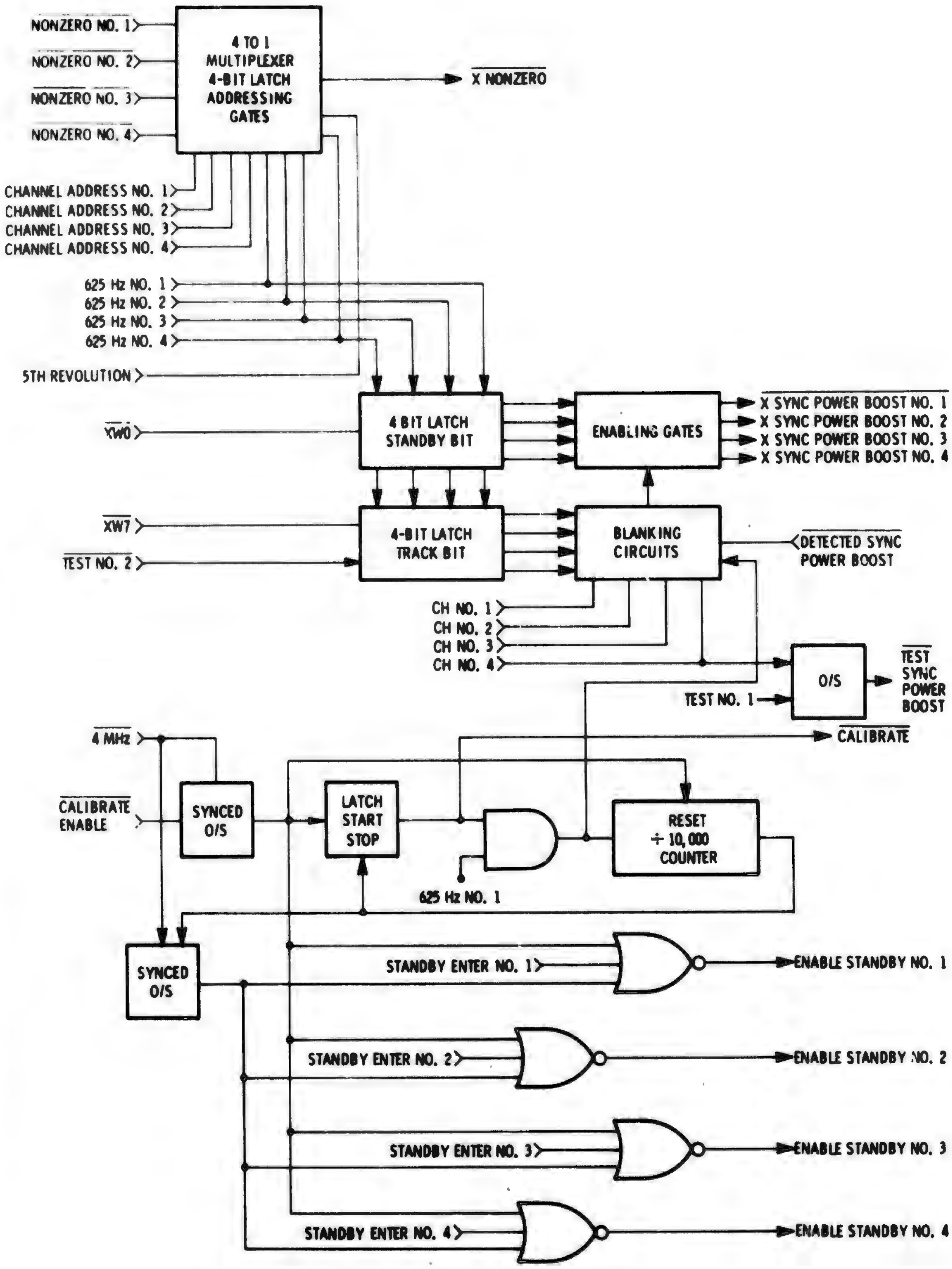


Figure 25. Master Controller Block Diagram

- Calibrate Enable
- Blanking Disable with X Sync Power Boost 1

The master controller contains the logic needed to selectively enable channel acquisition by control of individual sync power boosts. During acquisition, a channel will receive a sync power boost only if it is presently in standby status and if this particular sync power boost has not been blanked by a tracking channel. Blanking occurs if the "all ones" vector of an acquired channel's code aligns with a detected sync power boost. The master controller monitors the standby and track status bits of all channels by demultiplexing X word 0 and X word 7, respectively.

2.2.9.2 Calibrate Mode

Upon system-on or calibrate enable commands, the master controller forces a calibrate sequence by generating command signals. All channel controllers are initialized to standby status, a calibrate pulse of 16 seconds duration is generated, and simulated sync power boost pulses are sent in place of the sync power boost detector pulses to all four channels. At the end of 16 seconds, the channel controllers are reinitialized to standby status and all calibration signals are disabled. At this moment all channels are waiting to be begin their acquisition phase.

In this calibrate mode, each of the four channels simultaneously tracks a common code and a carrier frequency derived from the local frequency reference. During this process the receiver measures the relative delays between the locally simulated transmitter code and the individual channel codes by comparing the respective range accumulators induced as a result of the different electrical paths traversed by the simulated transmitter code. These delays are accumulated in what will be referred to as range registers until the end of the calibrate mode at which point in time the range registers are reset to zero and thereby compensate for the static differential delay among the four channels.

Under normal operating conditions the calibrate mode of operation initializes the signal processor by supplying a CAL code (which is simply a 1, 1, 0, 0 binary sequence at a 2.5 MHz rate) and a 20 MHz fixed frequency CW signal from the frequency synthesizer of the signal processor to the test signal generator in the microwave receiver. (Refer back to figure 6.) This generator provides a 1575 MHz biphase modulated signal at a constant level of -123 dBm to the input of the microwave receiver.

When a calibrate mode is initiated, all 4 channel processor channels switch to a CAL code and acquire the calibrate signal. Sixteen seconds later, after the tracking loops have nulled and AGC transients have settled out, the calibrate signal is removed and a master reset pulse (generated from the 5 MHz reference oscillator) zeros the 4 pseudorange data registers and forces the processor channels to a standby mode to await the arrival of a synchronizing power boost signal.

After a calibrate cycle is completed, any differential delay between processor channels is cancelled and zero range is referenced to the input port of the microwave receiver.

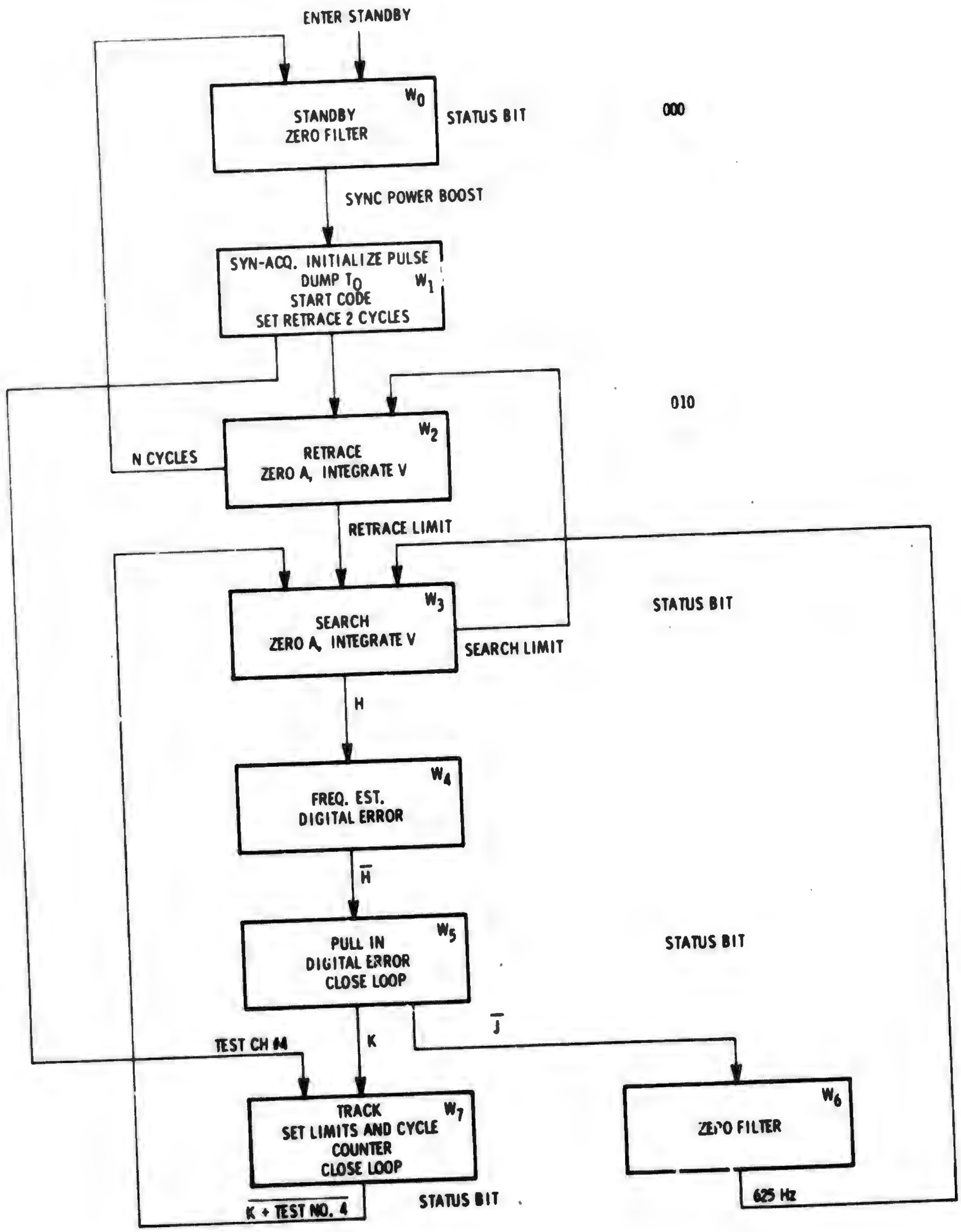


Figure 26. Channel Controller State Diagram

2.2.9.3 Channel Controller

Each channel controller board contains hard-wired programmers for two channels. A reduction in number of output wires is obtained by multiplexing programmer output enable signals. Each programmer duplicates the flow-state diagram of eight words shown in figure 26. Word cycle time is 250 nanoseconds, which is the minimum decision delay of this machine. This design is capable of iterating and counting loops, and weighting multiple exits from selected states. Unconditioned entry points are provided to initialize the program and to force selected test states. Conditional jump decisions are also provided for test modes.

The object of each programmer is to reach word 7 (track state) through the monitoring of channel symptoms and the resultant corrective commands.

A typical initial acquisition sequence for one channel is as follows: Starting from standby, one bit is entered into an eight-stage shift register of the controller. This bit clears the digital filter carrier and clock memory. It also monitors sync power boost and will remain in word 0 (standby) until sync power boost occurs. Word 1 is the next bit in the 8-stage shift register and is entered upon receipt of a sync power boost from the master controller. During word 1, the cocer is initialized and the ipm is advanced until the 1/4 and 1/2 bit positions in the lower 8 bits of pseudorange are zero. If the test switch is in track position, the program would have jumped from word 1 to word 7 and continued to track in word 7 regardless of normal system operations.

At the end of sync power boost, the program advances to word 2 as the upper 12 bits of the range counter are replaced with the present time-of-day counter state. The pseudorange counter can be initialized from any sync power boost that results in a track status. Word 2 enables an advance in code clock relative to a reference 10-MHz rate. During initial acquisition, upon receipt of a sync power boost, the code clock is advanced 512 bits. Upon reaching this retrace limit the program steps to word 3 (search). Search pulses are also counted for 512 bits of code-clock backward movement. The actual mechanism which implements code clock retrace and search is an incremental phase modulator (ipm). The program provides $\pm 1/4$ bit pulses to the ipm during search or retrace. The retrace rate is 1 MHz and the search rate is approximately 1000 chips per second but is dependent upon the sequential search decision circuit. Detection of a search limit jumps the program back to word 2, if H (initial sync decision) did not fire during the search process. If this loop is counted for 4 cycles, the program returns to word 0 (standby). Words 0 through 3 will automatically loop through in the above sequence until H fires during search, at which time a new sequence is developed.

By the time H fires during the search process, an estimate of carrier doppler has been collected. It is scaled and injected into the carrier and clock loop filters. Word 4 enables the injection of a coarse doppler estimate during one iteration of the digital loop filter. The program steps to word 5 and continues to inject fine doppler corrections until the frequency error is within the pullin range of the loop and a track mode is established. During this process the program is waiting for either J (time doppler correction mode) to fall or for K (track mode) to fire, assuming J fired after H fired. If in fact J never fired or does fall before K fires, the program steps to word 6 and zeros the digital loop since the estimated doppler offset was in error due to a false alarm or a combination of events which drive the code out of correlation. For this case, the program loops out of word 6 to word 3 and continues the search sequence for the remainder of counted cycles.

Word 5 (pullin) can enable two exits. One has been described as stepping to word 6 and looping back to search. The remaining exit has priority, that is, if both J fell and K fired simultaneously, the program would jump to word 7 instead. Word 7 (track) closes the loop permanently and prepares the program for a reacquisition process if K falls at any time.

Reacquisition starts as a jump back to word 3 and searches the code clock while maintaining constant velocity by zeroing acceleration in the loop filter per that channel. An expanding search aperture is implemented in small, medium, and large partitions of 16 passes each.

Small	$\pm$256 bits	Δt = 8 seconds
Medium	$\pm$512 bits	Δt = 16 seconds
Large	$\pm$2048 bits	Δt = 64 seconds

If search rate is 1 kHz and retrace is 250 kHz at the bit rate the total reacquisition could take 39 seconds at which time the programmer jumps back to word 0 (standby) or initial acquisition.

2.2.10 RANGE EXTRACTOR

The range extractor (figure 27) is designed to monitor the alterations in coder clock and coder state in order to provide a running sum of range from propagation delay. The range extractor data is in the form of a 20-bit binary word, least-significant-bit equivalent to 1/256 of a code chip. The lower order 8 bits are accumulated

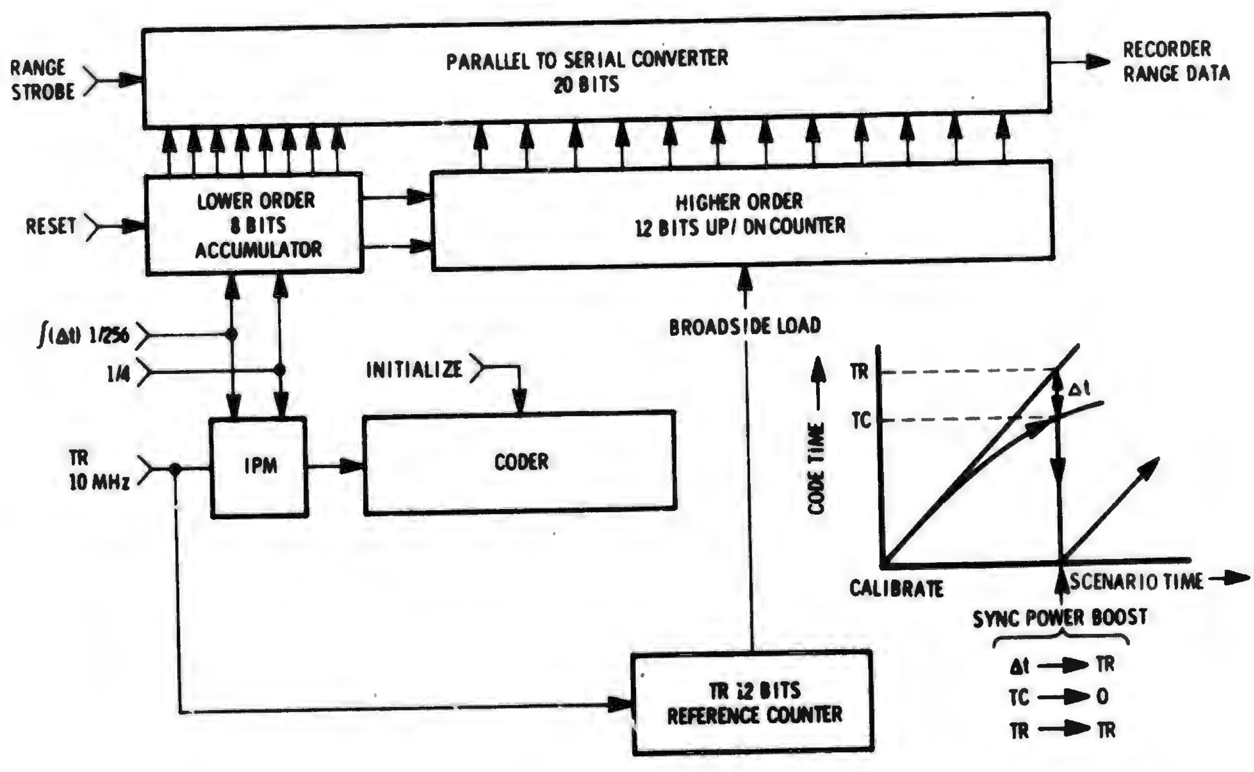


Figure 27. Range Extractor Operation

in two 4-bit parallel adders in order to add in both $\pm$ 1/256 and $\pm$ 1/4 of a code chip during the extrapolated search reacquisition mode. The higher order 12 bits are accumulated in three circuits each containing 4 bits of up/down binary counter. These higher order bits accept, carry, and borrow from the eighth stage of the lower order segment and can also be broadside loaded from a 12-stage binary counter which is running at the 10-MHz reference clock. All 20 bits of range data are converted by a parallel-to-serial converter into a serial format for inputting of the recorder interface range data.

The operational procedure for obtaining range in this manner is entirely automatic and once the system is tracking, range can be monitored to within $\pm$ 1/256 code chip. The main concern of the range data collection is to ensure simultaneous strobing of all four range extractors during system track mode. If any channel breaks lock and enters a reacquisition mode requiring a new code search, a re-establishment of code vector state is also required in the range register. The system utilizes a sync power boost to initialize the coder, and simultaneously enters the reference count from the 12-stage counter into the higher order bits of the range register. The lower order bits are previously adjusted so that the coder block is within 1/4 of a chip of the 10-MHz reference clock. This allows unambiguous broadside load of the running reference count. Prior to any system-track mode, the calibrate mode is entered in order to let all four channels track the reference coder and enters all zeros in the lower eight-order bits of range which establishes reference clock phase data.

2.2.11 DOPPLER EXTRACTOR

The doppler extractor (figure 28) is designed to monitor carrier frequency tracking data by integrating this data over 0.1 second in a binary format of 20 bits, with the least significant bit weighted at 1/128 carrier chip. Carrier-track data is available in pulse and sign digital signals. Therefore, by counting pulses weighted at 1/128 carrier chip and using the sign bit for directing an up/down binary counter

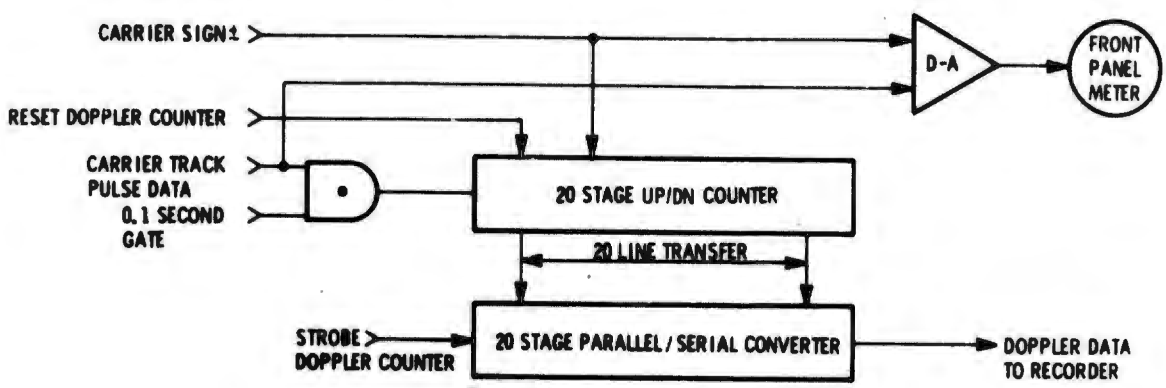


Figure 28. Doppler Extractor

over a range of 20 stages and over an interval of 0.1 seconds between clearing of this counter, doppler information is obtained. This 20-stage, up-down counter is strobed each 0.1 second and dumped into a 20-stage, parallel-to-serial converter for serial doppler data interfacing the recorder. Carrier track data is also displayed on the control box by meters. The pulse and sign data is integrated but not dumped in a digital-to-analog converter which drives the meter movement.

2.2.12 VELOCITY DIGITAL-TO-ANALOG CONVERTER

This circuit converts the doppler pulses from the carrier-rate multipliers to an analog voltage which is displayed on the control-display panel velocity meters (see figure 29).

The doppler pulses can occur at a maximum rate of 400 kHz. The sign bit is 1 for a positive velocity and 0 for a negative velocity. A positive sign pulse is inverted at the input to the upper exclusive or causing the one-shot to fire on a doppler pulse. This output is integrated through the R-C integrator and the analog current drives the meter. Alternatively a negative sign bit causes a negative current through the integrator and the meter.

Lamp drivers for the control/display panel are also located on the velocity digital-to-analog converter card.

2.2.13 RECORDER INTERFACE

The recorder interface performs the function of strobing each processor channel for range, doppler, and status data. It sequentially stores and frames these 32-bit words into one 2560-bit word for the airborne data acquisition system. It also sends each processor channel a multiplexer clock which controls two 20-bit, parallel-to-serial registers associated with the range and doppler for each channel. Every 0.2 second a strobe line parallel loads the registers in each channel processor. The serial data is then multiplexed into a memory which stores five sets of data each second. Once per second this storage is transferred to the airborne data acquisition system along with a 32-bit Barker sequence preamble. A logic diagram of the recorder interface is shown in figure 30, and a timing diagram is shown in figure 31.

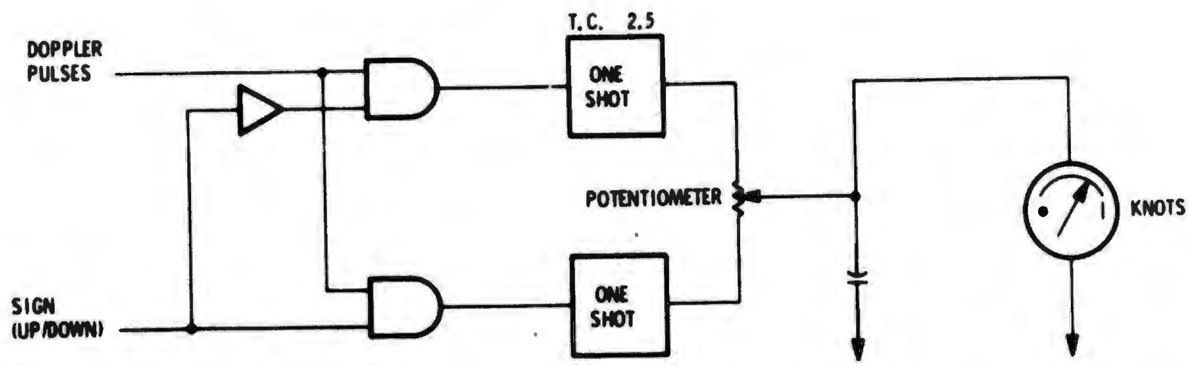


Figure 29. Velocity Digital-to-Analog Converter

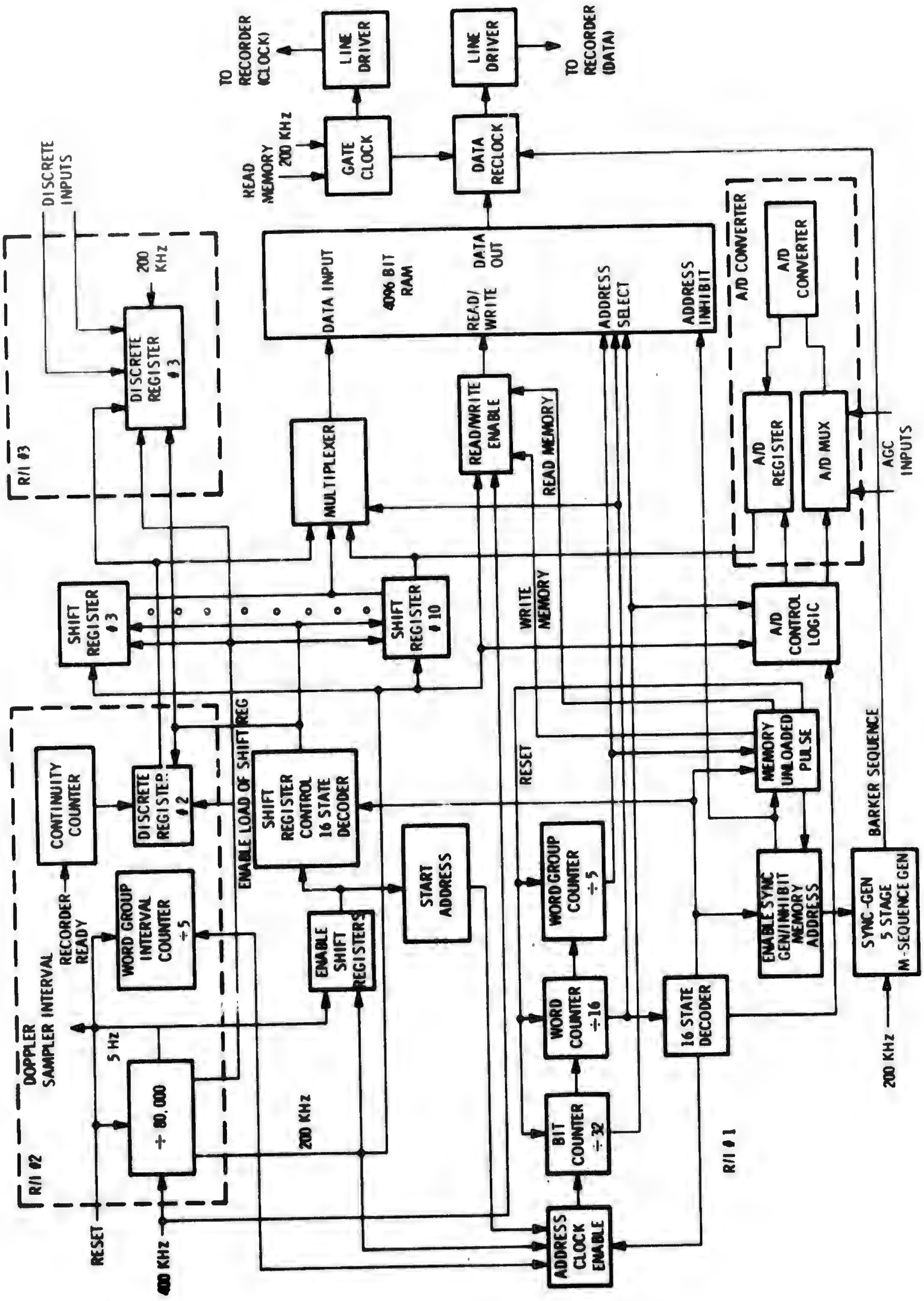


Figure 30. Recorder Interface Block Diagram

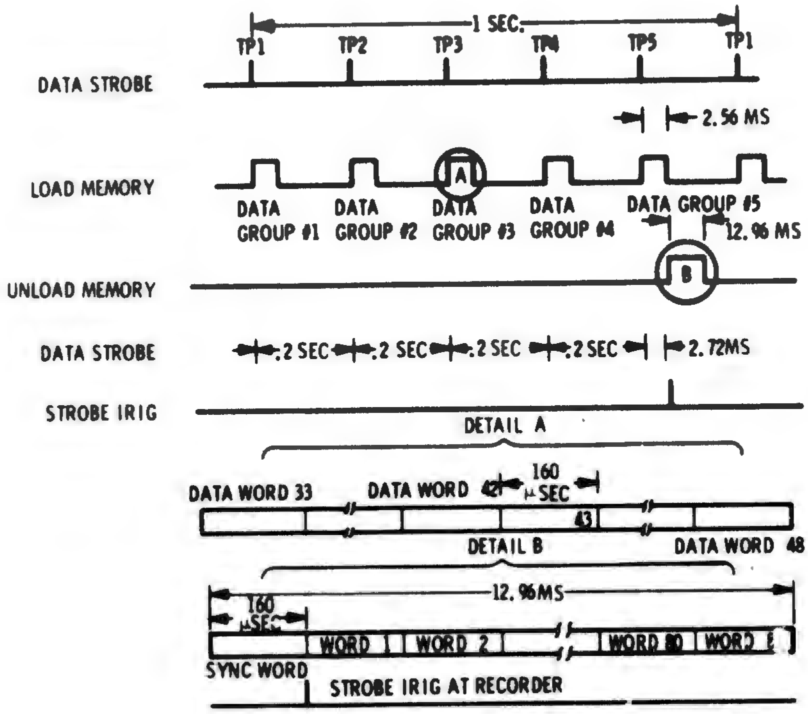


Figure 31. Recorder Interface, Timing Diagram

The recorder interface logic has been implemented on three printed-circuit assemblies which were constructed using point-to-point wiring techniques. The fourth card which is also part of the recorder interface group is an analog-to-digital converter assembly.

Recorder Interface #1, shown in figure 30, contains a 4096 bit random-access memory (ram) addressed by a 12-stage counter. Sixteen parallel signals are multiplexed and sent to the memory every 0.2 seconds. The output data from the memory is serially shifted out once per second. It is preceded by a sync word, reclocked and sent to the airborne recorder.

The first five stages of the address counter are the word counter. One cycle of this counter addresses 32-bit locations in memory (one word). The next four stages are the word group counter, one cycle of this counter addresses 16 word locations (word group). The next three stages are the frame counter, one cycle of this counter addresses five-word group locations (a frame).

The clock to the address counter is enabled by a start address clock pulse and disabled after a word group is loaded into memory once every 0.2 second. With the exception of the fifth time interval, the clock is not disabled after a word group continues running. The sync generator is enabled for a 32-bit period once per second, after which the address counter is reset. The memory is placed in the read mode and the entire contents of the memory is read out to the airborne recorder after which time a pulse is generated which disables the clock to the address counter, resets the address counter and generates a memory unloaded pulse. When the memory is placed into the write mode nothing happens until a start address clock pulse is received.

The multiplexer is controlled by the word-group counter. In addition, a 16-state decoder decodes the states of the word-group counter which enables the various remote-word registers.

The sync word is generated by a five-stage, m-sequence generator which is preset and enabled by address inhibit signal.

The read-write logic for the memory is controlled by the read-write flip-flop. The read-write signal is a 200-kHz square wave offset by one quarter period from the 200-kHz square wave that drives the address counter.

Recorder Interface #2 consists of a divide by 80,000 counter followed by a divide-by-five counter. The input to the divide by 80,000 is a 400 kHz square wave producing a 5-Hz, square-wave output which is used to gate range and doppler counters. The 5-Hz square wave in turn, drives a divide by five which produces a 0.2 second pulse every second. In addition, the 5-Hz square wave fires a Schmitt trigger which generates five short address clock pulses every second. These pulses are used to enable the address counter on Recorder Interface #1. The data clock is obtained from the first stage of the divide by 80,000.

In addition, this board contains a 32-stage parallel load serial shift status register, automatic malfunction monitor combining logic and a recorder ready pulse stretcher which lights a lamp on the control display panel for 0.2 seconds each time a recorder ready pulse is sent from the airborne recorder.

Recorder Interface #3 contains a 32-stage parallel load serial shift status register along with coder automatic malfunction monitor combining circuitry. In addition, a three-stage, analog-to-digital address counter is located on this board for use in multiplexing the six agc signals.

Recorder Interface Data Format

Figure 32 shows the format of recorder interface data. Notice that data words 1 through 16 are collected five times during each frame and that frame word 1 is a sync word which is not repeated but precedes the 80 data words upon delivery to the airborne recorder.

Frame Word 1 – This is a data synchronizing word. It consists of a 32-bit Barker Sequence which contains the desired correlation properties for synchronizing a serial data stream, even under noisy line conditions which result in bit errors.

Data Word 1 – The first 8 bits represent the flight number which is programmed using two thumwheel switches at the control-display panel. The remaining 24 discrete bits represent the modes of operation in each of the four processor channels and their assignment is shown in table II.

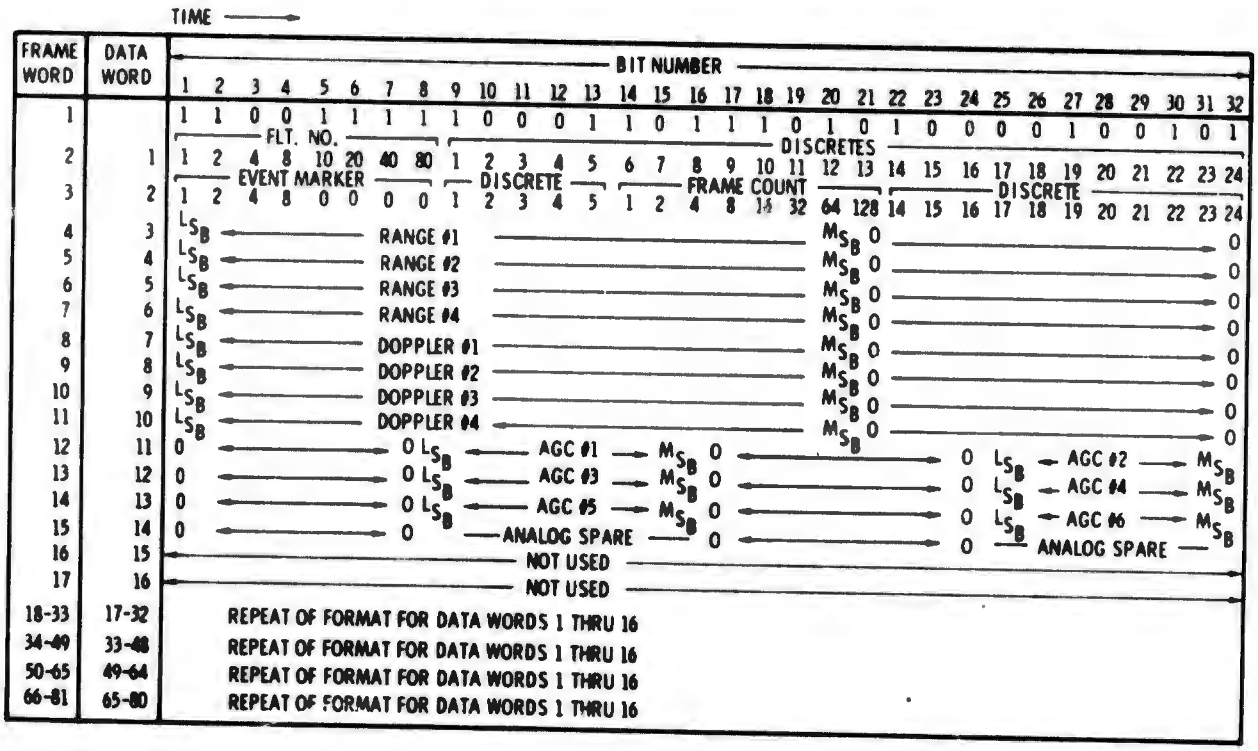


Figure 32. Recorder Interface Data Format

Table II. Discrete Bit Assignment

Channel Number	Stand By	Search	Pull In	Track	Code AMM	Spare
1	1	2	3	4	5	6
2	7	8	9	10	11	12
3	13	14	15	16	17	18
4	19	20	21	22	23	24

Data Words 2 – The first 4 bits represent the event marker numbei which is programmed using one thumbwheel switch at the control-display panel. Bits 14 through 21 represent a mod -128 frame counter output. This counter is toggled with 1 second ticks and its starting vector is arbitrary. The repeating 128 count sequence may be used as a diagnostic tool during data reduction to determine if the airborne recorder has skipped any frame. The discrete bit assignments for data word 2 are listed below:

1.	Synthesizer Automatic Malfunction Monitor
2.	Microwave PLL Automatic Malfunction Monitor
3.	Magnavox Research Laboratories/Hazeltine
4.	Calibrate Mode
5.	RF Signal Present
6-13.	Frame Count
14-24.	Spares

Data Word 3 through 6 – Represent pseudorange data for processor channels 1 through respectively. The digital weighting factors for each pseudorange word is given below

- Code phase of arriving signal minus code phase of (imaginary) airborne standard code
- 20-bit number (straight binary)
- Least significant bit = 1/256 code element duration

NOTE: Pseudorange is modulo 4096 chips (68 nautical miles)

Data Words 7 through 10 – Represent pseudodoppler data for processor channels 1 through 4 respectively. The digital weighting factors for each pseudodoppler word is given below:

- Frequency of arriving signal minus frequency of airborne reference averaging over 1.0 seconds just preceding the 6 per seconds sample time.
- 20-bit number (straight binary)
- Least significant bit = 10/128 Hz

NOTE: Negative values appear in twos complement form.

Data Words 11 through 13 – Contain six 8-bit agc words. The weighting of each agc word is given in the engineering performance data of section III. After converting and combining these six agc words in the software program, the signal level of each processor channel can be determined to within ±1 dBm. The agc designations are given below:

AGC 1	Channel 1
AGC 2	Channel 2
AGC 3	Channel 3
AGC 4	Channel 4
AGC 5	Maximum agc
AGC 6	Noncoherent agc

Data Word 14 – Represents two spare 8-bit analog-to-digital outputs.

Data Words 15 and 16 – Are not used.

2.2.13.1 Recorder Interface Specifications

The interface between the 621B User Receiver and the airborne recorder buffer is shown in figure 33. Additional specifications for this interface are given below:

- Data (from Receiver)

Frame Length	2560 bits (fixed)*
Words/Frame	80*
Word Length	32 bits (Fixed)
Format	NRZ
Gating	None
Sync Word	32 bit maximal sequence (Refer to Receiver Data Format Diagram)

- Clock (from Receiver)

Rate	200 kHz (nominal)
Gated or Continuous	Gated
Duty Cycle	50%
Clocking Edte	"1" to "0" transition

- Output Interface (from Receiver)

Levels	TTL
Source	100Ω (resistive)
Cable	RG 195
Connector	T.N.C. Female

- End of Frame (from Recorder)

Type of Signal	Pulse
Rate	1 pulse/sec
Duration	3μ S nominal
Rise Time	<30 nS

*Does not include sync word.

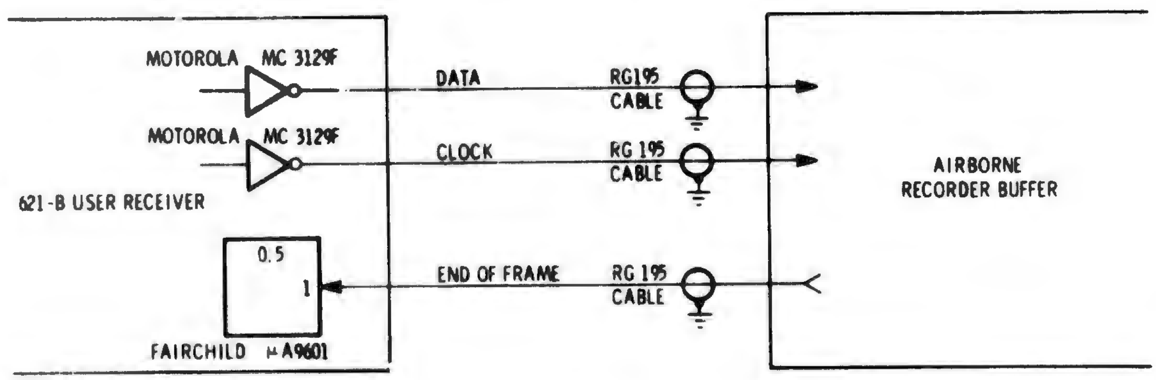


Figure 33. Recorder Buffer Interface Diagram

2.2.14 FREQUENCY SYNTHESIZER

All of the fixed frequencies required by the signal processor are generated on frequency synthesizer boards 1 and 2. All signals are generated from a stable 5-MHz frequency standard. Synthesis is accomplished using step recovery diodes for multiplication, double-balanced mixers for summing and emitter-coupled-logic (ecl) for division. A block diagram of the frequency synthesizer for the signal processor is shown in figure 34.

The two synthesizer boards were constructed on standard size boards using a combination of printed circuit wiring in the critical rf circuit areas and point to point wiring in the low frequency and dc signal areas. Figure 35 shows one of the frequency synthesizer boards.

Synthesizer Requirements

- 5 MHz Output

Number of Outputs	One
Level	TTL
Waveform	Square Wave
Destination	PC Receiver 1

- 8 MHz Output

Number of Outputs	One
Level	TTL
Waveform	Square Wave
Destination	Filter Timer

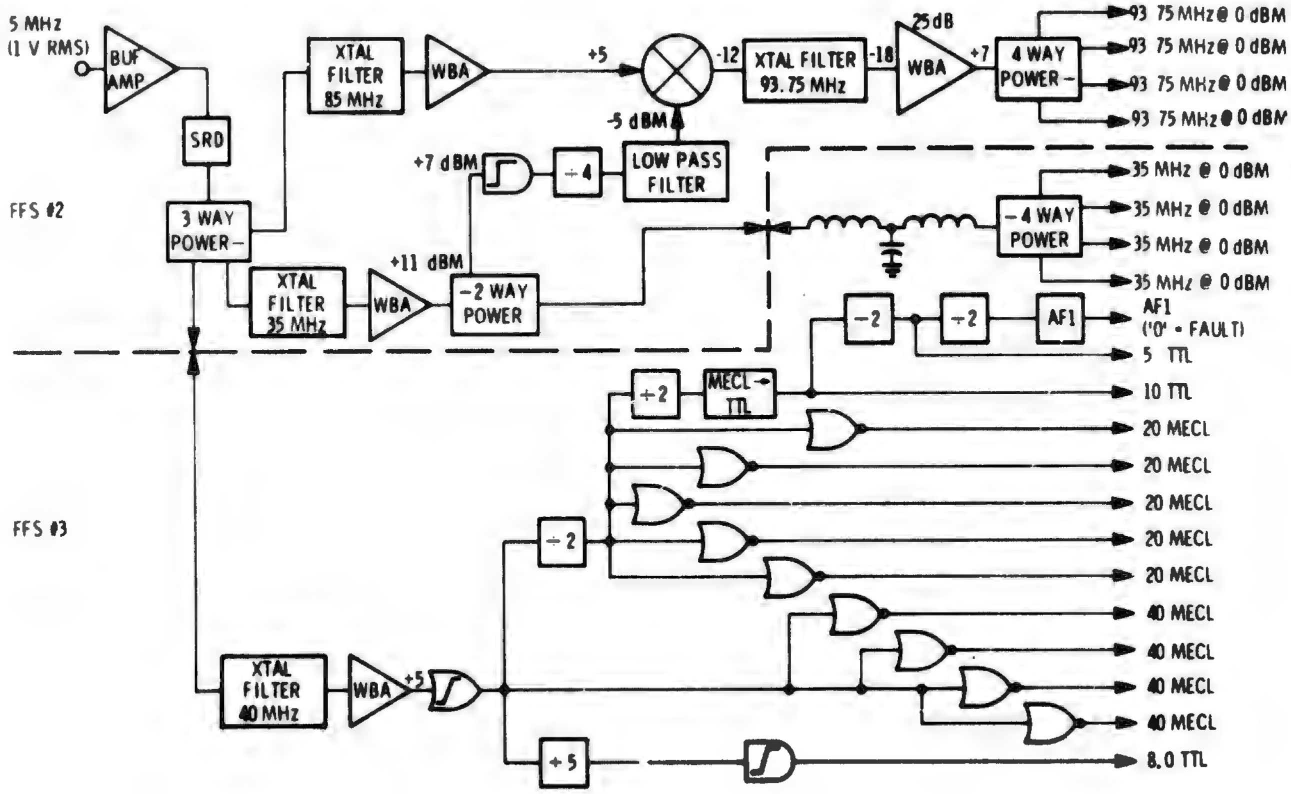


Figure 34. Frequency Synthesizer Diagram

- **10 MHz Output**

Number of Outputs	Five
Level	TTL
Waveform	Square Wave
Destination	Coders

- **20 MHz Output**

Number of Outputs	Five
Waveform	Square Wave
Level	ECL
Load	50-ohm nominal (each)
Destination	IF Assy and FFS 1

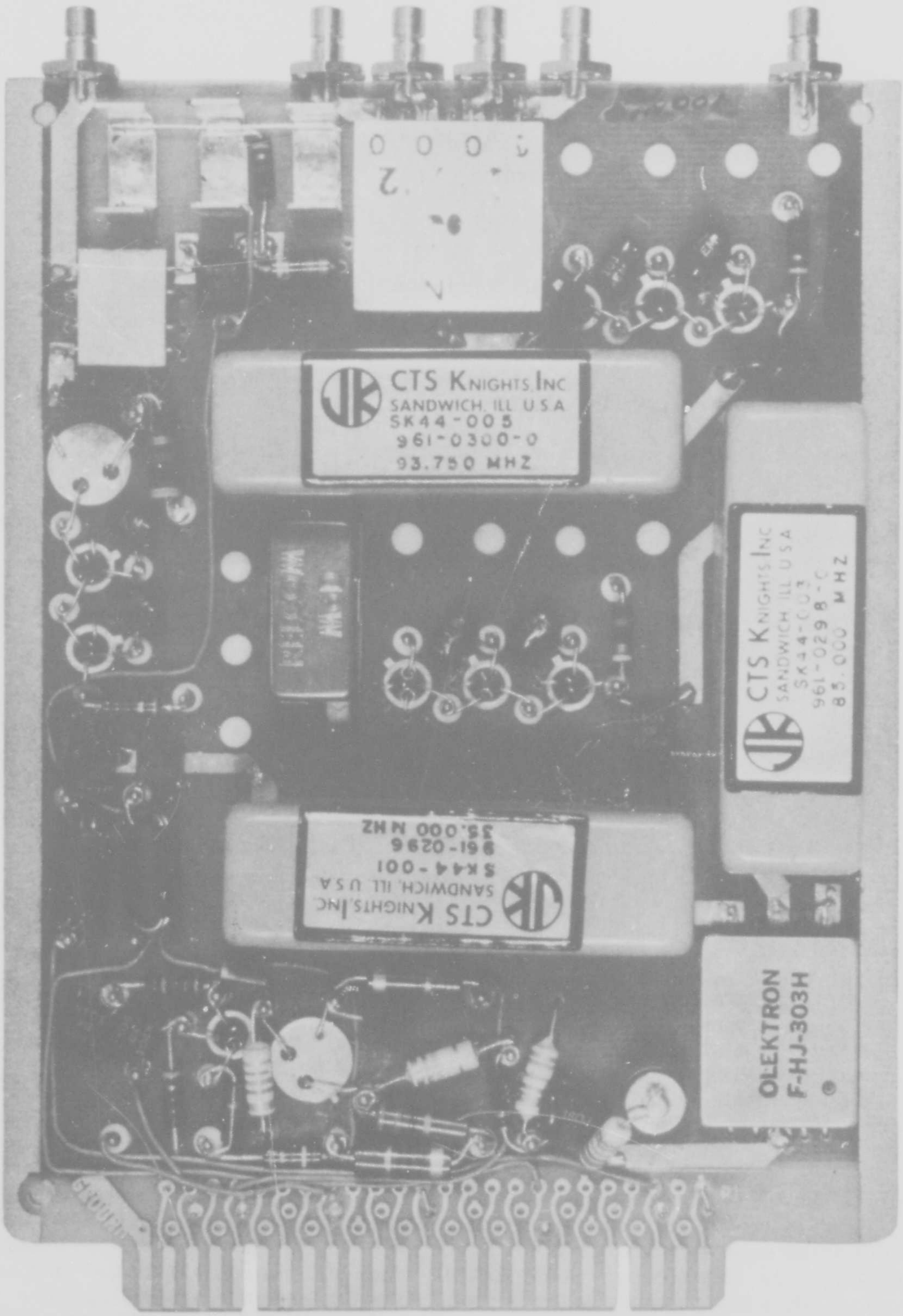


Figure 35. Frequency Synthesizer Board

- 35 MHz Output

Number of Outputs	Four
Waveform	Sine Wave
Level	C dBm $\pm$1 dB
Load	50-ohm nominal (each)
Spurious Responses	-40 dBm max.
Destination	IPM

- 40 MHz Output

Number of Outputs	Four
Waveform	Square Wave
Level	ECL
Load	50-ohm nominal (each)
Destination	IPM

- 93.75 MHz Output

Number of Outputs	Four
Waveform	Sine Wave
Level	0 dBm $\pm$1 dB
Load	50-ohm nominal (each)
Spurious Responses	-40 dBm max.
Destination	Correlators

Figure 36 shows how the 30-MHz and 93.75 MHz signals are generated. The 35-MHz signal is generated by multiplying 5 MHz by seven using a comb generator and a crystal filter to provide spectral purity. Four separate outputs were provided by using a four-way hybrid splitter. The 93.75-MHz signals were generated by synthesizing an 85-MHz signal and mixing with 35 MHz divided by 4. A crystal filter at 93.75-MHz was used to provide spectral purity.

The comb generator consists of three parts: a driver, a step recovery diode, and an output matching network. The step recovery diode has the capability of being driven in the recerse conduction state for a time controlled by the depletion rate of the majority carriers about the pn junction. When the pn junction becomes depleted, the step recovery diode abruptly shuts off, typically in the low pico seconds region and a sharp voltage spike is produced which is rich in harmonics of the fundamental. A matching network is employed to match the diodes low impedance to its respective crystal filter loads for extraction of the desired frequencies from the generated comb.

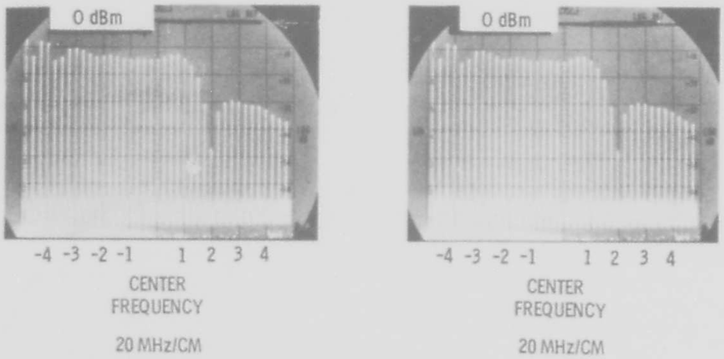


Figure 36. Comb Generator Output Spectrum

Figure 36 shows a typical output spectrum of the step recovery diode circuit used in the frequency synthesizer. The "tooth" notched out in the photo is 135 MHz; sweep speed of the spectrum analyzer is 20 MHz per centimeter; the "teeth" of the comb are spaced at 5-MHz increments.

A common wideband amplifier was used throughout the synthesizer design. This flexible design provides a wide range of gain variation, flat frequency response out to 200 MHz, low harmonic distortion at output levels up to + dBm and excellent temperature characteristics. The design is straightforward using common collector stages for gain and a common emitter stage for impedance matching of 50 ohms at the output. The response of this amplifier along with the relative second harmonic distortion at an output level of +5 and +12 dBm is shown in figure 37.

To insure the requirements for high spectral purity, crystal filters were used extensively in the frequency synthesizer design. The specifications for the various crystal filters are given below:

- Passband Characteristics: The bandwidth and insertion loss of each filter shall be such that the attenuation of the defined center frequency (above) shall be attenuated no more than 6.0 dB across all environmental conditions.
- Stopband Characteristics: The attenuation of each filter shall be 40 dB (minimum) from 5 MHz to F_o - 5 MHz and F_o + 5 MHz to 120 MHz.
- Temperature Range: 0 degrees to 70 degrees centigrade
- Source and Load Impedance: 50 ± 10 ohms in parallel with a capacitive component of 0 to 15 pf.
- Case Size: 1/2 inch high by 1.0 inch wide by 2.375 inches long (maximum sizes).

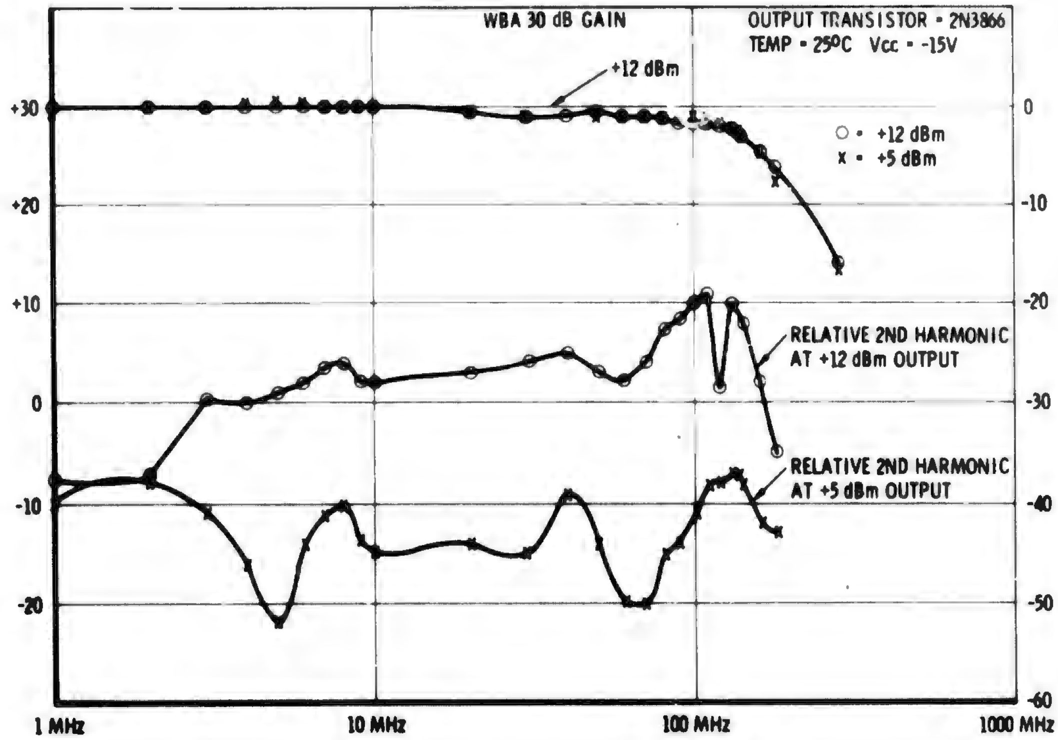


Figure 37. Wideband Amplifier Characteristics

The design of fixed frequency synthesizer number three (FFS 3) is similar to the design of FFS 2. Additionally, however, emitter coupled logic was used to divide 40 MHz down to 8 MHz. An ECL logic family manufactured by Motorola (MECL) was used to provide the high-speed countdowns. The ECL/TTL level converters were used to transform lower frequency squarewaves to TTL levels.

2.3 MECHANICAL DESIGN

2.3.1 SIGNAL PROCESSOR PACKAGING

The signal processor packaging shown in figure 38 is a basic 1-1/2 ATR size, 15.38 inches wide by 7.63 inches high by 18.1 inches long. The design is generally in accordance with the requirements of MIL-C-172 for an MS91403 case. Total weight, including electronics is 36 pounds. Basic construction of the unit is sheet aluminum, with integral honeycomb sections which, in addition to structure, allows free passage of cooling air and rfi protection between rows of circuit cards. A standard mounting arrangement is provided for mounting in MS91405 type mounting tray. The internal card rack is divided into three sections separated from each other by the honeycomb partitions. Each section is further divided into functional groupings of printed-circuit cards separated by rf shields. Figure 39 is a plan view indicating card locations. Packaging of the circuit elements makes broad use of microelectronic techniques. The circuit cards, supported in the case by means of metallic card slides, plug into printed circuit edge connectors located on the connector plate at the bottom of the unit. The circuit card outline is depicted in figure 40.

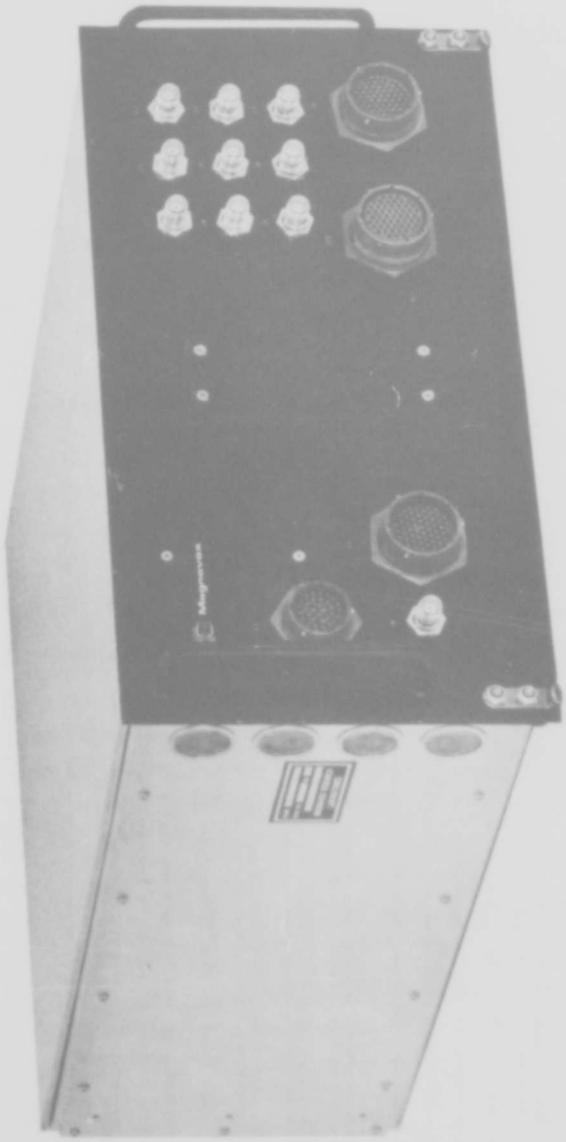


Figure 38. Signal Processor

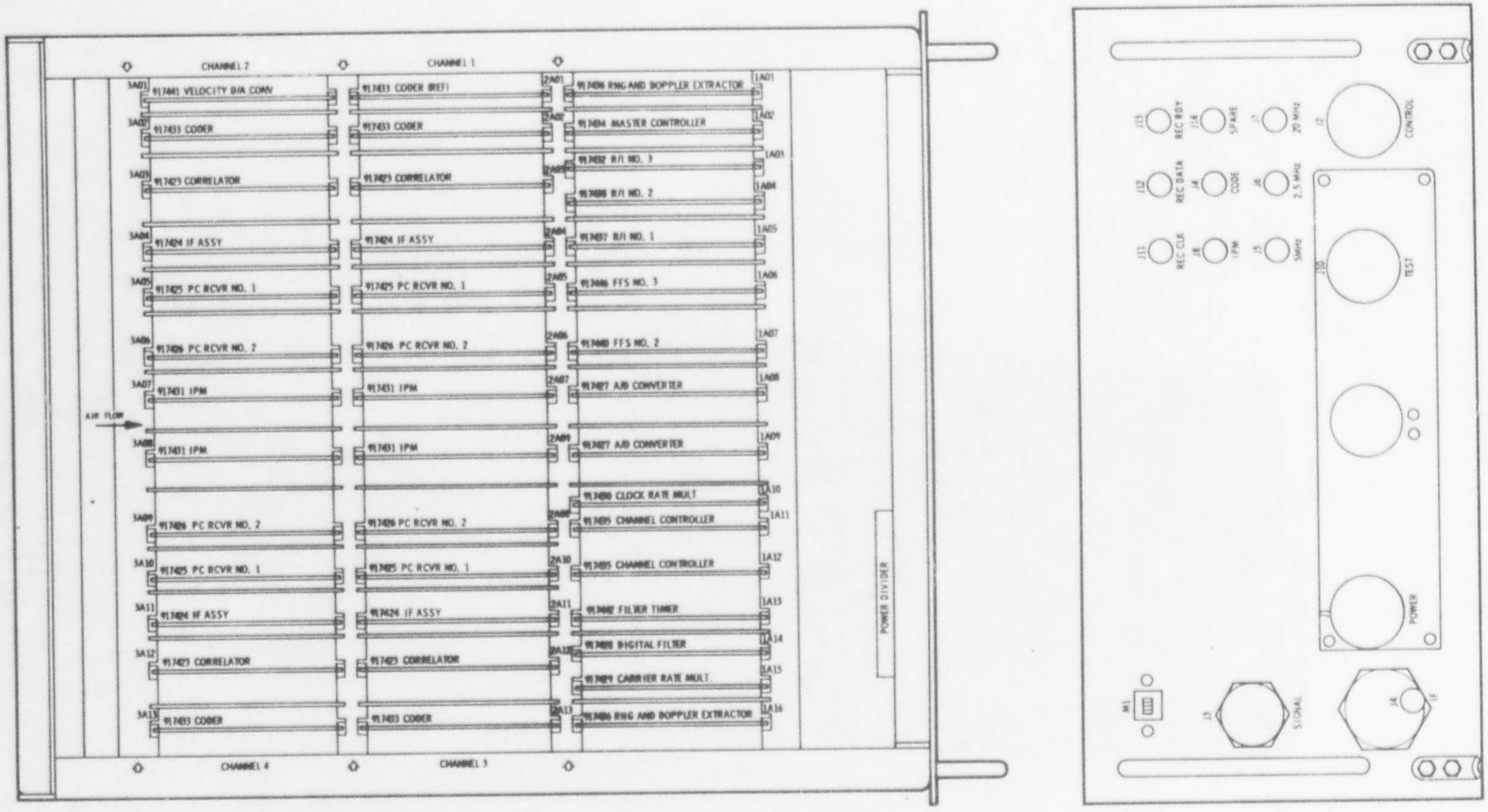


Figure 39. Signal Processor Plan View

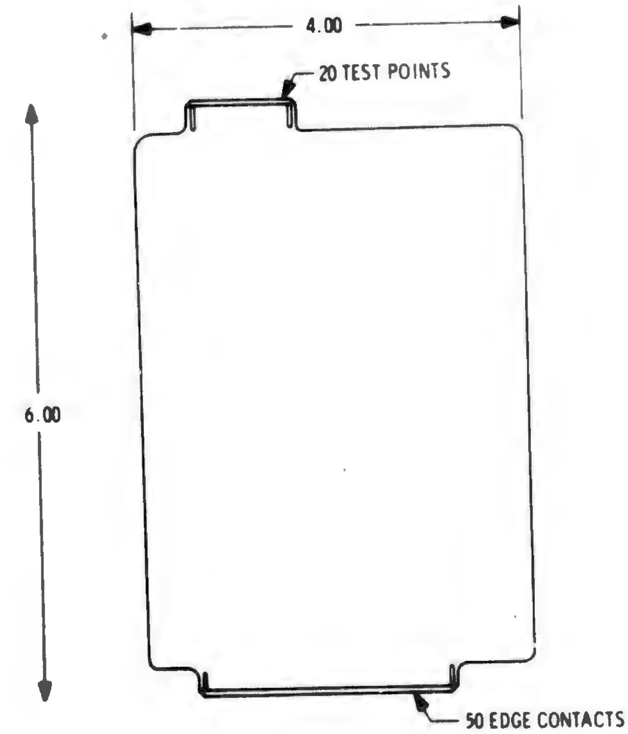


Figure 40. Circuit Card Outline

2.3.2 MICROWAVE RECEIVER PACKAGING

The microwave receiver is 15.38 inches wide by 4.00 inches high by 18.1 inches long (figure 41). Total weight, including electronics, is 16.25 pounds. Basic construction of the unit is sheet aluminum. The unit is basically a large plate that provides a convenient surface for layout of the microwave equipment and its interconnecting semirigid cable. Sides and cover are provided, as necessary for emi considerations, although some components are mounted to the vertical surfaces. Four long screws at the corners are provided for mounting the unit to a survace plate or to the auxilliary unit.

2.3.3 AUXILLIARY UNIT

The auxilliary unit is 15.38 inches wide by 10.00 inches high by 18.1 inches long (figure 42). Total weight, including electronics and power supplies is 88 pounds. Basic construction of the unit is sheet aluminum. The unit is divided into two sections, component and plenum. A top cover is not provided, since the microwave receiver, when installed, assumes that function and operation of the unit does not require a cover. A standard mounting arrangement is provided for mounting in an MS91405 type mounting tray.

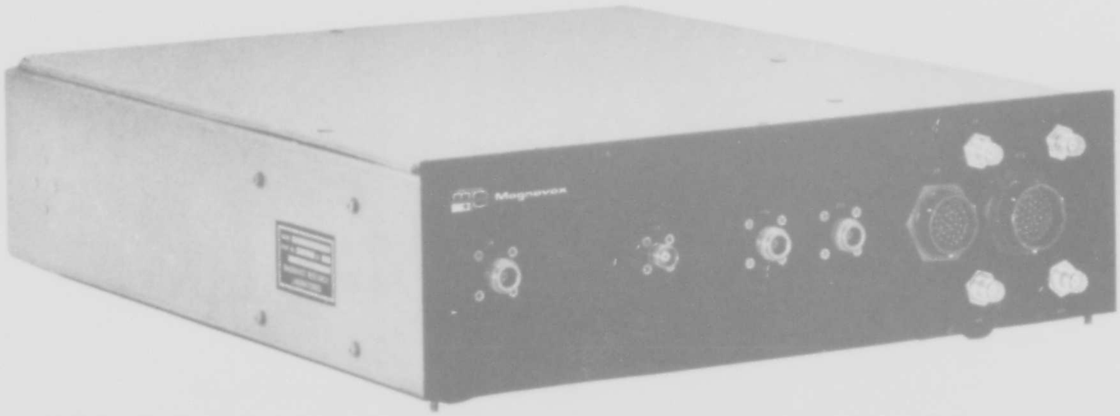


Figure 41. Microwave Receiver

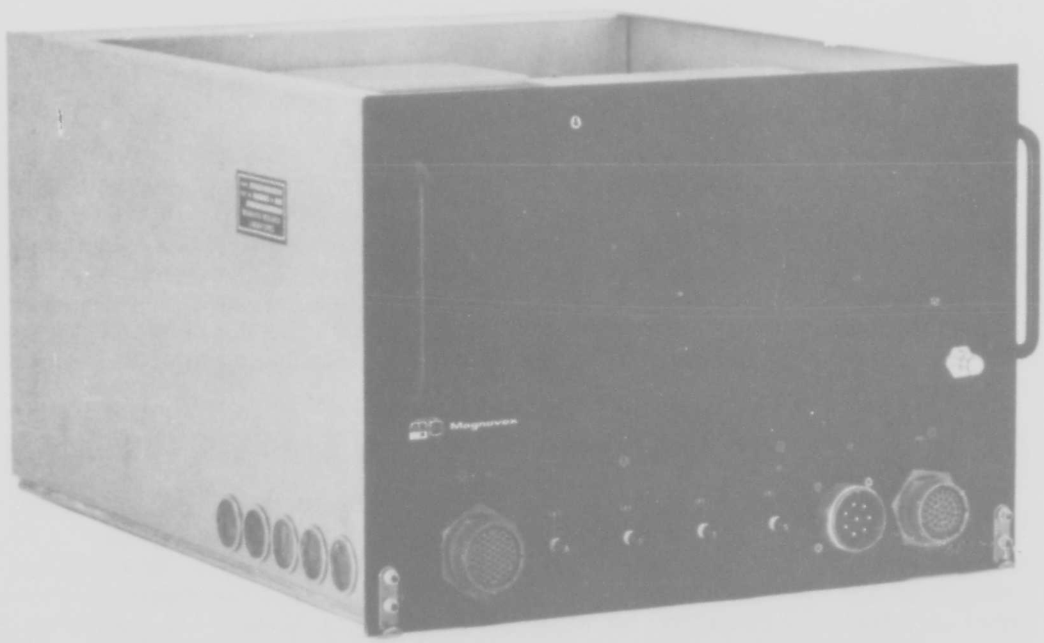


Figure 42. Auxilliary Unit

2.3.4 CONTROL DISPLAY UNIT

The control-display unit is 5.75 inches wide by 9.00 inches high by 6.00 inches long (figure 43). The unit is basically a control panel with a connector bracket and dust cover mounted to provide rear of the panel protection and weighs 4.25 pounds. Panel size and fastener arrangement is generally in accordance with MS25212. Indicators of acquisition and tracking for each channel augment the meters which indicate relative speed in knots. Calibrate, Lamp Test, and Power Switches are simple push-button switches. The automatic malfunction monitor lights upon receipt of a fault indication signal.

2.3.5 THERMAL CONSIDERATIONS

The cooling design is based on satisfying the requirements for installation in a transport aircraft of the KN-125 type. Since the quality of the cooling air (cabin air) is suitable for direct flow through the electronics, a simple fan/filter assembly attached to the rear of both the signal processor and auxilliary unit is all that is required. Cooling air therefore enters the enclosures at the rear and exhausts at the sides just behind the front panel. No air passes directly out the front of the boxes where it could cause discomfort to an operator.

As was noted previously, the honeycomb partitions allow free passage of air through the signal processor electronics. Power dissipation in the signal processor is less than 200 watts. Using a fan which is rated at 110 cfm at free delivery, airstream temperature rise does not exceed 5 degrees centigrade.

The auxilliary unit contains the power supplies which, in all but one case, are forced air cooled. Cooling air travelling through the plenum must pass through the power supply heat exchangers before reaching the exhaust ports. Temperature rise in the airstream is less than 10 degrees centigrade.

Both the microwave receiver and the control unit are low thermal dissipators and therefore do not require forced air cooling. Cooling of these units is by natural convection and conduction.

2.3.6 EMI CONSIDERATIONS

In the signal processor, a high degree of rf isolation is provided by the honeycomb partitions and the shields between the printed-circuit cards. In addition, local shielding is provided around critical circuit elements on the circuit cards themselves. To reduce the effects of conducted interference, filters are provided on input/output power and signal lines. To prevent radiated noise from entering or leaving the enclosure, the case is rf sealed using tight rivet connections at all joints and rf gaskets on the top and bottom covers.

A single point grounding philosophy is employed. A floating ground plane is provided at the bottom of the case to which all grounds are connected. Metallic card guides which are case grounded can provide additional grounding when in contact with the metallic edges of the circuit cards.

In the auxilliary unit the shielding requirements are less stringent. Since each of the power supply modules are provided with a sufficient degree of rf protection, no additional shielding or filtering is required.

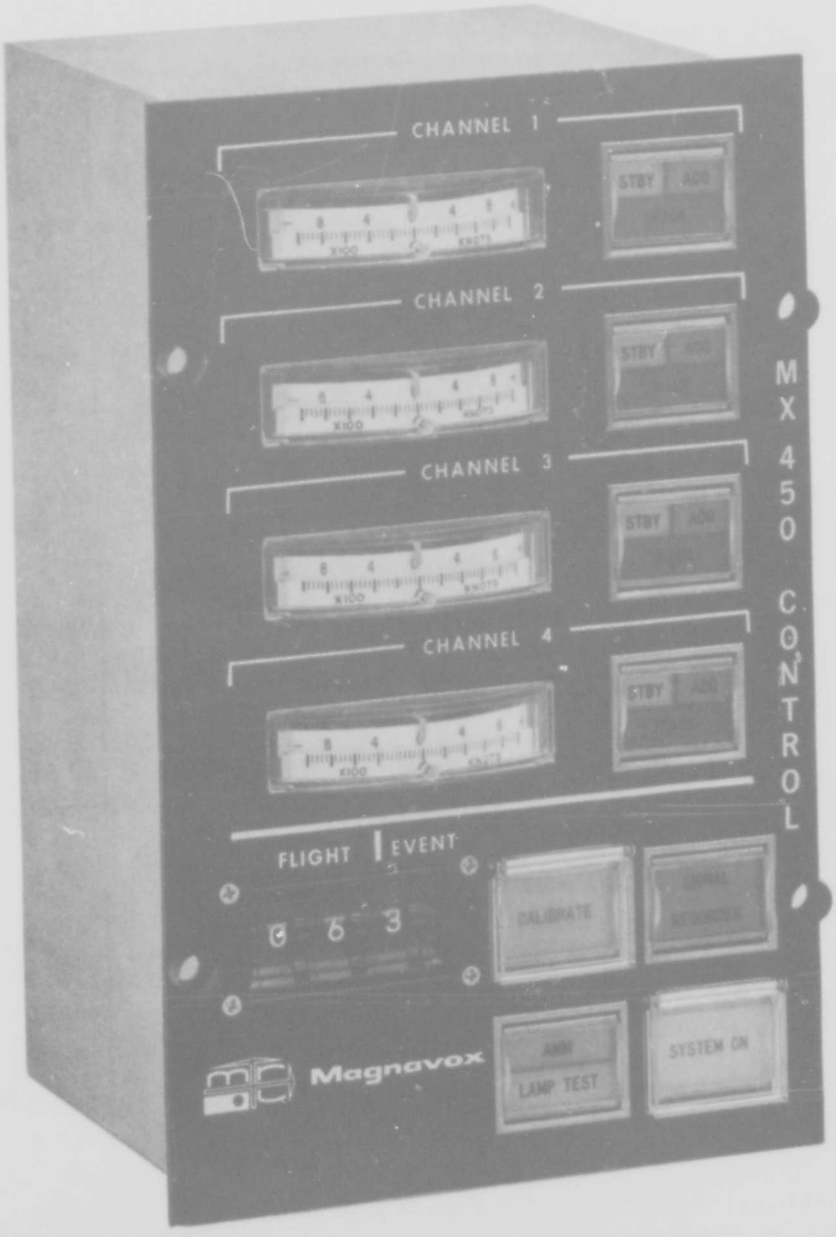


Figure 43. Control-Display Unit

The microwave receiver shell is fabricated from a single aluminum sheet. All corners are welded. The cover utilizes an oriented wire monel-silicone rubber gasket to seal the enclosure. The front panel is a separate piece, bolted on to prevent loss of rf integrity. All power and signal lines are filtered.

The control unit presents no discernable rfi problem.

2.3.7 MAINTAINABILITY

In the signal processor, virtually all circuitry is packaged on plug-in, printed-circuit cards. Removal of the top cover provides access to all cards in the rack. Test points are provided along the top edge of most cards to assist in fault isolation. All circuit cards plug into edge connectors located in the lower portion of the case. Faulty cards can, therefore, be simply extracted and replaced. Removal of the bottom cover permits access to the connector back plane wiring and the main wiring harness. Both covers utilize quick-turn fasteners to facilitate openings and closings. A test connector is located on the front panel to facilitate fault isolation. Since each power supply module in the auxilliary unit is a self contained unit, maintainability problems are minimized. The cover utilizes quick turn fasteners for ease of opening and closing.

Removal of the microwave receiver cover (which also utilizes quick turn fasteners) provides ready access to all elements of the electronics. Removal of the control unit dust cover provides access to all components.

2.3.8 VIBRATION

Design of this system was predicated on the system being operated in low-level input environments. Hence the trays of the signal processor and the auxilliary unit/microwave receiver are mounted on vibration isolators on the outside shell. In addition, the 5-MHz oscillator (located in the auxilliary unit), is provided with a (low frequency) second level of vibration isolation. This second level of vibration isolation, inside of the MX-450 mounts the oscillator into a special cavity suspended by damped springs. Figure 44 shows the cavity into which the oscillator is mounted. The figure does not show the oscillator but rather how the mount was tested using a simulated weight for the oscillator and a small accelerometer to measure loads. Hidden by the bottom bracket is a larger spring mounted on the underside of the oscillator which compensates for the downward weight. Outer dimensions of the mount are 6" x 3" x 3". The mount was designed for a 3.5 Hz, High Q resonance in each of the mutually perpendicular axes. The spring design was accomplished through use of a helical tension/compression spring computer program. The bottom spring is made of .041 diameter music wire, and its overall diameter is 1.088 inches. A three coil spring configuration was selected for ease of fabrication, low stacked height and high degree of directional stability. Maximum dynamic stress developed with the spring bottomed out was 75,000 PSI, which is well below the elastic limit of music wire. Static deflection was one inch with the 1 lb. oscillator, with 0.5 inches of deflection freedom still remaining, with the system capable of withstanding 0.6 G's of constant vertical acceleration.

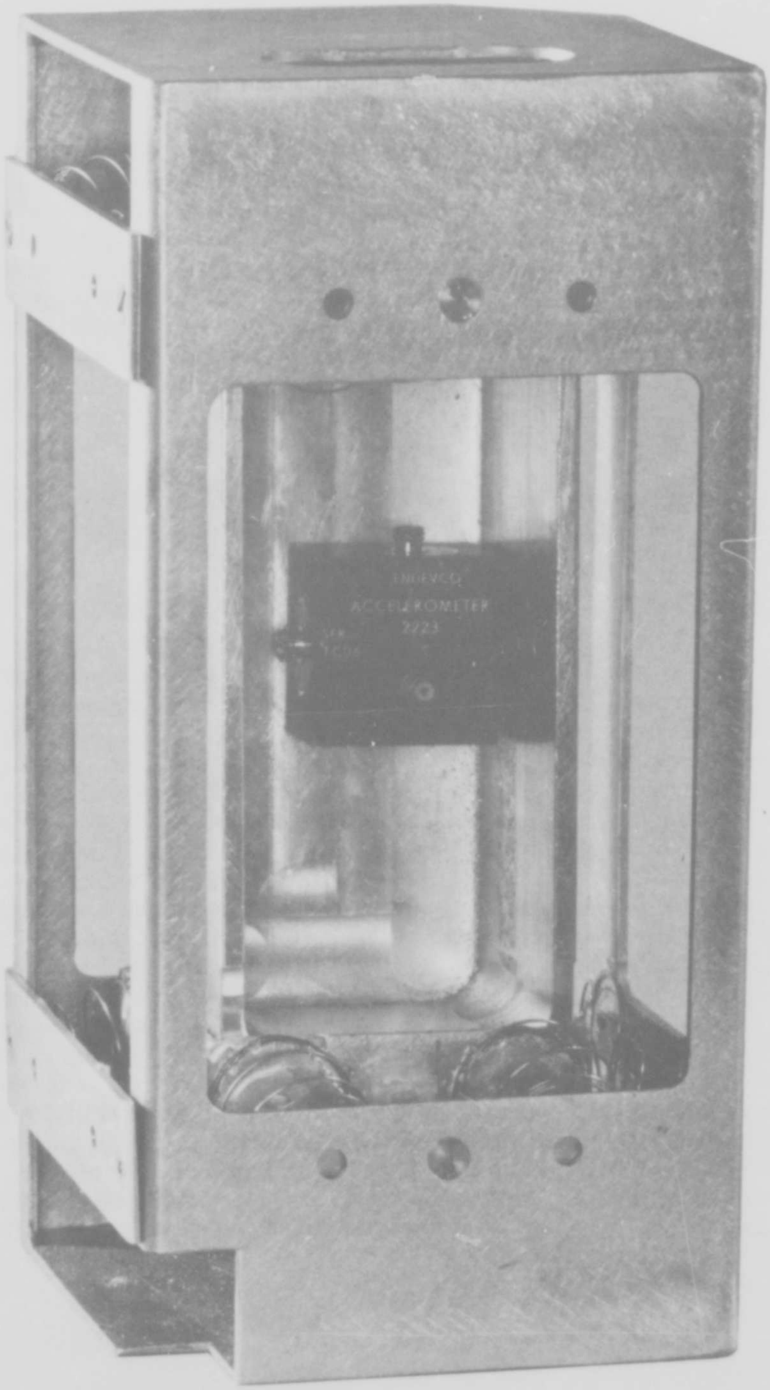


Figure 44. Oscillator Vibration Isolator

Side springs were made of 0.018 inch diameter music wire with an overall diameter of 0.705 inches. This three coil spring was also selected because of the low stacked height and high directional stability. The maximum dynamic stress developed with springs bottomed out was 75,000 PSI. 0.3 inches of deflection freedom remained for constant lateral acceleration of 0.4 G's of the input to the isolator. Test data on vibration can be found in section III.

2.3.9 RELIABILITY PREDICTION

A reliability prediction was performed on the MX-450 by the part-class, part-type technique described in MIL-HDBK-217A. This method provides guidelines for predicting reliability when the number of each part-class or part-type is available, but when part application stresses are not known. It is essentially a process of counting the number of parts of each class or type and multiplying this number by the generic failure rate for each part-class or type. The prediction was compiled under the following assumptions:

a. Airborne environment

b. Ambient temperature (35 degrees centigrade)

c. No redundancy or duty cycle considered

d. All circuit elements are in series

e. Failure rate for each part type assigned with assumed part stresses.

f. Failure rate sources are MIL-HDBK-217, RADC and vendor supplied data.

The mean-time between failure (mtbf) θ_t of a number of series elements is just

$$\theta_t = \lambda_1 + \lambda_2 + \lambda_3 + \ldots + \lambda_n$$

where λ_i is the failure rate per 10^6 hours. The following data was extracted from appendix G.

Unit	Failure Rate-f/10^6 Hours	MTBF (Hours)
Control Box Assembly	21.900	45662.1
Signal Processor	2051.229	487.5
Auxilliary Unit	638.970	1565.0
Total MX-450	2712.099	368.7

Thus, the predicted mtbf for the MX-450 is 369 hours.

2.4 POWER SUPPLIES

Four power supply modules are contained in the auxilliary unit. The modules are driven by the 400 Hz aircraft prime power supply. The output voltages are + 5, + 20, + and - 15 and - 5.2 volts. Specific features include short circuit protection through automatic current limiting which protects against momentary overloads and continuous shorts and overvoltage protection which protects the load in the event of a supply failure. Typical ripple is 0.2 percent + 10 mv over -20 degrees to +80 degrees centigrade. The specified mtbf is 35000 hours.

SECTION III

TESTING PROGRAM

3.1 TESTING PROGRAM RESULTS

During the course of this program, the MX-450 was subjected to extensive in-house testing in order that a high level of confidence would be obtained prior to field testing. This was borne out by the successful flight test program during which the MX-450 performed as advertised. This section of the report provides heretofore unpublished test data taken at Magnavox as well as performance data taken during the Readiness Test.

3.2 IN-HOUSE TESTING

Testing at Magnavox included a complete readiness test as well as various related tests which confirmed performance in new technology areas (e.g., digital discriminator). Other tests were performed to simulate the expected flight test environment. Finally a compatibility test was made between the MX-450 and a Hazeltine transmitter. The major in-house tests results are presented herein; many are appearing in print for the first time.

In preparation for the flight test environment, several tests were performed which simulated the temperature changes and vibrations to be encountered. The equipment was cycled up to 60 degrees centigrade and its performance verified. Significant vibration tests were run to determine the incidental frequency modulation induced in the oscillators. Table III shows the incidental fm induced on the 1440 MHz local oscillator. The oscillator was subjected to a 2g acceleration by rotating it 180 degrees on each axis. The corresponding frequency deviation in the output was measured.

Table III. 1.4 GHz Local Oscillator Vibration Test (Model No. SLN6039SP, Serial No. 108030)

Rotation	Induced Frequency Deviation $X10^{-9}/g$
X-axis	2.85
Y-axis	0.60
z-axis	0.52

Significant vibration tests were performed on the 5-MHz reference oscillator. Figure 45 shows the test set up for those tests. The oscillator under test was subjected to a double amplitude (d.a.) of 0.4 inches p-p. In three configurations; hard mounted, in the cage in the modem chassis and in the auxilliary unit. Figures 46 and 47 show the relative amplitude variations as the shake frequency was varied from 5 to 1000 Hz.

Various performance checks were made prior to the Readiness tests. Figure 48 shows a curve of the performance of the digital discriminator in channel 4. Differences in the I and Q voltages at the input to the discriminator produce pulses proportional to the difference in received carrier and local oscillator frequencies. The zero crossings represented by the pulses are accumulated in an up-down counter. The contents of the counter is an estimate of the frequency offset and is used to control the local-oscillator frequency.

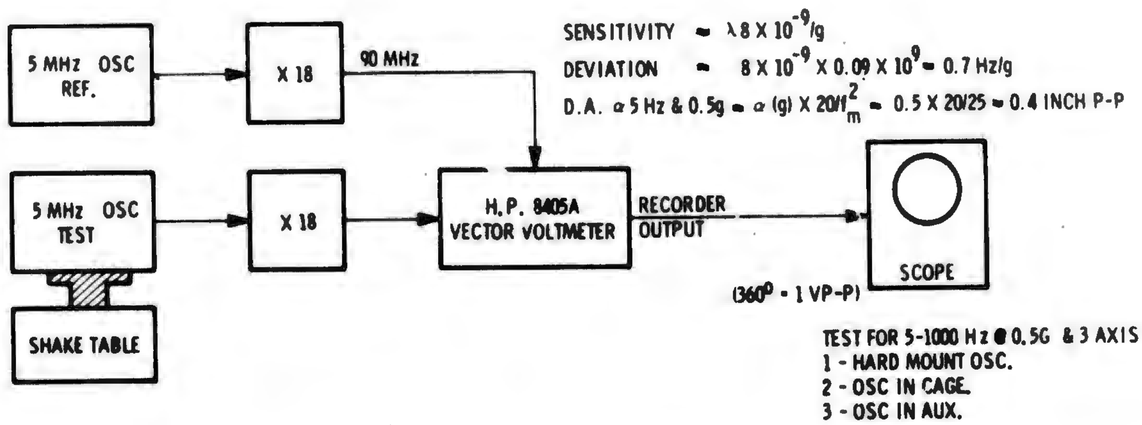


Figure 45. Reference Oscillator Vibration Tests

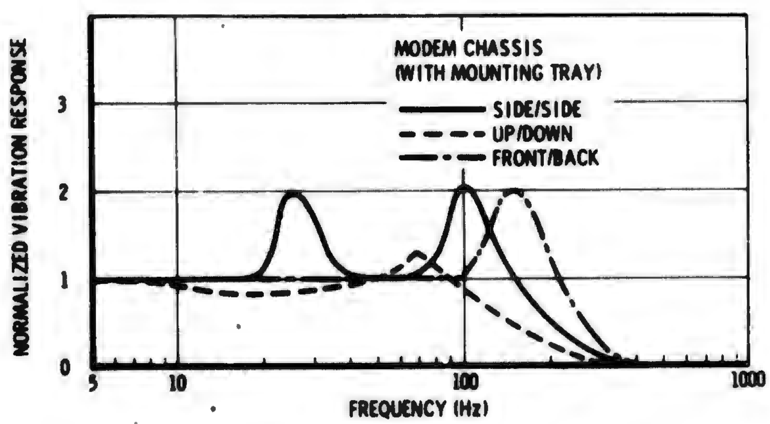


Figure 46. Reference Oscillator Vibration Response (Modem Mounted)

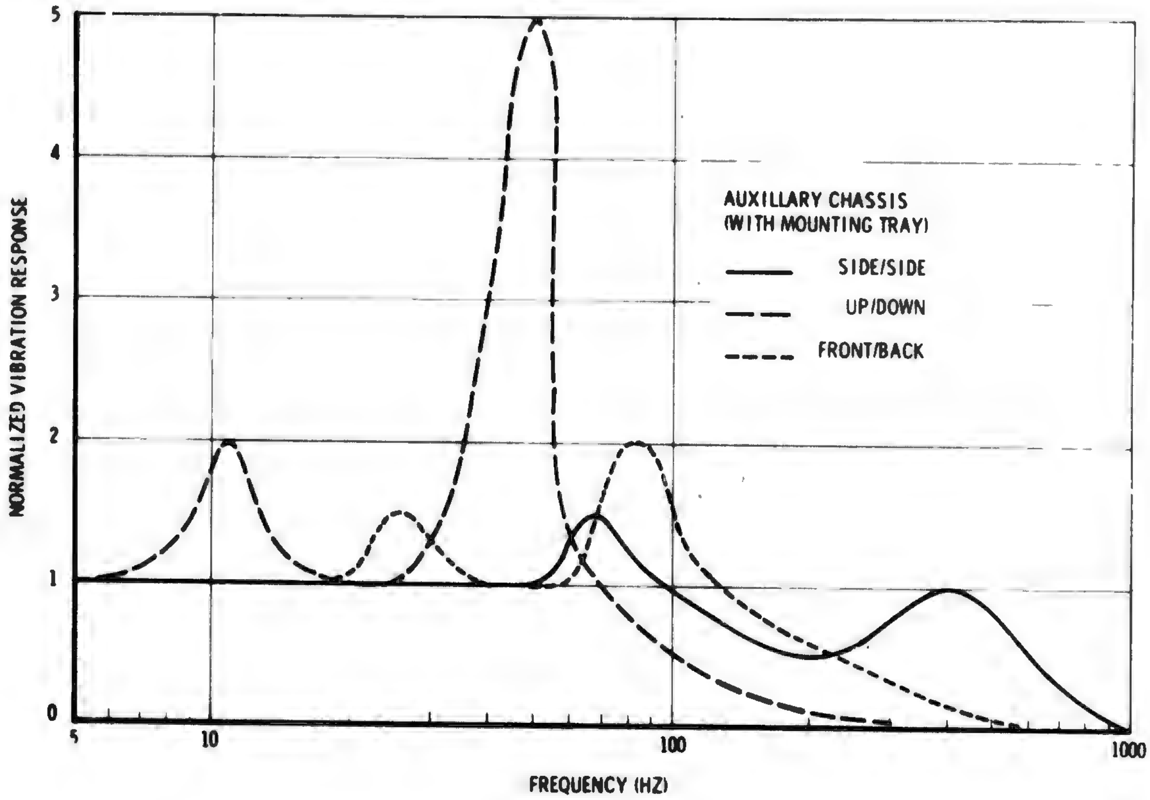


Figure 47. Reference Oscillator Vibration Response (Auxilliary Units Mounted)

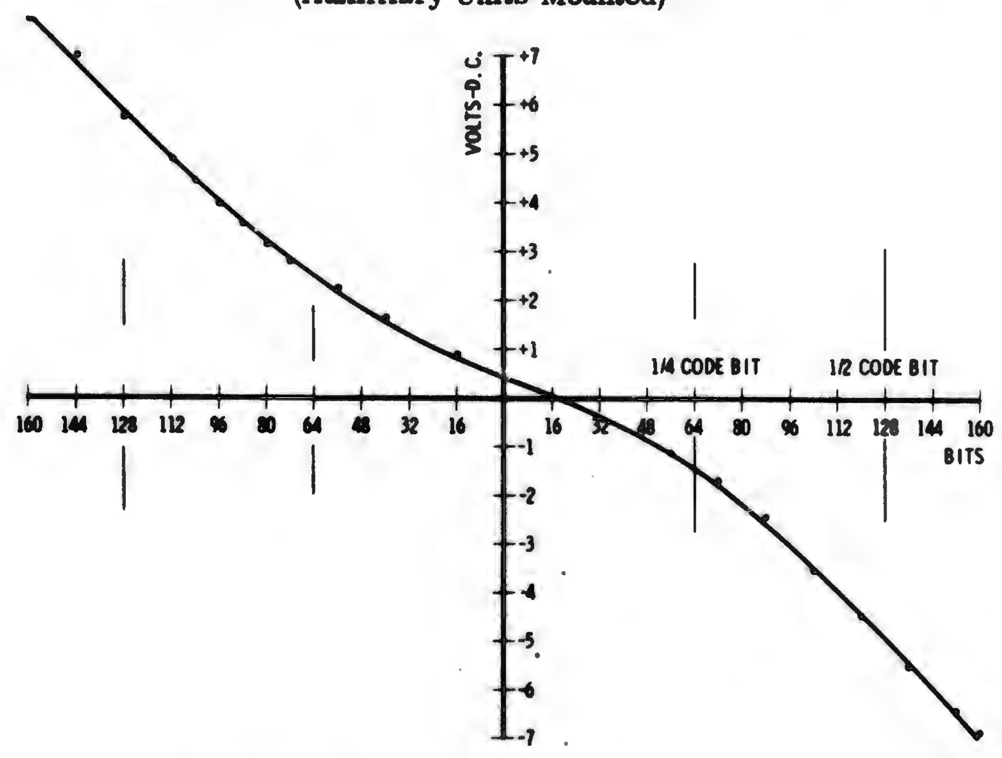


Figure 48. Channel 4 Digital Discriminator

The agc calibration curves were taken which enable a calculation of the input signal level to the MX-450 using the binary agc signals available on the receiver. Figures 49 through 54 show the calibrations of noncoherent, maximum and the various channel agc, all normalized to -123 dBm. To ascertain the input signal level from the agc counts, the corresponding attenuation for noncoherent, maximum and channel agc are added to -123 dBm. For example, if the following were typical airborne recorder data as shown in table IV, the corresponding input signal levels would be -123 dBm + (1/2 + 1-1/2) dB + (channel).

A test was run to compare the performance of the digital tracking loop with theory. Figure 55 shows two data points and the theoretical performance of loops with 1.5π and 3π noise bandwidths. The MX-450 loop has a $B = 2\pi$ so it was expected that the data points fall between the two theoretical curves. Actual implementation was about 1 dB from theory.

Performance under jamming was calculated using a similar computer program as given in the Readiness test results (appendix D). Figures 56 and 57 are curves of the standard deviation of pseudorange and pseudodoppler. For varying jammer to signal (J/s) ratios.

Finally in preparation for the readiness tests, a preliminary performance demonstration test was made on 25 October 1971 for SAMSO personnel.

Table IV. Signal Level Calculation

AGC	Binary Count	Attenuation (dB) from Curves	Input Signal Level (dBm)
Non-coherent	2	+ 1/2	
Maximum	6-1/2	+ 1-1/2	
Channel 1	3	+ 9	-110
Channel 2	18	- 4-1/2	-125 1/2
Channel 3	9	+ 2	-119
Channel 4	3	+ 10	-111

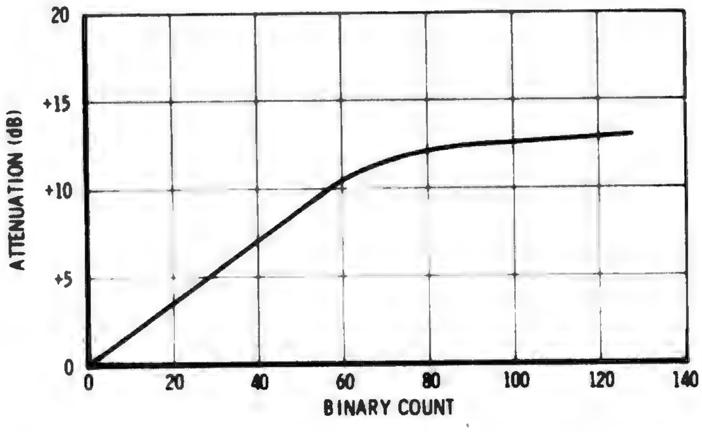


Figure 49. Noncoherent AGC (Normalized for Signal at -123 dBm)

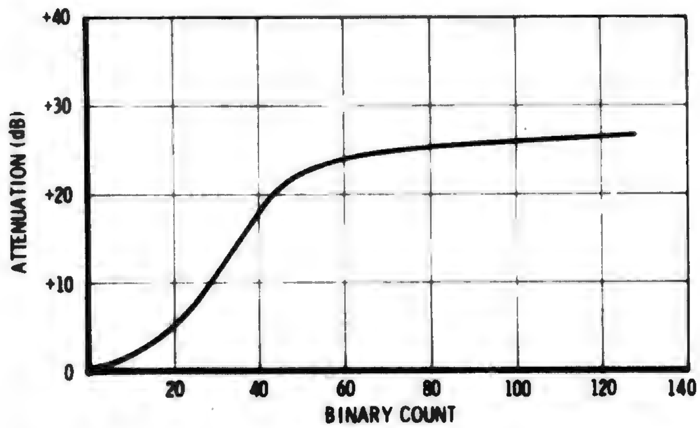


Figure 50. Maximum AGC (Normalized for Signal at -123 dBm)

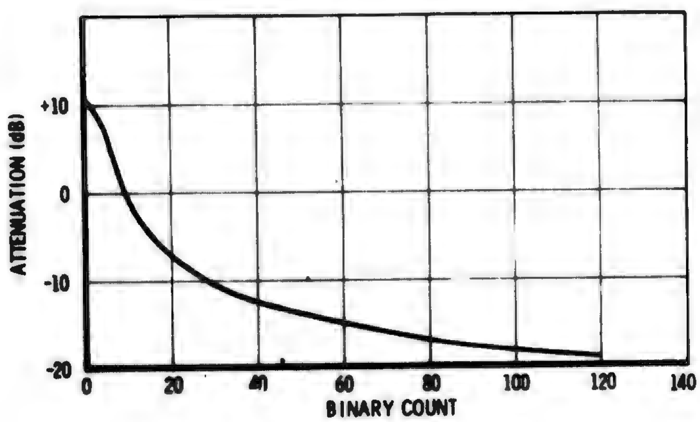


Figure 51. Channel 1 AGC (Normalized for Signal at -123 dBm)

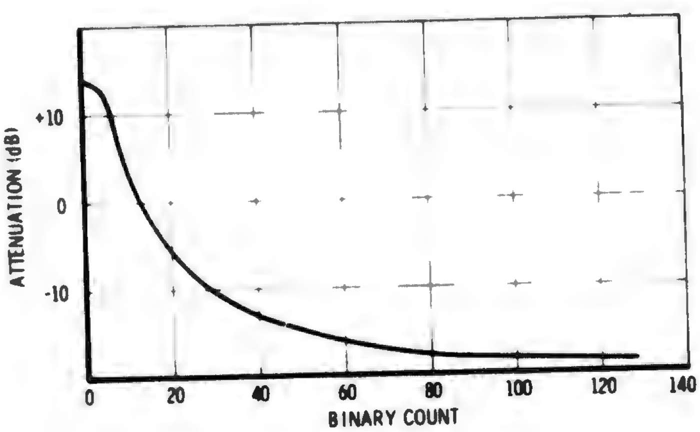


Figure 52. Channel 2 AGC (Normalized for Signal at -123 dBm)

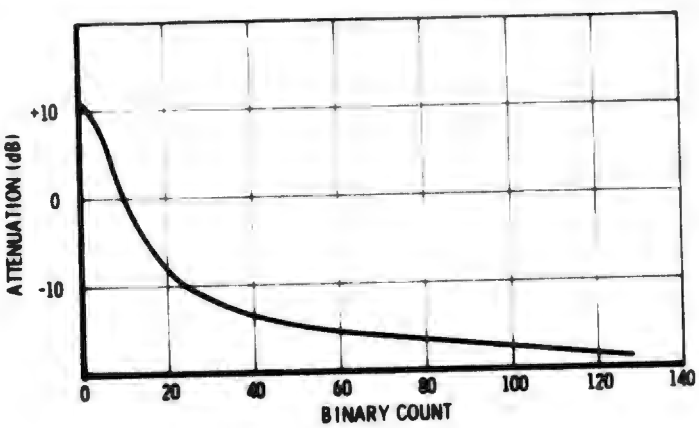


Figure 53. Channel 3 AGC (Normalized for Signal at -123 dBm)

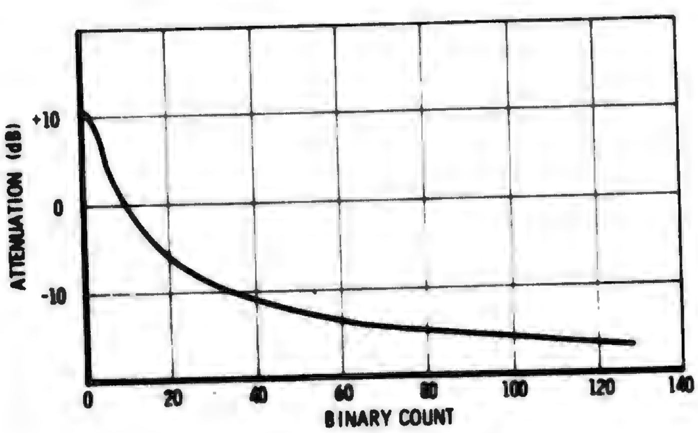


Figure 54. Channel 4 AGC (Normalized for Signal at -123 dBm)

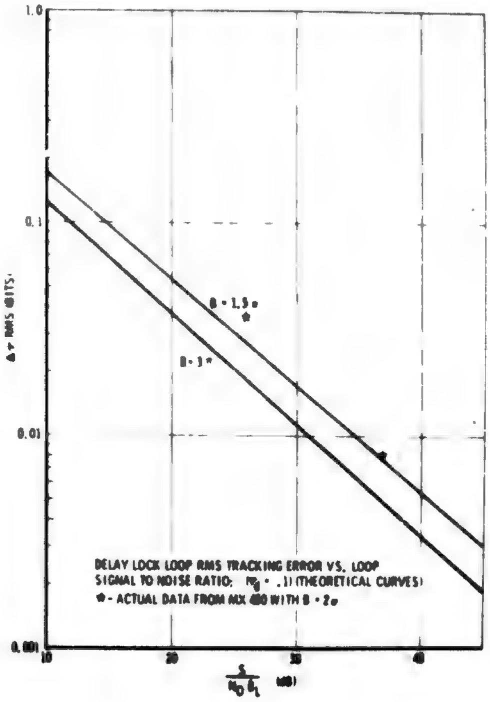


Figure 55. Delay Lock Loop RMS Tracking Error vs Loop Signal-to-Noise Ratio; ($\tau_d = 0.1$) (τ Receiver Channels) X = Actual Data from MX450 with B = 2π

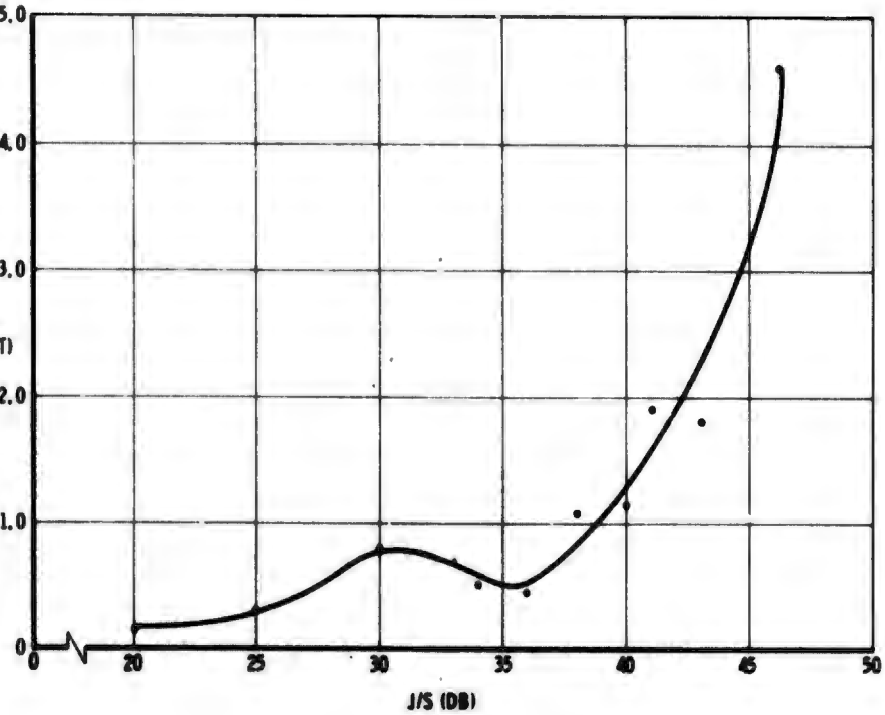


Figure 56. Pseudorange (Standard Deviation) Under Jamming (Signal at -123 dBm, Channel 2)

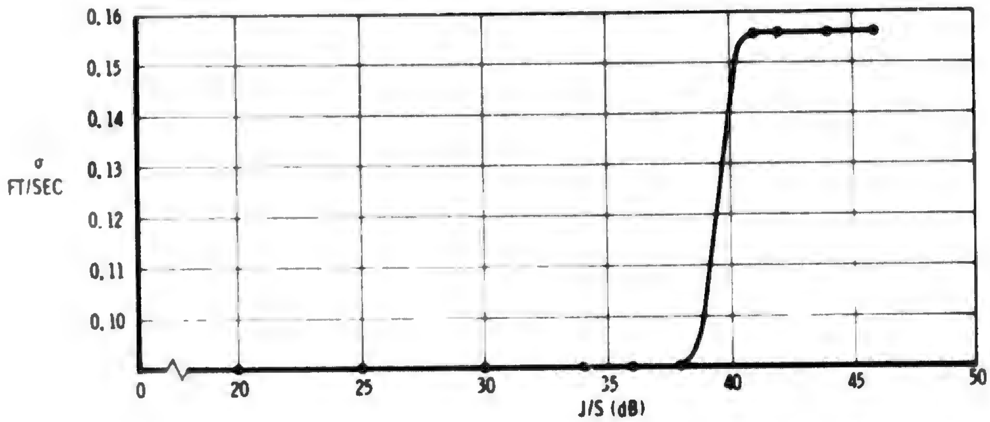


Figure 57. Pseudodoppler (Standard Deviation) Under Jamming (Signal at -123 dBm, Channel 2)

The demonstration consisted of the following tests:

a. Calibrate Mode: The Magnavox receiver has a self-calibrating mode which automatically neutralizes the differential static delay between channels. In this mode an internally generated calibrate signal is injected through a directional coupler into the receiver front end which all four channels track and cause the static delays through the receiver to be accumulated in the range registers. At the end of the calibrate mode (16 seconds) these registers are reset to zero so that differential delays between channels is effectively zero.

   Since Magnavox did not have a 621-B transmitter available, a portion of channel 4 in the signal processor was utilized to derive the appropriate 621-B transmit signal which is routed back to the front end in a manner similar to the calibrate signal for injection at 1575 MHz. The remaining three channels in the receiver then tracked this simulated transmit signal.

b. Initial Acquisition: The receiver repeatedly passed the initial acquisition test with the power boost synch signal at the -100 dBm level and the long code PN signal at -123 dBm.

c. Reacquisition: With the received signal level was set at -123 dBm in accordance with the specification, the receiver was deliberately forced to drop lock to determine its ability to reacquire. Each time the receiver reacquired easily. This test was successful for received signal levels as low as -126 dBm. At a signal level of -127 dBm not all channels could reacquire in a reasonable time.

   At a later point in the demonstration essentially the same performance as noted above was observed with simulated signal dynamics corresponding to 1000 knots of velocity.

d. Tracking - Hold on and Dynamics: In this test the signal level was set at -123 dBm for reacquisition. With all channels tracking the received signal level was decreased to -140 dBm to determine if the receiver hold on satisfied the specification. It was necessary to decrease the received signal level to -149 dBm before one or more channels broke lock.

At a later point in the demonstration essentially this same performance as noted above was observed for simulated signal dynamics corresponding to 1000 knots of velocity.

e. Tracking Acceleration Rates (Jerk): With the receiver tracking at a signal level of -140 dBm an acceleration rate (Jerk) of 320 ft/sec^3 was applied for approximately one-half second until the acceleration increased to 175 ft/sec^2. The acceleration was held constant at 175 ft/sec^2 until a velocity of 7000 ft/sec was reached. At this point a negative jerk was applied to reverse the signal dynamics. The dynamics simulation was automatically programmed from the System Test Set to cycle the dynamics as seen by the receiver between the limits of R = 320 ft/sec^3, R = 175 ft/sec^2 and R = 7000 ft/sec as specified for a signal level of -140 dBm. This test was repeated successfully for signal levels down to -145 dBm with all channels maintaining lock. At a signal level of -146 dBm not all channels could maintain lock.

f. Data: Correct pseudorange and doppler data readouts were observed with signal dynamics corresponding to 1000 knots and simulated range of 123 feet.

During November 10, 11, and 12, readiness tests were performed in accordance with the Readiness Test Procedures (MRL Document R-4168) shown as appendix C. The complete results for these tests are given in appendix D. The MX-450 met or exceeded all contractual specifications. Table V summarizes the readiness test results.

The MX-450 was checked out with a Hazeltine Transmitter at Magnavox to ensure compatibility during the flight test. Appendix E describes those compatibility tests which were performed on 27 October 1971.

Table V. Summary of MX-450 Readiness Tests, Parts 6.5.2 and 6.5.3

CHANNEL	PSEUDORANGE				PSEUDODOPPLER			
	V = 7000 fps	Samples	A = 175 fps^2	Samples	V 7000 fps	Samples	A 175 fps^2	Samples
1	2.28 ft.	10	3.87 ft.	5	0.156 fps	10	0.258 fps	6
2	1.93 ft.	10	0.625 ft.	5	0.172 fps	10	0.227 fps	5
3	2.94 ft.	10	4.48 ft.	16	0.436 fps	16	0.302 fps	8
4	3.20 ft.	10	2.33 ft.	10	0.253 fps	10	0.154 fps	7

3.3 RECOMMENDATIONS FOR MX-450 IMPROVEMENTS

The MX-450 utilized new technology in that it implemented its carrier and code loops digitally. A further advance in technology would occur if those digital loops were implemented by software within the airborne computer as opposed to by hardware within the MX-450. While this is not a direct improvement to the 450 it takes note of the fact that any 621B user equipment would contain a PN receiver as well as a processor for the navigation solution. The use of that processor to do digital PN receiver functions depends of course on the size and capability of the processor.

Obvious improvements to the MX-450 involve repackaging and productization for a mission oriented operational airborne environment as opposed to the relatively benign experimental environment of the Holloman tests.

APPENDIXES

APPENDIX A

POWER BOOST DETECTOR

The 621B experiment uses a power-boosted short code for initial synchronization. A simple method was implemented for detection of this power boost.

The quantitative problem statemnent is as follows: In a backgroundof white gaussian noise (N_o = -169.5 dBm), a 25 microsecond long burst of 10 Mpps pseudonoise (binary PSK) at -101 dBm appears; the problem is to detect the pulse. Other pseudonoise signals at -123 dBm or less may be present throughout.

The implemented technique is simply a square law detector, ac coupled to a threshold device. Davenport and Root (chapter 12) shows that in the absence of signal, the detector output spectrum near dc is

$$S_{nxn}(f) = N_o^2 B^2 \delta(f) + N_o^2 (B - |f|)$$

where B is the intermediate-frequency bandwidth, and with signal present

$$S(f) = N_o^2 B^2 \delta(f) + N_o^2 (B - |f|) + 2C N_o B \delta(f) + 2CN_o + C^2 \delta(f)$$

$$= (C + N_o B)^2 \delta(f) + 2 CN_o + N_o^2 (B - |f|)$$

where C is the carrier power. The ac coupling removes the $N_o^2 B^2 \delta(f)$ term in both places. If we place a low pass filter of noise bandwidth W^o (W<<B) prior to the threshold device, then the situation becomes

Noise Power to Threshold C/kT, no signal = $2 W N_o^2 B$

Noise Power to Threshold C/kT, with signal = $2 W N_o^2 B + 4 C N_o W$

Net increase in dc due to signal = C^2

Without any particular attempt to optimize the values, let B = 20 MHz, W = 30 kHz. Then relative to the no-signal noise power, the with-signal noise power is

$$\frac{N_{ws}}{N_{ns}} = \frac{2\,W\,N_o^2\,B + C\,N_o\,W}{2\,W\,N_o^2\,B} = \frac{N_o\,B + 2\,C}{N_o\,B} = 2.3\text{ dB}$$

and the 'dc rise' is

$$\frac{C^2}{N_{ns}} = \frac{C^2}{2\,W\,N_o^2\,B} = 16\text{ dB}$$

For a false alarm rate of about 2 per second, the detection probability is 96 percent. For a 3 dB drop in carrier power, the detection probability falls to 27 percent.

It is concluded that this power detection scheme is just adequate. Some optimization of bandwidths and threshold seems in order, but this is probably best done experimentally.

In the mechanization, when a "hit" occurs all search-mode channel coders are immediately started and a sliding search (in the usual slow-the-coder direction) over 100 to 200 chips is initiated. If there is a miss, stop the search and return to standby.

---

1. Davenport, W. B. and Root, W. L., Random Signals and Noise, McGraw Hill Book Co., N.Y. 1958.

APPENDIX B

PERFORMANCE OF DIGITAL FREQUENCY DISCRIMINATORS AND A DIGITAL AFC

In order to reduce phase-lock-loop acquisition time when there are relatively large frequency offsets, it is desirable to have an estimator of carrier frequency independent of the phase-lock carrier loop. A frequency discriminator is such an estimator. Digital frequency discriminators are of interest due to ease of mechanization and avoidance of mechanization problems such as drift. The performance of three digital frequency discriminators and an afc loop employing one of the discriminators is discussed in this appendix. The performance was determined by digital computer simulation of the devices. A discussion of the performance of frequency discriminators as determined analytically is also presented.

The first digital frequency discriminator (dfd) of interest is shown in figure 58. The signal plus noise is separated into its inphase and quadrature components after filtering by the bandpass filter centered at the nominal carrier frequency.

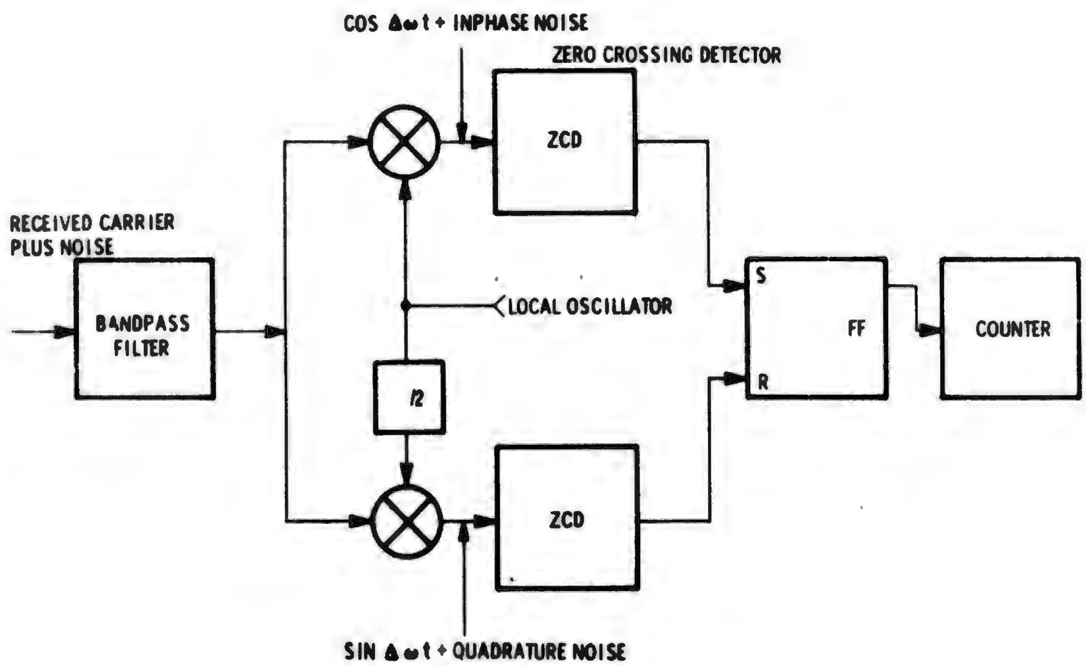


Figure 58. Digital Frequency Discriminator I Block Diagram

The bandpass filter used in the simulation was a two pole Butterworth filter. The two sided bandwidth was set equal to the total frequency uncertainty expected for a particular application, namely 6 kHz. The zero crossings of the two components are detected by zero crossing detectors (zcd) whose outputs set and reset a flip-flop. The number of resets per time of the flip-flop indicates frequency and the average value of the output indicates the polarity of the frequency offset. The effect of polarity reversal of the offset frequency is illustrated by the dfd waveforms shown in figure 59.

Examination of the waveforms associated with the dfd (for no noise) shows that the dfd can be looked at as a coincidence detection type of device. This stems from the fact that a count occurs only when an inphase zero crossing is followed by a quadrature crossing (the order is reversed when the offset frequency polarity is reversed). This tends to cancel false alarms or zero crossings due to noise. Reference to the "rotating vector" representation of the signal in figure 60a shows that an inphase positive going zero crossing means the signal vector has moved from either the second quadrant into the first or from the third into the fourth, i.e., from the

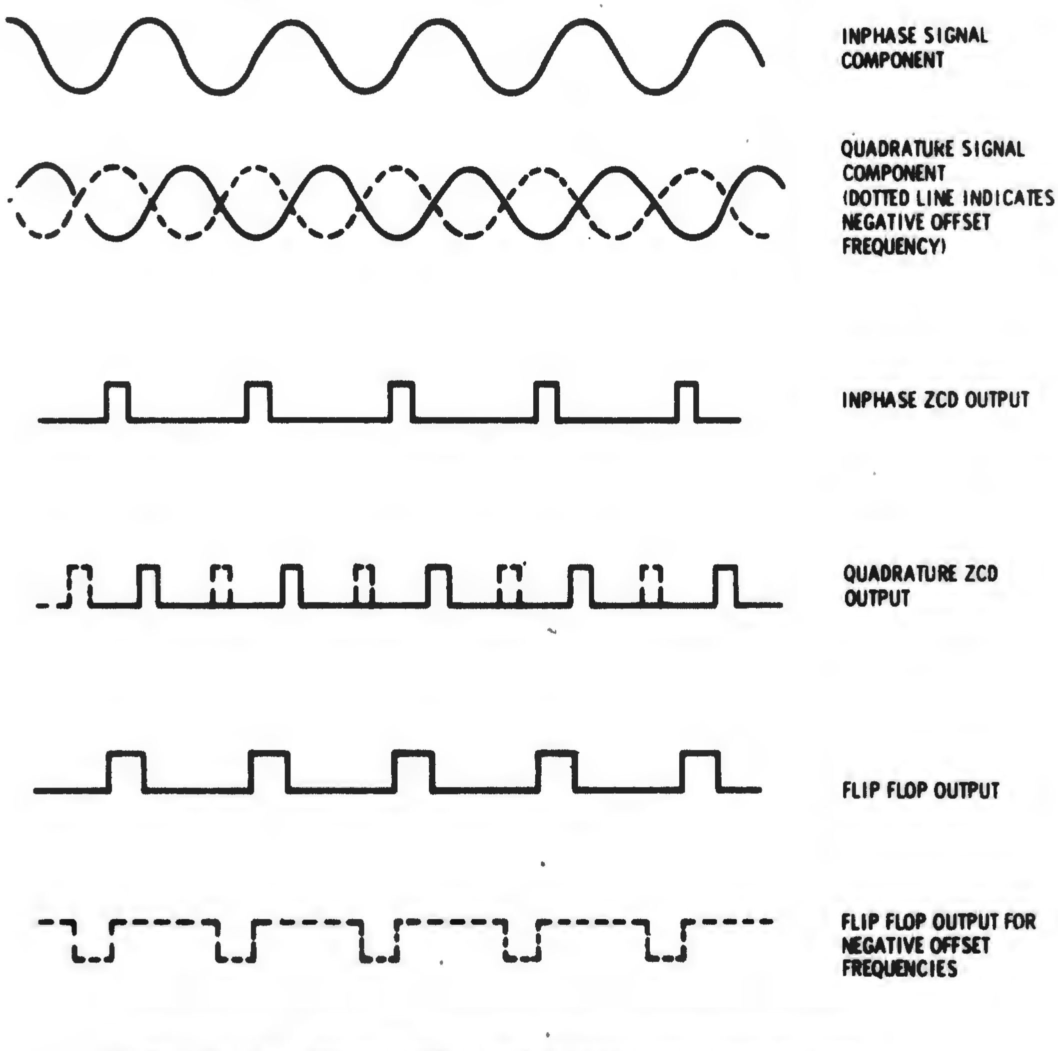


Figure 59. Waveforms (No Noise) Associated with Digital Frequency Discriminator I.

left half plane into the right. This followed by a positive going quadrant zero crossing is declared a frequency count. Note that between the inphase zero crossing and the quadrature zero crossing, the noise may cause the vector to move back into the left half plane, as shown in figure 60b. This event, followed by the quadrature zero crossing is still declared a frequency count.

The results of simulating this dfd are presented in table VI. The large bias error in the mean frequency at the low frequency offset (100 Hz) is the most significant single result. This bias at low offsets is explained by the fact that at low frequencies, the "window" or time between a set and reset of the flip-flop due to signal alone is longer and thus the probability of a reset due to noise is higher. The results in table VI were not plotted since the number of simulation trials was not high enough to insure adequate statistical averaging. However, the observable trends are valid.

The next dfd simulated was similar to the last except for the strategy for declaring a set and reset. The strategy used is best explained by referring to the rotating signal vector diagram in figure 61a. A cycle or frequency count is declared when the signal vector moves from Quadrant II to Quadrant IV. Reference to table VIII shows that this dfd has considerably improved performance over the first dfd discussed. This may be explained by the fact that in the first dfd, after a positive inphase zero crossing it is only necessary to move from the upper half plane to the lower half plane whereas in the second dfd it is necessary to move from one quadrant to the diagonally opposed quadrant. The biggest drawback with this second dfd is that due to the symmetry of the detection criteria, the polarity of the frequency offset is lost.

The third, and most successful dfd was implemented by using the detection strategy shown in figure 61b. In this case it is necessary for the signal vector (actually signal plus noise) to move from the left half plane to either the first or fourth quadrant. Once in either of these quadrants (positive going inphase zero crossing) a positive going quadrature zero crossing indicates a plus count and a negative going quadrature zero crossing indicates a minus count. Reference to table I shows that this dfd has superior performance to either of the two formerly considered.

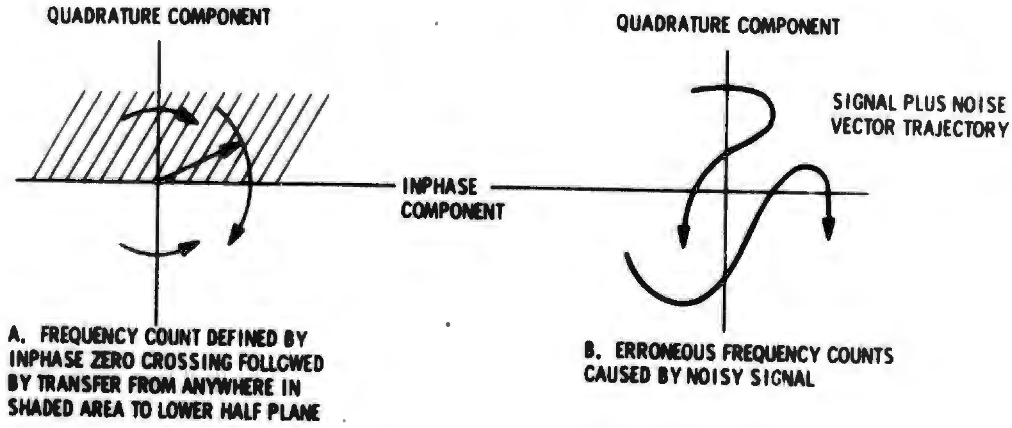
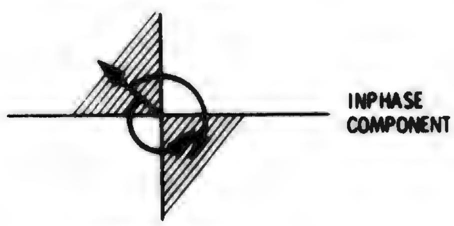


Figure 60. Vector Representation of Discriminator I Counting Process

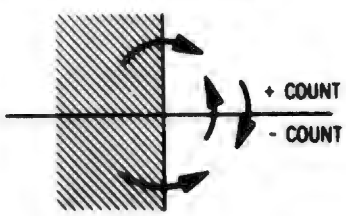
Table VI. Performance of the Three Digital Frequency Discriminators Obtained from Digital Computer Simulations

Counting Interval = 0.1 Sec

Type of Discriminator	Offset (Hz)	S/N (db)	Mean (Hz)	RMS (Hz)
I	100	40	100	0
	100	20	116	10
	100	6	274	29
	100	4	445	45
	100	2	705	64
	1000	6	1005	12
	1000	4	1044	39
	1000	2	1126	38
II	100	6	144	19
	100	4	254	40
	100	2	453	65
	1000	6	996.	5
	1000	4	1008	19
	1000	2	1038	16
III	100	6	85	15
	100	4	85	31
	100	2	40	37
	- 100	4	- 76	28
	1000	6	939	34
	1000	4	804	85
	1000	2	700	46
	-1000	4	- 845	28



A. DISCRIMINATOR II
FREQUENCY COUNT DEFINED BY TRANSFER FROM DIAGONALLY OPPOSED QUADRANTS



B. DISCRIMINATOR III
FREQUENCY COUNT DEFINED BY TRANSFER FROM LEFT HALF PLANE FOLLOWED BY EITHER POSITIVE OR NEGATIVE GOING QUADRATURE ZERO CROSSING

Figure 61. Vector Representation of Discriminator II and III Counting Process

This is most obvious at low frequencies, where the large bias error is not present as it is in the two other dfd's. This is due to the fact that this dfd allows for both positive and negative counts and positive going zero crossings due to noise are as equally probable as negative going zero crossings due to noise. Thus, noise caused counts tend to average out to zero. Furthermore, since this dfd counts in both directions, the polarity of the frequency offset is automatically accounted for. Finally, it can be seen from table VII that as the signal to noise ratio goes down, the output frequency goes down. Thus, this dfd suppresses the indicated frequency for low signal to noise ratios just as conventional analog frequency discriminators do. The compression and normalized error obtained from the simulation of this discriminator is compared in table VII with the analytical results. In considering the "coarseness" of the simulation data due to low number of simulation trials, the agreement is fairly good.

Table VII. Comparison of Digital Frequency Discriminator Simulation Results with Theoretical Results

	Theoretical Results		Simulation Results	
$S/2N_0B$ (db)	7	3	6	4
Compression	0.993	0.864	0.939	0.804
Normalized Error BT = 300	2.3×10^{-3}	1.1×10^{-2}	1.7×10^{-3}	4.2×10^{-3}

A digital afc loop was simulated by using the dfd III. The afc loop block diagram is shown in figure 62. The loop filter, 1/S, was mechanized digitally by simply adding the new dfd output to the old output on each successive sample. The vco gain was made variable to speed up frequency acquisition. The gain for the first 3 milliseconds of acquisition was set at 390 and thereafter the gain was set at 26. With the large value of vco gain, the loop nulls out the majority of the frequency offset with the first digital correction. The smaller remaining offset is then nulled out in small steps (lower value of vco gain) so that the final vco frequency quantization error is small enough for a phase lock loop to rapidly acquire. In addition to the gain change, the bandwidth of the bandpass filter was changed from 6 kHz (2 sided) to 1.5 kHz (2 sided) after 3 milliseconds had elapsed. This was done to increase the S/N in the loop once the loop started pulling in so as to reduce the frequency jitter. A plot of the loop pull in performance is shown in figure 63.

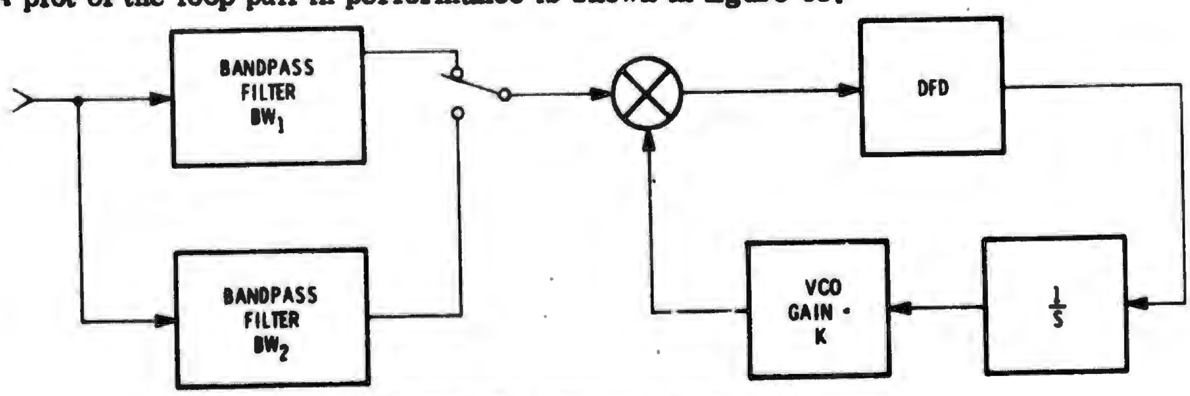


Figure 62. Digital AFC Loop

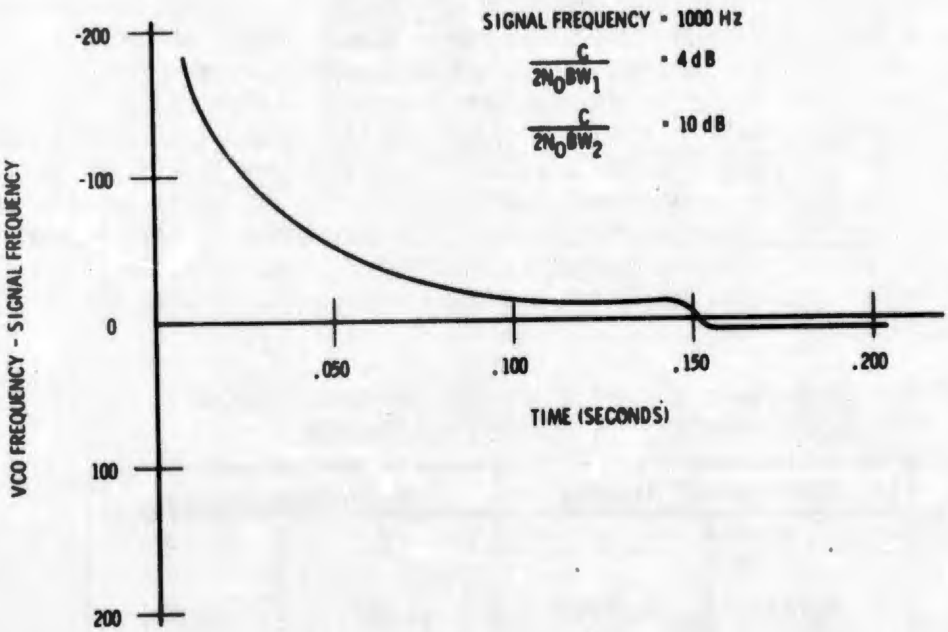


Figure 63. AFC Loop Pull in Performance

APPENDIX C

READINESS TEST PROCEDURE

READINESS TEST PROCEDURE

User Equipment Definition and Experiment Program

Task VI - Phase II Alternate Receiver

Contract No. F04701-71-C-0318

Prepared for:

Department of the Air Force
Headquarters, Space and Missile Systems Organization (AFSC)
Air Force Unit Post Office
Los Angeles, California 90045

Prepared by:

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2829 Maricopa Street
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1 November 1971

MRL Report No. R-4168

Prepared by: R. S. Cnossen, Project Engineer

Approved by: F. J. Charles, Program Manager

ACCEPTANCE TEST PROCEDURE

Magnavox
RESEARCH LABORATORIES

TORRANCE, CALIFORNIA

DWG. NO.	ES 877381
PAGE i OF PAGES	
BY:	

SUBJECT:

Assembly Drawing No. 709878

Acceptance Test Data Sheet No.

Schematic Drawing No.

Wiring Diagram No.

Master B/M No.

MX-450 Readiness Test Procedure

CHANGE NO.	NATURE OF CHANGE	DATE	BY	APPROVED	REV.

	NAME	DATE		NAME	DATE
TYPED			APPROVED		
CHECKED			APPROVED		
APPROVED			APPROVED		

MRL 66716-1

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ACCEPTANCE TEST PROCEDURE

Magnavox
RESEARCH LABORATORIES

TORRANCE, CALIFORNIA

DWG. NO. ES 877382

PAGE 1 OF PAGES

BY:

SUBJECT:

Readiness Test Procedure

1.0 SCOPE

The purpose of this document is to describe the test procedures to be followed during the readiness testing of the user receiver developed by the Magnavox Research Laboratories for the User Equipment Definition and Experiments Program Task VI - Phase II field tests. As required under this contract, the Magnavox Research Laboratories will perform tests on the receiver at Torrance, California, to ensure that the requirements contained in Appendix A are satisfied. SAMSO approval of the receiver readiness test results shall be required prior to delivery to the test range.

Although this procedure considers only those tests required to verify receiver performance as specified by Appendix A, it should be noted that considerable engineering data on the detailed operation of the receiver will be accumulated prior to the formal readiness tests. This engineering data will be available for review by the cognizant SAMSO/Aerospace personnel.

Section 2 of this procedure is a reprint of Appendix A entitled "Receiver General Requirements". Section 3 describes the testing area requirements appropriate to the readiness tests. Section 4 describes the standard laboratory test conditions under which the readiness tests will be performed. Section 5 lists the special test equipment required to perform the readiness tests. Section 6 addresses the specific tests to be performed to ensure that the requirements of Appendix A are satisfied.

Finally, Appendix I describes the MX 450 Test Set which will be used during the readiness test to exercise the receiver and to display test data. Appendix II describes the calibrate and test modes of operation.

REVISIONS

SUBJECT:

Readiness Test Procedure

2.0 RECEIVER GENERAL REQUIREMENTS (APPENDIX A)

The receiver shall extract precise range and range rate information from protected signals transmitted by four transmitters, and will be designed and packaged for an aircraft environment without in-flight maintenance. The receiver shall comprise 1 RF module, 4 precision signal processor modules, a frequency source module, an interface module to the GFE tape unit and power supply.

Input Specification

Signal Sensitivity Measurement	-140 dBm (min)
Center Frequency	1575 MHz
Anti-Jam Margin for Input Signal at -130 dBm	45 dB (min)
Dynamic Range	60 dB (min)
Maximum Dynamics for Measurement Accuracy(1)	$\dot{R}$ = 7000 ft/sec $\ddot{R}$ = 175 ft/sec^2 $\dddot{R}$ = 0 ft/sec^3
Maximum Dynamics for Tracking	$\dddot{R}$ = 320 ft/sec^3

(1) Specified limits of $\dot{R}$, $\ddot{R}$ and $\dddot{R}$ are upper limits, neither one may be exceeded when accuracy measurements are required.

Measurement Accuracies at -140 dBm

Standard Deviation	1σ
Pseudo-Range (each channel)	5 ft
Pseudo-Doppler (each channel)	0. 5 ft/sec

Measurement Bias Error

Pseudo-Range (each channel)	0. 2 ft (max)

Protected Signal Characteristics

Modulation	Bi-Phase
Bit Rate	10 MBPS
Code Length	2^{25} Bits
Code Type	Pseudo-Random

Initial Acquisition

The receiver shall have the capability to acquire the Grumman Aerospace Corporation acquisition signal at -100 dBm.

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SUBJECT:

Readiness Test Procedure

Reacquisition

The protected signal channels shall have the capability to reacquire without aiding in a reasonable time under reasonable aircraft velocity and acceleration conditions whenever such signals are momentarily lost due to maneuvers.

Digitizer Characteristics

Pseudo-Range Resolution (per channel)	0. 5 ft
Pseudo-Doppler Resolution (per channel) counted over 0. 1 sec nominal	0. 05 ft/sec

Output Characteristics

5 sets of measurements (i. e. , pseudo-range, pseudo-range rates) per second.

SUBJECT:

Readiness Test Procedure

3.0 TESTING AREA REQUIREMENTS

3.1 WORKING SPACE

3.1.1 Benches

Two standard 8 foot benches will be required for the MX-450 Navigation Receiver and its associated test equipment.

3.1.2 Screen Room

At least one screen room will be required for readiness testing. This screen room will be used in conjunction with tests requiring low signal levels on the order of -140 dBm.

3.2 CLEARANCE STATUS

The laboratory tests may be conducted in an Unclassified area. Attending personnel other than Magnavox employees will be escorted.

3.3 EXTERNAL INTERFACE

3.3.1 Cable Harness

Major Assemblies of the MX-450 Navigation Receiver will be interconnected using a Magnavox furnished interface wiring harness.

3.3.2 Prime Power

A prime power source of 115 VAC, 60 Hz, 8 amps., and 28 VDC, 4 amps., will be required by the MX-450 for laboratory readiness tests.

3.3.3 Test Set

An MX-450 Test Set will be utilized by Magnavox to simulate signal dynamics and to display receiver data in lieu of an airborne data recorder. A detailed description of this test set is presented in Appendix I.

REVISIONS

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Readiness Test Procedure.

4.0 STANDARD TEST CONDITIONS

The MX-450 Navigation Receiver will be tested under the following standard test conditions.

4.1 TEMPERATURE

Ambient room temperature between the limits of 15°C (59°F) and 35°C (90°F).

4.2 ATMOSPHERIC PRESSURE

Prevailing room ambient.

4.3 HUMIDITY

Prevailing room ambient.

4.4 WARM-UP PERIOD

The equipment shall be operated for 15 minutes before making any measurements for record.

SUBJECT:

Readiness Test Procedure.

5.0 TEST EQUIPMENT*

Item	Manufacturer	Type No.	Quantity
Counter	Hewlett Packard	5245L	2
Frequency Converter	Hewlett Packard	5254B	1
Interval Time Unit	Hewlett Packard	5262A	1
Oscilloscope	Tektronix	547	1
Spectrum Analyzer	Hewlett Packard	8554L/8552A/ 141S	1
Spectrum Analyzer	Hewlett Packard	8551B/851B	1
Power Meter	Hewlett Packard	432A	1
RF Voltmeter	Boonton	91H-S5	1
Power Supply	Harrison Labs	520A	1
Attenuator	Kay	461B	1
Coax Cable	--	RG-223	A/R

* Equivalent equipment may be substituted as required.

SUBJECT:
Readiness Test Procedure

6.0 READINESS TESTS

6.1 PROTECTED SIGNAL CHARACTERISTICS

6.1.1 Modulation

Monitor the correlator 113-3/4 MHz L.O. of channel 1 in the signal processor with a scope. Set the sweep rate to 5 nS per division and synchronize the scope to the coder clock. Observe the biphase modulation. Repeat for channels 2, 3 and 4.

Requirement: Biphase modulation

6.1.2 Code Type

Monitor the correlator 113-3/4 MHz L.O. of channel 1 in the signal processor with a spectrum analyzer. Set the horizontal scale to 5 MHz/division centered at 113-3/4 MHz. Notice the sin x/x distribution of the L.O. signal which characterizes a pseudo-random code. Repeat for channels 2, 3 and 4.

Requirement: Pseudo-random code

6.1.3 Code Bit Rate

Count the PN coder clock rate of channel 4. Repeat for channels 2, 3 and 4.

Requirement: Bit Rate = 10 MBPS

6.1.4 Code Length

Count the PN coder clock in channel 1. Use the "all ones" detector output of the coder to start/stop the counter. Count the number of clock pulses between the "all ones" intervals. Repeat for channels 2, 3 and 4.

Requirement: Code Length = 2^{25} = 33554432 bits

6.1.5 RF Frequency

Remove the PN modulation from the test signal in the microwave receiver and count the test signal output frequency. Use a H.P. 5248M counter and a H.P 5254B frequency converter. The frequency should be within the accuracy of the reference oscillator which is $\pm 5 \times 10^{-8}$.

Requirement: RF Frequency = 1575 MHz

REVISIONS

6.2 DATA OUTPUT CHARACTERISTICS

6.2.1 Format

The MX-450 Test Set which is described in detail in Appendix I, demultiplexes any 2 of 13 data words strobed from the signal processor during each 0.2 second interval. These two words are selected with toggle switches and are displayed on the front panel of the test set. Referring to the data format shown in Figure 6.1, select the desired words and verify the presence of the following data with the 0.2 second update rate:

Data Word Number	Type of Data
0	Flt. No. 4-channel Status
1	Event Marker System Status Frame Count
2, 3, 4, 5	4-Range Words
6, 7, 8, 9	4-Doppler Words
10, 11, 12	6-AGC Words

Requirement: 5 sets of measurements (i.e., pseudo-range, pseudo-range rate) per second.

6.2.2 Resolution

With the aid of the display charts and the data format shown in Figure 6.1, observe that the least significant bit is 2^{-8} of a code chip for pseudo-range readout.

The pseudo-range resolution is:

$$\frac{100\ \text{nS}}{\text{code chip}} \times \frac{2^{-8}\ \text{code chip}}{\text{LSB}} \quad 0.39\ \text{nS/LSB}$$

Requirement: Pseudo-range resolution = 0.5 ft.

DATA WORD	BIT NUMBER 32–25	BIT NUMBER 24–17	BIT NUMBER 16–9	BIT NUMBER 8–1
	32 31 30 29 28 27 26 25	24 23 22 21 20 19 18 17	16 15 14 13 12 11 10 9	8 7 6 5 4 3 2 1
0	DISCRETES: 24 23 22 21 20 19 18 17	DISCRETES: 16 15 14 13 12 11 10 9	DISCRETES: 8 7 6 5 4 3 2 1	FLIGHT #: 80 40 20 10 8 4 2 1
1	DISCRETE: 24 23 22 21 20 19 18 17	DISCRETE: 16 15 14; FRAME COUNT: M_{S_B} 12 11 10 9	FRAME COUNT: 8 7 L_{S_B}; DISCRETE: 5 4 3 2 1	EVENT MARKER: 0 0 0 0 8 4 2 1
2		2^{11} ←	CHANNEL #1 RANGE	→ 2^{-8}
3		2^{11} ←	CHANNEL #2 RANGE	→ 2^{-8}
4		2^{11} ←	CHANNEL #3 RANGE	→ 2^{-8}
5		2^{11} ←	CHANNEL #4 RANGE	→ 2^{-8}
6		2^{12} ←	CHANNEL #1 DOPPLER	→ 2^{-7}
7		2^{12} ←	CHANNEL #2 DOPPLER	→ 2^{-7}
8		2^{12} ←	CHANNEL #3 DOPPLER	→ 2^{-7}
9		2^{12} ←	CHANNEL #4 DOPPLER	→ 2^{-7}
10	M_{S_B} ← AGC #2 → L_{S_B}	X ←→ X	M_{S_B} ← AGC #1 → L_{S_B}	X ←→ X
11	M_{S_B} ← AGC #4 → L_{S_B}	X ←→ X	M_{S_B} ← AGC #3 → L_{S_B}	X ←→ X
12	M_{S_B} ← AGC #6 → L_{S_B}	X ←→ X	M_{S_B} ← AGC #5 → L_{S_B}	X ←→ X
13	←	NOT USED		→
14	←	NOT USED		→
15	←	NOT USED		→

WORD #0 DETAIL

CHNL #	STANDBY	SEARCH	PULLIN	TRACK	CODE AMM	SPARE
DISCRETE BIT ASSIGNMENT						
1	1	2	3	4	5	6
2	7	8	9	10	11	12
3	13	14	15	16	17	18
4	19	20	21	22	23	24

WORD #1 DETAIL

BIT #	DISCRETE BIT ASSIGNMENT
1	SYNTHESIZER AMM
2	MICROWAVE PLL AMM
3	MRL/HAZELTINE TAPE
4	CALIBRATE MODE
5	RF SIGNAL PRESENT
6-13	FRAME COUNT
14-24	SPARES

NOTE:

1 - LOGICAL 1 = TRUE = 5 V NOMINAL = LAMP ON
2 - AMM = AUTOMATIC MALFUNCTION MONITOR, LOGICAL 1 = MALFUNCTION
3 - FRAME COUNT = 8 BIT BINARY COUNT OF 1 SEC. DATA TRANSFER PULSES
4 - RANGE LSB = 100/256 FT
5 - DOPPLER LSB = 1/12.8 Hz
6 - AGC WEIGHTING = REFER TO ENGR DATA

Figure 6.1 MX-450 Test Set Data Format

REVISIONS

SUBJECT:
Readiness Test Procedure

For pseudo-doppler readout observe that the least significant bit is 2^{-7} Hz of carrier.

The pseudo-doppler resolution is:

$$\frac{1}{1.575\ \frac{\text{cycles}}{\text{ft}} \times 2^{7}\ \frac{\text{LSB}}{\text{cycle}} \times 0.1\ \text{second sample}} = 0.049\ \text{ft/sec/LSB}$$

Requirement: Pseudo-doppler resolution = 0.05 ft/sec

6.3 ACQUISITION TESTS

6.3.1 Initial Acquisition

For initial acquisition the receiver will operate in the test mode which is described in Appendix II. The synch power boost signal will be set at -100 dBm and the tracking signal level will be set at -123 dBm. To simulate a transmit signal, channel 4 will provide a PN code at 10 MHz, a 20 MHz L.O. and a synch power boost logic signal coincident with the "all ones" vector of the code to the test signal generator located in the microwave receiver. The signal level of this test signal will be adjusted with an external 0-100 dB attenuator. Channels 1, 2, and 3 will use the channel 4 code and will acquire and track this test signal. This procedure utilizes the test setup shown in Figure 6.2 and consists of the following steps:

A. Set the power boost signal level to -100 dBm.

1. Set the H.P. 614A signal generator to 1575 MHz and calibrate its output level at -20 dBm using a H.P. 432A power meter.
2. Apply a -100 dBm CW signal to the microwave receiver.
3. Disable the 135 MHz max. AGC.
4. Monitor the 135 MHz IF output with a H.P. 8554L/8552A spectrum analyzer.
5. Disconnect the PN modulation from channel 4 to the test signal generator.
6. Switch the test signal generator to a continuous power boost mode.
7. Adjust the test signal level with a Kay 461B attenuator as shown in Figure 6.2 until its level is equal to the CW generator level as measured at the 135 MHz IF output.
8. Remove the CW generator and terminate the RF input of the microwave receiver with a 50Ω resistive load.

SUBJECT:

Readiness Test Procedure

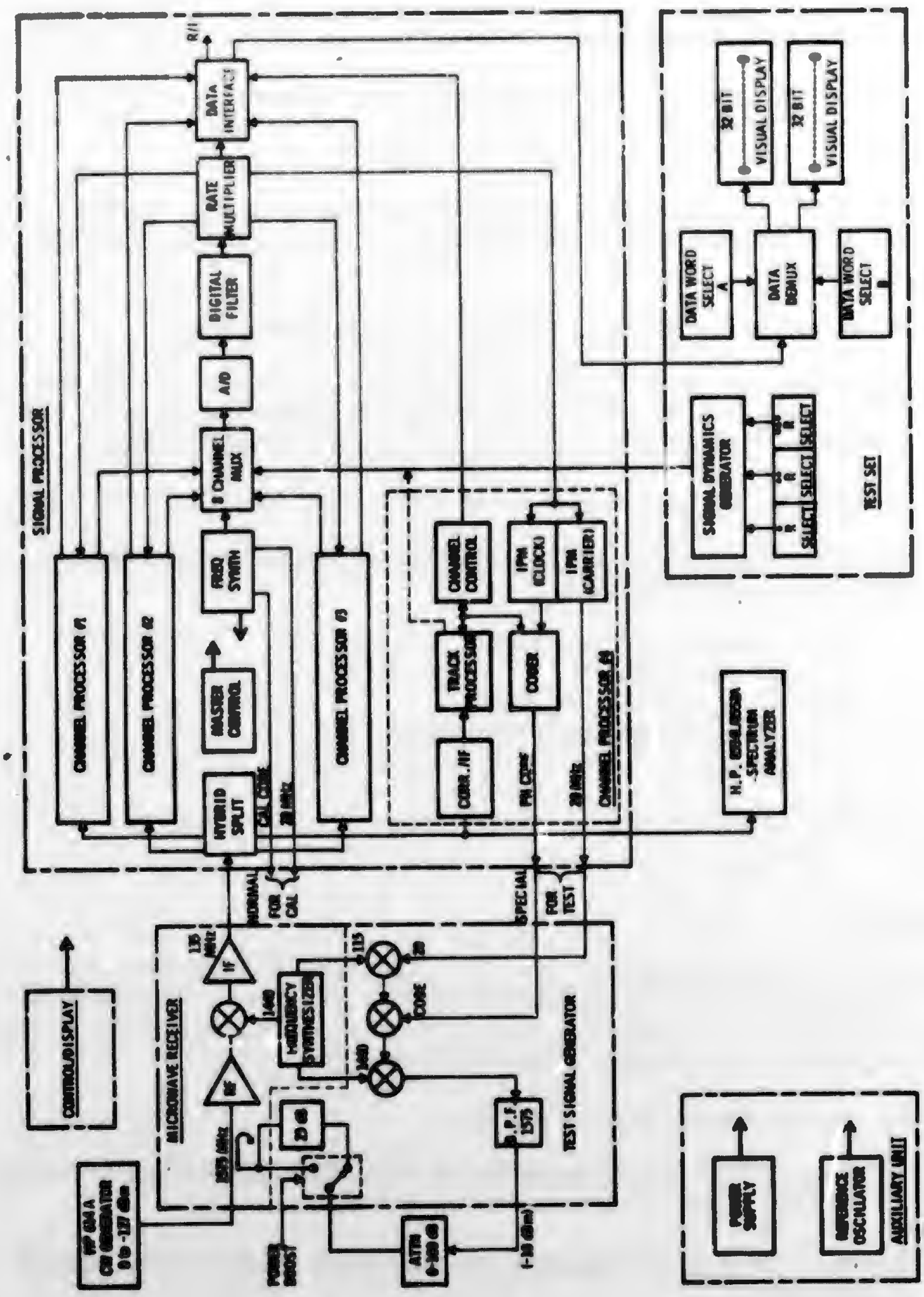

Figure 6.2 MX-450 Readiness Test Configuration

SUBJECT:
Readiness Test Procedure

9. Enable the 135 MHz AGC and remove the continuous power boost.

10. Reapply the PN modulation to the test set.

B. Acquire the test signal driven by channel 4 with channels 1, 2, and 3.

1. Initiate a test mode from the test set panel.

2. Observe the acquisition of processor channels 1, 2, and ? indicated by the track mode lights on the control/display panel. All up to 20 seconds for acquisition.

3. Repeat steps 1 and 2 ten times and record the successes.

4. Raise and lower the power boost level of the test signal in 1 dB steps from -97 to -103 dBm with the external attenuator and repeat steps 1, 2 and 3. (Note that the -123 dBm signal will vary ±3 dB during this test.)

5. Simulate a 1000 knot doppler at the test set and repeat steps 1, 2 and 3.

6. Exchange the following P.C. cards between channel 3 and 4 and repeat the applicable parts of steps 1, 2 and 3:

A - Correlator/Local Ref.
B - IF Assembly
C - P.C. Receiver #1 and 2
D - Incremental Phase Modulator
E - Coder

Requirement: The receiver shall initially acquire with a -100 dBm power boost signal.

6.3.2 Reacquisition

For this test the tracking signal will be set to -123 dBm and channel 4 will operate the test signal generator in the microwave receiver to provide a simulated transmit signal as described in Appendix II. This test procedure utilizes the test configuration shown in Figure 6.2 and consists of the following steps:

A. Set the tracking signal level to -123 dBm.

1. Set the H.P 614A signal generator to 1575 MHz and calibrate the signal level at -20 dBm using a H.P. 432A power meter.

2. Apply a -100 dBm CW signal to the microwave receiver from the CW signal generator.

3. Disable the 135 MHz AGC.

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4. Monitor the 135 MHz IF output with a H.P 8554L/8552A spectrum analyzer.

5. Disconnect PN modulation from the test signal.

6. Adjust the test signal level with the external attenuator until its level at the 135 MHz IF output is equal to the CW generator level.

7. To adjust the signal tracking level to -123 dBm, add an additional 23 dB attenuation to the test signal attenuator.

8. Remove the CW generator and terminate the RF input to microwave receiver.

9. Enable the 135 MHz AGC and reconnect the PN modulation from channel 4.

B. Acquire the test signal driven by channel 4 with channels 1, 2, and 3.

1. Initiate a test mode from the test set panel.

2. Observe the acquisition of processor channels 1, 2, and 3 indicated by the TRACK lamps on the control/display panel.

3. Disable the sync power boost at the test set.

C. Reacquire channels 1, 2, and 3.

1. Break lock by momentarily disconnecting the test signal with a switch at the test set.

2. Reapply the signal after a 5 second interval and observe the acquisition of channels 1, 2, and 3 at -123 dBm. Allow up to 20 seconds for reacquisition.

3. Repeat steps 1 and 2 ten times and record the successes.

4. Successively lower the signal tracking level with the test signal attenuator in 1 dB steps and each time break lock and reacquire by repeating steps 1, 2 and 3.

5. Return to a tracking level of -123 dBm.

6. Simulate a 1000 knot doppler, break lock and reacquire by repeating steps 1, 2 and 3.

7. Select a dynamics program at the test set which simulates a 175 ft/sec² with a max. velocity of 1000 knots. Break lock and reacquire by repeating steps 1, 2 and 3.

8. Follow step 6.3.1.B.6 to test channel 4. Repeat the applicable parts of 6.3.2 B and C.

Requirement: Protected signal channels shall have the capability to acquire without aiding in a reasonable time under reasonable aircraft velocity and acceleration conditions.

6.4 TRACKING TESTS

All tracking tests will utilize the same test mode described in Appendix II. Various signal and/or jamming levels will be set up to a reference level from a calibrated CW generator. The 4th channel processor will provide the common PN code to the test signal generator along with a power boost synch signal for initial acquisition. When driven with the signal dynamics generator in the test set, channel 4 will provide the required $\dot{R}$, $\ddot{R}$, and $\dddot{R}$ signal dynamics to the test signal generator in the microwave receiver.

6.4.1 Antijam Margin

A. Set the tracking signal level to -123 dBm.

   1. Follow steps 6.3.2-A.

B. Acquire channels 1, 2, and 3 with the test signal.

   1. Initiate a test mode from the test set panel.

   2. Observe the acquisition of channels 1, 2 and 3 indicated by the TRACK lamps on the control/display panel.

C. Reduce the tracking signal level to -130 dBm.

D. Provide a jamming signal source to test the antijam capability of channel processors 1, 2, and 3.

   1. Apply a calibrated 1575 MHz CW signal to the microwave receiver at a level of -100 dBm.

   2. Gradually increase the CW jammer to a level of -80 dBm. Observe that channels 1, 2, and 3 continue to track.

   3. Slowly increase the jamming level until each channel looses lock. Observe the antijam level at which lock was lost.

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4. Reacquire the three channels by raising the tracking signal level to -123 dBm and removing the CW jamming signal.

5. Repeat steps 1 - 4 ten times and compute the average antijam margin.

6. While tracking the test signal with a J/S ratio of 45 dBm, adjust the CW jamming signal to various points across the 20 MHz RF bandwidth to check for jamming sensitivity across the signal spectrum.

7. Follow step 6.3.1.B.6 to test channel 4. Repeat 6.4.1 with respect to channel 4.

Requirement: A minimum A/J margin of 45 dB for an input signal at -130 dBm.

6.4.2 Dynamic Range

A. Set the test signal level to -123 dBm and acquire channels 1, 2 and 3.

B. Vary the signal tracking level over the maximum dynamic range.

1. Vary the signal level from -80 to -140 dBm.

2. Raise the signal level from -80 dBm in 5 dBm steps until one of the three processor channels looses lock.

3. Reacquire the three channels and reduce the signal level from -140 dBm in 1 dB steps until loss of lock occurs in each channel.

4. Repeat step 3 ten times and calculate the average threshold to loss-of-lock for each channel.

5. Follow step 6.3.1.B.6 to test channel 4. Repeat the applicable portions of 6.4.2.

Requirement: A minimum dynamic signal range of 60 dB.

6.4.3 Tracking vs. Jerk

A. At the test set panel, set

$\dddot{R}$ 320 ft/sec^3

$\ddot{R}$ 175 ft/sec^2

$\dot{R}$ 7000 ft/sec

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2. To check the magnitude of the signal dynamics on the carrier, monitor the 20 MHz carrier signal and the output of the signal dynamics generator. Toggle the dynamics switch to AUTOMATIC and measure the duration of the jerk pulse. Ten seconds after the end of the jerk pulse, switch channel 4 to ACQUIRE and measure the doppler offset on the 20 MHz carrier. (ACQUIRE opens the loop and zeros the acceleration register.) Calculate the signal dynamics with the following equation:

$$1.575 \text{ Hz} = 1 \text{ ft/sec} \quad (1)$$

$$a = v/10 \quad (2)$$

$$j = a/t_2 = v/10 \times 1.6 \times t_2 \quad (3)$$

where

j = jerk ($\dddot{R}$)

a = acceleration ($\ddot{R}$)

v = velocity in Hz after 10 seconds ($\dot{R}$)

3. To check the magnitude of the signal dynamics on the code, repeat step 2 and measure the doppler offset on the code clock. Calculate the signal dynamics with the following equation:

$$1 \text{ code chip} = 100 \text{ ft.} \quad (4)$$

$$a = v/10 \quad (5)$$

$$j = a/t_2 = v/10 \times 1.6 \times t_2 \quad (6)$$

where

j = jerk ($\dddot{R}$)

a = acceleration ($\ddot{R}$)

v = velocity in Hz after 10 seconds ($\dot{R}$)

t_2 = jerk duration in seconds

B. Acquire and track channels 1, 2, and 3 with the test signal set to -123 dBm.

C. Apply the signal dynamics (set up in Step 6.4.3-A) to channel 4 by toggling the signal dynamic switch from MANUAL to AUTOMATIC.

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D. Monitor channels 1, 2, and 3 insure that they remain in the track mode for 10 jerk intervals

E. Follow step 6.3.1.b.6 to test channel 4. Repeat the applicable parts of section 6.4.3.

Requirement: Maximum dynamics for tracking is $\dddot{R}$=320 ft/sec^3

6.5 MEASUREMENT ACCURACY

Since the test data will be statistical in nature, it will be necessary to record sufficient test data in order to estimate the true statistical parameters of the actual measurement data. Criteria for measurement accuracy will be such that for a 90% confidence interval the product of the normalized confidence limit and the sampled standard deviation will not exceed the one-sigma specification for pseudo-range and pseudo-doppler.

The tests for measurement accuracies will be made with a signal level of -140 dBm. Pseudo-range and pseudo-doppler for the reference channel (4) and for the tracking channels (1, 2, and 3) will be read from the test set data display.

6.5.1 Pseudo Range Accuracy

A. Set the tracking signal level to -123 dBm.

B. Initialize all four processor channels with a calibrate mode as described in Appendix II.

1. Modulate the test signal generator with a CAL code and a 20 MHz CW signal from the signal processor synthesizer as shown in Figure 6.2.

2. Initiate a calibrate mode by depressing the CALIBRATE button on the control/display panel.

3. Wait 16 seconds for all four channels to go to a standby mode indicating that the calibrate mode is complete.

C. Track the test signal with channels 1, 2, and 3, and reduce the test signal level to -140 dBm.

D. Preset the maximum signal dynamics on the test set by following step 6.4.3-A and apply the signal dynamics to the test signal and observe that channels 1, 2, and 3 are tracking.

E. Test for pseudo range accuracy with a velocity of 7000 ft/sec. When the test signal reaches a doppler of 11 kHz switch channel 4 to STANDBY. (Standby mode removes the error signal from the loop filter and zeros its acceleration register.)

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F. Record pseudo-range data samples simultaneously from channel 4 on register A and channel 1 on register B of the test set. Repeat for channels 2 and 3.

G. Test for pseudo range accuracy with an acceleration of 175 ft/sec^2.

1. Between the limits of ±7000 ft/sec with a = 175 ft/sec^2, record pseudo-range data samples simultaneously from channel 4 on register A and from channel 3 on register B.

H. Repeat Step F for channels 2 and 3.

I. Follow Step 6.3.1.B.6 to test channel 4. Repeat the applicable portions of 6.5.1.

J. Calculate the standard deviation for pseudo range. For pseudo range, the equation for computing the standard deviation is:

$$\sigma \Delta R/R = \sqrt{\frac{1}{N} \sum_{i=1}^{N} \left[R_{(Chnl\ 4)} - R_{(Chnl\ 1,\ 2\ or\ 3)} \right]^2}$$

Requirement: With a signal level of -140 dBm, the standard deviation of pseudo-range shall not exceed 5 ft.

6.5.2 Pseudo Doppler Accuracy

A. Repeat Steps 6.5.1.A - D.

B. Test for pseudo doppler accuracy with a velocity of 7000 ft/sec. Follow Step 6.5.1.E.

C. Record pseudo doppler samples simultaneously from channel 4 on register A and channel 1 on register B of the test set. Repeat for channels 2 and 3.

D. Test for pseudo doppler accuracy with an acceleration of 175 ft/sec^2. Follow Step 6.5.1.G.

E. Repeat Step D for channels 2 and 3.

F. Follow Step 6.3.1.B.6 to test channel 4. Repeat the applicable portions of 6.5.2.

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G. Calculate the standard deviation for pseudo doppler. For pseudo-doppler the equation for computing the standard deviation is:

$$\sigma \Delta V/V = \sqrt{\frac{1}{N} \sum_{i=1}^{N} \left[V_{(\text{Chnl } 4)} - V_{(\text{Chnl } 1,\ 2 \text{ or } 3)} \right]^2}$$

Requirement: With a signal level of -140 dBm, the standard deviation of pseudo doppler shall not exceed 0.5 ft/sec.

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APPENDIX I

MX-450 TEST SET DESCRIPTION

Basically, the test set provides three major functions:

1. Receiver data display
2. Signal dynamics simulation
3. Mode control

Both the data display logic and the signal dynamics generator will be described in this section. The mode control simply consists of switches which provide logic levels into the channel and master controllers of the signal processor which override the existing modes of operation. A block diagram of the test set is shown in Figure I. 1.

I. 1 DATA DISPLAY LOGIC

In order to have qualitative short-term observable knowledge of the MX-450 data flow, the test set has two independent lamp banks (A and B) each containing 32 data bits. Three refresh rates are provided - continuous or synchronous with data flow, once a second, and a one time manually activated rate. Thumbwheel word select switches provide the operator a choice of 1 out of 13-32 bit data words which are strobed from the receiver at a 0. 2 second rate. These words are subsequently displayed at the selected refresh rate on either of the two lamp banks.

The hardware which implements the data display logic is straightforward. The word addressing logic for the recorder interface data in the receiver was merely duplicated and word select and data refresh logic was added. Thus, two gated clock streams enter data into two shift register groups of 32 static bits each. Lamp drivers translate the presence of a "1" or "0" bit to the front panel lamp bank. Thus, the data displayed will duplicate the data collected and simultaneously be entered into the recorder interface memory. Data eventually dumped to the recorder is not displayed. A logic diagram of the data display is shown in Figure I. 2.

I. 2 SIGNAL DYNAMICS GENERATOR

The signal dynamics generator works in conjunction with channel processor #4 to simulate a transmit signal with the desired signal dynamics. This generator provides analog error signals to the carrier and clock loops of channel 4. The error signals operate on the open loops to implement the desired signal dynamics responses selected on the test set panel. A logic diagram for the signal dynamics generator is shown in Figure I. 3.

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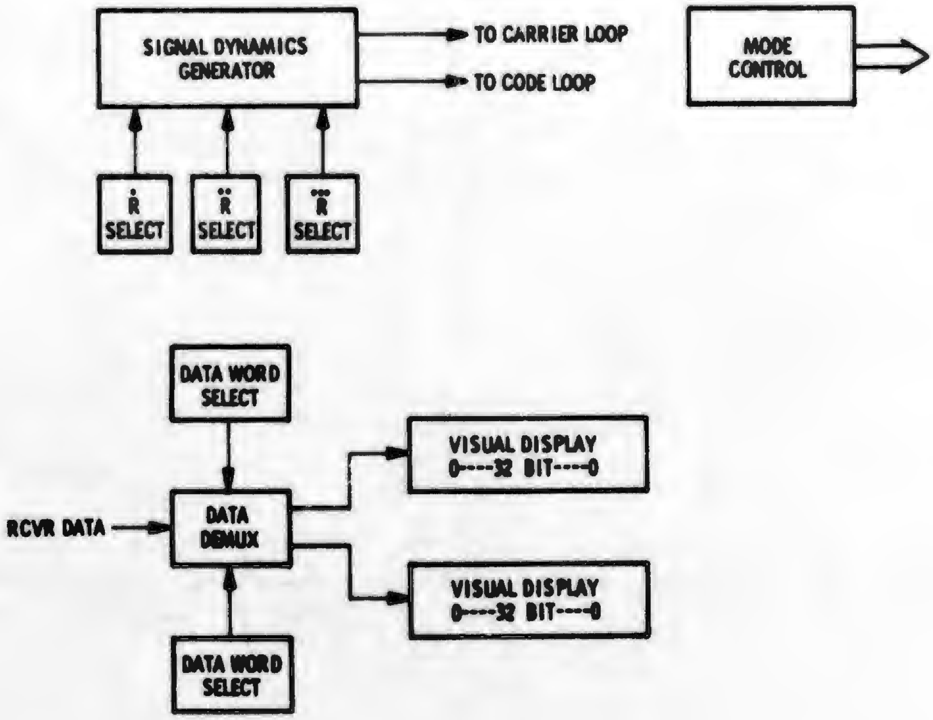

Figure I.1 Test Set Block Diagram

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Readiness Test Procedure

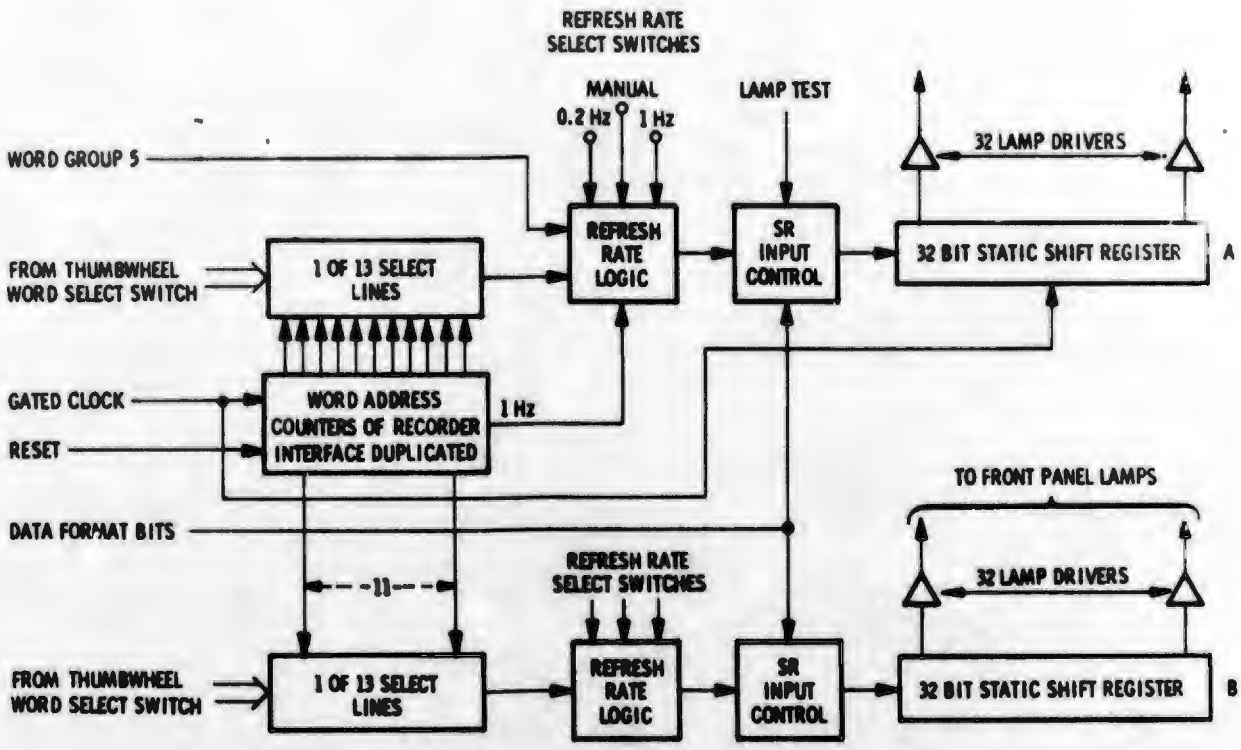

Figure I. 2 Test Set Data Display Logic Diagram

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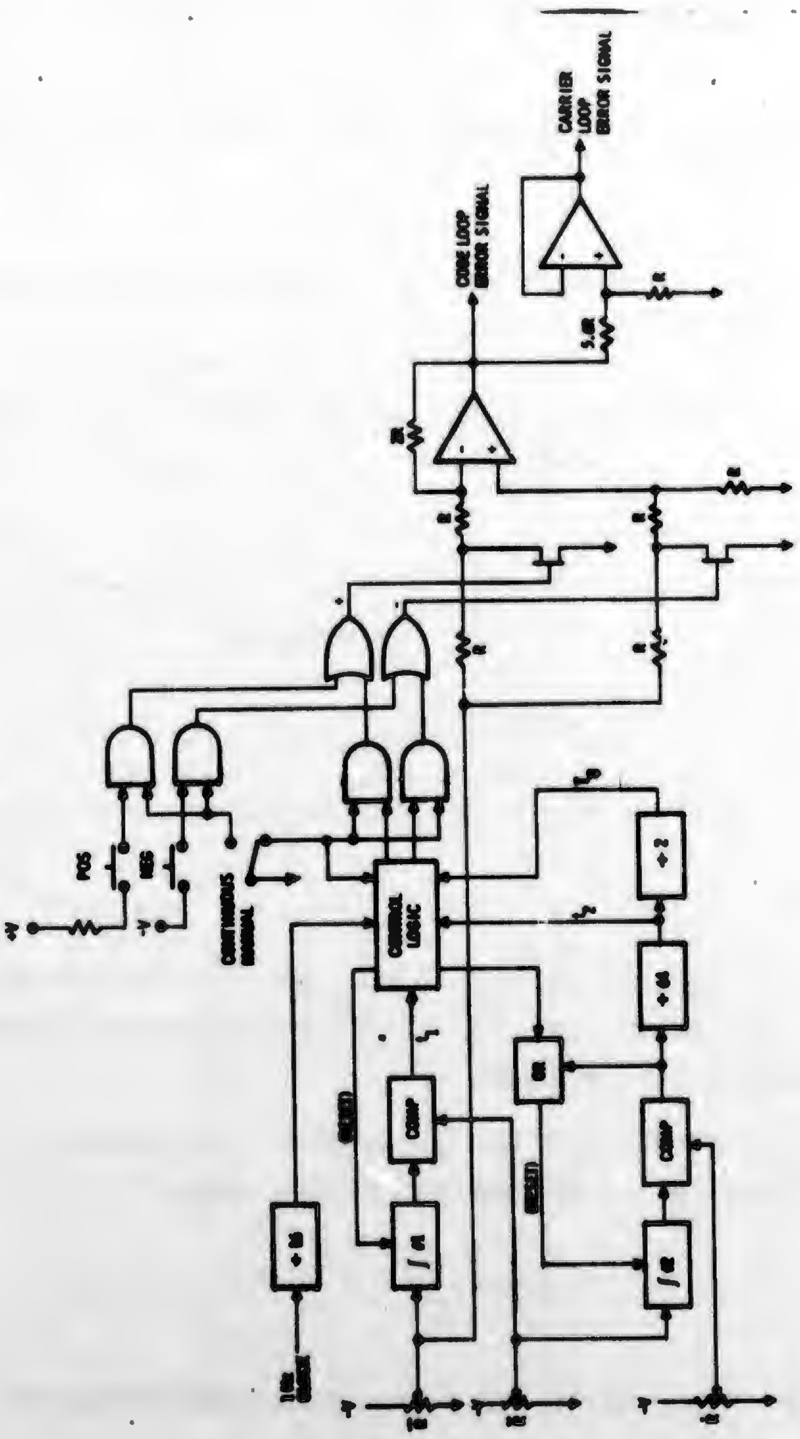

Figure I.3 Signal Dynamics Generator Logic Diagram

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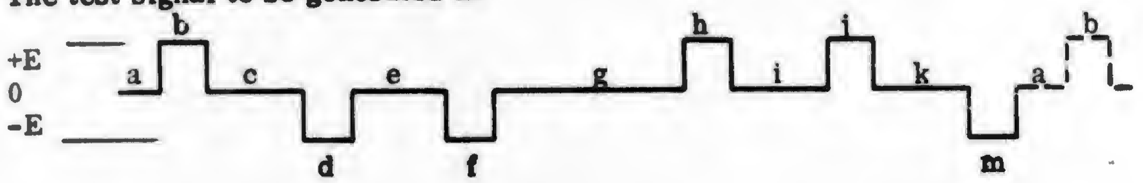
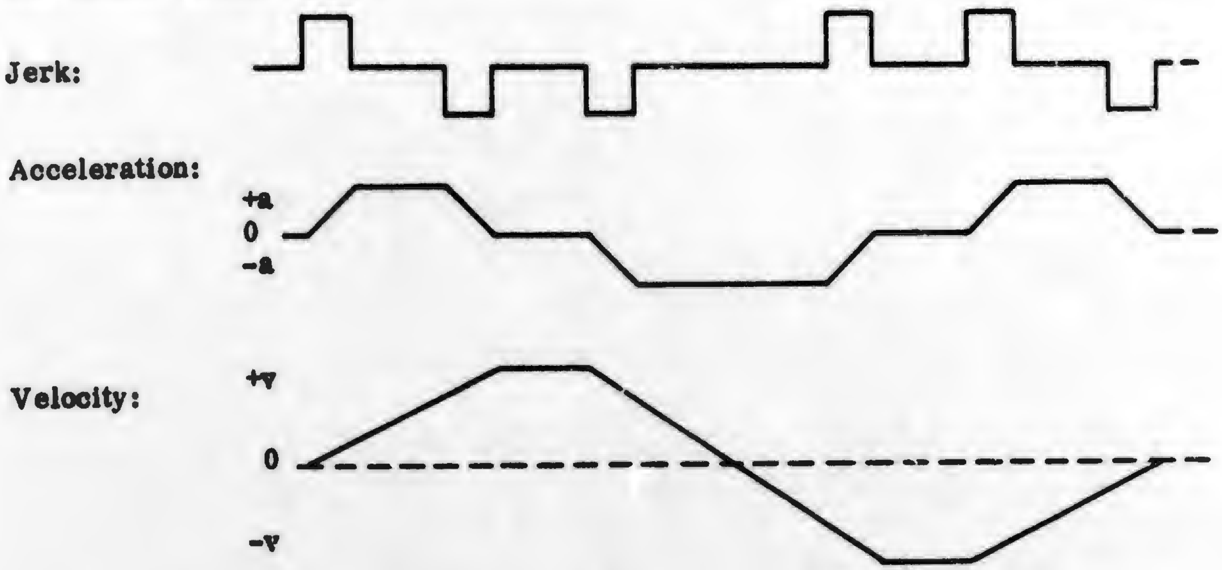
1.2.1 Automatic Mode of Operation

The test signal to be generated is



which, when applied to the channel 4 loop filter, will generate acceleration and velocity profile as follows:



Pulse amplitude $A_b = A_d = A_f = A_h = A_m = A_1 = E$, where $|E| \leq 2$ volt and is set by the $\dddot{R}$ pot on the test control panel. $\dddot{R} \doteq 2$ volt represents the maximum jerk that can be generated by the test signal.

Pulse duration $T_b = T_d = T_f = T_h = T_m = T_1 = t_1$ where t_1 is determined by the pot. settings of $\dddot{R}$ and $\ddot{R}$ and the integrator #1 time constant τ_1 (τ_1 = .24 sec) i.e.

$$t_1 = \frac{\ddot{R}\ \tau_1}{\dddot{R}}$$

For a given $\dddot{R}$, the $\ddot{R}$ pot will determine the maximum acceleration that can be attained in t_1 seconds, i.e.,

$$a = \dddot{R}\, t_1 = \ddot{R}\, \tau_1$$

Duration $T_c = T_k = t_2$, where t_2 is determined by the pot. Settings of $\ddot{R}$ and $\dot{R}$, a scale factor of 64 and the integrator no. 2 time constant τ_2 (τ_2 = .62 sec) i.e.,

$$t_2 = \frac{\dot{R}\,\tau_2\,(64)}{\ddot{R}} = \frac{40\,\dot{R}}{\ddot{R}}$$

For a given $\ddot{R}$, $\dot{R}$ will determine the maximum velocity that can be attained in t_2 seconds, i.e.,

$$v = at_2 = \ddot{R}\,\tau_1\, t_2 = 40\,\dot{R}\,\tau_1$$

The interval T_g (between positive max. V and negative max. V) is equal to $2t_2 + 3t_1$.

The maximum velocity seen by the receiver is determined by the following equation:

$$V_{max} = \ddot{R}\,\tau_1\,(t_1 + t_2) \approx \ddot{R}\,\tau_1\, t_2$$

Durations T_e and T_i are 16-seconds and are for measurement purposes after maximum velocity is attained.

I. 2. 2 Manual Mode of Operation

In the manual mode of operation, $\dot{R}$ sets the amount of jerk. The two push-button switches on the test control panel allow positive or negative jerk to be applied to the system for any duration desired.

APPENDIX II

MX-450 CALIBRATE AND TEST MODE DESCRIPTIONS

II. 1 CALIBRATION MODE

Under normal operating conditions the calibrate mode of operation serves to initialize the signal processor. This is accomplished as shown in Figure 6.2 by supplying a CAL code (which is simply a 1, 1, 0, 0 binary sequence at a 2.5 MHz rate) and a 20 MHz fixed frequency CW signal from the frequency synthesizer of the signal processor to the test signal generator in the microwave receiver. This generator provides a 1575 MHz biphase modulated signal at a constant level of -123 dBm to the input of the microwave receiver.

When a calibrate mode is initiated, all 4 channel processor channels switch to a CAL code and acquire the calibrate signal. Sixteen seconds later, after the tracking loops have nulled and AGC transcients have settled out, the calibrate signal is removed and a master reset pulse (generated from the 5 MHz reference oscillator) zeros the 4 pseudo-range data registers and forces the processor channels to a standby mode to await the arrival of a synchronizing power boost signal.

After a calibrate cycle is completed, any differential delay between processor channels is cancelled and zero range is referenced to the input port of the microwave receiver.

II. 2 TEST MODE

During a test mode of operation a transmit signal is simulated to provide signal dynamics for 3 of the 4 processor channels. The equipment configuration for this mode of operation is shown in Figure 6.2. In this configuration, channel 4 provides a PN code and a 20 MHz CW signal to the test signal generator which is part of the microwave receiver. Signal dynamics are simulated by providing error signals from the signal dynamics generator which is part of the test set to the open carrier and code clock loops of channel 4.

All four processor channels use a common code during a test mode of operation. For initial acquisition the test signal generator output is power boosted from -123

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to -100 dBm for 25 μs with a solid state switch during each "all ones" vector from the PN coder of channel 4.

When a test mode of operation is initiated at the test set, channels 1, 2 and 3 initially acquire and track the simulated transmit signal. During a track mode, signal dynamics is applied from the test set and the transmit signal amplitude is varied with an external attenuator at the microwave receiver.

APPENDIX D

READINESS TEST RESULTS

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Subject MX450 ACCEPTANCE TESTS 11-10-71

7:50 AM EDGAR / WINTERSORN / GILLOGLY ARRIVED

PER PROCEDURE (CHNL #1,2 & 3)

				RESULTS
6.1.1	Modulation			OK
6.1.2	Code Type			OK
6.1.3	Code [illegible] Rate			OK
6.[illegible]	Code Length			OK
6.1.[illegible]	RF Frequency			OK
6.2	Data Format			OK
6.3.1	Initial Acquisition	8/8	#2-9/10	OK
6.3.2	Reacquisition (0 dynamics)	8/8		OK
	(500 KNOTS)	8/8		OK
	(175 fps²)	8/8	#2-8/9	OK
6.4.1	A/J CENT FREQ	10/10		OK
	+10 MHz	10/10		OK
	-10 MHz	10/10		OK
6.4.2	DYNAMICS (-140 dBm)	8/8		OK
	(-80 dBm)	8/8		OK
6.4.3	JERK	9/9		OK
6.5.1	BIAS MEASUREMENT			OK
6.5.2	PR ACCURACY	(See attachment)		OK
6.5.3	PD ACCURACY	(See attachment)		OK

This page witnessed and understood by: [signature] (Witness)
on: 11/10/71 (Date)

This page witnessed and understood by: ________ (Witness)
on: ________ (Date)

This page recorded
by: R Cnossen (Engineer)
on: 11-10-71 (Date)

Project No. ENGINEERING DEPARTMENT The MAGNAVOX COMPANY Page No. 3630[illegible]

Subject MX 450 ACCEPTANCE TESTS. (CHNL #4 TESTS)

CHNL #4 NOW OCCUPIES CHNL #3 SLOT
WITNESSED BY AL GILLOGLY
(see attachment)

6.3.1	Initial Acq.		8/8	ok
6.3.2	Reacq	(2 dynamics)	8/8	OK
		(500 ± V)	8/10	ok
		(175 ± A)	8/10	OK
6.4.1	A/J	(Center Freq)	8/10	ok
		(+10 MHz)	8/10	ok
		(-10 MHz)	8/10	ok
6.4.2	Dynamic Range	ATTN = 62 dB for 110 dBm		
		-140	8/8	ok
		-80	8/8	ok
6.4.3	Jerk		9/9	ok
6.5.2	PR ACCURACY	(see attachment)		OK
6.5.3	PD ACCURACY	(see attachment.)		ok

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on: 11/11/71 (Date)

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on: ______ (Date)

This page recorded by: K.S. [illegible] (Engr.)
on: 11/11/71 (Date)

Project No.

ENGINEERING DEPARTMENT

The MAGNAVOX COMPANY

Page No. 363057

Subject MX 450 READINESS TESTS

NOMENCLATURE	SERIAL NUMBER OF P.C. CARD			
	CHNL #1	CHNL #2	CHNL #3	CHNL #4
CORRELATOR / LOCAL REFERENCE	2	1	3	4
I.F. ASSEMBLY	2	4	3	1
P.C. RECEIVER #1	3	1	2	4
P.C. RECEIVER #2	3	4	1	2
INCREMENTAL PHASE MODULATOR	3	1	5	2
CODER	3	2	5	1

SERIAL NUMBERS OF P.C. CARDS FOR EACH CHANNEL IN MX 450 SIGNAL PROCESSOR

This page witnessed and understood by: ______ (Witness)

on: ______ (Date)

This page witnessed and understood by: ______ (Witness)

This page recorded

by: K.S. Cross

on: 11-11-71.

Subject MX 450 READINESS TESTS.

CHNL	PSEUDO RANGE ACCURACY MEASUREMENT (1 SIGMA)			
	V = 7000 fps	SAMPLES	A = 175 fps²	SAMPLES
#1	2.28 ft.	10	3.87 ft.	5
#2	1.93 ft	10	0.625 ft	5
#3	2.94 ft	10	4.48 ft	16
#4	3.20 ft	10	2.33 ft	10

CHNL	PSEUDO DOPPLER ACCURACY MEASUREMENT (1 SIGMA)			
	V = 7000 fps	SAMPLES	A = 175 fps²	SAMPLES
#1	0.156 fps	10	0.258 fps	6
#2	0.172 fps	10	0.227 fps	5
#3	0.436 fps	16	0.302 fps	8
#4	0.253 fps	10	0.154 fps	7

SUMMARY OF MEASUREMENT ACCURACY TESTS.

This page witnessed and understood by: ________ (Witness)
on: ________ (Date)

This page witnessed and understood by: ________ (Witness)
on: ________ (Date)

This page recorded by: R.S. [signature] (Engineer)
on: 11-12-71 (Date)

Computer Program

```
LIST

PACSTA     12:51     11/15/71

10 PRINT"MAL STATISICAL PROGRAM TO COMPUTE STANDARD DEVIATIONS"
20 PRINT"OF PSEUDO-RANGE AND PSEUDO-DOPPLER FOR THE 621B RECEIVER"
30 PRINT
40 PRINT"TYPE 1 FOR PSEUDO RANGE, TYPE 0 FOR PSEUDO DOPPLER";
50 INPUT W1
60 PRINT
70 PRINT
80 PRINT "ENTER NO. OF SAMPLES";
90 INPUT N
100 DIM X(30),Y(30),E(30),A(30),B(30),C(7),P(30),H(30)
110 LET U1 = 100/256
120 LET U2=10/(128*1.575)
130 PRINT "ENTER OBSERVABLE,REFERENCE OCTAL DATA "
140 PRINT"DO NOT ENTER MORE THAN 7 DIGITS PER CHANNEL"
150 FOR I = 1 TO N
160 GO SUB 190
170 NEXT I
180 GO TO 760
190 PRINT "PR.NO.";I;
200 INPUT A(I),B(I)
210 IF A(I)>=4*10↑6 THEN 240
220 LET T = A(I)
230 GO TO 270
240 LET W = 7777777-A(I)
250 LET A(I) = -W
260 LET T= A(I)
270 LET C7=C6=C5=C4=C3=C2=C1=0
280 LET D7=D6=D5=D4=D3=D2=V=0
290 LET J = ABS(T)
300 LET C7=INT(U/10↑6)
310 LET C6=INT(U/10↑5-10*C7)
320 LET C5=INT(U/10↑4-(100*C7+10*C6))
330 LET C4=INT(U/10↑3-(10↑3*C7+100*C6+10*C5))
340 LET C3=INT(U/100-(10↑4*C7+10↑3*C6+100*C5+10*C4))
350 LET C2=INT(U/10-(10↑5*C7+10↑4*C6+10↑3*C5+100*C4+10*C3))
360 LET C1=INT(U-(10↑6*C7+10↑5*C6+10↑4*C5+10↑3*C4+100*C3+10*C2))
370 LET D7 = C7*8↑6
380 LET D6 = C6*8↑5
390 LET D5 = C5*8↑4
400 LET D4 = C4*8↑3
410 LET D3 = C3*8↑2
420 LET D2 = C2*8
430 LET V=C1+D2+D3+D4+D5+D6+D7
```

```
440 IF T < 0 THEN 460
450 GO TO 470
460 LET V = -V
470 LET X(I) = V
480 IF B(I)>=4*10↑6 THEN 510
490 LET T = B(I)
500 GO TO 540
510 LET Z = 7777777-B(I)
520 LET B(I) = -Z
530 LET T = B(I)
540 LET C7=C6=C5=C4=C3=C2=C1=0
550 LET D7=D6=D5=D4=D3=D2=V=0
560 LET U = ABS(T)
570 LET C7=INT(U/10↑6)
580 LET C6=INT(U/10↑5-10*C7)
590 LET C5=INT(U/10↑4-(100*C7+10*C6))
600 LET C4=INT(U/10↑3-(10↑3*C7+100*C6+10*C5))
610 LET C3=INT(U/100-(10↑4*C7+10↑3*C6+100*C5+10*C4))
620 LET C2=INT(U/10-(10↑5*C7+10↑4*C6+10↑3*C5+100*C4+10*C3))
630 LET C1=INT(U-(10↑6*C7+10↑5*C6+10↑4*C5+10↑3*C4+100*C3+10*C2))
640 LET D7 = C7*8↑6
650 LET D6 = C6*8↑5
660 LET D5 = C5*8↑4
670 LET D4 = C4*8↑3
680 LET D3 = C3*8↑2
690 LET D2 = C2*8
700 LET V=C1+D2+D3+D4+D5+D6+D7
710 IF T<0 THEN 730
720 GO TO 740
730 LET V = -V
740 LET Y(I) = V
750 RETURN
760 PRINT"TO REVIEW THE INPUT DATA TYPE 1, NO REVIEW TYPE 0";
770 INPUT N1
780 IF N1 = 0 THEN 870
790 PRINT"COMPLEMENTARY  DATA IS CONVERTED TO NEGATIVE EQUIVALANCE."
800 PRINT
810 PRINT"#";TAB(4);"OBSERVABLE","REFERENCE"
820 FOR I = 1 TO N
830 PRINT I;TAB(4);A(I),B(I)
840 NEXT I
850 PRINT
860 PRINT
870 PRINT"TO CHANGE INPUT DATA TYPE 1, NO CHANGE TYPE 0";
880 INPUT R
890 IF R = 0 THEN 980
900 PRINT " ENTER THE NUMBER OF CHANGES TO BE MADE";
910 INPUT Q
920 FOR J = 1 TO Q
930 PRINT "ENTER THE PR. NO. TO BE CHANGED";
940 INPUT I
950 GOSUB 190
960 NEXT J
970 GO TO 760
980 LET T1 = T2 = T3 = T4 = 0
990 FOR I = 1 TO N
```

(2 of 3)

```
1000 LET T1 = T1 + X(I)
1010 LET T2 = T2 + Y(I)
1020 LET T3 = T3 + (X(I) - Y(I))
1030 LET T4 = T4 + X(I)↑2
1040 NEXT I
1050 LET E = T1/N - T2/N
1060 LET T6 = T7 = 0
1070 FOR I = 1 TON
1080 LET H(I) = Y(I) + E
1090 LET P(I) = X(I) - H (I)
1100 LET T6 = T6 + P(I)↑2
1110 LET T7 = T7 + P(I)
1120 NEXT I
1130 LET G = T6/N
1140 LET M = (T7/N)↑2
1150 IF W1 = 0 THEN 1330
1160 LET S = U1*SQR(G-M)
1170 PRINT
1180 PRINT
1190 PRINT
1200 PRINT
1220 PRINT TAB(12)"PSEUDO RANGE TABULATION"
1230 PRINT"#";TAB(4);"OBS","REF"
1240 PRINT TAB (4);"FT","FT"
1250 PRINT
1260 FOR I = 1 TO N
1270 PRINT I;TAB(4);U1*X(I),U1*Y(I)
1280 NEXT I
1290 PRINT
1300 PRINT "THERE ARE ";N;" SAMPLES"
1310 PRINT"STANDARD DEVIATION OF THE ERROR(FEET)= ";S
1320 GO TO 1440
1330 LET S =U2*SQR(G-M)
1340 PRINT TAB(14)"PSEUDO DOPPLER VELOCITY TABULATION"
1350 PRINT
1360 PRINT "#";TAB(4);"OBS","REF"
1370 PRINT TAB(4);"FT/SEC","FT/SEC"
1380 FOR I = 1 TO N
1390 PRINT I;TAB(4);U2*X(I),U2*Y(I)
1400 NEXT I
1410 PRINT
1420 PRINT "THERE ARE ";N;" SAMPLES"
1430 PRINT "STANDARD DEVIATION OF THE ERROR(FT/SEC) = ";S
1440 PRINT
1450 PRINT
1460 PRINT"TYPE 1 FOR MORE RUNS,TYPE 0 IF FINISHED";
1470 INPUT M1
1480 IF M1 = 1 THEN 40
1490 FOR I = 1 TO 5
1495 PRINT
1500 NEXT I
1510 END
READY
```

CHNL #1
PSEUDO RANGE
VELOCITY = 7000 fps

```
NACSTA     15:45      11/10/71

NRL STATISICAL PROGRAM TO COMPUTE STANDARD DEVIATIONS
OF PSEUDO-RANGE AND PSEUDO-DOPPLER FOR THE 621B RECEIVER

TYPE 1 FOR PSEUDO RANGE, TYPE 0 FOR PSEUDO DOPPLER?1

ENTER NO. OF SAMPLES?10
ENTER OBSERVABLE,REFERENCE OCTAL DATA
DO NOT ENTER MORE THAN 7 DIGITS  PER CHANNEL
PR.NO. 1 ?676,711
PR.NO. 2 ?521,522
PR.NO. 3 ?412,414
PR.NO. 4 ?15,34
PR.NO. 5 ?330,336
PR.NO. 6 ?510,532
PR.NO. 7 ?156,170
PR.NO. 8 ?624,635
PR.NO. 9 ?137,144
PR.NO. 10 ?317,316
TO REVIEW THE INPUT DATA TYPE 1, NO REVIEW TYPE 0?1
COMPLEMENTARY  DATA IS CONVERTED TO NEGATIVE EQUIVALANCE.

                    PSEUDO RANGE TABULATION
#  OBS           REF
   FT            FT

 1  174.219       178.516
 2  131.641       132.031
 3  103.906       104.687
 4  5.07812       10.9375
 5  84.375        86.7187
 6  128.125       135.156
 7  42.9687       46.875
 8  157.812       161.328
 9  37.1094       39.0625
10   80.8594      80.4687

THERE ARE  10  SAMPLES
STANDARD DEVIATION OF THE ERROR(FEET)=   2.27905
```

CHNL #1
PSEUDO RANGE
ACCELERATION = 175 ft/s²

```
ENTER NO. OF SAMPLES?7
ENTER OBSERVABLE,REFERENCE OCTAL DATA
DO NOT ENTER MORE THAN 7 DIGITS  PER CHANNEL
PR.NO. 1 ?534,632
PR.NO. 2 ?564,675
PR.NO. 3 ?400,471
PR.NO. 4 ?001,274
PR.NO. 5 ?562,665
PR.NO. 6 ?731,1003
PR.NO. 7 ?457,536
```

PSEUDO RANGE TABULATION

#	OBS FT	REF FT
1	135.937	160.156
2	145.312	173.828
3	100	122.266
4	50.3906	73.4375
5	144.531	170.703
6	184.766	201.172
7	118.359	136.719

THERE ARE 7 SAMPLES
STANDARD DEVIATION OF THE ERROR(FEET)= 3.90864

```
ENTER NO. OF SAMPLES?5
ENTER OBSERVABLE,REFERENCE OCTAL DATA
DO NOT ENTER MORE THAN 7 DIGITS  PER CHANNEL
PR.NO. 1 ?24,273
PR.NO. 2 ?2,245
PR.NO. 3 ?270,563
PR.NO. 4 ?216,504
PR.NO. 5 ?341,606
```

PSEUDO RANGE TABULATION

#	OBS FT	REF FT
1	7.8125	73.0469
2	.78125	64.4531
3	71.875	144.922
4	55.4687	126.562
5	87.8906	152.344

THERE ARE 5 SAMPLES
STANDARD DEVIATION OF THE ERROR(FEET)= 3.81455

$$\sigma_T = \sqrt{\frac{7 \times (3.91)^2 + 5 \times (3.81)^2}{12}} = 3.87 \text{ (for 12 samples)}$$

CHNL # 1
PSEUDO DOPPLER
VELOCITY = 7000 fps.

```
MACSTA      14:09      11/11/71

M.L. STATISICAL PROGRAM TO COMPUTE STANDARD DEVIATIONS
OF PSEUDO-RANGE AND PSEUDO-DOPPLER FOR THE 621B RECEIVER

TYPE 1 FOR PSEUDO RANGE, TYPE 0 FOR PSEUDO DOPPLER?0

ENTER NO. OF SAMPLES?10
ENTER OBSERVABLE,REFERENCE OCTAL DATA
DO NOT ENTER MORE THAN 7 DIGITS  PER CHANNEL
PR.NO. 1 ?3,3
PR.NO. 2 ?7,12
PR.NO. 3 ?0,3
PR.NO. 4 ?4,3
PR.NO. 5 ?6,3
PR.NO. 6 ?11,3
PR.NO. 7 ?3,3
PR.NO. 8 ?3,3
PR.NO. 9 ?4,3
PR.NO. 10 ?12,3
TO REVIEW THE INPUT DATA TYPE 1, NO REVIEW TYPE 0?0
TO CHANGE INPUT DATA TYPE 1, NO CHANGE TYPE 0?0
                 PSEUDO DOPPLER VELOCITY TABULATION

#  OBS          REF
   FT/SEC       FT/SEC
 1  .14881       .14881
 2  .347222      .496032
 3  0            .14881
 4  .198413      .14881
 5  .2976190     .14881
 6  .446429      .14881
 7  .14881       .14881
 8  .14881       .14881
 9  .198413      .14881
 10  .496032     .14881

THERE ARE  10  SAMPLES
STANDARD DEVIATION OF THE ERROR(FT/SEC) =  .156545
```

CHISL #1
PSEUDO DOPPLER
ACCELERATION = 1.75 fps²

```
TYPE 1 FOR MORE RUNS,TYPE 0 IF FINISHED?1
TYPE 1 FOR PSEUDO RANGE, TYPE 0 FOR PSEUDO DOPPLER?0

ENTER NO. OF SAMPLES?6
ENTER OBSERVABLE,REFERENCE OCTAL DATA
DO NOT ENTER MORE THAN 7 DIGITS  PER CHANNEL
PR.NO. 1 ?41,42
PR.NO. 2 ?5,11
PR.NO. 3 ?13,2
PR.NO. 4 ?26,24
PR.NO. 5 ?25,31
PR.NO. 6 ?25,34
TO REVIEW THE INPUT DATA TYPE 1, NO REVIEW TYPE 0?0
TO CHANGE INPUT DATA TYPE 1, NO CHANGE TYPE 0?0
              PSEUDO DOPPLER VELOCITY TABULATION

#  OBS          REF
   FT/SEC       FT/SEC
 1  1.6369       1.68651
 2  .248016      .446429
 3  .545635     9.92063E-2
 4  1.09127      .992063
 5  1.04167      1.24008
 6  1.04167      1.38889

THERE ARE  6  SAMPLES
STANDARD DEVIATION OF THE ERROR(FT/SEC) =  .258408
```

CHNL # 2
PSEUDO RANGE
VELOCITY = 7000 fps.

MAGSTA 14:48 11/11/71

MRL STATISICAL PROGRAM TO COMPUTE STANDARD DEVIATIONS
OF PSEUDO-RANGE AND PSEUDO-DOPPLER FOR THE 621B RECEIVER

TYPE 1 FOR PSEUDO RANGE, TYPE 0 FOR PSEUDO DOPPLER

ENTER NO. OF SAMPLES?10
ENTER OBSERVABLE,REFERENCE OCTAL DATA
DO NOT ENTER MORE THAN 7 DIGITS PER CHANNEL
PR.NO. 1 ?34,33
PR.NO. 2 ?51,47
PR.NO. 3 ?47,51
PR.NO. 4 ?7,17
PR.NO. 5 ?56,55
PR.NO. 6 ?24,23
PR.NO. 7 ?5,5
PR.NO. 8 ?57,63
PR.NO. 9 ?2,5
PR.NO. 10 ?40,24
TO REVIEW THE INPUT DATA TYPE 1, NO REVIEW TYPE 0?0
TO CHANGE INPUT DATA TYPE 1, NO CHANGE TYPE 0?0

PSEUDO RANGE TABULATION

#	OBS FT	REF FT
1	10.9375	10.5469
2	16.0156	15.2344
3	15.2344	16.0156
4	2.73437	5.85937
5	17.9687	17.5781
6	7.8125	7.42187
7	1.95312	1.95312
8	18.3594	19.9219
9	.78125	1.95312
10	12.5	7.8125

THERE ARE 10 SAMPLES
STANDARD DEVIATION OF THE ERROR(FEET)= 1.92955

CHNL # 2
PSEUDO RANGE
ACCELERATION = 175 fps²

```
                                        1
TYPE 1 FOR PSEUDO RANGE, TYPE 0 FOR PSEUDO DOPPLER?1

ENTER NO. OF SAMPLES?5
ENTER OBSERVABLE,REFERENCE OCTAL DATA
DO NOT ENTER MORE THAN 7 DIGITS  PER CHANNEL
PR.NO. 1 ?135,504
PR.NO. 2 ?662,1231
PR.NO. 3 ?335,700
PR.NO. 4 ?305,654
PR.NO. 5 ?247,616
TO REVIEW THE INPUT DATA TYPE 1, NO REVIEW TYPE 0?0
TO CHANGE INPUT DATA TYPE 1, NO CHANGE TYPE 0?0


                      PSEUDO RANGE TABULATION
#   OBS            REF
    FT             FT

 1   36.3281        126.562
 2  169.531         259.766
 3   86.3281        175
 4   76.9531        167.187
 5   65.2344        155.469

THERE ARE  5  SAMPLES
STANDARD DEVIATION OF THE ERROR(FEET)=  .625
```

CHNL #2
PSEUDO DOPPLER
VELOCITY = 7000 fps.

0

```
ENTER NO. OF SAMPLES?10
ENTER OBSERVABLE,REFERENCE OCTAL DATA
DO NOT ENTER MORE THAN 7 DIGITS  PER CHANNEL
PR.NO. 1 ?2,3
PR.NO. 2 ?3,3
PR.NO. 3 ?7,13
PR.NO. 4 ?4,3
PR.NO. 5 ?3,3
PR.NO. 6 ?13,3
PR.NO. 7 ?1,3
PR.NO. 8 ?0,3
PR.NO. 9 ?7,13
PR.NO. 10 ?6,3
TO REVIEW THE INPUT DATA TYPE 1, NO REVIEW TYPE 0?0
TO CHANGE INPUT DATA TYPE 1, NO CHANGE TYPE 0?0
               PSEUDO DOPPLER VELOCITY TABULATION

#   OBS            REF
    FT/SEC         FT/SEC
 1  9.92063E-2     .14881
 2  .14881         .14881
 3  .347222        .545635
 4  .198413        .14881
 5  .14881         .14881
 6  .545635        .14881
 7  4.96032E-2     .14881
 8  0              .14881
 9  .347222        .545635
 10  .297619       .14881

THERE ARE  10  SAMPLES
STANDARD DEVIATION OF THE ERROR(FT/SEC) =  .171544
```

CHNL #2
PSEUDO DOPPLER
ACCELERATION = 175 fps^2

```
TYPE 1 FOR MORE RUNS, TYPE 0 IF FINISHED?1
TYPE 1 FOR PSEUDO RANGE, TYPE 0 FOR PSEUDO DOPPLER?0


ENTER NO. OF SAMPLES?5
ENTER OBSERVABLE,REFERENCE OCTAL DATA
DO NOT ENTER MORE THAN 7 DIGITS  PER CHANNEL
PR.NO. 1 ?270,302
PR.NO. 2 ?11,5
PR.NO. 3 ?45,50
PR.NO. 4 ?23,25
PR.NO. 5 ?75,75
TO REVIEW THE INPUT DATA TYPE 1, NO REVIEW TYPE 0?0
TO CHANGE INPUT DATA TYPE 1, NO CHANGE TYPE 0?0
             PSEUDO DOPPLER VELOCITY TABULATION

#  OBS          REF
   FT/SEC       FT/SEC
 1  9.12698      9.62302
 2  .446429      .248016
 3  1.83532      1.98413
 4  .94246       1.04167
 5  3.02579      3.02579

THERE ARE  5  SAMPLES
STANDARD DEVIATION OF THE ERROR(FT/SEC) =   .227094
```

CHNL # 3
PSEUDO RANGE
VELOCITY = 7000 fps.

MAGSTA 16:03 11/10/71

MIL STATISICAL PROGRAM TO COMPUTE STANDARD DEVIATIONS
OF PSEUDO-RANGE AND PSEUDO-DOPPLER FOR THE 621B RECEIVER

TYPE 1 FOR PSEUDO RANGE, TYPE 0 FOR PSEUDO DOPPLER?1

ENTER NO. OF SAMPLES?10
ENTER OBSERVABLE,REFERENCE OCTAL DATA
DO NOT ENTER MORE THAN 7 DIGITS PER CHANNEL
PR.NO. 1 ?641,645
PR.NO. 2 ?423,424
PR.NO. 3 ?225,227
PR.NO. 4 ?673,663
PR.NO. 5 ?206,204
PR.NO. 6 ?232,256
PR.NO. 7 ?156,164
PR.NO. 8 ?740,731
PR.NO. 9 ?632,641
PR.NO. 10 ?234,235
TO REVIEW THE INPUT DATA TYPE 1, NO REVIEW TYPE 0?1
COMPLEMENTARY DATA IS CONVERTED TO NEGATIVE EQUIVALANCE.

PSEUDO RANGE TABULATION

#	OBS FT	REF FT
1	162.891	164.453
2	107.422	107.812
3	58.2031	58.9844
4	173.047	169.922
5	52.3437	51.5625
6	60.1562	67.9687
7	42.9687	45.3125
8	187.5	184.766
9	160.156	162.891
10	60.9375	61.3281

THERE ARE 10 SAMPLES
STANDARD DEVIATION OF THE ERROR(FEET)= 2.93983

CHNL # 3
PSEUDO RANGE
ACCELERATION = 175 fps²


```
PR.NO. 1 ?530,626
PR.NO. 2 ?14,66
PR.NO. 3 ?66,165
PR.NO. 4 ?262,351
PR.NO. 5 ?752,1047
TO REVIEW THE INPUT DATA TYPE 1, NO REVIEW TYPE 0?0
TO CHANGE INPUT DATA TYPE 1, NO CHANGE TYPE 0?0
```

PSEUDO RANGE TABULATION

#	OBS FT	REF FT
1	134.375	158.594
2	4.6875	21.0937
3	21.0937	45.7031
4	69.5312	91.0156
5	191.406	215.234

THERE ARE 5 SAMPLES
STANDARD DEVIATION OF THE ERROR(FEET)= 3.05188

```
PR.NO. 1 ?366,456
PR.NO. 2 ?617,700
PR.NO. 3 ?345,444   → 354
PR.NO. 4 ?315,373
PR.NO. 5 ?048,120
PR.NO. 6 ?371,422
PR.NO. 7 ?334,401
PR.NO. 8 ?343,424
PR.NO. 9 ?332,371
PR.NO. 10 ?471,601
PR.NO. 11 ?315,411
```

PSEUDO RANGE TABULATION

#	OBS FT	REF FT
1	96.0937	117.969
2	155.859	175
3	92.1875	114.062
4	80.0781	98.0469
5	13.2812	31.25
6	97.2656	107.031
7	85.9375	100.391
8	88.6719	107.812
9	85.1562	97.2656
10	122.266	150.391
11	80.0781	103.516

THERE ARE 11 SAMPLES
STANDARD DEVIATION OF THE ERROR(FEET)= 4.9926

σ_T = PRINT SQR((11*4.99↑2+5*3.05↑2)/16)
4.47503 feet (for 16 samples)
READY

CHNL # 3
PSEUDO DOPPLER
VELOCITY = 7000 fps

NAGSTA 19:20 11/10/71

NRL STATISICAL PROGRAM TO COMPUTE STANDARD DEVIATIONS
OF PSEUDO-RANGE AND PSEUDO-DOPPLER FOR THE 621B RECEIVER

TYPE 1 FOR PSEUDO RANGE, TYPE 0 FOR PSEUDO DOPPLER?0

ENTER NO. OF SAMPLES?16
ENTER OBSERVABLE,REFERENCE OCTAL DATA
DO NOT ENTER MORE THAN 7 DIGITS PER CHANNEL
PR.NO. 1 ?40,31
PR.NO. 2 ?30,31
PR.NO. 3 ?35,32
PR.NO. 4 ?44,31
PR.NO. 5 ?36,31
PR.NO. 6 ?27,31
PR.NO. 7 ?53,32
PR.NO. 8 ?5,31
PR.NO. 9 ?21,31
PR.NO. 10 ?31,31
PR.NO. 11 ?34,31
PR.NO. 12 ?36,31
PR.NO. 13 ?21,32
PR.NO. 14 ?17,32
PR.NO. 15 ?34,31
PR.NO. 16 ?37,31
TO REVIEW THE INPUT DATA TYPE 1, NO REVIEW TYPE 0?0
TO CHANGE INPUT DATA TYPE 1, NO CHANGE TYPE 0?0

PSEUDO DOPPLER VELOCITY TABULATION

#	OBS FT/SEC	REF FT/SEC
1	1.5873	1.24008
2	1.19048	1.24008
3	1.43849	1.28968
4	1.78571	1.24008
5	1.4881	1.24008
6	1.14087	1.24008
7	2.13294	1.28968
8	.248016	1.24008
9	.843254	1.24008
10	1.24008	1.24008
11	1.38889	1.24008
12	1.4881	1.24008
13	.843254	1.28968
14	.744048	1.28968
15	1.38889	1.24008
16	1.5377	1.24008

THERE ARE 16 SAMPLES
STANDARD DEVIATION OF THE ERROR(FT/SEC) = .436314

CHNL # 3
PSEUDO DOPPLER
ACCELERATION = 175 fps²

```
TYPE 1 FOR MORE RUNS,TYPE 0 IF FINISHED?1
TYPE 1 FOR PSEUDO RANGE, TYPE 0 FOR PSEUDO DOPPLER?0

ENTER NO. OF SAMPLES?8
ENTER OBSERVABLE,REFERENCE OCTAL DATA
DO NOT ENTER MORE THAN 7 DIGITS  PER CHANNEL
PR.NO. 1 ?52,52
PR.NO. 2 ?53,41
PR.NO. 3 ?52,46
PR.NO. 4 ?63,52
PR.NO. 5 ?12,16
PR.NO. 6 ?46,40
PR.NO. 7 ?47,33
PR.NO. 8 ?33,36
TO REVIEW THE INPUT DATA TYPE 1, NO REVIEW TYPE 0?0
TO CHANGE INPUT DATA TYPE 1, NO CHANGE TYPE 0?0
                PSEUDO DOPPLER VELOCITY TABULATION

 #   OBS          REF
     FT/SEC       FT/SEC
 1   2.08333       2.08333
 2   2.13294       2.43056
 3   2.08333       1.88492
 4   2.52976       2.08333
 5   .496032       .694444
 6   1.38492       1.5873
 7   1.93452       1.33929
 8   1.33929       1.4881

THERE ARE  8  SAMPLES
STANDARD DEVIATION OF THE ERROR(FT/SEC) =   .302488
```

CHNL # 4
PSEUDO RANGE
VELOCITY = 7000 fps.

```
TYPE 1 FOR MORE RUNS, TYPE 0 IF FINISHED?1
TYPE 1 FOR PSEUDO RANGE, TYPE 0 FOR PSEUDO DOPPLER

ENTER NO. OF SAMPLES?10
ENTER OBSERVABLE,REFERENCE OCTAL DATA
DO NOT ENTER MORE THAN 7 DIGITS  PER CHANNEL
PR.NO. 1 ?15,20
PR.NO. 2 ?0,2
PR.NO. 3 ?10,24
PR.NO. 4 ?57,72
PR.NO. 5 ?13,30
PR.NO. 6 ?24,32
PR.NO. 7 ?706,671
PR.NO. 8 ?276,314
PR.NO. 9 ?36,47
PR.NO. 10 ?34,55
TO REVIEW THE INPUT DATA TYPE 1, NO REVIEW TYPE 0?0
TO CHANGE INPUT DATA TYPE 1, NO CHANGE TYPE 0?0
```

PSEUDO RANGE TABULATION

#	OBS FT	REF FT
1	5.07812	6.25
2	0	.78125
3	3.125	7.8125
4	18.3594	22.6562
5	4.29687	9.375
6	7.8125	10.1562
7	177.344	172.266
8	74.2187	79.6875
9	11.7187	15.2344
10	10.9375	17.5781

THERE ARE 10 SAMPLES
STANDARD DEVIATION OF THE ERROR(FEET)= 3.19836

CHNL # 4
PSEUDO RANGE
ACCELERATION = 175 fps²

```
TYPE 1 FOR MORE RUNS, TYPE 0 IF FINISHED?1
TYPE 1 FOR PSEUDO RANGE, TYPE 0 FOR PSEUDO DOPPLER.

ENTER NO. OF SAMPLES?10
ENTER OBSERVABLE, REFERENCE OCTAL DATA
DO NOT ENTER MORE THAN 7 DIGITS PER CHANNEL
PR.NO. 1 ?252,71
PR.NO. 2 ?7,17
PR.NO. 3 ?2772,3000
PR.NO. 4 ?15,36
PR.NO. 5 ?36,60
PR.NO. 6 ?3,3
PR.NO. 7 ?22,42
PR.NO. 8 ?6,13
PR.NO. 9 ?3,5
PR.NO. 10 ?671,700
TO REVIEW THE INPUT DATA TYPE 1, NO REVIEW TYPE 0?0
TO CHANGE INPUT DATA TYPE 1, NO CHANGE TYPE 0?0
```

PSEUDO RANGE TABULATION

#	OBS FT	REF FT
1	16.4062	22.2656
2	2.73437	5.85937
3	597.656	600
4	5.07812	11.7187
5	11.7187	18.75
6	1.17187	1.95312
7	7.03125	13.2812
8	2.34375	4.29687
9	1.17187	1.95312
10	173.266	175

THERE ARE 10 SAMPLES
STANDARD DEVIATION OF THE ERROR(FEET)= 2.32545

CHNL # 4
PSEUDO DOPPLER
VELOCITY = 7000 fps

```
TYPE 1 FOR MORE RUNS,TYPE 0 IF FINISHED?1
TYPE 1 FOR PSEUDO RANGE, TYPE 0 FOR PSEUDO DOPPLER?0

ENTER NO. OF SAMPLES?10
ENTER OBSERVABLE,REFERENCE OCTAL DATA
DO NOT ENTER MORE THAN 7 DIGITS  PER CHANNEL
PR.NO. 1 ?3,13
PR.NO. 2 ?10,3
PR.NO. 3 ?7,3
PR.NO. 4 ?4,13
PR.NO. 5 ?1,3
PR.NO. 6 ?3,3
PR.NO. 7 ?3,3
PR.NO. 8 ?5,13
PR.NO. 9 ?13,3
PR.NO. 10 ?5,3
TO REVIEW THE INPUT DATA TYPE 1, NO REVIEW TYPE 0?0
TO CHANGE INPUT DATA TYPE 1, NO CHANGE TYPE 0?0
                 PSEUDO DOPPLER VELOCITY TABULATION
```

#	OBS FT/SEC	REF FT/SEC
1	.14881	.545635
2	.396825	.14881
3	.347222	.14881
4	.198413	.545635
5	4.96032E-2	.14881
6	.14881	.14881
7	.14881	.14881
8	.248016	.545635
9	.545635	.14881
10	.248016	.14881

```
THERE ARE  10  SAMPLES
STANDARD DEVIATION OF THE ERROR(FT/SEC) =  .253122
```

CHUL # 4
PSEUDO DOPPLER
ACCELERATION = 175 fps²

```
TYPE 1 FOR MORE RUNS, TYPE 0 IF FINISHED?1
TYPE 1 FOR PSEUDO RANGE, TYPE 0 FOR PSEUDO DOPPLER?0


ENTER NO. OF SAMPLES?7
ENTER OBSERVABLE,REFERENCE OCTAL DATA
DO NOT ENTER MORE THAN 7 DIGITS  PER CHANNEL
PR.NO. 1 ?3,2
PR.NO. 2 ?15,22
PR.NO. 3 ?32,27
PR.NO. 4 ?60,55
PR.NO. 5 ?7,3
PR.NO. 6 ?3,2
PR.NO. 7 ?46,51
TO REVIEW THE INPUT DATA TYPE 1, NO REVIEW TYPE 0?0
TO CHANGE INPUT DATA TYPE 1, NO CHANGE TYPE 0?0
                PSEUDO DOPPLER VELOCITY TABULATION

#   OBS          REF
    FT/SEC       FT/SEC
 1  .14881        9.92063E-2
 2  .644841       .892857
 3  1.28968       1.14087
 4  2.38095       2.23214
 5  .347222       .14881
 6  .14881        9.92063E-2
 7  1.88492       2.03373

THERE ARE  7  SAMPLES
STANDARD DEVIATION OF THE ERROR(FT/SEC) =  .154277
```

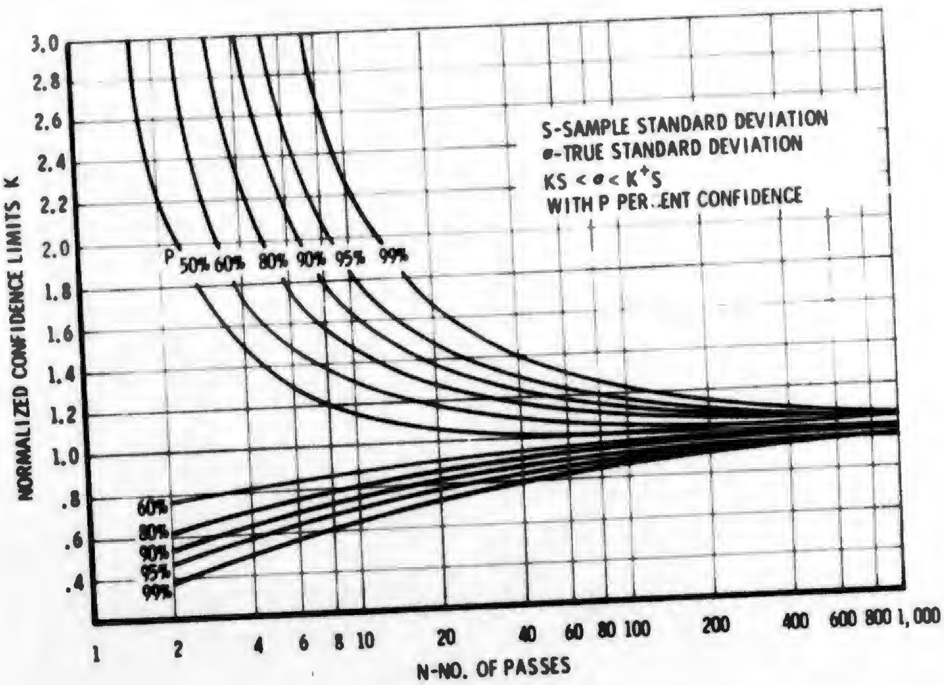

Figure 63. Standard Deviation Computation Confidence

APPENDIX E

RESULTS OF COMPATIBILITY TESTS BETWEEN 621B RECEIVER (MAGNAVOX) AND TRANSMITTER (HAZELTINE)

E.1 COMPENDIUM OF EVENTS

a. Ray Halen of GAC delivered the Hazeltine transmitter and witnessed the unpacking at 10:30 AM on 27 Octobrr 1971.

b. Jim Woolard of Hazeltine arrived at MRL about 1:30 P.M.

c. Xmtr. equipment was set up in a screen room at approximately 2:30 P.M.

d. At 3:00 P.M, the Hazeltine Xmtr and Magnavox Rcvr. were interfaced.

e. Upon application of the transmitter signal, all four of the receiver channels locked within 5 seconds.

f. An external lab power supply was substituted for the internal power supply of the transmitter at 9:00 A.M. on 28 October 1971.

g. Compatibility between the 4 Hazeltine codes and the 4 MRL codes was verified about 9:30 A.M.

h. The Hazeltine Xmtr. was repacked at 10:30 A.M.

i. Jim Wollard departed MRL at 11:00 A.M.

E.2 INTERFACE TEST RESULTS

a. Xmtr level referred to the Rcvr input was set to -123 dBm during long code and -100 dBm during the short code interval (power boost).

b. Hazeltine Code D and MRL Code No. 4 was used initially.

c. After acquisition had been established and during a track mode, the Q channel of processor No. 3 indicated the presence of incidental phase modulation on the transmit signal. The PM occurred at a rate of 120 Hz (synchronous to line) and with a deviation of approximately 20^{o} peak.

d. Initial acquisition performance indicated the following probability of detection for a given received power boost signal level:

$P_D \geq 0.8$ @ -102 dBm

$P_D \geq 0.5$ @ -103 dBm

e. Reacquisition performance was as follows:

$P_D \geq 0.9$ @ -126 dBm

$P_D \geq 0.5$ @ -127 dBm

f. A check for receiver track holdon performance indicated

4 channels remained locked @ -143 dBm
1 channel remained locked @ -146 dBm

g. An external lab. power supply (Lambda, Model LK-341A) was substituted for the internal supply of the Hazeltine Xmtr. As a result, the 120 Hz PM component in the transmit signal was substantially reduced.

h. Compatibility between the 4 Hazeltine codes and the 4 MRL codes was verified. Figure 1 shows the test setup for interfacing the xmtr and rcvr.

E.3 CONCLUSIONS

In general the Hazeltine transmitter and Magnavox receiver are compatible. Each of the four PN codes match. The power boost signal level appears to be 23 dB above the normal transmit signal level. The 120 Hz incidental PN component at the output of the Hazeltine transmitter using the internal power supply degrades the track performance of the MRL receiver about 2 dB. Experiments with an external supply indicate that, if a battery is "floated" across the output of the transmitter power supply to smooth the 120 Hz ripple during the flight tests, the tracking performance of the receiver will be degraded less than 1 dB.

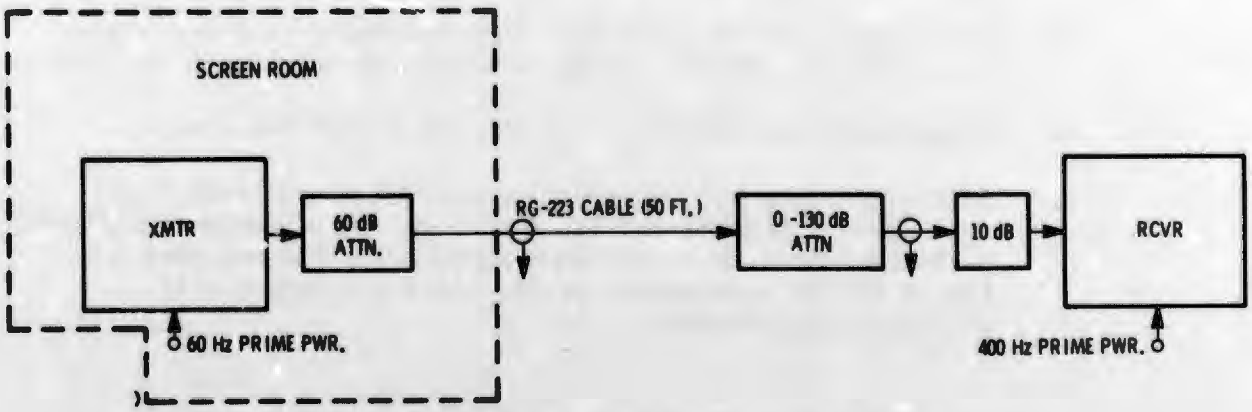

Figure 64. Transmitter/Receiver Test Setup

APPENDIX F

TRIP REPORTS

REPORT NO. 2612 **TRIP REPORT FORM** DATE 6 March 72

PLACE VISITED Holloman AFB, Alamorgordo, N.M. DATE 23 March 72

PURPOSE OF VISIT Field Support 621B Program

CUSTOMER PERSONNEL:	MAGNAVOX PERSONNEL
Ralph Laho	M. Taylor
Capt. Cecil Rose	
Ed Graber	

SUMMARY:

6 March 72

On site for preflight activities. Equipment installed and functionally tested.

7 March 72

PREFLIGHT NO. 1

621B/MX-450 functional. Test tapes made and the dump looks good. This being the first actual flight all seems to be going well.

INFLIGHT NO. 1

The inflight activities appeared to have gone smoothly. The equipment operators apparently have a reasonable understanding of how to operate the 621B equipments. The MRL receiver acquired the four transmitters and the power vs AGC profiles look encouraging Flight No. 1 looks very good.

POST FLIGHT NO. 1

It was later learned that two of the airborne data recorders did not function properly. No data was recorded from either of the airborne receivers.

FOLLOW UP ACTION REQUIRED

COGNIZANT FIELD SALES PERSON

REPORTED BY: Mel Taylor

cc: MRL Personnel Above
R. Cnossen
F. Charles
W. Trappen

MRL 62422A

16 March 72

Made initial checkout of the MX-450 system, all OK. Flight No. 2 departed on schedule, but the flight was aborted due to a fuel leak in the right wing.

21 March 72

FLIGHT NO. 2A

Preflight OK with master controller board. Inflight operations were no good, system would not acquire codes signal. The before mentioned Master Controller Board had been modified to inhibit the sync power boost signal during the calibrate cycle.

Post flight self test cycle was good, but the system would not acquire a coded signal. Replaced the modified master controller board with an unmodified board, and the system worked properly and would acquire the coded signal being transmitted.

After my return from WSMR I made a complete system checkout, and all did appear normal. I did notice that the MX-450 system had been turned on, but that in itself should pose no problems as long as external cooling is provided.

I talked to Capt. Bybee regarding the data tape recorder, and was advised that it had retested good and the probable cause of the sync word error was due to the position of the slope detector on the recorder itself. It appears the preflight tapes cut prior to Flight No. 1 were cut using plus and minus detection so it was assumed at that point it made no difference and the slope detector was placed in the positive position.

As Flight No. 1 progressed, the tolerance levels built up, the system (recording) could no longer detect the sync word.

16 March 1972

0530 - Preflight power on allowed five minute warmup, initial calibrate good and tracking "A" OK. Allowed 25 minute additional warmup at the same time going through various steps; system check OK.

0730 - Self cal OK system needed a little more warmup time.

I rebriefed the operator regarding basic operations and cal procedures.

Aircraft airborne 0850. We arrived on the range site and were advised that the flight had been aborted at 0813 due to a fuel leak in the right wing. Aircraft diverted to Kirtland. All equipments on board. Aircraft 0371 is scheduled to return to Holloman AFB Monday 20 March 1972.

20 March 72

Aircraft returned to Holloman today. Reinstalled control box, made system check, check OK. Changed master controller board, repeated checks, all checks good.

21 March 72

0530 - Preflight check begins. System check after five minute warmup OK. Made complete system check; all appears normal and correct at this point.

Aircraft departed on schedule, at this point I departed shop area enroute to MCS.

Prior to the flight I asked the project officer if a test tape had been made on the MRL tape recorder. The answer was affirmative.

INFLIGHT

1100 - First run begins. MRL would not calibrate recalibrate good. Hazeltine channel 1, 2, 3 and 4 OK prior to the first pass. MRL in "stby". Good signal indication, but no lock. Recalibrated. MRL calibrate cycle good, still no lock.

1900 Z 21 March 72

Aircraft 0371 departed range enroute to Holloman AFB. It was learned during the debrief both the MRL and Hazeltine data recorders were inoperative.

Post flight systems check did not reveal the system malfunction. Made a check of the signal splitter on the aircraft, appears normal and correct. Since all appeared normal to me at the time, I made a phone call to MRL. Contacted project personnel, talked the problem over. It was agreed the probable cause of the problem was in the Master Controller Board which had been modified to negate the signal power boost during the calibrate mode.

Replaced the Master Controller Board with an unmodified board, and the necessary switch from "Stby" to "ACQ" occurs with detected signal. On the suggestion of MRL project personnel, I down loaded the MX-450 system to run a confidence check on the equipment.

22 March 72

Some solutions are being obtained from the data sent to New York on Flight No. 1, Pass No. 4. I confirmed channel 1, 2, 3 and 4 are coded correctly and the data should be sequenced into the recorder when and where expected.

REPORT NO 2613 **TRIP REPORT FORM** DATE 26 March 72

PLACE VISITED Holloman AFB, Alamorgordo, N.M. DATE 29 March 72

PURPOSE OF VISIT Field Support 621B Program

CUSTOMER PERSONNEL:	MAGNAVOX PERSONNEL
Grumman Aero	M. Taylor
Hazeltine Aero	J. Kruse

SUMMARY:

Departed LAX 1945 the 26th of March. Arrived Alamorgordo N.M. on site 0730 27 March 72. Preflight OK for Flight No. 3.

MX-450 system performed well for flight, but tape recorders for Magnavox and Hazeltine did not function properly.

Magnavox tape recorder "GFE" functioning OK after third pass of Flight No. 3.

USAF indicates no more flight "on the range" until data recorders are functioning properly.

Jim Kruse and I trouble shot the recently modified Master Controller Board and a wire was found to have been misplaced. Correction was made and the board retested good.

We were unable to obtain a coded signal from a transmitter at this time, so just to be on the safe side we decided not to fly the modified board.

After making as many bench tests as possible, and satisfying ourselves that the equipment was performing properly we decided to install the system in the aircraft.

FOLLOW UP ACTION REQUIRED

COGNIZANT FIELD SALES PERSON

REPORTED BY

cc MRL Personnel Above
R. Cnossen
F. Charles
W. Trappen

MRL 62422A

28 March 72

0060 preflight system test good.

Capt. Bybee cut a test tape on the MRL recorder and the first displays were bad. A second tape was cut and it checked out OK. A third tape was cut and it didn't check properly using the C.R. display. Hazeltines tapes all checked out OK. The MRL tapes were taken to the computer building and a printout of the previous tapes were made. Two of the three tapes were good. It's unknown at this point why number one tape didn't come out OK.

At 1 plus 15 prior to flight it was learned that the signal processor at the MCS was inoperative, and thought was given to removing the Hazeltine Signal Processor from the aircraft and flying with the MRL 621B system. The signal processor used in the ACFT is interchangeable with the one in the MCS station.

The test bed aircraft made its initial pass over the sites at 0909 hours. The initial pass appeared normal and little or no information was received from the UHF link. During the second pass, it was noticed that the recorders were inoperative. The power was recycled and the record circuit breakers were reset. The HAZ recorder remained off the line but, the MRL recorder appears to be working properly. Twelve passes were made. Both receivers appeared to work.

During the 12th and final pass of Flight No. 3 the power from the site transmitters was reduced 3 dB, and than an additional 5 dB. The power reductions should be apparent in AGC levels when the tapes are made available.

The aircraft returned to the base at 1110 and I was on board at 1118. I rechecked the MRL system and it went through all the steps as programmed. Capt. Bybee met the aircraft and confirmed that the HAZ recorder was still inoperative. Since the MRL and HAZ recorders malfunctioned at or near the same time it's assumed at this point that something common to both systems must have caused a power transient and the HAZ recorder got the worst of it.

The USAF is very concerned about the recorder situation, and has implied that another range flight should not be scheduled until they are sure the GFE airborne recorders will work in flight.

There are flight schedules for the 4, 5 and 7th of April.

REPORT NO 2635 | TRIP REPORT FORM | DATE 30 May 72

PLACE VISITED Holloman AFB, New Mexico | DATE

PURPOSE OF VISIT Field Support Flight Test 621B

CUSTOMER PERSONNEL:	MAGNAVOX PERSONNEL
Ralph Laho, GAC	F. Charles
Capt. C. Rose USAF	J. Kruse
	M. Taylor

SUMMARY:

(1) 7 April 1972 Flight No. 5 Good flight.

(2) 11 April Channel 2 will not acquire. Others OK. Problem disappeared, not defined.

(3) 12 April Flight No. 6 MRL OK. No data recorder for HAZ.

(4) 13 April attended TDM F. Charles, J. Kruse others.

(5) 15 April shipped MX-450 to MRL for calibration.

(6) 17 through 24 April MX-450 repaired, calibrated shipped to HAFB.

FOLLOW UP ACTION REQUIRED

COGNIZANT FIELD SALES PERSON

REPORTED BY Mel Taylor

cc MRL Personnel Above
F. Charles
W. Trappen
R. Cnossen

MRL 62422A

7 April 1972 Flight No. 5

Flight No. 5 appeared to be a normal flight, nothing unusual occurred. GAC did some adjusting of the up link power levels down. For the most part we had a good flight.

11 April 72

Preflight, channel No. 2 will not track. Channels 1, 3 and 4 appear normal on the test set panel. The indications were:

(1) Standby

(2) Search

(3) Phase lock loop

(4) Track for a short period and back to standby and a repeat of the above steps.

Advised J. Kruse of problem. The problem was traced to P.C. Receiver No. 1.

Power on, problem in Channel No. 2 would not duplicate. The conditions I had experienced earlier could be forced to reoccur if moisture was applied to P.C. Rx Board No. 1.

It appears at this point, the board being one, with High Z circuits, we may have had a leakage problem due to dirt and metal contaminates which may have come from an unfiltered air conditioning unit in the aircraft. The system appears OK as is, some minor adjustments made to P.C. Rx No. 1.

12 April 72 Flight No. 6

Both airborne receivers ready for the flight, but the LTN 51 airborne recorder malfunctioned and at this point the LTN 51 system is an abort item.

14 April 72

Applied power to MX-450 system after removal from aircraft. What do you know, same problem as before.

15 April 1972

Packed and shipped MX-450 system to MRL.

17 April 72

MX-450 system set up in the lab. Cause of major failure was secondary and suspected cause was a voltage transient which shorted a chip on FFS No. 1. This could have been determined in the field, but the spare board was defective, which leads me to other areas of the system.

18 April 72

MX-450 repaired and functionally good. P.C. Receiver Boards No. 1 were cleaned, coated and cured. System on for long term reliability run.

24 April 72

I made a functional check of the system prior to disassembly and packing for shipment to Holloman AFB, New Mexico.

Actions taken while MX-450 was at MRL:

(1) Evaluate system problem
(2) Trouble shoot
(3) Repaired
(4) Calibrate, confirmed Cal sign - 123 dBm $\pm$ 1 dBm
(5) Run in
(6) Shipped to Holloman AFB

15 May 72

Flight No. 13 49206 "A"

Good MRL flight, no problems.

17 May 72

Flight No. 14 49203 GJ

Gen. Morgan on site. MRL equipment preflight, inflight and post flight good.

19 May 72

Flight No. 15

0600 preflight equipment working good.

Program Status as of 18 May 72

(1) 30.8 hours on aircraft - conserve aircraft hours for 621B

(2) Aircraft does not go into phase maintenance unless:

(a) It is retained by AFSWC past 621B test

(3) Fly Friday 19th - we did "A" OK.

(4) Stand down two weeks through 2 June 72.

(5) Review rules if there is a change in aircraft availability, if data problem is not resolved at the end of stand down then fly area nav until it is resolved.

When; if resolved and aircraft is available move to ILS ASAP

if resolved and insuffici nt time (2 weeks to move) then continue area nav.

if bias problem is fixed before stand down is over and data is good then the x-ray mission scheduled and move to ILS ASAP.

if bias problem is fixed and prior data is not usable then continue area nav.

REPORT NO 2636 **TRIP REPORT FORM** **DATE** 30 May 72

PLACE VISITED Holloman AFB, New Mexico **DATE** 25 April/25 May

PURPOSE OF VISIT Field Support 621B Program

CUSTOMER PERSONNEL:	MAGNAVOX PERSONNEL
R. Laho	J. Kruse
Capt. Rose	M. Taylor
Capt. Bybee	

SUMMARY:

(1) Functional test after shipment from MRL.

(2) Flight No. 8 through 15 OK for MRL.

(3) F. Charles and B. Glazer on site for TDM.

(4) Aircraft on stand down status until 2 June. Equipment removed from airborne installation.

FOLLOW UP ACTION REQUIRED

F. Charles
W. Trappen
R. Cnossen

COGNIZANT FIELD SALES PERSON

REPORTED BY: Mel Taylor

cc: MRL Personnel Above

MRL 62422A

25 April 72

Equipment ready for installation.

26 April 72

0700 Back on Site. Installed equipment in aircraft. Preflight OK.

Flight No. 8 49202a smooth - no problems.

1 May 72

Flight No. 9 preflight good - no problems. Run one started, all four channels locked. No problems were experienced with MX-450 during flight. EU cal should be -123 $\pm$ 1 dBm.

	Channel 1	Channel 2	Channel 3	Channel 4
Cal	-118.9	-120.1	-119.1	-119.7
Initial Track	-118.9	-124.0	-119.1	-116.0

2 May 72

Checked system, all appears normal. The AGC readings appeared normal and stable.

Ran long term burn test on MX-450. The AGC levels appear normal in all respects.

4 May 72 49204AB

Flight No. 10 was good as far as MRL equipment was concerned. However, channel No. 1 is slow to acquire what GAC believes to be -118 dB. In reviewing the EU data on Flight No. 8 it becomes apparent that the present indication of -118 dB is more like -123 dB based on the AGC measurements made when the equipment was in the labs the week of 17 April.

Runs 8 and 9 of this flight appeared good; however, the airborne data recorder failed due to a defective cooling fan and defective memory.

I talked to Captain Bybee after the flight and confirmed by reviewing some quick look data that the recorder had worked until about the last 20 minutes of the flight.

9 May 72 49208 FK

Flight No. 11 was good, for MRL nothing specific to report.

25 April 72

Equipment ready for installation.

26 April 72

0700 Back on Site. Installed equipment in aircraft. Preflight OK.

Flight No. 8 49202a smooth - no problems.

1 May 72

Flight No. 9 preflight good - no problems. Run one started, all four channels locked. No problems were experienced with MX-450 during flight. EU cal should be -123 ± 1 dBm.

	Channel 1	Channel 2	Channel 3	Channel 4
Cal	-118.9	-120.1	-119.1	-119.7
Initial Track	-118.9	-124.0	-119.1	-116.0

2 May 72

Checked system, all appears normal. The AGC readings appeared normal and stable.

Ran long term burn test on MX-450. The AGC levels appear normal in all respects.

4 May 72 49204AB

Flight No. 10 was good as far as MRL equipment was concerned. However, channel No. 1 is slow to acquire what GAC believes to be -118 dB. In reviewing the EU data on Flight No. 8 it becomes apparent that the present indication of -118 dB is more like -123 dB based on the AGC measurements made when the equipment was in the labs the week of 17 April.

Runs 8 and 9 of this flight appeared good; however, the airborne data recorder failed due to a defective cooling fan and defective memory.

I talked to Captain Bybee after the flight and confirmed by reviewing some quick look data that the recorder had worked until about the last 20 minutes of the flight.

9 May 72 49208 FK

Flight No. 11 was good, for MRL nothing specific to report.

REPORT NO 2653 TRIP REPORT FORM DATE 17 June 1972

PLACE VISITED Holloman AFB Alamogordo, New Mexico DATE

PURPOSE OF VISIT Flight Test 621B/MX 450

CUSTOMER PERSONNEL:	MAGNAVOX PERSONNEL
Capt. C. Rose	Mel Taylor
Lt. Col. Deem	
Capt. Wilson	
Capt. Edgar	
R. Lano	

SUMMARY:

(1) 7 June Flight No. 016 CNX due to WX and primary generator failure.

(2) 621B/MX 450 removed from installation for uplink monitor link doppler effects.

(3) 13 June Channel No. 2 slow to calibrate. Ok prior to first pass.

(4) 14 June Remove 621B/MX 450 for bench checks after flight "A" ok

FOLLOW UP ACTION REQUIRED

COGNIZANT FIELD SALES PERSON

REPORTED BY Mel Taylor

cc MRL Personnel Above
Frank Charles
R. Cnossen
W.H. Trappen

MRL 62422A

4 June 72

Scheduled to depart LAX to Alamogordo for 621B Flight No. 016. My departure cancelled due to flight rescheduling.

6 June 72

On site for Flight No. 016. MX-450/621B functionally checked good. Equipment installed in aircraft and again functionally checked good.

7 June 72

Flight No. 016 preflight tests were performed and performance checks indicate that the system is operating properly.

0700 flight crew on board No. 0371 departed aircraft for MCS.

1000 advised that aircraft takeoff had been delayed due to weather.

1030 Flight No. 016 cancelled due to weather and primary generator failure.

I was requested by R. Laho to pull the MX-450/621B system for uplink, monitor link delay measurements. I removed the system as requested and I'm setup and ready for measurement test. The delay measurements were made with the use of a Haz transmitter. The salt "1" "A" transmitter was used. The first step was to insure that the MX-450 receiver would acquire the transmitted coded signal, it did.

The MX-450 Receiver Test Set was then setup to monitor the channel one pseudorange (P/R) and pseudodoppler (P/D) when the receiver and transmitter clocks were sync.

After the P/D was set to a null the P/R was measured as displayed on the test set. The P/R was then recorded as read when the count was measured at the uplink output terminal. A second measurement was made at the monitor terminal and a range difference was obtained. The data recorded was inconclusive.

9 June 72

Flight scheduled for 12 June cancelled.

12 June 72

On site for flight scheduled the 13th of June. Bench tests performed on MX-450 receiver, all appears good, system installed on aircraft and retested. The test performance was good.

13 June 72

Calibration AGC's are as follows:

Readings taken at:

	Channel 1	Channel 2	Channel 3	Channel 4	Channel 5	Channel 6
0445	7	11	8	7	3	1
0600	7	12	8	8	1	-123

0600 Data recorders and video displays check.

9000. 0630 departed flight line for MCS.

In flight operations:

Just prior to takeoff cal cycle initiated but channel No. 2 would not calibrate. Power was recycled calibrate initiated but to no avail. Second power cycle made and extended calibration initiated and all four channel performed properly.

In flight operations were normal. Both receivers operational.

During pass 3 the salt "A" transmitter became intermittent and the MCS as well as both airborne receivers dropped lock.

(Haz representative) and I went to Salt site to check the transmitter. The battery power and low power monitors were both low. Changed battery, monitor power up some. MCS and airborne receivers appear normal.

In order to eliminate transmission delay differencies between the uplink and monitor link the MCS and airborne receivers were all locked to the uplink transmission signals. GAC plans to make 4 to 6 more flights in this configuration.

I removed the MX-450 system from the aircraft for bench test. The Salt Site "A" transmitter was brought into the lab from the range and this transmitter was again used to confirm the operational readiness of the MX-450 system. Several calibrate cycles were performed and all appears normal.

I looked at the alarm and locked signals of the PLM in the microwave section. The levels were as follows:

Locked test point:	Phase Locked 3.3 VDC	Phase Unlocked 1.9 VDC
	Phase Locked 1.6 VDC	Phase Unlocked 4.9 VDC

The MX-450 is functionally sound and all four channels acquire to at least -123 dBm as best can be determined with equipment available and field techniques.

REPORT NO. 2654 **TRIP REPORT FORM** DATE 30 June 72

PLACE VISITED Holloman AFB Almogordo, New Mexico **DATE**

PURPOSE OF VISIT Flight Test 621B/MX 450

CUSTOMER PERSONNEL:	**MAGNAVOX PERSONNEL**
	M. Taylor

SUMMARY:

(1) Flt No. 018 ok MRL
(2) Flt. No. 019 ok MRL.
(3) Flt. No. 020 Channel No. 2 would not cal. shortly before flight.
(4) Removed readjusted R32 "K" circuit
(5) Ready for flight
(6) Inflight abort. Plane struck a "goose"
(7) Decision made to put 0371 in phase. No more 621B flights until 19 July.

FOLLOW UP ACTION REQUIRED

COGNIZANT FIELD SALES PERSON

REPORTED BY Mel Taylor

cc MRL Personnel Above
F. Charles
R. Cnossen
W. Trappen

MRL 62422A

20 June 72

Flight No. 018

Preflight for MRL good. Pass No. 2 of this flight was aborted due to MCS unlock condition.

EC 50 xmtr inoperative aircraft holding
Runs No. 2 and 5 aborted or delayed
Runs No. 5, 6 and 7 OK.
Runs 1 through 5 had a 3 dB pad inserted in the ant line of both receivers. Runs 5 through 7 had a total of 13 dB inserted. The hold on signal level was in the area of -134 dBm.

22 June 72

Flight No. 019

MX-450 - OK

26 June 72

Flight No. 0201

On site 0700 preflight good. No apparent problems. System looks good and AGC's appear stable. At approximately 30 minutes before flight time the noise AGC Channel No. 2 went to a very high positive level +6 VDC. Tried to adjust the K trigger, but to no avail. Tried to adjust the noise AGC down still to no avail. Informed F. Charles of conditions, also talked to M. Wong, but still unable to repair prior to aircraft departure. During Flight Channel No. 2 would not calibrate and remained in the "acq" mode.

During the flight everything with the exception of channel two worked well.

The system was removed from aircraft. M. Wong was consulted regarding repair action.

I was soon able to adjust the noise, signal and K pots to proper levels and all seems to work normal.

27 June 72

0700 Equipment operational on for thermal drift test

1300 Readjusted suspect K amplifiers

1800 Levels appear stable

28 June 72

0400 Equipment on looks good

0800 Still looks good. Installed equipment on aircraft

1200 Post power transfer calibration OK.

1300 0371 returned to base after striking a goose while in flight.

29 June 72

1400 Decision not to fly aircraft 0371 made at this time. Frank Charles advised of same. I was asked to pack and return 621B/MX-450 to MRL for test and evaluation.

30 June 72

621B/MX-450 packed and shipped to LAX.

3 July 72

Equipment setup and analyzed. Replaced R32 of PC Receiver No. 1. R32 found to open intermittently. Replaced pot readjusted levels and all appears normal.

REPORT NO. 2667 **TRIP REPORT FORM** DATE 10 August 1972

PLACE VISITED Holloman AFB - Alamogordo, New Mexico DATE 7/24 - 8/1/72

PURPOSE OF VISIT Flight Test 621-B Program

CUSTOMER PERSONNEL:	**MAGNAVOX PERSONNEL**
GAC	M. Taylor
HAC	
SAMSO	
USAF	

SUMMARY:

- 621-B/MX-450 repair and re-shipment to HAFB
- Control Box shock test
- Project airplane returned from phase maintenance
- Project Flight #21, 27 July 1972
- Project Flight #22, 1 August 1972
- Project transition from area nav to ILS
- Equipment operating time estimate

FOLLOW UP ACTION REQUIRED

COGNIZANT FIELD SALES PERSON

REPORTED BY M. Taylor

cc MRL Personnel Above ; W. Trappen ; L. Jacobson; E. Long; F. Charles; J. Kruse

MRL 62422A

24 July 72

The 621-B/MX-450 was transported from MRL and was shipped direct to El Paso; and transported to Holloman AFB.

During the unpacking, and setup phase following shipment from LAX, the control box was inadvertently knocked off the signal processor onto the floor. I found it necessary to replace about eight or nine of the 327 bulbs, but for the most part, no other damage was observed.

25 July 72

The airplane 0371 returned from its GEANS mission. After the system was installed, I contacted Capt. Bybee regarding the cutting of a test tape. A short time later, I was advised that a test tape would not be necessary as long as the video display was functioning. I'm satisfied the recorder is working properly, since the monitored video display looked good.

1700 - The flight scheduled for the 26th may be delayed, or cancelled due to a Viking launch.

26 July 72

0600 - On site for preflight activities, the 621-B/MX-450 is all go.

HAZ appears to have a problem in locating the power cable for their auxilliary blower. It appears that while the airplane was in phase, several wires and cables relative to the 621B systems were removed, or tucked into a bundle in areas not relative to 621B. GAC could not locate a couple of cables necessary for the interface with the HAZ receiver. The cables were finally located in some obscured, out-of-the-way place. The overheating problem became very apparent when it was learned the aircraft air conditioning system was inoperative. The MRL 621B/MX-450 was on, and operative since its cooling system is internal and independent of aircrafts. No heating problems were apparent.

The flight was cancelled due to the Viking launch, and the 621B program is on the schedule for 27 July 72.

27 July 72

0700 - On site systems preflight is good. The flight was uneventful, and receiver worked as advertised.

31 July 72

1200 - On site. System functionally checked OK; data records and display operational; system ready for scheduled flight activities.

1 August 72

0700 - Systems preflight. The 621B/MX-450 is ready.

Inflight operations were pretty much the same as previous flights. However, during the first three passes of this flight (Flight No. 22) Channels 1 and 4 of MRL would not acquire and Channel 2 of HAZ would not acquire. It became necessary to adjust the power levels of the transmitter up by as much as 7 dB. All channels appear to function after power adjustments.

GAC has concluded the area nav portion of the 621B flight test program, and is in the process of moving from the 50 mile area, to the Northrup strip where the ILS tests will be performed.

The project aircraft 0371 departed Holloman AFB enroute to Alaska via Kirkland AFB for GEANS systems tests. The project aircraft is expected to return to Holloman AFB on 9 August 72 and the first ILS flight is scheduled 11 August 72. I have recently been informed (Mike Moore, GAC, via telecon) of changes in the 621B flight test schedule. At this wiring, the first ILS flight is scheduled for 16 August 72.

The 621B/MX-450 system has been operated in excess of 1400 hours. There were two (2) IC failures during system integration and checkout; these failures should be attributed to handling. There have been two (2) failures since the flight tests began.

The defective IC found on the IPM board may have been damaged due to troubleshooting and handling. The defective Pot R32 on the PC Receiver No. 1 may well have been defective from day One.

REPORT NO 2690 **TRIP REPORT FORM** DATE 5 October 72

PLACE VISITED Holloman AFB DATE 3 October 72

PURPOSE OF VISIT Flight Test 621B "ILS"

CUSTOMER PERSONNEL:	MAGNAVOX PERSONNEL
Major Denning	Mel Taylor
Captain Rose	
Captain Wilson	
Ralph Laho	
Lt. Montgomery	

SUMMARY:

(1) Flight No. 24. MRL functional Channel No. 1 SPB at xmtr. Low would not acquire channel No. 1.

(2) Flight No. 25 both receivers operational. Good flight.

(3) 22 August advised by R. Laho. No range or doppler information on Flight 24 and 25.

(4) 24 August 621B/MX-450 confirmed as working good. Problem in software programming.

(5) 27 September. First touch and go operations.

(6) 28 September Flight 29 six passes.

(7) 29 September Flight 30 Balloon xmtr inoperative after second pass

(8) 30 September Flight 31 MCS rx inoperative after 6th pass

(9) Flight test concluded. Equipment returned to plant.

(10) AGC readings

(11) Flight chart

FOLLOW UP ACTION REQUIRED

F. Charles	E. Long
L. Jacobson	W. Trappen
J. Kruse	R. Crossen

COGNIZANT FIELD SALES PERSON

REPORTED BY Mel Taylor

cc MRL Personnel Above

MRL 62422A

15 August 72

Arrived Holloman AFB 11:30 and proceeded to Project Aircraft 0371. Made normal system checkout, and everything checks good.

16 August 72

0700 on site and normal systems tests performed.

During the first pass of the ILS flight it was learned that Channel 1 of the MRL receiver would not acquire. It was soon learned that the SPB signal had been reduced below the useable level as a result of attenuation inserted in the short code line. Channels 2, 3 and 4 appeared to function OK.

17 August 72

Systems checked out good, MRL ready for flight scheduled for 18 August.

18 August 72

Normal preflight, no problems.

The inflight operations were much the same as flights in the past.

22 August 72

I received a phone call from Ralph Laho, and was advised that the MRL P/R, and P/D did not function for Flight 24 or 25. It was stated that P/R was 0000 or 2048. P/D was 0 or - .078 throughout both flights. I asked Ralph if any changes had been made to the computer program relative to the EU/VAL used. The answer was no.

I talked to J. Kruse, L. Jacobson, B. Glazer and L. Seidle about the problem. Armed with a wealth of information, I departed for Holloman Air Force Base. Lt. Montgomery arrived from Kirkland AFB with the MRL equipment. My approach, based on the information from Mr. Laho, was that we had an equipment problem. The initial tests did not confirm what I had been told. The data as displayed on the system tester indicated the system was working well. The information at the test data No. 2 output was perfect. The problem now is confirming the data into RAM is the same information that appears on the recorder data output. After a whole day of checking the system and finding nothing wrong, I decided to have a test tape made while dynamics were being applied. The data was good. This means nothing is wrong with the MRL system. "GAC" made another dump of the 25th flight original tape. The re-dump was good. The data which was at the Kirkland AFB was sent via link back down to us. The data was good. This means, of course, that the data written into the computer program was wrong. Now I learn that minor changes had been made to the computer program, those changes should not have effected the EU/VAL; they did.

25 August 72

Departed Holloman AFB for LAX. No flights this week. 621B flights cancelled due to defense suppression test.

8 September 72

Flight number 26 cancelled due to high wind conditions. The balloon crew is unable to launch the balloon due to high wind conditions.

14 September 72

Arrived Holloman 1145 and was advised that the flight scheduled for 15 September had been cancelled about an hour ago due to wet road conditions, and the inability of the optics crews to get to the Northrup strip area. I made the normal system tests and the equipment is functioning properly.

15 September 1972

I advised the home office of the events and that I would be departing. Flights are scheduled for the 20th, 21st and the 22nd of this month.

19 September 1972

Departed LAX for Holloman, arrived 1130. The ground crew for 0371 was out to lunch so I was unable to check equipment at this time. 1330 ground crew returned, 621B/ MX-450 system checks OK.

A transmitter was brought in for basic EMI tests while the TRW unit was operating. The HAZ and MRL receivers were locked to the channel two transmitter, the TRW unit didn't seem to effect the operation of either of the receivers.

20 September 72

Preflight for all receivers were good. Aircraft departed for Northrup strip, channel 1, 3 and 4 locked for MRL and HAZ, nothing received from the No. 2 transmitter. The MCS locked to all four channels.

21 September 72

Preflight normal, no problems. During the early portions of this flight, it was learned that the HAZ nor MRL Channel 2 on the airborne receiver would acquire. After a couple of passes the flight was called off because of the Channel 2 transmitter problem. Flight scheduled for Monday 25 September preflight schedule for 24 September.

25 September 72

Flight No. 27

Normal preflight, both receivers appear to be functional. The flight went smooth. It was learned that the optics film didn't come out so no solution appears to be likely.

27 September 72

Flight No. 28

This flight appeared to be a good one. Eleven touch and go passes were made.

It was learned that the GFE airborne recorder buffer on the MRL system didn't function properly. The result being, no data relative to a NAV solution. During one of the touch and go landings the MRL receiver dropped lock on all four channels. The MRL receiver reacquired one or two channels prior to rotation, and all channels were locked prior to flare point of the next pass.

28 September 72

Flight 29

Since it was not known at this point that the MRL airborne recorder had malfunctioned, and since the HAZ receiver Channel No. 1 was inoperative, it was decided by Ralph Laho to make only six touch and go landings this flight. The following events took place during the touch and go operation of this flight.

Pass #1 All channels dropped lock upon touchdown. All channels reacquired prior to next pass

Pass #2 All channels stayed in track

Pass #3 All channels dropped lock upon touchdown

Pass #4 All channels dropped lock upon touchdown

Pass #5 All channels remained in track

Pass #6 All channels remained in track

I requested the operator to place the MRL system in calibrate prior to landing at Holloman AFB. The system dropped lock upon touchdown. The test performed eliminates couplers and input cables to the system. Post flight tests didn't reveal anything out of the ordinary. I inspected the shock mounts in the aircraft relative to the MRL system. They are rated at 20 - 40 lbs each and they appear to be flat or very near the bottom of its travel. Since the system reacquires prior to flare of the succeeding pass, I decided to note the condition and not to troubleshoot the system.

29 September 72

Flight No. 30

Preflight good for MRL. The first pass of this flight looks good, however, Channel No. 4 "balloon" transmitter is intermittent. I think Pass No. 2 was a good one. All channels remained in track during the touch and go.

The "balloon" transmitter battery pack just died and there goes the flight for today.

30 September 72

Flight No. 31

Preflight good, both receivers operational. We are driving two recorders today which was done yesterday also. This is being done because nothing was found regarding the recorder problem on Wednesday. Both of the MRL recorders worked; still no reason for the failure Wednesday. The following events took place during the flight:

Pass #1	All channels remained in track "dry run"
Pass #2	Channel #4 dropped lock shortly after touchdown
Pass #3	Hard landing, all four channels dropped lock. MCS receiver intermittent at times.
Pass #4	All channels remained in track
Pass #5	Channel #1 dropped lock reacquired prior to rotation
Pass #6	Channel #1 dropped lock reacquired prior to rotation
Pass #7	All channels remained in track; however, MCS receiver is inoperative. Mission aborted at this time.

Flight #31 is the last flight for the 621B program. The equipments were removed from the aircraft and I'm shipping the MX-450 to MRL.

The following notes the AGC values taken at various times throughout the flight test program.

1 May 72 1 + 00

Chnl	Stby	Track
1	16	9
2	24	16
3	16	10
4	16	10
5	0	1
6	4	3

14 June 72 1 + 00 1 + 30

Chnl	Stby	Track	Track
1	MSG	7	7
2	MSG	11	12
3	MSG	8	8
4	MSG	7	8
5	MSG	3	3
6	MSG	1	127

MSG= Missing

20 June 1 + 00

Chnl	Stby	Track
1	16	8
2	22	12
3	15	9
4	14	9
5	2	2
6	122	122

26 June 1 + 00

Stby	Track
12	7
16	12
12	8
13	8
0	2
20	1

28 June + 50   1 + 25

Chnl	Stby	Track	Track
1	13	8	8
2	13	12	12
3	15	9	8
4	16	8	8
5	1	2	1
6	127	127	0

25 July +30   2 + 30

Chnl	Stby	Track	Stby	Track
1	17	14	16	10
2	17	12	16	12
3	16	12	15	10
4	16	12	15	11
5	2	2	1	2
6	8	10	127	122

16 August 1 + 00

Chnl	Stby	Track
1	16	10
2	15	11
3	15	10
4	13	10
5	0	1
6	3	3
1 + 30		
1	16	10
2	16	10
3	14	10
4	14	10
5	2	2
6	2	128
Time 2 + 50		
1	16	10
2	16	12
3	15	10
4	15	10
4	15	10
5	1	1
6	124	124

27 September

Chnl	Stby	Track
1	23	16
2	22	19
3	20	15
4	19	17
5	0	0
6	24	19
Time + 50		
1	13	8
2	13	12
3	15	9
4	16	8
5	1	2
6	127	127
28 September 1 + 00		
1	16	9
2	16	11
3	15	9
4	14	9
5	1	1
6	3	4

Chnl	Stby	Track
Time 2 + 30		
1	16	10
2	16	12
3	14	10
4	14	10
5	2	2
6	2	2

29 September Time 2 + 00

Chnl	Stby	Track
1	16	9
2	16	11
3	14	9
4	15	9
5	2	2
6	2	2

DATE	MRL RX	MRL RECORDER	REMARKS
7 Mar	OK	No good	Fuel leak
15 Mar	OK	No good	Mod to master controller incorrectly made
21 Mar	No SPB	No good	
28 Mar	OK	OK	
5 Apr	OK	OK	
7 Apr	OK	OK	Coin flip determined who would have recorder - MRL won
12 Apr	OK	OK	
13 Apr	OK	OK	Has airborne Rx used in MCS
27 Apr	OK	OK	
1 May	OK	OK	Sync poise detector in airborne rec. erratic
7 May	OK	Pass 8&9 no good	
9 May	OK	OK	
10 May	OK	OK	
15 May	OK	OK	
17 May	OK	OK	Channel 4 questionable
19 May	OK	OK	CNX acft generator
7 June	OK	OK	Glitch on HAZ recorder
14 June	OK	OK	HAZ driving two recorder
20 June	OK	OK	Has 15 MHz sync detuned no go lights throughout flight
22 June	OK	OK	

DATE	MRL RX	MRL RECORDER	REMARKS
26 June	No go	OK	Channel No. 2 remains in standby - pot
28 June	OK	OK	Spruce Goose
27 July	OK	OK	No record signal light
1 August	OK	OK	
16 August	OK	OK	Channel No. 1 xmtr inop-low SPB from Xmtr. PR/PD rpt no good, software
19 August	OK	OK	PR/PD report no good software problem
20 Sept	OK	OK	Aborted after a couple of passes
25 Sept	OK	OK	No coarse range Channel 1
27 Sept	OK	OK	No self test
28 Sept	OK	OK	No lock Channel No. 1 balloon xmtr
29 Sept	OK	OK	Balloon xmtr inop
30 Sept	OK	OK	MCS intermittent after 6th pass MSG aborted after 7th pass.

APPENDIX G

RELIABILITY PREDICTIONS

THE **Magnavox** COMPANY

FORT WAYNE, INDIANA 46803

COMPONENT STRESS ANALYSIS
RELIABILITY PREDICTION

DATE OF ISSUE:

REVISION DATE:

PROJECT: MX-450

EQUIPMENT: SIGNAL PROCESSOR ASSY.

DRAWING NO.: 917481

STRESS: AIRBORNE

PREPARED BY:

PAGE: 1 OF 2

FAILURE RATE: 2051.229 $f/10^6$ Hrs.

AMB. TEMPERATURE: 25°C

ITEM NO.	CIRCUIT NO.	FAILURE RATE CHART	TEMP °C	RATED STRESS	APPLIED STRESS	STRESS RATIO	QTY	K_A	STRESS FAILURE RATE	TOTAL FAILURE RATE	FR SOURCE
1		917423	35	CORRELATOR/ LOCAL REFERENCE			4		60.222	240.888	
2		917424		IF AMPLIFIER			4		48.940	195.760	
3		917425		POST CORRELATION RECEIVER 1			4		156.345	625.380	
4		917426		POST CORRELATION RECEIVER 2			4		90.702	362.808	
5		917427		A/D CONVERTER			2		19.460	38.920	
6		917428		DIGITAL LOOP FILTER			1		9.092	9.092	
7		917442		FILTER TIMER			1		5.434	5.434	
8		917429		CARRIER RATE MULTIPLIER			1		4.555	4.555	
9		917430		CLOCK RATE MULTIPLIER			1		3.635	3.635	
10		917431		INCREMENTAL PHASE MODULATOR			4		56.366	225.464	
11		917433		CODER			5		9.282	46.410	
12		917435		CHANNEL CONTROLLER			2		6.210	12.420	
13		917434		MASTER CONTROLLER			1		7.282	7.282	
14		917441		VELOCITY D/A CONVERTER			1		41.772	41.772	
15		917436	35	RANGE/DOPPLER EXTRACTOR			1		4.926	4.926	
									TOTAL	1824.746	

MRL 70-1014

THE **Magnavox** COMPANY

FORT WAYNE, INDIANA 46803

COMPONENT STRESS ANALYSIS
RELIABILITY PREDICTION

DATE OF ISSUE	REVISION DATE	PREPARED BY	PAGE 2 OF 2
PROJECT MX-450		FAILURE RATE 2051.229 $F/10^6$ Hrs.	
EQUIPMENT SIGNAL PROCESSOR	DRAWING NO. 917481	STRESS AIRBORNE	AMB. TEMPERATURE 25°C

ITEM NO.	CIRCUIT NO.	FAILURE RATE CHART	TEMP °C	RATED STRESS	APPLIED STRESS	STRESS RATIO	QTY	K_A	STRESS FAILURE RATE	TOTAL FAILURE RATE	FR SOURCE
16		917437	35	RECORDER INTERFACE 1			1		5.004	5.004	
17		917438		RECORDER INTERFACE 2			1		5.065	5.065	
18		917432		RECORDER INTERFACE 3			1		3.180	3.180	
19		917440		FREQUENCY SYNTHESIZER 2			1		32.821	32.821	
20		917446		FREQUENCY SYNTHESIZER 3			1		15.375	15.375	
21											
22			35	FRONT PANEL CHASSIS PARTS					165.038	165.038	

MRL 70-1014

TOTAL 226.483

THE **Magnavox** COMPANY

FORT WAYNE, INDIANA 46803

COMPONENT STRESS ANALYSIS
RELIABILITY PREDICTION

DATE OF ISSUE	REVISION DATE	PREPARED BY	PAGE 1 OF 1
PROJECT MK-450		FAILURE RATE 638.970 f/10⁶ hrs.	
EQUIPMENT AUXILLARY UNIT ASSY.	DRAWING NO.	STRESS AIRBORNE	AMB. TEMPERATURE 25°C

ITEM NO.	CIRCUIT NO.	FAILURE RATE CHART	TEMP °C	RATED STRESS	APPLIED STRESS	STRESS RATIO	QTY	K_A	STRESS FAILURE RATE	TOTAL FAILURE RATE	FR SOURCE
1		917443	35	MICROWAVE RECEIVER			1		184.457	184.457	
2		917445		135 MHZ IF/ POWER BOOST			1		127.561	127.561	
3		917446		FREQUENCY SYNTHESIZER 1			1		67.930	67.930	
4				POWER SUPPLY ASSY.			1		182.408	182.408	
5				OSCILLATOR ASSY (625W)			1		8.470	8.470	
6											
7			35	CHASSIS PARTS					68.144	68.144	

MRL 70-1014

TOTAL 638.970

MRL RELIABILITY ESTIMATE			ITEM NO.	ASSEMBLY NO. 917443	
PREPARED	DATE	JOB/EQUIPMENT MX-450	ASSEMBLY NAME MICROWAVE RECEIVER		
APPROVED			NEXT ASSEMBLY		PAGE OF

COMPONENTS	TYPE	QUANT	F.R./10^6 HR	TOTAL F.R.
RESISTORS	Compos.			
	Film			
	Film Pwr			
	Wire Wnd			
POTS	Film	1	9.360	9.360
	Wire Wnd			
FIXED CAPACITOR	Tantalum			
	Electroly			
	MICA	8	0.005	0.040
VARIABLE CAPACITOR	Vacuum			
TRANSFORMER	Filament			
	Power			
	Lo Pwr Pls			
ELECTRON TUBES	Receiver			
	Pwr Rect			
	Xmtr			
C.R.T.'S	1 - Gun			
	3 - Gun			
KLYSTRONS				
THYRATRONS				
MAGNETRONS				
T.W.T.'S				
AMPLITRONS				
TR OR ATR				
DUPLEXER				
MICROWAVE DIODE	Mixer			
	Detector			
MICROWAVE COMPONENTS	Attenuat			
	Direct Cpl			
	Loads			
	Stubs			
	Feed Horn			
	Rotary Jt			
FERRITE DEVICES	Isolator			
	Circulator			
	Modulator			
	Shifter			
RF FILTERS				
HI VOLTAGE DIODE PACK	Hi Power			
	Med Power			
PULSE FORM NETWORK	Lo Volt			
	Hi Volt			

COMPONENTS	TYPE	QUANT	F.R./10^6 HR	TOTAL F.R.
TRANSISTOR				
DIODES	General & Computer			
	HP	3	2.200	6.600
	Zener	2	1.260	2.520
MICROCIRCUITS	LINEAR	4	0.400	1.600
CONNECTORS	Coax	30	0.160	4.800
	≤ 25 Pin			
	> 25 Pin			
INDUCTORS	DC Filter			
	RF & Chok	1	0.225	0.225
	Chg React			
RELAYS				
SWITCHES	DIODE	1	2.798	2.798
SWITCH/LAMP ASSEMBLY	1 - Lamp			
	2 - Lamp			
	4 - Lamp			
INDICATOR (NON SWITCH)	1 - Lamp			
	2 - Lamp			
	4 - Lamp			
MOTORS FANS BLOWER — BRUSH-LESS	≤ 6,000 rpm			
	> 6,000 rpm			
MOTORS FANS BLOWER — BRUSH-TYPE	≤ 6,000 rpm			
	> 6,000 rpm			
QUARTZ CRYSTAL				
RESOLVER & SYNCHROS				
DELAY LINE	RLC			
	Quartz			
MULTIPLIER	—	1	86.400	86.400
PRE AMP	—	1	23.090	23.090
FILTER	—	7	0.400	2.800
DETECTOR	—	1	6.080	6.080
MIXER	—	2	1.514	3.028
POWER DIVIDER	—	2	0.436	0.872
ATTENUATOR	—	4	6.856	27.424
IF AMPL	—	1	4.000	4.000
LIMITER	—	1	2.200	2.000
SAMPLER	—	1	0.820	0.820
				184.457

MRL 70-1024

MRL RELIABILITY ESTIMATE

ITEM NO.		ASSEMBLY NO.	917483
PREPARED	DATE	JOB/EQUIPMENT	ASSEMBLY NAME: CONTROL BOX ASSY
APPROVED		MK-250	NEXT ASSEMBLY
			PAGE OF

COMPONENTS	TYPE	QUANT	F.R./10^6 HR	TOTAL F.R.
RESISTORS	Compos.			
	Film			
	Film Pwr			
	Wire Wnd			
POTS	Film			
	Wire Wnd			
FIXED CAPACITOR	Tantalum			
	Electroly			
VARIABLE CAPACITOR	Vacuum			
TRANSFORMER	Filament			
	Power			
	Lo Pwr Pls			
ELECTRON TUBES	Receiver			
	Pwr Rect			
	Xmtr			
C.R.T.'S	1 - Gun			
	3 - Gun			
KLYSTRONS				
THYRATRONS				
MAGNETRONS				
T.W.T.'S				
AMPLITRONS				
TR OR ATR				
DUPLEXER				
MICROWAVE DIODE	Mixer			
	Detector			
MICROWAVE COMPONENTS	Attenuat			
	Direct Cpl			
	Loads			
	Stubs			
	Feed Horn			
	Rotary Jt			
FERRITE DEVICES	Isolator			
	Circulator			
	Modulator			
	Shifter			
RF FILTERS				
HI VOLTAGE DIODE PACK	Hi Power			
	Med Power			
PULSE FORM NETWORK	Lo Volt			
	Hi Volt			

COMPONENTS	TYPE	QUANT	F.R./10^6 HR	TOTAL F.R.
TRANSISTOR				
DIODES	General & Computer			
	Rectifier			
	Zener			
MICROCIRCUITS				
CONNECTORS	Coax			
	≤ 25 Pin			
	> 25 Pin			
INDUCTORS	DC Filter			
	RF & Chok			
	Chg React			
RELAYS				
SWITCHES	No Lamp			
SWITCH/LAMP ASSEMBLY	1 - Lamp			
	2 - Lamp	3	5.300	15.900
	4 - Lamp			
INDICATOR (NON SWITCH)	1 - Lamp			
	2 - Lamp	5	0.800	4.000
	4 - Lamp			
MOTORS FANS BLOWER — BRUSHLESS	< 6,000 rpm			
	> 6,000 rpm			
MOTORS FANS BLOWER — BRUSH-TYPE	≤ 6,000 rpm			
	> 6,000 rpm			
QUARTZ CRYSTAL				
RESOLVER & SYNCHROS				
DELAY LINE	RLC			
	Quartz			
METER		4	0.500	2.000
				21.900

MRL 70-1024

MRL RELIABILITY ESTIMATE

PREPARED	DATE	JOB/EQUIPMENT	ITEM NO.	ASSEMBLY NO. 917445
APPROVED		MK-450	ASSEMBLY NAME 135 MHZ IF/POWER BOOST	
			NEXT ASSEMBLY	PAGE OF

COMPONENTS	TYPE	QUANT	F.R./10^6 HR	TOTAL F.R.
RESISTORS	Compos.			
	Film			
	Film Pwr			
	Wire Wnd			
POTS	Film	1	9.360	9.360
	Wire Wnd			
FIXED CAPACITOR	Tantalum			
	Electroly			
VARIABLE CAPACITOR	Vacuum			
TRANSFORMER	Filament			
	Power			
	Lo Pwr Pls			
ELECTRON TUBES	Receiver			
	Pwr Rect			
	Xmtr			
C.R.T.'S	1 - Gun			
	3 - Gun			
KLYSTRONS				
THYRATRONS				
MAGNETRONS				
T.W.T.'S				
AMPLITRONS				
TR OR ATR				
DUPLEXER				
MICROWAVE DIODE	Mixer			
	Detector			
MICROWAVE COMPONENTS	Attenuat			
	Direct Cpl			
	Loads			
	Stubs			
	Feed Horn			
	Rotary Jt			
FERRITE DEVICES	Isolator			
	Circulator			
	Modulator			
	Shifter			
RF FILTERS				
HI VOLTAGE DIODE PACK	Hi Power			
	Med Power			
PULSE FORM NETWORK	Lo Volt			
	Hi Volt			

COMPONENTS	TYPE	QUANT	F.R./10^6 HR	TOTAL F.R.
TRANSISTOR				
DIODES	General & Computer			
	Rectifier	6	2.200	13.200
	Zener			
MICROCIRCUITS	LINEAR	8	0.400	3.200
CONNECTORS	Coax	26	0.160	4.160
	≤ 25 Pin			
	> 25 Pin			
INDUCTORS	DC Filter			
	RF & Chok	2	0.225	0.450
	Chg React			
RELAYS				
SWITCHES	No Lamp			
SWITCH/LAMP ASSEMBLY	1 - Lamp			
	2 - Lamp			
	4 - Lamp			
INDICATOR (NON SWITCH)	1 - Lamp			
	2 - Lamp			
	4 - Lamp			
MOTORS FANS BLOWER — BRUSH-LESS	≤ 6,000 rpm			
	> 6,000 rpm			
MOTORS FANS BLOWER — BRUSH-TYPE	≤ 6,000 rpm			
	> 6,000 rpm			
QUARTZ CRYSTAL				
RESOLVER & SYNCHROS				
DELAY LINE	RLC			
	Quartz			
IF AMPL	—	5	4.000	20.000
ATTENUATOR	—	4	6.856	27.424
POWER DIVIDER	—	2	0.436	0.872
DETECTOR	—	1	6.080	6.080
917445-1	—	1	13.300	13.300
917445-2	—	1	18.475	18.475
917445-3	—	1	11.040	11.040
				127.561

MRL 70-1024

MRL RELIABILITY ESTIMATE

PREPARED	DATE	JOB/EQUIPMENT	ITEM NO.	ASSEMBLY NO. 917445-1
APPROVED		MX-450	ASSEMBLY NAME UTF-015 ATTEN. DRIVER AMPL.	
			NEXT ASSEMBLY	PAGE OF

COMPONENTS	TYPE	QUANT	F.R./10^6 HR	TOTAL F.R.
RESISTORS	Compos.	5	0.018	0.090
	Film	5	0.156	0.780
	Film Pwr			
	Wire Wnd			
POTS	Film	1	9.360	9.360
	Wire Wnd			
FIXED CAPACITOR	Tantalum			
	Electroly	1		
	CERAMIC	4	0.025	0.100
VARIABLE CAPACITOR	Vacuum			
TRANSFORMER	Filament			
	Power			
	Lo Pwr Pls			
ELECTRON TUBES	Receiver			
	Pwr Rect			
	Xmtr			
C.R.T.'S	1 - Gun			
	3 - Gun			
KLYSTRONS				
THYRATRONS				
MAGNETRONS				
T.W.T.'S				
AMPLITRONS				
TR OR ATR				
DUPLEXER				
MICROWAVE DIODE	Mixer			
	Detector			
MICROWAVE COMPONENTS	Attenuat			
	Direct Cpl			
	Loads			
	Stubs			
	Feed Horn			
	Rotary Jt			
FERRITE DEVICES	Isolator			
	Circulator			
	Modulator			
	Shifter			
RF FILTERS				
HI VOLTAGE DIODE PACK	Hi Power			
	Med Power			
PULSE FORM NETWORK	Lo Volt			
	Hi Volt			

COMPONENTS	TYPE	QUANT	F.R./10^6 HR	TOTAL F.R.
TRANSISTOR				
DIODES	General & Computer			
	Rectifier			
	Zener	2	1.260	2.520
MICROCIRCUITS				
CONNECTORS	Coax			
	≤ 25 Pin			
	> 25 Pin			
INDUCTORS	DC Filter			
	RF & Chok	2	0.225	0.450
	Chg React			
RELAYS				
SWITCHES	No Lamp			
SWITCH/LAMP ASSEMBLY	1 - Lamp			
	2 - Lamp			
	4 - Lamp			
INDICATOR (NON SWITCH)	1 - Lamp			
	2 - Lamp			
	4 - Lamp			
MOTORS FANS BLOWER — BRUSH-LESS	< 6,000 rpm			
	> 6,000 rpm			
MOTORS FANS BLOWER — BRUSH-TYPE	≤ 6,000 rpm			
	> 6,000 rpm			
QUARTZ CRYSTAL				
RESOLVER & SYNCHROS				
DELAY LINE	R L C			
	Quartz			
				13.300

MRL 70-1024

MRL RELIABILITY ESTIMATE

ITEM NO.	ASSEMBLY NO. 917445-2
PREPARED	DATE
APPROVED	
JOB/EQUIPMENT: MX - 450	ASSEMBLY NAME: POWER BOOST ATTEN. SW. AMPL
NEXT ASSEMBLY	PAGE OF

COMPONENTS	TYPE	QUANT	F.R./10⁶ HR	TOTAL F.R.
RESISTORS	Compos.	6	0.018	0.108
	Film	7	0.156	1.092
	Film Pwr			
	Wire Wnd			
POTS	Film			
	Wire Wnd			
FIXED CAPACITOR	Tantalum			
	Electroly			
	MICA	7	0.005	0.035
VARIABLE CAPACITOR	Vacuum			
TRANSFORMER	Filament			
	Power			
	Lo Pwr Pls			
ELECTRON TUBES	Receiver			
	Pwr Rect			
	Xmtr			
C.R.T.'S	1 - Gun			
	3 - Gun			
KLYSTRONS				
THYRATRONS				
MAGNETRONS				
T.W.T.'S				
AMPLITRONS				
TR OR ATR				
DUPLEXER				
MICROWAVE DIODE	Mixer			
	Detector			
MICROWAVE COMPONENTS	Attenuat			
	Direct Cpl			
	Loads			
	Stubs			
	Feed Horn			
	Rotary Jt			
FERRITE DEVICES	Isolator			
	Circulator			
	Modulator			
	Shifter			
RF FILTERS				
HI VOLTAGE DIODE PACK	Hi Power			
	Med Power			
PULSE FORM NETWORK	Lo Volt			
	Hi Volt			

COMPONENTS	TYPE	QUANT	F.R./10⁶ HR	TOTAL F.R.
TRANSISTOR	NPN	4	1.320	5.280
	PNP	3	3.040	9.120
DIODES	General & Computer			
	Rectifier			
	Zener	2	1.260	2.520
MICROCIRCUITS				
CONNECTORS	Coax	2	0.160	0.320
	≤ 25 Pin			
	> 25 Pin			
INDUCTORS	DC Filter			
	RF & Chok			
	Cho React			
RELAYS				
SWITCHES	No Lamp			
SWITCH/LAMP ASSEMBLY	1 - Lamp			
	2 - Lamp			
	4 - Lamp			
INDICATOR (NON SWITCH)	1 - Lamp			
	2 - Lamp			
	4 - Lamp			
MOTORS FANS BLOWER — BRUSH-LESS	≤ 6,000 rpm			
	> 6,000 rpm			
MOTORS FANS BLOWER — BRUSH-TYPE	≤ 6,000 rpm			
	> 6,000 rpm			
QUARTZ CRYSTAL				
RESOLVER & SYNCHROS				
DELAY LINE	R L C			
	Quartz			
				18.475

MRL 70-1024

MRL RELIABILITY ESTIMATE

PREPARED	DATE	JOB/EQUIPMENT MK - 250	ITEM NO.
APPROVED			ASSEMBLY NO. 917445-3
			ASSEMBLY NAME SYNC GEN. POWER BOOST
			NEXT ASSEMBLY
			PAGE OF

COMPONENTS	TYPE	QUANT	F.R./10^6 HR	TOTAL F.R.
RESISTORS	Compos.			
	Film	9	0.156	1.404
	Film Pwr			
	Wire Wnd			
POTS	Film			
	Wire Wnd			
FIXED CAPACITOR	Tantalum	2	1.200	2.400
	Electroly			
	CERAMIC	4	0.025	0.100
VARIABLE CAPACITOR	Vacuum			
TRANSFORMER	Filament			
	Power			
	Lo Pwr Pls			
ELECTRON TUBES	Receiver			
	Pwr Rect			
	Xmtr			
C.R.T.'S	1 - Gun			
	3 - Gun			
KLYSTRONS				
THYRATRONS				
MAGNETRONS				
T.W.T.'S				
AMPLITRONS				
TR OR ATR				
DUPLEXER				
MICROWAVE DIODE	Mixer			
	Detector			
MICROWAVE COMPONENTS	Attenuat			
	Direct Cpl			
	Loads			
	Stubs			
	Feed Horn			
	Rotary Jt			
FERRITE DEVICES	Isolator			
	Circulator			
	Modulator			
	Shifter			
RF FILTERS				
HI VOLTAGE DIODE PACK	Hi Power			
	Med Power			
PULSE FORM NETWORK	Lo Volt			
	Hi Volt			

COMPONENTS	TYPE	QUANT	F.R./10^6 HR	TOTAL F.R.
TRANSISTOR	NPN	4	1.320	5.280
DIODES	General & Computer	2	0.413	0.826
	Rectifier			
	Zener			
MICROCIRCUITS	DIGITAL	2	0.115	0.230
CONNECTORS	Coax			
	≤ 25 Pin			
	> 25 Pin			
INDUCTORS	DC Filter			
	RF & Chok			
	Chg React			
RELAYS				
SWITCHES	No Lamp			
SWITCH/LAMP ASSEMBLY	1 - Lamp			
	2 - Lamp			
	4 - Lamp			
INDICATOR (NON SWITCH)	1 - Lamp			
	2 - Lamp			
	4 - Lamp			
MOTORS FANS BLOWER — BRUSH-LESS	≤ 6,000 rpm			
	> 6,000 rpm			
MOTORS FANS BLOWER — BRUSH-TYPE	≤ 6,000 rpm			
	> 6,000 rpm			
QUARTZ CRYSTAL				
RESOLVER & SYNCHROS				
DELAY LINE	R L C			
	Quartz			
MICROCIRCUIT	LINEAR	2	0.900	1.800
				11.020

MRL 70-1024

MRL RELIABILITY ESTIMATE

ITEM NO.	ASSEMBLY NO. 717446
PREPARED	DATE
APPROVED	
JOB/EQUIPMENT	MX-450
ASSEMBLY NAME	FREQUENCY SYNTHESIZER 1
NEXT ASSEMBLY	PAGE OF

COMPONENTS	TYPE	QUANT	F.R./10^6 HR	TOTAL F.R.
RESISTORS	Compos.	3	0.0351	0.1054
	Film	44	0.156	6.864
	Film Pwr			
	Wire Wnd			
POTS	Film	2	9.360	18.720
	Wire Wnd			
FIXED CAPACITOR	Tantalum			
	MICA	6	0.005	0.030
	CERAMIC	34	0.025	0.850
VARIABLE CAPACITOR	Vacuum	5	0.006	0.030
TRANSFORMER	Filament			
	Power			
	Lo Pwr Pls			
ELECTRON TUBES	Receiver			
	Pwr Rect			
	Xmtr			
C.R.T.'S	1 - Gun			
	3 - Gun			
KLYSTRONS				
THYRATRONS				
MAGNETRONS				
T.W.T.'S				
AMPLITRONS				
TR OR ATR				
DUPLEXER				
MICROWAVE DIODE	Mixer			
	Detector			
MICROWAVE COMPONENTS	Attenuat			
	Direct Cpl			
	Loads			
	Stubs			
	Feed Horn			
	Rotary Jt			
FERRITE DEVICES	Isolator			
	Circulator			
	Modulator			
	Shifter			
RF FILTERS				
HI VOLTAGE DIODE PACK	Hi Power			
	Med Power			
PULSE FORM NETWORK	Lo Volt			
	Hi Volt			

COMPONENTS	TYPE	QUANT	F.R./10^6 HR	TOTAL F.R.
TRANSISTOR	NPN	12	1.320	15.840
	PWR	3	2.640	7.920
DIODES	General & Computer			
	HP	3	2.200	6.600
	Zener			
MICROCIRCUITS	DIGITAL	1	0.115	0.115
CONNECTORS	Coax			
	≤ 25 Pin			
	> 25 Pin			
INDUCTORS	DC Filter			
	RF & Chok	17	0.225	3.825
	Chg React			
RELAYS				
SWITCHES	No Lamp			
SWITCH/LAMP ASSEMBLY	1 - Lamp			
	2 - Lamp			
	4 - Lamp			
INDICATOR (NON SWITCH)	1 - Lamp			
	2 - Lamp			
	4 - Lamp			
MOTORS FANS BLOWER — BRUSH-LESS	≤ 6,000 rpm			
	> 6,000 rpm			
MOTORS FANS BLOWER — BRUSH-TYPE	≤ 6,000 rpm			
	> 6,000 rpm			
QUARTZ CRYSTAL				
RESOLVER & SYNCHROS				
DELAY LINE	RLC			
	Quartz			
POWER DIVIDER	DS-109	2	0.436	0.872
XTAL FILTER		2	0.184	0.368
MIXER		3	1.514	4.542
MICROCIRCUIT	MECL II	1	0.100	0.100
	MECL III	2	0.560	1.120
				67.930

MRL 70-1024

MRL RELIABILITY ESTIMATE

PREPARED	DATE	JOB/EQUIPMENT: MX-450	ITEM NO. / ASSEMBLY NO.
APPROVED			ASSEMBLY NAME: MX-450 POWER SUPPLY
			NEXT ASSEMBLY / PAGE OF

COMPONENTS	TYPE	QUANT	F.R./10^6 HR	TOTAL F.R.
RESISTORS	Compos.			
	Film			
	Film Pwr			
	Wire Wnd			
POTS	Film			
	Wire Wnd			
FIXED CAPACITOR	Tantalum			
	Electroly			
	Pcl...	1	0.034	0.034
VARIABLE CAPACITOR	Vacuum			
	[illegible]			
TRANSFORMER	Filament			
	Power			
	Lo Pwr Pls			
ELECTRON TUBES	Receiver			
	Pwr Rect			
	Xmtr			
C.R.T.'S	1 - Gun			
	3 - Gun			
KLYSTRONS				
THYRATRONS				
MAGNETRONS				
T.W.T.'S				
AMPLITRON'				
TR OR ATR				
DUPLEXER				
MICROWAVE DIODE	Mixer			
	Detector			
MICROWAVE COMPONENTS	Attenuat			
	Direct Cpl			
	Loads			
	Stubs			
	Feed Horn			
	Rotary Jt			
FERRITE DEVICES	Isolator			
	Circulator			
	Modulator			
	Shifter			
RF FILTERS				
HI VOLTAGE DIODE PACK	Hi Power			
	Med Power			
PULSE FORM NETWORK	Lo Volt			
	Hi Volt			

COMPONENTS	TYPE	QUANT	F.R./10^6 HR	TOTAL F.R.
TRANSISTOR				
DIODES	General & Computer			
	Rectifier	1	1.560	1.560
	Zener			
MICROCIRCUITS				
CONNECTORS	Coax			
	≤ 25 Pin	1	2.160	2.160
	> 25 Pin	2	3.420	6.840
INDUCTORS	DC Filter			
	RF & Chok			
	Chg React			
RELAYS		2	1.400	2.800
SWITCHES	No Lamp	4	0.500	2.000
SWITCH/LAMP ASSEMBLY	1 - Lamp			
	2 - Lamp			
	4 - Lamp			
INDICATOR (NON SWITCH)	1 - Lamp			
	2 - Lamp			
	4 - Lamp			
MOTORS FANS BLOWER — BRUSHLESS	≤ 6,000 rpm	1	9.000	9.000
	> 6,000 rpm			
MOTORS FANS BLOWER — BRUSH-TYPE	≤ 6,000 rpm			
	> 6,000 rpm			
QUARTZ CRYSTAL				
RESOLVER & SYNCHROS				
DELAY LINE	RLC			
	Quartz			
POWER SUPPLY	HFC	4	28.571	114.284
CONVERTER	BATAC	1	43.730	43.730
				182.408

MRL 70-1024

MRL RELIABILITY ESTIMATE

ITEM NO.		ASSEMBLY NO.	
PREPARED	DATE	JOB/EQUIPMENT: MK - 450	ASSEMBLY NAME: OSCILLATOR ASSY
APPROVED			NEXT ASSEMBLY / PAGE OF

COMPONENTS	TYPE	QUANT	F.R./10^6 HR	TOTAL F.R.
RESISTORS	Compos.			
	Film			
	Film Pwr			
	Wire Wnd			
POTS	Film			
	Wire Wnd			
FIXED CAPACITOR	Tantalum			
	Electroly			
VARIABLE CAPACITOR	Vacuum			
TRANSFORMER	Filament			
	Power			
	Lo Pwr Pls			
ELECTRON TUBES	Receiver			
	Pwr Rect			
	Xmtr			
C.R.T.'S	1 - Gun			
	3 - Gun			
KLYSTRONS				
THYRATRONS				
MAGNETRONS				
T.W.T.'S				
AMPLITRONS				
TR OR ATR				
DUPLEXER				
MICROWAVE DIODE	Mixer			
	Detector			
MICROWAVE COMPONENTS	Attenuat			
	Direct Cpl			
	Loads			
	Stubs			
	Feed Horn			
	Rotary Jt			
FERRITE DEVICES	Isolator			
	Circulator			
	Modulator			
	Shifter			
RF FILTERS				
HI VOLTAGE DIODE PACK	Hi Power			
	Med Power			
PULSE FORM NETWORK	Lo Volt			
	Hi Volt			

COMPONENTS	TYPE	QUANT	F.R./10^6 HR	TOTAL F.R.
TRANSISTOR				
DIODES	General & Computer			
	Rectifier			
	Zener			
MICROCIRCUITS				
CONNECTORS	Coax			
	≤ 25 Pin			
	> 25 Pin			
INDUCTORS	DC Filter			
	RF & Chok			
	Chg React			
RELAYS				
SWITCHES	No Lamp			
SWITCH/LAMP ASSEMBLY	1 - Lamp			
	2 - Lamp			
	4 - Lamp			
INDICATOR (NON SWITCH)	1 - Lamp			
	2 - Lamp			
	4 - Lamp			
MOTORS FANS BLOWER — BRUSH-LESS	< 6,000 rpm			
	> 6,000 rpm			
MOTORS FANS BLOWER — BRUSH-TYPE	< 6,000 rpm			
	> 6,000 rpm			
QUARTZ CRYSTAL				
RESOLVER & SYNCHROS				
DELAY LINE	R L C			
	Quartz			
OSCILLATOR	625111	1	8.470	8.470
				8.470

MRL 70-1024

MRL RELIABILITY ESTIMATE

PREPARED	DATE	JOB/EQUIPMENT MK-450	ITEM NO. / ASSEMBLY NO.
APPROVED			ASSEMBLY NAME AUXILLARY UNIT
			NEXT ASSEMBLY / PAGE OF

COMPONENTS	TYPE	QUANT	F.R./10^6 HR	TOTAL F.R.
RESISTORS	Compos.			
	Film			
	Film Pwr			
	Wire Wnd			
POTS	Film			
	Wire Wnd			
FIXED CAPACITOR	Tantalum			
	Electroly			
	Other	1	0.1034	0.1034
VARIABLE CAPACITOR	Vacuum			
	Other			
TRANSFORMER	Filament			
	Power			
	Lo Pwr Pls			
ELECTRON TUBES	Receiver			
	Pwr Rect			
	Xmtr			
C.R.T.'S	1 - Gun			
	3 - Gun			
KLYSTRONS				
THYRATRONS				
MAGNETRONS				
T.W.T.'S				
AMPLITRONS				
TR OR ATR				
DUPLEXER				
MICROWAVE DIODE	Mixer			
	Detector			
MICROWAVE COMPONENTS	Attenuat			
	Direct Cpl			
	Loads			
	Stubs			
	Feed Horn			
	Rotary Jt			
FERRITE DEVICES	Isolator			
	Circulator			
	Modulator			
	Shifter			
RF FILTERS				
HI VOLTAGE DIODE PACK	Hi Power			
	Med Power			
PULSE FORM NETWORK	Lo Volt			
	Hi Volt			

COMPONENTS	TYPE	QUANT	F.R./10^6 HR	TOTAL F.R.
TRANSISTOR	Silicon			
	Germanium			
DIODES	General & Computer			
	Rectifier			
	Zener			
MICROCIRCUITS				
CONNECTORS	Coax	5	0.160	0.800
	≤ 25 Pin	2	2.160	4.320
	> 25 Pin	3	3.420	10.260
INDUCTORS	DC Filter			
	RF & Chok			
	Chg React			
RELAYS				
SWITCHES	No Lamp			
SWITCH/LAMP ASSEMBLY	1 - Lamp			
	2 - Lamp			
	4 - Lamp			
INDICATOR (NON SWITCH)	1 - Lamp			
	2 - Lamp			
	4 - Lamp			
MOTORS FANS BLOWER — BRUSHLESS	≤ 6,000 rpm	1	9.000	9.000
	> 6,000 rpm			
MOTORS FANS BLOWER — BRUSH-TYPE	≤ 6,000 rpm			
	> 6,000 rpm			
QUARTZ CRYSTAL				
RESOLVER & SYNCHROS				
DELAY LINE	R L C			
	Quartz			
CONVERTER	BATAC	1	43.730	43.730
				68.144

MRL 70-1024

MRL RELIABILITY ESTIMATE			ITEM NO.	ASSEMBLY NO. 917781
PREPARED	DATE	JOB/EQUIPMENT	ASSEMBLY NAME SIGNAL PROCESSOR ASSY	
APPROVED			NEXT ASSEMBLY	PAGE OF

COMPONENTS	TYPE	QUANT	F.R./10^6 HR	TOTAL F.R.
RESISTORS	Compos.			
	Film			
	Film Pwr			
	Wire Wnd			
POTS	Film			
	Wire Wnd			
FIXED CAPACITOR	Tantalum			
	Electroly			
	Poly	2	0.034	0.068
VARIABLE CAPACITOR	Vacuum			
TRANSFORMER	Filament			
	Power			
	Lo Pwr Pls			
ELECTRON TUBES	Receiver			
	Pwr Rect			
	Xmtr			
C.R.T.'S	1 - Gun			
	3 - Gun			
KLYSTRONS				
THYRATRONS				
MAGNETRONS				
T.W.T.'S				
AMPLITRONS				
TR OR ATR				
DUPLEXER				
MICROWAVE DIODE	Mixer			
	Detector			
MICROWAVE COMPONENTS	Attenuat			
	Direct Cpl			
	Loads			
	Stubs			
	Feed Horn			
	Rotary Jt			
FERRITE DEVICES	Isolator			
	Circulator			
	Modulator			
	Shifter			
RF FILTERS				
HI VOLTAGE DIODE PACK	Hi Power			
	Med Power			
PULSE FORM NETWORK	Lo Volt			
	Hi Volt			

COMPONENTS	TYPE	QUANT	F.R./10^6 HR	TOTAL F.R.
TRANSISTOR				
DIODES	General & Computer			
	Rectifier			
	Zener			
MICROCIRCUITS				
CONNECTORS	Coax	76	0.160	12.160
	≤ 25 Pin	40	2.160	86.400
	> 25 Pin	4	3.420	13.680
INDUCTORS	DC Filter			
	RF & Chok			
	Chg React			
RELAYS				
SWITCHES	No Lamp			
SWITCH/LAMP ASSEMBLY	1 - Lamp			
	2 - Lamp			
	4 - Lamp			
INDICATOR (NON SWITCH)	1 - Lamp			
	2 - Lamp			
	4 - Lamp			
MOTORS FANS BLOWER — BRUSHLESS	≤ 6,000 rpm	1	9.000	9.000
	> 6,000 rpm			
MOTORS FANS BLOWER — BRUSH-TYPE	≤ 6,000 rpm			
	> 6,000 rpm			
QUARTZ CRYSTAL				
RESOLVER & SYNCHROS				
DELAY LINE	RLC			
	Quartz			
CONVERTER	BATAC	1	43.730	43.730
				165.038

MRL 70-1024

MRL RELIABILITY ESTIMATE

PREPARED	DATE	JOB/EQUIPMENT: MX-150	ITEM NO.
APPROVED			ASSEMBLY NO. 917423
			ASSEMBLY NAME: CORRELATOR/LOCAL REFERENCE
			NEXT ASSEMBLY / PAGE OF

COMPONENTS	TYPE	QUANT	F.R./10^6 HR	TOTAL F.R.
RESISTORS	Compos.	3	0.018	0.054
	Film	44	0.156	6.864
	Film Pwr			
	Wire Wnd			
POTS	Film	1	9.360	9.360
	Wire Wnd			
FIXED CAPACITOR	Tantalum	4	1.200	4.800
	MICA	10	0.005	0.050
	CERAMIC	26	0.025	0.650
VARIABLE CAPACITOR	Vacuum	3	0.006	0.018
	CERAMIC	1	0.006	0.006
TRANSFORMER	Filament			
	Power			
	Lo Pwr Pls	1	0.304	0.304
ELECTRON TUBES	Receiver			
	Pwr Rect			
	Xmtr			
C.R.T.'S	1 - Gun			
	3 - Gun			
KLYSTRONS				
THYRATRONS				
MAGNETRONS				
T.W.T.'S				
AMPLITRONS				
TR OR ATR				
DUPLEXER				
MICROWAVE DIODE	Mixer			
	Detector			
MICROWAVE COMPONENTS	Attenuat			
	Direct Cpl			
	Loads			
	Stubs			
	Feed Horn			
	Rotary Jt			
FERRITE DEVICES	Isolator			
	Circulator			
	Modulator			
	Shifter			
RF FILTERS				
HI VOLTAGE DIODE PACK	Hi Power			
	Med Power			
PULSE FORM NETWORK	Lo Volt			
	Hi Volt			

COMPONENTS	TYPE	QUANT	F.R./10^6 HR	TOTAL F.R.
TRANSISTOR	NPN	5	1.320	6.600
DIODES	General & Computer	2	0.413	0.826
	HP	3	2.200	6.600
	Zener	3	1.260	3.780
MICROCIRCUITS	LINEAR	1	0.400	0.400
CONNECTORS	Coax	4	0.160	0.640
	≤ 25 Pin			
	> 25 Pin			
INDUCTORS	DC Filter			
	RF & Chok	12	0.225	2.700
	Chg React			
RELAYS				
SWITCHES	No Lamp			
SWITCH/LAMP ASSEMBLY	1 - Lamp			
	2 - Lamp			
	4 - Lamp			
INDICATOR (NON SWITCH)	1 - Lamp			
	2 - Lamp			
	4 - Lamp			
MOTORS FANS BLOWER — BRUSH-LESS	≤ 6,000 rpm			
	> 6,000 rpm			
MOTORS FANS BLOWER — BRUSH-TYPE	≤ 6,000 rpm			
	> 6,000 rpm			
QUARTZ CRYSTAL				
RESOLVER & SYNCHROS				
DELAY LINE	RLC			
	Quartz			
MICROCIRCUIT	MECL II	9	0.100	0.900
	MECL III	7	0.600	4.200
MIXER		7	1.514	10.598
POWER DIVIDER		2	0.436	0.872
				60.222

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MRL RELIABILITY ESTIMATE

ITEM NO.	
ASSEMBLY NO.	917432
ASSEMBLY NAME	IF ASSEMBLY
NEXT ASSEMBLY	
PAGE OF	
PREPARED	
DATE	
APPROVED	
JOB/EQUIPMENT	MX-450

COMPONENTS	TYPE	QUANT	F.R./10^6 HR	TOTAL F.R.
RESISTORS	Compos.			
	Film	23	0.156	3.588
	Film Pwr			
	Wire Wnd			
POTS	Film	1	9.360	9.360
	Wire Wnd			
FIXED CAPACITOR	Tantalum	2	1.200	2.400
	Electroly			
	CERAMIC	22	0.025	0.550
VARIABLE CAPACITOR	Vacuum			
	CERAMIC	2	0.006	0.012
TRANSFORMER	Filament			
	Power			
	Lo Pwr Pls			
ELECTRON TUBES	Receiver			
	Pwr Rect			
	Xmtr			
C.R.T.'S	1 - Gun			
	3 - Gun			
KLYSTRONS				
THYRATRONS				
MAGNETRONS				
T.W.T.'S				
AMPLITRONS				
TR OR ATR				
DUPLEXER				
MICROWAVE DIODE	Mixer			
	Detector			
MICROWAVE COMPONENTS	Attenuat			
	Direct Cpl			
	Loads			
	Stubs			
	Feed Horn			
	Rotary Jt			
FERRITE DEVICES	Isolator			
	Circulator			
	Modulator			
	Shifter			
RF FILTERS				
HI VOLTAGE DIODE PACK	Hi Power			
	Med Power			
PULSE FORM NETWORK	Lo Volt			
	Hi Volt			

COMPONENTS	TYPE	QUANT	F.R./10^6 HR	TOTAL F.R.
TRANSISTOR	NPN	1	1.320	1.320
DIODES	General & Computer			
	Rectifier			
	Zener			
MICROCIRCUITS	LINEAR	1	0.450	0.450
CONNECTORS	Coax			
	≤ 25 Pin			
	> 25 Pin			
INDUCTORS	DC Filter			
	RF & Chok	2	0.225	0.450
	Chg React			
RELAYS				
SWITCHES	No Lamp			
SWITCH/LAMP ASSEMBLY	1 - Lamp			
	2 - Lamp			
	4 - Lamp			
INDICATOR (NON SWITCH)	1 - Lamp			
	2 - Lamp			
	4 - Lamp			
MOTORS FANS BLOWER — BRUSH-LESS	≤ 6,000 rpm			
	> 6,000 rpm			
MOTORS FANS BLOWER — BRUSH-TYPE	≤ 6,000 rpm			
	> 6,000 rpm			
QUARTZ CRYSTAL				
RESOLVER & SYNCHROS				
DELAY LINE	R L C			
	Quartz			
RF AMPL		6	4.000	24.000
MIXER		4	1.514	6.056
POWER DIVIDER		1	0.436	0.436
XTAL FILTER		2	0.184	0.368
				48.940

MRL 70-1024

MRL RELIABILITY ESTIMATE

ITEM NO.	
ASSEMBLY NO.	917825
PREPARED	
DATE	
APPROVED	
JOB/EQUIPMENT	MX-450
ASSEMBLY NAME	POST CORRELATION RCVR 1
NEXT ASSEMBLY	
PAGE OF	

COMPONENTS	TYPE	QUANT	F.R./10^6 HR	TOTAL F.R.
RESISTORS	Compos.	11	0.018	0.198
	Film	113	0.156	17.628
	Film Pwr			
	Wire Wnd			
POTS	Film	6	9.360	56.160
	Wire Wnd			
FIXED CAPACITOR	Tantalum	3	1.200	3.600
	Electroly			
	CERAMIC	46	0.025	1.150
VARIABLE CAPACITOR	Vacuum			
TRANSFORMER	Filament			
	Power			
	Lo Pwr Pls	3	0.304	0.912
ELECTRON TUBES	Receiver			
	Pwr Rect			
	Xmtr			
C.R.T.'S	1 - Gun			
	3 - Gun			
KLYSTRONS				
THYRATRONS				
MAGNETRONS				
T.W.T.'S				
AMPLITRONS				
TR OR ATR				
DUPLEXER				
MICROWAVE DIODE	Mixer			
	Detector			
MICROWAVE COMPONENTS	Attenuat			
	Direct Cpl			
	Loads			
	Stubs			
	Feed Horn			
	Rotary Jt			
FERRITE DEVICES	Isolator			
	Circulator			
	Modulator			
	Shifter			
RF FILTERS				
HI VOLTAGE DIODE PACK	Hi Power			
	Med Power			
PULSE FORM NETWORK	Lo Volt			
	Hi Volt			

COMPONENTS	TYPE	QUANT	F.R./10^6 HR	TOTAL F.R.
TRANSISTOR	NPN	8	1.320	10.560
	PNP	4	3.040	12.160
DIODES	General & Computer	14	0.413	5.782
	Rectifier			
	Zener	7	1.260	8.820
MICROCIRCUITS	DIGITAL	5	0.115	0.575
CONNECTORS	Coax			
	≤ 25 Pin			
	> 25 Pin			
INDUCTORS	DC Filter			
	RF & Chok			
	Chg React			
RELAYS				
SWITCHES	No Lamp			
SWITCH/LAMP ASSEMBLY	1 - Lamp			
	2 - Lamp			
	4 - Lamp			
INDICATOR (NON SWITCH)	1 - Lamp			
	2 - Lamp			
	4 - Lamp			
MOTORS FANS BLOWER — BRUSH-LESS	≤ 6,000 rpm			
	> 6,000 rpm			
MOTORS FANS BLOWER — BRUSH-TYPE	≤ 6,000 rpm			
	> 6,000 rpm			
QUARTZ CRYSTAL				
RESOLVER & SYNCHROS				
DELAY LINE	RLC			
	Quartz			
MICROCIRCUIT	LINEAR	21	0.400	8.400
TRANSISTOR	FET	10	3.040	30.400
				156.345

MRL 70-1024

MRL RELIABILITY ESTIMATE			ITEM NO.	ASSEMBLY NO. 917427
PREPARED	DATE	JOB/EQUIPMENT	ASSEMBLY NAME A/D CONVERTER	
APPROVED		MX-050	NEXT ASSEMBLY	PAGE OF

COMPONENTS	TYPE	QUANT	F.R./10^6 HR	TOTAL F.R.
RESISTORS	Compos.			
	Film	5	0.156	0.780
	Film Pwr			
	Wire Wnd			
POTS	Film	1	9.360	9.360
	Wire Wnd			
FIXED CAPACITOR	Tantalum	3	1.200	3.600
	Electroly			
	CERAMIC	3	0.025	0.075
VARIABLE CAPACITOR	Vacuum			
TRANSFORMER	Filament			
	Power			
	Lo Pwr Pls			
ELECTRON TUBES	Receiver			
	Pwr Rect			
	Xmtr			
C.R.T.'S	1 - Gun			
	3 - Gun			
KLYSTRONS				
THYRATRONS				
MAGNETRONS				
T.W.T.'S				
AMPLITRONS				
TR OR ATR				
DUPLEXER				
MICROWAVE DIODE	Mixer			
	Detector			
MICROWAVE COMPONENTS	Attenuat			
	Direct Cpl			
	Loads			
	Stubs			
	Feed Horn			
	Rotary Jt			
FERRITE DEVICES	Isolator			
	Circulator			
	Modulator			
	Shifter			
RF FILTERS				
HI VOLTAGE DIODE PACK	Hi Power			
	Med Power			
PULSE FORM NETWORK	Lo Volt			
	Hi Volt			

COMPONENTS	TYPE	QUANT	F.R./10^6 HR	TOTAL F.R.
TRANSISTOR	NPN	1	1.320	1.320
DIODES	General & Computer			
	Rectifier			
	Zener			
MICROCIRCUITS	DIGITAL	5	0.115	0.575
CONNECTORS	Coax			
	≤ 25 Pin			
	> 25 Pin			
INDUCTORS	DC Filter			
	RF & Chok			
	Chg React			
RELAYS		1	2.550	2.550
SWITCHES	No Lamp			
SWITCH/LAMP ASSEMBLY	1 - Lamp			
	2 - Lamp			
	4 - Lamp			
INDICATOR (NON SWITCH)	1 - Lamp			
	2 - Lamp			
	4 - Lamp			
MOTORS FANS BLOWER — BRUSH-LESS	≤ 6,000 rpm			
	> 6,000 rpm			
MOTORS FANS BLOWER — BRUSH-TYPE	≤ 6,000 rpm			
	> 6,000 rpm			
QUARTZ CRYSTAL				
RESOLVER & SYNCHROS				
DELAY LINE	RLC			
	Quartz			
MICROCIRCUIT	LINEAR	3	0.400	1.200
				19.460

MRL 70-1024

MRL RELIABILITY ESTIMATE

PREPARED	DATE	JOB/EQUIPMENT: MY-450	ITEM NO.
APPROVED			ASSEMBLY NO. 9174-6
			ASSEMBLY NAME: P.C. RECEIVER 2
			NEXT ASSEMBLY
			PAGE OF

COMPONENTS	TYPE	QUANT	F.R./10^6 HR	TOTAL F.R.
RESISTORS	Compos.			
	Film	39	0.156	6.084
	Film Pwr			
	Wire Wnd			
POTS	Film	3	9.360	28.080
	Wire Wnd			
FIXED CAPACITOR	Tantalum	4	1.250	4.950
	MICA	3	0.005	0.015
	CERAMIC	11	0.025	0.275
VARIABLE CAPACITOR	Vacuum			
TRANSFORMER	Filament			
	Power			
	Lo Pwr Pls			
ELECTRON TUBES	Receiver			
	Pwr Rect			
	Xmtr			
C.R.T.'S	1 - Gun			
	3 - Gun			
KLYSTRONS				
THYRATRONS				
MAGNETRONS				
T.W.T.'S				
AMPLITRONS				
TR OR ATR				
DUPLEXER				
MICROWAVE DIODE	Mixer			
	Detector			
MICROWAVE COMPONENTS	Attenuat			
	Direct Cpl			
	Loads			
	Stubs			
	Feed Horn			
	Rotary Jt			
FERRITE DEVICES	Isolator			
	Circulator			
	Modulator			
	Shifter			
RF FILTERS				
HI VOLTAGE DIODE PACK	Hi Power			
	Med Power			
PULSE FORM NETWORK	Lo Volt			
	Hi Volt			

COMPONENTS	TYPE	QUANT	F.R./10^6 HR	TOTAL F.R.
TRANSISTOR	NPN	1	1.320	1.320
	PNP	6	3.040	18.240
DIODES	General & Computer	16	0.413	6.608
	Rectifier			
	Zener	8	1.260	10.080
MICROCIRCUITS	DIGITAL	32	0.115	3.680
CONNECTORS	Coax			
	≤ 25 Pin			
	> 25 Pin			
INDUCTORS	DC Filter			
	RF & Chok			
	Chg React			
RELAYS				
SWITCHES	No Lamp			
SWITCH/LAMP ASSEMBLY	1 - Lamp			
	2 - Lamp			
	4 - Lamp			
INDICATOR (NON SWITCH)	1 - Lamp			
	2 - Lamp			
	4 - Lamp			
MOTORS FANS BLOWER — BRUSH-LESS	≤ 6,000 rpm			
	> 6,000 rpm			
MOTORS FANS BLOWER — BRUSH-TYPE	≤ 6,000 rpm			
	> 6,000 rpm			
QUARTZ CRYSTAL				
RESOLVER & SYNCHROS				
DELAY LINE	RLC			
	Quartz			
MICROCIRCUIT	LINEAR	6	0.400	2.400
TRANSISTOR	FET	3	3.040	9.120

70.102

MRL 70-1024

MRL RELIABILITY ESTIMATE

ITEM NO.	
ASSEMBLY NO.	917423
PREPARED	
DATE	
APPROVED	
JOB/EQUIPMENT	MX-450
ASSEMBLY NAME	DIGITAL FILTER
NEXT ASSEMBLY	
PAGE OF	

COMPONENTS	TYPE	QUANT	F.R./10^6 HR	TOTAL F.R.
RESISTORS	Compos.			
	Film	22	0.156	3.432
	Film Pwr			
	Wire Wnd			
POTS	Film			
	Wire Wnd			
FIXED CAPACITOR	Tantalum			
	Electroly			
	CERAMIC	6	0.025	0.150
VARIABLE CAPACITOR	Vacuum			
TRANSFORMER	Filament			
	Power			
	Lo Pwr Pls			
ELECTRON TUBES	Receiver			
	Pwr Rect			
	Xmtr			
C.R.T.'S	1 - Gun			
	3 - Gun			
KLYSTRONS				
THYRATRONS				
MAGNETRONS				
T.W.T.'S				
AMPLITRONS				
TR OR ATR				
DUPLEXER				
MICROWAVE DIODE	Mixer			
	Detector			
MICROWAVE COMPONENTS	Attenuat			
	Direct Cpl			
	Loads			
	Stubs			
	Feed Horn			
	Rotary Jt			
FERRITE DEVICES	Isolator			
	Circulator			
	Modulator			
	Shifter			
RF FILTERS				
HI VOLTAGE DIODE PACK	Hi Power			
	Med Power			
PULSE FORM NETWORK	Lo Volt			
	Hi Volt			

COMPONENTS	TYPE	QUANT	F.R./10^6 HR	TOTAL F.R.
TRANSISTOR				
DIODES	General & Computer			
	Rectifier			
	Zener	1	1.260	1.260
MICROCIRCUITS	DIGITAL	35	0.115	4.025
CONNECTORS	Coax			
	≤ 25 Pin			
	> 25 Pin			
INDUCTORS	DC Filter			
	RF & Chok	1	0.225	0.225
	Chg React			
RELAYS				
SWITCHES	No Lamp			
SWITCH/LAMP ASSEMBLY	1 - Lamp			
	2 - Lamp			
	4 - Lamp			
INDICATOR (NON SWITCH)	1 - Lamp			
	2 - Lamp			
	4 - Lamp			
MOTORS FANS BLOWER — BRUSH-LESS	≤ 6,000 rpm			
	> 6,000 rpm			
MOTORS FANS BLOWER — BRUSH-TYPE	≤ 6,000 rpm			
	> 6,000 rpm			
QUARTZ CRYSTAL				
RESOLVER & SYNCHROS				
DELAY LINE	R L C			
	Quartz			
				9.092

MRL 70-1024

MRL RELIABILITY ESTIMATE

PREPARED	DATE	JOB/EQUIPMENT	ITEM NO.	ASSEMBLY NO.
		MX-450		917442
APPROVED			ASSEMBLY NAME: FILTER TIMER	
			NEXT ASSEMBLY	PAGE OF

COMPONENTS	TYPE	QUANT	F.R./10^6 HR	TOTAL F.R.
RESISTORS	Compos.			
	Film	4	0.156	0.624
	Film Pwr			
	Wire Wnd			
POTS	Film			
	Wire Wnd			
FIXED CAPACITOR	Tantalum			
	Electroly			
	CERAMIC	4	0.025	0.100
VARIABLE CAPACITOR	Vacuum			
TRANSFORMER	Filament			
	Power			
	Lo Pwr Pls			
ELECTRON TUBES	Receiver			
	Pwr Rect			
	Xmtr			
C.R.T.'S	1 - Gun			
	3 - Gun			
KLYSTRONS				
THYRATRONS				
MAGNETRONS				
T.W.T.'S				
AMPLITRONS				
TR OR ATR				
DUPLEXER				
MICROWAVE DIODE	Mixer			
	Detector			
MICROWAVE COMPONENTS	Attenuat			
	Direct Cpl			
	Loads			
	Stubs			
	Feed Horn			
	Rotary Jt			
FERRITE DEVICES	Isolator			
	Circulator			
	Modulator			
	Shifter			
RF FILTERS				
HI VOLTAGE DIODE PACK	Hi Power			
	Med Power			
PULSE FORM NETWORK	Lo Volt			
	Hi Volt			

COMPONENTS	TYPE	QUANT	F.R./10^6 HR	TOTAL F.R.
TRANSISTOR				
DIODES	General & Computer			
	Rectifier			
	Zener			
MICROCIRCUITS	DIGITAL	39	0.115	4.485
CONNECTORS	Coax			
	≤ 25 Pin			
	> 25 Pin			
INDUCTORS	DC Filter			
	RF & Chok	1	0.225	0.225
	Chg React			
RELAYS				
SWITCHES	No Lamp			
SWITCH/LAMP ASSEMBLY	1 - Lamp			
	2 - Lamp			
	4 - Lamp			
INDICATOR (NON SWITCH)	1 - Lamp			
	2 - Lamp			
	4 - Lamp			
MOTORS FANS BLOWER — BRUSH-LESS	≤ 6,000 rpm			
	> 6,000 rpm			
MOTORS FANS BLOWER — BRUSH-TYPE	≤ 6,000 rpm			
	> 6,000 rpm			
QUARTZ CRYSTAL				
RESOLVER & SYNCHROS				
DELAY LINE	RLC			
	Quartz			
				5.434

MRL 70-1024

MRL RELIABILITY ESTIMATE

ITEM NO.		ASSEMBLY NO.	917427
PREPARED	DATE	JOB/EQUIPMENT: MX-450	ASSEMBLY NAME: CARRIER RATE MULTIPLIER
APPROVED			NEXT ASSEMBLY / PAGE OF

COMPONENTS	TYPE	QUANT	F.R./10^6 HR	TOTAL F.R.
RESISTORS	Compos.			
	Film	5	0.156	0.780
	Film Pwr			
	Wire Wnd			
POTS	Film			
	Wire Wnd			
FIXED CAPACITOR	Tantalum			
	Electroly			
	CERAMIC	4	0.025	0.100
VARIABLE CAPACITOR	Vacuum			
TRANSFORMER	Filament			
	Power			
	Lo Pwr Pls			
ELECTRON TUBES	Receiver			
	Pwr Rect			
	Xmtr			
C.R.T.'S	1 - Gun			
	3 - Gun			
KLYSTRONS				
THYRATRONS				
MAGNETRONS				
T.W.T. S				
AMPLITRONS				
TR OR ATR				
DUPLEXER				
MICROWAVE DIODE	Mixer			
	Detector			
MICROWAVE COMPONENTS	Attenuat			
	Direct Cpl			
	Loads			
	Stubs			
	Feed Horn			
	Rotary Jt			
FERRITE DEVICES	Isolator			
	Circulator			
	Modulator			
	Shifter			
RF FILTERS				
HI VOLTAGE DIODE PACK	Hi Power			
	Med Power			
PULSE FORM NETWORK	Lo Volt			
	Hi Volt			

COMPONENTS	TYPE	QUANT	F.R./10^6 HR	TOTAL F.R.
TRANSISTOR				
DIODES	General & Computer			
	Rectifier			
	Zener			
MICROCIRCUITS	DIGITAL	30	0.115	3.450
CONNECTORS	Coax			
	≤ 25 Pin			
	> 25 Pin			
INDUCTORS	DC Filter			
	RF & Chok	1	0.225	0.225
	Chg React			
RELAYS				
SWITCHES	No Lamp			
SWITCH/LAMP ASSEMBLY	1 - Lamp			
	2 - Lamp			
	4 - Lamp			
INDICATOR (NON SWITCH)	1 - Lamp			
	2 - Lamp			
	4 - Lamp			
MOTORS FANS BLOWER — BRUSH-LESS	≤ 6,000 rpm			
	> 6,000 rpm			
MOTORS FANS BLOWER — BRUSH-TYPE	≤ 6,000 rpm			
	> 6,000 rpm			
QUARTZ CRYSTAL				
RESOLVER & SYNCHROS				
DELAY LINE	RLC			
	Quartz			
TOTAL				4.555

MRL 70-1024

MRL RELIABILITY ESTIMATE

PREPARED	DATE	JOB/EQUIPMENT: UX-451	ITEM NO.
APPROVED			ASSEMBLY NO. 917930
			ASSEMBLY NAME: CLOCK RATE MULTIPLIER
			NEXT ASSEMBLY
			PAGE OF

COMPONENTS	TYPE	QUANT	F.R./10^6 HR	TOTAL F.R.
RESISTORS	Compos.			
	Film	5	0.156	0.780
	Film Pwr			
	Wire Wnd			
POTS	Film			
	Wire Wnd			
FIXED CAPACITOR	Tantalum			
	Electroly			
	Ceramic	4	0.025	0.100
VARIABLE CAPACITOR	Vacuum			
TRANSFORMER	Filament			
	Power			
	Lo Pwr Pls			
ELECTRON TUBES	Receiver			
	Pwr Rect			
	Xmtr			
C.R.T.'S	1 - Gun			
	3 - Gun			
KLYSTRONS				
THYRATRONS				
MAGNETRONS				
T.W.T.'S				
AMPLITRONS				
TR OR ATR				
DUPLEXER				
MICROWAVE DIODE	Mixer			
	Detector			
MICROWAVE COMPONENTS	Attenuat			
	Direct Cpl			
	Loads			
	Stubs			
	Feed Horn			
	Rotary Jt			
FERRITE DEVICES	Isolator			
	Circulator			
	Modulator			
	Shifter			
RF FILTERS				
HI VOLTAGE DIODE PACK	Hi Power			
	Med Power			
PULSE FORM NETWORK	Lo Volt			
	Hi Volt			

COMPONENTS	TYPE	QUANT	F.R./10^6 HR	TOTAL F.R.
TRANSISTOR				
DIODES	General & Computer			
	Rectifier			
	Zener			
MICROCIRCUITS	DIGITAL	22	0.115	2.530
CONNECTORS	Coax			
	≤ 25 Pin			
	> 25 Pin			
INDUCTORS	DC Filter			
	RF & Chok	1	0.225	0.225
	Chg React			
RELAYS				
SWITCHES	No Lamp			
SWITCH/LAMP ASSEMBLY	1 - Lamp			
	2 - Lamp			
	4 - Lamp			
INDICATOR (NON SWITCH)	1 - Lamp			
	2 - Lamp			
	4 - Lamp			
MOTORS FANS BLOWER — BRUSH-LESS	≤ 6,000 rpm			
	> 6,000 rpm			
MOTORS FANS BLOWER — BRUSH-TYPE	≤ 6,000 rpm			
	> 6,000 rpm			
QUARTZ CRYSTAL				
RESOLVER & SYNCHROS				
DELAY LINE	RLC			
	Quartz			
TOTAL				3.635

MRL 70-1024

MRL RELIABILITY ESTIMATE

PREPARED	DATE	JOB/EQUIPMENT MX-450	ITEM NO.
APPROVED			ASSEMBLY NO. 917431
			ASSEMBLY NAME IPM (MOTHER)
			NEXT ASSEMBLY
			PAGE OF

COMPONENTS	TYPE	QUANT	F.R./10^6 HR	TOTAL F.R.
RESISTORS	Compos.			
	Film	6	0.156	0.936
	Film Pwr			
	Wire Wnd			
POTS	Film			
	Wire Wnd			
FIXED CAPACITOR	Tantalum	3	1.200	3.600
	MICA	2	0.005	0.010
	CERAMIC	9	0.025	0.225
VARIABLE CAPACITOR	Vacuum			
	CERAMIC	1	0.006	0.006
TRANSFORMER	Filament			
	Power			
	Lo Pwr Pls			
ELECTRON TUBES	Receiver			
	Pwr Rect			
	Xmtr			
C.R.T.'S	1 - Gun			
	3 - Gun			
KLYSTRONS				
THYRATRONS				
MAGNETRONS				
T.W.T.'S				
AMPLITRONS				
TR OR ATR				
DUPLEXER				
MICROWAVE DIODE	Mixer			
	Detector			
MICROWAVE COMPONENTS	Attenuat			
	Direct Cpl			
	Loads			
	Stubs			
	Feed Horn			
	Rotary Jt			
FERRITE DEVICES	Isolator			
	Circulator			
	Modulator			
	Shifter			
RF FILTERS				
HI VOLTAGE DIODE PACK	Hi Power			
	Med Power			
PULSE FORM NETWORK	Lo Volt			
	Hi Volt			

COMPONENTS	TYPE	QUANT	F.R./10^6 HR	TOTAL F.R.
TRANSISTOR	NPN	1	1.320	1.320
DIODES	General & Computer			
	Rectifier			
	Zener			
MICROCIRCUITS				
CONNECTORS	Coax	1	0.160	0.160
	≤ 25 Pin			
	> 25 Pin			
INDUCTORS	DC Filter			
	RF & Chok	4	0.225	0.900
	Chg React			
RELAYS				
SWITCHES	No Lamp			
SWITCH/LAMP ASSEMBLY	1 - Lamp			
	2 - Lamp			
	4 - Lamp			
INDICATOR (NON SWITCH)	1 - Lamp			
	2 - Lamp			
	4 - Lamp			
MOTORS FANS BLOWER — BRUSH-LESS	≤ 6,000 rpm			
	> 6,000 rpm			
MOTORS FANS BLOWER — BRUSH-TYPE	≤ 6,000 rpm			
	> 6,000 rpm			
QUARTZ CRYSTAL				
RESOLVER & SYNCHROS				
DELAY LINE	RLC			
	Quartz			
POWER DIVIDER		1	0.036	0.036
MICROCIRCUIT	MECL II	1	0.100	0.100
RF SUBASSY	917421	4	5.619	22.476
DIGITAL SUBASSY	917422-1	2	9.280	18.560
DIGITAL SUBASSY	917422-2	1	7.637	7.637
				56.366

MRL 70-1024

MRL RELIABILITY ESTIMATE

PREPARED	DATE	JOB/EQUIPMENT: MK-450	ITEM NO.
APPROVED			ASSEMBLY NO. 917421
			ASSEMBLY NAME: IPM RF DAUG BD.
			NEXT ASSEMBLY 917431
			PAGE OF

COMPONENTS	TYPE	QUANT	F.R./10^6 HR	TOTAL F.R.
RESISTORS	Compos.	12	0.018	0.216
	Film	1	0.156	0.156
	Film Pwr			
	Wire Wnd			
POTS	Film			
	Wire Wnd			
FIXED CAPACITOR	Tantalum			
	MICA	5	0.005	0.025
	CERAMIC	6	0.025	0.150
VARIABLE CAPACITOR	Vacuum			
	CERAMIC	3	0.006	0.018
TRANSFORMER	Filament			
	Power			
	Lo Pwr Pls			
ELECTRON TUBES	Receiver			
	Pwr Rect			
	Xmtr			
C.R.T.'S	1 - Gun			
	3 - Gun			
KLYSTRONS				
THYRATRONS				
MAGNETRONS				
T.W.T.'S				
AMPLITRONS				
TR OR ATR				
DUPLEXER				
MICROWAVE DIODE	Mixer			
	Detector			
MICROWAVE COMPONENTS	Attenuat			
	Direct Cpl			
	Loads			
	Stubs			
	Feed Horn			
	Rotary Jt			
FERRITE DEVICES	Isolator			
	Circulator			
	Modulator			
	Shifter			
RF FILTERS				
HI VOLTAGE DIODE PACK	Hi Power			
	Med Power			
PULSE FORM NETWORK	Lo Volt			
	Hi Volt			

COMPONENTS	TYPE	QUANT	F.R./10^6 HR	TOTAL F.R.
TRANSISTOR	NPN	2	1.320	2.640
DIODES	General & Computer			
	Rectifier			
	Zener			
MICROCIRCUITS				
CONNECTORS	Coax			
	≤ 25 Pin			
	> 25 Pin			
INDUCTORS	DC Filter			
	RF & Chok	4	0.225	0.900
	Chg React			
RELAYS				
SWITCHES	No Lamp			
SWITCH/LAMP ASSEMBLY	1 - Lamp			
	2 - Lamp			
	4 - Lamp			
INDICATOR (NON SWITCH)	1 - Lamp			
	2 - Lamp			
	4 - Lamp			
MOTORS FANS BLOWER — BRUSH-LESS	≤ 6,000 rpm			
	> 6,000 rpm			
MOTORS FANS BLOWER — BRUSH-TYPE	≤ 6,000 rpm			
	> 6,000 rpm			
QUARTZ CRYSTAL				
RESOLVER & SYNCHROS				
DELAY LINE	RLC			
	Quartz			
MIXER		1	1.514	1.514
				5.619

MRL 70-1024

MRL RELIABILITY ESTIMATE

ITEM NO.	
ASSEMBLY NO.	917822-811
PREPARED	
DATE	
APPROVED	
JOB/EQUIPMENT	MK-450
ASSEMBLY NAME	IPM DIGITAL DAUG (501)
NEXT ASSEMBLY	917431
PAGE OF	

COMPONENTS	TYPE	QUANT	F.R./10^6 HR	TOTAL F.R.
RESISTORS	Compos.	7	0.018	0.162
	Film	2	0.156	0.312
	Film Pwr			
	Wire Wnd			
POTS	Film			
	Wire Wnd			
FIXED CAPACITOR	Tantalum			
	MICA	1	0.005	0.005
	CERAMIC	3	0.025	0.075
VARIABLE CAPACITOR	Vacuum			
TRANSFORMER	Filament			
	Power			
	Lo Pwr Pls			
ELECTRON TUBES	Receiver			
	Pwr Rect			
	Xmtr			
C.R.T.'S	1 - Gun			
	3 - Gun			
KLYSTRONS				
THYRATRONS				
MAGNETRONS				
T.W.T.'S				
AMPLITRONS				
TR OR ATR				
DUPLEXER				
MICROWAVE DIODE	Mixer			
	Detector			
MICROWAVE COMPONENTS	Attenuat			
	Direct Cpl			
	Loads			
	Stubs			
	Feed Horn			
	Rotary Jt			
FERRITE DEVICES	Isolator			
	Circulator			
	Modulator			
	Shifter			
RF FILTERS				
HI VOLTAGE DIODE PACK	Hi Power			
	Med Power			
PULSE FORM NETWORK	Lo Volt			
	Hi Volt			

COMPONENTS	TYPE	QUANT	F.R./10^6 HR	TOTAL F.R.
TRANSISTOR				
DIODES	General & Computer	2	0.413	0.826
	Rectifier			
	Zener			
MICROCIRCUITS				
CONNECTORS	Coax			
	≤ 25 Pin			
	> 25 Pin			
INDUCTORS	DC Filter			
	RF & Chok			
	Chg React			
RELAYS				
SWITCHES	No Lamp			
SWITCH/LAMP ASSEMBLY	1 - Lamp			
	2 - Lamp			
	4 - Lamp			
INDICATOR (NON SWITCH)	1 - Lamp			
	2 - Lamp			
	4 - Lamp			
MOTORS FANS BLOWER — BRUSH-LESS	≤ 6,000 rpm			
	> 6,000 rpm			
MOTORS FANS BLOWER — BRUSH-TYPE	≤ 6,000 rpm			
	> 6,000 rpm			
QUARTZ CRYSTAL				
RESOLVER & SYNCHROS				
DELAY LINE	RLC			
	Quartz			
MICROCIRCUIT	MECL II	1	0.100	0.100
	MECL III	13	0.600	7.800
TOTAL				9.280

MRL 70-1034

MRL RELIABILITY ESTIMATE		ITEM NO.	ASSEMBLY NO. 917422-802
PREPARED	DATE	JOB/EQUIPMENT MK-450	ASSEMBLY NAME IPM DIGITAL DAUG BD. (802)
APPROVED			NEXT ASSEMBLY 917431 — PAGE OF

COMPONENTS	TYPE	QUANT	F.R./10^6 HR	TOTAL F.R.
RESISTORS	Compos.	6	0.018	0.108
	Film	2	0.156	0.312
	Film Pwr			
	Wire Wnd			
POTS	Film			
	Wire Wnd			
FIXED CAPACITOR	Tantalum			
	MICA	2	0.005	0.010
	CERAMIC	3	0.025	0.075
VARIABLE CAPACITOR	Vacuum			
TRANSFORMER	Filament			
	Power			
	Lo Pwr Pls			
ELECTRON TUBES	Receiver			
	Pwr Rect			
	Xmtr			
C.R.T.'S	1 - Gun			
	3 - Gun			
KLYSTRONS				
THYRATRONS				
MAGNETRONS				
T.W.T.'S				
AMPLITRONS				
TR OR ATR				
DUPLEXER				
MICROWAVE DIODE	Mixer			
	Detector			
MICROWAVE COMPONENTS	Attenual			
	Direct Cpl			
	Loads			
	Stubs			
	Feed Horn			
	Rotary Jt			
FERRITE DEVICES	Isolator			
	Circulator			
	Modulator			
	Shifter			
RF FILTERS				
HI VOLTAGE DIODE PACK	Hi Power			
	Med Power			
PULSE FORM NETWORK	Lo Volt			
	Hi Volt			

COMPONENTS	TYPE	QUANT	F.R./10^6 HR	TOTAL F.R.
TRANSISTOR				
DIODES	General & Computer	4	0.413	1.632
	Rectifier			
	Zener			
MICROCIRCUITS				
CONNECTORS	Coax			
	≤ 25 Pin			
	> 25 Pin			
INDUCTORS	DC Filter			
	RF & Chok			
	Chg React			
RELAYS				
SWITCHES	No Lamp			
SWITCH/LAMP ASSEMBLY	1 - Lamp			
	2 - Lamp			
	4 - Lamp			
INDICATOR (NON SWITCH)	1 - Lamp			
	2 - Lamp			
	4 - Lamp			
MOTORS FANS BLOWER — BRUSH-LESS	≤ 6,000 rpm			
	> 6,000 rpm			
MOTORS FANS BLOWER — BRUSH-TYPE	≤ 6,000 rpm			
	> 6,000 rpm			
QUARTZ CRYSTAL				
RESOLVER & SYNCHROS				
DELAY LINE	RLC			
	Quartz			
MICROCIRCUIT	MECL II	1	0.1100	0.1100
	MECL III	9	0.1600	5.1400
				7.637

MRL 70-1024

MRL RELIABILITY ESTIMATE

ITEM NO.	ASSEMBLY NO.
	917433

PREPARED	DATE	JOB/EQUIPMENT	ASSEMBLY NAME
		MV-450	CODER
APPROVED			NEXT ASSEMBLY / PAGE OF

COMPONENTS	TYPE	QUANT	F.R./10^6 HR	TOTAL F.R.
RESISTORS	Compos.	1	0.018	0.018
	Film	13	0.156	2.028
	Film Pwr			
	Wire Wnd			
POTS	Film			
	Wire Wnd			
FIXED CAPACITOR	Tantalum			
	Electroly			
	GLASS	12	0.143	1.716
VARIABLE CAPACITOR	Vacuum			
TRANSFORMER	Filament			
	Power			
	Lo Pwr Pls			
ELECTRON TUBES	Receiver			
	Pwr Rect			
	Xmtr			
C.R.T.'S	1 - Gun			
	3 - Gun			
KLYSTRONS				
THYRATRONS				
MAGNETRONS				
T.W.T.'S				
AMPLITRONS				
TR OR ATR				
DUPLEXER				
MICROWAVE DIODE	Mixer			
	Detector			
MICROWAVE COMPONENTS	Attenuat			
	Direct Cpl			
	Loads			
	Stubs			
	Feed Horn			
	Rotary Jt			
FERRITE DEVICES	Isolator			
	Circulator			
	Modulator			
	Shifter			
RF FILTERS				
HI VOLTAGE DIODE PACK	Hi Power			
	Med Power			
PULSE FORM NETWORK	Lo Volt			
	Hi Volt			

COMPONENTS	TYPE	QUANT	F.R./10^6 HR	TOTAL F.R.
TRANSISTOR				
DIODES	General & Computer			
	Rectifier			
	Zener			
MICROCIRCUITS		48	0.115	5.520
CONNECTORS	Coax			
	≤ 25 Pin			
	> 25 Pin			
INDUCTORS	DC Filter			
	RF & Chok			
	Chg React			
RELAYS				
SWITCHES	No Lamp			
SWITCH/LAMP ASSEMBLY	1 - Lamp			
	2 - Lamp			
	4 - Lamp			
INDICATOR (NON SWITCH)	1 - Lamp			
	2 - Lamp			
	4 - Lamp			
MOTORS FANS BLOWER — BRUSH-LESS	≤ 6,000 rpm			
	> 6,000 rpm			
MOTORS FANS BLOWER — BRUSH-TYPE	≤ 6,000 rpm			
	> 6,000 rpm			
QUARTZ CRYSTAL				
RESOLVER & SYNCHROS				
DELAY LINE	RLC			
	Quartz			
TOTAL				9.282

MRL 70-1024

MRL RELIABILITY ESTIMATE

PREPARED	DATE	JOB/EQUIPMENT: MX-450	ITEM NO.
APPROVED			ASSEMBLY NO. 717435
			ASSEMBLY NAME: CHANNEL CONTROL
			NEXT ASSEMBLY
			PAGE OF

COMPONENTS	TYPE	QUANT	F.R./10^6 HR	TOTAL F.R.
RESISTORS	Compos.			
	Film			
	Film Pwr			
	Wire Wnd			
POTS	Film			
	Wire Wnd			
FIXED CAPACITOR	Tantalum			
	Electroly			
VARIABLE CAPACITOR	Vacuum			
TRANSFORMER	Filament			
	Power			
	Lo Pwr Pls			
ELECTRON TUBES	Receiver			
	Pwr Rect			
	Xmtr			
C.R.T.'S	1 - Gun			
	3 - Gun			
KLYSTRONS				
THYRATRONS				
MAGNETRONS				
T.W.T.'S				
AMPLITRONS				
TR OR ATR				
DUPLEXER				
MICROWAVE DIODE	Mixer			
	Detector			
MICROWAVE COMPONENTS	Attenuat			
	Direct Cpl			
	Loads			
	Stubs			
	Feed Horn			
	Rotary Jt			
FERRITE DEVICES	Isolator			
	Circulator			
	Modulator			
	Shifter			
RF FILTERS				
HI VOLTAGE DIODE PACK	Hi Power			
	Med Power			
PULSE FORM NETWORK	Lo Volt			
	Hi Volt			

COMPONENTS	TYPE	QUANT	F.R./10^6 HR	TOTAL F.R.
TRANSISTOR				
DIODES	General & Computer			
	Rectifier			
	Zener			
MICROCIRCUITS	DIGITAL	54	0.115	6.210
CONNECTORS	Coax			
	≤ 25 Pin			
	> 25 Pin			
INDUCTORS	DC Filter			
	RF & Chok			
	Chg React			
RELAYS				
SWITCHES	No Lamp			
SWITCH/LAMP ASSEMBLY	1 - Lamp			
	2 - Lamp			
	4 - Lamp			
INDICATOR (NON SWITCH)	1 - Lamp			
	2 - Lamp			
	4 - Lamp			
MOTORS FANS BLOWER — BRUSH-LESS	≤ 6,000 rpm			
	> 6,000 rpm			
MOTORS FANS BLOWER — BRUSH-TYPE	≤ 6,000 rpm			
	> 6,000 rpm			
QUARTZ CRYSTAL				
RESOLVER & SYNCHROS				
DELAY LINE	R L C			
	Quartz			
TOTAL				6.210

MRL 70-1024

MRL RELIABILITY ESTIMATE

PREPARED	DATE	JOB/EQUIPMENT	ITEM NO.	ASSEMBLY NO. 917434
		MX-450	ASSEMBLY NAME MASTER CONTROLLER	
APPROVED			NEXT ASSEMBLY	PAGE OF

COMPONENTS	TYPE	QUANT	F.R./10^6 HR	TOTAL F.R.
RESISTORS	Compos.			
	Film	17	0.156	2.652
	Film Pwr			
	Wire Wnd			
POTS	Film			
	Wire Wnd			
FIXED CAPACITOR	Tantalum	1	0.360	0.360
	Electroly			
	CERAMIC	10	0.025	0.250
VARIABLE CAPACITOR	Vacuum			
TRANSFORMER	Filament			
	Power			
	Lo Pwr Pls			
ELECTRON TUBES	Receiver			
	Pwr Rect			
	Xmtr			
C.R.T.'S	1 - Gun			
	3 - Gun			
KLYSTRONS				
THYRATRONS				
MAGNETRONS				
T.W.T.'S				
AMPLITRONS				
TR OR ATR				
DUPLEXER				
MICROWAVE DIODE	Mixer			
	Detector			
MICROWAVE COMPONENTS	Attenuat			
	Direct Cpl			
	Loads			
	Stubs			
	Feed Horn			
	Rotary Jt			
FERRITE DEVICES	Isolator			
	Circulator			
	Modulator			
	Shifter			
RF FILTERS				
HI VOLTAGE DIODE PACK	Hi Power			
	Med Power			
PULSE FORM NETWORK	Lo Volt			
	Hi Volt			

COMPONENTS	TYPE	QUANT	F.R./10^6 HR	TOTAL F.R.
TRANSISTOR				
DIODES	General & Computer			
	Rectifier			
	Zener			
MICROCIRCUITS	DIGITAL	33	0.115	3.795
CONNECTORS	Coax			
	≤ 25 Pin			
	> 25 Pin			
INDUCTORS	DC Filter			
	RF & Chok	1	0.225	0.225
	Chg React			
RELAYS				
SWITCHES	No Lamp			
SWITCH/LAMP ASSEMBLY	1 - Lamp			
	2 - Lamp			
	4 - Lamp			
INDICATOR (NON SWITCH)	1 - Lamp			
	2 - Lamp			
	4 - Lamp			
MOTORS FANS BLOWER — BRUSH-LESS	≤ 6,000 rpm			
	> 6,000 rpm			
MOTORS FANS BLOWER — BRUSH-TYPE	≤ 6,000 rpm			
	> 6,000 rpm			
QUARTZ CRYSTAL				
RESOLVER & SYNCHROS				
DELAY LINE	RLC			
	Quartz			
				7.282

MRL 70-1024

MRL RELIABILITY ESTIMATE		ITEM NO.	ASSEMBLY NO. 717441
PREPARED	DATE	JOB/EQUIPMENT MK-450	ASSEMBLY NAME VELOCITY D/A CONVERTER
APPROVED			NEXT ASSEMBLY / PAGE OF

COMPONENTS	TYPE	QUANT	F.R./10^6 HR	TOTAL F.R.
RESISTORS	Compos.			
	Film	17	0.156	2.652
	Film Pwr			
	Wire Wnd			
POTS	Film	4	9.360	37.440
	Wire Wnd			
FIXED CAPACITOR	Tantalum			
	Electroly			
	CERAMIC	12	0.025	0.300
VARIABLE CAPACITOR	Vacuum			
TRANSFORMER	Filament			
	Power			
	Lo Pwr Pls			
ELECTRON TUBES	Receiver			
	Pwr Rect			
	Xmtr			
C.R.T.'S	1 - Gun			
	3 - Gun			
KLYSTRONS				
THYRATRONS				
MAGNETRONS				
T.W.T.'S				
AMPLITRONS				
TR OR ATR				
DUPLEXER				
MICROWAVE DIODE	Mixer			
	Detector			
MICROWAVE COMPONENTS	Attenuat			
	Direct Cpl			
	Loads			
	Stubs			
	Feed Horn			
	Rotary Jt			
FERRITE DEVICES	Isolator			
	Circulator			
	Modulator			
	Shifter			
RF FILTERS				
HI VOLTAGE DIODE PACK	Hi Power			
	Med Power			
PULSE FORM NETWORK	Lo Volt			
	Hi Volt			

COMPONENTS	TYPE	QUANT	F.R./10^6 HR	TOTAL F.R.
TRANSISTOR				
DIODES	General & Computer			
	Rectifier			
	Zener			
MICROCIRCUITS	DIGITAL	12	0.115	1.380
CONNECTORS	Coax			
	≤ 25 Pin			
	> 25 Pin			
INDUCTORS	DC Filter			
	RF & Chok			
	Chg React			
RELAYS				
SWITCHES	No Lamp			
SWITCH/LAMP ASSEMBLY	1 - Lamp			
	2 - Lamp			
	4 - Lamp			
INDICATOR (NON SWITCH)	1 - Lamp			
	2 - Lamp			
	4 - Lamp			
MOTORS FANS BLOWER, BRUSH-LESS	≤ 6,000 rpm			
	> 6,000 rpm			
MOTORS FANS BLOWER, BRUSH-TYPE	≤ 6,000 rpm			
	> 6,000 rpm			
QUARTZ CRYSTAL				
RESOLVER & SYNCHROS				
DELAY LINE	RLC			
	Quartz			
				41.772

MRL 70-1024

MRL RELIABILITY ESTIMATE			ITEM NO.	ASSEMBLY NO. 917436
PREPARED	DATE	JOB/EQUIPMENT	ASSEMBLY NAME RANGE/DOPPLER EXTRACTOR	
APPROVED		MX-450	NEXT ASSEMBLY	PAGE OF

COMPONENTS	TYPE	QUANT	F.R./10^6 HR	TOTAL F.R.
RESISTORS	Compos.	2	0.018	0.036
	Film			
	Film Pwr			
	Wire Wnd			
POTS	Film			
	Wire Wnd			
FIXED CAPACITOR	Tantalum			
	Electroly			
	CERAMIC	7	0.025	0.175
VARIABLE CAPACITOR	Vacuum			
TRANSFORMER	Filament			
	Power			
	Lo Pwr Pls			
ELECTRON TUBES	Receiver			
	Pwr Rect			
	Xmtr			
C.R.T.'S	1 - Gun			
	3 - Gun			
KLYSTRONS				
THYRATRONS				
MAGNETRONS				
T.W.T.'S				
AMPLITRONS				
TR OR ATR				
DUPLEXER				
MICROWAVE DIODE	Mixer			
	Detector			
MICROWAVE COMPONENTS	Attenuat			
	Direct Cpl			
	Loads			
	Stubs			
	Feed Horn			
	Rotary Jt			
FERRITE DEVICES	Isolator			
	Circulator			
	Modulator			
	Shifter			
RF FILTERS				
HI VOLTAGE DIODE PACK	Hi Power			
	Med Power			
PULSE FORM NETWORK	Lo Volt			
	Hi Volt			

COMPONENTS	TYPE	QUANT	F.R./10^6 HR	TOTAL F.R.
TRANSISTOR				
DIODES	General & Computer			
	Rectifier			
	Zener			
MICROCIRCUITS	DIGITAL	41	0.115	4.715
CONNECTORS	Coax			
	≤ 25 Pin			
	> 25 Pin			
INDUCTORS	DC Filter			
	RF & Chok			
	Chg React			
RELAYS				
SWITCHES	No Lamp			
SWITCH/LAMP ASSEMBLY	1 - Lamp			
	2 - Lamp			
	4 - Lamp			
INDICATOR (NON SWITCH)	1 - Lamp			
	2 - Lamp			
	4 - Lamp			
MOTORS FANS BLOWER — BRUSHLESS	< 6,000 rpm			
	> 6,000 rpm			
MOTORS FANS BLOWER — BRUSH-TYPE	≤ 6,000 rpm			
	> 6,000 rpm			
QUARTZ CRYSTAL				
RESOLVER & SYNCHROS				
DELAY LINE	RLC			
	Quartz			
				4.926

MRL 70-1024

MRL RELIABILITY ESTIMATE

PREPARED	DATE	JOB/EQUIPMENT: UV-450	ITEM NO.
APPROVED			ASSEMBLY NO. 917437
			ASSEMBLY NAME: RECORDER INTERFACE 1
			NEXT ASSEMBLY
			PAGE OF

COMPONENTS	TYPE	QUANT	F.R./10^6 HR	TOTAL F.R.
RESISTORS	Compos.	2	0.018	0.036
	Film	3	0.156	0.468
	Film Pwr			
	Wire Wnd			
POTS	Film			
	Wire Wnd			
FIXED CAPACITOR	Tantalum			
	Electroly			
	CERAMIC	10	0.025	0.250
VARIABLE CAPACITOR	Vacuum			
TRANSFORMER	Filament			
	Power			
	Lo Pwr Pls			
ELECTRON TUBES	Receiver			
	Pwr Rect			
	Xmtr			
C.R.T.'S	1 - Gun			
	3 - Gun			
KLYSTRONS				
THYRATRONS				
MAGNETRONS				
T.W.T.'S				
AMPLITRONS				
TR OR ATR				
DUPLEXER				
MICROWAVE DIODE	Mixer			
	Detector			
MICROWAVE COMPONENTS	Attenuat			
	Direct Cpl			
	Loads			
	Stubs			
	Feed Horn			
	Rotary Jt			
FERRITE DEVICES	Isolator			
	Circulator			
	Modulator			
	Shifter			
RF FILTERS				
HI VOLTAGE DIODE PACK	Hi Power			
	Med Power			
PULSE FORM NETWORK	Lo Volt			
	Hi Volt			

COMPONENTS	TYPE	QUANT	F.R./10^6 HR	TOTAL F.R.
TRANSISTOR				
DIODES	General & Computer			
	Rectifier			
	Zener	1	1.260	1.260
MICROCIRCUITS	DIGITAL	26	0.115	2.990
CONNECTORS	Coax			
	≤ 25 Pin			
	> 25 Pin			
INDUCTORS	DC Filter			
	RF & Chok			
	Chg React			
RELAYS				
SWITCHES	No Lamp			
SWITCH/LAMP ASSEMBLY	1 - Lamp			
	2 - Lamp			
	4 - Lamp			
INDICATOR (NON SWITCH)	1 - Lamp			
	2 - Lamp			
	4 - Lamp			
MOTORS FANS BLOWER — BRUSH-LESS	≤ 6,000 rpm			
	> 6,000 rpm			
MOTORS FANS BLOWER — BRUSH-TYPE	≤ 6,000 rpm			
	> 6,000 rpm			
QUARTZ CRYSTAL				
RESOLVER & SYNCHROS				
DELAY LINE	RLC			
	Quartz			
				5.004

MRL 70-1024

MRL RELIABILITY ESTIMATE

PREPARED	DATE	JOB/EQUIPMENT	ITEM NO. / ASSEMBLY NO. 917438
APPROVED		MX-450	ASSEMBLY NAME: RECORDER INTERFACE 2
			NEXT ASSEMBLY / PAGE OF

COMPONENTS	TYPE	QUANT	F.R./10^6 HR	TOTAL F.R.
RESISTORS	Compos.			
	Film	2	0.156	0.312
	Film Pwr			
	Wire Wnd			
POTS	Film			
	Wire Wnd			
FIXED CAPACITOR	Tantalum	1	1.200	1.200
	Electroly			
	CERAMIC	6	0.025	0.150
VARIABLE CAPACITOR	Vacuum			
TRANSFORMER	Filament			
	Power			
	Lo Pwr Pls			
ELECTRON TUBES	Receiver			
	Pwr Rect			
	Xmtr			
C.R.T.'S	1 - Gun			
	3 - Gun			
KLYSTRONS				
THYRATRONS				
MAGNETRONS				
T.W.T.'S				
AMPLITRONS				
TR OR ATR				
DUPLEXER				
MICROWAVE DIODE	Mixer			
	Detector			
MICROWAVE COMPONENTS	Attenuat			
	Direct Cpl			
	Loads			
	Stubs			
	Feed Horn			
	Rotary Jt			
FERRITE DEVICES	Isolator			
	Circulator			
	Modulator			
	Shifter			
RF FILTERS				
HI VOLTAGE DIODE PACK	Hi Power			
	Med Power			
PULSE FORM NETWORK	Lo Volt			
	Hi Volt			

COMPONENTS	TYPE	QUANT	F.R./10^6 HR	TOTAL F.R.
TRANSISTOR				
DIODES	General & Computer	1	0.413	0.413
	Rectifier			
	Zener			
MICROCIRCUITS	DIGITAL	26	0.115	2.990
CONNECTORS	Coax			
	≤ 25 Pin			
	> 25 Pin			
INDUCTORS	DC Filter			
	RF & Chok			
	Chg React			
RELAYS				
SWITCHES	No Lamp			
SWITCH/LAMP ASSEMBLY	1 - Lamp			
	2 - Lamp			
	4 - Lamp			
INDICATOR (NON SWITCH)	1 - Lamp			
	2 - Lamp			
	4 - Lamp			
MOTORS FANS BLOWER — BRUSH-LESS	≤ 6,000 rpm			
	> 6,000 rpm			
MOTORS FANS BLOWER — BRUSH-TYPE	≤ 6,000 rpm			
	> 6,000 rpm			
QUARTZ CRYSTAL				
RESOLVER & SYNCHROS				
DELAY LINE	RLC			
	Quartz			
				5.065

MRL 70-1024

MRL RELIABILITY ESTIMATE

ITEM NO.		ASSEMBLY NO.	917432
PREPARED		DATE	
APPROVED			
JOB/EQUIPMENT	MX-450	ASSEMBLY NAME	RECORDER INTERFACE 3
NEXT ASSEMBLY		PAGE	OF

COMPONENTS	TYPE	QUANT	F.R./10^6 HR	TOTAL F.R.
RESISTORS	Compos.			
	Film	5	0.156	0.780
	Film Pwr			
	Wire Wnd			
POTS	Film			
	Wire Wnd			
FIXED CAPACITOR	Tantalum			
	Electroly			
	CERAMIC	4	0.025	0.100
VARIABLE CAPACITOR	Vacuum			
TRANSFORMER	Filament			
	Power			
	Lo Pwr Pls			
ELECTRON TUBES	Receiver			
	Pwr Rect			
	Xmtr			
C.R.T.'S	1 - Gun			
	3 - Gun			
KLYSTRONS				
THYRATRONS				
MAGNETRONS				
T.W.T.'S				
AMPLITRONS				
TR OR ATR				
DUPLEXER				
MICROWAVE DIODE	Mixer			
	Detector			
MICROWAVE COMPONENTS	Attenuat			
	Direct Cpl			
	Loads			
	Stubs			
	Feed Horn			
	Rotary Jt			
FERRITE DEVICES	Isolator			
	Circulator			
	Modulator			
	Shifter			
RF FILTERS				
HI VOLTAGE DIODE PACK	Hi Power			
	Med Power			
PULSE FORM NETWORK	Lo Volt			
	Hi Volt			

COMPONENTS	TYPE	QUANT	F.R./10^6 HR	TOTAL F.R.
TRANSISTOR				
DIODES	General & Computer			
	Rectifier			
	Zener			
MICROCIRCUITS	DIGITAL	20	0.115	2.300
CONNECTORS	Coax			
	≤ 25 Pin			
	> 25 Pin			
INDUCTORS	DC Filter			
	RF & Chok			
	Chg React			
RELAYS				
SWITCHES	No Lamp			
SWITCH/LAMP ASSEMBLY	1 - Lamp			
	2 - Lamp			
	4 - Lamp			
INDICATOR (NON SWITCH)	1 - Lamp			
	2 - Lamp			
	4 - Lamp			
MOTORS FANS BLOWER — BRUSH-LESS	≤ 6,000 rpm			
	> 6,000 rpm			
MOTORS FANS BLOWER — BRUSH-TYPE	≤ 6,000 rpm			
	> 6,000 rpm			
QUARTZ CRYSTAL				
RESOLVER & SYNCHROS				
DELAY LINE	RLC			
	Quartz			
				3.180

MRL 70-1024

MRL RELIABILITY ESTIMATE

PREPARED	DATE	JOB/EQUIPMENT: MX-450	ITEM NO.
APPROVED			ASSEMBLY NO. 917737
			ASSEMBLY NAME: FREQUENCY SYNTHESIZER 2
			NEXT ASSEMBLY
			PAGE OF

COMPONENTS	TYPE	QUANT	F.R./10^6 HR	TOTAL F.R.
RESISTORS	Compos.	2	0.018	0.036
	Film	30	0.156	4.680
	Film Pwr			
	Wire Wnd			
POTS	Film			
	Wire Wnd			
FIXED CAPACITOR	Tantalum			
	MICA	3	0.005	0.015
	CERAMIC	25	0.025	0.625
VARIABLE CAPACITOR	Vacuum	1	0.006	0.006
TRANSFORMER	Filament			
	Power			
	Lo Pwr Pls			
ELECTRON TUBES	Receiver			
	Pwr Rect			
	Xmtr			
C.R.T.'S	1 - Gun			
	3 - Gun			
KLYSTRONS				
THYRATRONS				
MAGNETRONS				
T.W.T.'S				
AMPLITRONS				
TR OR ATR				
DUPLEXER				
MICROWAVE DIODE	Mixer			
	Detector			
MICROWAVE COMPONENTS	Attenuat			
	Direct Cpl			
	Loads			
	Stubs			
	Feed Horn			
	Rotary Jt			
FERRITE DEVICES	Isolator			
	Circulator			
	Modulator			
	Shifter			
RF FILTERS				
HI VOLTAGE DIODE PACK	Hi Power			
	Med Power			
PULSE FORM NETWORK	Lo Volt			
	Hi Volt			

COMPONENTS	TYPE	QUANT	F.R./10^6 HR	TOTAL F.R.
TRANSISTOR	NPN	9	1.320	11.880
	PWR	2	2.640	5.280
DIODES	General & Computer			
	HP	1	2.200	2.200
	Zener			
MICROCIRCUITS				
CONNECTORS	Coax			
	≤ 25 Pin			
	> 25 Pin			
INDUCTORS	DC Filter			
	RF & Chok	13	0.225	2.925
	Chg Rect			
RELAYS				
SWITCHES	No Lamp			
SWITCH/LAMP ASSEMBLY	1 - Lamp			
	2 - Lamp			
	4 - Lamp			
INDICATOR (NON SWITCH)	1 - Lamp			
	2 - Lamp			
	4 - Lamp			
MOTORS FANS BLOWER — BRUSHLESS	≤ 6,000 rpm			
	> 6,000 rpm			
MOTORS FANS BLOWER — BRUSH-TYPE	≤ 6,000 rpm			
	> 6,000 rpm			
QUARTZ CRYSTAL				
RESOLVER & SYNCHROS				
DELAY LINE	RLC			
	Quartz			
POWER DIVIDER		3	0.436	1.308
XTAL FILTER		3	0.184	0.552
MIXER		1	1.516	1.514
MICROCIRCUIT	MECL III	3	0.600	1.800
				32.821

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MRL RELIABILITY ESTIMATE

PREPARED	DATE	JOB/EQUIPMENT: MX-150	ITEM NO.
APPROVED			ASSEMBLY NO. 117220
			ASSEMBLY NAME: FREQUENCY SYNTHESIZER 3
			NEXT ASSEMBLY
			PAGE OF

COMPONENTS	TYPE	QUANT	F.R./10^6 HR	TOTAL F.R.
RESISTORS	Compos.			
	Film	25	0.156	3.900
	Film Pwr			
	Wire Wnd			
POTS	Film			
	Wire Wnd			
FIXED CAPACITOR	Tantalum	1	0.360	0.360
	CERAMIC	7	0.025	0.175
VARIABLE CAPACITOR	Vacuum			
TRANSFORMER	Filament			
	Power			
	Lo Pwr Pls			
ELECTRON TUBES	Receiver			
	Pwr Rect			
	Xmtr			
C.R.T.'S	1 - Gun			
	3 - Gun			
KLYSTRONS				
THYRATRONS				
MAGNETRONS				
T.W.T.'S				
AMPLITRONS				
TR OR ATR				
DUPLEXER				
MICROWAVE DIODE	Mixer			
	Detector			
MICROWAVE COMPONENTS	Attenuat			
	Direct Cpl			
	Loads			
	Stubs			
	Feed Horn			
	Rotary Jt			
FERRITE DEVICES	Isolator			
	Circulator			
	Modulator			
	Shifter			
RF FILTERS				
HI VOLTAGE DIODE PACK	Hi Power			
	Med Power			
PULSE FORM NETWORK	Lo Volt			
	Hi Volt			

COMPONENTS	TYPE	QUANT	F.R./10^6 HR	TOTAL F.R.
TRANSISTOR	NPN	3	1.320	3.960
DIODES	General & Computer			
	Rectifier			
	Zener			
MICROCIRCUITS	DIGITAL	4	0.115	0.460
CONNECTORS	Coax			
	≤ 25 Pin			
	> 25 Pin			
INDUCTORS	DC Filter			
	RF & Chok	4	0.225	0.900
	Chg React			
RELAYS				
SWITCHES	No Lamp			
SWITCH/LAMP ASSEMBLY	1 - Lamp			
	2 - Lamp			
	4 - Lamp			
INDICATOR (NON SWITCH)	1 - Lamp			
	2 - Lamp			
	4 - Lamp			
MOTORS FANS BLOWER — BRUSH-LESS	≤ 6,000 rpm			
	> 6,000 rpm			
MOTORS FANS BLOWER — BRUSH-TYPE	≤ 6,000 rpm			
	> 6,000 rpm			
QUARTZ CRYSTAL				
RESOLVER & SYNCHROS				
DELAY LINE	RLC			
	Quartz			
POWER DIVIDER		1	0.436	0.436
XTAL FILTER		1	0.184	0.184
MICROCIRCUIT	MECL II	2	0.100	0.200
	MECL II	8	0.650	4.850
				15.375

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DOCUMENT CONTROL DATA - R & D

(Security classification of title, body of abstract and indexing annotation must be entered when the overall report is classified)

1. ORIGINATING ACTIVITY (Corporate author) Magnavox Research Laboratories Torrance, California 90503	2a. REPORT SECURITY CLASSIFICATION UNCLASSIFIED 2b. GROUP

3. REPORT TITLE

FINAL REPORT (DRAFT) SYSTEM 621B USER EQUIPMENT DEFINITION AND EXPERIMENTS PROGRAM TASK VI- PHASE II ALTERNATE RECEIVER

4. DESCRIPTIVE NOTES (Type of report and inclusive dates)

Final (Draft)

5. AUTHOR(S) (First name, middle initial, last name)

Leonard J. Jacobson

6. REPORT DATE 1 November 1972	7a. TOTAL NO. OF PAGES 215	7b. NO. OF REFS
8a. CONTRACT OR GRANT NO F04701-71-C-0318 b. PROJECT NO. 621B c. d.	9a. ORIGINATOR'S REPORT NUMBER(S) R-4[illegible] 9b. OTHER REPORT NO(S) (Any other numbers that may be assigned this report) SAMSO-TR-72-213	

10. DISTRIBUT

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11. SUPPLEMENTARY NOTES	12. SPONSORING MILITARY ACTIVITY Department of the Air Force Headquarters, SAMSO (AFSC) Los Angeles, CA 90045

13. ABSTRACT

System 621B is a concept for a highly-accurate, satellite-navigation system which enables any number of users anywhere on the globe to determine in real time, their position and velocity in three dimensions. The most important performance parameter of this system is the degree of navigational accuracy which is provided the users. This accuracy and other pertinent performance characteristics depend to a large extent upon the chosen orbit configuration and the resulting geometry between the user and the satellites. However, it has been necessary to evolve user navigation receiver designs capable of performing within the system constraints and which contribute negligibly to the overall system accuracy degradation. It is the purpose of this report to document one such receiver design, designated the MX-450 Navigation Receiver, which was developed to further refine and verify the predicted performance of System 621B.

DD FORM 1 NOV 65 1473

14. KEY WORDS	LINK A		LINK B		LINK C	
	ROLE	WT	ROLE	WT	ROLE	WT
Navigation Satellite						
Pseudonoise						
Receiver						
621B						