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PYROELECTRIC/INTEGRATED CIRCUIT INFRARED IMAGING ARRAY DEVELOPMENT

A. BOORNARD, et al.

RCA

TECHNICAL REPORT AFAL-TR-72-406

November 1972

(Interim Report: 22 Feb 1972 through 2 Oct 1972)

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PYROELECTRIC/INTEGRATED CIRCUIT INFRARED IMAGING ARRAY DEVELOPMENT

Interim Technical Report

(22 Feb 1972 — 2 Oct 1972)

A. Boornard, D. Hall, E. Herrmann,
R. D. Larrabee, P. D. Southgate, and W. L. Stephens

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Contract Number:	F33615-72-C-1804
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Project Engineer:	D. J. Peacock
Phone:	513 255-3804
Short Title:	Pyroelectric Imaging Array

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November 1972

FOREWORD

The work reported in this Interim Report was performed under Air Force Contract No. F33615-72-C-1804, entitled "Uncooled IR Image Mosaic Development," by the RCA Advanced Technology Laboratories of the Government and Commercial Systems Division, Camden, New Jersey, and by the RCA Laboratories, Princeton, New Jersey. The work was sponsored by the Advanced Research Projects Agency under ARPA Order No. 1916.

The following RCA personnel contributed to the work and to this report: A. Boornard (Principal Investigator), D. Hall, E. Herrmann, Dr. R. D. Larrabee, Dr. P. D. Southgate, and Dr. W. L. Stephens. The authors wish to acknowledge the assistance of W. Morren in carrying out much of the experimental work on the polycrystalline pyroelectric array effort. Gratitude is expressed to P. E. Wright, Director of the Advanced Technology Laboratories, and to D. J. Woywood, Manager of the Applied Physics Group for their continued interest, support, and consultation.

This report covers work performed from 22 February 1972 to 2 October 1972, and was submitted by the authors 17 November 1972.

This technical report has been reviewed and is approved.

Donald J. Peacock
Air Force Avionics Laboratory
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ABSTRACT

Progress made toward the development of pyroelectric/integrated circuit thermal imaging area arrays and their associated address and sense circuits is described. The processing techniques and steps required to form two-dimensional arrays of thin film triglycine sulfate detectors on field-effect integrated circuit substrates are reviewed. The approach to providing the required high degree of thermal isolation between the polycrystalline detectors and the silicon portion of the circuit is to etch away the silicon underlying the detectors. A second pyroelectric imaging array consisting of a thin permanently poled single crystal section of TGS positioned above the integrated circuit substrate is also described. In this arrangement the resulting air gap provides the thermal isolation and contacts to the array detectors are made by means of vacuum deposited microfinger springs. The relative merits of X-Y addressed versus bucket brigade pyroelectric arrays are discussed. An analysis of the performance capabilities of an X-Y addressed polycrystalline TGS array indicates that a system noise equivalent temperature difference of 0.42°C at 10 frames/second should be achievable in an array consisting of 10-μm thick detectors 4 mils on a side and spaced on 8-mil centers.

GLOSSARY OF ABBREVIATIONS

BB	bucket brigade
D	drain region of an FET
FET	field-effect transistor
G	gate region of an FET
LSI	large scale integration
MOS	metal-oxide-semiconductor
NEΔT	noise equivalent temperature difference
P-MOS	p-channel MOS
S	source region of an FET
S/N	signal-to-noise voltage ratio
TGS	triglycine sulfate

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Interim Teehnical Report
Period 22 February 1972 — 2 October 1972

The objective of this program is to develop the technology required for the fabrication of large scale uncooled two-dimensional pyroelectric/integrated circuit arrays suitable for passive infrared imaging over the 8- to 14-μm transmission window of the Earth's atmosphere. The pyroelectric detector material of principal interest to this program is the organic compound triglycine sulfate (TGS), selected because of its high figure of merit for passive infrared imaging applications.

The detectors of the two-dimensional arrays are composed of thin sections (10- to 25-μm thick) of either polycrystalline or single crystal TGS sandwiched between two thin film electrodes. The resulting detector configuration, essentially a minute temperature sensitive capacitor, forms an extremely sensitive detector of infrared radiation. An infrared image, when focused on the array, produces a spatial temperature distribution corresponding to the intensity of the radiation emitted by the scenc. The spatial temperature distribution is accompanied by a change in the spontaneous electrical polarization of each detector element, which produces a pyroelectric signal voltage proportional to the scene radiation.

The pyroelectrie effect has emer ,ed as one of the more promising mechanisms upon which to base passive infrared imaging systems. The most attractive features of pyroelectric detectors are operation at room temperature, which obviates the need for a cryogenic environment, and the ability to form two-dimensional arrays, which circumvents the need for complex optomechanical scanners. The laek of a refrigerator and optomeehanical scanner should assure large savings in system size, weight, cost, and complexity, and should result in highly improved reliability. Although lacking in sensitivity as compared with infrared imaging systems which utilize eryogenieally cooled linear arrays of quantum detectors (sueh as mercury cadmium telluride or gold doped germanium), the advantages noted should allow the use of pyroelectric infrared imaging systems in applieations where cryogenieally cooled scan systems are not feasible.

The primary approach being developed to realize pyroelectric/integrated circuit arrays is to form a mosaic of individual delineated polycrystalline TGS detectors over a silicon integrated circuit substrate which contains the necessary detector sampling field effect transistors (FETs) and the required address and signal output lines. Key development problems include the formulation of suitable photolithographic and etching techniques to delineate thin TGS films into individual detectors, and the formulation of techniques to provide a high degree of thermal isolation of the detectors from the integrated circuit substrate. Progress in these areas is described in Section II of the report, in which the basic polycrystalline TGS materials work is also described.

Thermal isolation is particularly important since, without adequate isolation, degradation in detector voltage responsivity and accordingly poor temperature resolution capability will result. The thermal isolation technique applicable to polycrystalline TGS films requires preferentially removing (by chemically etching away) the portions of the silicon substrate under each row of detectors up to the thermally grown silicon dioxide (SiO_2) layer which covers the integrated circuit. In this manner the detectors are supported on top of the thin SiO_2 membrane (12,000-Å thick). Detector heat loss by conduction to the remaining substrate material is greatly diminished, owing to the high thermal resistance of the thin SiO_2 membrane. This thermal isolation arrangement is illustrated in Section II and analyzed in considerable detail in Section V, in which the thermal time constants are calculated and in which the thermal conductance is calculated as a function of detector size, detector center-to-center spacing, and SiO_2 membrane thickness.

A second approach toward realizing pyroelectric/integrated circuit arrays, which utilizes a thin slab of single crystal TGS (about 25-μm thick), is also being developed. This approach uses the same integrated circuit substrates, but the undelineated detector array -- formed on a single crystal slab -- is positioned above the integrated circuit by means of thin shims located at the periphery of the array. Electrical contact to the array detectors is established by thin film microfingers made of bimetallic vacuum-deposited strips; these form minute curled springs, attached to the substrate, which contact the array. The air gap between the TGS detector section and the silicon substrate thermally isolates the detectors from the substrate. This arrangement is described and analyzed in Section III.

Two types of infrared imaging arrays are being developed, an X-Y addressed array and a bucket brigade array; both of these will initially contain 16-by-16 pyroelectric detector elements, each measuring about 4 mils on a side, with a center-to-center spacing of 8 mils in both the x- and y-directions. The pyroelectric material may be either polycrystalline or single crystal in either type of array.

The X-Y addressed array, described in Sections I and IV and analyzed in Section V, contains a TGS detector element and two FETs within each sensor cell: a signal FET and a reference FET. This arrangement permits extraction of low level pyroelectric signals by subsequent amplification in difference amplifiers located external

to the imaging array. The array is shuttered (at rates of 10/second to 30/second) and digitally addressed one column at a time. The calculations of Section V indicate that the temperature resolution capabilities of such an array should be adequate for many applications. The calculations predict a noise equivalent temperature difference of 0.42°C at a frame rate of 10/second and of 0.48°C and 0.58°C at frame rates of 20/second and 30/second, respectively.

The bucket brigade array is the pyroelectric counterpart of the visible light bucket brigade image sensor array. Each sensor cell contains a pyroelectric detector capacitor, a metal oxide semiconductor (MOS) capacitor, and two FETs. The pyroelectric induced charge, which is proportional to the scene radiation, is transferred from cell to cell along a series of linear bucket brigade arrays which comprise the two-dimensional array. The bucket brigade array is described in Section IV; analysis of its temperature resolution capabilities is awaiting the development of a noise model for bucket brigade arrays.

Section I

INTRODUCTION

This program is being carried out to develop the technology required for the fabrication of large scale, two-dimensional pyroelectric/integrated circuit detector arrays suitable for imaging over the 8- to 14-μm transmission window of the Earth's atmosphere. The primary approach to realizing such arrays is to form a mosaic of delineated pyroelectric detectors (of polycrystalline material) over a silicon integrated circuit substrate which contains the necessary detector-sampling field-effect transistors (FETs) and the required address and signal output lines.

A second approach is to utilize the same integrated circuit substrate, but to form the detectors on a thinned single crystal section of the pyroelectric material positioned above the integrated circuit substrate and contact them by means of thin film metallic microfingers.

Two types of arrays are being developed, an X-Y addressed array and a bucket-brigade (BB) array; both of these will initially contain 16-by-16 pyroelectric detector elements, each element measuring about 4 mils on a side, with a center-to-center spacing of 8 mils in both the x- and y-directions.

Since pyroelectric detectors are heat-sensitive elements, effective thermal isolation of the detectors from the integrated circuit substrate must be provided if high array sensitivity is to be obtained. Additionally, delineation of the detector elements is also desirable in order to obtain the least thermal cross-talk, or equivalently to realize the highest spatial resolution possible.

The pyroelectric effect (i.e., the temperature induced change in spontaneous polarization of certain materials) has emerged as one of the more promising mechanisms upon which to base passive thermal imaging systems. The most attractive features are operation at room temperature, which obviates the need for providing a cryogenic environment, and the ability to form two-dimensional arrays, which circumvents the need for complex optomechanical scanners. The lack of a refrigerator and optomechanical scanner should assure large savings in size, weight, cost, and complexity and should result in highly improved reliability. Although lacking in sensitivity as compared with thermal imaging systems which utilize cryogenically cooled linear arrays of quantum detectors (such as mercury cadmium telluride or gold doped germanium), the advantages noted should permit the use of pyroelectric thermal imaging systems in applications where cryogenically cooled scan systems are not feasible.

A. PYROELECTRIC EFFECT

Certain materials exhibit a spontaneous electrical polarization, an alignment of the internal electric dipoles even in the absence of an applied electric field. The polarization decreases with increasing temperature and vanishes at a specific temperature, called the Curie temperature after the analogous behavior in ferromagnetic materials. Because the polarization is temperature dependent, materials exhibiting this property are called pyroelectric. The polarization temperature dependence of triglycine sulfate (TGS), a material of particular interest to this program, is illustrated in Fig. 1-1. Measurements of the rate of change of polarization with respect to temperature, dP/dT, known as the pyroelectric coefficient, range from 3.5×10^{-8} coulombs/cm^2 - °K at 27°C to 1×10^{-7} coulombs/cm^2 - °K at 40°C for single crystal TGS.[1,2] Other properties of single cyrstal TGS are listed in Table 1-1. Polycrystalline TGS, which forms the basis for one of the pyroelectric/integrated circuit approaches described in this report, has properties which differ from those of the single crystal material. The differences and their effects are discussed in various sections of the report.

An external electric field is not normally observable in the vicinity of a pyroelectric material, even if it is an insulator, because the polarization field ultimately becomes neutralized by leakage currents and/or by stray charges which are attracted to and bound to the surface. The bound surface charge is unable to respond to rapid changes in the polarization. Thus, a sudden temperature-induced change in the polarization will be accompanied by an observable external electric field while the surface charge is adjusting to the new conditions. It is the measurement of this transient electric field that forms the basis of pyroelectric detectors.

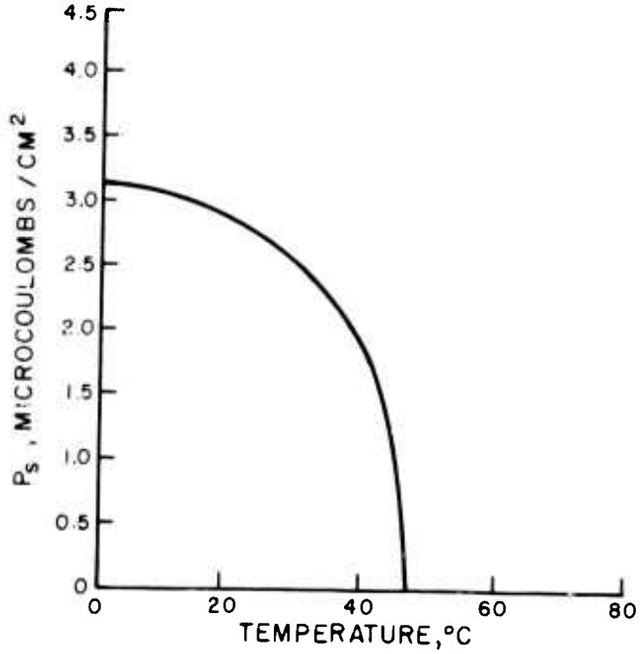


Fig. 1-1. Spontaneous polarization of TGS as a function of temperature (from Reference 2).

TABLE 1-1. SELECTED PROPERTIES OF SINGLE CRYSTAL TRIGLYCINE SULFATE AT 300° K (After Putley, Ref. 1)

Pyroelectric Coefficient, dP/dT	2-3.5 x 10^{-8} C/cm^2 - ° K
Relative Dielectric Constant, ϵ_r	25 - 50
Dielectric Coefficient, ϵ	2.1 - 4.42 x 10^{-12} F cm^{-1}
Specific Heat, C_p	0.97 J/gm-° K
Thermal Conductivity, K	6.8 x 10^{-3} W/cm-° K
Mass Density, ρ_m	1.69 gm/cm^3
Thermal Diffusivity	0.41 x 10^{-2} cm^2/s

B. PYROELECTRIC DETECTORS FOR THERMAL IMAGING

The pyroelectric effect can be utilized to form a sensitive infrared detector by constructing a parallel plate capacitor with the pyroelectric material as the dielectric. The absorption of infrared radiation results in a temperature-induced change in the polarization which is accompanied by a transient change in the potential across the detector electrodes. A pyroelectric detector, with its associated high input resistance and low input capacitance FET amplifier, is shown in Fig. 1-2. The resistance, R_d, which shunts the capacitance, C_d, of the detector is always present by virtue of the leakage resistance of the pyroelectric material. The transient electric field that develops when the detector is subjected to radiation can be measured by the voltage drop across R_d.

For application to infrared imaging systems, the detector RC time constant should be large compared with the frame time to ensure negligible loss of charge during exposure. In this mode of operation, the detector integrates the infrared scene radiation for the total exposure, and to a first approximation the change in the detector open-circuit voltage, ΔV, is proportional to the change in temperature, ΔT.

$$\Delta V \approx \Delta Q / C_d \qquad (1\text{-}1)$$

where ΔQ is the temperature-induced change in charge on the detector electrodes in coulombs and C_d is the capacitance of the detector in farads. C_d is given by

$$C_d = \frac{\epsilon A_d}{d}$$

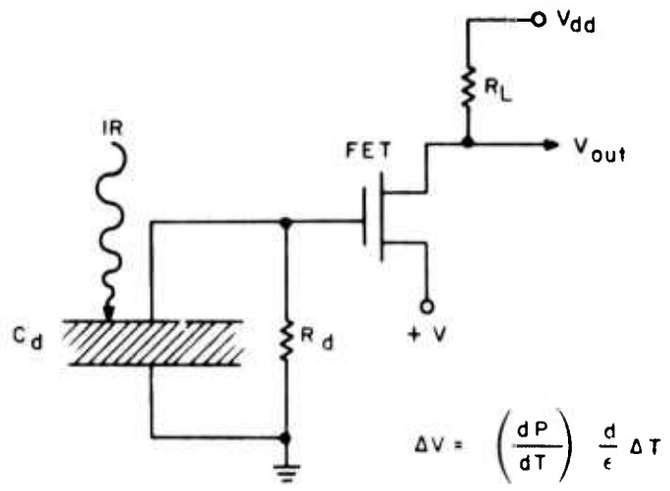


Fig. 1-2. Basic arrangement of a pyroelectric thermal detector.

Here A_d is the area of the capacitor plates in square centimeters, d is the thickness of the pyroelectric material in centimeters and ϵ is the dielectric coefficient of the pyroelectric material in farads/centimeter.

Since the polarization is equivalent to the charge per unit area,

$$\Delta Q \approx \frac{dP}{dT} A_d \Delta T \tag{1-2}$$

which leads to

$$\Delta V \approx \frac{dP}{dT} \frac{d}{\epsilon} \Delta T \tag{1-3}$$

The expression for ΔV shows that for thermal imaging arrays, an applicable figure of merit for the pyroelectric material is $(dP/dT)\frac{1}{\epsilon}$. Triglycine sulfate was selected for use in integrated circuit sensor arrays because it has one of the highest known figures of merit. [1,3]

Because the dielectric constant of TGS increases with increasing temperature along with the pyroelectric coefficient, the dependence of this figure of merit on temperature is less than the dependence of the pyroelectric coefficient, and to a first approximation is almost independent of temperature in TGS from somewhat below room temperature to just below its Curie temperature. Consequently, the necessity of accurately controlling the operating temperature is not as serious as would first be thought from an examination of Fig. 1-1.

Note that a pyroelectric detector has no response to a steady signal (i.e., ΔQ of Eq. (1-2) leaks away through R_d of Fig. 1-2 with a time constant equal to $R_d C_d$). This means that it is necessary to view the scene alternately with a reference (uniform temperature) scene so that the detector output will be proportional to the difference between the scene and reference temperatures. One inherent advantage of this mode of operation is that the detector is insensitive to the background radiation (herein defined as that portion of the radiation from the background equivalent to the reference temperature) because it is, in effect, a steady signal. This relaxes the severe uniformity of response requirements that sensitivity to background imposes on quantum detectors, and makes pyroelectric thermal imaging arrays practical without the necessity of elaborate gain control (responsivity equalizing) schemes.

C. POLYCRYSTALLINE APPROACH

In order that the incident scene radiation increase the temperature of the detector elements as much as possible, it is necessary that the detector thickness be no greater than that required to absorb the radiation, and that they be thermally isolated from their surroundings. Using appropriate values for TGS,[1,4] it is found that a good compromise design occurs when the detector material is about 10-μm thick. This thickness is attainable with polycrystalline TGS films but it is smaller than is permitted by the present state of the art for unsupported single crystal TGS. The polycrystalline approach also inherently provides a way to obtain thin uniform pyroelectric layers that can be readily deposited on thin film integrated circuit substrates.

The technique being developed for providing thermal isolation of polycrystalline TGS detectors from the silicon integrated circuit substrate upon which the detectors are formed is illustrated in Fig. 1-3 for the case of an X-Y addressed array. The upper portion of the Fig. 1-3 shows the top view of a single sensor cell of the 16-by-16 array currently under development. The lower portion of the figure shows a delineated polycrystalline TGS detector supported by a thin thermally grown silicon dioxide membrane that remains after the silicon under the detector has been preferentially etched away. In this manner loss of heat from the detector to the silicon is greatly reduced since the heat must be conducted along the thin silicon dioxide membrane.

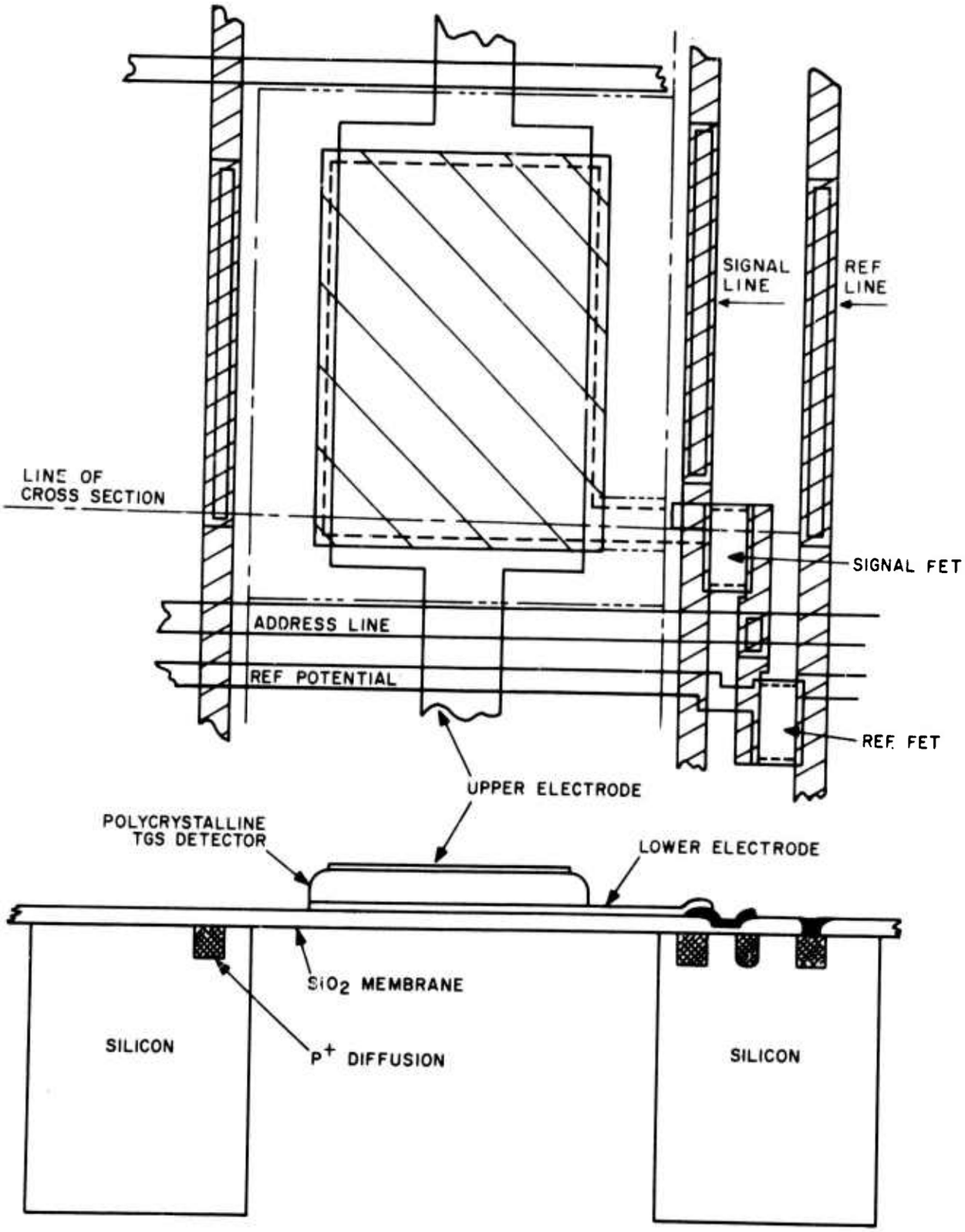


Fig. 1-3. Arrangement of a single sensor cell of a polycrystalline TGS detector array illustrating the thermal isolation technique.

The polycrystalline approach is not as degrading as might be expected because once poled, all the components of spontaneous polarization of the individual grains in the poling direction add coherently and only their perpendicular components are ineffective. This results in a degradation in detector voltage responsivity by nearly a factor of two compared to single crystal detectors. Some advantages of the polycrystalline approach that tend to compensate for this relatively small loss in responsivity are:

1) Small inhomogeneities in the parent pyroelectric source material are averaged out in a composite layer, thus providing a technique for producing large areas of uniform photoresponse without having to impose severe restrictions on the permissible inhomogeneity of the source material.

2) Since the preparative procedures are virtually identical for one single detector as for large two-dimensional arrays of many detectors, this approach is ideally suited for multielement imaging arrays.

3) Some important film properties (e.g. resistivity) are, in principle, independently controllable by judicious choice of fillers and/or "glue" used to cement the component pyroelectric particles into a coherent film.

Some problems associated with the polycrystalline approach should be noted. Although uniform in their electrical properties and capable of being formed on virtually any substrate, the films are difficult to prepare and a number of time-consuming steps are required. Additionally, while single crystal TGS can be permanently poled, as for example by the addition of L-alanine,[5] no technique is presently known for permanently poling polycrystalline pyroelectric films.

D. SINGLE CRYSTAL APPROACH

The use of single crystal material in a pyroelectric/integrated circuit array requires contacting each of the detector elements formed on the thin "freely-supported" section of single crystal material to the silicon integrated circuit substrate. This is accomplished using thin metallic film microfingers. Since thermal isolation is provided by the air gap separating the single crystal pyroelectric slab from the integrated circuit, etching of the silicon substrate is not required. The approach is suitable for use in either X-Y addressed or bucket brigade arrays. The basic arrangement used to achieve thermal isolation of the sensor portion of the array from the integrated circuit is illustrated in Fig. 1-4, which shows a cross-sectional view of a thin single crystal sheet of TGS contacted by means of microfingers to the integrated circuit substrate. A high degree of thermal isolation is provided by the air gap.

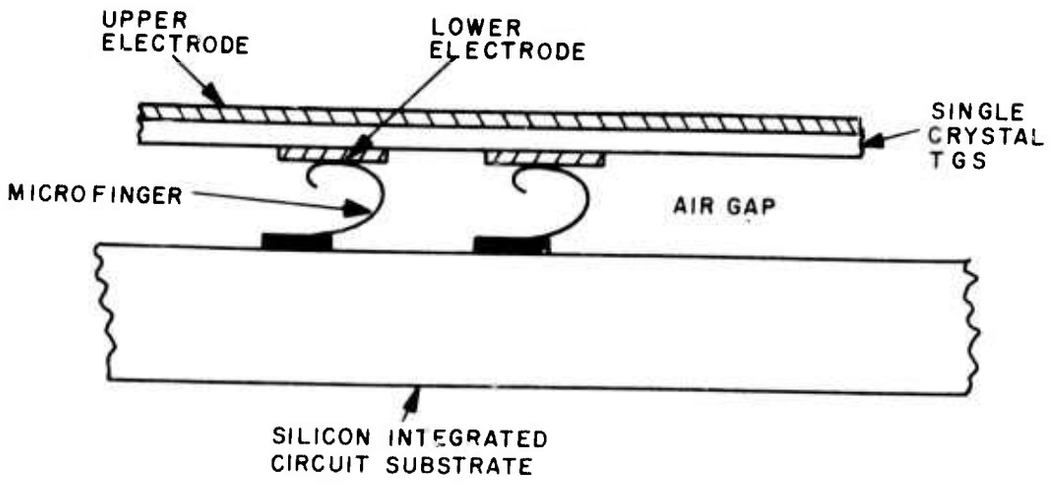


Fig. 1-4. Thermal isolation teehnique for the single crystal TGS array.

The primary advantage of the single crystal approach is that it permits the use of permanently poled pyroelectrie materials. Problems assoeiated with the single erystal approaeh inelude the development of techniques to reproduеibly obtain the thin metallie microfingers, and the development of techniques to further reduee the thiekness of single crystal TGS (presently about 25-μm thick) in order to improve spatial resolution. Additionally, ways must be found to produee uniform permanently poled materials. The problem, to date, has been that small regions of opposite polarization are formed.

E. PYROELECTRIC THERMAL IMAGING SYSTEM

The manner in which the pyroelectric arrays being developed under this program would be utilized in a thermal imaging system is illustrated in block diagram form in Fig. 1-5. The infrared scene radiation, after passing through the aperture of a eontinuous motion shutter, is focused onto the two-dimensional pyroelectric array. As the opaque portion of the shutter eovers the first exposed column of detectors readout of the array is begun, one eolumn at a time. Each eolumn of detectors receives the seene radiation for the full exposure period. The pyroeleetric signals derived from each column of detectors are simultaneously amplified and then multiplexed to form a eorresponding line of scene information on the display. The sequence is repeated with each column of detectors being addressed. Calculations indicate that an array of polycrystalline TGS dctectors, each 4 mils on a side and on 8-mil centers should be eapable of aehieving noise equivalent temperature differcnees of 0.42° C, 0.48° C, and 0.58° C at frame rates of 10/s, 20/s and 30/s, respectively.

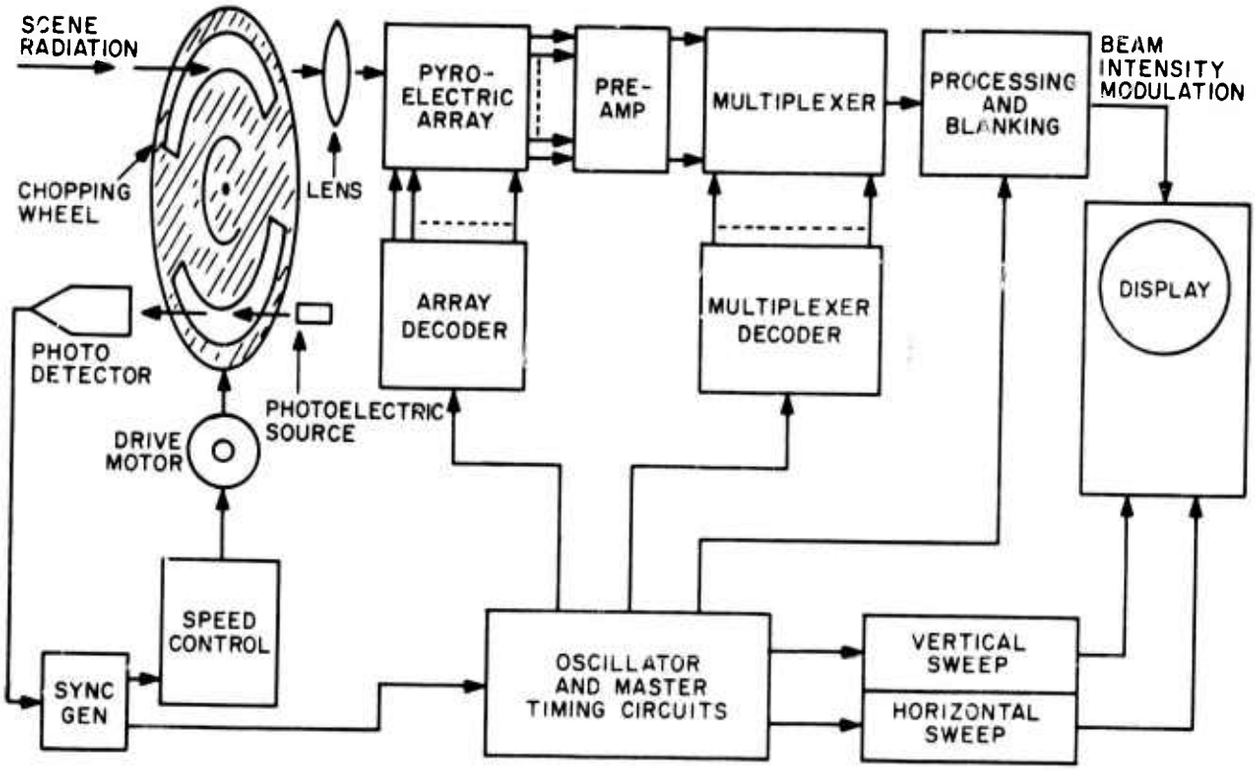


Fig. 1-5. Block diagram of a pyroelectric thermal imaging system.

The remaining sections of this report will describe the progress made to date in developing the technology required to realize the pyroelectric/integrated circuit array approaches mentioned herein. Section II will discuss the progress made in forming polycrystalline TGS films, delineating the films into individual detector elements, obtaining continuous metallization of the upper electrodes, and in providing thermal isolation by preferential etching of the silicon substrate. Section II also summarizes the properties of the polycrystalline TGS films formed to date. Section III describes the single crystal pyroelectric array. Section IV discusses operation of the X-Y addressed array and of the bucket brigade pyroelectric imaging array. In section V an analytical assessment is made of the performance capabilities of an X-Y addressed array containing polycrystalline TGS detector elements.

Section II

POLYCRYSTALLINE TGS (TRIGLYCINE SULFATE) DETECTOR ARRAY FABRICATION TECHNOLOGY

A number of the processing steps employed in the fabrication of a pyroelectric/integrated circuit thermal imaging array are illustrated in Fig. 2-1, which shows a 16-by-16 prototype X-Y addressed array. This array was designed and a number of units were fabricated prior to the present program. The array accommodates 256 10-mil by 10-mil pyroelectric detectors, but the design does not permit thermal isolation by back etching through the silicon. Referring to Fig. 2-1, the first processing step depicted is the formation of a 12,000-Å thick thermally grown silicon dioxide layer over the silicon wafer. This is followed by processing the integrated circuit substrate to form the required array of FETs (field effect transisters), the lower electrodes for the detectors, and the address and sense lines. The next steps shown are: deposition of the pyroelectric film material upon the processed substrate, definition of the active areas, application of the upper electrode metallization over the pyroelectric film material, dicing of the wafers into individual array chips, and finally packaging of the array chips. Not shown in Fig. 2-1 are the steps required to realize thermal isolation between the array of detectors and the substrate, the pyroelectric film densification technique and the steps involved in the preparation of the thin polycrystalline TGS films.

A. PREPARATION OF THIN POLYCRYSTALLINE TGS FILMS

Many materials can be prepared in thin film form by vacuum evaporation or sputtering techniques. However, TGS is a delicate organic compound that quickly decomposes below its melting point (233°C) and at temperatures at which it exhibits appreciable vapor pressure.[6] In addition, TGS is a molecular compound composed of glycine and sulfuric acid molecules, neither of which is very susceptible to being prepared in situ by chemical reactions. Attempts to prepare TGS films by solvent (water) evaporation techniques demonstrated the remarkable ability of TGS to grow into large single crystals. The resulting "films" consisted of large (several millimeters), needle-like crystals on an otherwise bare substrate and were unsuitable for the present purpose. The only known successful techniques are all based on deposition of (preexisting) small particles of TGS into a film and providing some means of holding them together. Beerman[7] and Weiner[8] have made films by mixing finely ground TGS with a binder (plastic) to form a paint which may then be applied to a substrate. The binder, however, "dilutes" the pyroelectric properties of the

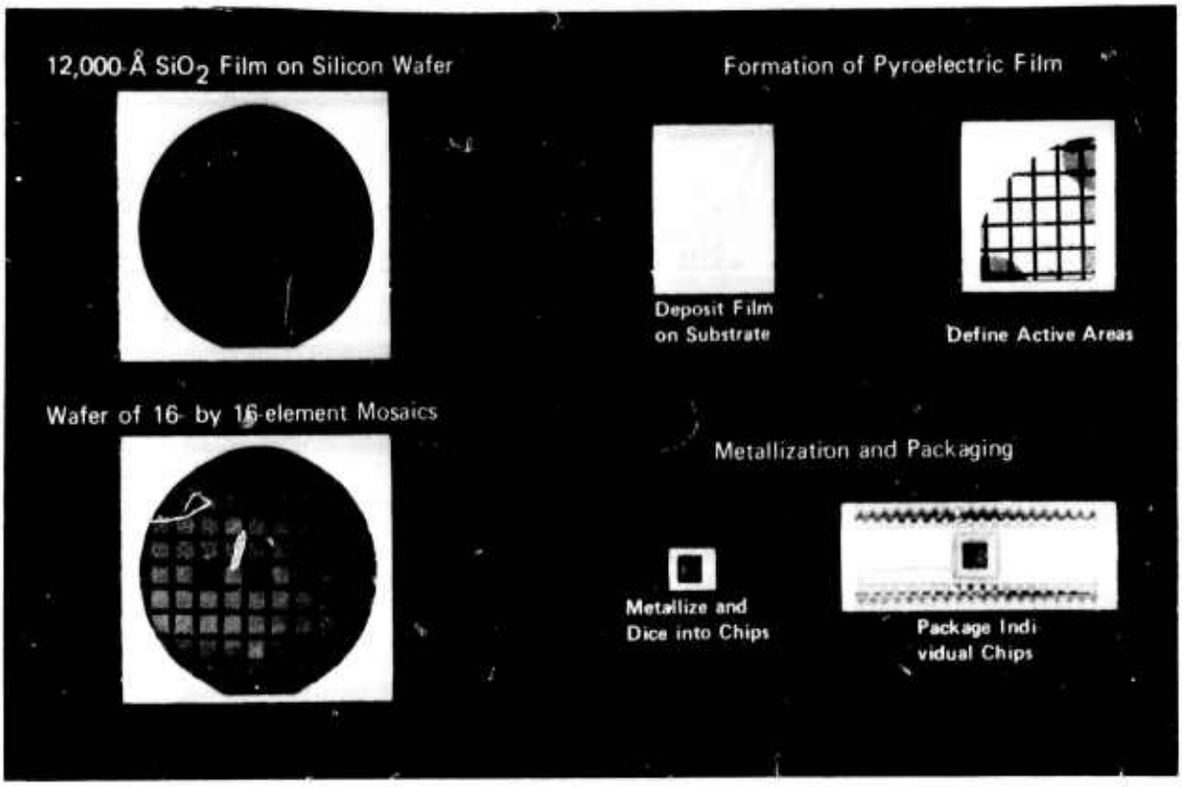


Fig. 2-1. A number of processing steps in the fabrication of pyroelectric/integrated circuit thermal imaging arrays.

film and its use may preclude any possibility of delineating the film into small individual detectors by photolithographic masking and etching techniques. In early RCA work, it was found that relatively uniform thin films of essentially pure TGS could be produced by spraying suspensions containing TGS particles of less than one micrometer in size onto hot substrates or by allowing the particles to settle onto a substrate and subsequently permitting the suspending fluid to evaporate.

1. Suspension Spraying and Settling Techniques

Suspension spraying and settling techniques have been actively pursued under the present contract. The major effort has centered on attaining the prerequisite stable suspensions of submicron sized TGS particles necessary for smooth uniform films. Isopropyl alcohol has been found to be a satisfactory suspending fluid. It is sufficiently volatile for both the spraying and settling processes and exhibits sufficient wettability to TGS and to the intended substrate materials to prevent surface tension induced "balling-up" of the material. However, TGS is slightly soluble in isopropyl alcohol (to the extent of about 0.4 grams/liter at room temperature) and, by so dissolving, introduces the sulfate radical into the suspending medium. The presence of the sulfate radical has been found to increase the tendency of the individual TGS particles to agglomerate and settle. Therefore, in the interest of obtaining and

maintaining suspension stability, one desires to avoid all possible sources of sulfate contamination of the suspending medium. The most effective way found for inhibiting the solubility of TGS is by presaturating the isopropyl alcohol with glycine. In fact, the use of glycine presaturated isopropyl alcohol as the suspending medium has been the largest single factor responsible for the recent attainment of reproducibly stable* suspensions of TGS.

2. Preparation of Submicron TGS Particles

The most satisfactory method of preparing suspensions of submicron sized TGS particles has been ball milling a mixture of the component parts for approximately one week. It has been found, however, that even a small amount of contamination introduced during the milling operation is remarkably effective in altering the physical properties of the resulting film. Therefore, a study was made to optimize the milling operation, as measured by the attainment of stable suspensions with a minimum of milling time and contamination. The best results were obtained using a ball milling jar, consisting of a 1000-ml polyethylene container partially filled with 125 glass marbles and 300 ml of glycine saturated isopropyl alcohol, to which 2 grams of TGS is added just prior to milling. If, after one week of milling, a stable suspension is not obtained, it can usually be made stable by treating it ultrasonically for a few minutes (taking care not to heat it in the process). The contamination introduced by this process has been measured to be about 2% glass, 10% plastic, and 3% glycine. Since glycine is soluble in virtually all TGS etches, its presence does not seriously affect the etchability of the resulting film. The glass and plastic contaminants are another matter and will be discussed later.

In addition to the ball milling process described above, a number of other approaches to obtaining contamination free TGS of submicron particle size were examined. A commercial tungsten carbide grinding mill was found to be far more contaminating than the plastic mill using glass balls.

TGS was also ground in a jet mill which employs two opposing high speed air jets. The material to be ground is introduced into one of the jets. It then passes through a centrifugal separator and the larger material is transferred to the second air jet. The larger material then bombards the incoming material in the first jet. Grinding is thus accomplished by the impact of the TGS particles with each other and should be contamination free. TGS ground by this method has resulted in particle sizes of 3-μm to 5-μm. It should be possible to achieve a smaller particle size by optimizing the operating conditions of the mill and by making more than one pass through the mill.

*Stability is herein defined as no visible settling for several hours to, perhaps, one day.

Precipitation from aqueous solutions was also attempted. A saturated solution of TGS in water was sprayed into isopropyl alcohol which was violently stirred in a blender. After spraying the suspensions were allowed to dry, thus producing a fine powder of water-free TGS. The powder then was put in suspension in isopropyl alcohol. This method produced TGS with a particle size ranging from 0.5-μm to 5-μm. Further improvements in technique should produce in a reduction in particle size.

3. Film Densification

The "as deposited" sprayed or settled TGS films are loosely packed and have only 0.5 to 0.25 of bulk density. In precontract work, RCA densified the films by a water vapor treatment that controllably saturated the film with water and dissolved the TGS (and glycine), holding the grains together. This allowed the existing loose structure of individual grains to collapse and, with subsequent evaporation of the water, to be re-cemented into a coherent film. This process is quite acceptable on all but two points; it does not completely eliminate the granular top surface texture of the TGS layer or the porous structure of the body of the film. The surface roughness and volume porosity are not conducive to good definition of individual detectors by photolithographic techniques, and the granular surface texture introduces undesirable shadowing effects when a thin metallic electrode is subsequently evaporated over the top surface. A photograph of a TGS film formed on a test substrate, showing its condition before and after water vapor densification, is given in Fig. 2-2.

In searching for an alternative technique of densification, a process of rapid melting and recrystallization was explored; this process produced the smoothest surface of any technique known and virtually eliminated volume porosity. However, it was found to be a transient and poorly controllable process which, at best, is capable of producing detectors with only one-third of the voltage responsivity of similar detectors fabricated with the water densification technique. For this important reason,

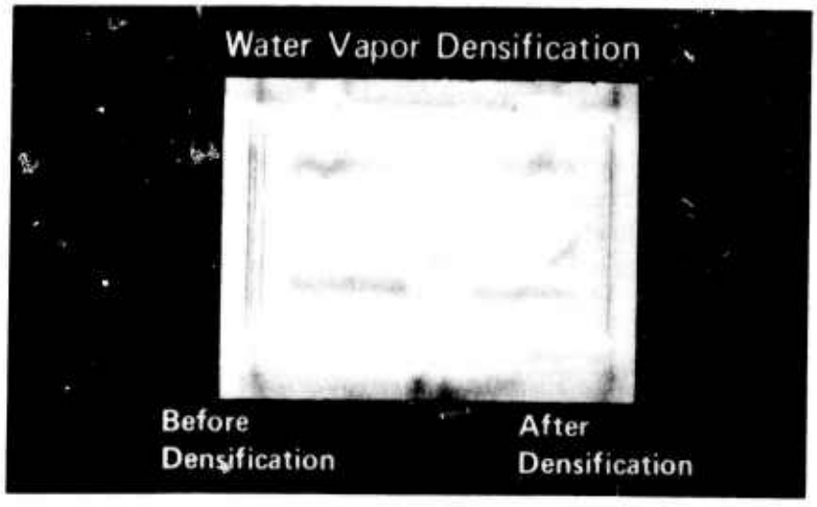


Fig. 2-2. Water vapor densification of a polycrystalline TGS test sample.

the thermal densification process does not a ɐear sufficiently promising to warrant further investigation. Accordingly, ways will be sought to circumvent and/or reduce the surface roughness and porous texture of the water densified films.

4. Laser Evaporation of TGS Films

The laser evaporation technique uses the pulsed output of a laser to vaporize material from a target which subsequently condenses onto a substrate. The technique offers the capability for producing extremely pure films. A typical experimental setup is shown in Fig. 2-3. The pressure and composition of the gases within the vacuum chamber can be varied as desired. Either inert or reactive gases can be used and the evaporating layer can be subjected to both high temperatures and pressures. Consequently, the laser evaporation process is quite different from normal vacuum deposition. Laser evaporation has been used to obtain congruent evaporation of materials which normally evaporate incongruently and to evaporate organic materials without decomposition.

An exact understanding of the processes which occur when a high energy laser beam impinges upon the surface of an organic solid, such as TGS, remains to be formulated. It is believed that the rapid heating produced by the high-power laser beam (10^8 to 10^{10} watts/cm^2) causes the boiling point of the material to be reached in 10^{-7}

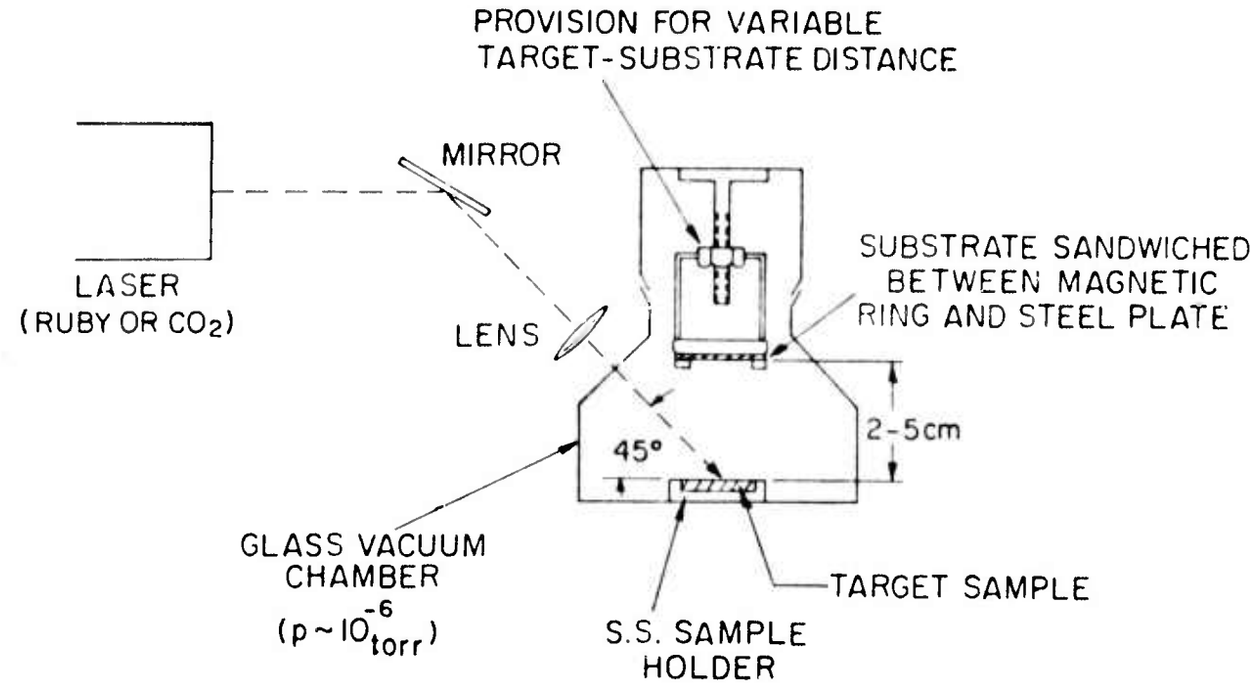


Fig. 2-3. Schematic diagram of laser evaporation process.

second or less. However, since only a small region is heated, large thermal gradients are set up. The heated material is completely vaporized, leaving a crater. The vapor escapes in the form of a plume with velocities of between 10^5 and 10^7 cm/s, exerting a recoil pressure of 10^3 to 10^5 atmospheres.

The organic materials evaporated to date are TGS, polyvinylidene fluoride, and polyvinylcarbazole. They have been found to condense on the substrate with little or no decomposition, based upon infrared spectrograms and x-ray diffraction patterns of the resulting films. Evaporation of organic materials with either a ruby or neodymium laser is difficult, however, because of the low absorption of these materials to 0.694- and 1.06-μm radiation. To increase the absorption, dyes were incorporated into some TGS samples and others were coated with carbon. This led to efficient laser evaporation, but the resulting TGS films were found to be more conducting than could be tolerated for long electrical time constant detectors of the type required in an imaging array. This problem of low film resistivity was overcome by omitting the dyes and carbon coatings and focusing the laser beam to a smaller spot size, thus increasing the power density. However, this method has the disadvantage of causing spalling of the material, resulting in particles being deposited on the substrate.

Films of laser evaporated TGS in the thickness range of 3-μm to 10-μm have been made by the above described method. The material has been identified as polycrystalline TGS by Debye-Scherrer x-ray analysis. The infrared spectrum of the material also indicates that it is primarily TGS with a small amount of an unidentifiable component also being present.

Several laser evaporated films have been fabricated in a form suitable for detector evaluation. The laser evaporated TGS was deposited onto an aluminum electrode on a glass slide. A top electrode of aluminum was then evaporated over the TGS layer. Most of these devices were found to be shorted due to pinholes in the laser-deposited TGS. One device which was not shorted was evaluated further. This film had a thickness of 8.84 μm and a capacitance of 64.5×10^{-9} farads. The loss tangent was 0.55 at 1 KHz and the resistivity 1.1×10^{13} ohm-cm.

It was not possible to observe any hysteresis loop on this specimen. Further evaluation has shown that hysteresis loops cannot be observed on any polycrystalline samples of TGS. This effect may be caused by several mechanisms. Briefly, these mechanisms involve the effect of capacitance between the individual grains, charge leakage, and the fields necessary to pole the individual grains.

The specimen was subjected to a poling field of 23 kV/cm for a period of one hour without shorting. An attempt to measure the pyroelectric coefficient proved to be unsuccessful. It is not presently known why this specimen did not exhibit any pyroelectric effect. X-ray analysis showed that the laser-deposited material was TGS, and it exhibited the birefringence associated with pyroelectric TGS.

The laser evaporation system is presently being modified to operate with a carbon dioxide laser. This system will allow TGS to be much more effectively evaporated due to its high absorption at 10.6-μm. The CO_2 laser evaporated material should be free of contaminants (since an absorbing dye is not required) and free of spalling effects (because vaporization should occur only at the exposed surface).

B. DELINEATION OF FILMS INTO DETECTOR ELEMENTS

Conventional photolithographic masking and etching techniques are being developed as means for delineating TGS films into mosaics of individual detector elements. TGS will neither dissolve in nor react with the common photoresist formulations. On the other hand, TGS is so soluble in water (~330 grams/liter at 20°C) that water alone should serve as a suitable etchant. However, in practice a number of difficulties are encountered in directly applying standard photolithographic techniques to TGS films. For example, the glass and plastic contaminants resulting from the ball milling operation, being insoluble in water, are effective etch retardants. It has been found necessary to remove the plastic from the finished TGS films by boiling in a suitable solvent (e.g. trichloroethylene) before photoresist application, and to perform the etching in a buffered hydrofluoric acid solution to enable the etchant to attack the glass contaminant. Incomplete densification (i.e., intergrain spaces) poses another problem in that pathways exist for the etch under the photoresist mask, causing serious undercutting. Because of roughness of the top surface of the TGS layer it is difficult to obtain pinhole-free photoresist coverage. This condition can also lead to etching out of the TGS under the photoresist mask.

The problems outlined above were quickly identified by analyzing the results of preliminary delineation experiments. Since it appeared that successful delineation depended upon the solution of several prerequisite problems (contamination, densification, surface roughness), these problems were given first priority.

Progress in thin film TGS delineation has recently reached the point where low contamination films with reasonably good surfaces have been made. Since further progress will necessarily involve evaluation of the delineation characteristics of films, an intensified effort in developing a suitable delineation technology was recently initiated. It is clear that future progress will involve an interplay between further improvements in the film preparation procedure and new developments in the delineation technology itself.

C. EVAPORATION OF TOP LAYER METALLIZATION

The lower electrode of each detector comprising the two-dimensional array can be laid down on the substrate prior to the TGS deposition and thus presents no particular difficulty. The top electrode is another matter because it must be deposited on

the granular surface of the delineated TGS detector elements. It must be continuous (electrically conducting), and at the same time be thin enough to be semitransparent (i.e., nonreflecting) to the infrared radiation to be detected.

The rough top surface of the present TGS layers gives rise to nonuniform films (e.g., by shadowing effects) that contain thin spots which dominate in determining the film sheet resistance. These thin spots are very sensitive to oxidization and/or migration effects and can cause loss of electrical continuity. Bismuth metallization has been observed to slowly lose all of its initial conductivity in a few days of air storage, chromium has been observed to rapidly increase in sheet resistance by a factor of from three to infinity when first exposed to air, and aluminum, while not exhibiting strong oxidization effects, has its sheet resistance drastically increased in a few minutes by the passage of large (by the present standards) currents through the film. However, it has recently been shown that the thin spots (i.e., the shadowing effects) can be virtually eliminated by simply rotating (or oscillating) the TGS film during metallization so that the evaporated metal arrives at varying angles of incidence (with respect to the TGS layer) and fills in the shadows. This technique has produced semitransparent films of aluminum that have sheet resistances atop TGS which are within a factor of two of those deposited simultaneously on glass, whereas without rotation there would have been a difference of one to two orders of magnitude (see Fig. 2-4).

Figure 2-5 is a photograph of the apparatus which was built to oscillate the TGS layer during metallization. The holder used to support the TGS samples and a glass monitor slide are shown at the top of the picture in a tilted position. During metallization a motor continually oscillates the holder through a wide angle about the normal. The oscillation frequency (about 1.5 Hz) is high enough that there can be many oscillations in the time required to evaporate the upper electrode, and thus effectively fill in all the shadowed areas of surface granularity that would otherwise occur.

One remaining potential problem in this general area, currently under study, concerns maintaining the continuity of the metallization over the top edge of the delineated TGS detector elements, down the side, and across the (bare) substrate to the associated electronic circuitry. However, it is anticipated that the rotation necessitated by the rough top surface will also be of considerable aid in accomplishing this task.

Electrical shorting between the upper and lower electrodes had been a common failure mechanism in early detectors. At first the shorts were caused by pinholes and/or cracks in the TGS films. Later, when the films were improved to eliminate these defects, electrical shorts appeared during poling or just after top layer metallization. Experiments determined that shorting during poling arose from migration of the chromium electrode material away from the positive electrode, into the TGS layer. Once this effect was recognized, it was quickly demonstrated that it

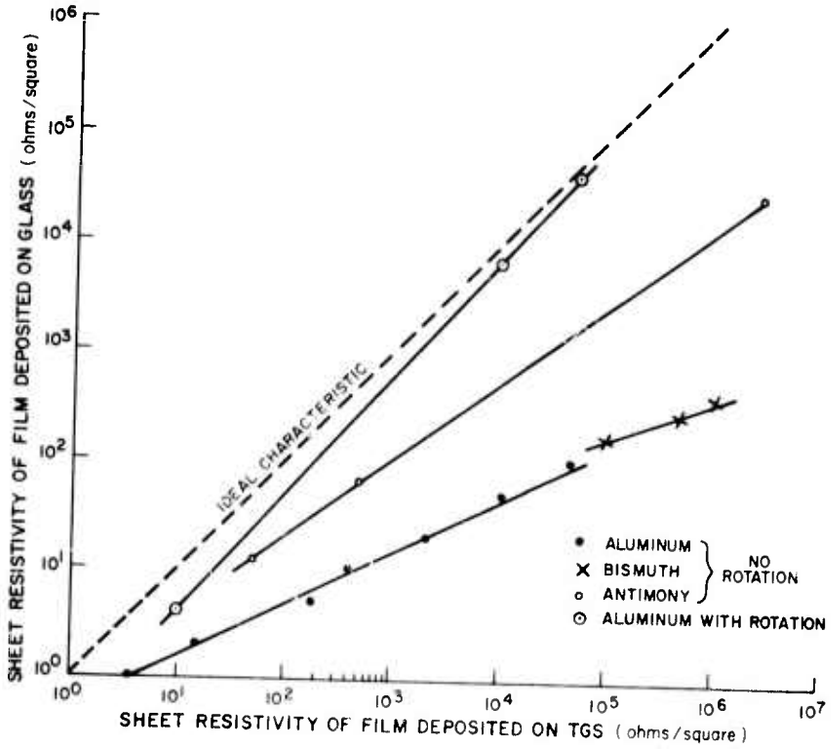


Fig. 2-4. Sheet resistivity of various metallic films deposited on glass and TGS substrates.

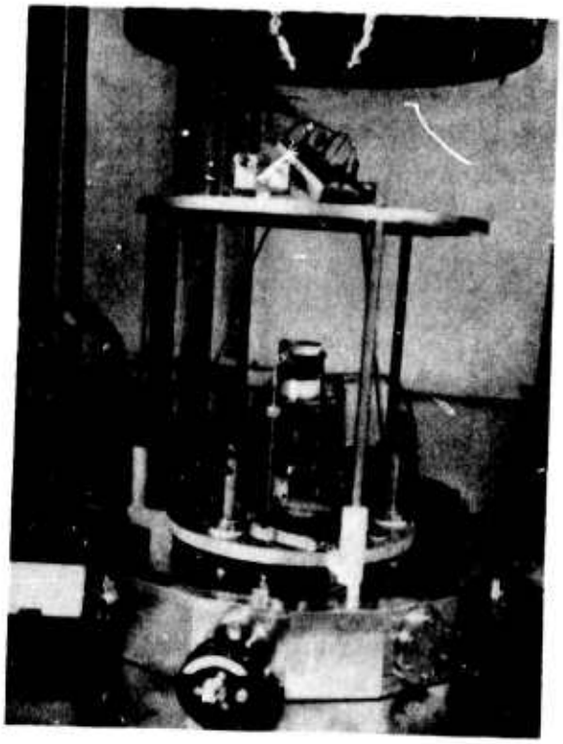


Fig. 2-5. Photograph of the substrate oscillating mechanism used to circumvent shadowing effects during metallization of the TGS top surface.

does not occur when aluminum electrodes are used. Since the use of chromium must be avoided, it may be desirable to select a replacement metal (or alloy) with a very low thermal conductivity in the interest of lowering the heat loss out of the contacts, and improving the desired thermal isolation of the individual detectors. Aluminum, therefore, may not be the ultimate choice of contact material. However, for test detectors which are designed for TGS film evaluation experiments, aluminum is quite satisfactory. A study of the feasibility of using bismuth, antimony, and other low thermal conductivity metals and alloys is in progress. Other metals deemed worthy of evaluation are currently being identified and will be used in evaluation experiments.

D. DEVELOPMENT OF TECHNIQUES FOR THERMALLY ISOLATING THE DETECTORS

In common with other types of thermal detectors, pyroelectric detectors must be provided with a high degree of thermal isolation from their surroundings. Without adequate thermal isolation, the detector's voltage responsivity becomes seriously degraded, resulting in poor sensitivity. Additionally, when arranged in array form, it becomes necessary to prevent thermal communication between detector elements in order to reduce thermal crosstalk to a minimum.

A number of schemes for accomplishing thermal isolation between the detectors of the array and its surroundings have been proposed. In the arrangement using polycrystalline TGS and an integrated circuit substrate, the selected approach is to etch away the silicon from under the regions that would contain the detectors up to the thin (12,000-Å) thermally grown silicon dioxide layer. The etched regions form a series of slots as shown in Fig. 2-6. The long narrow silicon beams that remain contain the FETs required to sample the detectors of the array, with the detectors being formed on top of the silicon dioxide film that bridges the silicon beams. The dominant heat loss mechanism in this arrangement is sideways conduction through the thin silicon

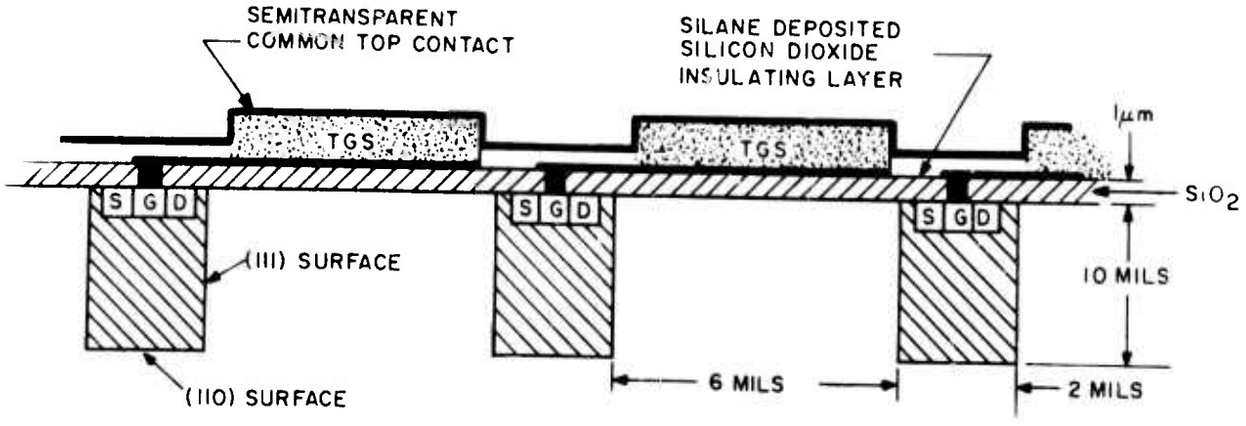


Fig. 2-6. Cross-sectional view of thermally isolated TGS detectors formed over long slots back-etched through the silicon substrate.

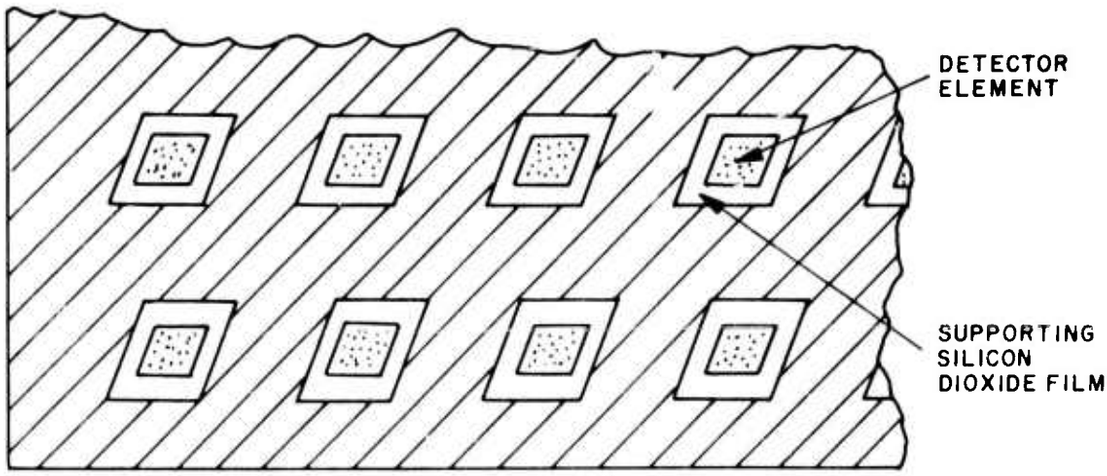
dioxide film and the electrode metallization to the supporting silicon framework. By making the detectors smaller, one can increase the distance over which the heat must flow and accordingly reduce the convective heat flow. These considerations are presented in greater quantitative detail in Section V, where the expected performance of such thermally isolated arrays is assessed.

Preferential Etching of Silicon Substrates

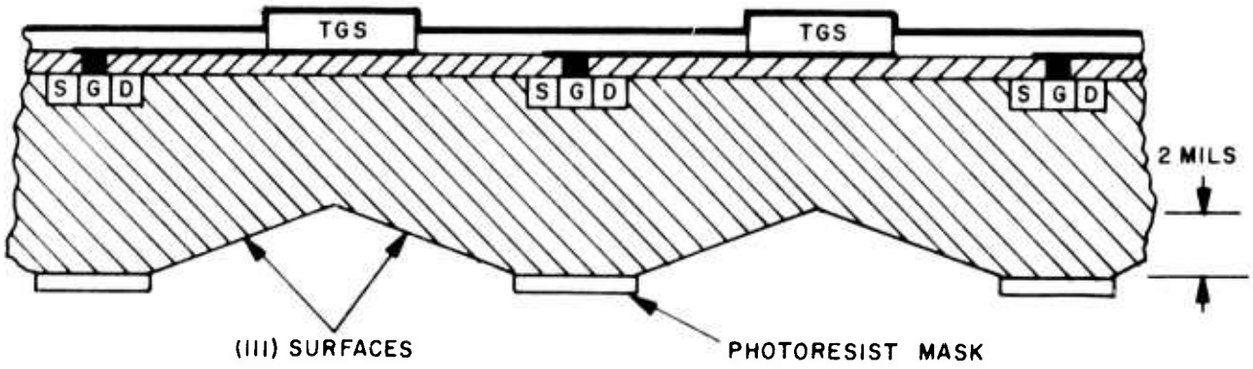
Many alkaline etches for silicon attack (111) crystallographic planes very slowly compared to all other crystallographic planes. Therefore, straight sided holes can be etched out of the silicon substrate if the straight sided surfaces (as shown in Fig. 2-6) are arranged to be (111) planes. For the case of individual holes under each detector (as illustrated in the top view of Fig. 2-7(a)), there are two pairs of opposite sides to be independently specified as (111) planes. This forces the holes to have the rhombic shape shown in Fig. 2-7(a) and requires that the wafer surface be a (110) plane. However, when attempting to etch such holes, one quickly finds that there is yet another set of (111) planes that are not perpendicular to the (110) surface, and the etch exposes these planes before "finding" the desired perpendicular (111) planes. The etching stops when the configuration shown in the cross-sectional view of Fig. 2-7(b) is reached. For the 6-mil wide holes illustrated in Fig. 2-6, the etching stops with the apex of the holes only about 2 mils deep, as shown in Fig. 2-7(b). Although some modifications of this basic scheme exist (such as that shown in Fig. 2-7(c)), they all involve thinning the wafer to less than two mils total thickness, thus materially reducing the strength of the supporting silicon substrate.

However, if one considers slots (i.e., long narrow "holes" spanning many detectors, as shown in Fig. 2-8), the above problems with extraneous (111) planes and the necessity of wafer thinning largely vanish. The disturbing (111) planes give rise to the sloping ends to the slots (as shown in Fig. 2-8), which can be arranged to be outside of the mosaic area proper. Since the sloping ends on opposite ends of the long slot do not meet each other (as they do in Fig. 2-7(b)) the necessity of thinning the wafer never arises.

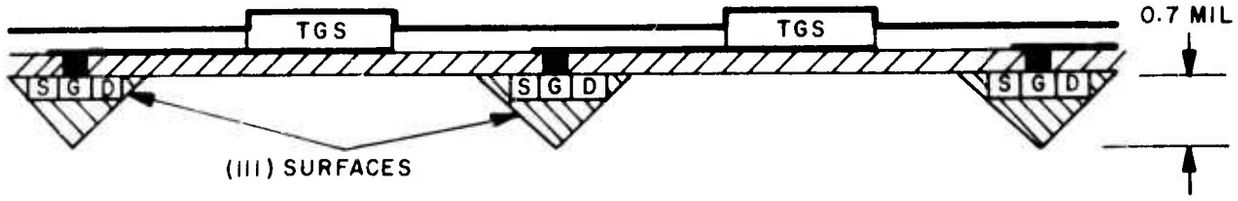
An etch masking technique was recently developed that uses chrome-gold to stand up to the hours of etching required to etch through a standard 8- to 10-mil thick silicon integrated circuit substrate. This technique was used to produce a sample in which a series of parallel slots passes completely through an 8-mil thick (110) oriented silicon wafer, exactly as shown in Fig. 2-8 (including the etched (111) ramps). The slots were approximately 10 mils wide and 0.375 inch long with a bar of silicon approximately 4 mils wide between them. These silicon bars are remarkably strong and the samples withstood unusually rough treatment without breakage. Since both the strength and technology appear favorable for slots, the original idea of holes has been abandoned.



a. Top view of TGS detectors arranged over a mosaic of holes etched in silicon.

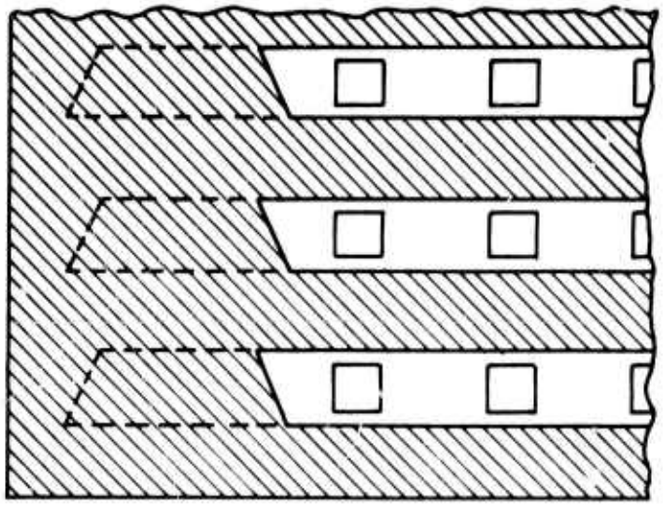


b. Cross-sectional view showing incomplete etch-through in thick silicon substrates.

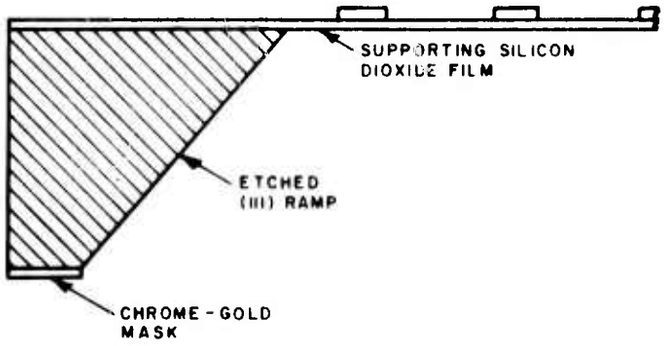


c. Cross-sectional view showing complete etch-through in thinned silicon substrates.

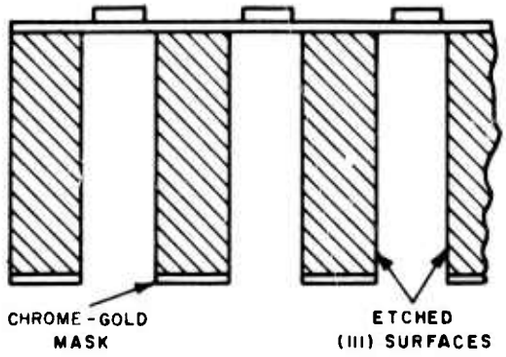
Fig. 2-7. Etching of small holes in silicon and associated problems.



a. Top view of an array of TGS detectors formed over etched-through slots.



b. Cross-sectional view normal to the axis of the slots.



c. Cross-sectional view along the axis of the slots.

Fig. 2-8. Etching of slots through silicon substrates to achieve thermal isolation.

Etching experiments have shown that an etch consisting of 210 grams of KOH, 700 ml of H_2O, and 210 ml of n-propyl alcohol used at 73°C etches (111) planes at 10% of the rate that (110) planes are etched. Thus the undercutting effect can be compensated for by designing an appropriately oversize mask. For a 10-mil thick wafer, for example, the etch mask should extend 1 mil beyond the boundary of the desired slot. The sides of the slot will be a straight (111) planes in spite of the controlled undercutting.

Another feasibility demonstration indicated that a 20,000-Å thick film of thermally grown silicon dioxide spanning a crudely etched 9-mil square hole was also strong enough to survive rough processing and would easily support a TGS detector. These two separate demonstrations of the strength of silicon bars and silicon dioxide films indicate quite strongly that the present approach is, in fact, a feasible solution to the problem of thermal isolation.

Recently, the entire composite structure of bars, slots, and bridging silicon dioxide was fabricated as the ultimate test of strength and technology development. In the one wafer completed to date, the bars and slots had the same dimensions as discussed above, and the bridging silicon dioxide film was only 12,000 Å thick (the thickness presently being considered in the final design). Figure 2-9 is a photograph of this structure as viewed by transmitted light. The silicon is opaque and appears dark in the picture, whereas the silicon dioxide over the slots is transparent and appears light in the picture. Note that the ends of the slots (light areas of Fig. 2-9 are

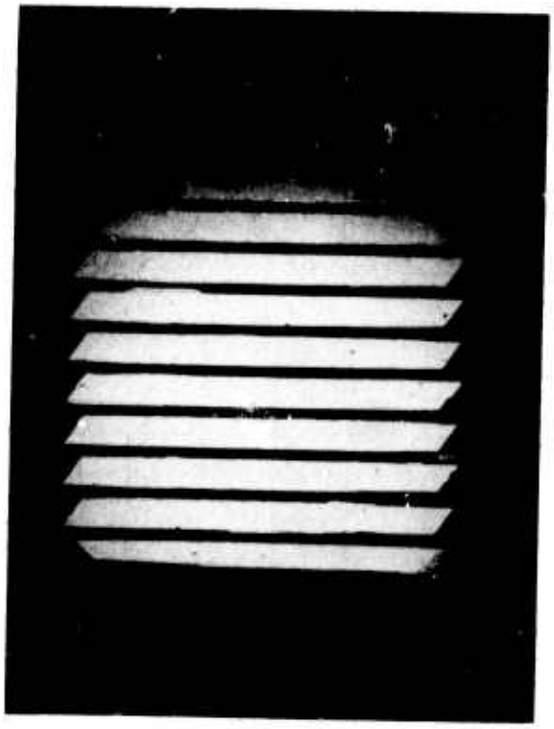


Fig. 2-9. Photograph of silicon dioxide film bridging 10-mil wide slots in an 8-mil thick silicon wafer.

tapered as shown in Fig. 2-8 due to the effects of the sloping (111) planes. The complete structure of slots, bars, and silicon dioxide films has been demonstrated to be a viable approach to thermal isolation; it will be further tested by attempts to deposit and define TGS detectors upon the silicon dioxide film.

The present technique of thermal isolation presents an additional benefit worth noting. Since the circuitry necessary for addressing the detector elements will be confined to the webs of silicon between the slots, and to the unetched framing peripheral area, this isolation technique is fully compatible with standard integrated circuit technology. Nothing must be done to implement thermal isolation except the initial optical polishing of the back side of the wafer so that it will present a smooth surface for the chrome-gold etch mask and for the photoresist used to define that etch mask. Ordinarily the back side of a silicon wafer is left with a rough ground finish; no difficulties are envisioned from its being optically polished. It is only after all standard processing steps are completed (but just before the wafer would be subdivided into individual chips) that the new techniques of etching from the back are initiated. Therefore, no problems of compatibility should arise between the presently proposed thermal isolation technology and the conventional fabrication procedures used in the manufacture of integrated circuits.

E. EVALUATION OF POLYCRYSTALLINE TGS FILMS

Since the technology of making TGS detectors in their final mosaic structure is not yet fully developed, it has been necessary to evaluate the TGS films by fabricating much larger test devices by more conventional means. A very convenient and useful geometry has been an undelineated film (and top layer metallization) atop a 5-mil thick glass substrate upon which a lower electrode has been previously deposited and delineated. Although not thermally isolated, these devices do permit meaningful evaluations of the TGS film properties to be made with a minimum of new technology and/or complex preparative procedures.

1. Dielectric Properties

Viewed in their simplest form, the present detectors are simply capacitors with a TGS dielectric. Room-temperature measurements of such TGS test capacitors at 1 kHz indicate an effective relative dielectric constant of 14.4 and a loss tangent of 0.1. Since the films are polycrystalline with no a priori orientation, an estimate of the expected relative dielectric constant can be made by summing the spatially averaged contributions along the major axes of the TGS crystal. Using the values quoted by Jona and Shirane[9] at 23°C and 500 kHz, one estimates a value of 28.7 assuming bulk density. The lower experimental value of 14.4 is attributed partly to film porosity and partly to the temperature not being 23°C at the time of measurement. If

the temperature were accurately controlled, this technique would afford a convenient way to measure film porosity.

Very little has been reported on the loss tangent of TGS but the indications of present measurements and of results elsewhere [5,10] are that it increases at the lower frequencies of current interest. Measurements of the loss in alanine doped TGS by Lock[5] suggest that doping lowers the ac conductivity by about an order of magnitude. However, to date, such doped TGS has not yielded to repoling, thus effectively ruling out its use in polycrystalline films unless some way can be found to initially deposit the films with the grains all oriented in the same direction. These considerations should be explored further because a high loss tangent is a potential contributor to noise in the completed device.

The dc leakage resistivity was measured to be about 10^{14} ohm-cm when thoroughly dry and about 10^{12} ohm-cm when exposed to humid room air. The latter value compares favorably with measurements on single crystal TGS.[4]

Therefore, except possibly for the loss tangent, the present TGS films appear to have dielectric properties that are well suited to the present application.

2. Poling

The as-deposited TGS films consist of randomly oriented grains that collectively show little or no preferred orientation. It is necessary to pole the pyroelectric dielectric to align all of the spontaneous polarization vectors of the individual grains so that their components along the line between contacts are all in the same direction. If this is not done, symmetry demands (and experiment generally confirms) that the polycrystalline films produce no output voltage when heated.

Poling is most easily accomplished by applying a dc voltage to the TGS capacitor either at room temperature or while the device is cooled through its Curie temperature (49°C for TGS).[9] Figure 2-10 shows how the responsivity of a test detector (which is proportional to the degree of poling) varies with average dc poling field (i.e., applied voltage divided by the film thickness). Notice that electric fields in excess of 30 kV/cm are required for saturation polarization. Unlike single crystals, polycrystalline films are slow to respond to the poling field, often requiring up to one hour to reach equilibrium polarization. Figure 2-10 presents the equilibrium polarization attained after several days of poling at room temperature. Notice that this implies that one can not trade electric field for time — both are needed for effective poling. The one-hour time requirement effectively precludes the standard hysteresis loop methods of studying ferroelectric materials, and other techniques will be required if the need should arise for studying the ferroelectric properties of these TGS films in greater detail.

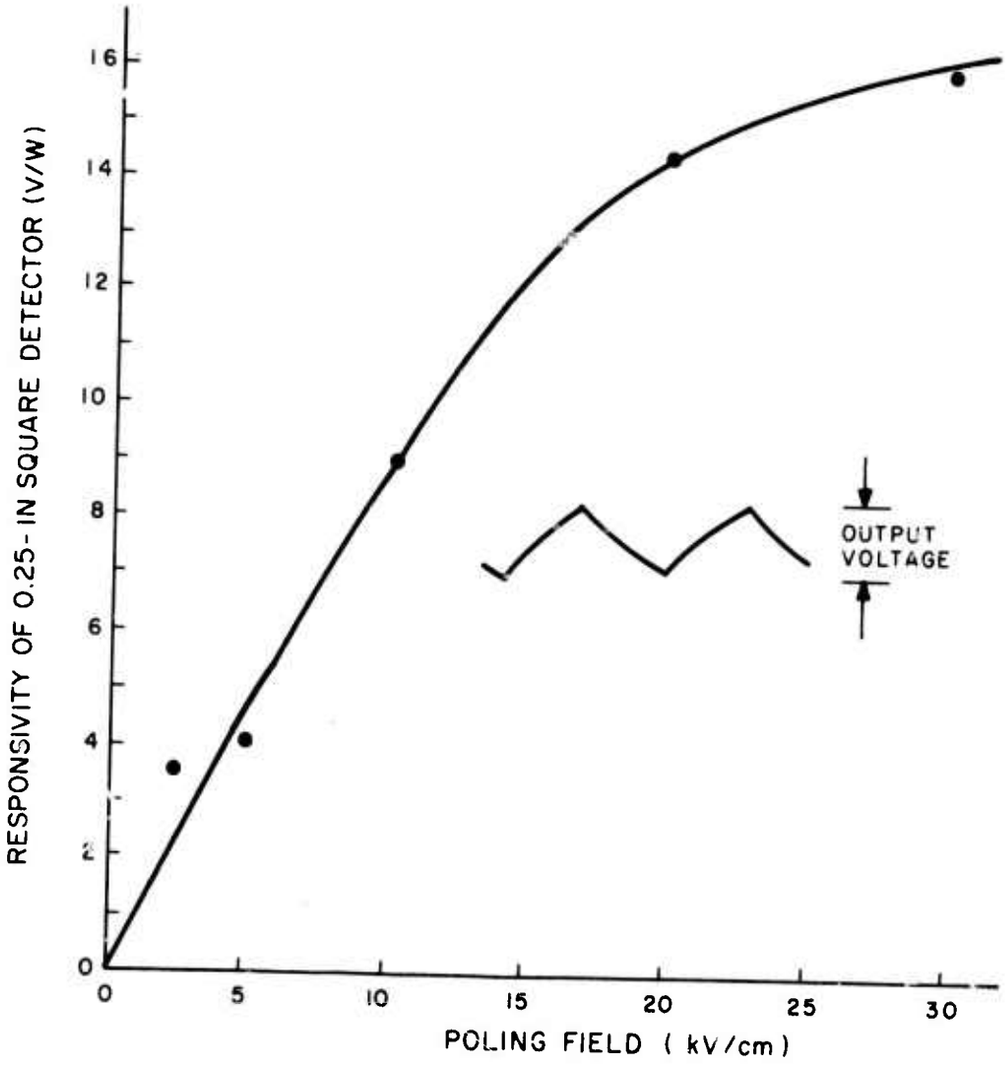


Fig. 2-10. Voltage responsivity of polycrystalline TGS detectors as a function of poling electric field intensity.

Once equilibrium polarization is obtained, the poling electric field can be removed. In a single TGS sample set aside for life test, no degradation in voltage responsivity was observed over a period of several months, indicating that polycrystalline TGS may not require frequent repoling. However, to assure optimum performance, a means for periodically repoling the array should be provided. Since this should only require the application of a dc voltage for approximately one hour, a simple switch (or timer) connected to some appropriate switching circuit may be all that is required.

3. Responsivity

Figure 2-10 also indicates that the saturation polarization from a 20-μm thick polycrystalline TGS detector of area 1/16 square inch leads to a responsivity of about 16 volts/watt (for a 500°K blackbody and a 120-Hz chopping frequency). Experimentally it is found that the responsivity is relatively insensitive to most experimental parameters (details of film deposition, metal used for the electrodes, optical transmissivity of the top layer metallization, etc.) and depends most critically on the TGS film thickness and the thermal loading of the substrate (5 mil thick glass in the case of Fig. 2-10). The measured responsivity of 16 volts/watt is slightly higher than one calculates using published values[8] for the parameters of single crystal TGS and attempting to take the thermal loading of the glass substrate and polycrystallinity into account. It would therefore appear that the attainment of the expected responsivity of the TGS per se will not be a serious problem. The actual system responsivities expected for TGS mosaic detectors of various sizes and degrees of thermal isolation are discussed in Section V.

4. Optical Properties

TGS is quite transparent in the visible and near ultraviolet, thus making it convenient for visual inspection and photoresist exposure purposes. However, over the 8- to 14-μm spectral range of interest it is highly absorbing in both single crystal and polycrystalline form. A 10-μm thick film is sufficient to absorb virtually all of the incident light in this spectral region without the necessity of adding absorbing (black) layers. Any radiation that does pass through the film is reflected at the lower electrode and passed through the film a second time, thus effectively doubling the optical path length. TGS is unique among pyroelectric materials in exhibiting such strong absorbtion over the 8- to 14-μm spectral interval.

The top layer metallization can be thin enough to be transparent while still exhibiting sufficiently low sheet resistance to provide adequate electrical conduction (see Fig. 2-11). In addition, it appears that metallization over the rough granular TGS surface is much less reflecting (and thus more absorbing) than the same thickness on smooth substrates. This was vividly demonstrated when a top layer metallization of 1 ohm/square of aluminum was used in a detector sample designed for electrical evaluation. The aluminum on a companion glass monitor slide was highly reflecting and totally opaque to visible light. The detector, however, exhibited a responsivity that was only a factor of two lower than that measured on similar detectors with visibly semitransparent metallizations of much higher sheet resistivities. Thus, no serious optical problems are anticipated with respect to the top layer metallization.

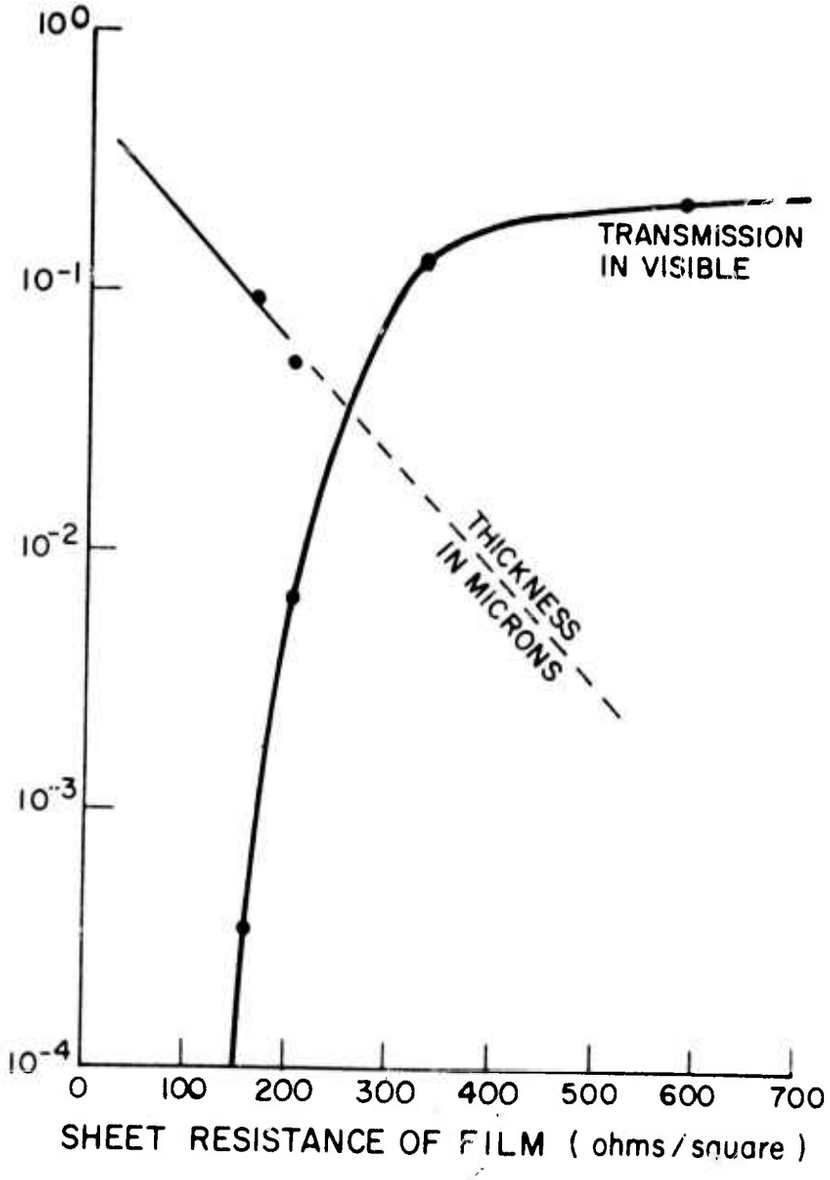


Fig. 2-11. Properties of thin bismuth films on glass substrates.

5. Thermal Stability

TGS is a delicate organic compound that, in time, decomposes (i.e. visibly chars and eventually turns black) at moderately high temperatures. Figure 2-12 shows the effects of a five-minute exposure at various temperatures. The length of time required for visible charring is a strong function of temperature, as indicated in Fig. 2-13. This places an upper limit on the time and/or temperature that is permitted in such processing steps as photoresist drying and thermal densification. At

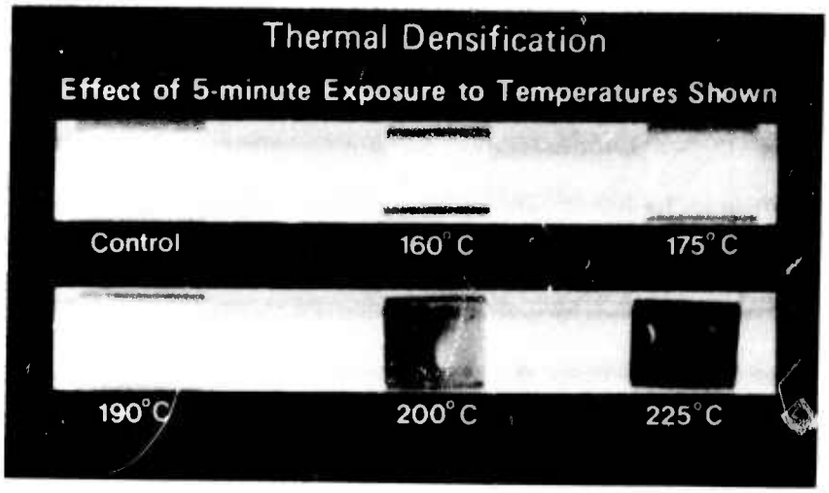


Fig. 2-12. Effects of exposure of TGS to various temperatures.

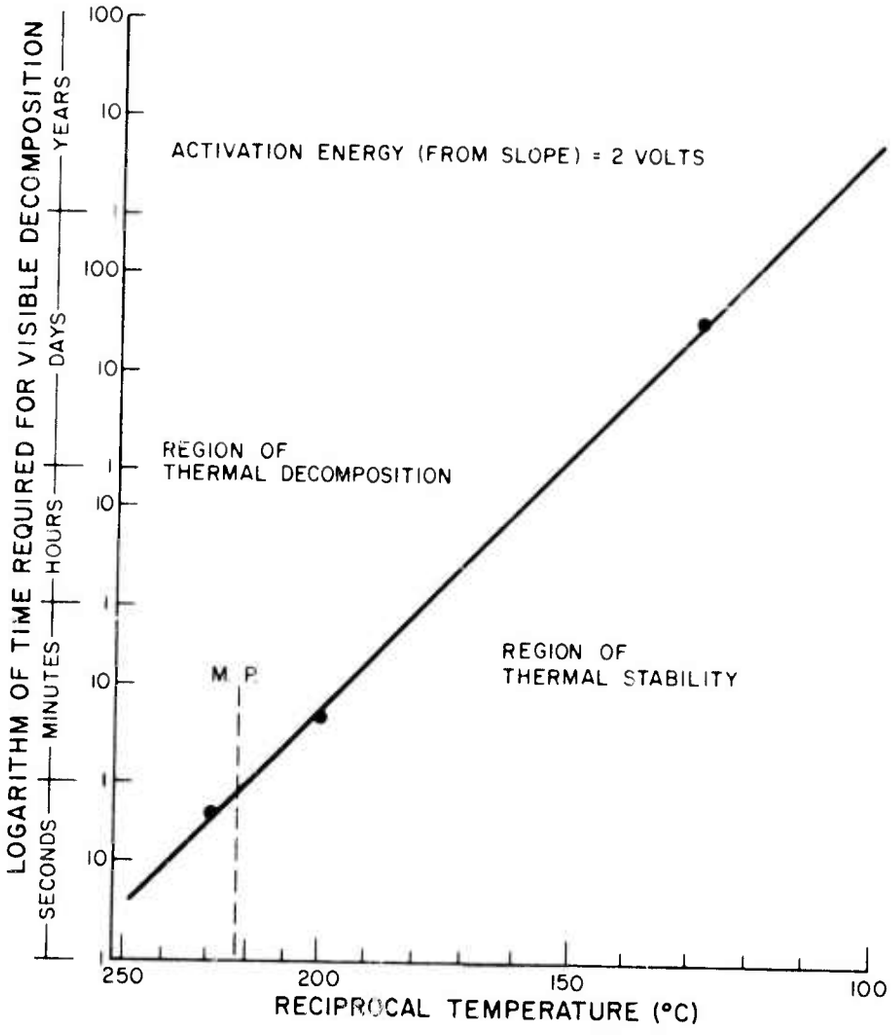


Fig. 2-13. Thermal decomposition of TGS.

its melting point (233°C), TGS visibly chars in less than one minute. However, at commonly encountered storage and operating temperatures (say up to 100°C), the estimated time for visible charring is measured in years. Therefore, no thermal stability problems with TGS (other than possible depoling) are anticipated, and even depoling can be remedied in situ with a repoling circuit built directly into the imaging system.

Section III

SINGLE CRYSTAL PYROELECTRIC ARRAY

A. DESCRIPTION

An alternative approaeh to producing a thermally isolated array of sensors is indicated in Fig. 3-1. Here the sheet of sensor pyroelectric material is a thin single crystal element which is spaced a small distance from the addressing integrated circuit array. Contact is made between the FET (field effect transistor) gates in the addressing array and metal pads on the pyroelectric layer by thin metal springs, the thermal conduetion of the springs being low enough that they do not act as strong heat sinks. A merit of the system is that the material may be permanently polarized before assembly, thus avoiding the need to apply large voltages after connection to the FET gate.

Fabrication of the springs is effected as follows. First, Shipley photoresist is laid down over the substrate, leaving clear areas where the ends of the springs are to be attaehed. Metal fingers are then evaporated through a suitable mask in the sequence 50 Å of ehromium, 1000 Å of gold, and 500 Å of chromium. Finally, the photoresist is dissolved away in acetone. When this is done, the greater tension in the Cr as compared with the Au causes the fingers to curl to the desired radius. Figure 3-2 shows several sueh springs on a substrate of glass with metal crossbars. Figure 3-3 shows a test assembly of fingers before the photoresist is dissolved, each finger having a separate external connection for test purposes. The element spacing in these initial devices is 10 mils. The prescribed thicknesses of metal layers produce a satisfactory curl to the spring; further checks on reproducibility and optimization need to be made.

A eomplete assembly has been made using a small wafer of TGS polished to 1 mil thick. This material was grown from L-alanine-doped solution and thus is permanently polarized. The wafer is mounted on a ring with epoxy resin, and square conducting areas evaporated on the side which will eontaet the springs (Au, 500 Å). The wafer is then aligned with the substrate so the springs contact the areas, a 1-mil thick shim being inserted and attached with epoxy resin. Finally, a ground-plane of gold (200 ohms per square) is evaporated on the exposed surface of the TGS. One such assembly is shown in Fig. 3-4; conneetions are led out from rows of elements. At the time of writing, a separately connected assembly has not been completed.

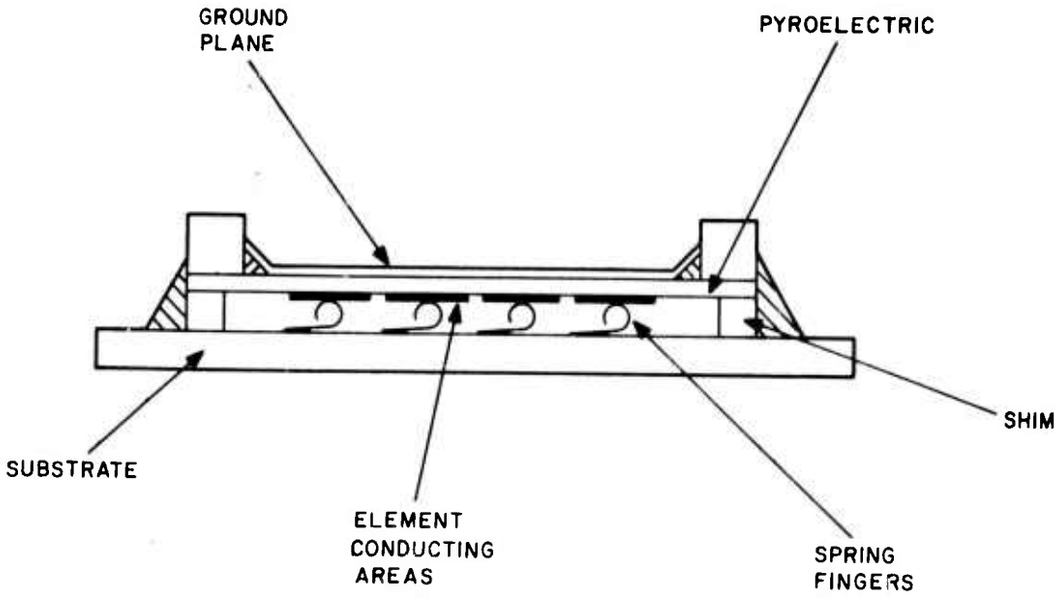


Fig. 3-1. Schematic section of sensor array.

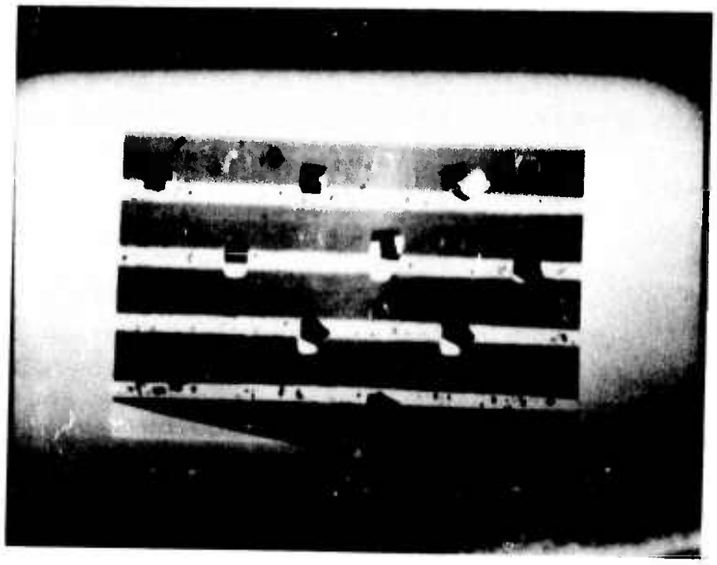


Fig. 3-2. Curled-up spring fingers on strip conductors.

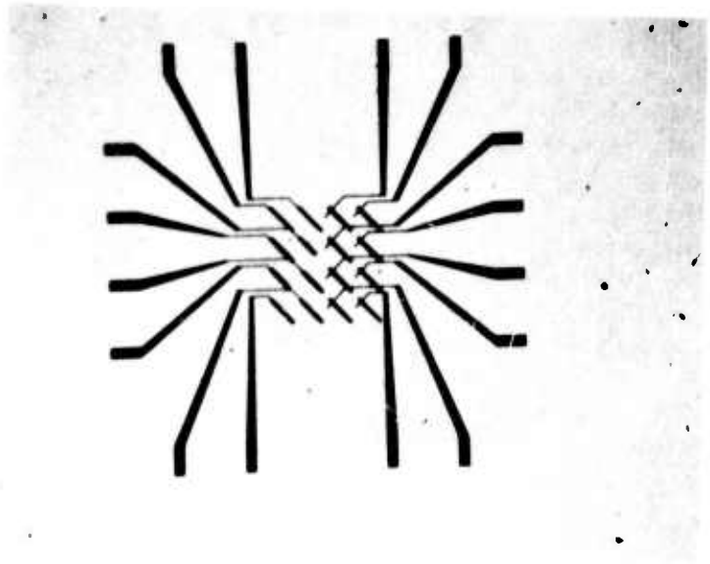


Fig. 3-3. Fingers on fan-out connectors before photoresist removal.

B. MEASURED RESPONSE

The voltage response (peak-to-peak) of the triangular waveform resulting from square-wave excitation, for a wafer with small heat loss, is given by:

$$V = \left(\frac{\frac{dP}{dT}\,\tau}{2\,C_v\,\epsilon} \right) (W/A)$$

where

W/A = incident power/unit area

$\frac{dP}{dT}$ = pyroelectric coefficient

C_v = volume specific heat

ϵ = permittivity

τ = shutter open time

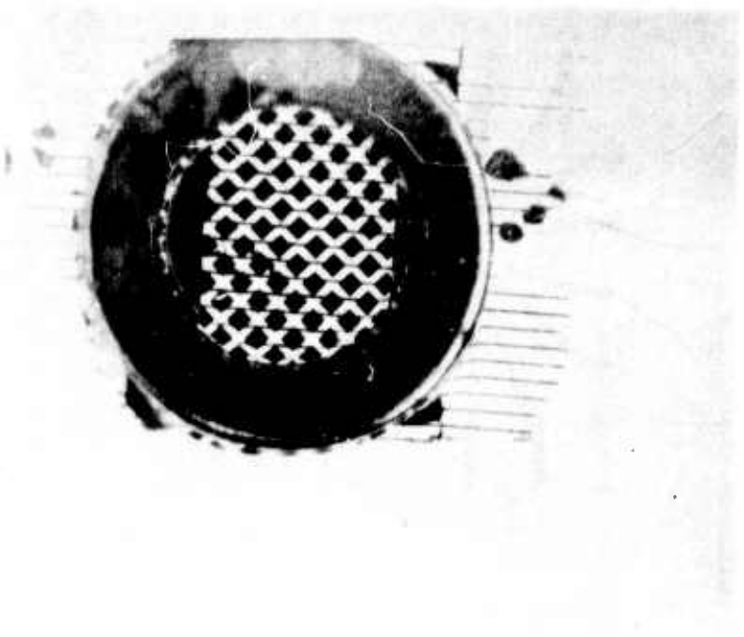


Fig. 3-4. Complete assembly showing separate sensor element areas.

If the source is a black body at 500°K with a 1.5-cm diameter opening 6 cm from the array, and the shutter open time is 1/30 second, the steady-state voltage output into a high impedance has the theoretical value of 390 mV.

In practice this will be degraded by incomplete absorption of incident heat, by the shunt capacitance of the amplifier, and by conductive heat losses. Measurements of the array in Fig. 3-4 give output voltages as follows:

Number of parallel elements	1	2	3
Peak-to-peak millivolts	13	20	30

The capacitance of the amplifier is relatively large, estimated to be on the order of 4 pF, and since the capacitance of the elements is 1 pF, the rise in output with number of elements is to be expected. A low-capacitance amplifier should give an output of about 50 mV, a satisfactorily high proportion of the ideal 390 mV. Referred to a 7-mil square, the active detector element size on this assembly, the responsivity is 3000 volts/watt.

The springs proved to be remarkably elastic, withstanding compression until they were bent almost double without permanent change of shape. The contacts to the

conducting pads on the TGS are believed adequate; they need not be low resistance, since any resistance less than 10^{10} ohms will discharge the sensor element.

C. THEORETICAL CONSIDERATIONS

1. Heat sinking

There are two heat loss paths from the pyroelectric layer; through the metal spring fingers and through the air. Radiative loss is negligible compared with that along these paths. If the dimensions are as follows

Area of element	$A = 1.6 \times 10^{-4}$ cm^2
Thickness of pyroelectric	$d_1 = 10\,\mu$m
Gap between pyroelectric and substrate	$d_2 = 50\,\mu$m
Cross section area of finger	$A_2 = 2 \times 10^{-8}$ cm^2
Total free length of finger	$L = 10^{-2}$ cm
Thermal conductivity of finger	$k_1 = 3$ watt cm^{-1} K^{-1}
Thermal conductivity of air	$k_2 = 2.4 \times 10^{-4}$ watt cm^{-1} K^{-1}

then the thermal conductance of the metal finger and air path in series may be calculated. The thermal time constant is the ratio of the heat capacity of the element to the total thermal conductance, which is

$$\tau_T = \frac{C_v d_1}{k_1 A_2/AL + k_2/d_2} \qquad (3\text{-}1)$$

With the values listed above, which are for 5 mil element spacing, τ_T is 0.02 second. Thus, a loss of signal due to this conduction of about exp $(-\tau_T/\tau_f)$ where τ_f is the frame period, can be expected, that is, a factor of about four normal frame times. A thicker pyroelectric element would increase the thermal time constant but would also reduce the capacitance and thus increase signal loss due to the shunting effect of the amplifier input capacitance. With the above dimensions, the conduction of heat along the finger is approximately equal to the air conduction.

A number of methods of increasing the thermal time constant can be envisaged: thinning the fingers, increasing the air gap, or evacuating the region, but these all bring in increasing technological problems for only small signal increases. There is a considerable advantage in maintaining the thermal constant at close to the frame time, in that the thermal history of the target is not retained and smearing of the image of moving objects will not occur.

2. Spatial resolution

Spatial resolution in this system is limited by lateral thermal diffusion. Calculations have been made of the resolution limit for a bar pattern imaged on a uniform sheet of sensor material and the details are given in Appendix A. The limiting line-pair resolution, i.e., that at which the signal contrast falls to half of that occurring in the absence of thermal diffusion, is

$$d_p = 2.9 \sqrt{D\tau}$$

where D is the thermal diffusivity and τ is the shutter-open time, half the total thermal cycle time. Note that this limit is independent of the thickness of the sensor sheet. For $\tau = 0.03$ s and $D = 5 \times 10^{-3}$ cm^2 s^{-1}, as for TGS, d_p is 3.5×10^{-2} cm (13.8 mils). All the available information in the image can be obtained if three elements are contained in this line-pair spacing, giving an optimum element spacing of 5 mils.

D. WORK PLANNED FOR NEXT PERIOD

The success of the present method of forming spring fingers has led us to proceed with the fabrication of a 16-by-16 sensor array. Masks to evaporate the fingers and form the photoresist cover are being made. The array will be superimposed over the previously fabricated 16-by-16 x-y addressed substrate integrated circuit. This has an array of surface pads available to attach the fingers; although the capacitance of these pads is 1 pF, rather larger than desirable, it should not result in a major signal loss. Attempts will then be made to address the entire matrix electronically and form a thermal image.

Section IV

DETECTOR ARRAY ARRANGEMENTS AND SIGNAL READOUT TECHNIQUES

The pyroelectric detectors used in the thermal imaging arrays of this program are fabricated in the form of minute capacitors. Accordingly, it is necessary to sense the signal voltage from each detector of the array with a high impedance amplifier having minimum shunt capacitance. The small detector capacitance also dictates that the amplifying element associated with each detector be located as closely as possible to the detector to avoid unwanted lead capacitance. The requirements for high input impedance and low input and lead capacitance are readily met through the use of metal-oxide-semiconductor field effect transistor (MOS-FET) integrated circuits. These circuits are used in both types of two-dimensional pyroelectric/integrated circuit arrays under development. In the X-Y addressed array, the FETs serve as switched buffer amplifiers which sample the signal voltage generated by the pyroelectric detectors. In the bucket brigade (BB) array, the FETs serve as switching elements which transfer the signal charge from one pyroelectric capacitor to the other. In both the X-Y and BB image arrays, the image sensor portion consists of a mosaic of thin TGS (triglycine sulfate) detectors equally spaced in two dimensions.

A. X-Y ADDRESSED ARRAY

1. Circuit Layout of the X-Y Addressed Array

A schematic of the X-Y addressed pyroelectric imaging array is shown in Fig. 4-1. Each sensor cell contains a thin film TGS detector and two P-MOS (p-channel metal-oxide-semiconductor) enhancement mode FETs (a signal FET and a reference FET). One electrode of the TGS detector is connected to the gate of the signal FET while the gate of the reference FET is connected to a common line. All pairs of FETs have their sources connected to their respective column address lines, and their drains connected to their respective signal lines and reference lines. The signal and reference lines are connected to pairs of matched load resistors located external to the array, and the outputs of the signal and reference FETs appear as voltages across the load resistors. The signals from each row of sensor cells are sensed in a difference amplifier which is also located external to the imaging array.

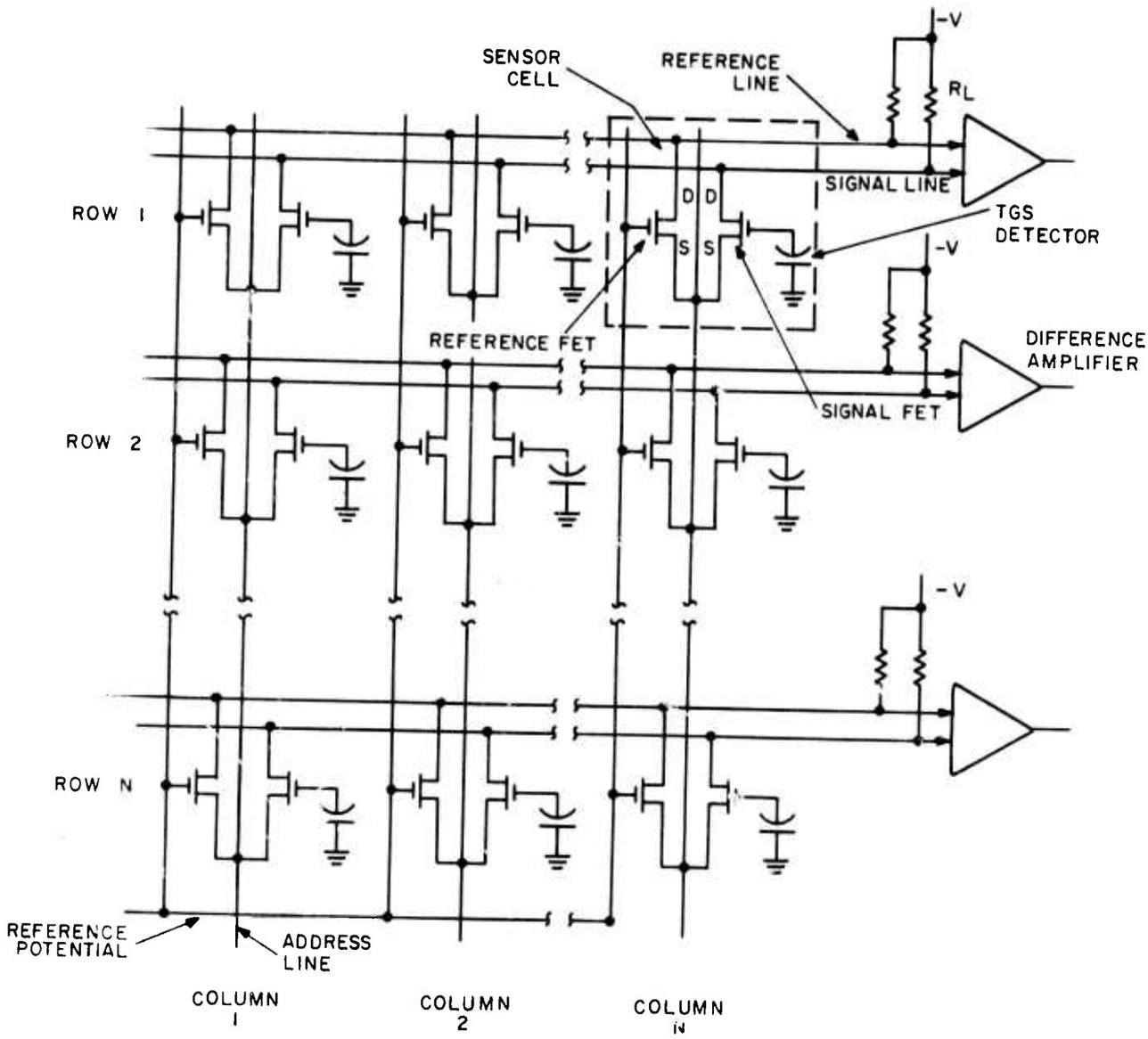


Fig. 4-1. Sehematic diagram of an X-Y addressed pyroeleetrie/integrated eircuit IR imaging array.

2. Addressing Cireuitry and Signal Multiplexing in the X-Y Addressed Array

A sehematie of the array with its assoeiated addressing and multiplexing eireuitry is illustrated in Fig. 4-2. Operation is as follows: the gates of the FETs are initially biased at ground potential. The gate of the referenee FET is tied to a eommon ground bus while the gate of the signal FET is biased at ground potential through the resistance of the deteetor. Two FETs are used per sensor eell and a differenee

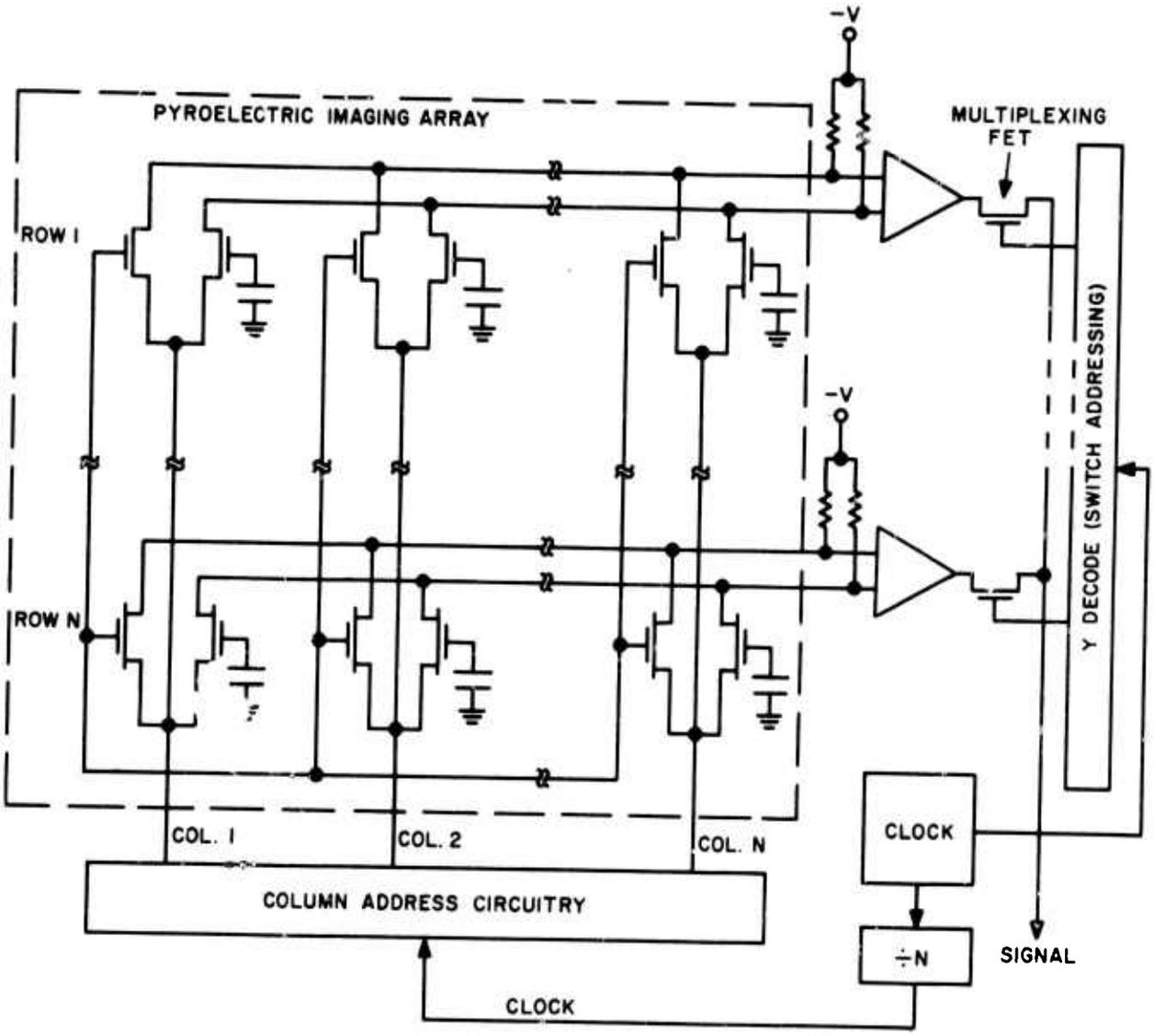


Fig. 4-2. Schematic of an X-Y addressed pyroelectric sensor array, with block diagrams of the addressing and multiplexing circuitry.

amplifier is used for each row of sensor cells in order to cancel the unmodulated outputs of the signal FETs, i.e., the pulse amplitudes from the signal FETs that occur even in the absence of a pyroelectric signal. The pyroelectric signal component can be many orders of magnitude smaller than the unmodulated FET output. However, since each reference FET produces virtually the same unmodulated output as its companion signal FET, a difference amplifier can be used to cancel the unmodulated FET components.

Following exposure to the scene, which would occur by means of a continuous motion shutter, the shuttered column line is pulsed positive, creating a negative gate-to-source potential which biases each FET in the addressed column into saturation (i.e. into conduction). The signal and reference FET output voltages that appear across the pairs of matched load resistors are sensed by the differential amplifiers and multiplexed sequentially onto the video output line by the multiplexing FETs. The addressed column is then returned to ground potential, the adjacent column is pulsed positive and the sequence is repeated as each column of detectors becomes covered by the shutter.

The duration of the column address pulse is t_{ex}/N, where N is the number of columns in the array and t_{ex} is the exposure period. The ON period of each of the multiplexing FETs is t_{ex}/N^2, assuming an N-by-N array and equal exposure and shuttered periods, but the bandwidth of the preamplifiers need only extend to N/t_{ex}.

3. Signal Uniformity in the X-Y Addressed Array

Signal uniformity and fixed pattern noise are prime considerations in the design of any image sensor array. Both the X-Y addressed and the bucket brigade arrays have been designed to obtain high signal uniformity and to minimize fixed pattern noise. In the X-Y addressed array, the arrangement of the reference and signal FETs within each sensor cell takes advantage of the fact that two FETs formed in close proximity and on a common substrate have virtually identical characteristics. The drain currents of the signal and reference FETs may be written, respectively as

$$I_{ds} = K_s (V_g + v_s - V_{Ts})^2 \qquad (4\text{-}1)$$

and

$$I_{dR} = K_R (V_g - V_{TR})^2 \qquad (4\text{-}2)$$

The subscripts s and R denote the signal and reference FETs,

V_g = the applied gate voltage

V_T = the FET threshold voltage

v_s = the pyroelectric signal voltage

I_d = the drain current,

and

$$K = \frac{\epsilon_{ox} \mu_p}{2 t_{ox}} \frac{Z}{L} \tag{4-3}$$

where

ϵ_{ox} = dielectric coefficient of the thermally grown silicon dioxide

μ_p = effective mobility of holes in the channel

t_{ox} = thickness of the gate oxide

Z = channel width

L = channel length

a. Signal and Reference FETs Assumed to be Identical

If we assume that the dielectric coefficient of the oxide, the thickness of the oxide, the mobility of the holes in the channel, and the FET dimensions are identical in both the reference and signal FETs of a particular sensor cell, we may write

$$K_s = K_R = K$$

The output of the difference amplifier to which the signal and reference FETs of the sensor cell are connected is

$$v_o = A_v (v_s - V_R) \tag{4-4}$$

where

A_v = the voltage gain of the difference amplifier

$v_s = I_{ds} R_s$ = the voltage derived from the signal FET

$V_R = I_{dR} R_R$ = the voltage derived from the reference FET.

If the load resistors are made identical, i.e. $R_S = R_R = R$, and if $V_{TS} = V_{TR}$, we obtain for the output voltage from a particular sensor cell

$$v_o = 2 A_v K R v_s (V_g - V_T) \tag{4-5}$$

The FET transconductance is

$$g_m = 2 K (V_g - V_T) \tag{4-6}$$

so that Eq. (4-5) may also be written as

$$v_o = A_v R g_m v_s \tag{4-7}$$

b. Cell-to-Cell Variations Due to g_m

Since some variation in g_m from one sensor cell to another is expected to occur over the area of the integrated circuit array, there will be an accompanying variation in the output of the cells or equivalently a variation in gain from one sensor cell to another. The variation in signal output from cell to cell may be written as

$$\Delta v_o = A_v R \Delta g_m v_s \tag{4-8}$$

where Δg_m represents the expected variation in g_m from one cell to the other. An estimate of the expected variation in g_m can be made from measured variations in I_d under conditions of constant gate voltage and drain voltage. It has been found that in a typical large scale P-MOS array

$$\frac{\Delta I_{d\ av.}}{I_{d\ av.}} = 0.029$$

and

$$\left.\frac{\Delta I_d}{I_d}\right|_{max} = 0.12$$

From Eqs. (4-2) and (4-6) it follows that

$$I_d = \frac{g_m^2}{4 K}$$

which leads to

$$\frac{\Delta g_m}{g_m} = \frac{1}{2} \frac{\Delta I_d}{I_d} \tag{4-9}$$

Based on these calculations, it is estimated that the average variation in g_m will be 1.5%, and that the maximum variation across the entire array will not exceed 6%. The accompanying variations in gain would not be large enough to produce a discernible degradation in picture quality.

e. Signal and Reference FETs not Identical

If the signal and reference FETs within a particular sensor cell are not identical, the net effect, in the absence of subsequent processing, can be a reduction in the sensitivity of the sensor cell, along with gain variations from cell to cell. We will again express I_{ds} by Eq. (4-1), but I_{dR} will now be written as

$$I_{dR} = K_R (V_g - V_T \pm \delta V_T)^2 \tag{4-10}$$

showing that the threshold voltage of the reference FET differs from that of the signal FET by an amount $\pm \delta V_T$. K_R will again be assumed to be equal to K_s, and since δV_T^2 and v_s^2 will be small compared with other products which result when Eqs. (4-10) and (4-1) are expanded, the resulting expression for the signal voltage derived from a particular sensor cell is

$$v_o = 2 A_v K R (V_g - V_T) (v_s + \delta V_T) \tag{4-11}$$

Since $g_m = 2 K (V_g - V_T)$, Eq. (4-11) may also be written as

$$v_o = A_v R g_m (v_s + \delta V_T) \tag{4-12}$$

which may be compared with Eq. (4-7) for which the signal and reference FETs were assumed to be identical.

From Eqs. (4-11) and (4-12) it is seen that if δV_T is much smaller than v_s, no degradation in cell sensitivity and accordingly no degradation in the temperature resolution capability of the thermal imaging array will occur. However, if δV_T is large compared with v_s, the sensitivity of the detector cells will be degraded unless frame storage and subtraction is employed to cancel δV_T.

d. Variation due to Nonuniform g_m and V_T

For a particular sensor cell, say cell number 1, we may write

$$v_{o1} = A_{v1} R_1 g_{m1} (v_s + \delta V_{T1}), \tag{4-13}$$

while for some other cell, say the Nth cell, whose FETs have a g_m differing from g_{m1} by an amount Δg_m, we may write

$$V_{oN} = A_{vN} R_N (g_{m1} + \Delta g_m) (v_s + \delta V_{TN}). \tag{4-14}$$

The difference in output voltage between cell 1 and cell N as seen at the outputs of their respective preamplifiers is therefore

$$\Delta v_o = A_v R \left[g_{m1} (\delta V_{T1} - \delta V_{TN}) - \Delta g_m (v_s + \delta V_{TN}) \right] \tag{4-15}$$

where it has again been assumed that the load resistors are equal and that the preamplifiers have identical gains.

In the absence of a pyroelectric signal, i.e., $v_s = 0$, Eq. (4-15) becomes

$$\Delta v_o = A_v R \left[g_{m1} (\delta V_{T1} - \delta V_{TN}) - \Delta g_m (\delta V_{TN}) \right] \tag{4-16}$$

Ideally, Δv_o should be zero when v_s is zero: a condition that can occur if $\delta V_{T1} = \delta V_{TN}$ and $\Delta g_m = 0$. As previously noted, $\Delta g_m / g_m$ is estimated to have a maximum value of 0.06 for P-MOS FETs. The FETs designed for the 16-by-16 array will have $g_m = 36 \times 10^{-6}$ mhos, so that a maximum Δg_m of 2.2×10^{-6} mhos is expected. The term δV_T is expected to be governed by variations in the density of trapping states in the FET gate regions which is estimated to be on the order of $10^{11}/cm^2$. Based upon measurements made on the existing 16-by-16 array, it is estimated that the cell-to-cell variation in threshold voltage will be on the order of 1 mV for the FETs of the developmental array. For $A_V = 100$, $R = 25\ K\Omega$, $g_m = 36 \times 10^{-6}$ and $\delta V_{T1} - \delta V_{TN} = 1$ mV, $\Delta v_o = 90$ mV, which again indicates that frame storage and subtraction will be needed in the X-Y addressed array.

e. Switching Transients

Switching transients in the X-Y addressed array will be introduced by capacitive coupling of the edges of the address pulses through the array crossover capacitances. The amplitude of the switching transient is given by

$$V_{tr} = \left\{ \frac{C_{\text{cross-over}}}{C_{\text{signal line}}} \right\} V_p$$

where V_{tr} is the peak amplitude of the switching transient and V_p is the peak amplitude of the address pulse. Each array crossover region will have a capacitance of 0.003 pF, and the total of the capacitance between the signal line (which will be a P+ diffused line in the developmental 16-by-16 array) and the substrate plus the capacitance of the metallization attached to the diffused line is calculated to be 3 pF. The amplitude of the switching transients for the above capacitances and for $V_p = 5$ volts would therefore be 5 millivolts. This can readily be reduced to a negligible value without sacrificing frequency response by adding shunt capacitors across the off-chip signal load resistors. For example, by adding a 3-nF capacitor to each signal line the switching transient would be reduced to 5 μV. It should be pointed out that since all outputs appear in parallel before multiplexing, only the first output switched onto the video line will be affected by the transients. The multiplexing switches also introduce transients, but since they occur after the signals are amplified by the difference amplifiers, the multiplexing transients will not be significant. In addition, while one line introduces a positive transient, the adjacent line generates an equal negative transient, tending to cancel some of the transient swing.

f. Address Circuitry and Difference Preamplifier

The address pulse circuitry is illustrated in Fig. 4-3. The circuitry employs active feedback to equalize pulse amplitudes, reducing the common mode requirements of the differential preamplifiers. The amplitude of each pulse is fed back in unity gain fashion to the driving operational amplifier referenced to the desired potential. Switch selection is generated by a "serial in-parallel out" shift register. A single pulse is applied to the input of the register and is sequentially clocked to subsequent outputs of the register. A system utilizing only the register is used to address the multiplexing switches. A photograph of the address circuitry constructed for a 16-by-16-element array is shown in Fig. 4-4, and the first 8 output pulses derived from the address circuitry are shown in the oscilloscope output of Fig. 4-5.

The design of the difference preamplifier is shown in Fig. 4-6. With the values shown, this amplifier has 10-dB gain and common mode rejection ratio of 72 dB. Gain can be increased by increasing resistors R_1 and R_2 at the expense of common mode rejection (due to the high source impedance), but the common mode rejection is more than adequate.

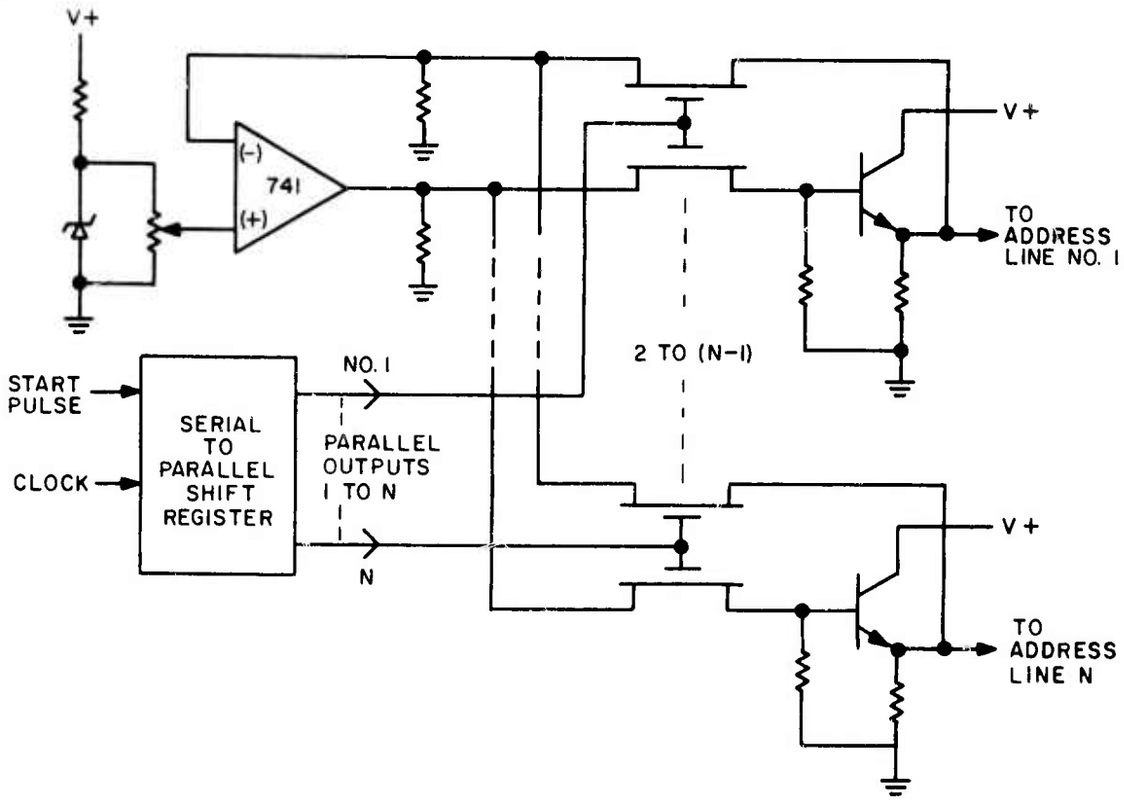


Fig. 4-3. Schematic of column address circuitry.

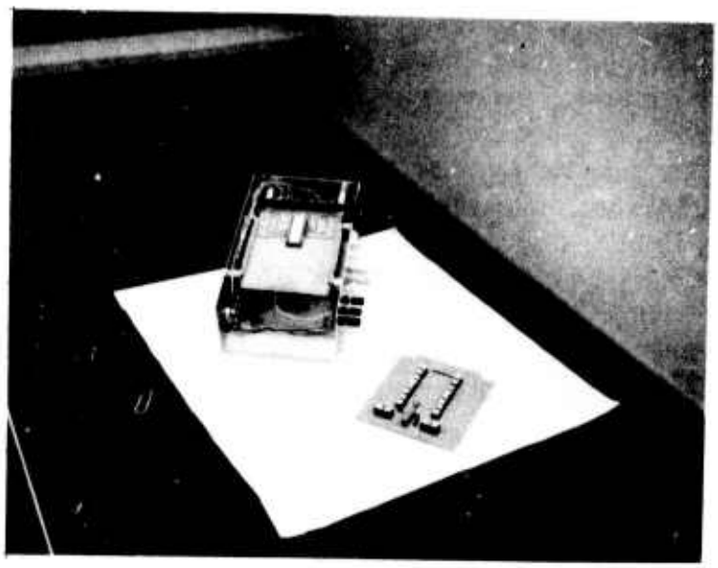


Fig. 4-4. Address circuitry for 16-by-16 TGS array.

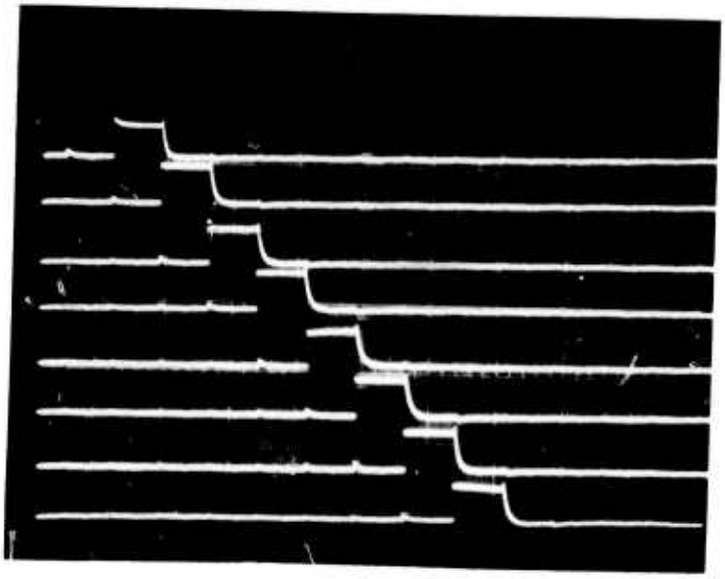


Fig. 4-5. First 8 output pulses from X-Y address circuitry (H: 50 μs/cm; V: 10 V/cm).

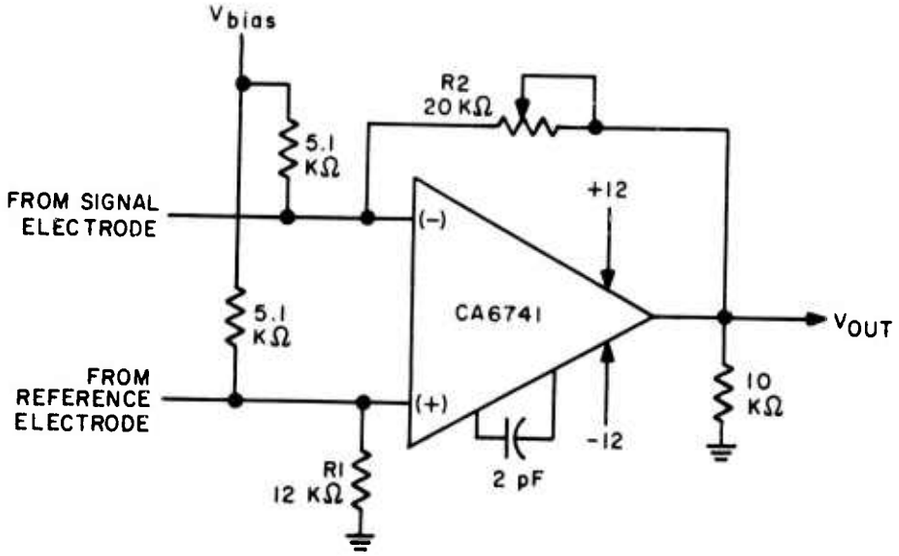


Fig. 4-6. Differential preamplifier circuit.

g. Poling the Detectors on the X-Y Array

Poling of the detectors on the X-Y array must be accomplished in association with the signal FET gate impedance. The effective circuit diagram is shown in Fig. 4-7. The FET gate resistance is several orders of magnitude greater than the TGS shunting resistance. A dc potential applied from top electrode to substrate divides as the resistance ratios and prohibits effective poling in this fashion. Alternatively, if the circuit is pulsed with a current, the capacitors will charge and subsequently discharge through their respective shunt resistances. In this way it is possible to maintain an average value of voltage across the detector and pole it. This has been experimentally accomplished on simulated detector-gate circuits and will be tried on the 16-by-16 test arrays. To date, results have been inconclusive.

4. Noise Model for the X-Y Addressed Array

The noise model employed for the detector-FET combination is shown in Fig. 4-8. The gate referred noise voltage (v_{ng}) of the FET,[11] assumed to be all 1/f components, is given by

$$v_{ng}^2/B = \frac{Q}{ZL\omega} \tag{4-17}$$

The noise voltage generated by the passive elements (v_{nJ}) is

$$v_{nJ}^2/B = 4\,kT\,R_c\,(Z') \tag{4-18}$$

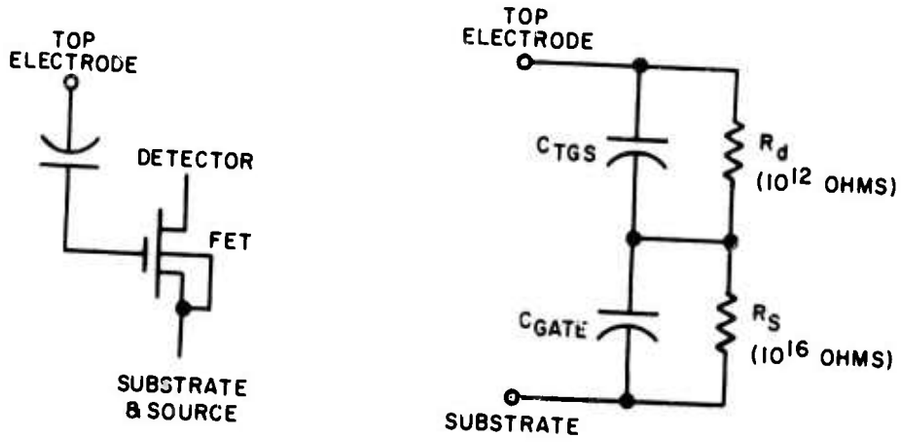


Fig. 4-7. Schematic and model of detector for poling considerations in X-Y addressed array.

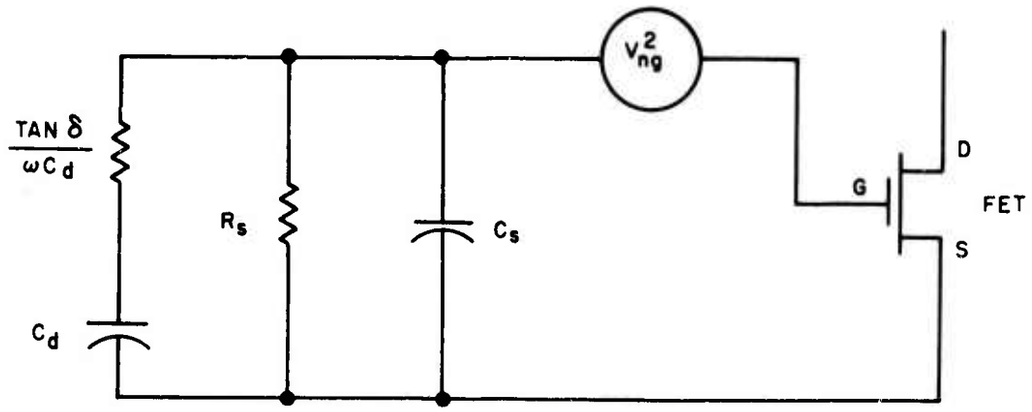


Fig 4-8. Detector-FET combination noise model.

where

B = the requisite bandwidth

Q = a parameter containing processing variables, intrinsic silicon characteristics, energy states, and other factors

ω = radian frequency

k = Boltzmann's constant

T = temperature

Z' = complex impedance

The total noise is the sum of v_{ng}^2 and v_n^2

$$\frac{V_n^2}{B} = \frac{V_{ng}^2}{B} + \frac{V_{nJ}^2}{B} \qquad (4\text{-}19)$$

Total noise over the system bandwidth is found by integrating over the frequency range

$$v_n^2 = \int_{f_1}^{f_2} \frac{v_{nJ}^2}{B}\,df + \int_{f_3}^{f_2} \frac{v_{ng}^2}{B}\,df \qquad (4\text{-}20)$$

Different limits must be imposed on the two integrals as different noise mechanisms exist. The noise generated by the FET is present only during conduction and the mechanism is presumed to be reset when the device is cut off. This sets the lower limit f_3 at one-half the frame rate F. The upper limit f_2 is equal to the maximum signal frequency attainable on one output line, i.e. 0.5 NF. (N is the number of elements in one row; the integrals were actually extended to NF.) Noise mechanisms on the detector are omnipresent, and since it is employed in a sampled system, the lower frequency limit must be extended to zero. Thus f_1 and f_2 are zero and NF respectively. Upon performing the integration,

$$v_n^2 = \frac{Q}{2\pi ZL} \ln 2N + kT \left\{ \frac{1 - \frac{C_d^2}{C_T^2} \tan\delta}{1 + \overline{\tan\delta}^2 \frac{C_a + C_d}{}} \right\}$$

$$+ \frac{kT\,C_d}{\pi C_T^2} \tan\delta \ln \left\{ \frac{4\pi^2 F^2 N^2 R_s^2 C_T^2}{1 + \overline{\tan\delta}^2} \right\} \qquad (4\text{-}21)$$

where

$$C_T^2 = (1 + \overline{\tan\delta}^2)\, C_A^2 + C_d^2 + 2C_A C_d \qquad (4\text{-}22)$$

with

$\tan\delta$ = loss tangent of the detector capacitor

C_d = detector capacitance

R_d = detector shunt resistance

C_a = FET gate capacitance

C_o = FET gate capacitance/unit area

If one assumes tan δ to be small compared with 1, the signal to noise ratio can be optimized by adjusting the FET channel area. This parameter is the one over which there is most control in circuit design. The signal voltage to noise voltage ratio (S/N) is

$$S/N = \frac{v_s' C_d}{C_d + ZLC_o} \Bigg/ \sqrt{\frac{kT}{C_d + ZLC_o} + \frac{Q \ln 2N}{2\pi ZL}} \qquad (4\text{-}23)$$

and

$$S/N_{opt} = \frac{\sqrt{C_d}\, v_s'}{\left[kT + \frac{C_o Q \ln 2N}{\pi} + 2\sqrt{C_o kT + \frac{C_o^2 Q \ln 2N}{2\pi}}\sqrt{Q \ln 2N} \right]^{1/2}} \qquad (4\text{-}24)$$

where v_s' is the signal voltage generated by the detector with no shunting capacitance. Equation (4-24) shows that S/N increases with detector capacitance and with decreasing surface state density (implied in Q) and has been used to design the FETs for the X-Y addressed arrays analyzed in Section V.

B. PYROELECTRIC BUCKET BRIGADE SENSOR ARRAYS

A bucket brigade register is a device for transferring or delaying analog signals.[12,13] Two modes of operation are possible. The signals may be introduced serially at one end of the register and transferred to the output end, or they may be introduced in parallel at the different storage locations of the array and shifted out serially. The latter mode of operation can be utilized to form a two-dimensional pyroelectric sensor array. A partial schematic of a bucket brigade register is illustrated in Fig. 4-9. Operation is such that when the clock line labeled ϕ_1 is pulsed, transistors T_1, T_3, and T_5 are biased into saturation, acting as source follower amplifiers with capacitive loads supplied by the capacitors labeled C_2. The C_2 capacitors are charged to a reset potential, with the amount of charge required being supplied by the C_1 capacitors. The analog signal that is transferred in the register (from left to right in Fig. 4-9) consists of variations in the potential across the C_1 capacitors. Clock ϕ_1 then goes off and the line labeled ϕ_2 is pulsed, repeating the above sequence with alternate transistors (labeled T_2 and T_4) and capacitors, thereby shifting the charge variation one more step along the register. The potential of the last capacitor in the register is sampled, yielding the output signal, or the drain of the last transistor may be tied to a resistor and the charging current monitored.

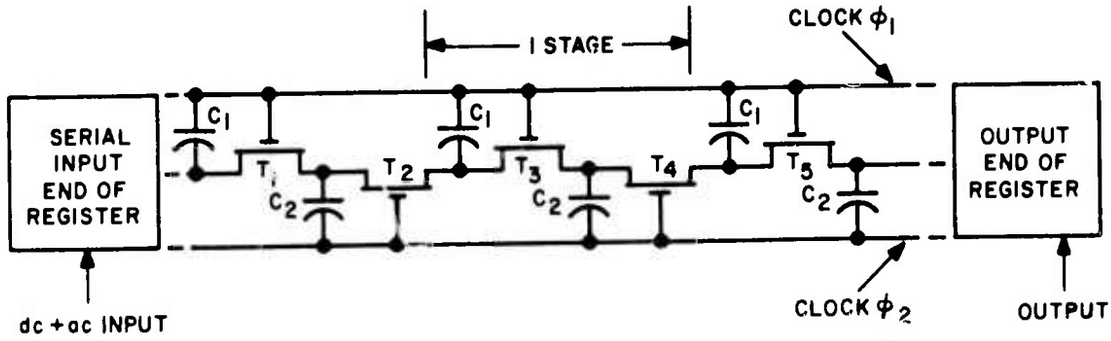


Fig. 4-9. Partial schematic of MOS bucket brigade register.

1. Two-Dimensional Pyroelectric Bucket Brigade Imaging Array

A pyroelectric bucket brigade array can be made, utilizing the circuit of Fig. 4-9, by replacing the capacitor labeled C_1 with pyroelectric detector elements having the same capacitance. The temperature-induced change in detector charge during exposure to the infrared scene can be transferred out of the array in much less time than the detector electrical leakage time constant. A two-dimensional pyroelectric bucket brigade thermal imaging array, composed of N linear bucket brigade registers, each register having N detector elements, is illustrated in Fig. 4-10. The clocks are gated to one register at a time, allowing total readout of each linear register. Clock gating is performed sequentially, register to register, until the entire array has been scanned. The register outputs are simultaneously multiplexed onto a common output electrode.

Referring to Fig. 4-10, electrodes A_1 through A_1' are pulsed simultaneously by a common decoder. This decoder may be the same as that illustrated for the X-Y addressed array but without the active feedback portion of the circuit. The buffer amplifier is a simple source follower amplifier consisting of two FETs.

During readout of a bucket brigade register, all of the charge contained at each storage location, i.e., at each pyroelectric detector, is removed and accordingly thermal memory is automatically eliminated. The size of the array along the direction of transfer eventually becomes limited by the efficiency with which charge can be transferred. It is believed that arrays containing up to 500 by 500 pyroelectric detector

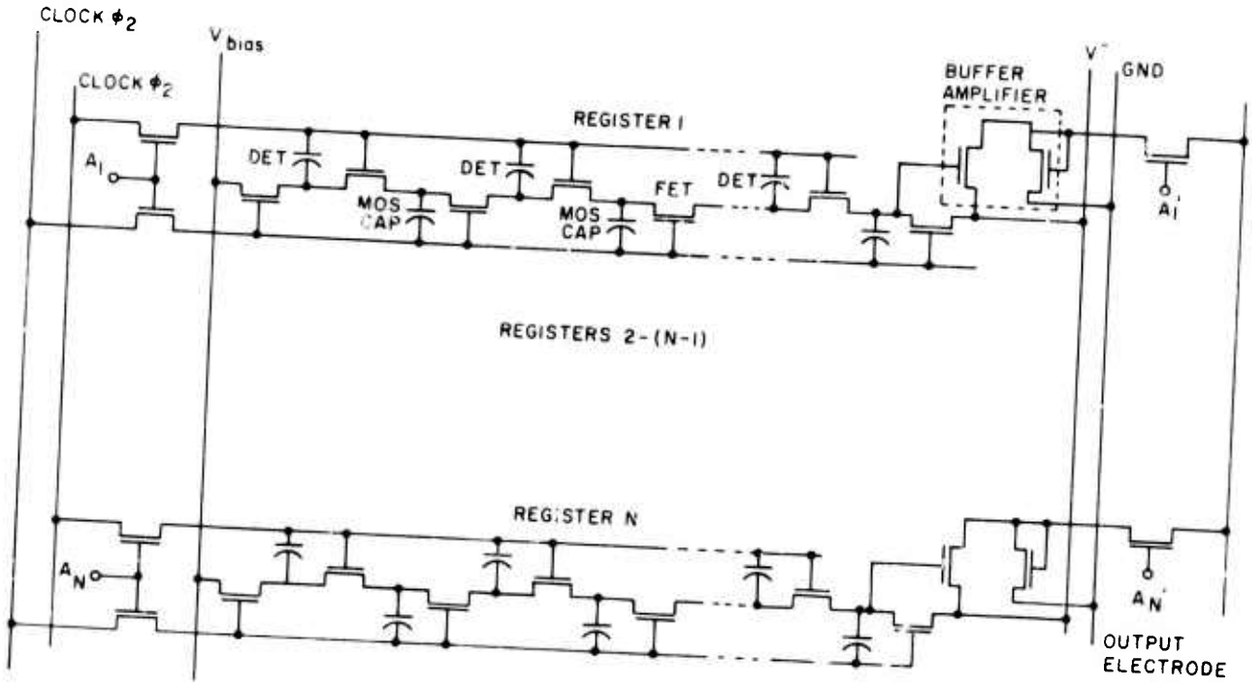


Fig. 4-10. Partial schematic of a two-dimensional pyroelectric bucket brigade imaging array.

elements should be possible. It should be noted that the pyroelectric bucket brigade layout is entirely compatible with both types of thermal isolation techniques discussed in Section II.

A one-by-sixteen linear integrated circuit array has been designed and is presently being fabricated. A photograph of the driver constructed for the 16-element TGS array is shown in Fig. 4-11 and a scope trace of the output pulse is shown in Fig. 4-12. A 16-by-16-element TGS bucket brigade array has also been designed and the necessary masks are being prepared. In this array, the buffer amplifiers will be fabricated on the chip. The integrated circuit layout of one detector cell in the 16-by-16 bucket brigade array is shown in Fig. 4-13.

2. Poling of Bucket Brigade Detector Arrays

Poling of the detectors on a bucket brigade array is performed by applying a dc potential across the clock line connected to one detector electrode and the substrate of the array. The potential is connected to the lower electrode through the forward biased source-drain resistance of the FETs. Operation of the register also imposes a potential across the detector, tending to maintain the poling of the detectors during operation.

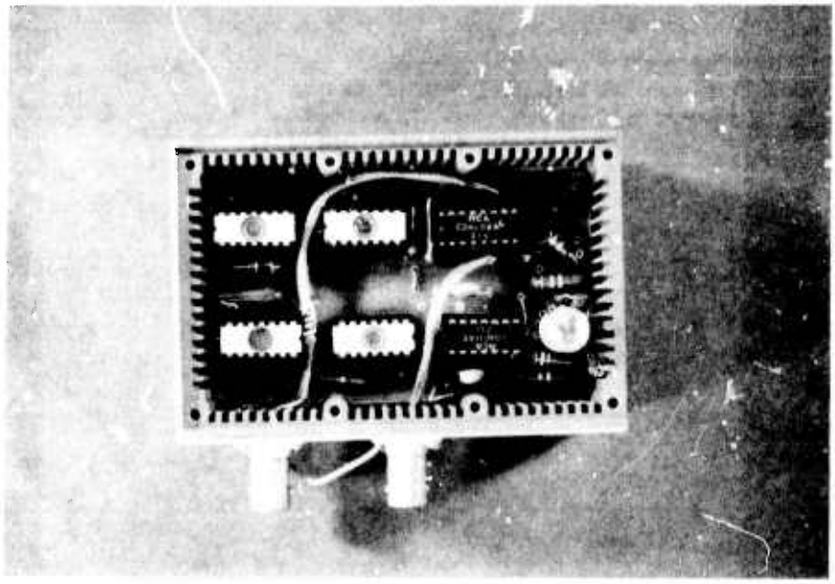


Fig. 4-11. Driver for 16-element TGS bucket brigade sensor array.

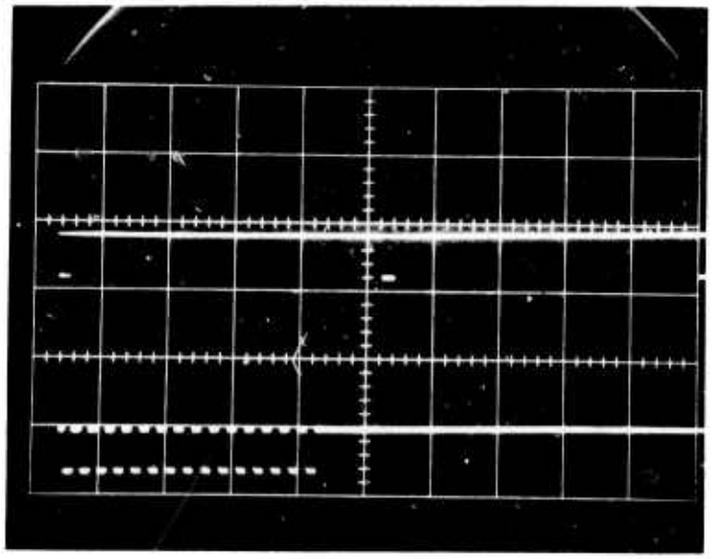


Fig. 4-12. Bucket brigade driver output pulses. (Upper trace - H: 5 ms/cm, V: 10 V/cm. Lower trace - H: 0.2 ms/cm, V: 10 V/cm).

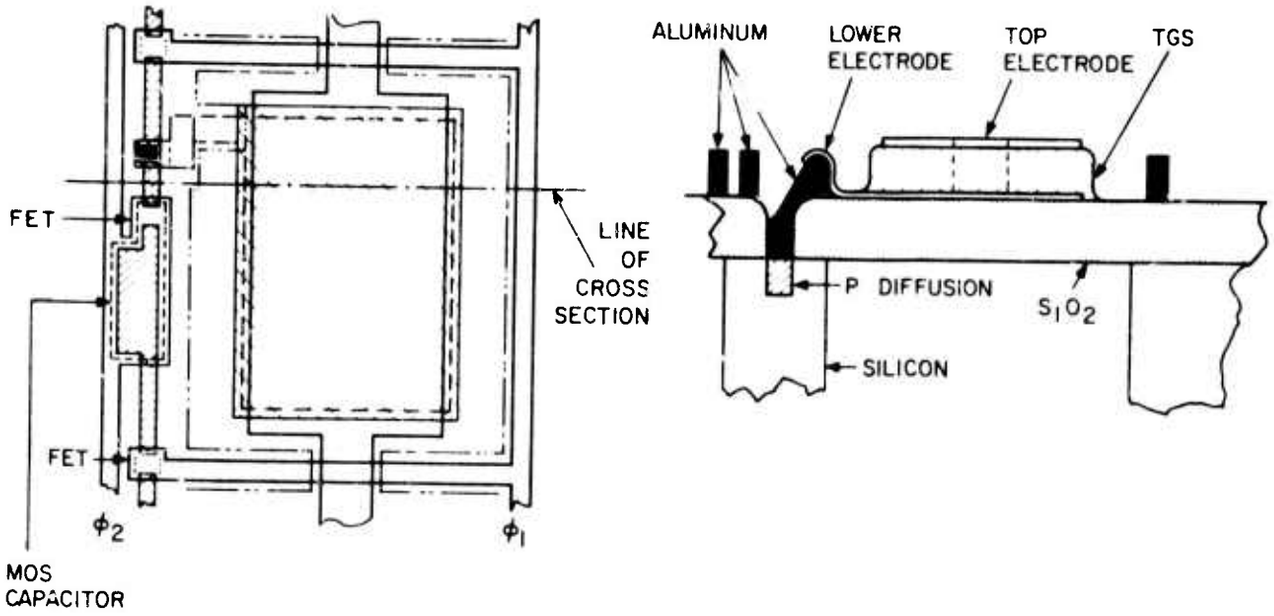


Fig. 4-13. Bucket brigade detector structure.

3. Noise Considerations in Bucket Brigade Arrays

At present, a satisfactory noise model for bucket brigade registers is not available. In addition, it is very difficult to measure the absolute value of noise at the output of a register due to its particular type of output signal. In an attempt to determine the low level signal handling capability of a bucket brigade register, a 16-bit register was constructed of discrete FETs and capacitors. Low level analog signals were introduced into the register. The amplitude of the signals was lowered until the output became obscured by noise. Results indicate that signals with amplitudes of less than one millivolt can be handled with S/N ratios equal to 1. Alternate capacitors in the discrete component bucket brigade register were replaced by TGS detectors. No degradation in system performance was noted. The circuit was then set up to operate as a line scan sensor array, but the large leakage currents due to the discrete FETs used in the register completely degraded the IR signal, making the test inconclusive.

In order to avoid the large leakage currents of discrete FETs (which are due to package leakage) a new linear bucket brigade array was recently assembled using unpackaged FETs mounted on an alumina hybrid circuit board. The array, which contains

12 discrete TGS detectors formed on a glass substrate, is shown in Fig. 4-14. Testing of this array is now in progress.

Figure 4-15 shows a block diagram of the system utilized in signal level investigation. Figure 4-16 illustrates the circuitry for operating a linear bucket brigade register as a line scan sensor array.

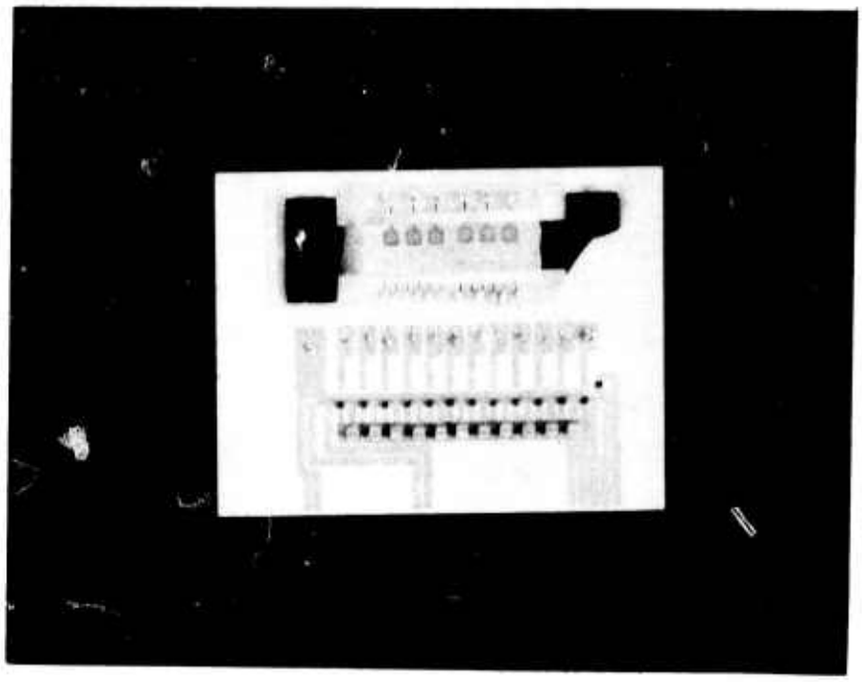


Fig. 4-14. Twelve-element discrete component TGS bucket brigade sensor array with hybrid FETs.

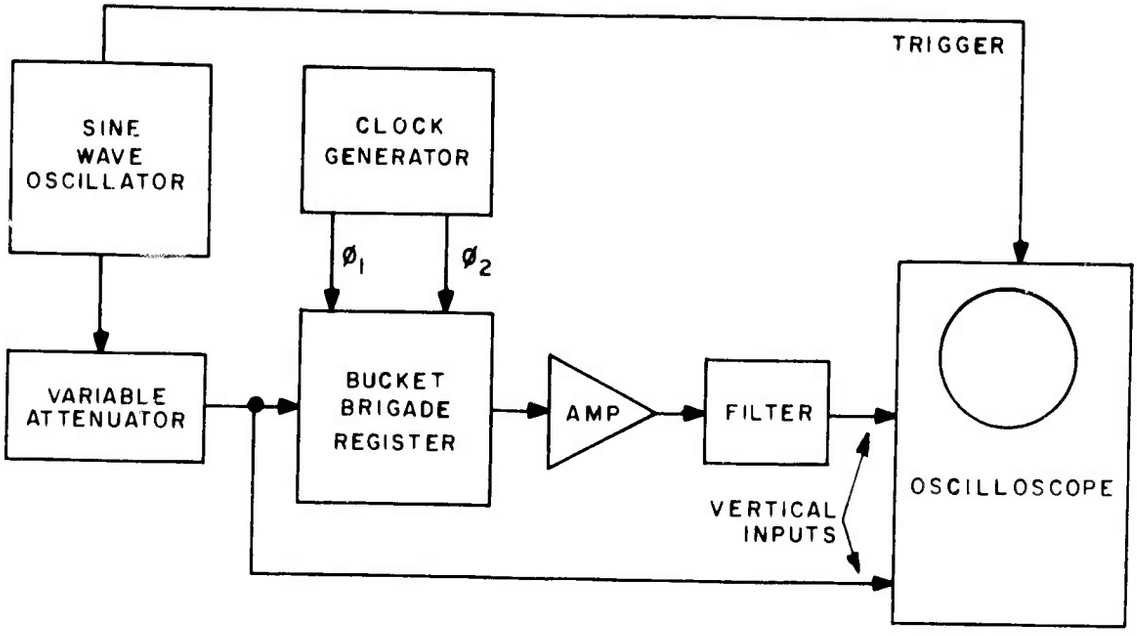


Fig. 4-15. Circuitry for low level bucket brigade array signal investigation.

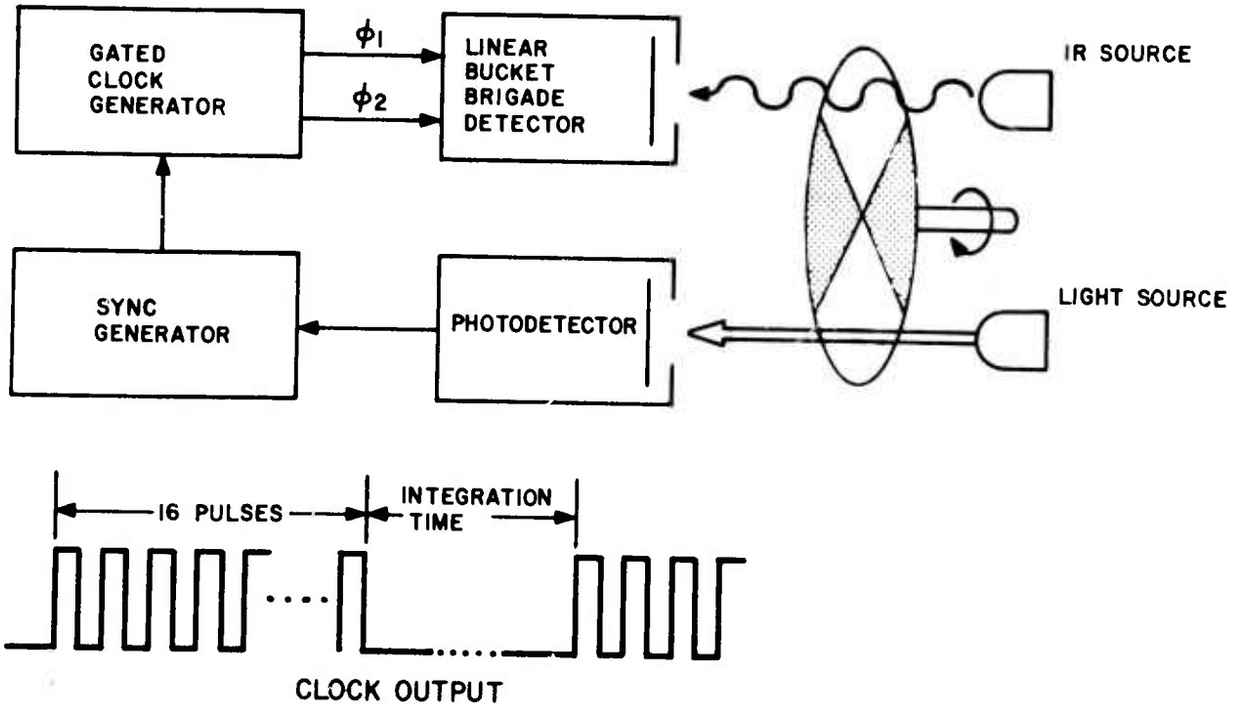


Fig. 4-16. Linear bucket brigade detector array test setup.

Section V

ANALYSIS OF PYROELECTRIC INTEGRATED CIRCUIT ARRAY PERFORMANCE

In this section an analytical assessment is made of the performance capabilities of large-scale infrared imaging systems containing two-dimensional pyroelectric detector arrays formed on integrated circuit substrates. The analysis assumes an X-Y addressed detector array configuration consisting of delineated and thermally isolated thin film TGS (triglycine sulfate) elements positioned over slots etched into the silicon substrate. Calculations are made of the imaging system's noise equivalent temperature difference, the voltage responsivity of the detector elements, the thermal conductance, and of the various noise processes present in the array. These are the Johnson noise, the temperature fluctuation noise, and the gate referred 1/f noise of the amplifying FETs (field effect transistors). Omitted from consideration are the effects of FET switching noise and the effects of any differences in the threshold voltages of the FET contained within each sensor cell. The calculations cover a range of detector sizes and operating frame rates.

The results of the calculations show that uncooled infrared imaging systems having a temperature resolution of nearly 0.4 °C should be possible at a frame rate of 10 Hz for arrays composed of 4-mil by 4-mil detectors on 8-mil centers. The use of larger detectors on correspondingly larger centers leads to further improvement in temperature resolution. For 10-mil by 10-mil detectors on 15-mil centers, for example, the calculations predict a noise equivalent temperature difference of 0.07 °C.

A. ARRANGEMENT OF PYROELECTRIC/INTEGRATED CIRCUIT ARRAY

The arrangement of a pyroelectric detector within the integrated circuit array of interest is illustrated in Fig. 5-1. The pyroelectric elements are formed on top of a thin thermally grown silicon dioxide layer which bridges slots etched into the integrated circuit substrate. In this manner, a high degree of thermal isolation is provided between the pyroelectric detectors and the unetched silicon regions which are in the form of long narrow beams. In the 16-by-16 TGS arrays under development, the silicon beams will be approximately 2 mils wide and 8 mils in height. The active area of each detector element is defined by the lower electrode, which is attached to the gate of the signal FET. The signal and reference FETs, along with the diffused signal lines, are formed in the silicon substrate prior to etching of the slots. The unetched silicon beams prevent thermal crosstalk between detectors in the column direction (see Fig. 5-1). Similarly, the metallized address lines which run over the surface of the SiO_2

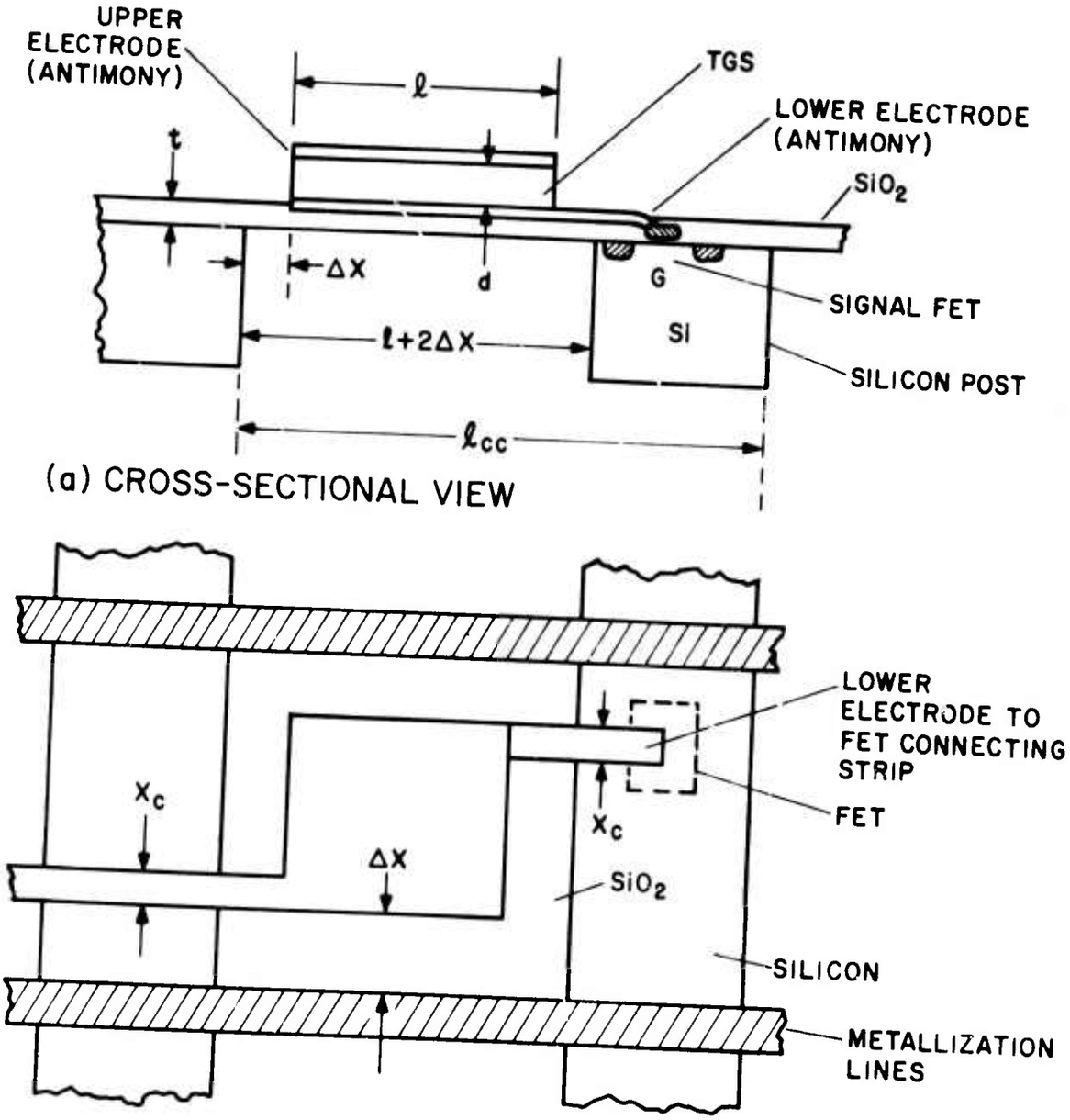


Fig. 5-1. Arrangement of a pyroelectric detector on a thermally isolated integrated circuit substrate.

membrane serve as a thermal shunt between detectors located on a common row; accordingly these lines eliminate thermal crosstalk in the row direction. The dimensions given in Fig. 5-1 are defined as follows:

t = thickness of the SiO_2 supporting membrane

d = thickness of the pyroelectric material

ℓ = length of a side of the (square) detector

ΔX = separation between the detector and the silicon beams and metallization lines

X_c = width of the upper and lower electrode connecting strips

ℓ_{cc} = detector center-to-center spacing

B. PARAMETERS USED IN THE ANALYSIS

Analysis of the pyroelectric/integrated circuit array requires the consideration of a number of factors which are not precisely known. These include the magnitudes of the pyroelectric and dielectric coefficients of polycrystalline TGS, the thermal conductance of the thin films used in the detector electrodes, the dielectric loss tangent of the pyroelectric material, and the noise characteristics of the FETs. It has therefore been necessary to estimate certain parameters in order to perform the analysis. Accordingly, the analysis is subject to improvement and upgrading; this will be performed as more reliable data become available.

The values of the detector and array properties used in this analysis are listed below:

Polycrystalline triglycine sulfate (TGS)

Pyroelectric coefficient, dP/dT	1.48×10^{-8} coulomb/cm^2 - °K
Dielectric coefficient, ϵ	2.45×10^{-12} farad/cm*
Specific heat, C_p	0.97 joule/gm - °K
Mass density, ρ_m	1.69 gm/cm^3

Other materials

Thermal conductivity (SiO_2), k_s[14]	1.18×10^{-2} W/cm - °K
Thermal conductivity (antimony electrodes), k_c[15]	0.2 W/cm - °K

*Averaged over the principal crystallographic directions

Figure 5-2 illustrates the detector FET preamplifier arrangement being considered. Each detector element of the array is assumed to be a square ℓ units of length on a side and d units of length thick. P_{IRS} represents the infrared signal power incident upon the detector. Other quantities shown in Fig. 5-2 are:

C_d = detector capacitance

R_d = detector resistance

$\tan \delta$ = loss tangent of polycrystalline TGS

C_a = FET preamplifier input capacitance

R_a = FET preamplifier input resistance

C. DETECTIVITY, NOISE EQUIVALENT TEMPERATURE DIFFERENCE AND VOLTAGE RESPONSIVITY

The specific detectivity of the detector/preamplifier may be written as

$$D^*_{\Delta\lambda,\,eff} = \frac{\bar{v}_s}{\bar{v}_N} \frac{\sqrt{A_d \Delta f}}{P_{IRS}} \qquad (5\text{-}1)$$

Since the voltage responsivity of the detector is $V_R = \bar{v}_s / P_{IRS}$,

$$D^*_{\Delta\lambda eff} = \frac{V_R}{\bar{v}_N} \sqrt{A_d \Delta f} \qquad (5\text{-}2)$$

which leads to

$$\frac{\bar{v}_s}{\bar{v}_N} = SNR = \frac{V_R}{\bar{v}_N} P_{IRS} \qquad (5\text{-}3)$$

In Eqs. (5-1) through (5-3),

$\bar{v}_s$ = rms signal voltage

$\bar{v}_N$ = total rms noise voltage referred to the detector

A_d = detector area

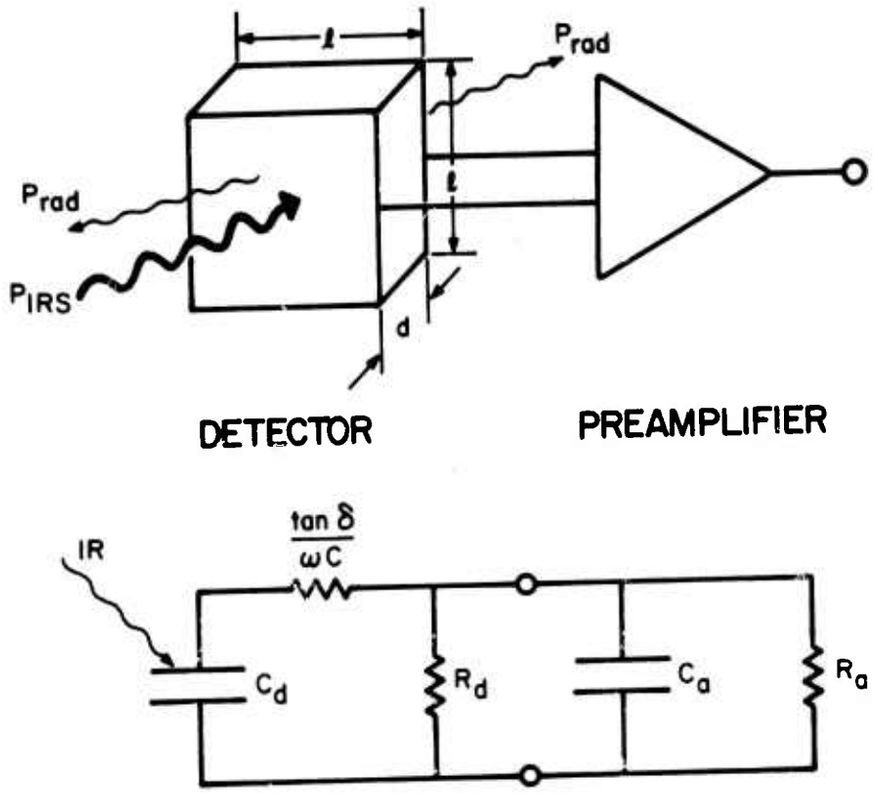


Fig. 5-2. A pyrolectric detector/preamplifier and its associated equivalent circuit.

Δf = detector noise bandwidth

SNR = signal to noise voltage ratio

$\Delta\lambda$ refers to the spectral interval of interest (8-μm to 14-μm)

For radiation over the 8- to 14-μm spectral interval,

$$P_{IRS} = (\Delta W_{\Delta\lambda})\, A_d \delta_{opt} / 4\, F_{NO}^2 \quad (W) \tag{5-4}$$

where for a background temperature of T = 300 °K,

$$\Delta W_{\Delta\lambda} = 0.38\, (4\eta\sigma T^3)\, \Delta T \quad (W/cm^2) \tag{5-5}$$

which gives

$$P_{IRS} = \frac{0.38\, \eta\, \sigma\, T^3 A_d \Delta T}{F_{NO}^2} \tag{5-6}$$

(The factor 0.38 arises because 38% of the power radiated by a 300° K blackbody is contained within the 8- to 14-μm spectral interval.)

In Eqs. (5-4) through (5-6),

$\Delta W_{\Delta\lambda}$ = radiant power, over the 8- to 14-μm spectral interval, per unit area incident upon the collector optics

σ_{opt} = optical transmission loss due to absorption and reflection by the collector optics

F_{NO} = system optical f/number

η = emissivity of the viewed object

σ = Stefan-Boltzmann constant (5.67×10^{-12} W/cm^2 - $^oK^4$)

Substituting Eq. (5-6) into Eq. (5-3), and noting that when SNR = 1, $\Delta T = NE\,\Delta T$, the noise equivalent temperature difference, leads to

$$NE\,\Delta T = \frac{\bar{v}_N}{V_R} \quad \frac{F_{NO}^2}{0.38\,\eta\sigma\,\delta_{opt}} T^3 A_d \quad (°C) \tag{5-7}$$

The voltage responsivity of a pyroelectric detector is given by [1]

$$V_R = \frac{\eta_d \left[\omega \frac{dP}{dT} \quad \frac{RA_d}{G}\right]}{(1 + \omega^2 \tau_E^2)^{1/2} \quad (1 + \omega^2 \tau_T^2)^{1/2}} \quad (V/W) \tag{5-8}$$

where

η_d = emissivity of the detector surface

ω = angular frame rate

τ_E = electrical time constant

τ_T = thermal time constant

G = total thermal conductance

R = parallel combination of the detector and preamplifier resistances

The electrical time constant is

$$\tau_E = \frac{R_d R_a}{R_d R_a} (C_a + C_d) \quad \text{(seconds)} \tag{5-9}$$

and the thermal time constant is given by

$$\tau_T = \frac{H}{G} \quad \text{(seconds)} \tag{5-10}$$

where H, the heat capacity of the detector is

$$H = m C_p = A_d d \rho_m C_p \quad (J/^\circ K)$$

and m is the mass of the pyroelectric detector material.

D. THERMAL CONDUCTANCE AS A FUNCTION OF DETECTOR SIZE AND CENTER-TO-CENTER SPACING

The total thermal conductance is given by

$$G = G_C + G_R + G_K, \quad (W/^oK) \tag{5-11}$$

G_C is the thermal conductance associated with the transport of heat along the SiO_2 detector supporting membrane and through the two electrode connecting strips shown in Fig. 5-1, G_R is the radiative conductance, and G_K is the convective conductance. Assuming both sides of the detector radiate equally,

$$G_R = 8 \eta_d \sigma T^3 A_d \tag{5-12}$$

G_K may be expressed as

$$G_K = h A_d$$

where the convection coefficient h is 2.81×10^{-4} W/cm^2 - ^oK for still air at a temperature of 300^oK and at a pressure of one atmosphere.

G_C, which is by far the largest of the three thermal conductance terms, is given by

$$G_C = \frac{k_s A_c}{\Delta X} + \frac{2k_c A_t}{\Delta X} \tag{5-13}$$

where the previously undefined quantities are:

A_c = cross-sectional area for heat transport through the SiO_2 detector supporting membrane

A_t = cross-sectional area for heat transport through the electrode connecting strips

A_t is determined by the thickness of the antimony electrode films and the width of the connecting strips, taken to be fixed at 500 Å and 0.3 mils respectively. Thus in all of the calculations to be performed, A_t has a constant value of 3.81×10^{-9} cm^2. A_c however will vary with detector size, thickness of the SiO_2 membrane, and the spacing between the detector and the silicon sections and metallization lines. It is given to a very close approximation by

$$A_c = 4t \left[\ell + \left(\frac{\ell^2}{4} + \frac{\Delta X \, (\ell + \Delta X)}{2} \right)^{1/2} - \frac{\ell}{2} \right] (cm^2) \qquad (5\text{-}14)$$

We wish to determine G for various detector sizes, i.e. various values of ℓ, as a function of ℓ_{cc}, the detector center-to-center spacing, for a representative frame rate of 10 frames/second and for a detector thickness of 10 μm and SiO_2 membrane thickness of 12,000 Å. It will be assumed that the silicon sections and the metallization lines to which the detector heat is conducted are heat sunk at 300°K. The results of the calculations for detectors ranging in size from 1 mil on a side to 10 mils on a side and for center-to-center spacings ranging from 3 to 17 mils are shown in Fig. 5-3. The large increase in G_C that occurs as ℓ_{cc} approaches the value ℓ + 2 mils is due to the decrease in ΔX which this condition reflects.

Values of G_R and G_K for the same conditions applicable to Fig. 5-3 (and assuming a detector emissivity η_d of 0.8) are listed in Table 5-1. Comparison of Fig. 5-3 with the values of G_R and G_K of Table 5-1 shows G_C to be between 2 and 4 orders of magnitude greater than either G_R or G_K.

E. DETECTOR AND PREAMPLIFIER NOISE

The total noise voltage referred to the pyroelectric detector is

$$\bar{v}_N = \left[\bar{v}_{nJ}^2 + \bar{v}_{ng}^2 + \bar{v}_{nT}^2 \right]^{1/2} \qquad (5\text{-}15)$$

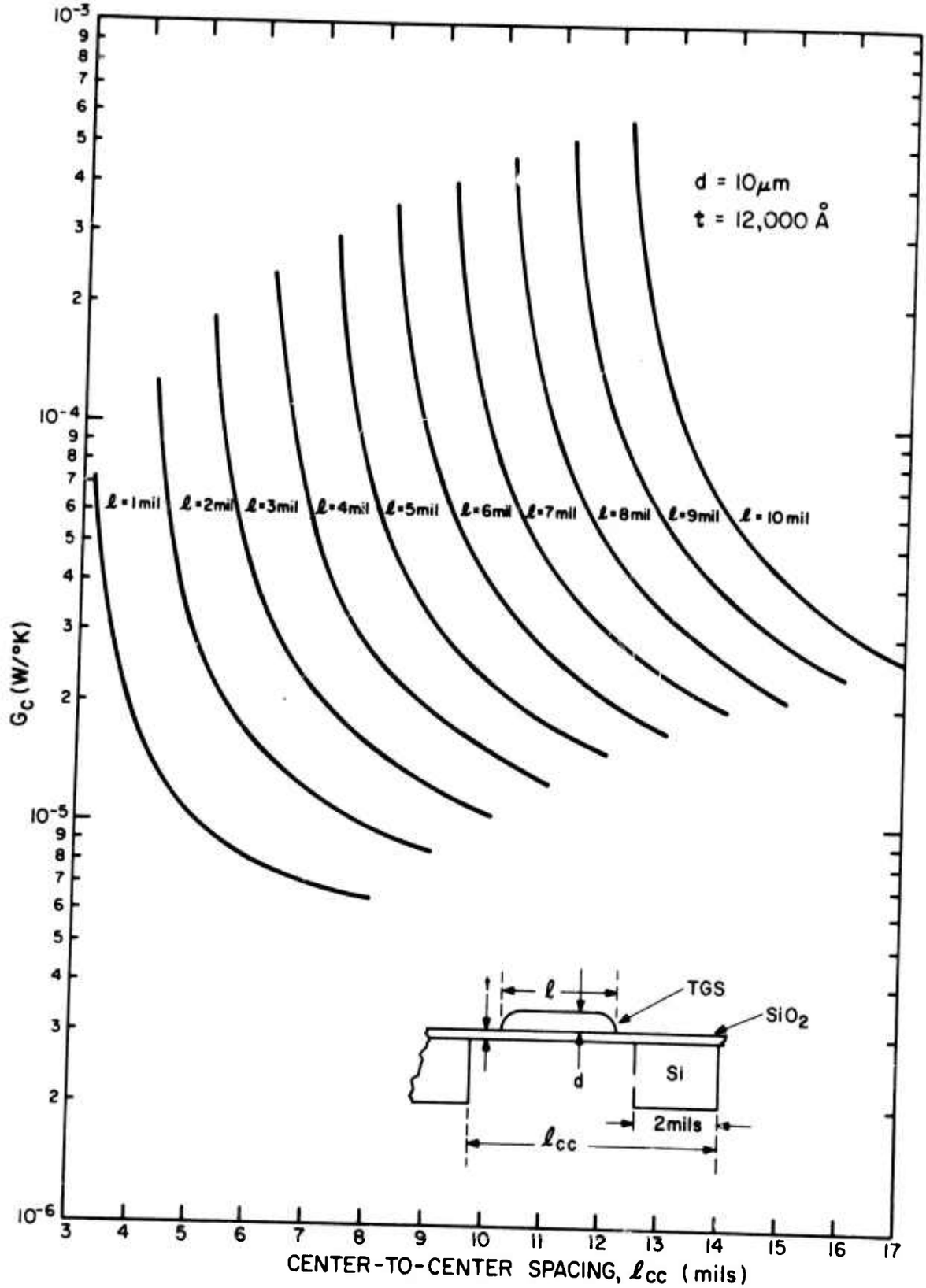


Fig. 5-3. Thermal conductance due to heat transport within SiO_2 membrane and detector connecting strips as a function of detector center-to-center spacing.

TABLE 5-1. RADIATIVE AND CONVECTIVE CONDUCTANCE FOR VARIOUS DETECTOR SIZES

Detector Size (mils)	Radiative Conductance G_R (W/°K)	Convective Conductance G_K (W/°K)
1	6.32×10^{-9}	1.81×10^{-9}
2	2.53×10^{-8}	7.24×10^{-9}
3	5.69×10^{-8}	1.63×10^{-8}
4	1.01×10^{-7}	2.90×10^{-8}
5	1.58×10^{-7}	4.53×10^{-8}
6	2.28×10^{-7}	6.52×10^{-8}
7	3.10×10^{-7}	8.32×10^{-8}
8	4.05×10^{-7}	1.16×10^{-7}
9	5.12×10^{-7}	1.47×10^{-7}
10	6.32×10^{-7}	1.81×10^{-7}
T = 300°K η = 0.8		

where $\bar{v}_{n_J}$ is the Johnson noise, $\bar{v}_{ng}$ is the gate referred 1/f noise of the FET, and $\bar{v}_{nT}$ is the temperature fluctuation noise voltage. The temperature fluctuation noise, which arises from either radiative exchange with the background or conductive exchange with the substrate, is the limiting noise process in all thermal detectors. A thermal detector in which the temperature noise is due solely to radiative exchange with the background is said to be at its theoretical limit. The rms temperature fluctuation ($\overline{\Delta T}$) is derived from:[16]

$$\Delta T^2 = \frac{2KT^2}{\pi G} \int_{\omega_\ell}^{\omega_u} \frac{d\omega}{1 + \tau_T \omega^2}$$

$$= \frac{2KT^2}{\pi G} \frac{1}{\tau_T} \tan^{-1} \omega \tau_T \Big|_{\omega_\ell}^{\omega_u} \qquad (5\text{-}16)$$

Taking the lower and upper angular frequency limits to be $\omega_\ell = 0$ and $\omega_u = \infty$, respectively, yields

$$\overline{\Delta T} = \left[\frac{KT^2}{H}\right]^{1/2} \qquad (^{o}K \text{ rms}) \qquad (5\text{-}17)$$

The noise voltage associated with the temperature fluctuation is

$$\bar{v}_{nT} = \frac{V_R G}{\eta} \overline{\Delta T} \qquad (V \text{ rms}) \qquad (5\text{-}18)$$

The gate referred 1/f noise of the input FET is dependent upon the length and width of the channel, the gate oxide capacitance, and the density of trapping states.[11] To a first approximation it is given (for a 32- by 32-element array) by

$$\bar{v}_{ng} = \left[\frac{4.16Q}{2\pi aL}\right]^{1/2} \qquad (V \text{ rms}) \qquad (5\text{-}19)$$

where a is the channel width, L is the channel length and Q is a term that includes (among other parameters) the density of trapping states, the number of charge carriers flowing through the channel, and the oxide capacitance. For PMOS (p-channel metal-oxide-semiconductor) FETs of the type planned for use in the pyroelectric/ integrated circuit arrays, Q is calculated to be 6.15×10^{-10} V^2 - mil^2.

The Johnson noise is given by

$$\bar{v}_{nJ}^2 = \frac{4KT}{2\pi} \int_{\omega_\ell}^{\omega_u} \mathrm{Re}(Z)\, d\omega \qquad (5\text{-}20)$$

where K is Boltzmann's constant (1.38×10^{-23} J/°K) and Re (Z) is the real part of the detector/amplifier impedance. From the equivalent circuit of the deteetor/pre-amplifier combination, and assuming tan δ to be frequeney independent,

$$\mathrm{Re}(Z) = \frac{R\left[R\frac{\tan\delta}{\omega C} + \frac{\tan\delta^2}{\omega^2 C^2} + \frac{1}{\omega^2 C^2}\right]}{R^2 + 2R\frac{\tan\delta}{\omega C} + \frac{\tan^2\delta}{\omega^2 C^2} + \frac{1}{\omega^2 C^2}} \tag{5-21}$$

For $\tan\delta^2 << 1$, and $\tan\delta << \frac{1}{\omega\tau_E}$, Re (Z) becomes

$$\mathrm{Re}(Z) = \frac{R}{1 + \omega^2 C^2 R^2} \tag{5-22}$$

Taking the lower limit to be $\omega_\ell = 0$, the upper limit to be $\omega_u = \infty$, and performing the integration leads to

$$\bar{v}^2_{nJ} = \frac{4KT}{2\pi C} \tan^{-1} \omega RC \Bigg|_0^\infty \tag{5-23}$$

which yields

$$\bar{v}_{nJ} = \left[\frac{KT}{C_d + C_a}\right]^{1/2} \tag{5-24}$$

The total noise $\bar{v}_N$, the Johnson noise, the temperature fluctuation noise voltage, and the gate referred 1/f noise are listed in Table 5-2 for TGS detectors ranging in size from 1 mil by 1 mil to 10 mils by 10 mils. The detectors are assumed to be 10-μm thick and the SiO_2 membrane is taken to be 12,000 Å thick. The values of the temperature fluctuation noise shown in Table 5-2 were calculated for $\Delta X = 1$ mil for each detector, which represents a worst case (as will be evident later) since for minimum NEΔT, ΔX will always be larger than 1 mil. For detectors up to 7 mils in size, the FET area was optimized to yield the minimum $\bar{v}_{ng}$. The FET area was not optimized for detectors larger than 7 mils because it becomes impraetically large. The values of the detector resistance, detector eapacitance, FET area, FET capacitance, and electrical time constant that apply to the ealculated noise voltages of Table 5-2 are listed in Table 5-3.

TABLE 5-2. NOISE VOLTAGE IN A TGS DETECTOR ARRAY FOR VARIOUS DETECTOR SIZES

Detector Size (mils)	Total Noise Voltage v_n (microvolts)	Johnson Noise Voltage v_{nJ} (microvolts)	Temperature* Fluctuation Noise v_{nT} (microvolts)	Gate Referred 1/f Noise v_{ng} (microvolts)
1	298	286	19.3	82.3
2	214	201	19.2	71.3
3	149	141	14.0	48.2
4	115	109	11.1	37.0
5	93.5	88	9.13	30.4
6	78.4	73.9	7.72	25.0
7	67.7	63.9	6.73	21.6
8	61.7	57.5	6.23	21.6
9	56.8	52.2	5.76	21.6
10	52.6	47.7	5.34	21.6

For

$d = 10\,\mu m$
$t = 12,000$ Å
$\Delta X = 1$ mil
$F_R = 10$/second

*Maximum values of V_{nT}

TABLE 5-3. RESISTANCE AND CAPACITANCE OF 10-μm THICK TGS DETECTORS, ASSOCIATED FET PROPERTIES, AND ELECTRICAL TIME CONSTANTS

Detector Size, ℓ (mils)	Detector* Resistance R_d, (ohms)	Detector** Capacitance C_d, (pico F)	FET Area A_a, (mil^2)	FET*** Capacitance C_a, (pico F)	Electrical Time Constant τ_E, (seconds)
1	1.55×10^{14}	0.024	0.060	0.035	6.82
2	3.88×10^{13}	0.096	0.080	0.039	3.81
3	1.73×10^{13}	0.261	0.175	0.067	3.54
4	9.69×10^{12}	0.386	0.297	0.099	3.38
5	6.20×10^{12}	0.600	0.440	0.140	3.30
6	4.31×10^{12}	0.876	0.650	0.190	3.25
7	3.16×10^{12}	1.18	0.870	0.241	3.20
8	2.42×10^{12}	1.54	0.870	0.241	3.03
9	1.92×10^{12}	1.95	0.870	0.241	2.91
10	1.55×10^{12}	2.41	0.870	0.241	2.82

*$\rho_d = 10^{12}$ ohm-cm
**Relative dielectric coeff. = 28.7
***gate oxide thickness = 1,000 Å
FET Resistance = 10^{16} ohms

F. THERMAL TIME CONSTANT

The only quantity in the expression for the voltage responsivity remaining to be discussed is the thermal time constant,

$$\tau_T = \frac{H}{G_C + G_R + G_K}$$

Plots of τ_T for the conditions previously referred to are shown in Fig. 5-4. As would be expected, τ_T increases with increasing detector size, and for any particular detector it increases with separation from the silicon section and metallization lines. It should be noted that for an "ideal detector", i.e., a detector for which G_C and G_K are zero and $G_R = 8\,\eta_d\,\sigma\,T^3\,A_d$, τ_T would be on the order of 1 second (assuming d = 10 μm, t = 12,000 Å and $\eta_d = 1.0$).

G. VARIATION OF V_R AND NEΔT WITH DETECTOR SIZE AND CENTER-TO-CENTER SPACING

The variation in voltage responsivity with detector center-to-center spacing, as calculated from Eq. (5-8), is shown in Fig. 5-5 for a frame rate of 10 frames/second. It is seen that V_R generally decreases with increasing detector size; for any particular detector, it is seen to increase with separation from the silicon section and metallization lines.

The various terms contained in the expression for the NEΔT of a pyroelectric/integrated circuit array have been discussed. It is now of interest to calculate NEΔT as a function of detector center-to-center spacing for a number of detector sizes. Referring to Eq. (5-7), we will consider a thermal imaging system for which

$$F_{NO} = 1.0$$

$$\eta = 0.8$$

$$\delta_{opt} = 0.5$$

The system frame rate and the emissivity of the detector elements will be taken to be F_R = 10/second and $\eta_d = 0.8$, respectively, and the width of the silicon section is again taken to be 2.0 mils. The results of the calculations are shown in Fig. 5-6. The general character of the curves shows that, as expected because of decreased noise voltage, the temperature resolution improves with increasing detector size. The large increase in NEΔT that occurs as the detector size approaches the value $\ell + 2\Delta X + 2$ mils is due to the accompanying large increase in G_C, which in turn results in reduced voltage responsivity. The relatively poor NEΔT of the small 2- and 3-mil detectors is attributed to the larger Johnson noise associated with small detectors.

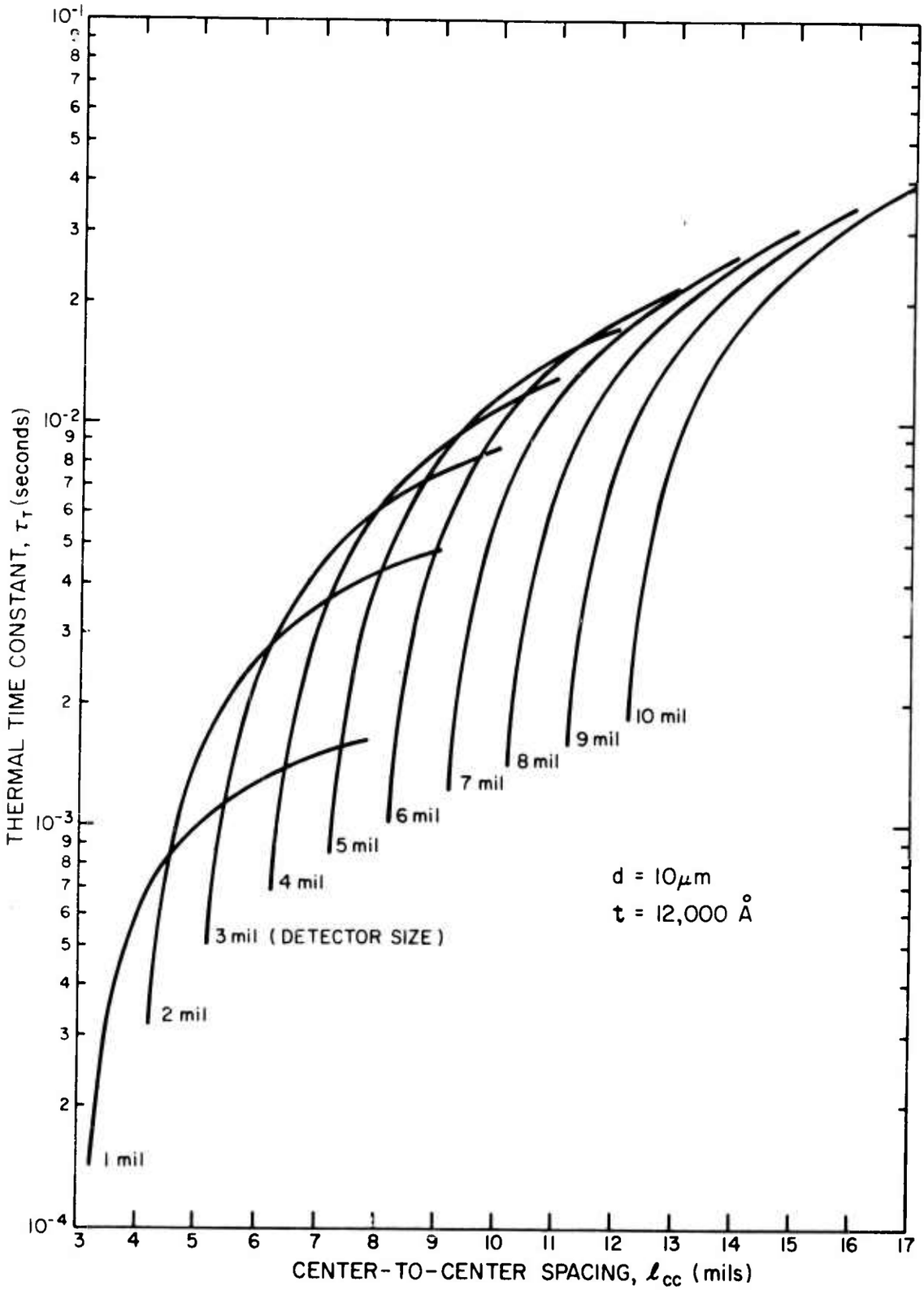


Fig. 5-4. Detector thermal time constant as a function of detector center-to-center spacing.

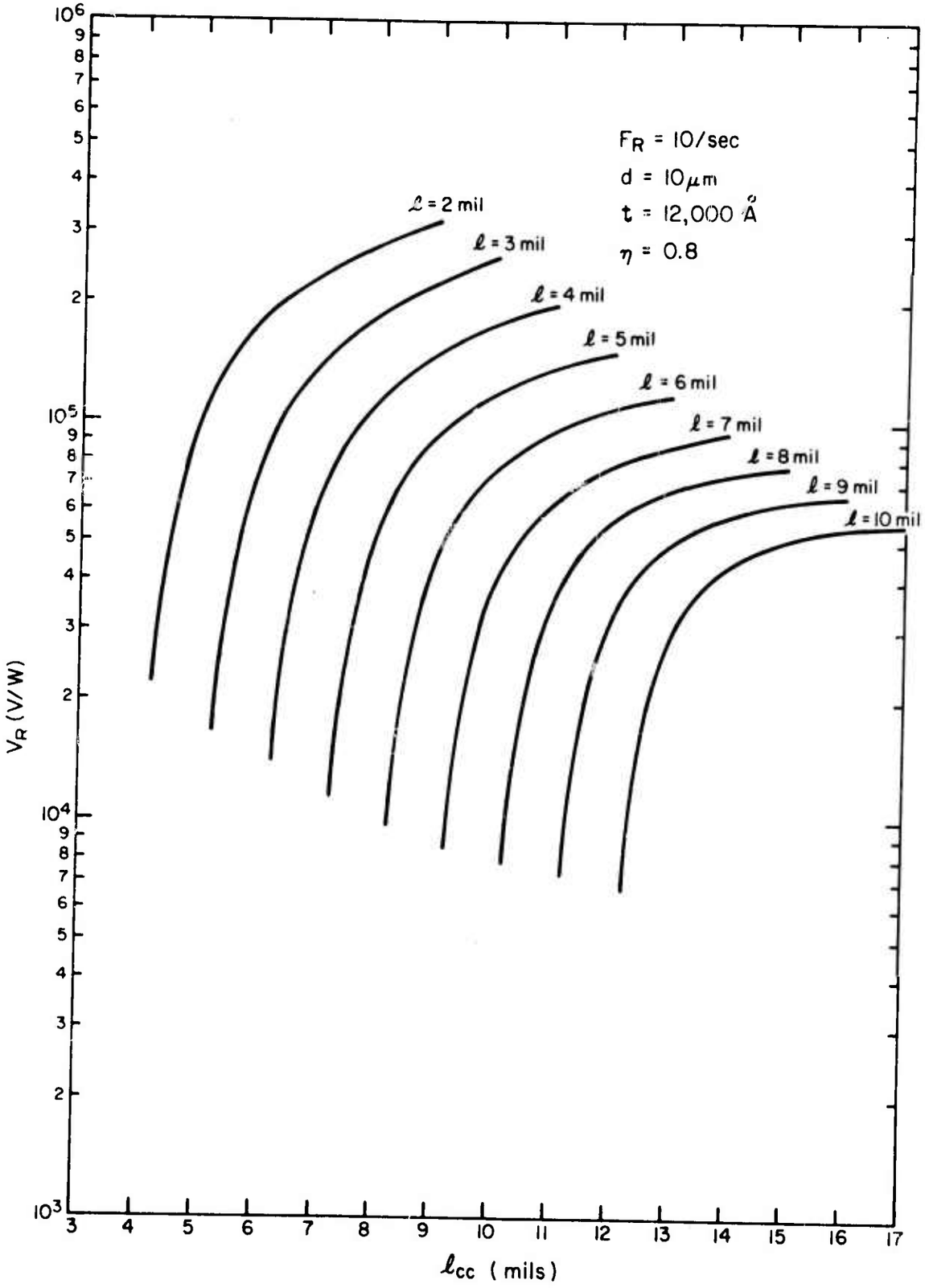


Fig. 5-5. Voltage responsivity as a function of center-to-center spacing.

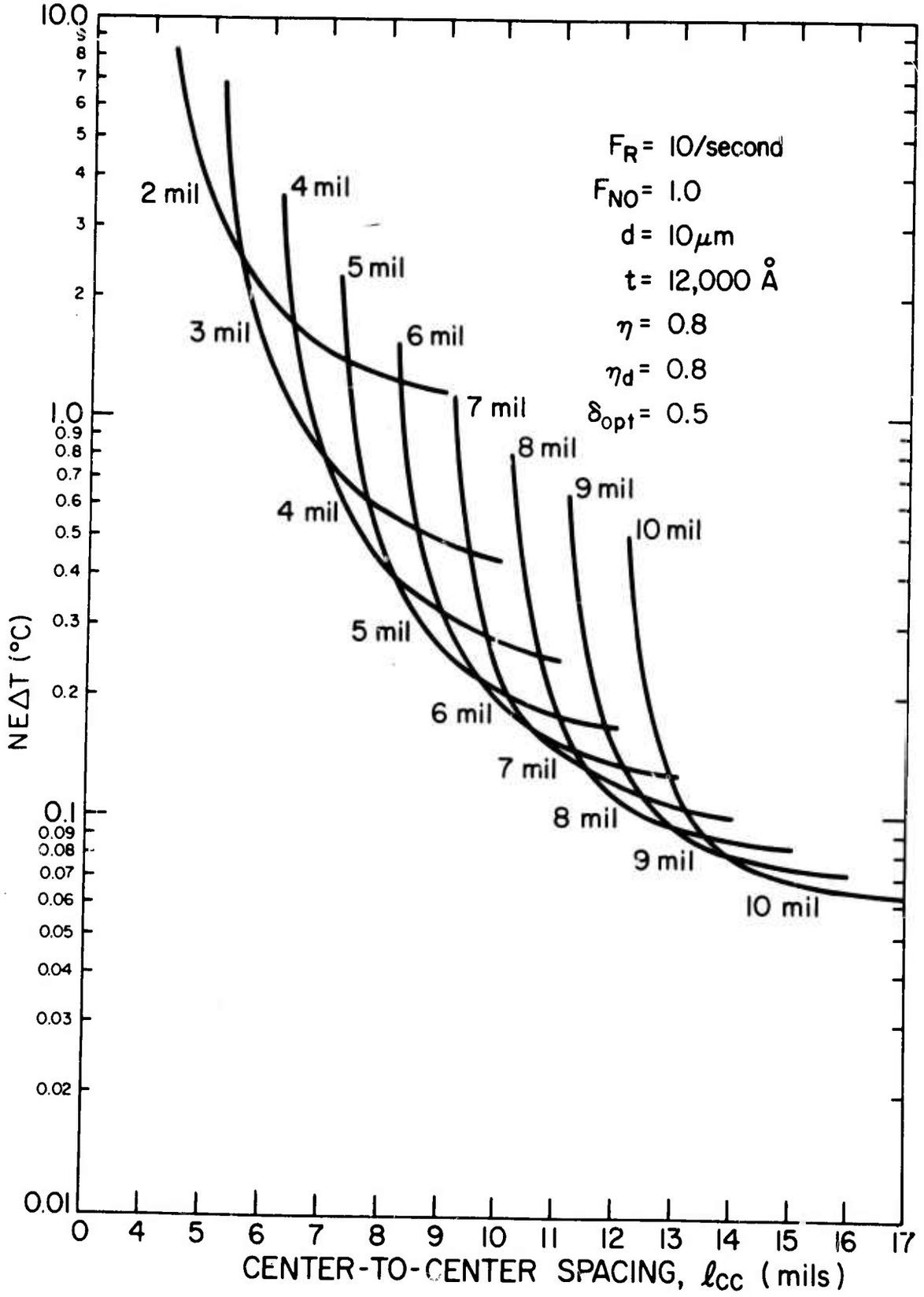


Fig. 5-6. Noise equivalent temperature difference as a function of center-to-center spacing.

The detector size and center-to-center spacing of interest to the present program are $\ell = 4$ mils and $\ell_{cc} = 8$ mils. The data of Fig. 5-6 show that for a thermal imaging system composed of an array of such detectors, NEΔT is predicted to be 0.42°C.

From Fig. 5-6, it is noted that the minimum NEΔT for a particular center-to-center spacing is given by the lower bounding envelope of the family of curves. Figure 5-7 shows such curves for two frame rates, $F_R = 10$/second and $F_R = 20$/second, with the remaining parameters being identical to those of Fig. 5-6. The numbers along the two curves denote the optimum detector sizes (in mils) corresponding to the particular center-to-center spacings on which they are located. It is noted that for the detector geometry of interest in the developmental array (4-mil detectors on 8-mil centers), the increase in NEΔT that occurs in going to 20 frames/second is relatively small (0.42°C at 10 frames/second vs. 0.48 at 20 frames/second). It is also noted that there is virtually no change in NEΔT for 2-mil detectors, which indicates that system degradation is appreciable even at 10 frames/second. In contrast, relatively large degradation in NEΔT occurs in the larger detectors. For example, for the 10-mil detector on 17-mil centers, NEΔT at $F_R = 10$/second is 0.06°C, whereas at $F_R = 20$/second it increases to 0.12°C.

Figure 5-8, which is similar to Fig. 5-7, shows the variation in the minimum NEΔT with center-to-center spacing at frame rates of 15/second and 30/second.

H. VARIATION OF NEΔT WITH DETECTOR AND SiO_2 MEMBRANE THICKNESSES

The manner in which NEΔT varies with the thickness of the SiO_2 detector supporting membrane is shown in Fig. 5-9 for 4-mil by 4-mil detectors of the type to be used in the X-Y addressed and bucket brigade arrays. At the 8-mil center-to-center spacing planned for the pyroelectric arrays, the NEΔTs for t = 10,000, 12,000, 18,000 and 24,000 Angstroms are 0.36, 0.42, 0.49 and 0.64°C respectively, showing that NEΔT is a relatively sensitive function of the SiO_2 thickness.

The dependence of NEΔT of a detector array composed of larger TGS detectors upon SiO_2 membrane thickness is shown in Fig. 5-10 for 10-mil by 10-mil detectors. The degradation in NEΔT is seen to be relatively small at large values of ℓ_{cc}.

The variation in NEΔT with detector thickness is shown in Fig. 5-11 for a 4-mil by 4-mil detector and for center-to-center spacings of 7, 8 and 9 mils. It is seen that for the planned spacing of 8 mils, NEΔT is relatively insensitive to detector thickness over the broad range of d = 10 μm to d = 15 μm. The improved temperature resolution attainable by increasing the center-to-center spacing to 9 mils is evident in Fig. 5-11. This improvement, of course, can only be obtained at the expense of an accompanying reduction in spatial resolution.

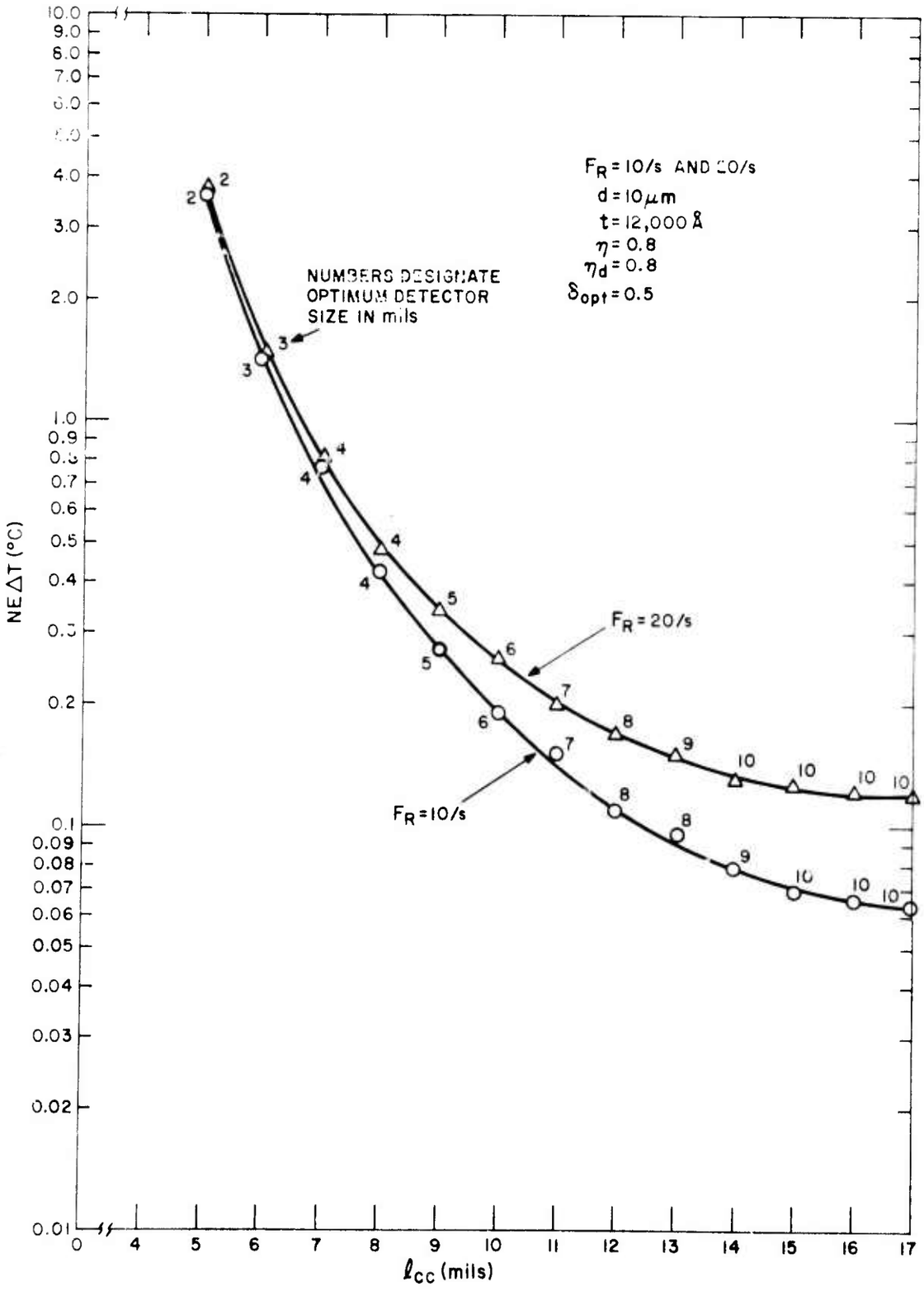


Fig. 5-7. Minimum NEΔT (noise equivalent temperature difference) as a function of center-to-center spacing (frame rates 10/second and 20/second).

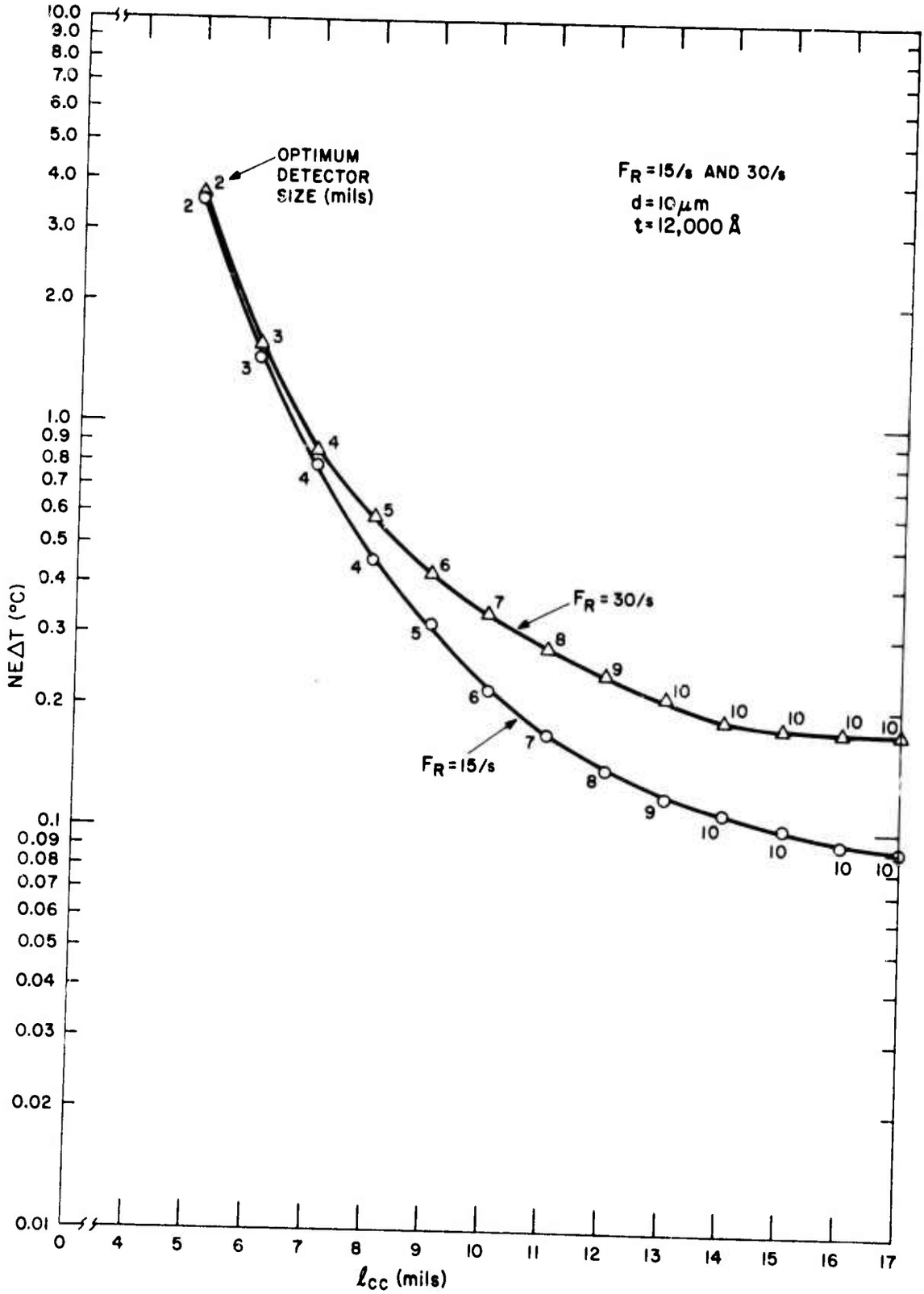


Fig. 5-8. Minimum NEΔT as a function of center-to-center spacing (frame rates 15/second and 30/second).

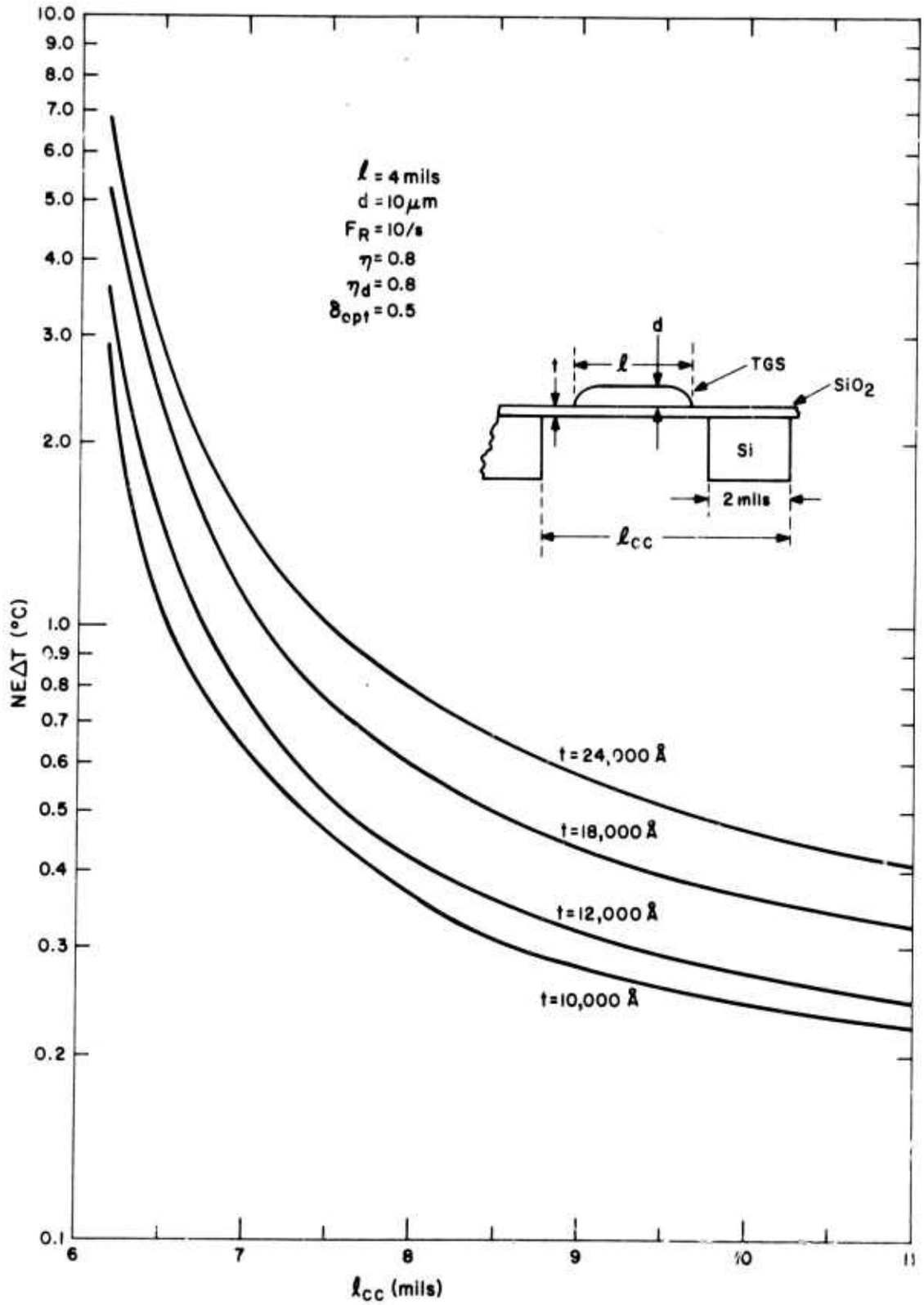


Fig. 5-9. NEΔT of 4-mil detectors as a function of center-to-center spacing for several SiO_2 membrane thicknesses.

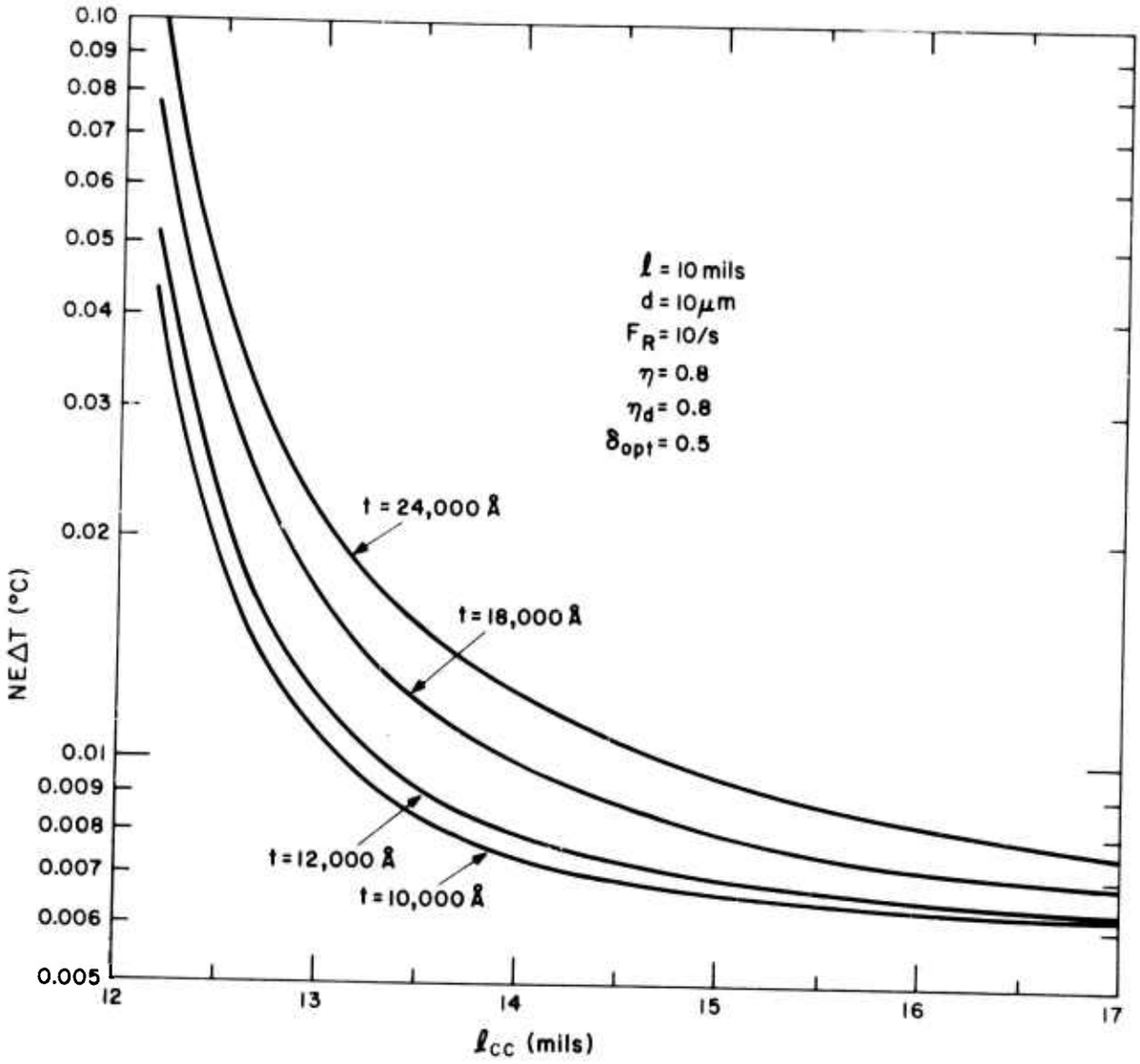


Fig. 5-10. NEΔT of 10-mil detectors as a function of center-to-center spacing for several SiO_2 membrane thicknesses.

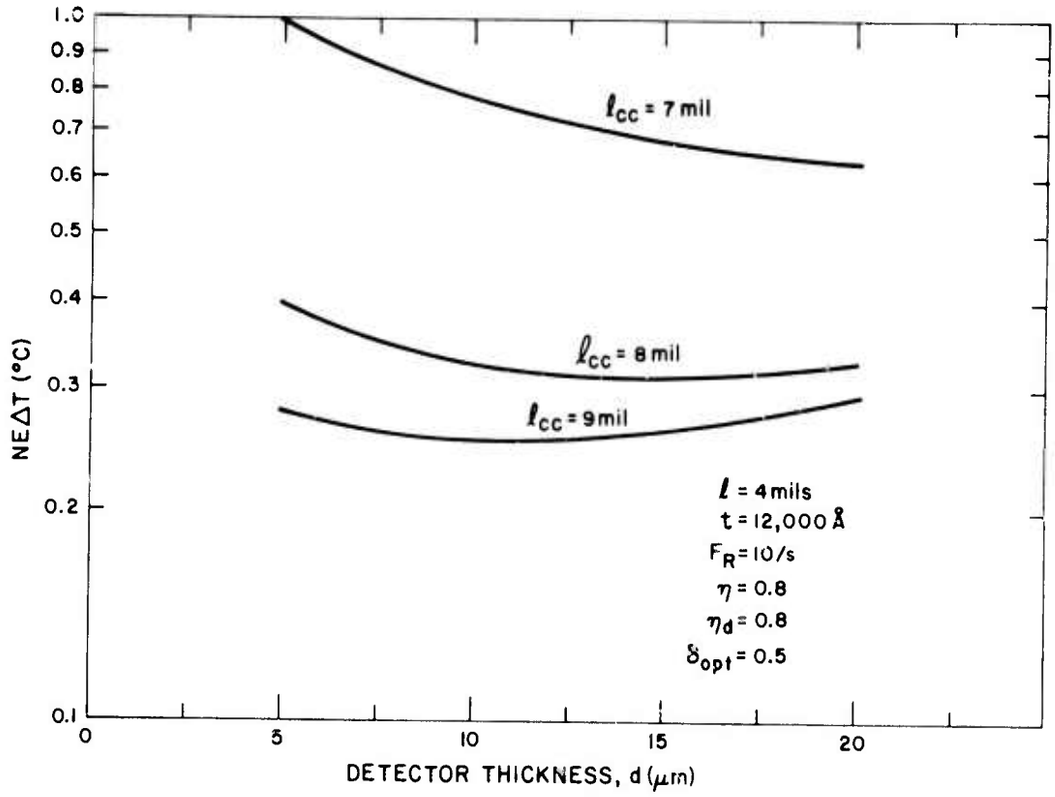


Fig. 5-11. Variation of NEΔT with detector thickness for several center-to-center spacings.

Section VI

CONCLUSIONS

A. MATERIALS DEVELOPMENT

The process for making thin polycrystalline TGS films in the range of 10- to 15-μm thick has basically been formulated. Higher purity TGS is desirable and some additional development effort in this direction will be expended. Modifications in the milling operation and additional milling with the jet mill are planned. To date, ball milling of TGS particles suspended in isopropyl alcohol in a polyethelyene jar with glass balls has been found to be the most satisfactory technique for obtaining the submicrometer size particles required for uniform TGS layers. The most effective way found to inhibit the solubility of TGS in the suspending isopropyl alcohol, and to thereby avoid the presence of the sulfate radical in the suspension, is by presaturating the alcohol with glycine. Although thermal densification leads to TGS films of greatly reduced surface roughness and high mass density, the resulting detectors have voltage responsivities of about one-third of those prepared by the water vapor densification technique. Because of the reduced voltage responsivity and the critical nature of thermal densification, it will not be pursued further.

The laser evaporation technique, while leading to TGS films having smooth surfaces, has not as yet been shown to be a viable approach since the films have not exhibited a pyroelectric effect. Modification of the laser evaporation system to permit the use of a CO_2 laser is in progress. Since the highly-absorbing CO_2 laser radiation will eliminate the need for absorbing dyes in the target TGS, the resulting films may be pyroelectric.

B. ARRAY TECHNOLOGY DEVELOPMENT

The approach to thermal isolation by etching slots in the silicon is progressing satisfactorily, but it remains a low yield process. A series of slots 10 mils wide on 14 mil centers and 0.38 inch long have been preferentially etched through 8-mil thick silicon wafers, leaving the thermally grown silicon dioxide layer intact in several sections of the wafer. Silicon dioxide layers 20,000-Å thick were found to be quite rugged but 12,000-Å thick layers were susceptible to cracking. Further refinements in the etching technique will be needed to improve the yield. Specifically, masking materials capable of better withstanding the hours of etching required to etch through 8 mil thick wafers are needed. Experiments using boron doped silicon dioxide as the masking material are planned.

Delineation of the polycrystalline TGS films remains a problem. Recently progress has been made by saturating the TGS films with dilute Kodak Thin Film Photoresist and drying in vacuum. The developed films are fairly well defined, but some undercutting of the TGS still occurs. The use of Shipley photoresist is planned and a different approach involving stripping of a photoresist pattern underlying a continuous TGS film will be tried.

Continuity of the upper electrode metallization over thin polycrystalline TGS films has been realized by using a rocking substrate holder during vacuum deposition of the upper electrode metallization. Films made in this manner have electrical sheet resistivities corresponding to films formed on smooth glass substrates.

Poling of detectors in the X-Y addressed array by application of an external electric field has yielded inconclusive results. The problem arises because of the high resistance of the FET gate. One array appeared to be poled spontaneously but in no instance has saturation polarization been achieved. Poling by application of voltage pulses is being attempted but, to date, no satisfactory technique for poling the detectors on the X-Y addressed array has been achieved. Poling of the detectors in the bucket brigade array is not as difficult because the FET drain-to-source resistance is much lower than that of the gate oxide. The discrete linear TGS bucket brigade array was successfully poled by application of a dc voltage.

1. Single Crystal TGS Array

A complete assembly using a small wafer of 1-mil thick permanently poled TGS (grown from L-alanine solution) was made and tested. A peak-to-peak output of 30 mV was measured using an FET amplifier having an input capacitance of 4 pF. For the same conditions, a low capacitance amplifier should yield an output of 50 mV as compared with the theoretical value of 390 mV for an ideal detector.

The microfinger springs used to contact the detectors on the single crystal array proved remarkably elastic and no permanent deformation was noted. Further improvements in the process for making the microfingers are in progress.

The fabrication and testing of a 16-by-16 X-Y addressed array using permanently poled TGS is planned during the next reporting period using the existing 16-by-16 array. Attempts will then be made to address the array and to form a thermal image.

2. Detector Array Arrangements

Much of the addressing and signal processing circuitry required for the X-Y addressed array has been assembled and tested. Cell-to-cell variations in the

threshold voltages of the FETs are expeeted to limit the sensitivity of X-Y addressed arrays, and frame storage and subtraction will be needed for improved sensitivity. Switching transients are not expeeted to be a serious problem.

The bucket brigade array appears to offer an important advantage over the polycrystalline X-Y addressed array. Poling of the detectors, which remains to be conclusively demonstrated for a polycrystalline X-Y addressed array, is readily accomplished in a bucket brigade array. The bucket brigade arrangement is also less sensitive to variations in FET characteristics. Further, it does not suffer from thermal memory because the reading out of charge automatically resets the detector potentials to a fixed value. Finally the possibility exits for performing frame storage and subtraction within the bucket brigade array itself, provided the change transfer efficiency is sufficiently high.

A noise model for the bucket brigade array has not as yet been formulated. As a result, estimates of the temperature resolution capabilities of pyroelectric bucket brigade thermal imaging arrays have not been made. The question of the magnitude of dark current variations in bucket brigade arrays also remains to be examined.

C. ARRAY FABRICATION STATUS

Two linear TGS arrays, each containing 16 TGS detector elements, have been designed and are now in the process of being fabricated. One is an X-Y addressed array and the other is a bucket brigade array. The purpose of these arrays is to permit a direct comparison of the X-Y addressed versus the bucket brigade mode of operation.

A 16-by-16 X-Y addressed array and its bucket brigade counterpart have been designed. Masks for these arrays are currently being fabricated. Since the bucket brigade array appears to offer greater potential, it will be fabricated before the X-Y addressed array.

D. ANALYSIS OF PYROELECTRIC ARRAY PERFORMANCE

The results of the analysis of polycrystalline X-Y addressed TGS arrays indicate that such arrays should be capable of moderately high temperature resolution for targets viewed against a 300° K background. The calculations, for example, predict a noise equivalent temperature difference 0.42° C at a frame rate of 10/second and of 0.48° C and 0.58° C at frame rates of 20/second and 30/second, respectively, for 4-mil detectors on 8-mil centers. Detector Johnson noise and loss of detector

heat by conduction to the substrate are the principal factors limiting the temperature resolution capabilities of the arrays. All other factors being equal, improved temperature resolution is obtainable by increasing detector size and center-to-center spacing, but this is accompanied by a decrease in spatial resolution.

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APPENDIX A

PERIODIC HEAT FLUX ACTING UPON A THIN, SEMI-INFINITE SLAB

The problem of a line source with a periodic flux input is considered by Carslaw and Jaeger.* The specific form taken is of a bar heated at one end and radiating from the sides. They show that if the radiation loss from the bar is included in the heat conduction equation in the form

$$\frac{\partial T}{\partial t} = D \frac{\partial^2 T}{\partial x^2} - aT$$

a transformation of the type

$$T = ue^{-at}$$

converts the equation to a normal heat diffusion equation. The boundary condition of interest is of alternating heat flux in and out for periods τ so that

$$\frac{\partial T}{\partial x} = g(t) \quad (x = 0)$$

where g(t) is a square wave. The solution of the above equations for a periodic flux impressed from time 0 to t is

$$T = (D/\pi)^{1/2} \int_0^t g(t-z) e^{-(az+x^2/4Dz)} dz/z^{1/2} \qquad \text{(A-1)}$$

The above integral has been computed as a function of the dimensionless distance parameter $x(\pi/2D\tau_f)^{1/2}$ when g(t) is a square wave of period $2\tau_f$ in the steady state case, that is, when t is large. Figure A-1 shows the resulting form of the temperature variation for two phases of the input flux, the temperature being scaled by

$$(D/\pi)^{1/2} \quad (F/K)$$

*H.S. Carslaw, J.C. Jaeger, Conduction of Heat in Solids, 2nd ed. Oxford: University Press, 1959, pp. 76, 134.

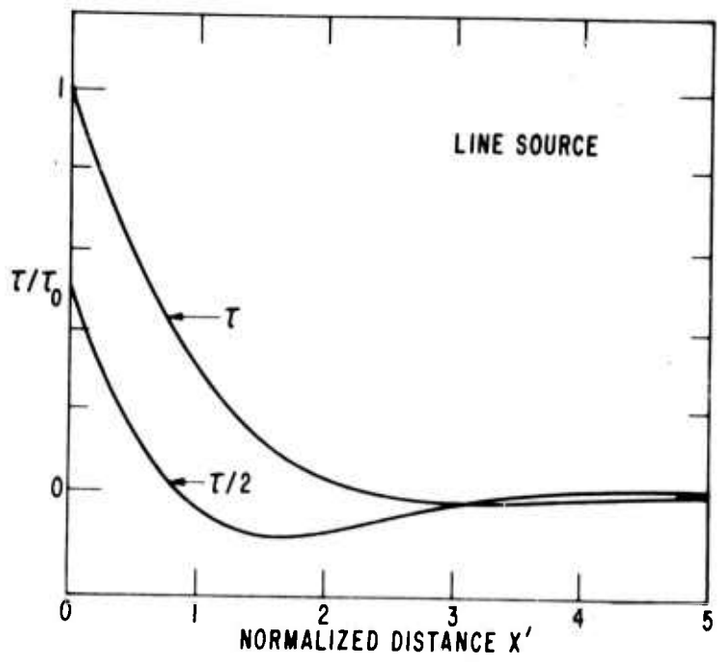

Fig. A-1. Temperature distribution in a thin sheet due to square-wave time-varying flux into a line source, as a function of the normalized distance $x' = x(\pi/2D\tau_f)^{1/2}$. Temperatures shown at end of exposure period and halfway through.

where F is the input flux variation amplitude and K the thermal conductivity. The radiation loss in this case is that due to black body radiation from the surface of the heat stored in the sheet of thickness d and volume specific heat C_v, so that

$$a = 8\sigma T^3/dC_v.$$

In fact, this heat loss, normally of the order of $0.3\ s^{-1}$, has very little effect on the form of the temperature distribution; its inclusion in the integral of Eq. (A-1) is convenient since it produces a reasonably rapid convergence of the integral which otherwise would have the slowly converging form $g(t-z)/z^{1/2}$.

The heat distribution from an arbitrary spatial pattern may now be found by integrating these line-source contributions. The results are shown in Figs. A-2 and A-3 for bar patterns of two different spacings. Temperature distributions at the end of frame exposure and half way through are shown as well as that which would result if there were no thermal diffusion. It can be seen that the spatial resolution limit occurs for a line-pair spacing of

$$\delta = 2.9\ (D\tau_f)^{1/2}.$$

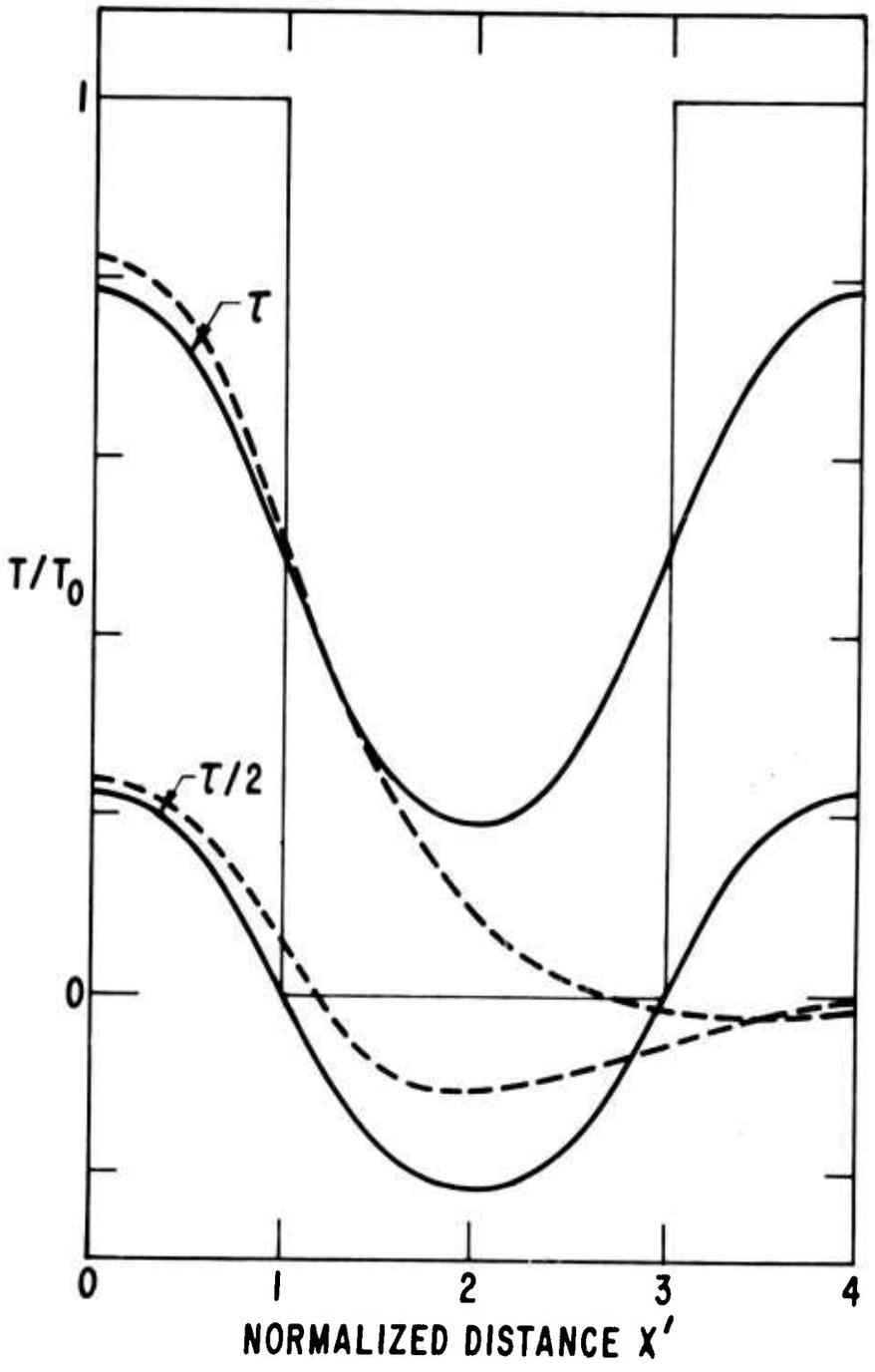

Fig. A-2. Temperature distribution from periodic bar pattern (solid) and single bar (dashed) (as in Fig. A-1). Bar width 2.0 normalized units. Square distribution is that in absence of thermal diffusion.

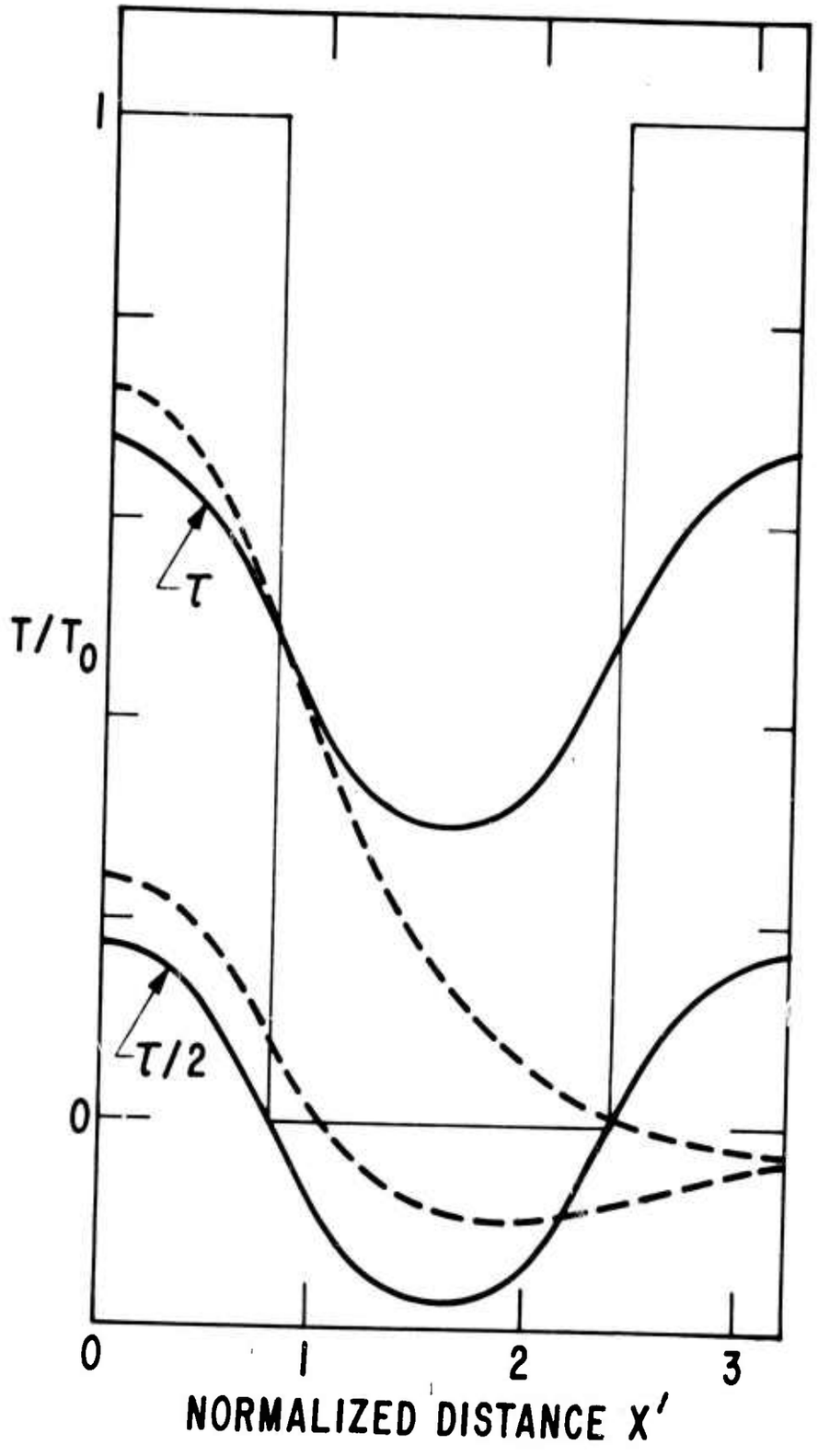

Fig. A-3. Temperature distributions for a bar width of 1.6 normalized units, as in Fig. A-2.

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13. ABSTRACT

Progress made toward the development of pyroelectric/integrated circuit thermal imaging area arrays and their associated address and sense circuits is described. The processing techniques and steps required to form two-dimensional arrays of thin film triglycine sulfate detectors on field-effect integrated circuit substrates are reviewed. The approach to providing the required high degree of thermal isolation between the polycrystalline detectors and the silicon portion of the circuit is to etch away the silicon underlying the detectors. A second pyroelectric imaging array consisting of a thin permanently poled single crystal section of TGS positioned above the integrated circuit substrate is also described. In this arrangement the resulting air gap provides the thermal isolation and contacts to the array detectors are made by means of vacuum deposited microfinger springs. The relative merits of X-Y addressed versus bucket brigade pyroelectric arrays are discussed. An analysis of the performance capabilities of an X-Y addressed polycrystalline TGS array indicates that a system noise equivalent temperature difference of 0.42°C at 10 frames/second should be achievable in an array consisting of 10-μm thick detectors 4 mils on a side and spaced on 8-mil centers.

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