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E-BEAM SIGNAL PROCESSOR DESIGN

A. Bahrcman
Northrop Research and Technology Center
Hawthorne, California 90250

and

G. Döhler
Warnecke Electron Tubes, Inc.
Des Plaines, Illinois 60018

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TECHNICAL REPORT AFAL-TR-73-167

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E-BEAM SIGNAL PROCESSOR DESIGN

A. Bahraman
Northrop Research and Technology Center
Hawthorne, California 90250

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G. Döhler
Warnecke Electron Tubes, Inc.
Des Plaines, Illinois 60018

This Final Report, submitted pursuant to the performance requirements of Contract No. F33615-72-C-1547, contains a description including details of construction, function and operation of an invention for an E-Beam Signal Processor which Northrop asserts was first conceived and first actually reduced to practice at Contractor's private expense prior to award of aforementioned contract, which invention is described, shown and claimed in U.S. Patent Application Serial Number 251018 filed 8 May 1972 under the title "High Speed Deflection Modulated Electron Beam Signal Processor" by Walter E. Crandall et al.

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FOREWORD

The authors would like to express their appreciation to others who have contributed to this program. The dual stage processing concept was proposed by Dr. W. E. Crandall and the deflection addressing scheme was suggested by Dr. O. L. Curtis, Jr. The targets were fabricated by Dr. K. K. Schuegraf. Many thanks to Mr. Sheldon Isenberg and Mr. J. Ashe for their valuable contributions. The authors would also like to thank Capt. C. Owens and Mr. D. McLaine of the Avionics Laboratory and Mr. L. Grohe of Warnecke Electron Tubes for their continuous support during the course of this program. Discussions and suggestions by Drs. O. Döhler, S. Othmer, K. Chun, and C. Ang are also acknowledged. Mr. R. L. Tanquary built most of the experimental hardware for testing the targets.

Publication of this report does not constitute Air Force approval of the report's findings or conclusions. It is published only for the exchange and stimulation of ideas.

WILLIAM J. EDWARDS
Chief, Radar & Microwave Technology Br
Electronic Technology Division
Air Force Avionics Laboratory

ABSTRACT

The significance of this research and development to the Air Force is that a dual stage signal processor system has been developed which has a potential capability of achieving output data rates exceeding 2 Gbit/sec. The design is realized by a state-of-the-art solid state stage and an Electron-Beam-Semiconductor signal processor assembled in series. The former is fabricated from commercially available IC logic chips and has been efficiently interfaced with the EBS processor. The solid state processor multiplexes 64 ns input data pulses into 8 ns pulses to drive the EBS signal processor. The latter multiplexes 8 ns data pulses from 16 input lines into a single output. In this approach, information is placed on the electron beam and read out at the semiconductor target. Output pulse amplitude of one volt into 50 Ω and a pulse width of 0.5 ns has been achieved.

TABLE OF CONTENTS

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LIST OF ILLUSTRATIONS

ILLUSTRATIONS (continued)

SECTION I

INTRODUCTION

In millimeter wave communication systems, PIN diodes are commonly used as modulators in biphase phase shift keying systems. Present state-of-the art silicon device technology has made possible the development of PIN-diodes with switching speeds approaching 2 Gbits/sec. However, data rates higher than 1 Gbit/sec have not been possible because of the power-frequency limitations of transistor drivers. This report describes the design and development of an Electron-Beam-Semiconductor (EBS) signal processor that is potentially capable of achieving more than 2 Gbit/sec output data rate and should provide sufficient output current to drive a PIN-diode at these rates.

The primary design goal is to obtain output pulses of 0.5 ns minimum width and 1V amplitude into 50 Ω load. The desired pulse rise-time is 0.1 ns. To make the design compatible with solid state logic circuitry and provide for ability to process data from more than 100 lines, a dual stage processor system is designed which consists of a solid-state and an electron-beam processor. The latter includes a pencil-beam electron gun, a beam modulation system, and a single semiconductor target designed for 5GHz bandwidth. Information is placed on the electron beam and is read at the target as described in Section II. The solid state processor multiplexes 128 data lines into 16 and provides the data and the RF power to the e-beam processor inputs.

In addition to wide bandwidth, our EBS signal processor design offers considerable versatility. Higher output data rates can be achieved by increasing the input RF frequency and data rate. At still higher input frequencies, the target may be exchanged with a higher bandwidth device to increase the output data rate. Furthermore, the EBS processor provides for complete isolation of the output from the input. The single diode target design offers high yield in fabrication, processing, and target replacement.

SECTION II

TECHNICAL APPROACH

The design approach to the e-beam signal processor system described in this report stems from our understanding of the basic function of a signal processor, as depicted in Figure 2.1. The processor output signal drives a PIN-diode modulator at data rates of 2 Gbit/sec or higher. The drive signal is produced by the interaction of an electron beam with a semiconductor target. At the processor inputs, a set of e-beam address-gates are used to place information on the electron beam and hence produce the desired data pattern at the output.

The program goal is to multiplex 64 ns-wide data pulses into 0.5 ns-wide pulses at the processor output. We achieve this in two processing stages: a state-of-the art solid state stage, and an e-beam signal processor assembled in series. The 0.5 ns minimum output pulse-width is determined from the PIN-diode modulator response limitations - the switching speed of the present state-of-the art PIN diodes does not exceed 2 Gbit/sec. The input minimum pulse-width of 64 ns is chosen from the following considerations: (1) design and fabricate the solid state processor from commercially available off-the-shelf integrated circuit packages so that development costs are kept at a minimum, (2) provide the e-beam processor with 2^n, $n \leq 4$, data inputs in order to make the device compatible with commercial high speed solid state logic circuits, and (3) keep the input RF frequency sufficiently low so that the power levels required for beam modulation and addressing could be attained with little difficulty and at low cost. The system design approach is described below.

2.1 E-BEAM PROCESSOR

Figure 2.2 shows a schematic presentation of the e-beam processor design approach. The device includes (1) a CRT-type electron gun which produces a pencil beam, (2) a deflection system which launches the beam into conical

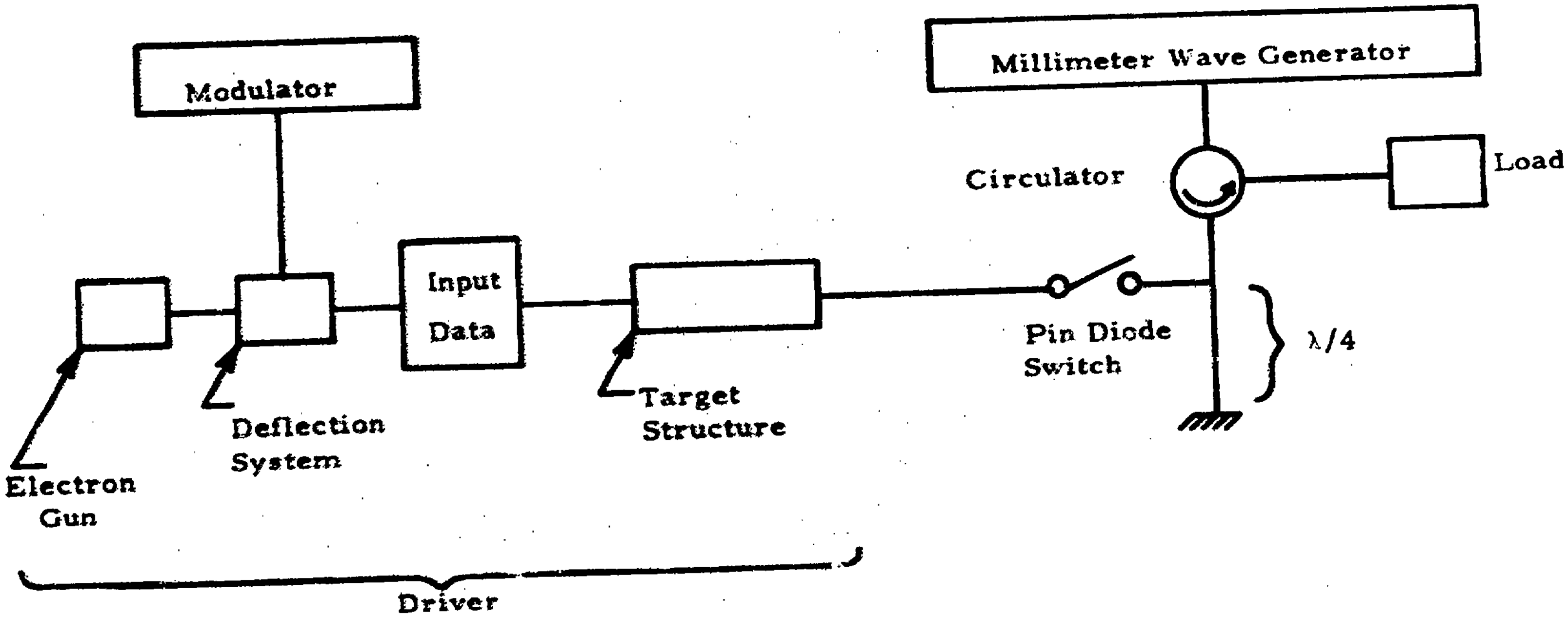

Figure 2.1. Schematic of the e-beam data processor driving a PIN-diode switch.

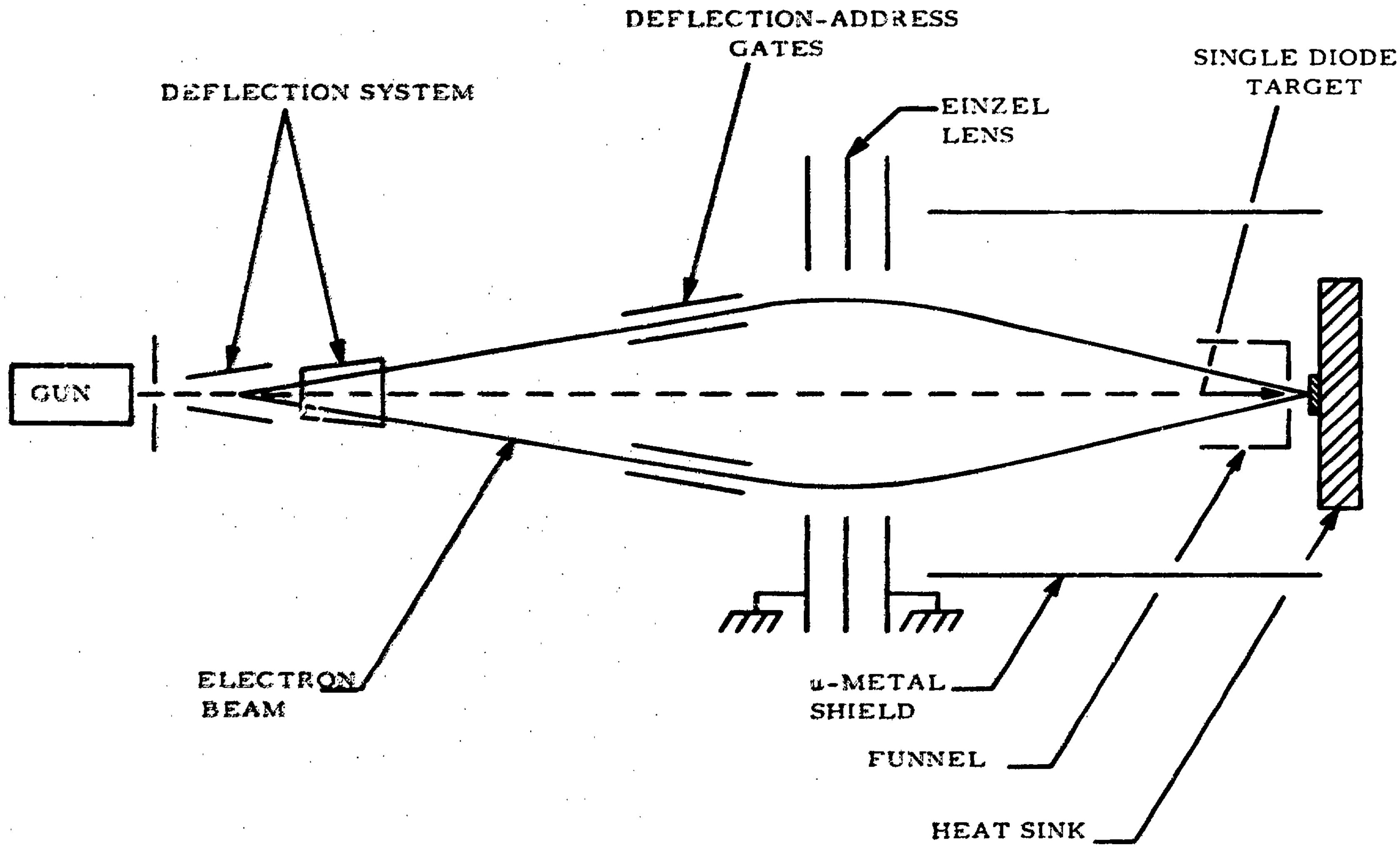

Figure 2.2. Single target e-beam processor design.

rotation about the processor center axis, (3) a gate structure for addressing the beam, (4) an Einzel lens which bends and focuses the beam onto the target, (5) a semiconductor target which, when bombarded by the beam, provides the output signal, and (6) a funnel which further focuses and aligns the beam onto the target.

The processor operates in the following manner: the electron gun is biased to provide an electron beam along the axis. A sinusoidal signal (125 MHz) on the deflection system causes the beam to go into conical rotation, i.e., once the beam exits the deflection system, it traces a circle in any plane perpendicular to the center axis. The gate structure consists of 16 pairs of deflection plates mounted in a ring concentric with the center axis, and each pair of plates is a beam address-gate. As indicated in Figure 2.2, the electron beam emerges from the deflection system with the proper angle to go through the address-gates. Then it enters the Einzel lens and is bent and focused onto the target. If an information signal is present on an address-gate when the beam goes through it, the beam gets deflected off the target and a pulse appears at the output. It is also possible to operate in the opposite mode, that is, the beam is off the target in the absence of a gate signal and on the target when there is a gate signal.

2.2 SOLID STATE PROCESSOR

The solid state processor provides the RF signal for the beam-rotation deflection system and the data for the address-gates of the e-beam processor. The oscillator is tuned to the beam rotation frequency of 125 MHz. With 16 beam address-gates, the solid state processor would include 16 multiplexers, with each one multiplexing 8 input data lines into one output line terminated at an address-gate. Only one multiplexer section is built under this contact. Figure 2.3 illustrates the solid state processor design concept. The synchronous counter shown in the figure binarily divides the oscillator output by 8 to supply the line-select signals for the multiplexers. This scheme ensures that the outputs of the oscillator and the

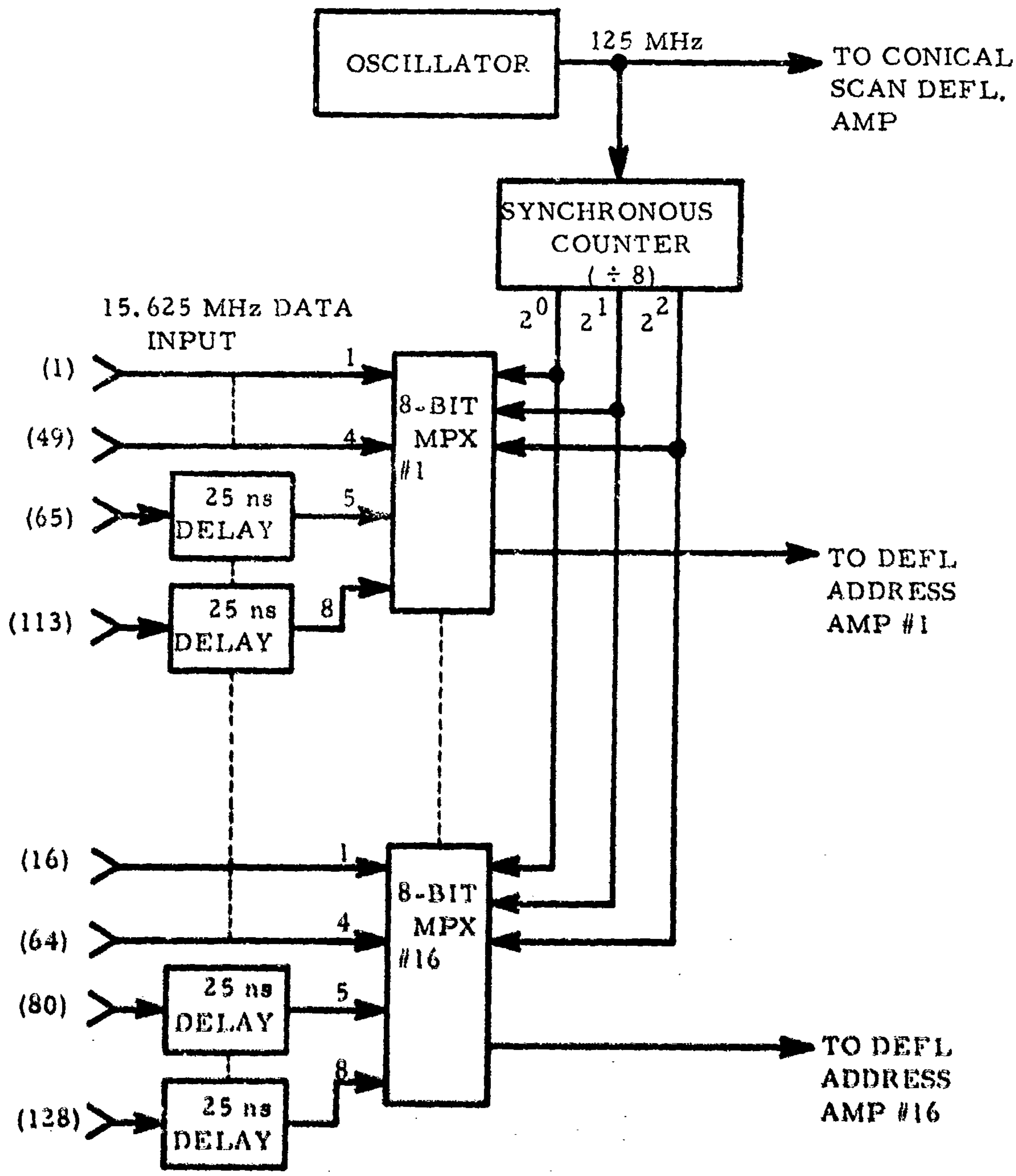

Figure 2.3. Block diagram presentation of solid-state processor design. The processor multiplexes 128 input lines into 16.

multiplexers are synchronized and hence the data is read at the e-beam processor in correct sequence and timing. To interface the solid state processor with the e-beam processor, amplifiers are used at the outputs of the oscillator and the multiplexers, as indicated in Figure 2. 3

The dual stage data processing sequence is achieved in the following manner. A set of 128 input lines are multiplexed into 16 lines by 16 multiplexers that are connected to the 16 e-beam address-gates. Multiplexer #1 processes the eight input lines #1, 17, 33, 49,....., 113; multiplexer #2 is addressed by lines #2, 18, 34, 50,....., 114; multiplexer #3 processes input lines #3, 19, 35, 51,..... 115; and so on; multiplexer #16 has input lines #16, 32, 48, 54,....., 128. Assume time zero begins when the beam just enters address-gate #1. The information on line #1 (multiplexer #1) is now transmitted to the beam. After about 0.5 ns, the beam enters address-gate #2 and receives the information on line #2. After another 0.5 ns, the beam enters the address-gate #3 and is addressed by the information on line #3, and so on through 16. Thus at time t = 8 ns, the beam is back at the input of address-gate #1 and reads the information on line #17. At t = 8.5 ns, the beam enters the address-gate #2 and receives the information on line #18. At t = 9 ns, the information on line #19 is read in, and so on through 32. In the next 8 ns, bits #33 through 48 are processed. Thus in eight beam revolutions, i.e., 64 ns, 128 bits on the 128 input lines are read-in. Since it is desirable to have the sampling of each bit occur at a reasonable time interval from the beginning and from the end of the data pulse, it is suggested that the data on lines 65 through 128 be delayed by 25 ns relative to data on lines 1 through 64, as indicated in Figure 2. 3.

SECTION III

E-BEAM PROCESSOR DESIGN AND FABRICATION

Figure 3.1 shows the schematic of the demountable E-Beam Signal Processor system, including 4 demountable "0" type flanges allowing the removal or adjustment of the electron gun (left), the 16-gate system and/or deflection magnifier (central left), the Einzel-lens system (middle right) and the target funnel system (right). The different components inside the demountable E-Beam Signal Processor will be discussed in the following.

3.1 THE ELECTRON GUN

The electron gun is an oxide cathode CRT type electron gun. Figure 3.2 shows the schematic of the electron gun. Three different types of electron guns are available, giving similar results when current and resolution are compared. They are different from each other in the final apertures listed as A, B and C in Figure 3.2. The electrodes, from left to right, are as follows: grid (voltage up to - 200V/cathode), lower (or first) anode (voltage up to + 4 kV/cathode), focus, and upper anode (grounded). Due to the length of the lower anode barrel, a lower magnification ratio was achieved without an appreciable decrease in the net current output of the gun. A spot size of less than 1 mm was obtained at the 16-gate system position, the current measured at the target position was in excess of 100 µA. The ratio between cathode current and final beam current was measured to be less than 30 - under some conditions, less than 15.

The electron beam exiting the electron gun is slightly convergent, with a maximum diameter corresponding to the "C" diameter (.067" maximum).

3.2 DEFLECTION SYSTEM

Satisfactory operation of the signal processor very critically depends on the generation of perfect conical beam rotation. Three methods have been used to produce conical beam rotation. Since magnetic deflection at 125 MHz

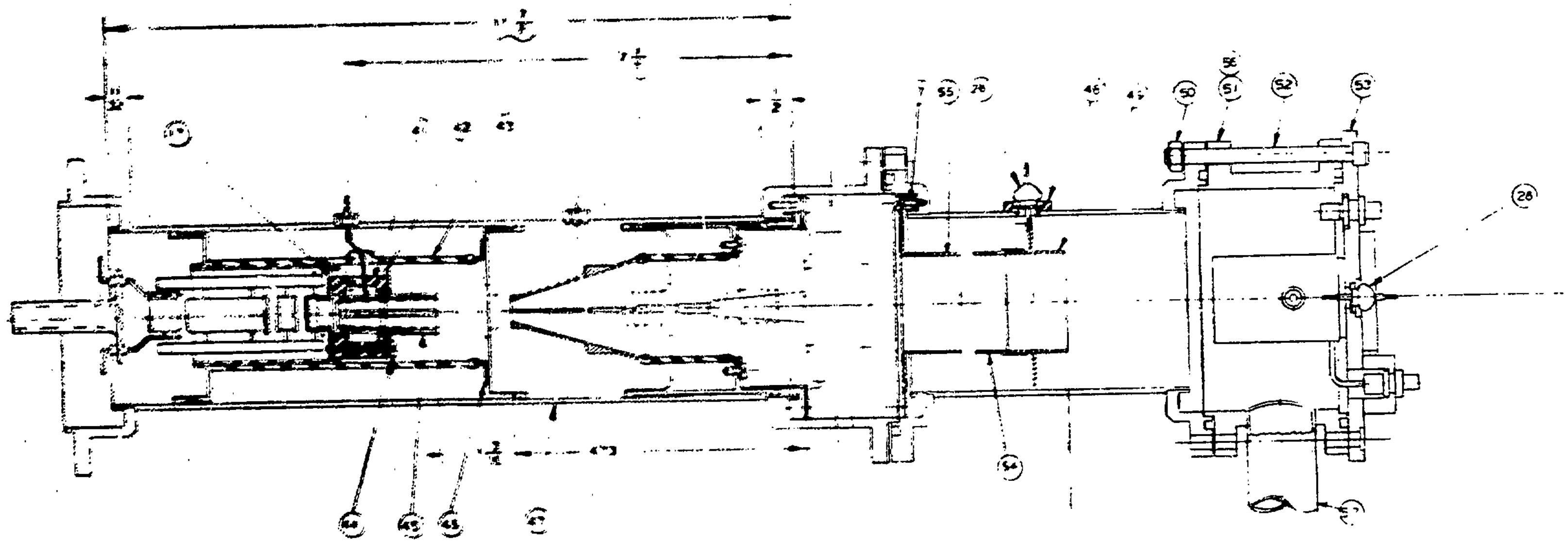

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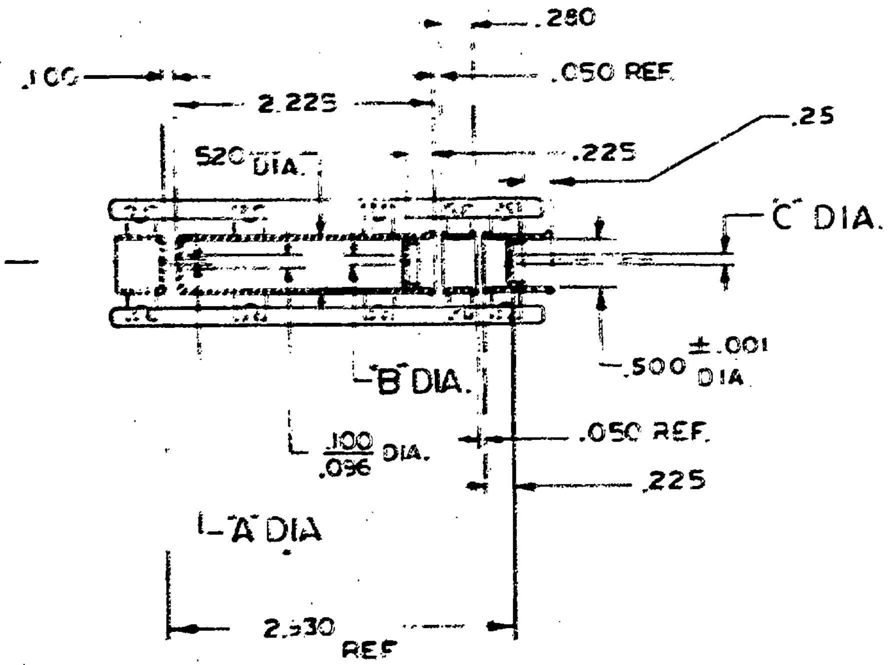
Figure 3.1. Schematic of the demountable e-beam signal processor.



PART NUMBER	"A" DIA.	"B" DIA.	"C" DIA.
-001	.036	.067	.067
-002	.031	.067	.050
-003	.031	.050	.050

Figure 3.2. Signal processor electron gun.

is difficult to achieve, electrostatic deflection had to be used. The classical double pair of horizontal and vertical deflection plates was inadequate: the centers of deflection of the two pair of plates are physically apart; hence, one can generate a circle only in one chosen plane perpendicular to the center axis - the rotation pattern is elliptical in any other plane.

Another system which gave satisfactory results consisted of three pairs of deflection plates, say, horizontal-vertical-horizontal deflection plates. Analytical results indicated that by proper design it is possible to have the center for horizontal deflection coincide with that for vertical deflection for small deflection angles. The system would therefore achieve the desired conical beam rotation, i.e., a circular beam rotation pattern in any plane perpendicular to the center axis. The design and theoretical analysis is given in Appendix I.

A problem with optimal operation of a system of three pairs of deflection plates is that the beam may have an appreciable deflection when it enters the third pair of plates and the gap between these plates must be sufficiently large to insure the beam does not get cut-off. In addition, if the beam does get through, some distortion will result because of the leakage fields at the edges of the plates. To minimize these problems, it is necessary to allow for a smaller cone angle, i.e., make the distance from the deflection system to the gates large, and increase the gaps on the horizontal deflection plates. The latter, in turn, requires more input drive power.

In order to achieve a larger cone angle and eliminate the distortion problems mentioned above, a new deflection system called deflectron[1] was considered. Theoretical and experimental results showed that more than 2000V was necessary on each axis of the deflectron to produce the required deflection with a 10 kV electron beam. This was achieved with a very high Q resonant circuit, but adjustments for the proper amplitude and phase on both axes were too critical for practical applications. Moreover, the coupling between the two axes was excessive. These problems were solved by using a deflection amplifier, as schematically represented in Figure 3.3.

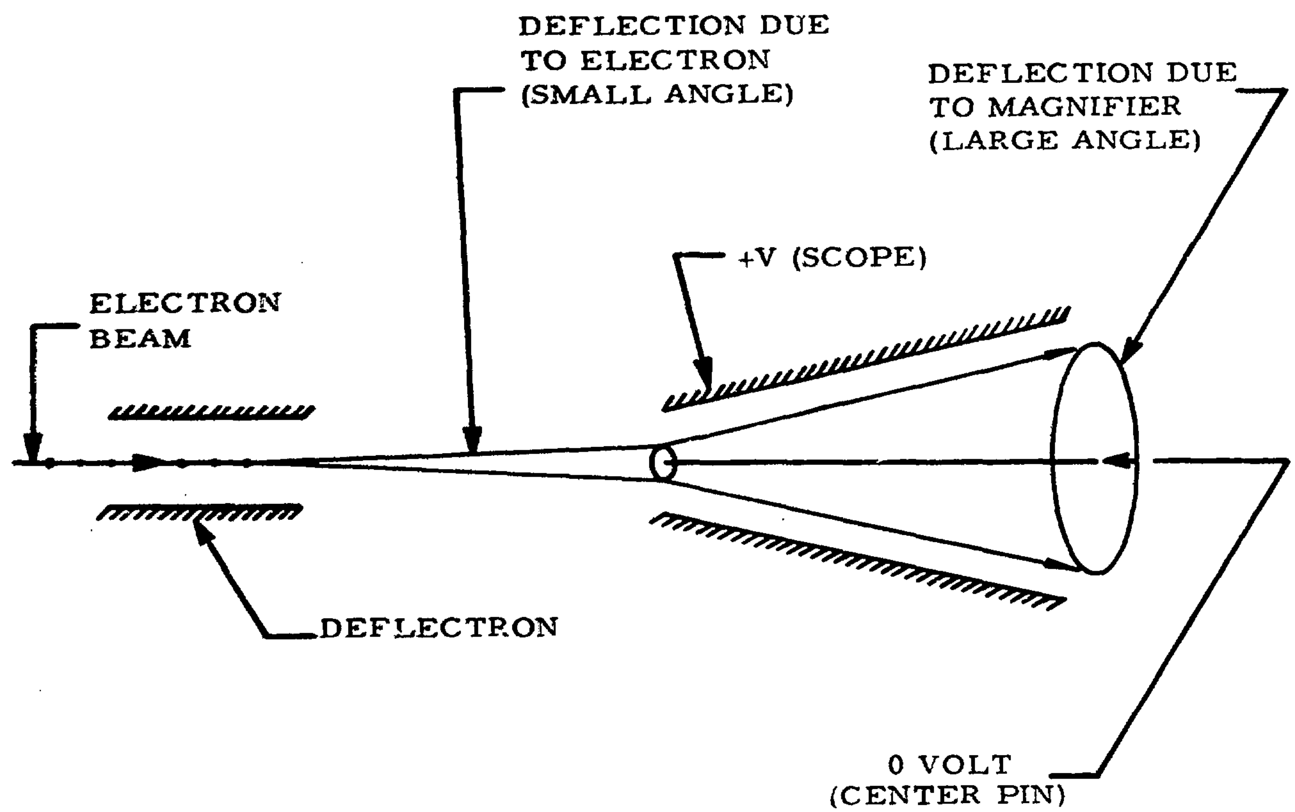


Figure 3.3. Schematic of the deflection system.

Figure 3.4 shows the actual device mounted in position for assembly. The electron gun is shielded into the metal cylinder on the left side of the picture. The deflectron is the short cylinder mounted just to the right of it. The deflection cone is in the center of the picture and the center pin is supported by the 16-gate system (right side), as shown.

Figure 3.5 shows the subassembly of the deflectron on top of the metal cylinder used for the electron gun alignment. Figure 3.6 shows the center pin supported by the 16-gate system, and Figure 3.7 shows the subassembly of the cone of the deflection magnifier.

The deflectron has two deflection axes which require two equal RF signals with about 90° phase difference in order to generate conical beam rotation. In order to obtain sufficient deflection, the two axes should be resonated at the desired frequency and the coupling between the two axes need also be tuned out. Since it is not advisable to have any of the tuning components inside the vacuum system, a triangular deflection box was built on the lower neck of the E-Beam Processor which contains the necessary deflection circuits, schematically represented in Figure 3.8. There are two tank-circuits, one compensation network to reduce coupling between the two axes of deflection, and two dc correction networks. The three variable, high voltage quartz trimmers have been adjusted for a frequency of 126 MHz. Coupling between the two tank circuits has been reduced to a minimum for that frequency. The three trimmers can be adjusted externally to the deflection box.

3.3 DEFLECTION-ADDRESS-GATES

This structure is made in annular cone sections and consists of a grounded metal piece with 16 metal plates mounted around it in the form of a ring. Figure 3.9 shows a schematic cross section of a gate structure. The structure is precision-mounted to have its center axis aligned with the axis of the gun and the deflectron.

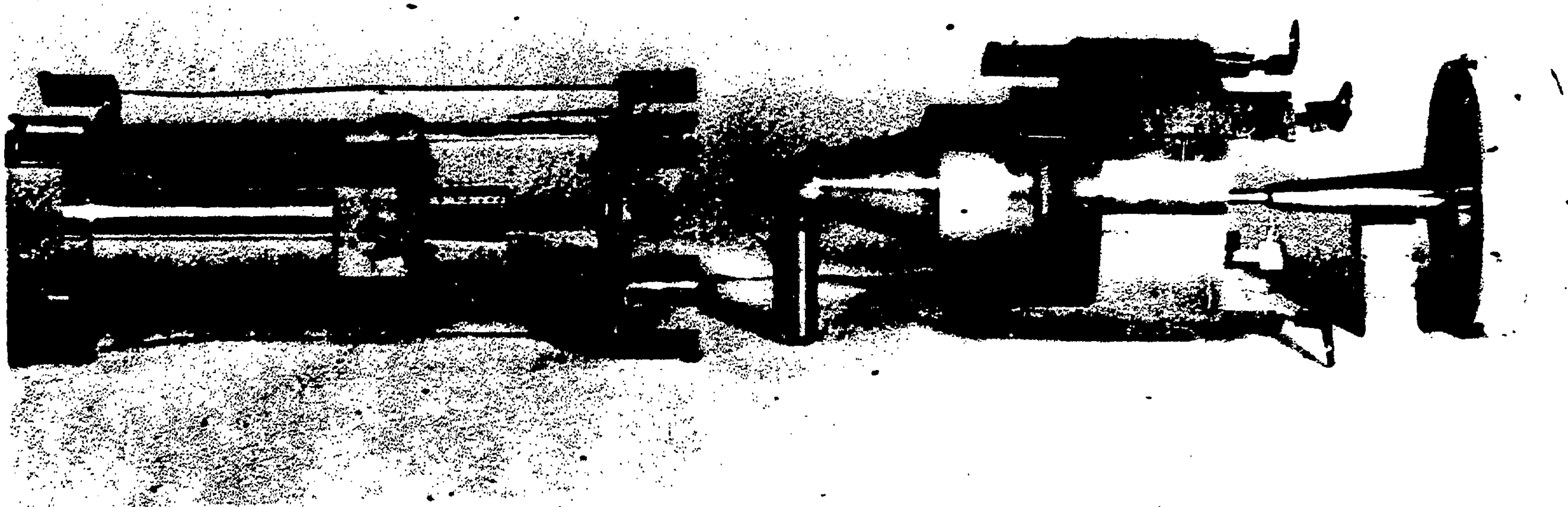


Figure 3.4. Subassembly of the Deflection System

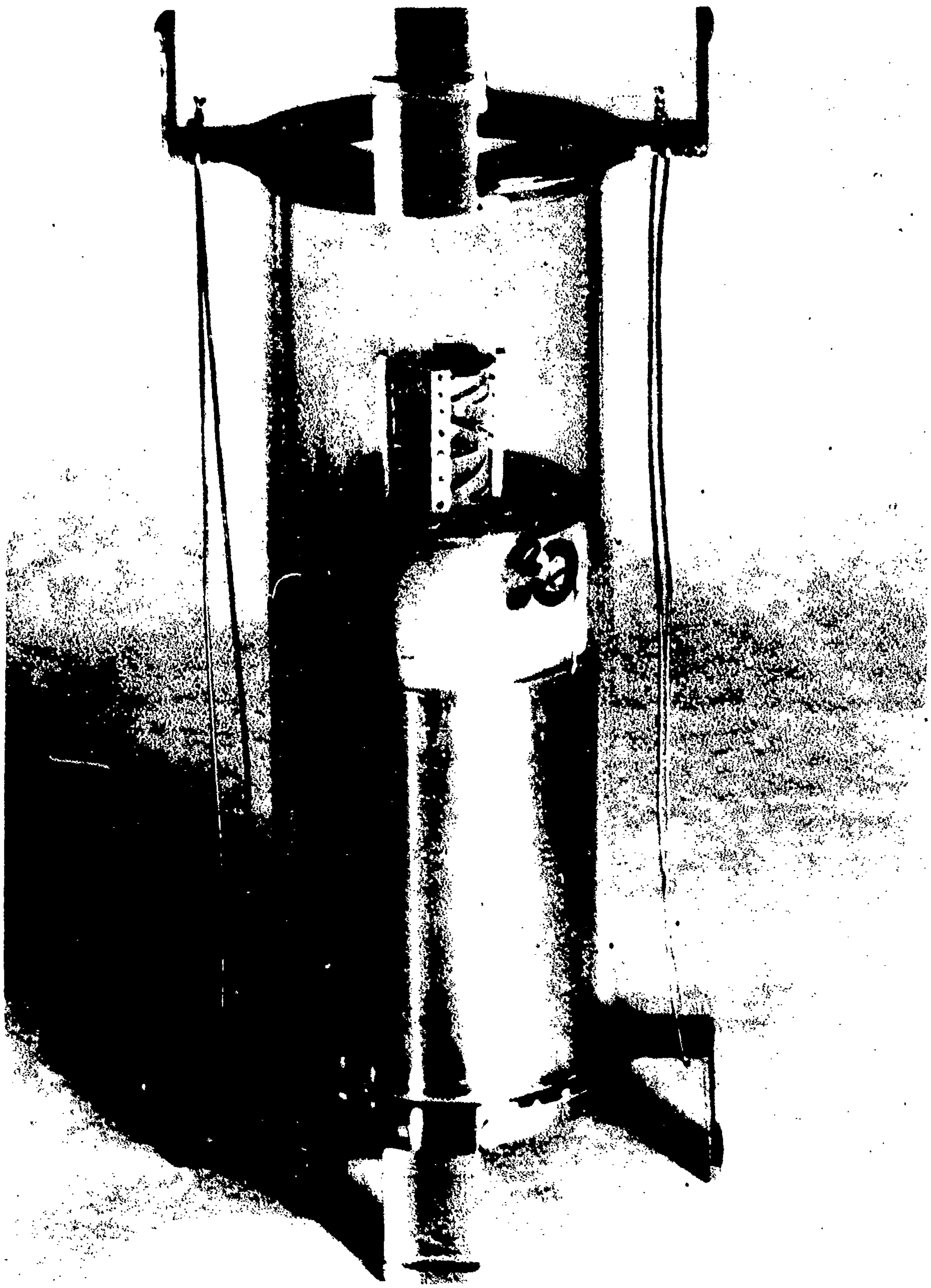


Figure 3.5. Deflectron mounted on top of the electron gun insertion tubing.

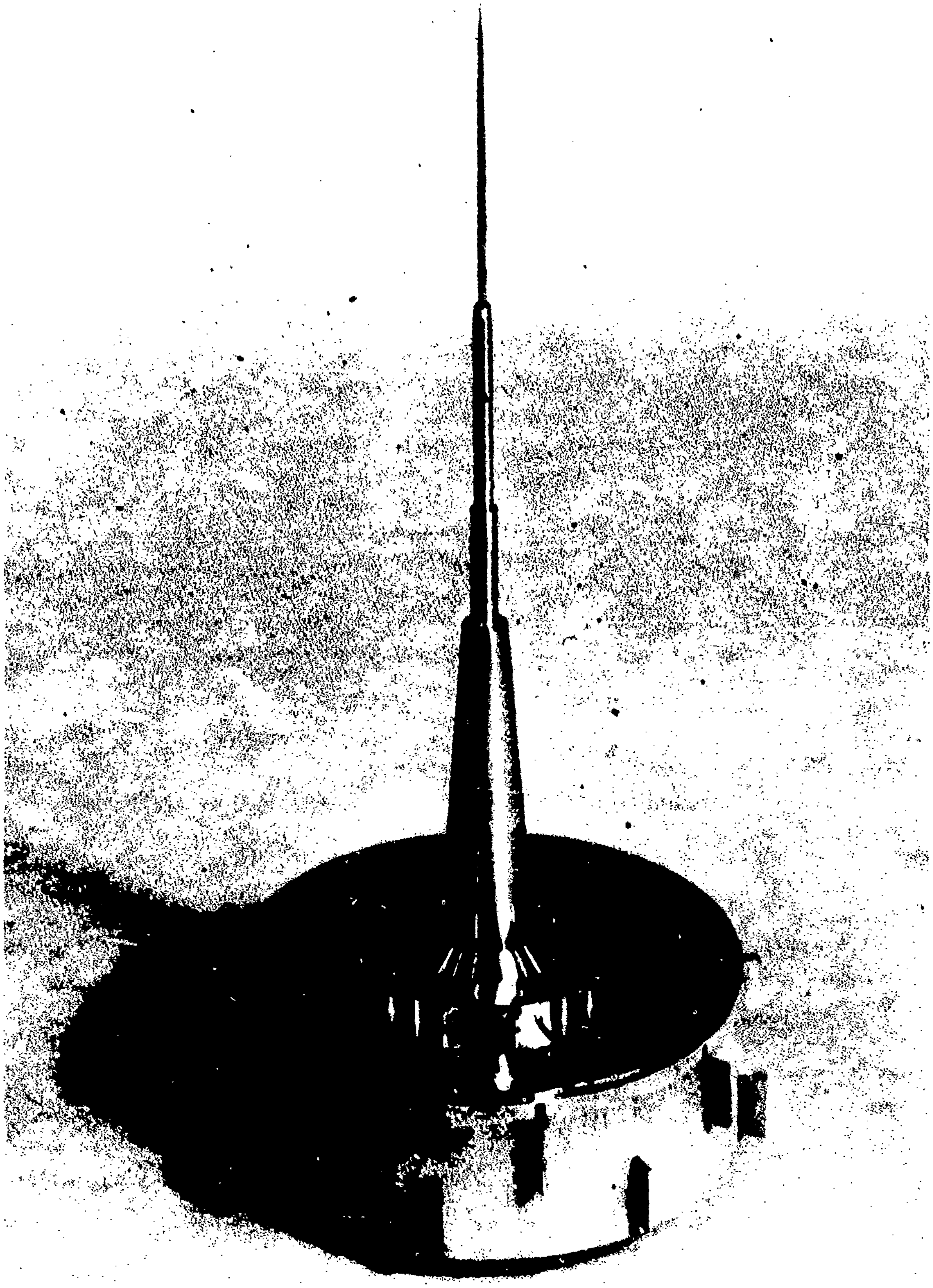


Figure 3.6. Center pin of the deflection magnifier supported by the gate assembly.

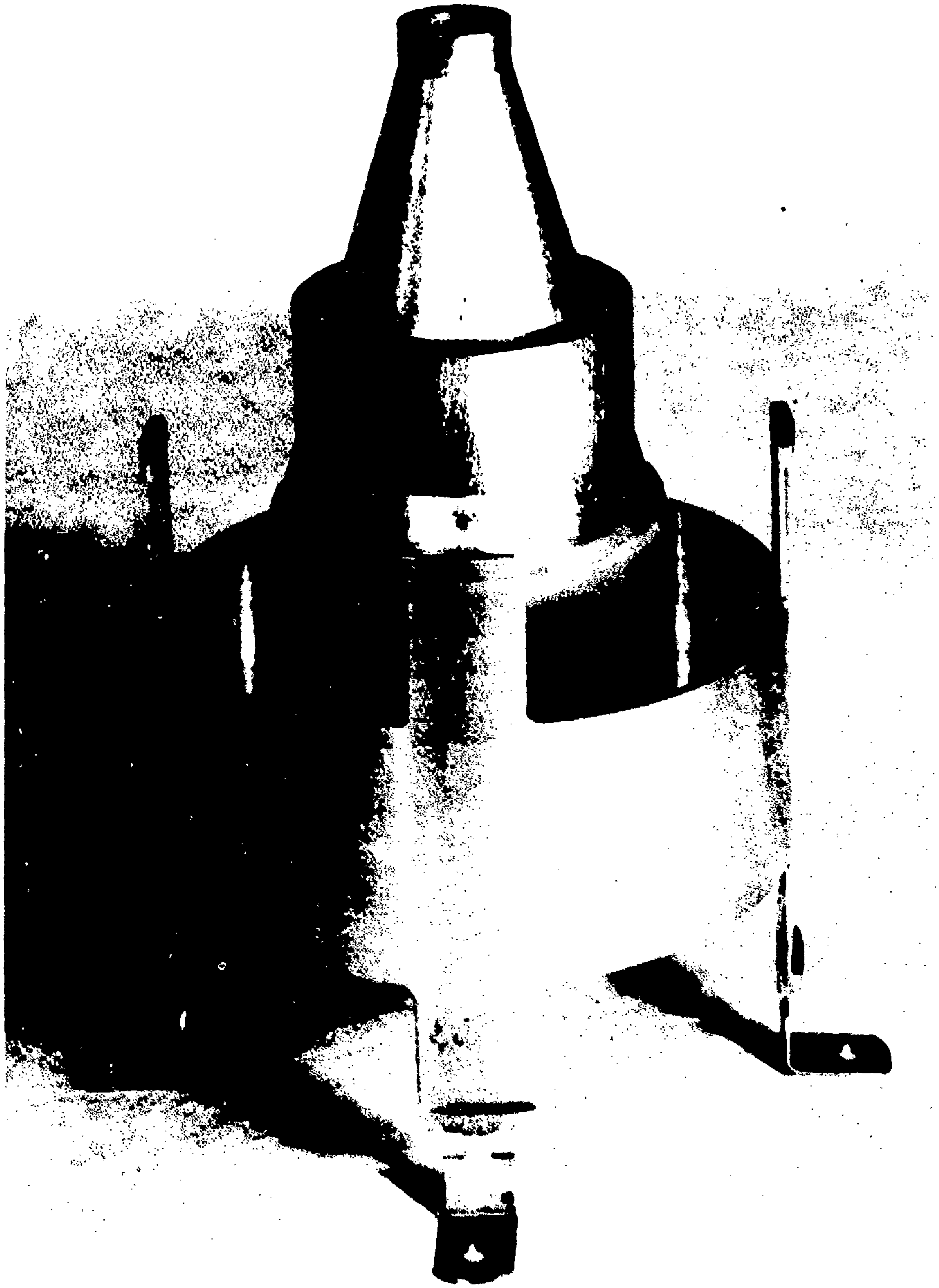
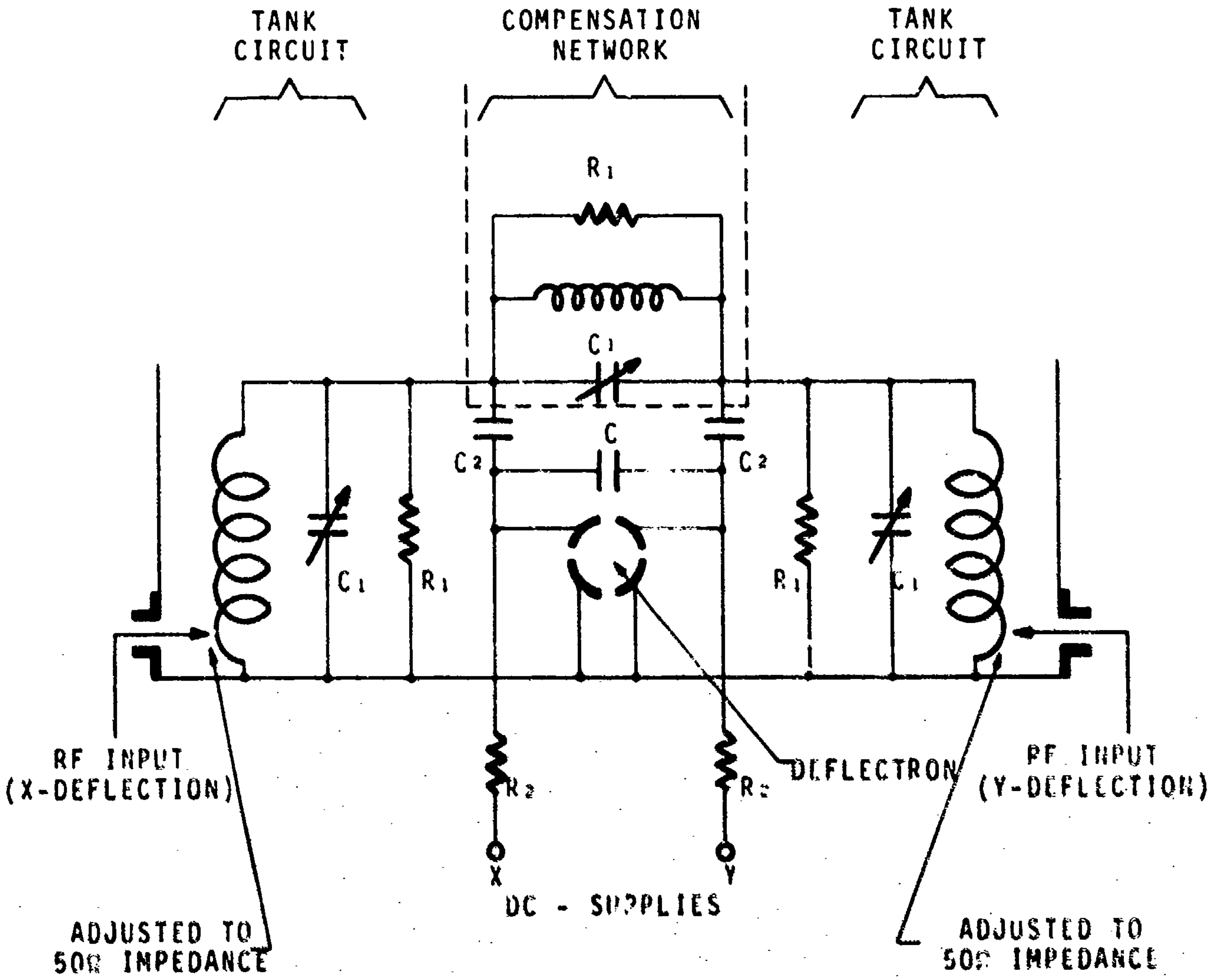


Figure 3.7. Subassembly of the deflection mangifier core.



C_1 = High rf voltage quartz trimmer capacitors, variable .8 - 10 pf, voltage rating 2500 V (Newark Catalog 101, p. 284, Stk No. 17F194, by Johanson).

C_2 = 2000 pf, 6 kV Standby voltage (Newark Electronics, Stk No. 19F498).

C = Deflectron Coupling Capacitor.

R_1 = Carbon Resistor 150-200 kΩ.

R_2 = Carbon Resistor 1-2 MΩ.

Figure 3.8. Schematic of the deflectron circuitry.

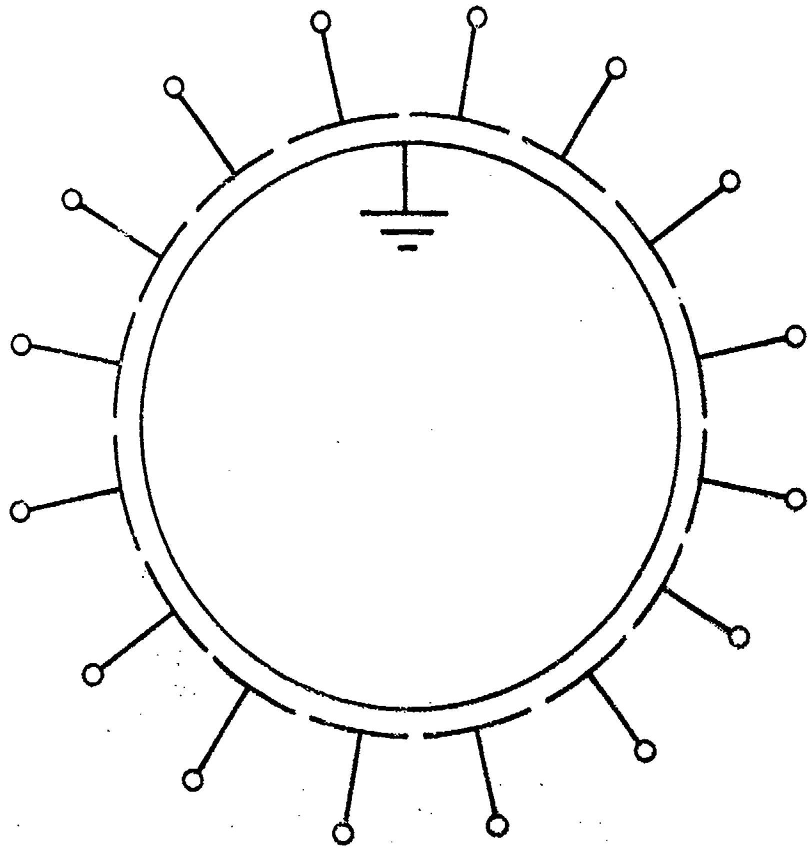


Figure 3.9. A schematic of the Deflection-Address System.

In each rotation cycle the electron beam reads the data on all the gates. That is, during each cycle, a number of bits equal to the number of address gates appears at the target output. The output data rate is therefore equal to the beam rotation frequency times the number of address gates. Hence, for 16 gates and beam rotation at 125 MHz, the output data rate is 2 Gbits/sec. The time period that each gate operates on the beam in one rotation cycle is T/N, where T is the period of rotation and N is the number of gates. For our design T = 8 ns, N = 16, and T/N = 0.5 ns, i.e., the pulse width for each bit at the target output is about 0.5 ns. Since one bit is read from each gate in one period T, data must arrive at each gate at the rate of 1/T = 125 Mbits/sec.

In order to make the design compatible with high speed solid state logic circuits, the number of gates was chosen a binomial 2^n. With n = 4, i.e., 16 gates, the beam rotation frequency is 125 MHz and it was felt that the design and fabrication of the solid state processor to drive the e-beam processor could be achieved without much difficulty. With n ≤ 3, the solid state processor would be costly and difficult to fabricate. With n ≥ 5, the realization of the e-beam processor would become difficult.

The design requirements for the address gates are: (1) the width of each gate plate must exceed five beam widths, (2) the separation between two adjacent gates should be about one beam width. These restrictions insure a pulse rise-time of less than 0.1 ns and pulse width of ~0.5 ns at the target, as required in the program, (3) the coupling between gates should be minimized by using ground planes inbetween adjacent plates, (4) the capacitance of each gate should be kept to less than 10 pf in order to facilitate the loading of 8 ns input data pulses. Figures 3.10a and b show the first 16-gate system constructed. Note that 5 mil thick "fins" have been introduced between the single gates, so as to minimize the coupling from gate to gate. Figure 3.11 shows the display obtained on a phosphor screen located behind the 16 gate system. The beam voltage was 7.8 kV, beam current on the screen lowered to 10 μA. Eight gates were tied to ground potential (the center cone is grounded). The other 8 gates were tied

Figure 3.10. First deflection-address system (front view).

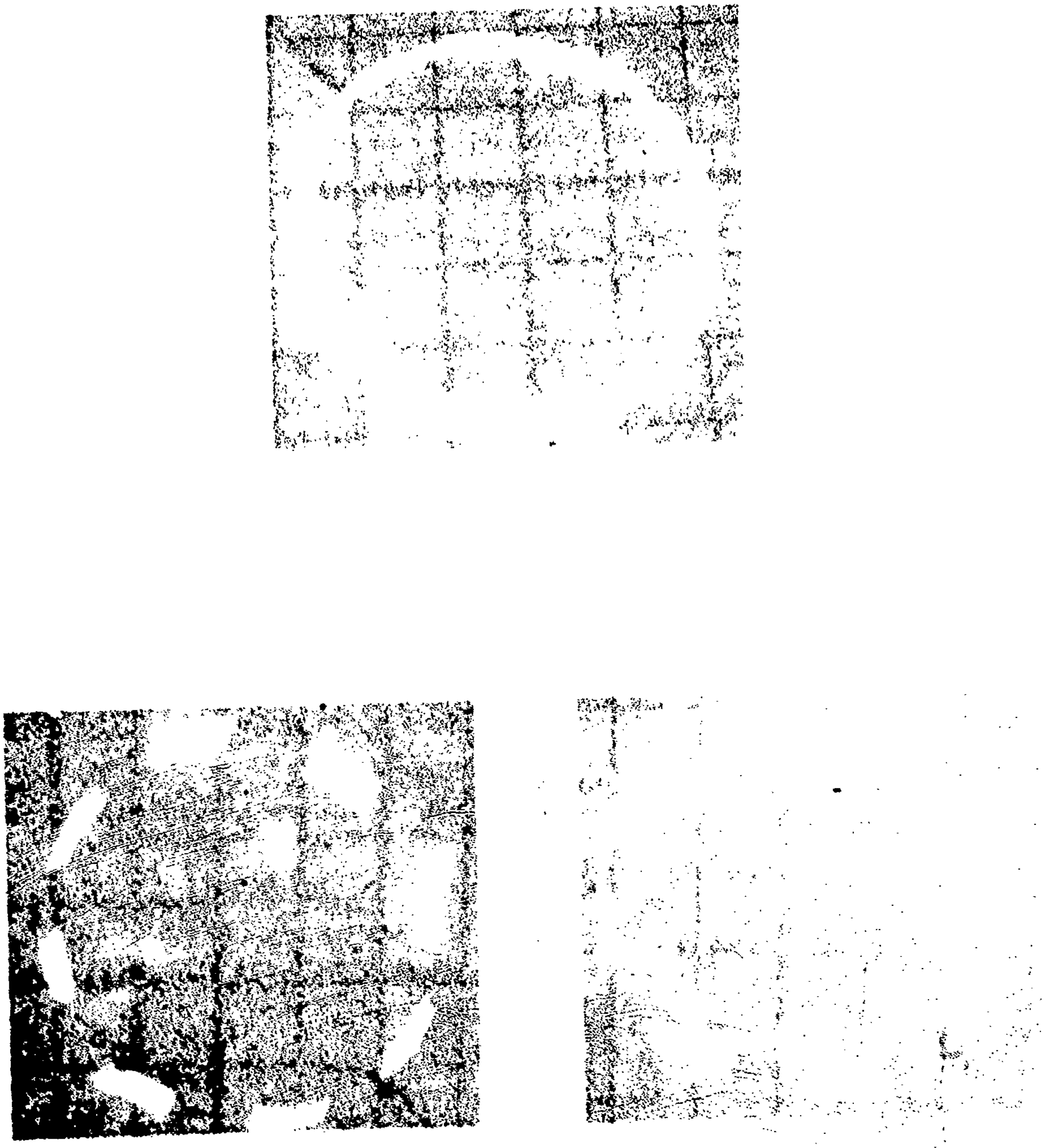


Figure 3.11. Beam pattern emerging through the gate system of Figure 3.10.

together, and some dc voltage applied. By increasing this dc voltage, alternate gates displayed a deflected electron beam. On the lower right picture, sufficient voltage was applied to the gates in order to remove the beam totally from the screen. Note that the elliptic display observed on the screen (see, for example, upper left picture in Figure 3.11) is not only due to the angle at which the pictures were taken, but also due to the non-common center of deflection. Furthermore, these pictures and the experiments carried out showed:

a) a common center of deflection for all axes, especially x and y-axes, is absolutely necessary.
b) the switch voltage for the gates had to be reduced, thus requiring an increase of the length of the gates and/or a decrease of the gate to ground spacing.
c) the signal on the screen does not seem to be sharp enough to fulfill the requirement of a 0.1 ns rise time on the target. Thus, the spacing between gate and fin had to be reduced.

Figure 3.12a and 3.12b show the final 16-gate system with increased gate length, slightly decreased gate to ground spacing, and reduced spacing between gates and fins. Note that the center pin has not been assembled onto the gate system.

Finally, Figure 3.13 shows the gate system inserted into the demountable E-Beam Signal Processor.

The spacing between gate and ground plane has been reduced to about 62 mils. The capacity of a gate with respect to ground is about 8.9 pf.

3.4 EINZEL LENS

The Einzel lens is a three aperture or a three cylinder strong lens. Its function in the processor is to bend and focus the conically rotating beam onto the target. The lens should be designed for very low spherical

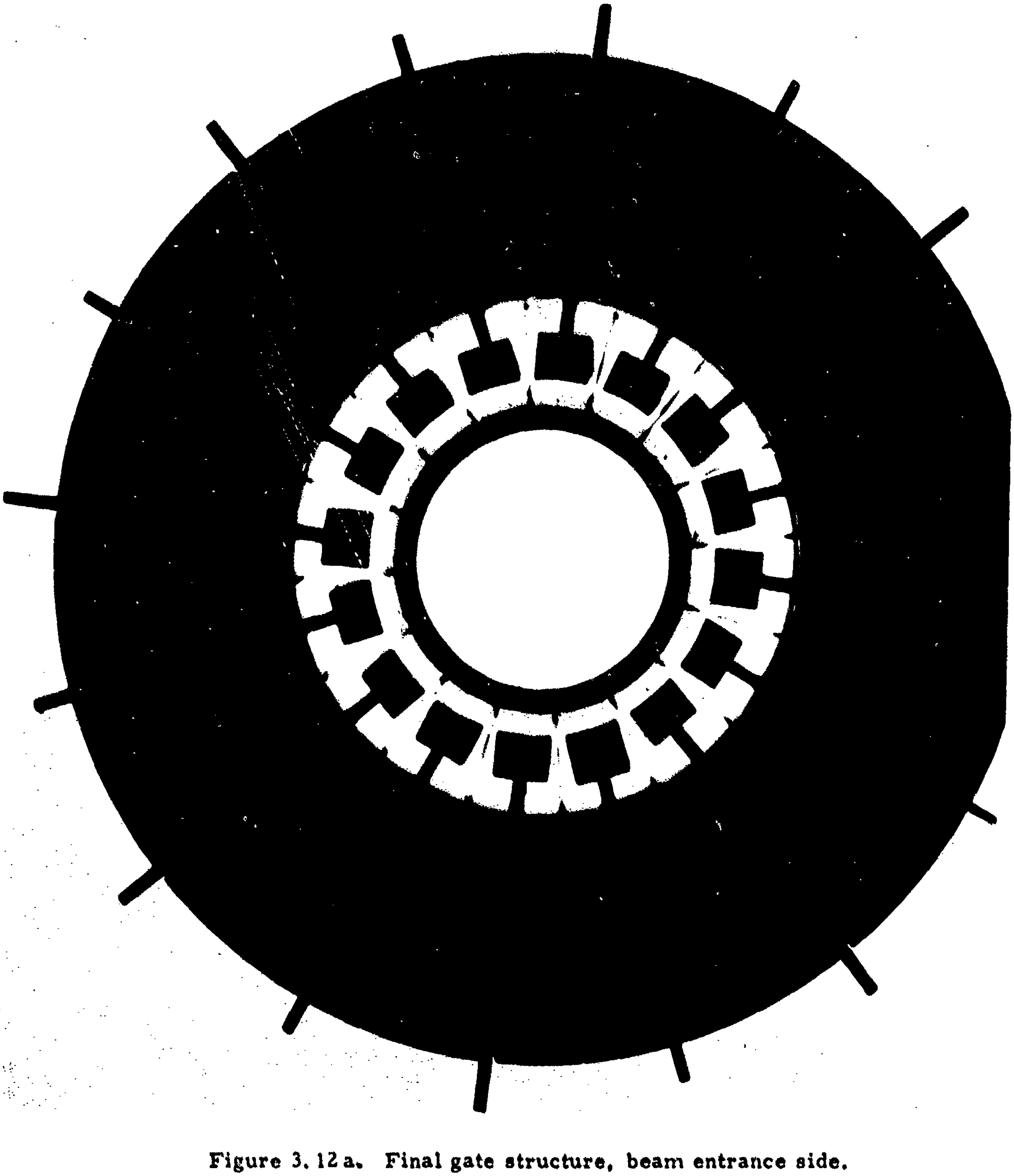


Figure 3. 12 a. Final gate structure, beam entrance side.

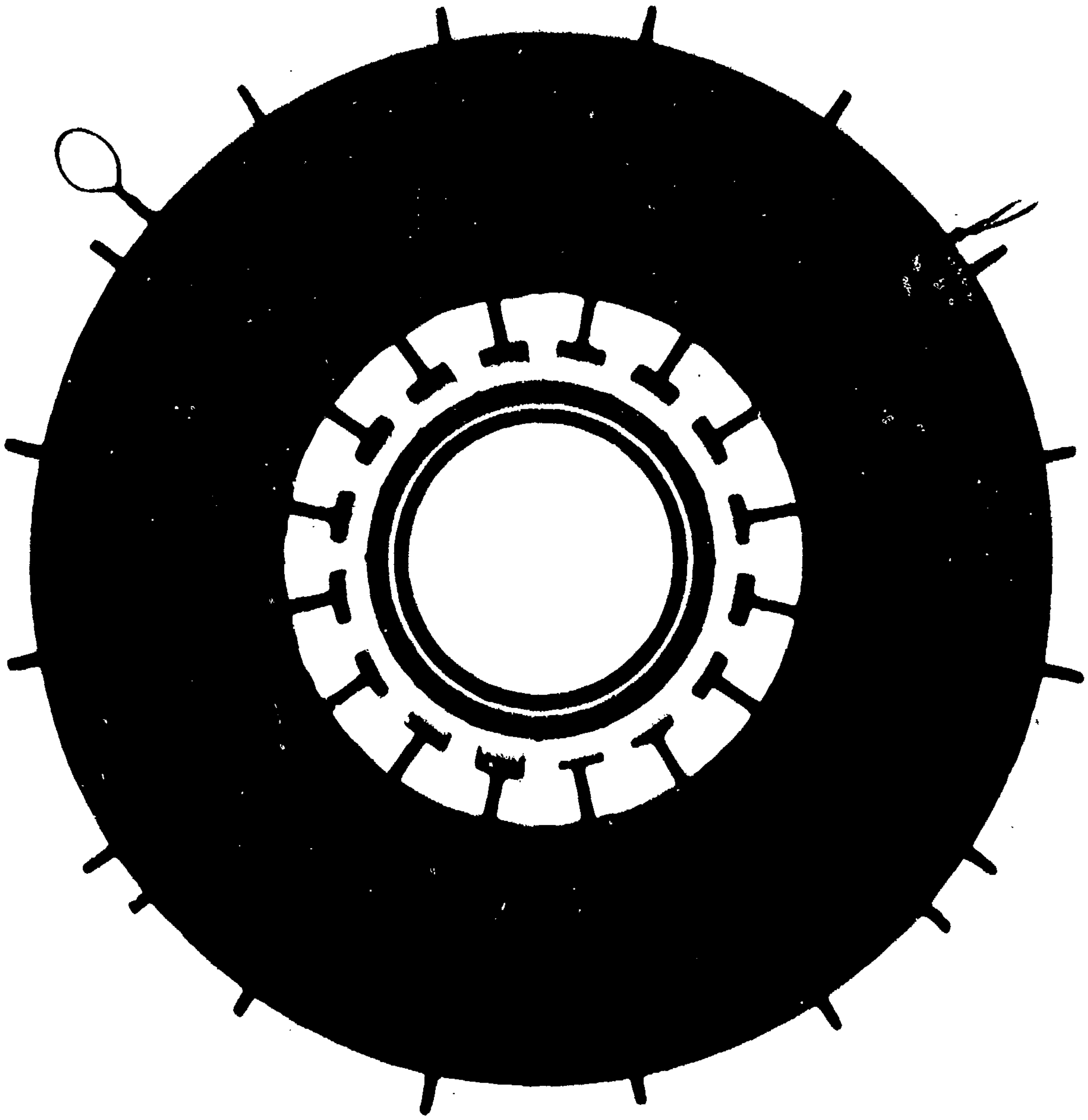


Figure 3.12b. Final gate structure, beam exit side

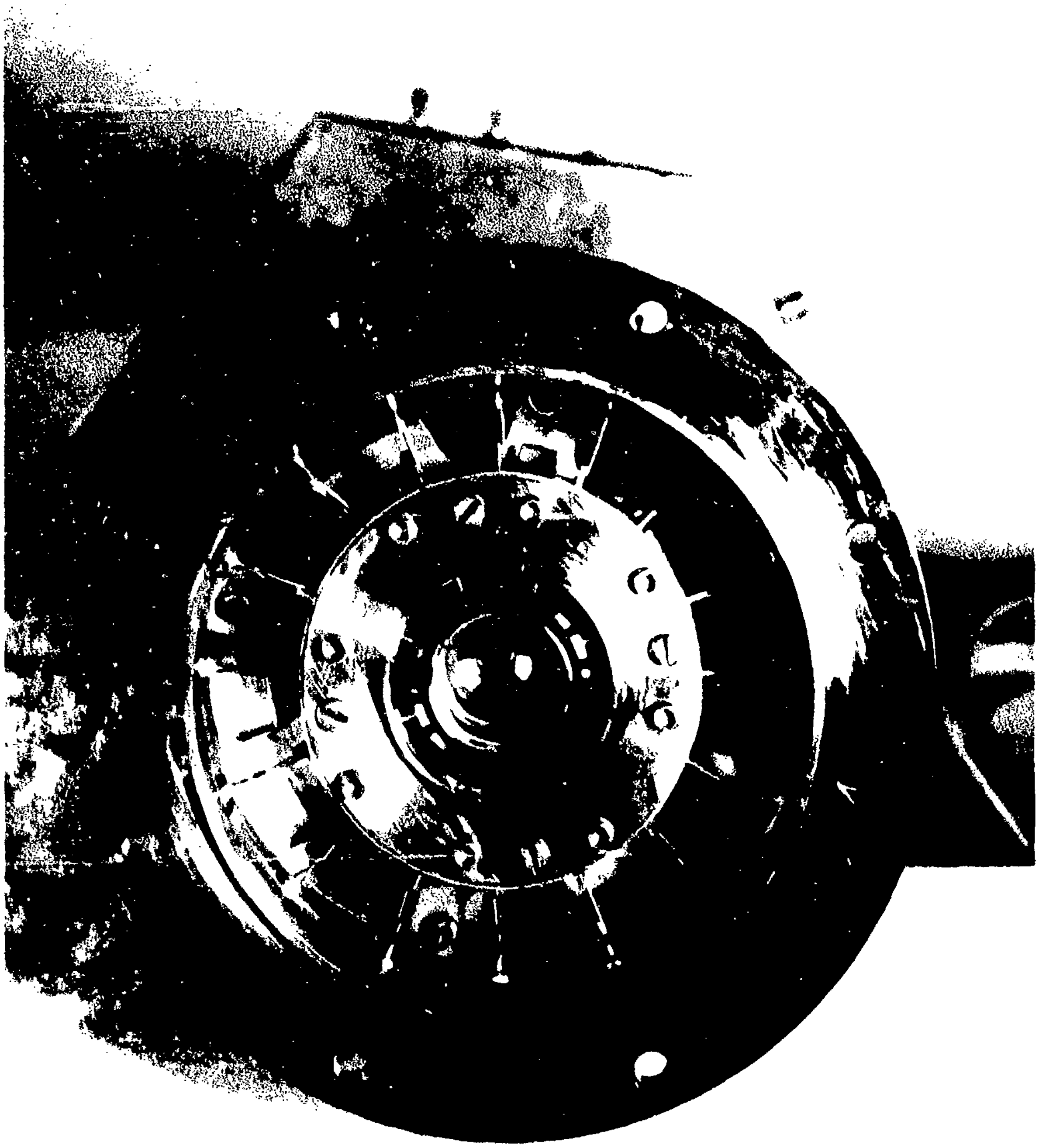


Figure 3.13. Final gate system inserted into the demountable e-beam processor.

aberration and its center axis should be exactly aligned with the axis of the processor. If the beam rotation pattern is elliptic rather than circular, the beam could not be focused onto the target from all azimuthal positions. Similar results will follow with even perfect conical beam rotation if the lens is misaligned, and especially so if the lens exhibits large spherical aberration. The latter causes another problem which can only be solved by changing the lens design: the variation of the lens focal length across the diameter of the beam will produce a cross-over point in front of the target plane. Hence the beam reaches the target diverging. We have observed this behavior experimentally by putting a phosphor screen in place of the target plate.

Aberration becomes worse as one moves away from the center of the lens. Hence, to reduce aberration problems, the lens radius must be made about twice the radius of beam rotation where the beam enters the lens. Also, the theoretical results of El-Kareh et al.[2,3] may be used to design a lens with low spherical aberration. A lens fabricated on their results showed good focusing characteristics.

The position of the Einzel lens in the processor is shown in Figure 3.1. Figure 3.14 gives the lens data. The first lens used in the tube had a shorter and larger-diameter inner electrode. However, with the cathode at - 10 kV, about - 15 kV was needed to bend the beam onto the target. To reduce the voltage, it was necessary to make the lens stronger, which was achieved by increasing the length of the inner cylinder and reducing its diameter.

3.5 FUNNEL

This device is used to ease the alignment requirements on the target. The function of the funnel is to position and center the electron beam, after it is bent by the Einzel lens, onto the target. Two different structures were used. The first was a magnetic funnel. The iron-core magnetic circuit

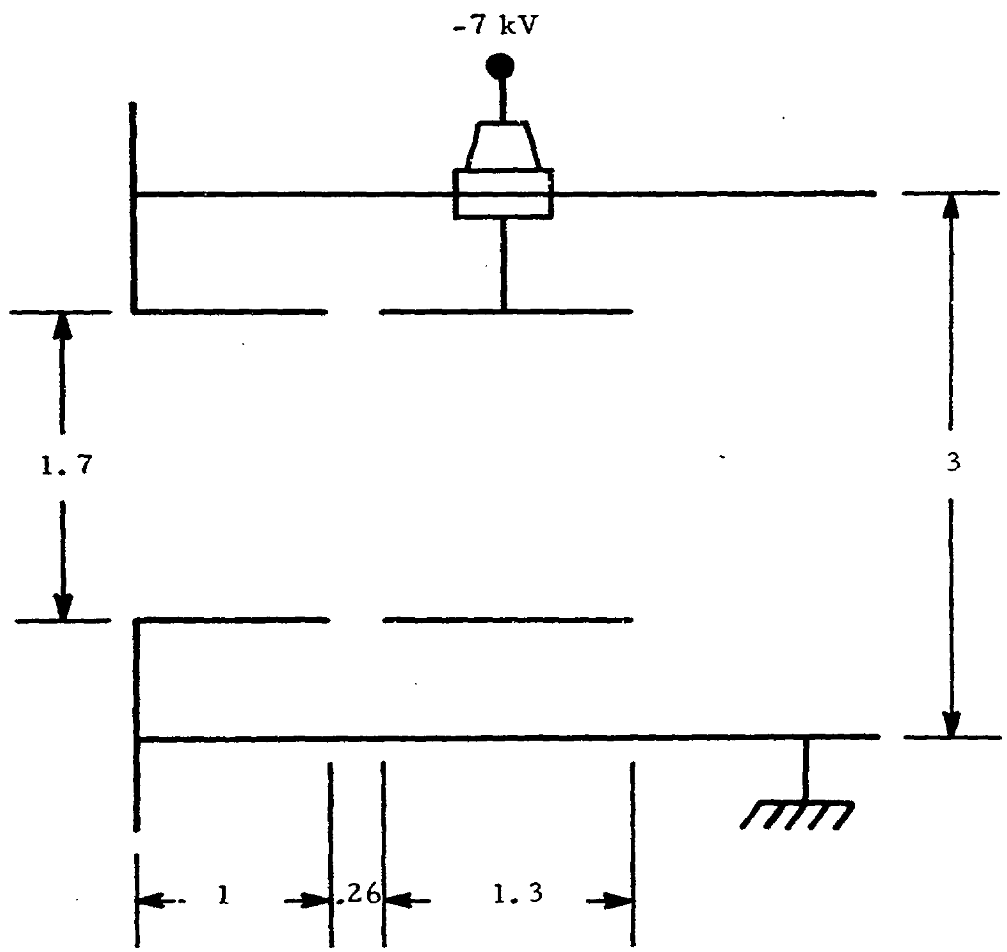


Figure 3.14. Schematic of the refocusing Einzel lens. Dimensions in inches.

produced a high density of field lines through the target and hence focused the electrons onto the target position. The effectiveness of this design depends on the highest achievable magnetic field and the length of time an electron spends in the field. Experimental results showed that the funnel functioned properly. However, the input power required (250 mA at 30V) was too high and did not permit efficient heat-sinking of the target. An electrostatic funnel was therefore developed which could be built on the target heat sink.

Consider a three cylinder Einzel lens. If one cylinder is removed and a flat plate perpendicular to the cylinder axis is inserted in place of it, a funnel-like device results. The design of this device is now similar to the design of an Einzel lens and the data of El-Karch et al.[2,3] may be used. The flat plate constitutes the target mounting plate, and the dimensions of the cylinders are chosen to achieve strong lensing action and also allow for easy entry of the converging electron beam which emerges from the processor Einzel lens. Figure 3.15 shows the funnel and target assembly.

3.6 TARGET

The target is a single silicon p-n junction device. The main program requirements in the development of the target are to achieve 5 GHz bandwidth and 0.1 ns pulse rise-time into 50 Ω when the device is excited by a modulated electron-beam source. Target life under bombardment by 10 keV electrons is also of primary concern. Semiconductor diodes usually show degradation in their reverse current-voltage characteristics in an electron beam environment. The degradation is associated with an increase in reverse current and a decrease in breakdown voltage. This damage is not fundamental and may be prevented by proper design, to be discussed below.

Consider a p^+- n - n^+ diode with an electron beam incident on the p^+ side of the device. It can be shown that for maximum bandwidth the device must satisfy the equations[4]

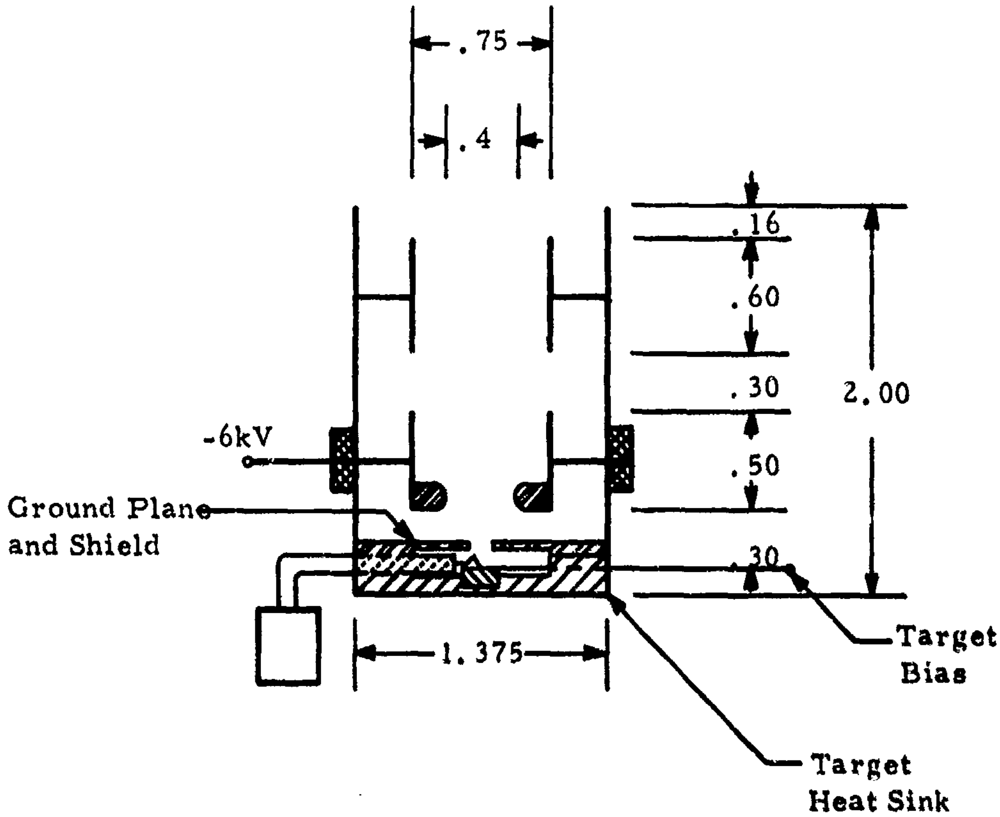


Figure 3.15. Schematic of the funnel and target assembly. Dimensions are in inches.

$$\omega_{3db} \cdot T = 1.895$$

$$RC = T/2.77$$

$$T = W/v_s$$

where ω_{3db} is the 3db frequency, T is the electron transit time across the depletion region, R is the load impedance, C is the device capacitance, W is the depletion region width, and v_s is the electron saturation velocity. The capacitance is given by

$$C = \frac{\varepsilon \cdot \varepsilon_o A}{W}$$

where A is the diode area, ε is the diode dielectric constant, and ε_o is the permittivity of free space. For $\varepsilon = 12$, $\omega_{3db} = 5$ GHz, $R = 50\,\Omega$, and $v_s = 8 \times 10^6$ cm/sec for Si, the above equations give the following design parameters:

$$T = 6 \times 10^{-11} \text{ sec} \quad RC = 2.2 \times 10^{-11} \text{ sec}$$
$$W \simeq 5\ \mu m \quad C = .44 \text{ pf}$$
$$A = 2.2 \times 10^{-2}\ mm^2 \quad D = 150\ \mu m$$

where D is the diode diameter. The saturation velocity of $\sim 8 \times 10^6$ cm/sec is reached in Si at an electric field of about 20 kV/cm[5]. Therefore, for $W = 5\ \mu m$, a reverse bias of at least 10V is needed on the diode to insure saturation velocity conditions in the depletion region. On the other hand, whether 10V bias will actually deplete a 5 μm junction depletion region depends on the n-layer carrier concentration. For a p^+-n step junction[6]

$$N_B = \frac{2\varepsilon\varepsilon_o}{q} \cdot \frac{V + V_o}{W^2}$$

where V is the reverse bias, V_o is the junction built-in voltage, and N_B is the n-layer doping. The ratio $V + V_o/W$ is the average junction electric field E. Hence

$$N_B = \frac{2 \epsilon \epsilon_o}{q} \cdot \frac{E}{W}$$

Using E = 20 kV/cm, W = 5 μm, and ϵ = 12, we find $N_B = 5 \times 10^{14}$ cm^{-3}. That is, the n-layer resistivity must be ρ = 9 Ωcm[7]. For a p^+ -n diode, if ρ is chosen larger than that calculated above, the junction width at 10V will exceed 5 μm and the average junction field will be less than 20 kV/cm. Both of these will result in lower bandwidth. On the other hand, if ρ is chosen smaller, a voltage of more than 10V will be required to achieve a 5 μm depletion width. The average junction field will also exceed 20 kV/cm, and at 5 μm depletion width, the device will satisfy maximum bandwidth requirements. However, because of the larger needed reverse bias, power dissipation will be higher than in the case with ρ = 9 Ωcm.

For a p^+-n-n^+ diode, the n- epitaxial layer should be exactly 5 μm. The resistivity may then be chosen greater than 9 Ωcm. Thus at 10V, the whole 5 μm n-layer will be depleted and the electric field will be at 20 kV/cm.

The penetration depth of 10 keV electrons in Si is about one micron. The energy loss profile is not linear in the 1 μm region and peaks within this distance.[8] Hence, for efficient carrier multiplication and collection it is desirable to locate this peak in the depletion region. From the data of Reference 8, the junction depth, i.e., the thickness of the p^+-layer should be 0.3 - 0.5 μm.

The above data provide all the necessary information for the fabrication of devices. However, other considerations are needed in order to achieve a reliable device under electron beam bombardment. For unpassivated diodes, direct exposure of the junction depletion region to an e-beam results in an appreciable increase in reverse leakage current. This is probably due to creation of tunneling and/or generation-recombination centers in the junction. For SiO_2 passivated diodes, charging of the oxide layer by an electron beam will create a field-induced junction and inversion layer under the oxide and hence will give rise to channel currents and low breakdown voltage.[6] The principal problem is therefore to provide for complete passivation of the device where the p-n junction interfaces the surface. The usual SiO_2 passivation is inadequate as described above. To deal with the problem, we have used two techniques: (1) the use of polycrystalline silicon for electron charge leakage and as a protective beam shield on the oxide layer, and (2) a p^+- guard ring at the junction periphery which removes the junction interface at the surface to a more protected region under the oxide. Also, a diffused 0.3 μm p^+ region has a small radius of curvature where the junction reaches the surface. This small radius causes premature breakdown near the surface. The guard ring provides for a much larger radius of curvature and hence eliminates the difficulty.

Our deposited polycrystalline silicon has sheet resistivities of the order of 0.5-1 megohms/cm^2. Furthermore, we have not observed any appreciable carrier multiplication in poly-Si when bombarded by up to 15 keV electrons. Therefore, the material provides good shielding without affecting high frequency device operation. Nevertheless, the poly-Si and the guard-ring add some extra capacitance to the diode which will reduce the bandwidth by 10 to 15%, especially since the diode capacitance is calculated to be as low as 0.44 pf.

Figure 3.16 shows our target design based on the above analysis. The output current is specified at 20 mA. At 10 kV, we expect, due to losses in 500 Å aluminum layer, a carrier multiplication of about 2000. The diode output current density is 100 mA/cm^2. Hence, a beam current density of 100/2000 or 50 mA/cm^2 is needed. At 11V bias, the power dissipation in the target is 1 kW/cm^2 peak from the power supply and 0.5 kW/cm^2 from the beam. Total peak power dissipated in the target is 0.3W. Actual average power depends on the mode of operation (beam on target with 1 or 0) and the ratio of the number of 1's to 0's during use. The design of the heat sink is given in Appendix II.

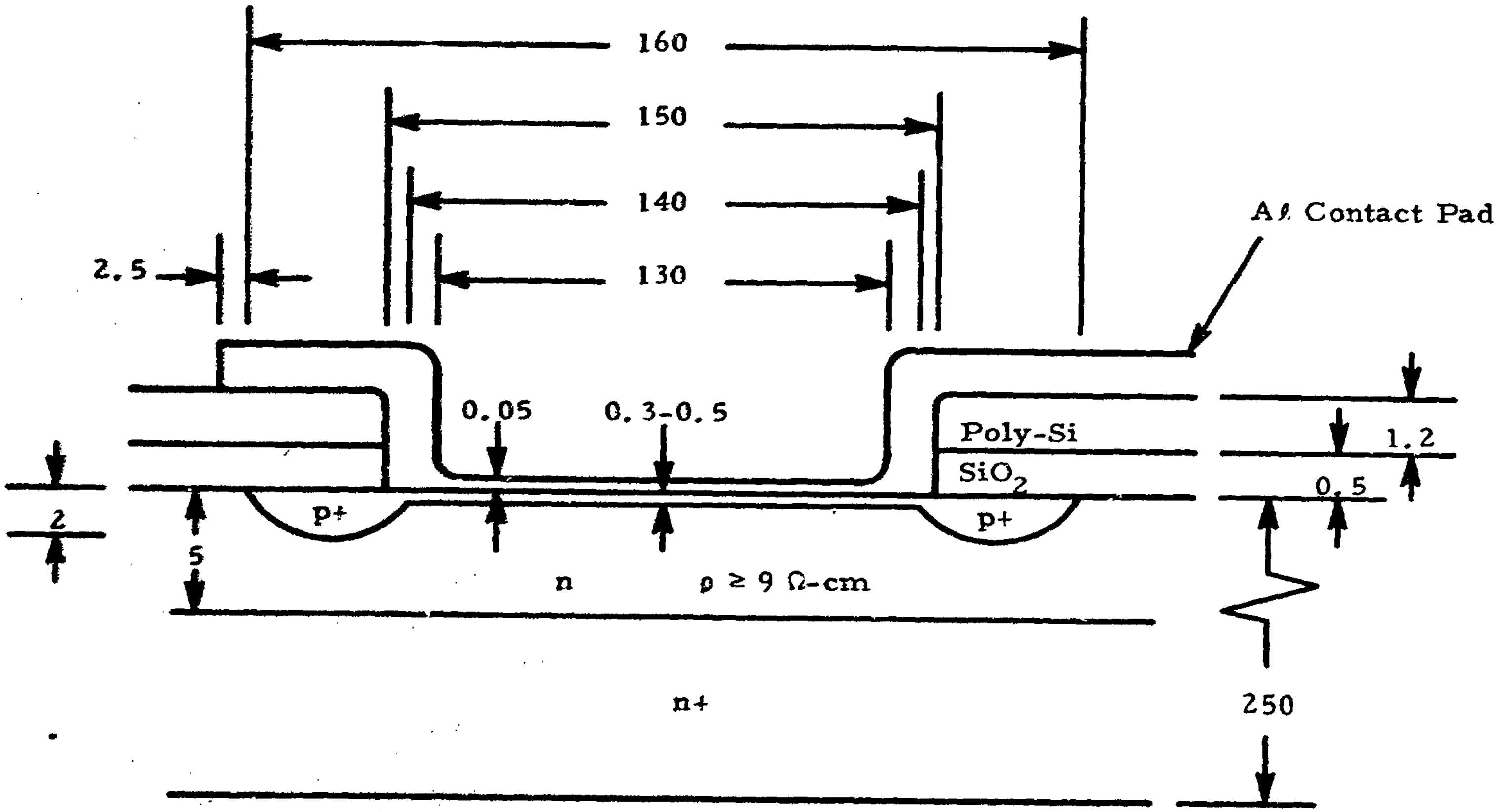


Figure 3.16a. Signal Processor Target. Diode cross-section at its center. (All dimensions in microns.)

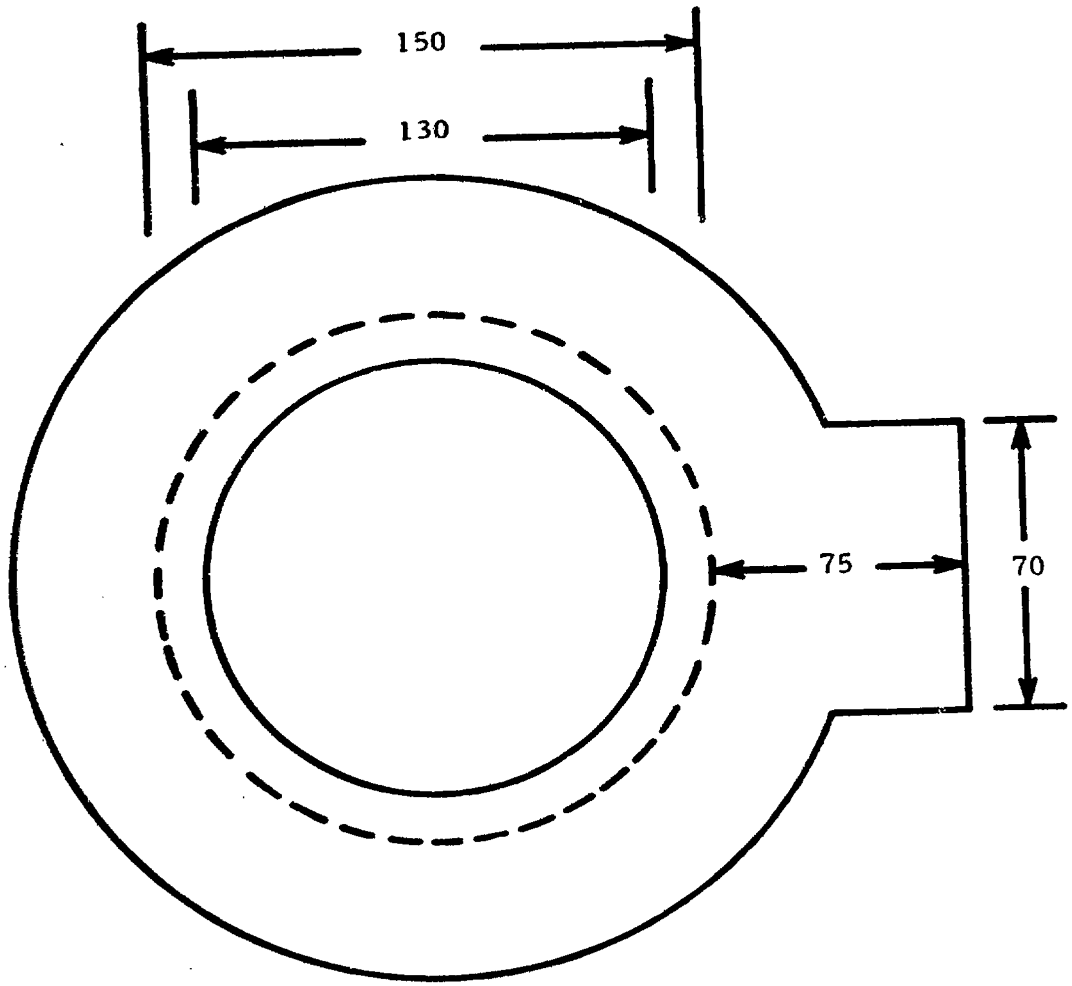


Figure 3.16b. Signal Processor Target. Top view of the p-side metal contact. (All dimensions in microns.)

The following steps were used in the fabrication of diodes:

1.	MATERIAL:	0.01 Ωcm, [111] Silicon, Sb doped, 2" diameter, 0.014 ±0.002" thick etch-polished
2.	EPI-GROWTH:	Resistivity: $10\ {}^{+2}_{-1}$ Ωcm Thickness: $5 \left\{ {+2 \atop -0} \right\} \mu$
3.	OXIDATION:	Thickness: 0.47 μ
4.	PHOTOTECH:	P ±Guard Ring
5.	P+ DIFFUSION:	Diborane deposition P ±diffusion Sheet resistivity: 15 ±2 Ω/□ Junction depth: 2 ±0.5 μ
6.	POLY SILICON DEPOSITION:	Deposit Poly Si. Silane $1.2 \left\{ {+0.2 \atop -0.1} \right\} \mu$
7.	SiO_2 DEPOSITION:	Deposit 0.4 ±0.1 μ Pyrolytic SiO_2
8.	PHOTOETCH:	Photoetch Poly Si for diffusion
9.	OXIDATION:	4700 Å
10.	PHOTOETCH:	P- diffusion window (Leave SiO_2 on poly silicon)
11.	P- DIFFUSION:	Sheet resistivity: 800 Ω/□ Junction depth: $0.3 \left\{ {+0.05 \atop -0.1} \right\} \mu$
12.	PHOTOETCH:	Contacts in SiO_2
13.	METAL DEPOSITION:	Deposit > 10,000 Å Al
14.	PHOTOETCH:	Etch thick metal pattern
15.	PHOTOETCH SiO_2:	Etch SiO_2 over poly silicon
16.	METAL DEPOSITION II:	Deposit 450 ±100 Å Al

17. PHOTOETCH: Etch thin metal pattern

18. ELECTRICAL TEST: Breakdown voltage and reverse current

19. BACK LAP: Remove oxide and diffused layers

20. DEPOSIT GOLD: Deposit 0.2 $\pm$0.05 μ Au on backside of wafer

21. SCRIBE AND BREAK

22. FINAL ELECTRICAL TEST: BV_R & I_R

Several methods were used for mounting the targets. Soldering directly to a gold-plated heat sink was unsuccessful. Bonding the diode on the heat sink using the gold-silicon eutectic resulted in cracked diode during the cooling cycle due to the large difference in the thermal conductivity of silicon and copper. Bonding on the heat sink using gold-tin preforms, however, resulted in well-bonded diodes. This configuration required a dc block on the target output when installed in the e-beam processor. Since dc blocks with sufficiently wide bandwidth were not available commercially, the above method of target mounting was discontinued.

The diode was then mounted on a gold plated 7 x 7 x .5 mm^3 BeO chip using gold silicon eutectic bond. The BeO chip was then soldered on the gold-plated heat sink in forming gas atmosphere. In this mount, the BeO chip together with two high frequency 100 pf ATC 100 capacitors provided the capacitive RF bypass for the power supply. The top connection to the diode was provided by making an ultrasonic aluminum bond from the target bonding pad to the center conductor of a copper-shielded 50 Ω coax cable which was mounted right next to the diode. This achieved coupling the output signal from the diode to a 50 Ω load with very little stray inductance or capacitance. Figure 3.17 shows the target circuit diagram as described above. In Figure 3.18 a photograph of a mounted target and heat sink is presented.

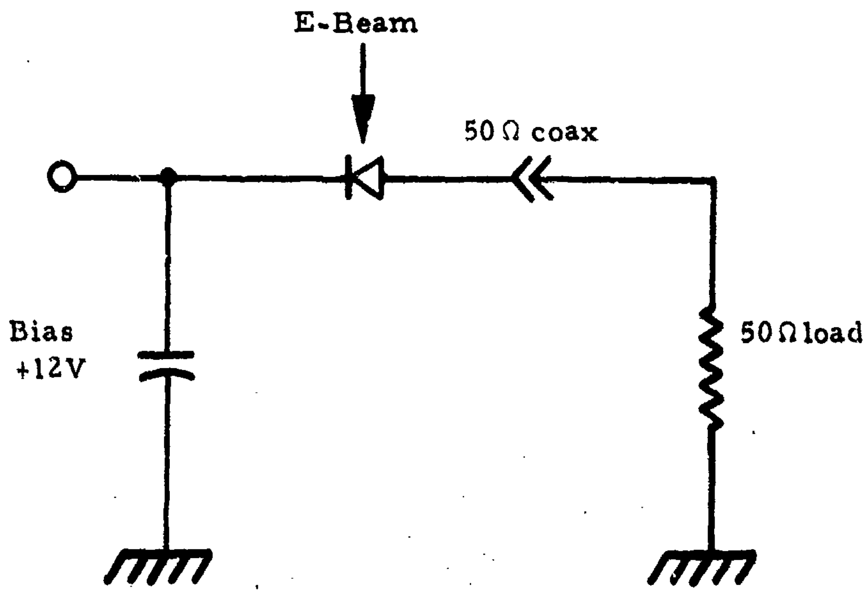


Figure 3.17. Target circuit diagram.

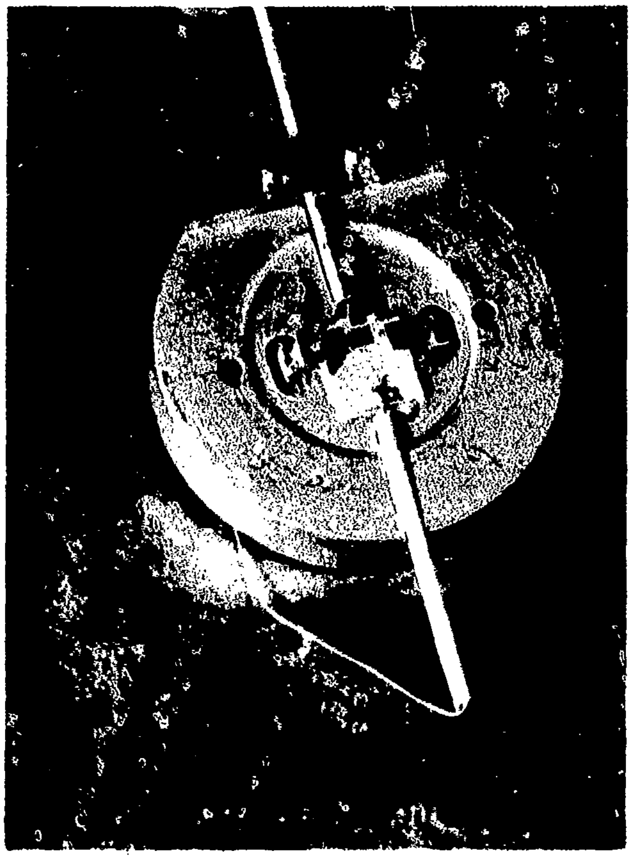


Figure 3.18. Target assembly and heat sink.

SECTION IV

SOLID-STATE PROCESSOR DESIGN

Our original solid-state processor design included a phase-locked-loop circuit in place of the oscillator shown in Figure 2. 3. The design was based on the assumption that all input data were synchronized with a 15.625 MHz (i. e., 1/64 ns clock rate, where the multiplexing period is 64 ns) clock driving the phase-locked-loop. The latter consisted of a phase detector, an active filter and a voltage controlled oscillator in line and a divide-by-8 ripple counter providing feedback from the oscillator to the phase detector. The VCO was tuned for oscillation at 125 MHz. However, if the input clock rate changed, the dc level at the active filter would change, which would in turn change the VCO output frequency. The phase-locked-loop circuit was therefore used to (1) provide an oscillator output phase-locked with the multiplexers outputs, and (2) achieve a versatile system that would automatically accomodate any small variation in the input data rate (i. e., the clock rate).

Results on a fabricated phase-locked loop circuit showed that the circuit responded to variations in clock rate in a time period much longer than the multiplexing period (for 128 data lines) of 64 ns. The slow response is mostly due to the high Q resonant circuit of the VCO. In addition, the deflection system uses high Q tuned circuits which are expected to have very slow transient response. Therefore, the second function of the phase-locked-loop circuit mentioned above could not be realized. The feedback loop also produced some jitter (mostly FM) in the oscillator output that was difficult to eliminate. Hence, the phase-locked-loop was replaced by an oscillator. Thus the solid state processor circuit includes a capacitively tunable oscillator, a divide-by-8 counter, and an 8-bit multiplexer. In the complete circuit, 16 multiplexers are necessary to drive the 16 address gates of the E-Beam Processor. In this program, however, only one multiplexer is used to demonstrate the dual-stage processing. The processor outputs are amplified by a set of amplifiers for coupling to the e-beam processor. The above components are described below.

4.1 OSCILLATOR AND MULTIPLEXER CIRCUIT

The solid state procesor performs the following basic functions; (1) generates the 125 MHz sinusoidal signal for conical beam deflection, (2) synchronously and binarily divides the sinusoidal signal by 8 and (3) multiplexes, 8 data input lines into 1-line to provide the address-gate drive signal.

The 125 MHz oscillator consists of an emitter coupled logic integrated circuit, MC1684L, with an L-C tunable tank circuit. The frequency of oscillations can be varied by varying the capacitance of the trim capacitor in parallel with the coil.

The output of the oscillator (125 MHz) is coupled to (a) a 50 Ω output (to be connected to the conical-beam rotation amplifier input) via a capacitively coupled narrow-band 1200 to 50 Ω Tee network impedance transformer, and (b) the divide-by-8-counter input circuit. The 1200 Ω load impedance is required at the output of the MC1648L oscillator.

The divide-by-8 synchronous binary counter consists of 3 MECL "D" flip flops, MC1034L, and a one-fourth MECL NOR Gate, MC1664L. The three output gates which provide the drive signals to the multiplexers include two 1/4 MC1664L gates and a 1/2 MC10110L gate. A schematic diagram of the oscillator and counter circuit is given in Figure 4.1.

The multiplexer is an 8-line to 1-line emitter-coupled logic, Fairchild ECUL 9581. With 2^3 input data lines, it requires 3 line-select inputs with binary word encoding. The divide-by-8 synchronous counter supplies the latter as a binary word generator. Because the counter is a synchronous unit, the multiplexer output is synchronized with respect to the oscillator output. This synchronization establishes a fixed phase/time relationship between the data arriving at each gate and the beam rotation and prevents any data from not being processed.

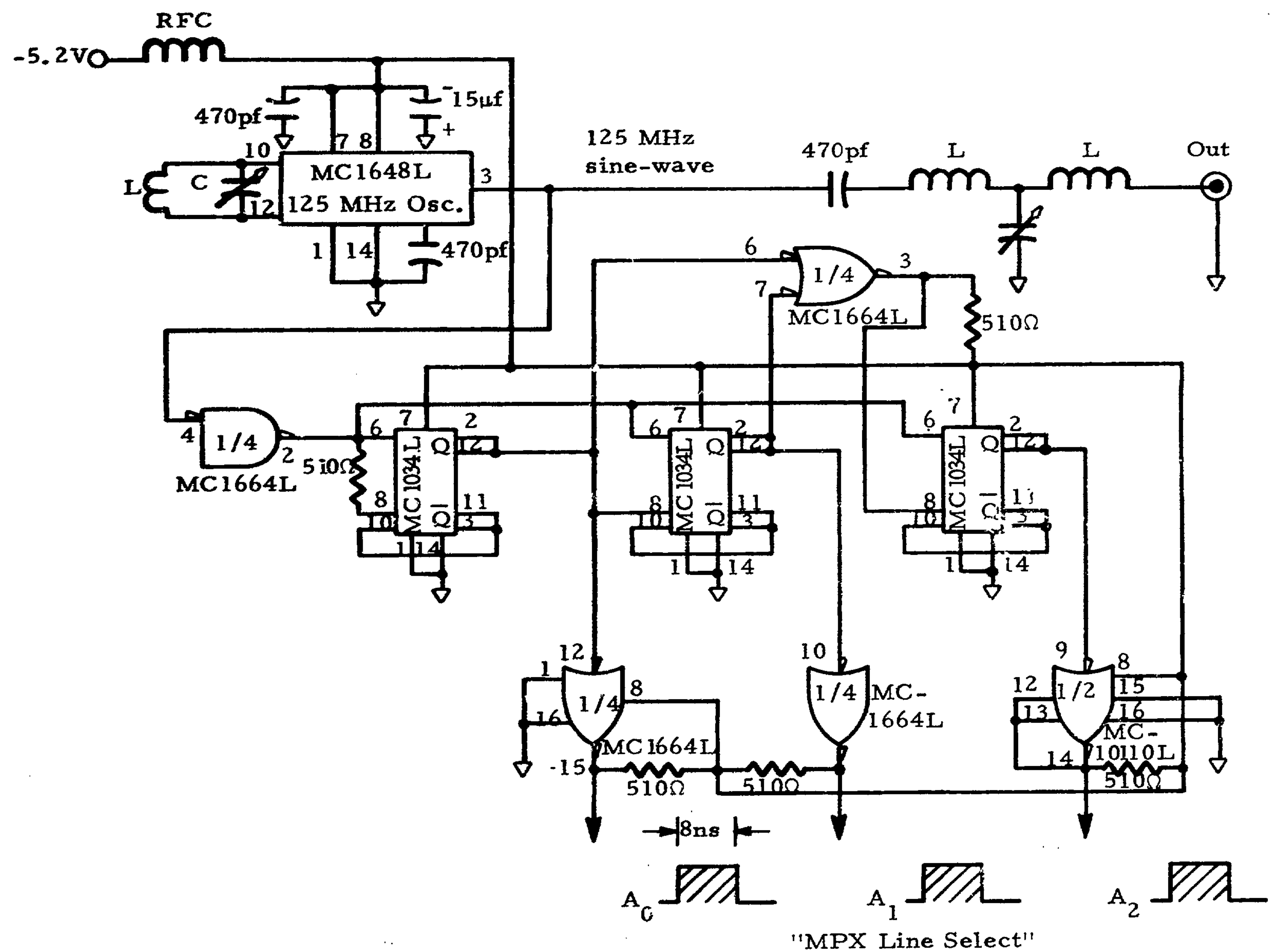


Figure 4.1. Solid state multiplexer circuit diagram.

The multiplexer output, PIN No. 6, should be connected to the input of the address-gate driver amplifier. For test purposes, the 8-line mpx inputs are provided by an ECL "D" flip-flop, MC1034L. Alternate inputs are connected to Q and $\overline{Q}$ respectively to demonstrate the system's multiplexing capability (Figure 4.2). This produces a continuous 1-0 bit pattern at the multiplexer output.

The power requirement for the circuit is -5.2V (±0.3V) at 500 mA. The circuit is provided with a dc input, and the oscillator and multiplexer outputs.

4.2 AMPLIFIERS

4.2.1 Conical Beam Rotation Amplifier

The amplifiers drive the horizontal and vertical deflection circuits of the conical beam rotation system. Two 50 Ω outputs are provided for the two deflection circuits and a single 50 Ω input connects to the output of the oscillator in the logic circuits. A maximum of 8W per output has been achieved at 125 MHz with about 180 mV peak from the oscillator. Higher output levels are possible with more input power.

The amplifiers are designed in two separate 50 Ω systems. The two-part design is done in order to facilitate attenuation and/or phase shifting of one output with respect to the other at low power levels. Thus, a phase shifter and a power attenuator may be used in between the two amplifiers to achieve the required functions. The phase shift and power attenuation are needed for adjusting the signal phase and amplitude at either the horizontal or vertical circuits of the conical beam rotation system. The signals arriving at the two circuits must have approximately 90° phase difference.

The first part consists of a three-stage Class A tuned transistor amplifier with a 50 Ω input line and two 50 Ω output lines. (If only one output is being used, the other should be terminated by 50 Ω). The maximum power level obtainable in the two outputs is 1.5W. The transistors are Motorola

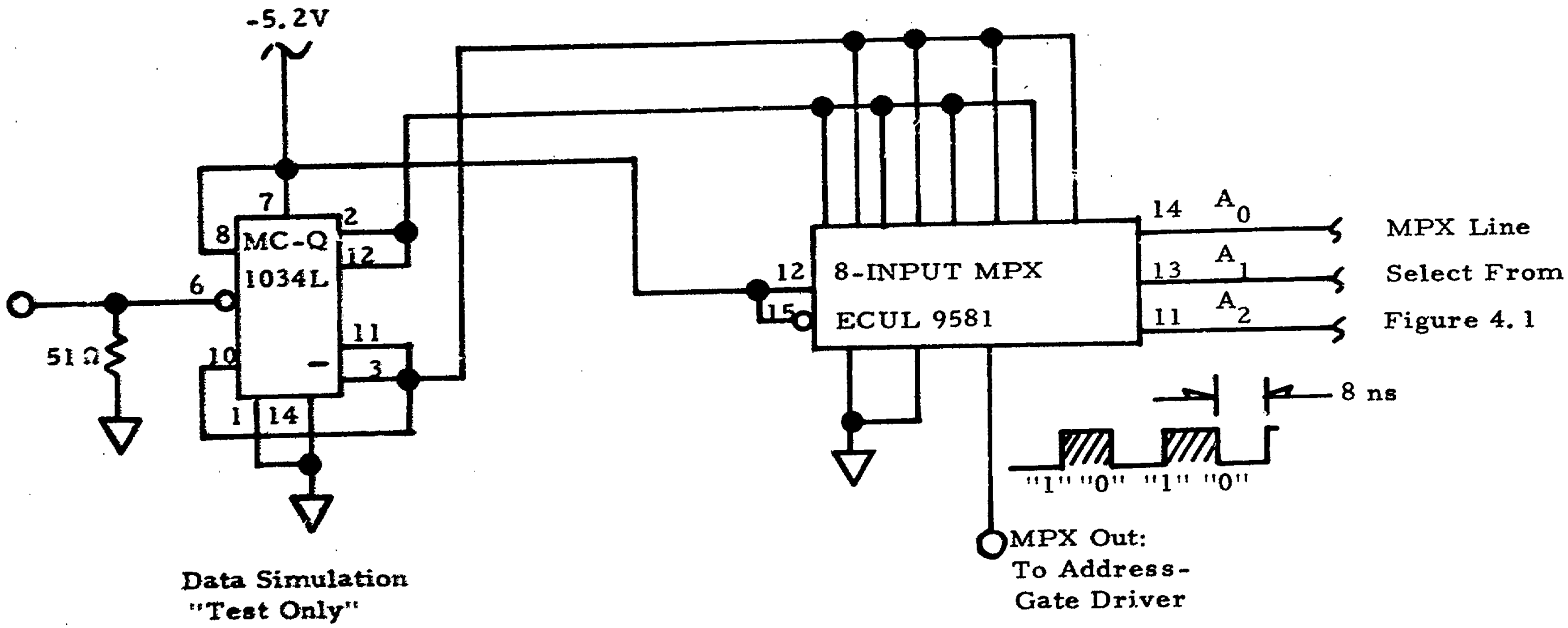


Figure 4.2. Solid State Multiplexer

2N3866, and the tuned input and output circuits for each transistor are designed on the basis of the following y-parameters supplied by the manufacturer for Class A operation at I_c = 80 mA, V_{ce} = 15V, where I_c and V_{ce} are the (dc operating point) collector current and voltage.

$$Y_{11} = 36 + j12 \qquad Y_{12} \simeq -j1.5$$
$$Y_{21} = 20 - j300 \qquad Y_{22} = 1.5 + j5 \qquad \text{mmohs}$$

The output circuit for each transistor is designed for 160 Ω (dynamic) load impedance. The schematic diagram of the amplifier and the component values are given in Figure 4.3.

The second amplifier is made of two single-stage Class C tuned transistor amplifiers, with each looking into a 50 Ω terminated load. The transistors are Motorola 2N5642, and the following input and output parameters (manufacturer's specifications) were used for design at 125 MHz.

$$C_{in} = 65 \text{ pF} \qquad R_{in} = 2.5\,\Omega$$
$$C_o = 46 \text{ pF} \qquad R_L = \frac{(V_{cc} - V_{sat})^2}{2P_o}$$

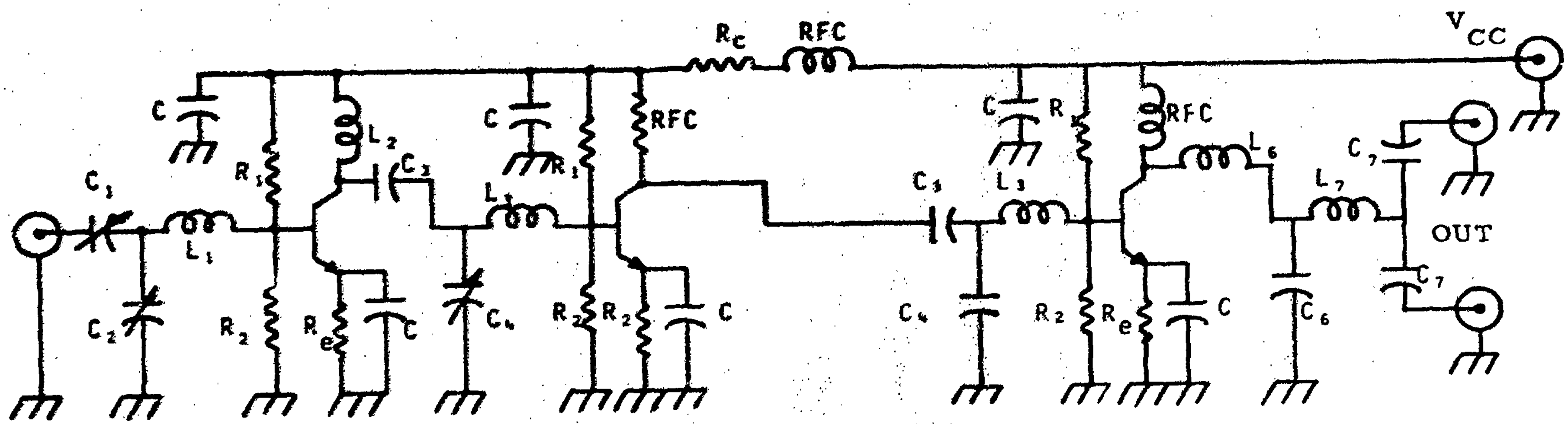
where, C_{in}, C_o = input and output capacitance

R_{in}, R_L = input and load resistance

The schematic diagram of the amplifiers is shown in Figure 4.4.

4.2.2 Deflection-Address-Gates Amplifier

This amplifier system drives the deflection-address-gates. The output impedance is therefore a parallel RC, where C is the gate capacitance, and R is the terminating resistor which is also used for charge leakage from the gate when the latter is bombarded by electrons. The requirement here is large gain, high output power and wide bandwidth. The output of the



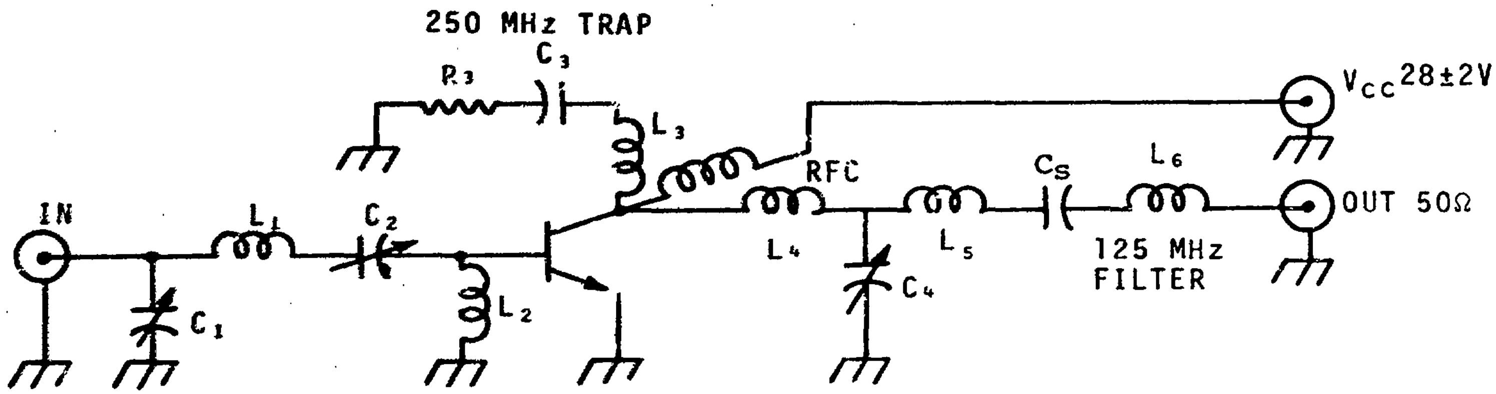
COMPONENTS	CALCULATED	AFTER BENCH TEST
C_1	5.5 pf	5.5-18
C_2	13 pf	5.5-18
L_1	0.1 uh	3 t
L_2	0.2 uh	5.6 t
L_3	.085 uh	2.5 t
C_3	7 pf	5.5-18
C_4	10.5 pf	1-20
L_6	.3 uh	9 t
L_7	.125	3.5 t
C_6	19 pf	5-30
C_7	.01 uf	.01 uf
C	{0.1 uf, 100 pf}	{.1 uf, 100 pf}

R_1 = 1.5 K
R_2 = 510 Ω
R_e = 51 Ω
RFC = 1 uh
R_c = 51 Ω
Transistor = Motorola 2N3866
V_{cc} = 17V
All inductors made from #19 insulated copper wire.
Each turn 1/4" I.D.

Figure 4.3. Three-Stage Class A Tuned Amplifier

ECL gate circuit is 0.6 - 0.8V, and the amplifier should amplify this to more than 25V in order to deflect the beam on or off the target. Furthermore, the amplifier should have sufficient pass-band to amplify an 8-ns pulse and a, say, 80-ns pulse to the same output level without too much pulse distortion. These requirements make inter-stage and load coupling difficult; AC capacitive coupling cannot be used and direct coupling is almost mandatory. Furthermore, the multiplexer output requires -1V dc level on the load termination. The amplifier input must therefore provide this dc level.

The design has been achieved by using a two-stage amplifier consisting of a Class A driver and a transistor switch output stage. The circuit diagram is shown in Figure 4.5. Care must be taken that the power supplies are turned on in the order V_3, V_2, V_1, respectively, in order to prevent damage to the transistors. Output pulse waveform can be adjusted by slowly varying V_1 or V_2. Also, V_1 should be more than 1.5V positive with respect to V_2. The voltage ranges are given below: V_3: 20-30V, V_2: -14 to -16V, V_1: -12 to -14V.



	COMPONENT VALUES	CALCULATED	IN CIRCUIT AFTER BENCH TEST
	C_1	125 PF	80 - 140
INPUT	C_2	156 PF	80 - 140
	L_1	22 nh	0.5 turn
	L_2	25 nh	1.5 turn
	C_3	5 PF	5 PF
	L_3	80 nh	3 turn
OUTPUT	R_3	100 Ω	100 Ω
	RFC	1.5 μh	1.5 μh
	C_4	18 PF	1-20
	C_5	15 PF	15 PF
	L_4	.14 μh	4.5 turns
	L_5	.25 μh	7 turns
	L_6	0.1 μh	3 turns

FIGURE 4.4. SINGLE-STAGE CLASS C TUNED AMPLIFIER

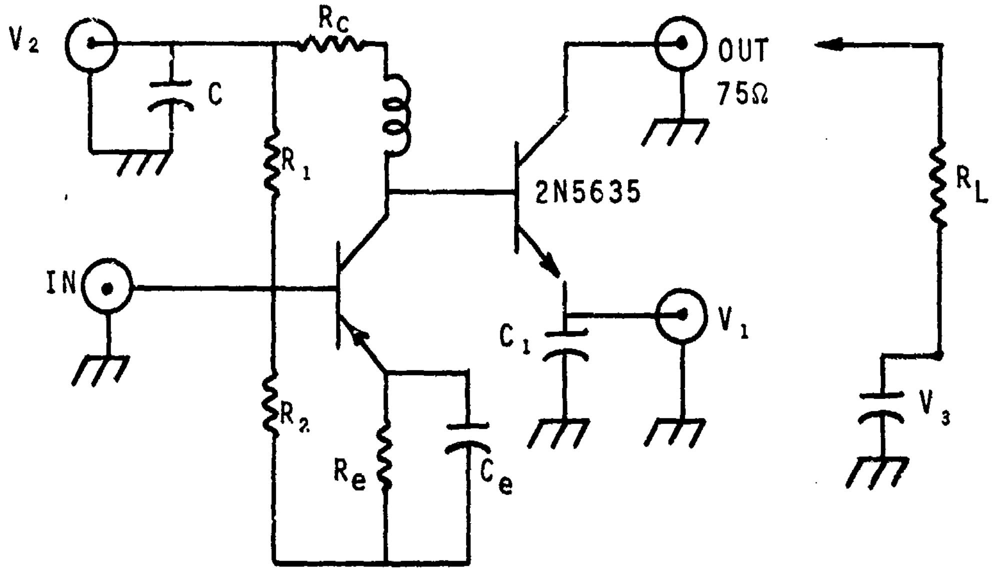


Figure 4.5. Deflection-address-gates amplifier.

COMPONENTS:

Transistors: Motorola 2N5583, 2N5635

R_1 = 2.1 KΩ, R_2 = 190 Ω, R_e = 10 Ω, R_c = 100 Ω

C_e = ATC 200 PF chip in parallel with 200 PF

C_1 = ATC 470 PF chip in parallel with 0.1 μF and 100 PF

C = 0.1 μF in parallel with 100 PF

SECTION V

RESULTS AND DISCUSSION

During the course of this work various experiments were done to check each component of the processor for proper operation. After the completion of the device, several tests were made for its evaluation.

Test results with the electron gun indicated that it provided sufficient electron current at 10 kV to produce the specified 20 mA target output current. Due to the rather long travel distance from the gun to the target, the beam spot at the target position was about 2 mm in diameter, as measured on a phosphot screen.

The realization of a satisfactory beam-rotation deflection system has been the major problem area. With the double pair of horizontal and vertical deflection systems a circular beam rotation pattern was achieved at the deflection-address gates. However, the pattern was elliptical after the beam exited the gates, as expected.

Conical beam rotation was produced by three pairs of deflection plates with each pair series resonated at 125 MHz. Some distortion in the rotation pattern could be observed at large deflection amplitudes due to the leakage fields at the end of the third pair of deflection plates (the electron beam exits the deflection system at the end of the third pair of plates). The distortion could also result from possible distortion at the amplifiers outputs at high power levels, or from an uncommon center of deflection.

The deflectron and deflection magnifier system generated a satisfactory conical rotation after the coupling between the two deflectron axes was tuned out. Precise resonating of the two axes was also critical in achieving circular rotation patterns. Again, some distortion in the pattern was observed when the amplifiers used in the deflectron circuits were over-driven. However, the amplifiers that were developed for this program provided enough power to obtain satisfactory conical rotation with sufficient amplitude for the beam to clear the deflection-address structure.

With the beam bent and focused on the target, a voltage of 25V or less on an address-gate was sufficient to deflect the beam off (or onto) the target. Some of the other results on the gate system were described in Section 3. 3.

Test results with the Einzel lens showed that with the beam at 10 keV, a potential of about -6. 5 to -8 kV was sufficient to bend the beam (emerging from the address-gates) onto the target. The actual voltage depended on the voltage setting on the funnel. However, due to lens aberration, the beam spot at the target in the absence of a funnel voltage was too large, indicating that a cross-over was formed in front of the target plane, as discussed in Section 3. 4. With the present lens design, the 20 mA target output current could not be achieved without the funnel.

The target pulse response was measured at various stages of the target development effort. The first set of targets fabricated were Si p^+-n diodes with no n^+ substrates. These diodes showed a series resistance of about 40 - 70 Ω, typically 50 Ω, and hence the diode pulse rise-time was about 0. 2 to 0. 25 ns. The series resistance resulted from the resistance of the n-layer and the contact resistance at the bottom of the chip. In addition, the poly-Si layer on the diodes was 0. 7 um and was not sufficiently thick to stop 10 keV electrons from penetrating into the oxide layer (see Figure 3. 16).

The next set of targets were p^+-n - n^+ diodes with a 1 to 1. 2 μm poly-Si protective layer and did not exhibit the 50 Ω series resistance. The pulse response of the diodes showed a 10-90% pulse rise-time of about 0. 15 ns. Furthermore, at a pulse-width of about 0. 3 ns, the pulse amplitude was still equal to the target dc output, indicating that the target had sufficient bandwidth to do better than 2 Gbit/sec processing.

The target pulse response was measured by sinusoidally deflecting a beam back and forth across the diode. The deflection amplitude was much larger than the beam width of about 3 mm. Consider sinusoidal deflection $y = Y \cdot \sin\omega t$, which for small y, becomes $y \simeq Y\,\omega t$. The beam is on the target a time period equal to the time it takes the beam to move one beam width. That is, $\Delta t = (2y_o/Y\omega) = (2y_o/Y)(T/\omega T)$, where $2y_o$ is the beam-width and T is the sine-wave period. For T = 8 ns, $2y_o = 0.3$ cm, and Y = 1 cm, $\Delta t = 0.38$ ns, i.e., target output pulse width is about 0.38 ns if the target has sufficient bandwidth to pass the pulse without broadening. Note that the pulse width can be changed by varying the deflection amplitude Y or the period T. Figure 5.1 shows a typical target response. Target life under 10 keV electron bombardment varied from diode to diode. This was traced to a misalignment in the diodes processing masks which had occurred at the step-and-repeat point of the processing cycle. Consequently, in some diodes the SiO_2 layer was exposed whereas in some it was not. A new set of masks is therefore necessary to fabricate diodes which do not degrade in an e-beam environment. (Sufficient funds and time were not available in the program to fabricate new masks.)

Figure 5.2 shows the completed e-beam signal processor with the target flange not mounted. The tube has three "o" ring flanges which permit the removal of the gun, the deflection-address gates, and the target assembly. On the target plate, the target assembly could be removed and a phosphor screen inserted in place of it. Beam alignment and proper conical beam rotation could thus be checked on the phosphor screen.

To test the completed e-beam processor, the phosphor screen was used to align the beam, produce conical beam rotation, and focus the beam onto the target position after it exited the address-gates structure. The voltages on the various components of the processor and the RF frequency on the deflectron were recorded. The phosphor screen was then replaced by the target

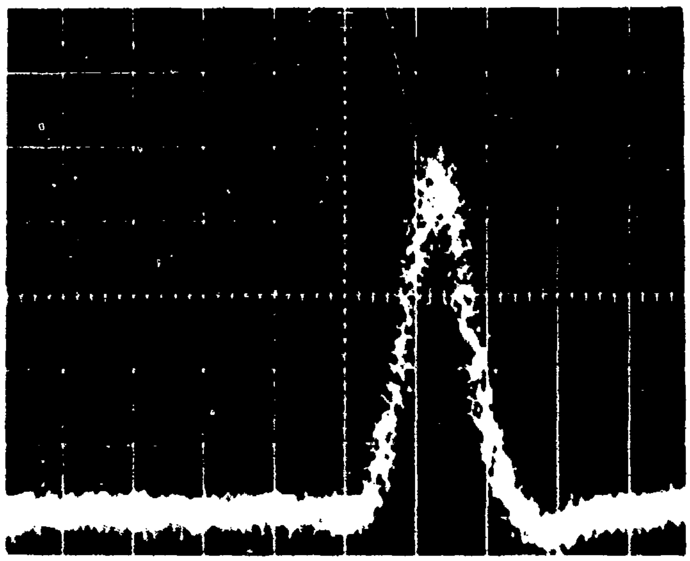


Figure 5.1. Signal Processor target pulse response. Horizontal 0.2 ns/div, vertical 10 mV/div. Sampling scope rise-time: 25 ps.

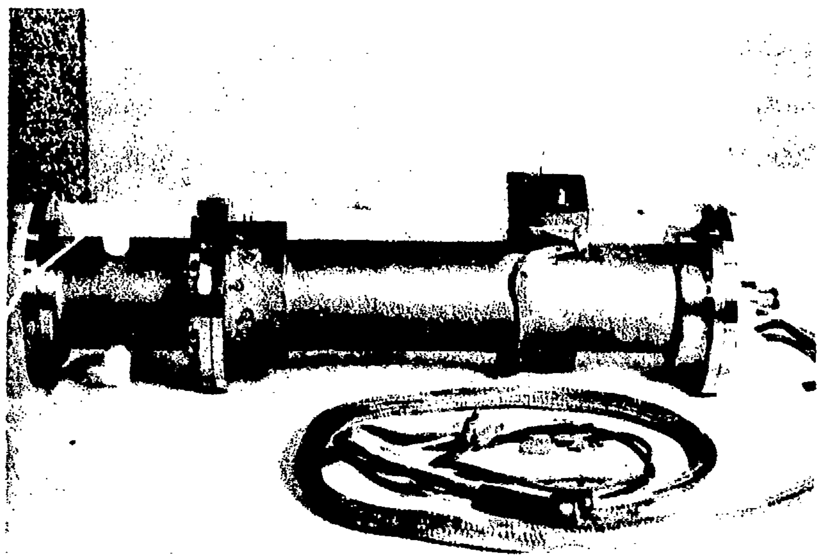


Figure 5.2. Signal Processor tube built at Warnecke. Target flange is not mounted.

and an output was obtained at those pre-recorded voltages and frequency. The maximum pulse amplitude achieved was 1V, and the minimum pulse width was 0.5 ns. Pulse rise-time was in the range 0.25 - 0.4 ns. This long rise-time compared to 0.15 ns measured for the target may be due to (1) the beam spot being too large at the address-gates, (2) fringing fields on the address-gates which have the effect of increasing the beam rise-time. Gate-to-gate coupling could also produce a long output rise-time, but since the coupling has been greatly reduced by putting a grounded fin between two adjacent gates, coupling is not expected to contribute to the long rise-time problem. The Einzel lens and the funnel voltages to produce 1V output were at -7 and -6 kV, respectively.

Not all the gates could produce an output signal; the variation of the voltage on some gates did not change the output state (1 or 0). There are only two possible explanations: either the beam did not clear those gates or the target was off center. The latter was more likely, though a small variation on the phase or amplitude of the deflectron input signals could change the beam circular pattern at the address-gates structure. The difficulty was that neither the beam alignment (with respect to the target) nor the conical rotation could be checked.

In order to be able to do the above check-out, a new target plate with a built-in glass phosphor screen was designed. The plate would have a phosphor screen ring around the target heat sink that would allow seeing the circular beam rotation pattern with the funnel voltage set at zero. Fabrication of the structure, however, has not been completed because some difficulties were encountered in making a glass-to-metal seal on the two edges of the glass ring.

The interfacing of the solid state processor and the e-beam processor has been achieved smoothly. The power delivered by the deflection-system amplifiers was more than sufficient to generate the desired conical beam rotation. Up to 18W in two outputs was achieved at 125 MHz. Also, the output signal from the address-gates amplifier was large enough to deflect the beam on or off the target. In addition, the amplifier output waveform, measured on a sampling scope, did not change appreciably when the amplifier output was connected to an address-gate (in parallel with a terminating resistor which was the scope 50 Ω input impedance).

Figure 5.3a shows the multiplexer output 1-0 waveform pattern. This signal, amplified by the address-gate amplifier, is shown in Figure 5.3b. The load in Figure 5.3b is the parallel combination of a 50 Ω terminating resistor and a 5 pf capacitor simulating an address-gate capacitance. By changing the amplifier output impedance to 75 Ω, up to 30V of signal has been achieved. The higher impedance was used in order to reduce power dissipation.

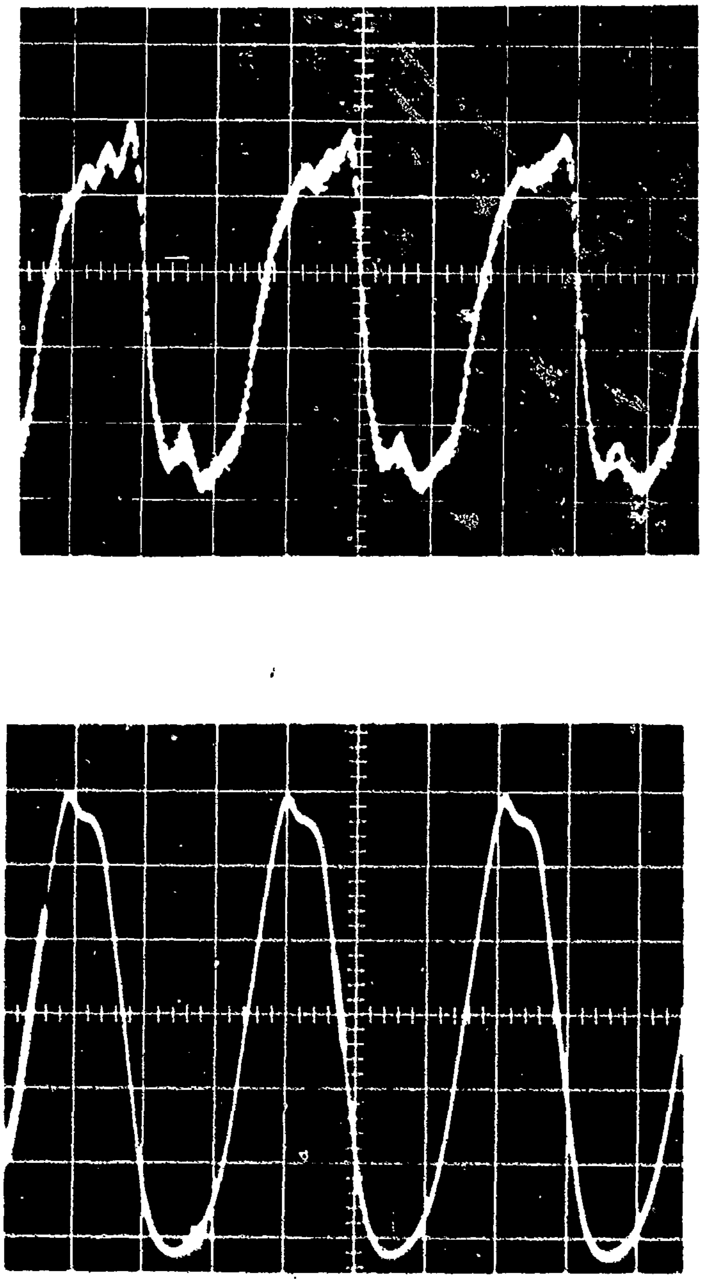


Figure 5.3. (a) Multiplexer output 1-0 pattern. Horizontal 5 ns/div. Vertical 200 mV/div.

(b) Signal in (a) amplified by address-gates amplifier. Horizontal 5 ns/div. Vertical 4V/div.

SECTION VI

CONCLUSIONS AND FUTURE EFFORTS

A dual stage signal processor system has been developed which has the potential for achieving output data rates exceeding 2 Gbit/sec. The system consists of an EBS signal processor driven by a solid state stage. It is shown that the latter may be fabricated from commercially available high speed integrated circuit chips and can be efficiently interfaced with the EBS processor stage.

The solid state processor would multiplex 128 input data lines into 16 lines using 16 multiplexer sections. Multiplexing of 64 ns input data pulses into 8 ns pulses was demonstrated by fabricating one multiplexer section. The EBS processor multiplexes 8 ns data pulses from 16 lines into a single output with 2 Gbit/sec data rate. Output pulse amplitude of one volt into 50 Ω load and pulse width of 0.5 ns has been achieved.

The EBS processor includes an electron gun, a deflection system which launches the beam into conical rotation, an address-gate structure for putting information on the beam, an Einzel lens and an electrostatic funnel which bend and focus the beam onto the target, and a Si p-n junction target. The major problem area in the development of the processor has been the realization of conical beam rotation. The latter was achieved by a deflectron and deflection mangifier system and also by a set of three pairs of electrostatic deflection plates. However, the two systems are not optimized and further work is needed in this area.

Unfortunately the duration and scope of the program effort has been too limited to allow the optimization of the processor system. For example, the signal processor output pulse rise-time is not satisfactory. Although a target rise-time of 0.15 ns was demonstrated, the processor output rise-time achieved has been 0.25 ns or higher. In addition, the random switching of only some, but not all, of the 16 gates of the EBS processor could be demonstrated. These problems can be solved by incorporating the improvements discussed below. Furthermore, the additional effort should significantly upgrade the signal processor performance and result in an optimal design.

a) The deflection system, although presently satisfactory, should be simplified. It is especially desirable to remove the deflection magnifier. This will permit the electron beam to reach the target position along the center axis of the processor tube when the deflection system has no RF input. In this manner the alignment of the target and the electron beam along the center axis can be checked and corrected. In addition, one input voltage port to the tube will be eliminated. With the removal of the deflection magnifier, however, a higher deflection sensitivity must be obtained. The latter can be achieved by designing a longer deflectron or using an optimal system of electrostatic deflection plates, and by post acceleration, i.e., generate conical rotation at a low beam voltage, say, 2-4 kV, and then post accelerate to 10 kV at the deflection-address gates. Note that a post acceleration just in front of the gate system may be designed to bend the beam to a direction parallel to the center axis. This would considerably simplify the construction of the gate structure.

b) In order to reduce the processor output pulse rise-time, the beam spot size at the address-gates must be reduced and the gate structure should be redesigned. The fringing fields on the gate can result in an appreciable broadening of the pulse rise-time. A profile of the electric field lines on each gate should be plotted to determine the extent of the fringing fields spread and arrive at an optimal gate design that can achieve less than 0.1 ns beam pulse rise-time at the target. It is also desirable to have the electron beam enter the gate structure parallel to the tube axis rather than in an angle. This would not only simplify the gate structure fabrication, but would also reduce the aberration problems at the Einzel lens. As explained in a) above, bending the beam to parallel the center axis may be achieved by post acceleration.

c) The spherical aberration on the refocusing Einzel lens needs to be reduced. Spherical aberration produces a cross-over in front of the target plane and hence a single spot will not be formed at the target. This could contribute to not being able to switch all the gates as mentioned above. Theoretical results of El-Karch and Sturan[2, 3] may be used for lens design optimization. Better results may also be obtained by putting a second lens in front of the electrostatic funnel.

d) A double pair of horizontal and vertical electrostatic deflection plates may be used just in front of the funnel to eliminate the target alignment problem. The electron beam is bent by the Einzel lens and goes through these deflection plates before it reaches the target plane. By varying the voltages on the plates, the beam position can be changed until it coincides with the target. Hence, switching of all the gates can be insured.

e) A new set of targets with new processing masks should be fabricated to insure target long life under e-beam bombardment. Furthermore, it is not at all clear if the present design requirements are optimal for driving a PIN diode at rates of ~2 Gbit/sec. Neither the 5 GHz bandwidth nor the 0.1 ns rise-time specified in the contract goals are necessary requirements for 2 Gbit/sec signal processing. A significant improvement in the output signal amplitude (by almost a factor of 3) can be achieved by designing the target for 3 GHz bandwidth. This will increase the actual measured target rise-time to 0.2 ns, but the rise-time to the one volt (or 20 mA) level will be less than 0.1 ns. In addition, the dynamic impedance of the PIN diode modulator is not known, and the 50 Ω output impedance requirement is not essential. The ultimate optimal system is to fabricate the EBS target and the PIN diode on the same silicon chip so that the two devices are in close proximity and the coupling of the signal from the target to the PIN diode can be achieved most efficiently. In this case, a computer analysis of circuit model presentation of the PIN diode should be made so that an optimal EBS target may be designed. With the above arrangement, a waveguide must be built into the signal processor target assembly.

f) The construction of the e-beam processor may be considerably simplified by reducing the number of gates from 16 to 8. The beam deflection amplitude will be reduced by half and this will significantly improve device performance. Because of the smaller deflection radius, the Einzel lens will be smaller and the aberration problems can be to a large extent eliminated. In addition, less beam defocusing will occur and a higher beam current density (and hence output) may be realized at the target. The only draw-back may be the solid-state processor design. The rotation frequency will be 250 MHz and the solid-state processor must be capable of 250 Mbit/sec data rate. Since we have already realized a 125 Mbit/sec system, the development of the 250 Mbit/sec system, though costly, seems quite feasible.

Finally, the intended application of the EBS processor in this program is driving a PIN diode modulator in millimeter-wave communication systems. This application needs to be demonstrated with an experimental wave-guide system using a 2 Gbit/sec PIN diode switch for biphase phase shift keying.

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APPENDIX I

CONICAL BEAM-ROTATION BY ELECTROSTATIC DEFLECTION PLATES

Consider two pairs of horizontal and vertical deflection plates used to deflect a constant velocity beam in a field free region, as shown in Figure I-1. Beam deflection amplitudes at $z = L$ from the end of the vertical plates are

$$y(L) = \frac{V_y \cdot b\,(L + \frac{b}{2})}{2\,V_B\,a} \qquad (1)$$

$$x(L) = \frac{V_x \cdot b \cdot (L - \frac{b}{2} - d)}{2\,V_B \cdot a} \qquad (2)$$

where V_B is the beam voltage, V_y and V_x are signal amplitudes on the deflection plates, and the other dimensions are shown in Figure I-1. In order to obtain a circular pattern at $z = L$, we put $V_y = V_1 \sin\omega t$, $V_x = V_2 \cos\omega t'$, where t' is the time measured in the horizontal deflection plates coordinates; that is $t' = t - \tau$, where τ is the electron transit time for a travel from the beginning of the vertical plates to the beginning of the horizontal plates.

In general, the beam traces an alliptical pattern at a plane located at $z = L$. This should be clear since the beam travel distance to the plane $z = L$ is longer for the vertical plates than the corresponding distance for the horizontal plates. To correct for this difference, V_1 may be reduced with respect to V_2. That is, a circular pattern is obtained at $z = L$ if from Eqs. (1) and (2),

$$V_1\,(L + \frac{b}{2}) = V_2\,(L - \frac{b}{2} - d) \qquad (3)$$

However, the pattern is elliptical in any other plan $z \neq L$. The difficulty is that a common center of deflection does not exist for the two axes.

Now consider three pairs of deflection plates, a vertical-horizontal-vertical system, as shown in Figure I-1. By proper design, it is possible to make

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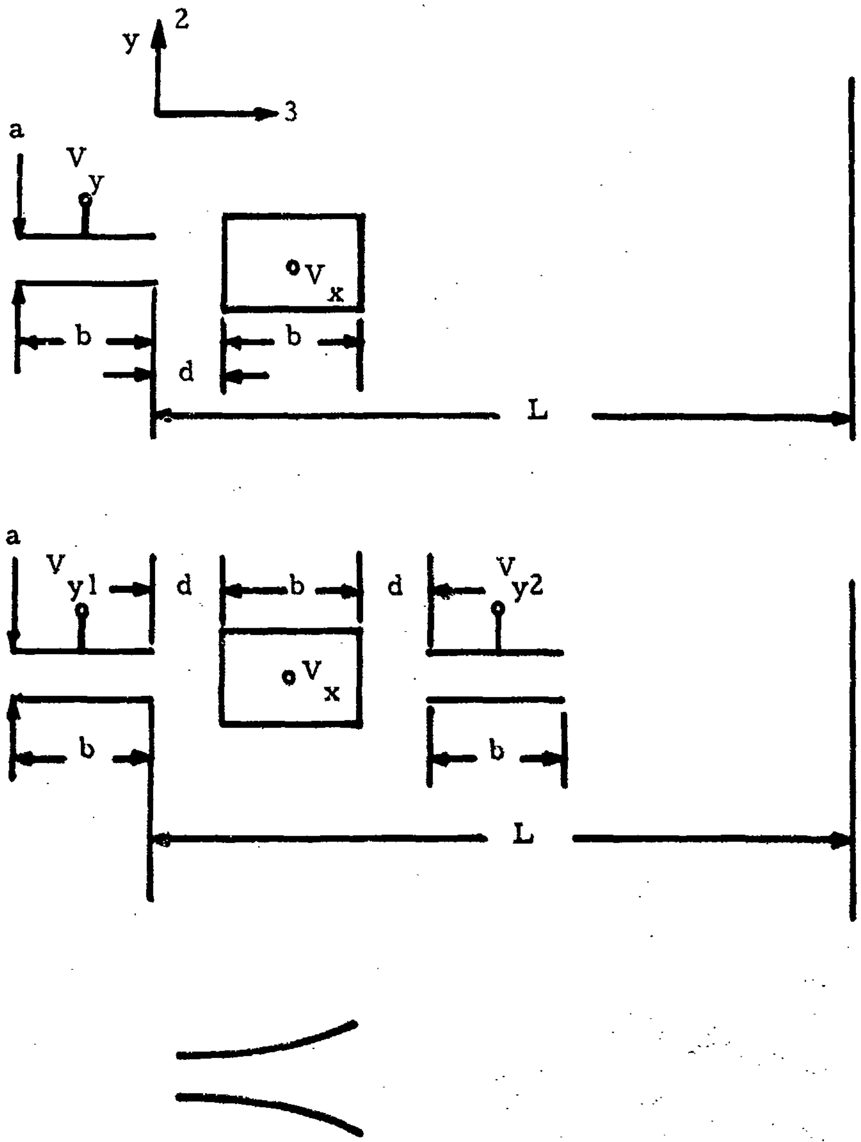

(a)

(b)

(c)

Figure I-1. Electrostatic deflection plates.
(a) A double pair of vertical and horizontal deflection plates.
(b) A deflection system for generating conical beam rotation.
(c) Bell-shaped deflection plates used to minimize fringing field effects.

the center for vertical deflection coincide with that for horizontal deflection. The amplitudes at $z = L$ are

$$x(L) = \frac{V_x \cdot b \cdot (L - \frac{b}{2} - d)}{2\, V_B \cdot a} \tag{4}$$

$$y(L) = \frac{V_{y1} \cdot b \cdot (L + \frac{b}{2})}{2\, V_B \cdot a} + \frac{V_{y2} \cdot b \cdot (L - \frac{3b}{2} - 2d)}{2\, V_B \cdot a} \tag{5}$$

Again, we set the voltages as,

$$\begin{aligned} V_{y1} &= V_1 \sin\omega t \\ V_x &= V \cos\omega t' \qquad t' = t - \tau \\ V_{y2} &= V_1 \sin\omega t'' \qquad t'' = t - 2\tau \end{aligned} \tag{6}$$

and Eq. (5) for maximum beam deflection amplitude becomes

$$y_{max}(L) = \frac{b \cdot V_1 \left[2L - b - 2d\right]}{2\, V_B \cdot a} \tag{7}$$

If we now set $V_1 = V/2$, we find $x_{max}(L) = y_{max}(L)$ for all L and $x(L)^2 + y(L)^2 =$ constant. That is, the beam rotates conically about the z-axis.

There are other solutions for Eqs. (4) - (6) which also result in conical rotation. For example, one may have $V_1 = V$ and $a_x = \frac{1}{2} a_{y1} = \frac{1}{2} a_{y2}$, where a_x is the gap between a pair of horizontal plates, etc.

To reduce the fringing field effects on the deflection plates, they may be shaped as in Figure I-1. This form was used in our experiment.

APPENDIX II

TARGET COOLING

Figure II-1 shows a schematic of target cooling arrangement. When an electron beam of power density 50 mA/cm^2 x 10 kV impinges on the silicon chip, the power must dissipate at best within a few micrometers of the chip surface. This heat conducts through the diode and then disperses through the copper base block.

It is desired that the maximum temperature of the chip should be 150°C or lower. The major temperature drops from the top of the chip to the ambient forced-flow air and may be estimated as follows.

The heat generated by the dissipation of electron kinetic energy is

$$Q_A = 10 \text{ mA} \times 10 \text{ kV} = 0.1 \text{ watt}$$

The junction dissipation is

$$Q_B = 20 \text{ mA} \times 10\text{V} = 0.2 \text{ watt}$$

and the power per unit area with a 2.2×10^{-4} cm^2 junction area is

$$q = 0.3/2.2 \times 10^{-4} \approx 1400 \text{ watts/cm}^2$$

If the chip thickness δ is 200 μm

$$T_1 - T_2 = \frac{q\delta}{k} = \frac{1400 \times 2 \times 10^{-2}}{1.45} \approx 19^\circ\text{C}$$

Here, the thermal conductivity of 1.45 watts/cm - $^\circ$C for silicon is used.

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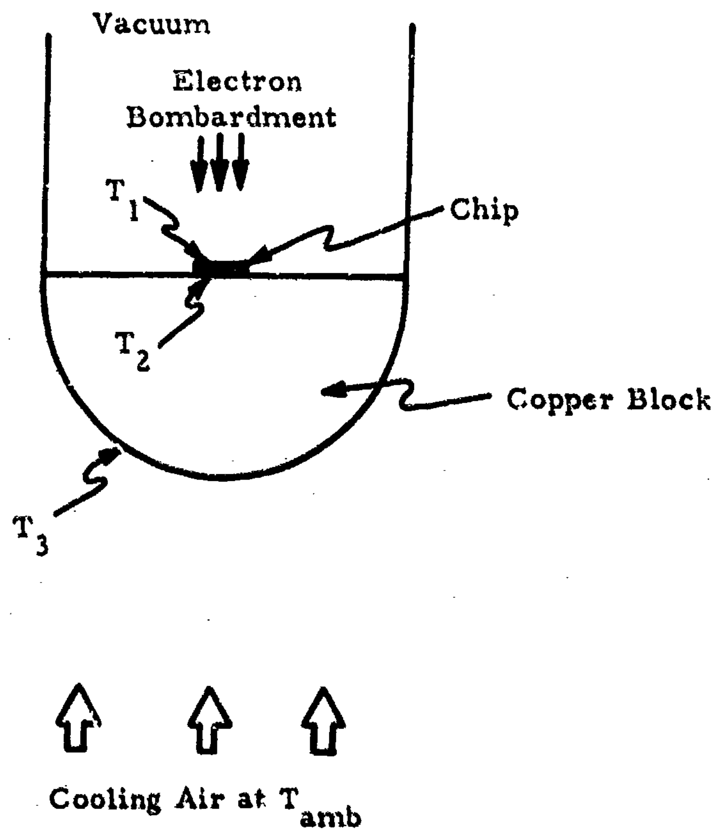

Figure II-1. Schematic of a target structure for thermal analysis.

Assuming a hemispherical copper block of 1.5 cm radius under the chip, one can estimate the temperature drop from the chip-copper junction to the outer surface of the hemisphere to be

$$(T_2 - T_3) = \frac{Q_o\,(b - a)}{2\,\pi\,k_{Cu}\,ab} \approx 8^{\circ}C$$

where a = inner radius of the hemisphere assumed to be 0.25 mm,

b = outer radius of the hemisphere, 1.5 cm

Q_o = total heat into the inner hemisphere which is about 1 watt for 0.5 mm dia. beam,

k_{Cu} = copper thermal conductivity, 4 watts/cm$^{\circ}$C.

The temperature drop from the copper surface to the cooling air is

$$T_3 - T_{amb} = \frac{Q_o}{\pi D^2/2} \quad \frac{1}{h_{air}} = 7^{\circ}C$$

where $h_{air} \approx 10^{-2} \dfrac{\text{watts}}{\text{cm}^2\ {}^{\circ}\text{C}}$ is assumed for air at moderate cooling speeds.

Thus the total drop is

$$T_1 - T_{amb} = 19^{\circ}C + 8^{\circ}C + 7^{\circ}C \approx 34^{\circ}C.$$

If 30°C ambient air is assumed, T_1 becomes about 64°C.

The analysis above indicates that a copper base block of 3 cm diameter with ambient air at moderate speed would be sufficient to cool the target below 150°C.

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13. ABSTRACT

The significance of this research and development to the Air Force is that a dual stage signal processor system has been developed which has a potential capability of achieving output data rates exceeding 2 Gbit/sec. The design is realized by a state-of-the-art solid state stage and an Electron-Beam-Semiconductor signal processor assembled in series. The former is fabricated from commercially available IC logic chips and has been efficiently interfaced with the EBS processor. The solid state processor multiplexes 64 ns input data pulses into 8 ns pulses to drive the EBS signal processor. The latter multiplexes 8 ns data pulses from 16 input lines into a single output. In this approach, information is placed on the electron beam and read out at the semiconductor target. Output pulse amplitude of one volt into 50 Ω and a pulse width of 0.5 ns has been achieved.

14. KEY WORDS	LINK A		LINK B		LINK C	
	ROLE	WT	ROLE	WT	ROLE	WT
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PN Junction						
Electron Optics						
Data Processor						
Multiplexer						
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