

UNCLASSIFIED

AD NUMBER
AD913326
NEW LIMITATION CHANGE
TO Approved for public release, distribution unlimited
FROM Distribution authorized to U.S. Gov't. agencies only; Test and Evaluation; APR 1973. Other requests shall be referred to Air Force Avionics Lab., AFSC, Wright-Patterson AFB, OH 45433.
AUTHORITY
WRDC ltr, 2 Jul 1990

THIS PAGE IS UNCLASSIFIED

AFAL-TR-73-155

AD913326

A STUDY OF THE APPLICATION OF REFLECTIVE DISPLAYS TO SYNTHETIC ARRAY RADAR

M. N. Ernstoff
R. N. Winner
Hughes Aircraft Company

TECHNICAL REPORT AFAL-TR-73-155

AUGUST 1973



Distribution limited to U.S. Government agencies only; test and evaluation; April 1973. Other requests for this document must be referred to AFAL/NVT, Wright-Patterson AFB, Ohio.

Air Force Avionics Laboratory
Air Force Systems Command
Wright-Patterson Air Force Base, Ohio

DDC
REFORMED
SEP 26 1973
RECEIVED
B

NOTICE

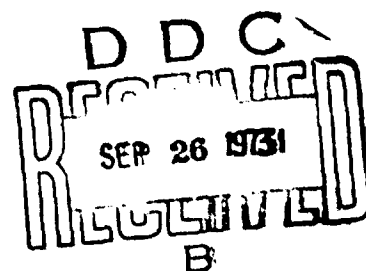
When Government drawings, specifications, or other data are used for any purpose other than in connection with a definitely related Government procurement operation, the United States Government thereby incurs no responsibility nor any obligation whatsoever; and the fact that the government may have formulated, furnished, or in any way supplied the said drawings, specifications, or other data, is not to be regarded by implication or otherwise as in any manner licensing the holder or any other person or corporation, or conveying any rights or permission to manufacture, use, or sell any patented invention that may in any way be related thereto.

Copies of this report should not be returned unless return is required by security considerations, contractual obligations, or notice on a specific document.

AD 913 326

A STUDY OF THE APPLICATION OF REFLECTIVE DISPLAYS TO SYNTHETIC ARRAY RADAR

M. N. Ernstoff
R. N. Winner



Distribution limited to U. S. Government agencies only; test and evaluation; April 1973. Other requests for this document must be referred to AFAL/NVT, Wright-Patterson AFB, Ohio.

FOREWORD

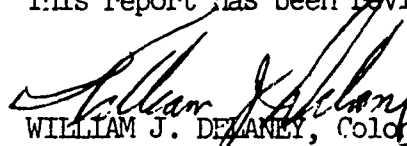
This study program has been supported by the Avionics Laboratory of the United States Air Force Systems Command, Research and Technology Division, Wright-Patterson Air Force Base, Dayton, Ohio 45433.

This effort was performed under contract by the Display Systems Laboratory, Equipment Engineering Divisions, Aerospace Group of the Hughes Aircraft Company. This report was submitted during April 1973 and covers work accomplished in the one year period beginning April 1, 1972, under Project No. 7662, Contract Number F33615-72-C-1415. The program monitor has been Mr. A.S. Jahren, (AFAL/NVT).

The authors are personally grateful to Dr. Alex M. Leupp, Mr. Lawrence A. Hendrix, and Dr. J. David Margerum of Hughes Aircraft Company for their contributions; and to Ms. Charlotte Evans and Ms. Anita Stoudt for their assistance in the preparation of this report.

This report contains no classified information.

This report has been reviewed and is approved for publication.


WILLIAM J. DELANEY, Colonel, USAF
Chief, Navigation and
Weapon Delivery Division

ABSTRACT

The purpose of this study was to establish the performance requirements for an airborne synthetic-array-radar (SAR) display and investigate the feasibility of meeting these requirements with a reflective display mechanization. A reflective liquid crystal display was chosen as the baseline mechanization to be evaluated with respect to its operational performance, fabrication feasibility and cost effectiveness.

A set of performance requirements were established from psychophysical considerations that would provide for the transfer of the maximum amount of information that can be realistically used in the named application. They are: size, 10 by 10 inches; resolution, 1024 by 1024 pixels; contrast ratio, 64 to 1 under 10,000 ft. C. ambient (13 shades of gray); reflectance, 20 percent of lambertian surface.

The baseline liquid crystal display is fabricated by sandwiching a thin layer of liquid crystal material between a transparent planer conductive electrode and a large semiconductor wafer. Prior to assembly, an X-Y addressed matrix array of transistor-controlled reflective-electrodes is formed in and on the surface of the semiconductor wafer. An image is formed on the display by programming the brightness of each picture element in an appropriate manner. Picture element brightness is dependent upon the reflective characteristics of the dynamic scattering liquid crystal material in contact with the elemental electrode and the ambient illumination.

A SAR display system mechanization is recommended that is built around the capabilities of a reflective liquid crystal pictorial display. Such a system could present high-resolution synthetic-array radar on board an aircraft in real-time with improved performance and decreased complexity over systems that utilize CRTs.

CONTENTS

1.0 INTRODUCTION. 1

1.1 General 1

1.2 Purpose and Scope 1

1.3 Background 2

1.4 Accomplishments 3

1.4.1 Requirements 3

1.4.2 Feasibility 4

1.4.3 Recommendations 4

2.0 REQUIREMENTS 7

2.1 Resolution and Display Size 8

2.1.1 Human Engineering Considerations 8

2.1.2 Resolution Density 9

2.1.3 Display Size 10

2.1.4 Total Resolution 11

2.2 Brightness and Dynamic Range 13

2.2.1 Gray-Shade/Contrast Relationship 13

2.2.2 Dynamic Range 15

2.3 Recommendations 17

3.0 FEASIBILITY ANALYSIS 19

3.1 Baseline Design - Overall Description 19

3.1.1 How the Concept has Been Made to Work 22

3.1.2 The Advantages of the Hughes Approach 27

3.2 Electrical Operation and Circuit Fabrication 27

3.2.1 Addressing 27

3.2.2 Sweep Circuits 30

3.2.3 Video Circuits 32

3.2.4 Wafer Fabrication - Feasibility Analysis 39

CONTENTS (Continued)

3.3	Illumination and Viewing	41
3.3.1	Lighting Under Natural Sunlight	42
3.3.2	Artificial Lighting of the Display	46
3.3.3	Summary Guidelines	48
3.4	Fabrication Costs	48
3.4.1	Cost Projection	49
3.4.2	Electrode Array Chip Modules	50
3.4.3	Drive Circuit Chip Modules	51
3.4.4	Assembly Costs	51
3.4.5	Support Equipment	52
4.0	CONCLUSION	53
4.1	Recommendations	53
4.1.1	HIRSADAP Radar	53
4.1.2	Display	55
4.2	Program Plans for Future Development	57
4.2.1	Concept Demonstration	57
4.2.2	Detailed Design and Evaluation	58
4.2.3	Component Fabrication and Assembly	58
4.2.4	Display Refinement	59
APPENDIX A - TECHNICAL FACTORS PERTAINING TO LIQUID CRYSTALS IN DISPLAY APPLICATIONS		61
APPENDIX B -ELEMENTAL ADDRESSING CIRCUITS COMPUTER SIMULATION AND ANALYSIS OF FEASIBILITY . . .		69

LIST OF ILLUSTRATIONS

Figure		Page
1	The Hughes Experimental Liquid Crystal Pictorial Display . .	5
2	Modulation Sensitivity Function of Human Visual System	10
3	Preferred Viewing Distances for Visual Detection Related to CRT Diameter	11
4	Optimum Display Size and Resolution Density as a Function of Viewing Distance	12
5	Display Gray Scale Range With Adaptation Mismatch	16
6	Early Feasibility Model of a 1 Inch by 1 Inch Section of the Hughes Liquid-Crystal	20
7	Digitized Image of an Eye	21
8	Liquid Crystal Cell Operation	22
9	Module Construction	24
10	Building Block Approach to Large Panel Display	25
11	Basic Module Construction Illustrating Picture Element Details	25
12	Electrical Operation of Hughes LX Pictorial Display	26
13	Schematic Diagram of Line-At-A-Time Addressing Circuit . .	28
14	Dual, 64 Bit, Shift Register	31
15	Schematic Diagram of Sweep Driver Amplifier	32
16	Typical Serial/Parallel Video Converter	34
17	Sixteen Channel Serial/Parallel Video Converter	36
18	Schematic Diagram of Video Driver Amplifier	37
19	Ideal Lighting and Viewing	42
20	Effect of Lighted Object in Reflected Field of View	43
21	Conceptual Idea - Cockpit Installation Using a Nonlouvered Light Trap	44

LIST OF ILLUSTRATIONS (Continued)

Figure		Page
22	Conceptual Idea - Cockpit Installation Using Overhead Louvered Light Trap.	45
23	Conceptual Idea - Cockpit Installation Using Front Louvered Light Trap	46
24	Edge Lighting Configuration of Liquid Crystal Display	47
25	Trends of Actual Device Cost	49
26	Wafer Processing Projection	50
27	Wafer Yield Projection of Device Fabrication Costs	50
28	Block Diagram of Radar System	54
29	Assembly of LX Display From Semi-Conductor Modules	55
30	Program Plan for Liquid Crystal Pictorial Display Developments	57
31	Diagrams of Packing Effects in Liquid Crystals.	62
32	Schematic Diagram of Line-At-A-Time Addressing Circuit	69
33	Schematic Diagram of Capacitor Charging Circuit	70
34	Formulation of Contrast Equation	72
35	Equivalent Circuits of Elemental Cell	73
36	Graphical Presentation of Equation Solutions as Functions of Time	75
37	Contrast as a Function of OFF/ON Ratio.	76

1.0 INTRODUCTION

1.1 General

Recent advances in digital synthetic aperture radar signal processing have increased the quality of sensor video to a point where a simple cathode-ray tube can no longer adequately perform the information display function for this class of system. Other military airborne applications, such as: cockpit vertical situation displays, master monitor displays, high-resolution radar displays, helmet-mounted displays, and head-up displays have reemphasized this disparity between the system requirements and the basic capabilities of the CRT. The primary system disadvantages of the CRT are its length (in high-resolution configurations), its need for a high-voltage anode supply, and its poor visibility under direct sunlight. This report presents the findings of a study on the application of a liquid crystal pictorial display to synthetic array radar (SAR). A reflective liquid crystal display was chosen for this application because in earlier development work by Hughes it was demonstrated to have great potential for replacing the CRT in future military applications where good visibility is required under high ambient illumination. In this regard, the liquid crystal pictorial display should prove to be an improvement — not merely a replacement.

1.2 Purpose and Scope

The purpose of the study effort described herein has been to identify a promising reflective display subsystem approach and to establish the feasibility of the approach for the display of high-quality SAR sensor information in an airborne environment. In addition, a set of device requirements has been defined and a course for future development is suggested that will aid the USAF in future planning for SAR display subsystem development.

1.3 Background

Digital synthetic-aperture radar systems, currently under development by the USAF, have resulted in sensor video imagery of unprecedented resolution and dynamic range. This combination of attributes has proven to be too great for conventional cathode-ray tubes (CRTs) to cope with, however, a relatively recent application of multi-beam cathode-ray tubes to SAR display offers considerable promise. Nevertheless, for the present, it appears that the multi-beam technique can achieve the required image quality only at the expense of considerably greater package length than could ultimately be tolerated by the airborne application. Other factors, inherent to the formation of images on CRTs, contribute to further degradation of image quality in the display of very high-quality radar information. This includes the effects of deflection spot defocusing, aperture distortion (spot deformation), electron-gun anomalies, beam array skewness, loss of beam convergence, and beam interaction. Good image performance can be achieved with the multi-beam method, however, and Hughes Aircraft Company, as well as others in the field, are working toward reducing the overall size and the complexity of the technique.

The development strategy in the Air Force and at Hughes Aircraft Company has involved the parallel pursuit of alternative techniques for the display of SAR imagery. Some of the alternatives that have been investigated in the past for this application include rapid film processors, thermoplastic schlieren projection systems, and nucleation recording media. Unfortunately, these are cumbersome for the airborne environment; also, they do not interface efficiently with the digital signal processing used in contemporary SAR systems.

For the past two years, Hughes Aircraft Company has sponsored the development of solid-state displays. The goal of this internal research and development has been to provide a more attractive alternative to high-quality cockpit display than is presently provided by cathode-ray tubes. Early in 1971, this work led to the first practical configuration for providing a real-time, shades-of-gray, pictorial display using a reflective liquid crystal (LX) medium.

The continuing pursuit of this program by Hughes has led to the construction of several one-by-one inch display cells that provide shades of gray display and image storage (an effect analogous to phosphor persistence) on a picture elemental basis. Through the use of ion-implanted, MOSFET technology, Hughes had demonstrated this technique on a one-inch square display cell composed of a matrix array of 100 x 100 picture elements (pixels).

Display cells constructed under that program and performance data obtained from them have provided the experimental basis for the study recommendations of this report.

1.4 Accomplishments

The work accomplished under this study is reported on in three major sections:

Section 2. Requirements Analysis

Section 3. Feasibility Analysis

Section 4. Conclusion and Recommendations

The significant findings will now be summarized.

1.4.1 Requirements

An investigation of the operational requirements for a real-time high-resolution airborne display subsystem has been conducted from the standpoint of optimizing the operator tasks of target acquisition and identification. Display visibility is a key factor in this process and a set of realistic requirements that define the degree of display visibility that is needed have been formulated. They are:

- | | |
|--------------------------|---------------------------------------|
| • Display Resolution | 1000 x 1000 pixels |
| • Display Size | 10 x 10 inches |
| • Brightness/Reflectance | 20 percent of lambertian surface |
| • Video Encoding | 4 bits |
| • Contrast Ratio | 64:1 |
| • Gray Shade Rendition | 13 shades under 10,000 ft. C. ambient |

1.4.2 Feasibility

For a display concept to be feasible, it must:

- Meet the specific requirements of the SAR display application.
- Have other applications over which the development cost can be spread.
- Be fabricated at a cost competitive to existing displays used for similar purposes.

A baseline design, based upon an experimental display being fabricated by Hughes, has been formulated for the SAR application. This baseline design and experience with the experimental display (see Figure 1) were used as investigative tools in conducting a series of detailed feasibility analyses. These encompassed the following areas:

- Electrical Operation. Includes addressing, display sweep, video register operations, timing, and wafer circuit fabrication.
- Illumination and Viewing. Includes guidelines to be applied when designing reflective display installations for aircraft cockpits.
- Fabrication Costs. Includes production cost estimates and yield factors extrapolated from similar existing production programs.

From the foregoing analyses and from measurements which were taken on the Hughes LX pictorial display, it was concluded that the LX reflective display is not only feasible for application to SAR radars, but provides a capability for simplifying the SAR-to-display interface and for reducing the complexity and hence the cost of auxiliary scan conversion equipment.

1.4.3 Recommendations

A reflective liquid crystal pictorial display having a total resolution of 1024 x 1024 picture elements and useful dimensions of 10.2 x 10.2 inches has been recommended for future development. A unique feature of the display subsystem is the scan-converter to display interface which is configured to provide 16 parallel video channels, thereby reducing the SAR scan-converter data rates to achieve a significant increase in reliability at lower memory cost than is presently possible.

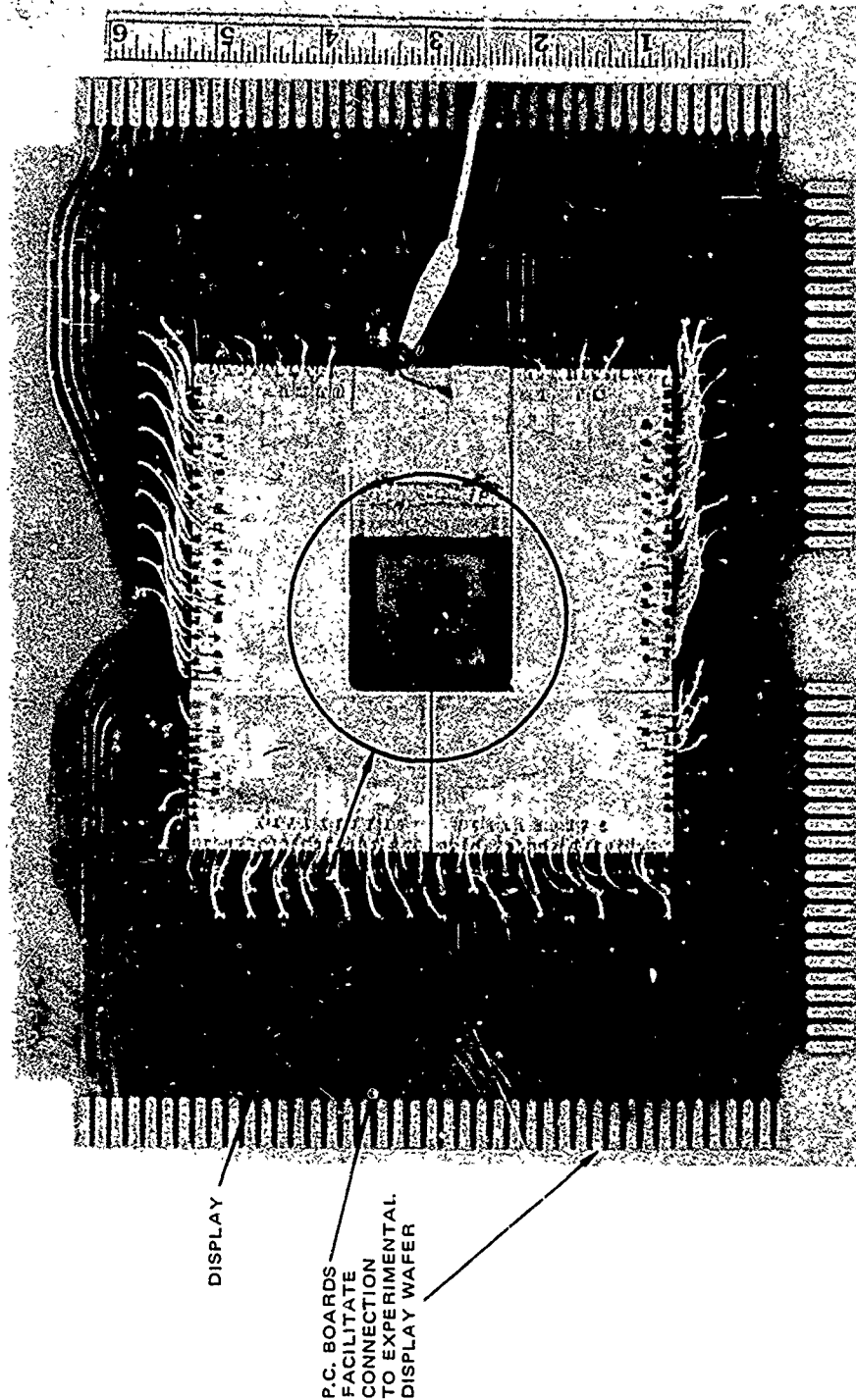


Figure 1. The Hughes experimental liquid crystal pictorial display.

2.0 REQUIREMENTS

In the application of reflective display techniques to SAR systems, new opportunities arise to achieve performance objectives heretofore considered difficult or impossible to meet with other classes of displays. For this reason, it becomes possible to realistically set forth display requirements that more closely respond to pilot or observer needs. In this context, displays that will be used primarily for target acquisition and identification must provide an information input to the operator that will result in his optimum speed-of-response. Optimization of display visibility is key to this process and therefore has been the central objective of performance analyses which follow.

Several interdependent factors enter into the requirements analysis; they are: range of operator-to-panel viewing distance, display size, resolution, brightness, and contrast. They are dealt with by first formulating a set of requirements based upon the maximum capabilities of the human observer and then adjusting these requirements so as not to exceed the information capability of the sensor.

Of considerable importance is the fact that either the CRT or the reflective panel display are sequentially addressed devices that represent a volatile storage media for the presentation of sensor video and as a consequence must be refreshed to avoid objectionable flicker. Also, the scan format of the sensor must be converted into the scan format of the display. The foregoing results in a requirement for scan conversion which, for a practical system, implies the use of digital techniques. Inherent in these techniques is the necessity to digitally encode the video signal. Thus, the gray-scale response of the display subsystem is dependent upon the number

of bits used for the digital encoding of the video in addition to the ultimate contrast of the display subsystem itself. The number of bits required for this process is determined from human observer requirements, based upon consideration of the effect of the number of gray shade steps on the quality and hence the acceptability of transferred information, and upon the effect of the surround brightness on the number of gray shades that can be perceived.

2.1 Resolution and Display Size

2.1.1 Human Engineering Considerations

The purpose of a display is the communication of information to the observer and any new display device is useful only to the extent that it achieves that end. Known principles of human vision and of the associated cognitive processes have been applied to the delineation of requirements for the LX reflective display and its future development. The following paragraphs briefly review the current knowledge of human vision as it applies to the operator tasks postulated for the LX display.

One of the primary requirements of any transmission medium is the frequency response characteristics, which is defined as the modulation transfer function (MTF). Because of extreme retinal nonlinearity, the use of the MTF concept has been constrained in its application to vision; however, a counterpart is found in the modulation sensitivity function (MSF), which is enunciated for specific conditions of illumination and retinal position. Implications of the visual MSF for display design are discussed in the following section entitled "Resolution Density."

The amount of information transmitted by a display is a function of its total resolution, intensity encoding, and temporal characteristics (e.g., repetition rate). User preference in viewing displays, while performing time-critical search and detection tasks is cited, and a range of visual angles — and, hence, display sizes is derived from the data. Similarly, experimental evidence is cited as a basis for estimating the required number of gray shades.

A problem that frequently arises in the use of displays in an aircraft cockpit is degradation due to extremely high ambient illumination. Because the liquid crystal medium forms a reflective display, its visibility can be expected to improve under high brightness with the result that brightness and dynamic range requirements can now be chosen which more closely match the input capabilities of the observer. The discussion that follows is concerned with the bandwidth of the observer/display system. It is important to note that brightness affects these data, which were taken at nominal values of 740 fL and at 0.5 msec duration, in that the image contrast perceived by the observer will be reduced as a logarithmic function of the image intensity (Weber's Law).

2.1.2 Resolution Density

An optimum display design is one that provides a minimum resolution density or a minimum number of resolution picture elements (pixels) per unit length while conveying the necessary information to the observer. The minimum number of raster resolution elements in a real-time display application is dictated by the number that permits the required comprehension rate of the data presented and not the minimum number that permits merely comprehension under steady-state conditions. It has been found that, for rapid comprehension, the pattern or granularity resulting from the discrete nature of the repetitive elements forming the raster must not be objectionable. To estimate the point at which the discrete nature becomes objectionable, one must understand the visual response phase of the human observer. MSF peaks for the human observer at 5 to 7 cycles per degree (see Figure 2). Thus any structure such as pixels or scan lines will be highly visible at that value. The 50 percent point has been chosen as a value for which regular structure ceases to be visibly objectionable; this corresponds to a spatial frequency of 18 cycles per degree.*

Two viewing distances are typical for cockpit displays: 30 inches, which corresponds to the nominal task eye position and 20 inches, which

*T.M. Cornsweet, Visual Perception, Academic Press, New York 1971, pp 341 to 343.

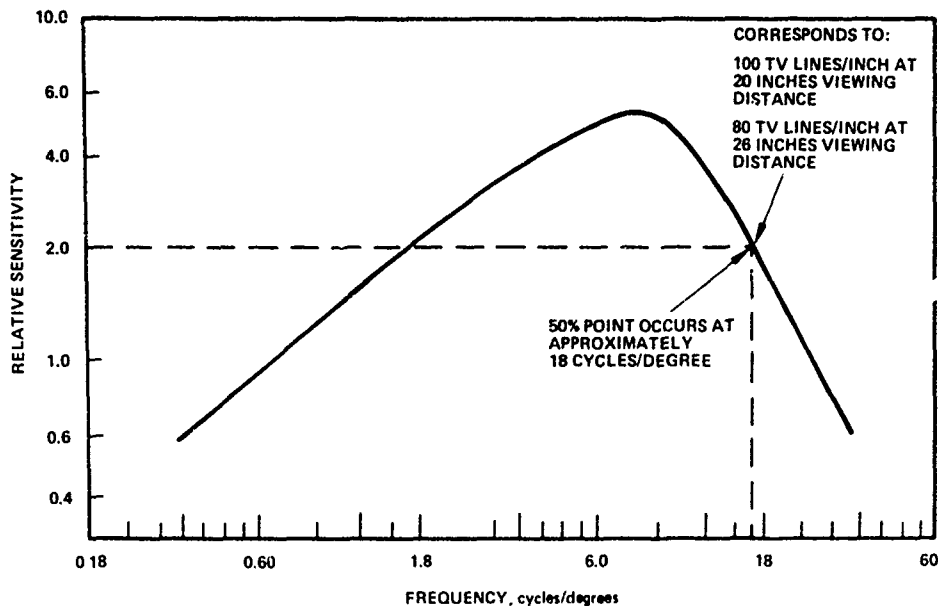


Figure 2. Modulation sensitivity function of human visual system.

corresponds to a vigilant condition. Resolution of 18 cycles per degree is equivalent to 36 pixels per degree. Referring to Figure 4, it can be seen that the most demanding condition for resolution density occurs when the pilot is in the vigilant viewing position (20 inches) corresponding to 104 pixels per inch. On this basis, 100 pixels per inch has been chosen for the LX pictorial display. At this resolution density, viewing distances of 21 inches and greater meet the minimum stipulation of 18 cycles per degree.

2.1.3 Display Size

Several aspects of the manner in which operators search a display for relevant information bear on the display size. For example, it has been common practice to favor large displays wherever possible, under the "the bigger, the better" assumption. Yet operators can search only about fifteen degrees visual angle (equivalent to a 7-inch diameter circle at 26 inches viewing distance) with only eye movement, greater search areas require head movement and attendant loss of time.

In a study performed at Hughes, a group of operators was given a series of typical radar displays ranging in diameter from 6 inches to 12 inches. They were asked to perform optimum speed-of-response search

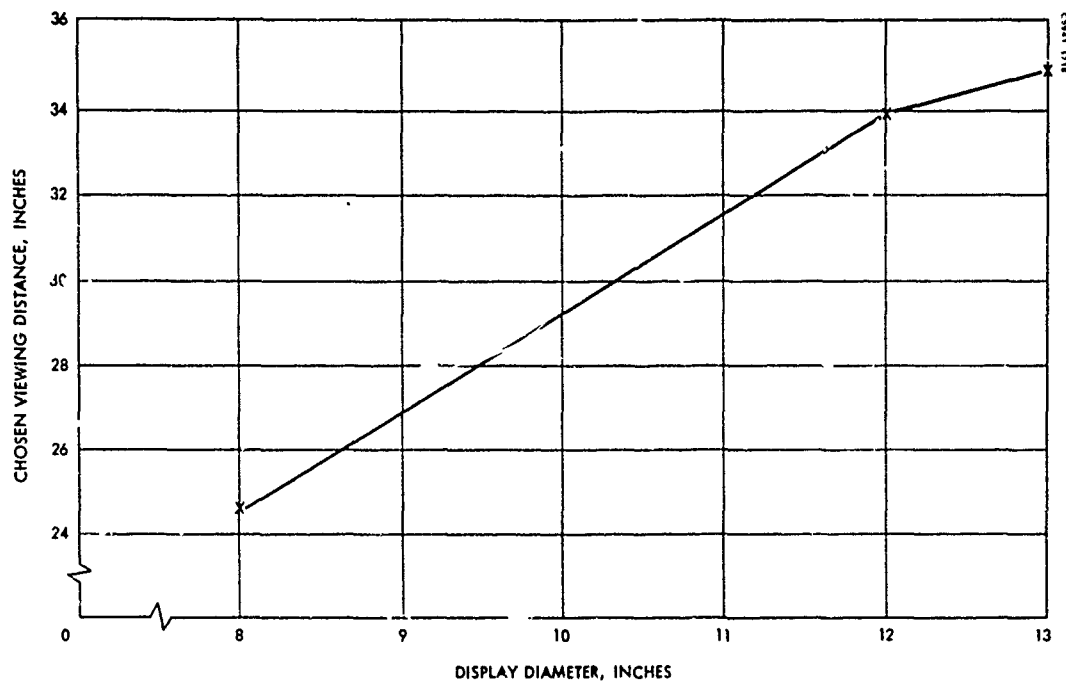


Figure 3. Preferred viewing distances for visual detection related to CRT diameter.

and detection tasks, and the average viewing distance selected by each operator was recorded during the task. As shown in Figure 3, operators in this group varied their distance exactly proportionally to the diameter of the display, choosing a distance such that the entire display subtended about 20 degrees visual angle. The fact that other studies have shown that operators tend not to search the outer 20 to 30 percent of planned-position indicator display substantiates this and indicates the choice of a 20-degree visual angle to be preferred for search and detection tasks. A line representing the 20-degree visual boundary has been added to Figure 4 and indicates that to meet the most demanding requirement for display visibility, viewing from 30 inches, will require a display size of 10.4 inches.

2.1.4 Total Resolution

The total resolution of the display is the product of the resolution density and display size. The resolution density is selected based upon the criteria that the discrete nature of the display not be objectionable at the closest viewing distance. The display size is selected based upon the criteria that the display subtend the preferred viewing angle at the nominal

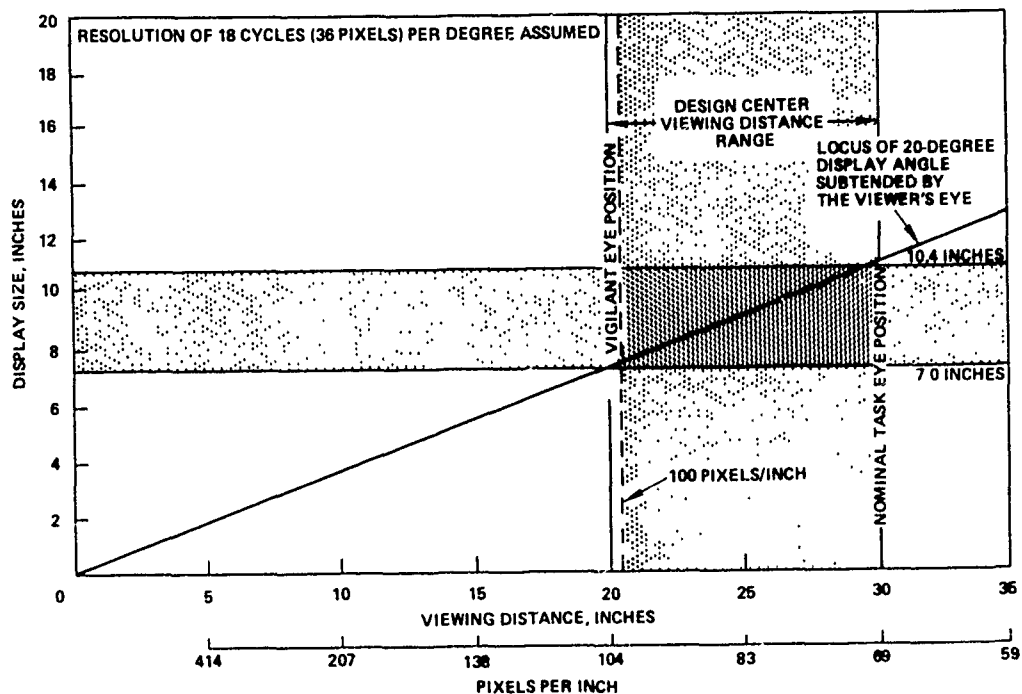


Figure 4. Optimum display size and resolution density as a function of viewing distance.

viewing distance. From the previously developed requirements, it has been shown that the optimum resolution density is approximately 100 pixels per inch and that the optimum display size is approximately ten inches, leading to the conclusion that the optimum total resolution of the display is approximately 1000 pixels. This resolution is greater than the 700 pixels required by the 18-cycles per degree criterion, at the nominal viewing distance of 30 inches. Selection of a lower resolution, however, will lead to reduced information flow to the observer, because his ability to discern detail will be impaired by the pixel structure as he moves closer to the display. Thus, 1000 pixels are required for rapid data assimilation at all viewing distances. The 1000-pixel figure is a guideline requirement because the psychophysical data upon which it is based are typically subject to a ± 20 percent variation. The actual number, therefore, can be tailored to meet specific system standards; for example, a digital system would require 1024 or 2^{10} pixels, while a standard high-resolution television system would require 945.

The total resolution or the number of pixels across the display width may also be influenced by the capabilities of the signal source or sensor. If the sensor resolution is matched to the resolution of an optimized display, the system is man-limited. In matching the sensor resolution to the display resolution, one must consider not only the number of elements but also the phase relationship between the display and the sensor elements. If the display is synchronized to the sensor and if there is a one-to-one relationship between the elements of the display and the elements of the sensor, a display results that is *isomorphic* to the sensed imagery. In this case, displaying less than the number of transmitted elements would result in a loss of information. If it is impossible to achieve an isomorphic relationship, the loss due to the resulting mismatch can be minimized by increasing the number of display elements. When a discrete element display, such as the liquid crystal display, is used with an existing sensor having less than 1024 element total resolution, then the total resolution and the size of the display should be scaled down proportionally if it will permit an isomorphic relationship to be established.

2.2 Brightness and Dynamic Range

The gray shade rendition of a reflective LX display depends upon the following:

- Maximum value of contrast ratio
- Transfer function (reflectivity-to-electrical input)
- Ambient illumination

These factors must be considered when estimating the number of gray shades available from a liquid crystal display.

2.2.1 Gray-Shade/Contrast Relationship

The number of effective gray shades available on a display is ordinarily determined by calculation from the maximum value of the contrast ratio based on the assumption that a luminance ratio between adjacent elements of 0.707:1 is a just-barely discernible change. Weber's law, which is approximately true for the range of brightness contemplated for the liquid crystal display, states that this ratio remains the same regardless

of the absolute brightness of the image. The number of shades of gray equals the number of 0.707:1 steps plus 1 for the black level.

Liquid crystal display luminance ratios of greater than 100:1 have been measured in the laboratory using materials that also have stable electro-optical transfer characteristics. A luminance ratio of 100:1 corresponds to approximately 14 shades of gray including black. The maximum range of the human eye is approximately 1000:1, or 20 gray shade steps, but the adaptation of the eye to the peripheral illumination level typically reduces the observable range to less than the 14 levels because a high adaption level increases the threshold or the minimum luminance at which an image can be perceived.

Effect of Surround

Defining the minimum luminance is difficult, since it is related to the intensity, area, and retinal location of the surround image. Immediate surrounds will reduce display brightness linearly and inversely as a function of the surround brightness. It is therefore advisable to minimize the effects of surrounds by making the immediate display periphery as nonreflective as possible.

The greater cockpit environment including instrumentation, outside ambient illumination, and so on, exerts a second-order effect on display brightness and on effective contrast by increasing the preadaptation level of the observer. This is a temporal effect and in the analysis that follows, it is assumed that the operator has been viewing the display long enough for preadaptation effects to be negligible.

Granularity and Viewer Acceptance — Gray Scale Encoding

A practical reflective display implementation will require digitally encoded video and it is now pertinent to consider how many encoding bits are required for an effective display.

The best data available in this regard come from a study performed by Technicolor, Inc., concerning the encoding of image density for motion picture scenes. Typical scenes (faces, sets, etc.) were reproduced with 2, 3, 4, and 5 bit intensity encoding, yielding 4, 8, 16, and 32 discrete

gray shades, respectively. The scenes were shown to a group of observers who rated them with respect to their ability to recognize faces, the naturalness of the rendition, and the general acceptance of picture quality. The results are shown in Table 1. The estimated information transfer is derived empirically from the viewer recognition data. Two-bit encoding was quite poor in this regard and received a poor quality rating. Three-bit encoding (8 discrete density values) produced an acceptable picture that generally succeeded in conveying picture information, albeit somewhat crudely. Four- and 5-bit encoded renditions received excellent ratings with 4 bits considered adequate for picture reproduction and 5 bits considered virtually indistinguishable from the original material.

TABLE 1. INFORMATION TRANSFER AND VIEWER ACCEPTANCE RELATED TO INTENSITY ENCODING

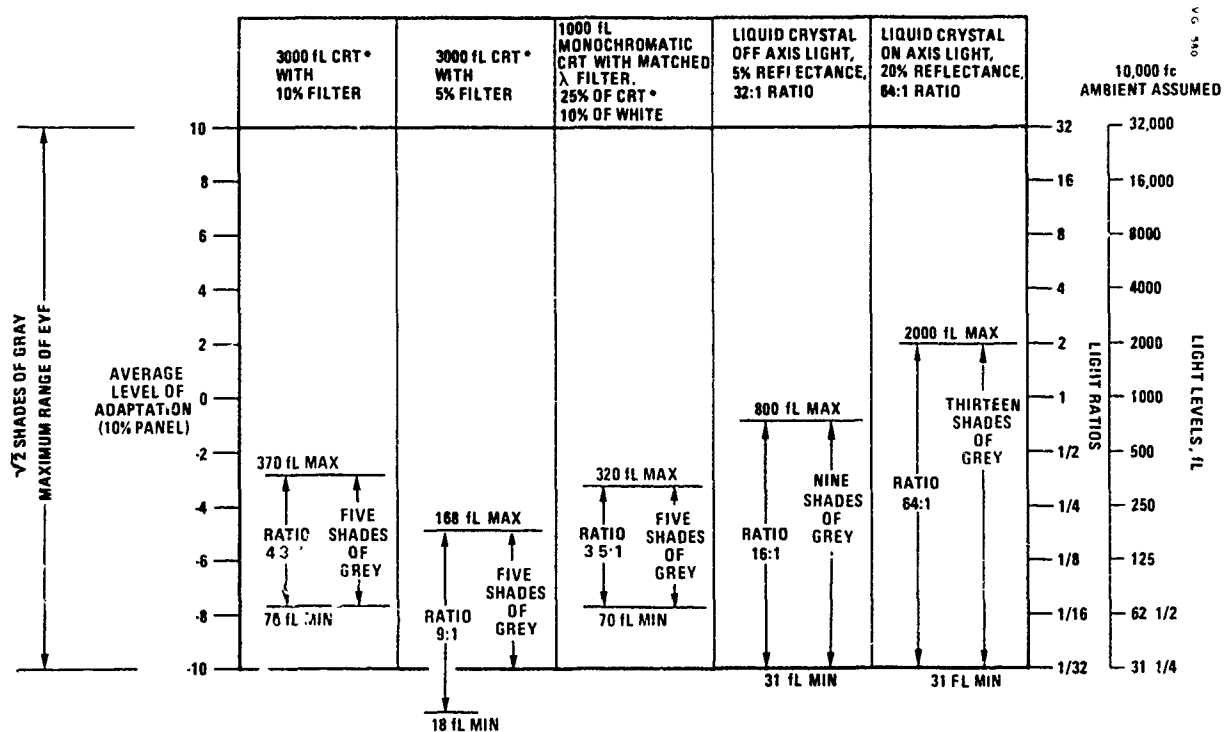
Intensity Bandwidth, bits	Number of Gray Shades	Estimated Information Transfer*	User Acceptability
2	4	40%	Poor
3	8	85%	Good
4	16	95%	Excellent
5	32	99%	Excellent
* Based on ability to recognize forms, faces, etc., in typical motion picture scenes. Study performed by Technicolor Motion Picture Corporation, 1954. Personal communication to Dr. J.G. Rogers.			

2.2.2 Dynamic Range

The values recommended for video encoding (4- and 5-bit renditions) were obtained under theatre viewing conditions which are subdued and highly idealized when compared to the 10,000 fc ambient typically found in aircraft cockpits. Under cockpit viewing conditions, any display will be limited to a dynamic range that is less than can be obtained under idealized circumstances. As the following discussion will illustrate, the LX reflective display requirements can be chosen to provide increased performance over CRT systems even under adverse illumination.

In Figure 5, the effect of ambient illumination on the brightness of CRT's is compared to the LX display for two different values of reflectance.

Although LX reflectance values approaching 50 percent of an ideal lambertian surface have been achieved under careful arrangement of lighting and viewing geometry within the laboratory, it is reasonable to assume a value of 20 percent will be more realistic under on-axis airborne viewing, where minor variations in illumination and viewing angles will be encountered. For off-axis illumination, which could occur due to unfavorable sun angles, this figure could become as low as five percent which for a 10,000 fc ambient, still results in a contrast ratio of 16:1 and a dynamic range of nine shades of gray. Under favorable on-axis illumination, (20 percent reflectance) contrast ratios of 64:1 can be expected with a dynamic range of 13 shades-of-gray. It is interesting to note that, due to the high level of adaptation (observer 0 reference is at 1,000 fL) typical CRT's with good faceplate treatments (10 percent transmission) are limited to six shades-of-gray. Even if CRT brightness is stretched to an impractically high limit, an



*NOTE: ASSUMES 70% CRT PHOSPHOR REFLECTANCE

Figure 5. Display gray scale range with adaptation mismatch.

efficient broadband phosphor producing 10,000 fc brightness could only provide nine shades-of-gray under these viewing conditions and the spot growth under the high beam currents required to produce this range would restrict its use to low-resolution imagery.

For this reason, the CRT brightnesses listed in Figure 5 are limited to the values shown, in the interest of providing a quality image consistent with the 18 cycles/deg. required for target acquisition.

2.3 Recommendations

From the foregoing analysis, a set of realistic performance objectives has been formulated based upon the capabilities of the operator as well as the capabilities of the liquid crystal reflective display. Optimum display visibility for the tasks of target detection and designation will be achieved if the following requirements are met:

- Display resolution 1000 x 1000 pixels
- Display size 10 x 10 inches
- Brightness/Reflectance . . . 20 percent
- Video encoding 4 Bits
- Contrast Ratio 64:1
- Gray Shade Response
($\sqrt{2}$ luminance steps) 13 shades under 10,000 fc ambient

3.0 FEASIBILITY ANALYSIS

For a display concept to be feasible, it must:

- Meet the specific requirements of the SAR display application
- Have other applications over which the development cost can be spread.
- Be fabricated at a cost competitive to existing displays used for similar purposes.

The technique used to investigate the feasibility of the proposed reflective liquid crystal display technology consisted of formulating a baseline design and evaluating specific areas of that design in their ability to meet the above criteria. These aspects will now be discussed in detail beginning with a description of the design followed by an assessment of the feasibility in each case.

3.1 Baseline Design - Overall Description

In formulating the baseline design, care was taken to use techniques that would avoid either basic advances in the current art, or the addition of costly facilities and processing equipments.

An early evaluation model of a one-by-one-inch section of the Hughes liquid crystal pictorial display is shown in Figure 6. The image is produced by a series of square picture elements, each of a different luminance. This can be seen in some of the coarse depictions of the human eye shown in Figure 7. The discrete nature of the display is not noticeable in the finer depictions of Figure 7, however, because the elements are so closely spaced that they are not discernible to the naked eye at normal viewing distances. The proposed display will have 100 picture elements (pixels) per

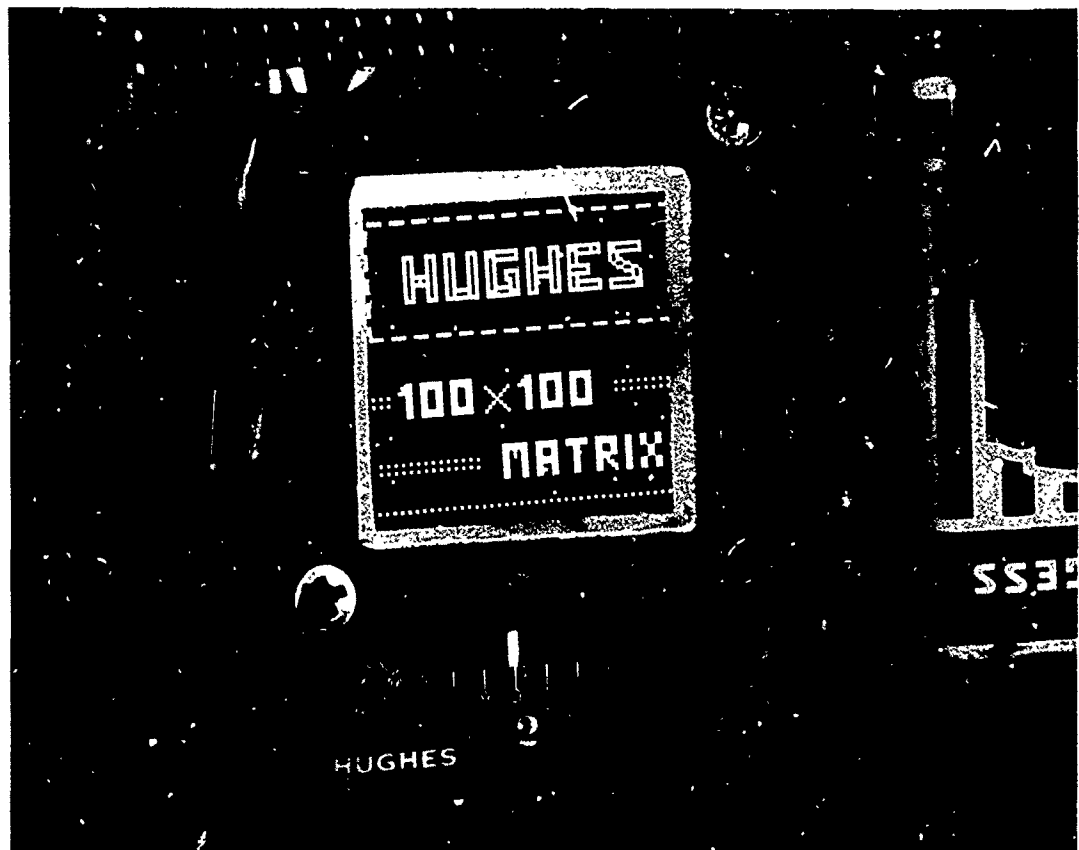


Figure 6. Early feasibility model of a 1 inch by 1 inch section of the Hughes liquid-crystal.

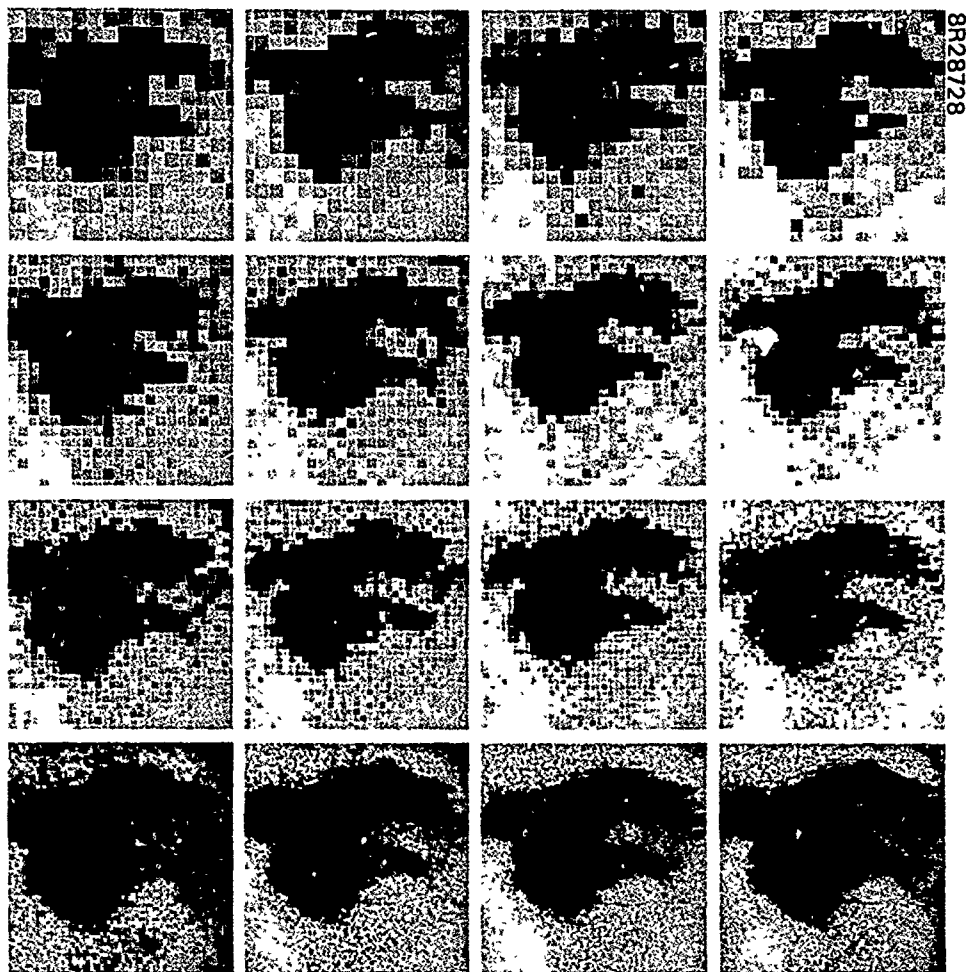


Figure 7. Digitized image of an eye.*

inch and a feeling for this resolution level can be gained by studying the bottom row of photographs in Figure 7 which are respectively from left to right, 60, 80, 100, and approximately 120 pixels/inch. The process used to print this report volume causes some degradation in the resolution of Figure 7. Irrespective of this, the illustration indicates that the discrete nature of the display is barely noticeable at normal viewing distances.

*Photograph reprinted through the courtesy of Information International, Inc.

3.1.1 How the Concept has Been Made to Work

The basic electro-optical phenomenon used to control the light is shown in Figure 8. In a typical cell, a thin layer of liquid crystal material is sandwiched between two electrodes, one of which is transparent, and one of which is reflecting. When the electrodes are at the same potential, the liquid crystal material is clear, and if the cell is positioned correctly, the observer will see a reflection of a dark light trap giving him the impression that the cell is black. When the electrodes are at different potentials, the material appears smokey and if enough light is incident on the cell, light will be scattered to give the observer the impression that the cell is white. The amount of light scattered forward to the observer can be controlled by the electrode potentials.

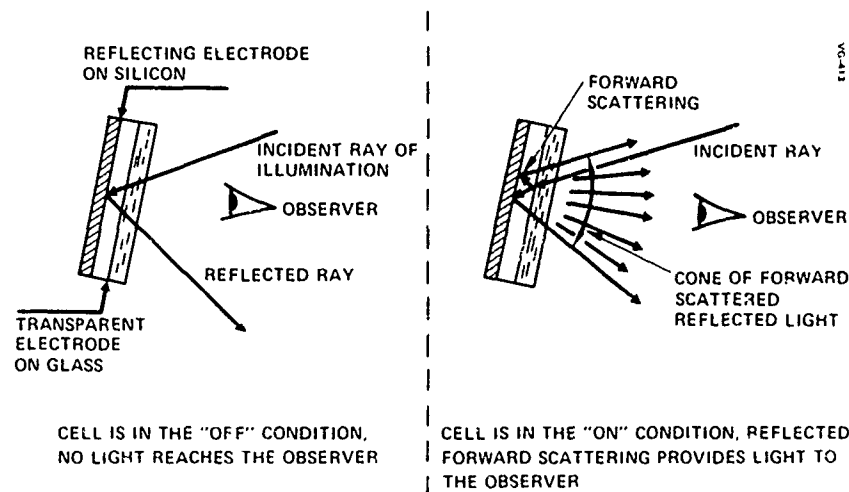


Figure 8. Liquid crystal cell operation.

The multitude of individually controllable cells are formed economically by using large scale integrated (LSI) semiconductor circuit technology developed by the Hughes Semiconductor Research Laboratory, Newport Beach, California. This technology forms electrical circuit components by a series of photographically controlled selective etching processes. The repetitive pattern on the photographic masks is made by copying a single master drawing with a step-and-repeat process. With this process, ten-thousand or more individually controllable liquid crystal cells can be fabricated simultaneously within one wafer.

A simplified sketch of a liquid crystal display fabricated in this manner is shown in Figure 9 (Detail A). The lower layer is a semiconductor wafer in and on which a matrix array of individually controllable reflective electrodes have been deposited. A top cover layer contains a transparent electrode common to all the cells. The space in between contains a layer of liquid crystal material. Each reflective electrode when combined with its companion transparent electrode and the liquid crystal material form an individual liquid crystal cell picture element. A detailed sketch in Figure 9 (Detail B) shows that each of the elemental cells are square with a portion of the display surface allocated for the row and column electrode addressing busses.

A large (10 x 10 inch) liquid crystal display cannot be fabricated as a single LSI device, because of current state-of-the-art limitations on yield, semiconductor chip size, and the size of the processing equipment currently utilized by the industry. These limitations have been bypassed at Hughes through the use of a modular display design shown in Figure 10. To achieve the desired display size, individual square modules are cut from round semiconductor wafer chips and are assembled in building-block fashion to form an array that functions as a single large display. A single glass plate covers the entire display area.

In a large display, the time available to address an individual element is very short compared to the response-time of the liquid crystal material. A sample-and-hold circuit (see Figure 11, Detail C) is provided for each element to stretch the microsecond addressing pulses to the millisecond pulses required by the liquid crystal material.

Practical implementation via existing LSI fabrication techniques requires that the display be addressed a line at a time; a method for doing so appears in Figure 12.

With line-at-a-time addressing, all of the picture elements along any given line are written simultaneously. The sweep shift register controls which line is to be written while the serial/parallel video converters provide, in-parallel, analog video signals to each of the picture elements along the line. The video converters are commanded to alternate their functions, so that while one is collecting data the other is outputting data to a line. Also,

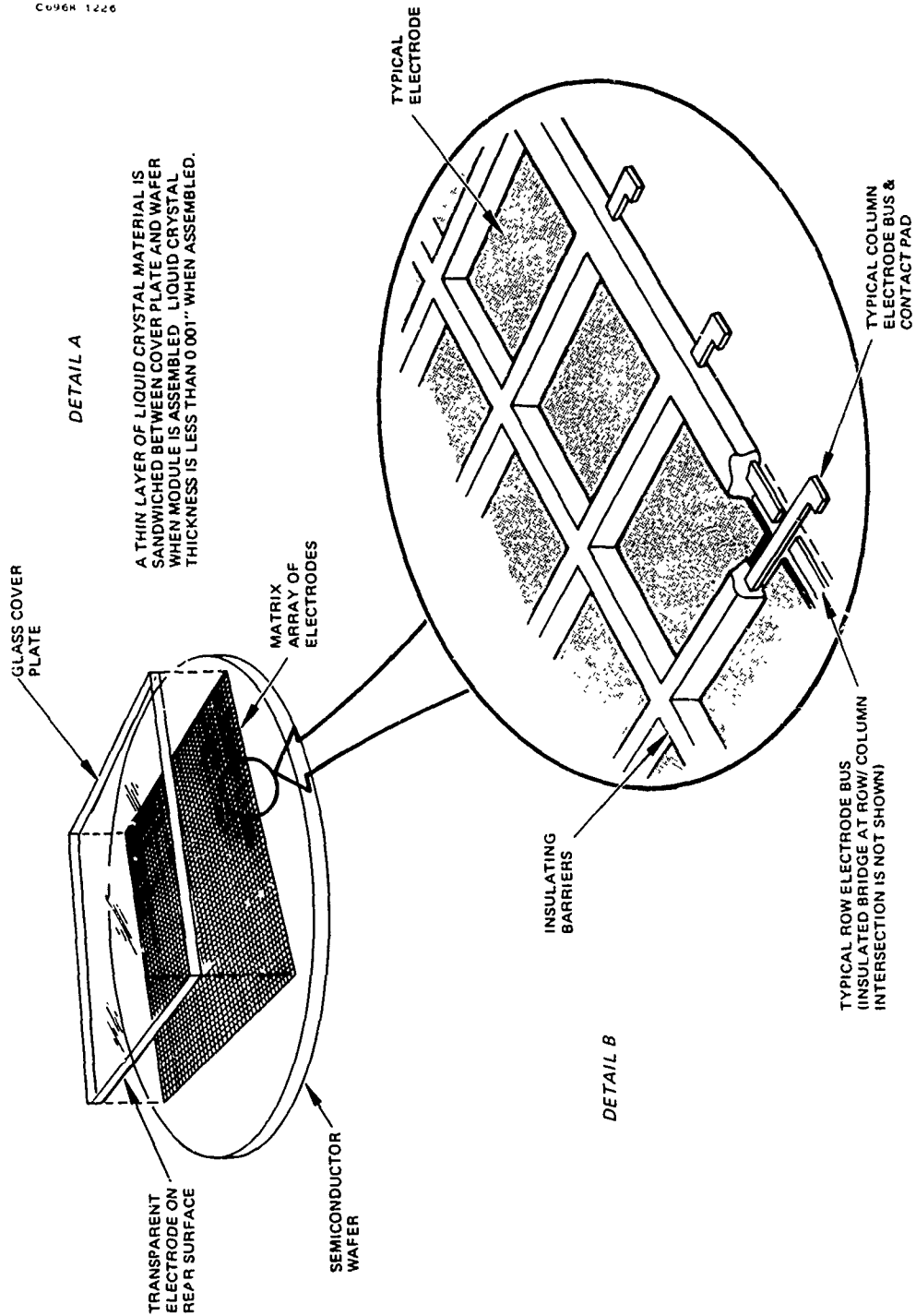


Figure 9. Module construction.

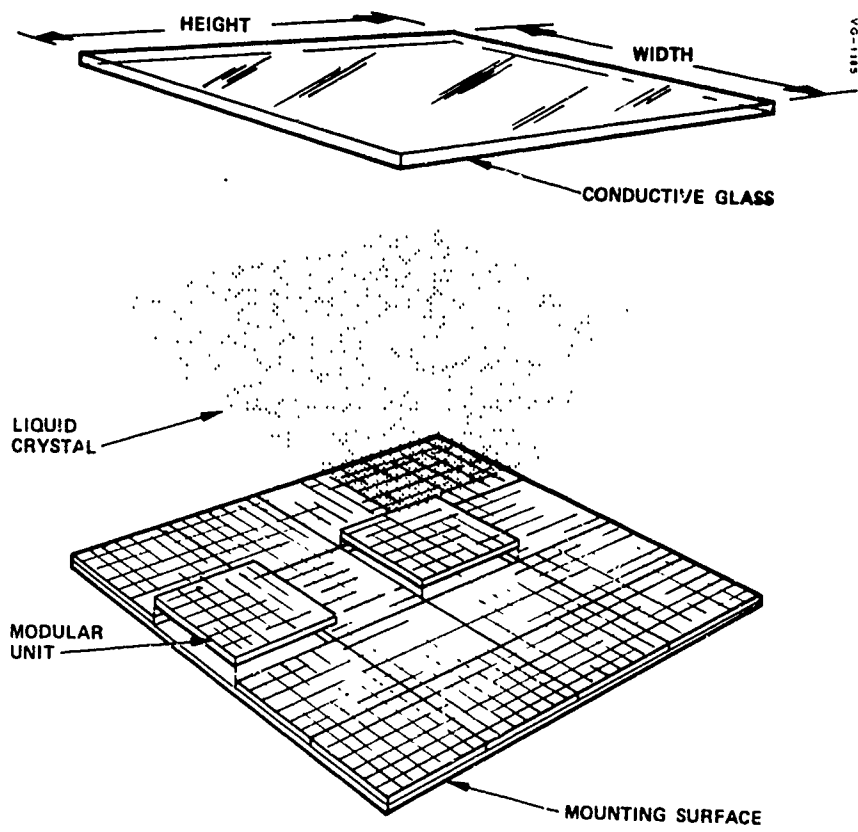


Figure 10. Building block approach to large panel display.

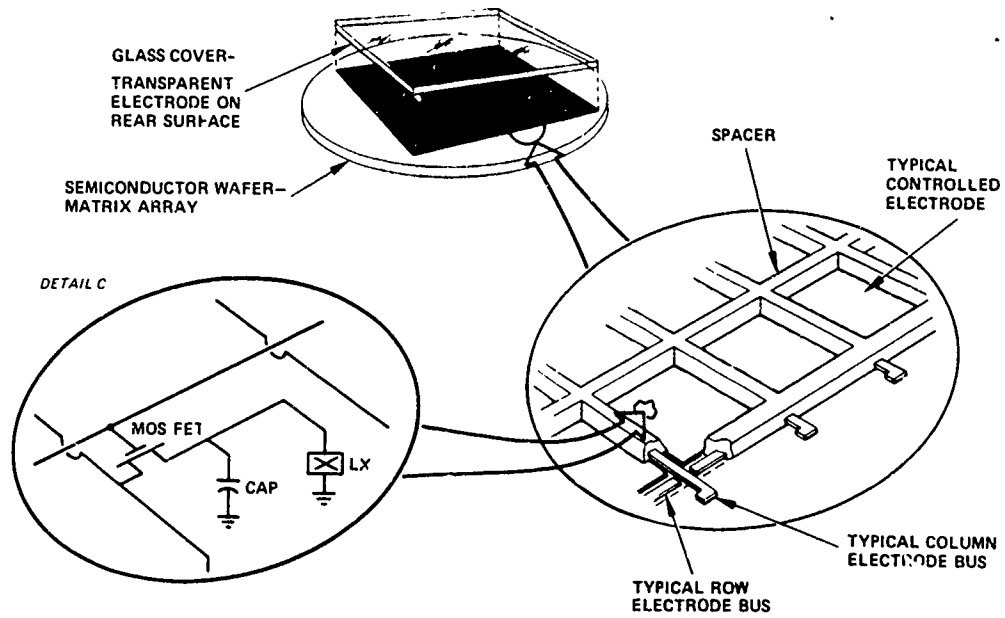


Figure 11. Basic module construction illustrating picture element details.

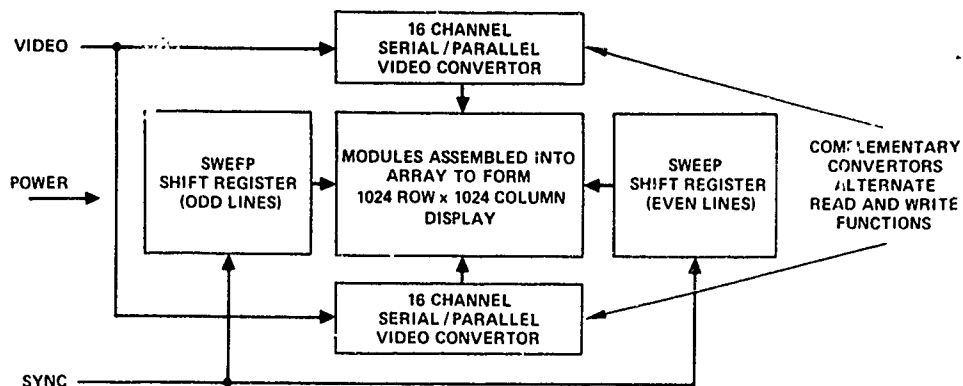


Figure 12. Electrical operation of Hughes LX pictorial display.

two shift registers are utilized, one for each field, providing a two-to-one interlaced display frame, which is compatible with a television raster scan or with scan converted sensors. The line-at-a-time method of scanning has been chosen for the baseline design because it presents the maximum addressing rate that is practical to achieve with the current art in LSI circuitry. Similarly, a television scan format was chosen for the LX display because the time constant required for pixel video storage is commensurate with the maximum values that can sensibly be achieved with the current art in MOSFET devices.

This means that to achieve flicker-free display of SAR data on a liquid crystal display, the radar will need to be scan converted to near-television rates.

An LX reflective display was constructed by Hughes under a company-sponsored research program and the features of the baseline design reported, herein, are taken directly from that effort. Furthermore, the SAR feasibility studies that have been undertaken and that are reported in this section are the direct result of practical experience gained in the design, fabrication, and operation of the Hughes LX Display developed under the company-sponsored program.

3.1.2 The Advantages of the Hughes Approach

From the feasibility studies conducted by Hughes with this class of device, it has been established that the following advantages accrue.

- True digital deflection.
- Unprecedented resolution uniformity - each active element is identical to every other.
- Resolution of 100 elements per inch is readily achieved.
- Unlimited parallel video channels are available for bandwidth reduction and new more efficient display/processor interfaces.
- Good display visibility under typical cockpit ambient illumination.
- Dynamic range (shades of gray) superior to CRT's under high ambient illumination for daytime operation.
- Display output wavelength and brightness are solely a function of the illumination source. For instance, under night operations, red-illumination, or other desired wavelengths may be chosen.
- Easy cockpit installation - very little panel depth is required.
- The viewing area or format may be made to match any likely cockpit panel configuration.

3.2 Electrical Operation and Circuit Fabrication

Electrical operation is concerned with how a dynamic, shades-of-gray display is formed at the elemental picture element (pixel) level. The operations of addressing, the formation of an electric field sufficient to form scattering centers within the LX medium, and the retention of the scattering centers (an effect analogous to phosphor persistence) until they can be refreshed are essential items in this process; they are discussed in the following.

3.2.1 Addressing

In conventional television systems, one video channel carries all the pictorial information in a serial analog data format. The camera (sensor) scans the scene from the upper left hand corner along the top horizontal line from left to right. One scan from top to bottom of the picture area is defined as one field. A second field is then drawn beginning at the upper left-hand corner; but, this time lines are interlaced between the previously drawn lines. Together these two fields form an interlaced frame of the entire pictorial information.

In the LX display, the pixels are accessed by matrix methods, thus for television display a serial line of television analog video data must be converted to parallel data for simultaneous presentation to a line of liquid crystal picture elements. This demultiplexing function is performed in the LX display by a dual serial/parallel analog converter. The line-at-a-time scan proceeds sequentially from the top to the bottom in two alternating fields. In the odd field, the odd-numbered lines are written. Together, the odd and even-numbered lines constitute a full frame of pictorial information. The sweep function is performed by two shift registers: one for each field. They are enabled a line-at-a-time, with one register assigned to the odd lines and the other register assigned to the even lines.

Element Addressing Circuits

The schematic diagram in Figure 13 shows that each pixel is composed of three parts: (1) "typical elemental liquid crystal cell," which is characterized by a small capacitance and a high leakage resistance, (2) a field-effect transistor (FET), and (3) a monolithic capacitor. Together, these parts

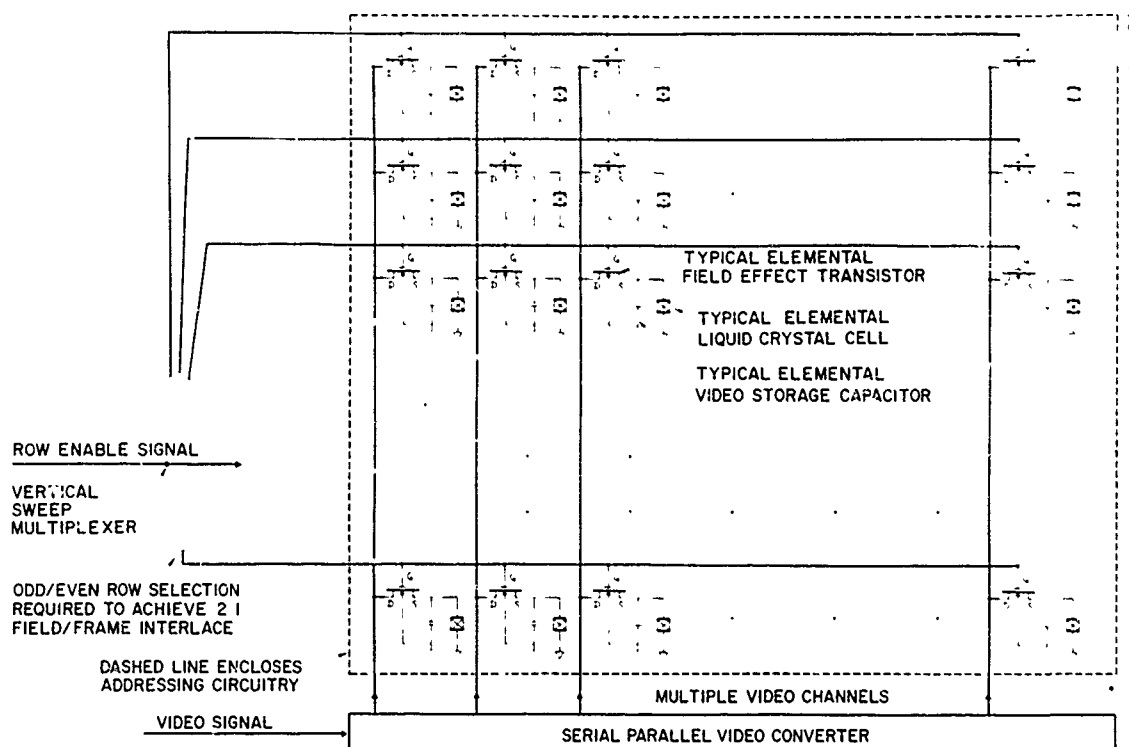


Figure 13. Schematic diagram of line-at-a-time addressing circuit.

constitute an elemental sample and hold circuit to stretch the 30-microsecond addressing pulses to the millisecond lengths needed to energize the liquid crystal material.

Each FET is connected so that when the gate is driven by an enabling signal, the FET is turned on and the elemental capacitor is connected to its corresponding column electrode bus. Conversely, when the gate drive is removed the capacitors are effectively disconnected from the column bus lines by the high FET off resistance. The FETs along each display line are connected in parallel gate electrode bus so that an enable signal from the sweep multiplexer will cause all the pixel storage capacitors along the selected line to become charged to the video level that is present on each of the column electrode busses.

Video information from the serial/parallel converter is provided in parallel, to each column of the matrix, and is updated in synchronism with the sweep multiplexer. Thus, each pixel element along a line is provided with new and unique video information during the time normally allotted to one television horizontal line period (sweep plus blanking interval).

Element Addressing Circuits - Feasibility Analysis

A computer simulation of the operation of a liquid crystal cell in a matrix array was performed (see Appendix B) as a means of estimating circuit parameter values so that the feasibility of achieving them with the proposed LSI techniques could be evaluated. The computer simulation investigated the effect of: (1) the OFF/ON resistance ratio of the field-effect transistor (FET) switch, and (2) the size of the element storage capacitor, on display contrast. The range of initial conditions explored included OFF/ON resistance ratios between 2500 and 25,000 and RC time constants between one eighth and eight times the addressing (ON) interval for a 1000-line, line-at-a-time addressed display.

A set of characteristic curves has been generated as a result of this simulation effort. They show: (1) the OFF/ON resistance ratio of the FET must be at least one order of magnitude greater than the number of lines in a line-at-a-time addressed display if eight shades of gray (plus black) are to be presented, and (2) the optimum size of the elemental storage capacitor

is the size that makes the time constant of the charging circuit (formed by the ON resistance of the FET switch and the elemental capacitor) approximately equal to twice the addressing ON time. The conclusion drawn is that the proposed concept is feasible because: (1) FETs with the required OFF/ON resistance ratio have been routinely fabricated with silicon LSI technology and (2) optimally sized capacitors can be fabricated within the allocated space.

3.2.2 Sweep Circuits

The line enable signal, which commands each of the lines in sequence is analogous to the vertical sweep function required for television raster scan. The function labelled vertical sweep multiplexer in Figure 13 is implemented with a serial-input/parallel-output shift register which has an associated driver circuit for each line of the display. One bit in the shift register corresponds to the address of one line (gate bus), and a single ONE in a field of ZEROS is shifted through the register to cause the lines to be sequenced (swept) in the vertical dimension.

Sweep Circuits - Feasibility Analysis

The feasibility of the baseline design sweep circuits approach is concerned principally with the practicality of providing the necessary gate drive voltage for the display lines and the switching rates that will be required by a 1024 x 1024 pixel SAR display. When a 1024-line display is being refreshed 30 times per second, the basic clock rate of the shift register is 1024×30 , or approximately 30 kHz. This rate is more than two orders of magnitude below the state of the art for LSI-fabricated shift registers of the type illustrated in Figure 14.

The feasibility of providing sufficient gate drive amplitude, i.e.: enough to just exceed the peak-to-peak amplitude of the maximum video signal is now discussed. For the current configuration of the Hughes experimental LX display, the dynamic scattering mode of the liquid crystal material is utilized. The video signal, under this mode of operation, must be approximately 20 volts to excite the liquid crystal to its maximum scattering condition (maximum brightness). The threshold voltage of the FET's within

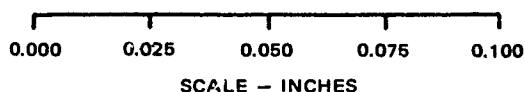
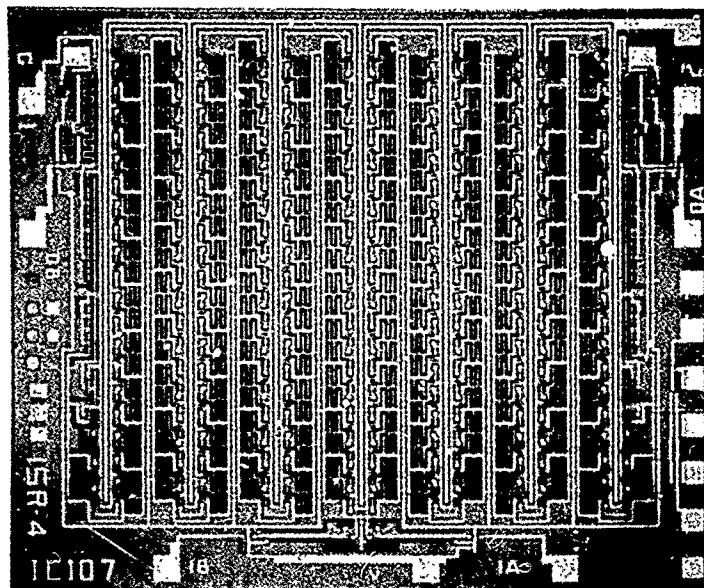


Figure 14. Dual, 64 bit, shift register.

the liquid crystal wafer is approximately 4 volts, resulting in a gate voltage drive requirement of 24 volts. Because the output level of the shift register is 3 to 4 volts, a buffer amplifier is required to provide load isolation and voltage gain. The amplifier must have a 24-volt output voltage swing with a sufficiently high gain-bandwidth product and power drive capability to preserve the line drive pulse shape when loaded with a typical line electrode capacitance of 300 pf. Good pulse shape is necessary to prevent inadvertent enabling of one display line before the adjacent line has been turned off, as the latter could result in image smear. A 33-microsecond line period is required for a 1024-line scan, interlaced 2 to 1, and presented at 30 Hz. Experiments with the Hughes LX display have shown that 27 microseconds are typically required to charge the pixel storage capacitors to new video amplitude values, leaving a balance of 6 microseconds in which to turn on and to turn off the line enabling pulse, if overlap between adjacent lines is to be totally avoided. Actually, some overlap can occur without affecting the image, because of the dynamic resistance characteristics of the FETs

associated with each pixel. Six microseconds is a conservative number for the baseline design, however, and further empirical measurements are necessary before this value can be relaxed or the active line can be increased.

A line-sweep driver amplifier capable of providing quality operation is shown in Figure 15. The amplifier is constructed using integrated circuit techniques and is capable of providing a 30-volt pulse into a 300 pf load with a slewing rate of 10 volts per microsecond. This design should provide a satisfactory switching time since the total desired is approximately 6 microseconds, i.e., 3 microseconds for turn-on and 3 microseconds for turn-off.

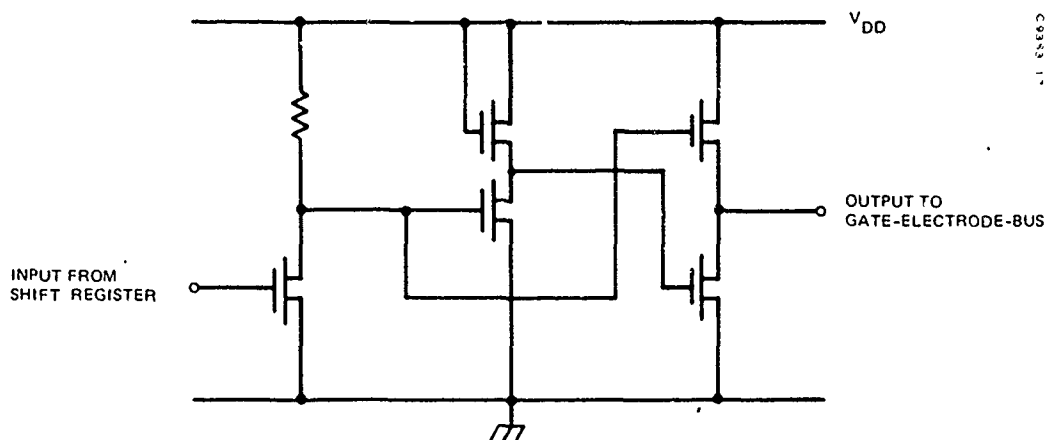


Figure 15. Schematic diagram of sweep driver amplifier.

3.2.3 Video Circuits

Video is applied to the column electrode busses in-parallel, via a serial/parallel video converter and its associated driver circuits. This general arrangement is the one that appears in the baseline design and is the one which has been implemented in the Hughes LX experimental display. For ultimate use with a scan-converted SAR processor video output, it is desirable to provide multiple parallel video inputs to reduce the scan converter complexity, and thereby improve the overall SAR system performance.

How a single serial/parallel conversion is implemented and a discussion of its feasibility as well as the feasibility of converting multiple video inputs for use with scan-converted SAR processors is contained in the following.

Serial/Parallel Analog Conversion

The term serial/parallel analog converter describes a circuit that performs a function analogous to that of a conventional serial/parallel digital converter with the exception that the amplitude (analog value) of the signal is preserved. A serial/parallel converter takes sequentially presented data and stores it in a series of data bins that can be interrogated in parallel. The simplest serial/parallel analog converter consists of a set of sample-and-hold circuits with one sample-and-hold circuit for each of the parallel output channels and a shift-register to cause the sampling function to be enabled sequentially, thereby providing a sample and hold function for each pixel along a line.

Dual Serial/Parallel Analog Conversion

Accessing of the accumulated data requires that there be a pause in the accumulation (sampling) process while the video is being applied to the line of pixels. These pauses would result in a loss of video data, for there is no provision in a real-time display for pauses to occur, unless they can be accommodated during the inactive line-blanking-interval. This interval is impractically short, 6 microsec. nds for the baseline design, requiring a data rate of 171 MHz to permit 1024 sample and hold circuits to be serially updated.

A better scheme is to use two converters (see Figure 16) in an alternating read-write sequence. In this manner one converter is sampling video during the entire time the other converter is outputting data to the line. Thus 32 microseconds are available* for the serial conversion of 1024 bits and a data rate of 32 MHz ensues, which is still beyond the current art of LSI circuits. This is the scheme that has been implemented on the Hughes experimental LX display; however, it is workable because in that display the

*The total frame time available (33.3 msec) would normally result in a line interval of $33.3/1024$, or 32.6 microseconds, but 0.6 microseconds are required for resetting registers.

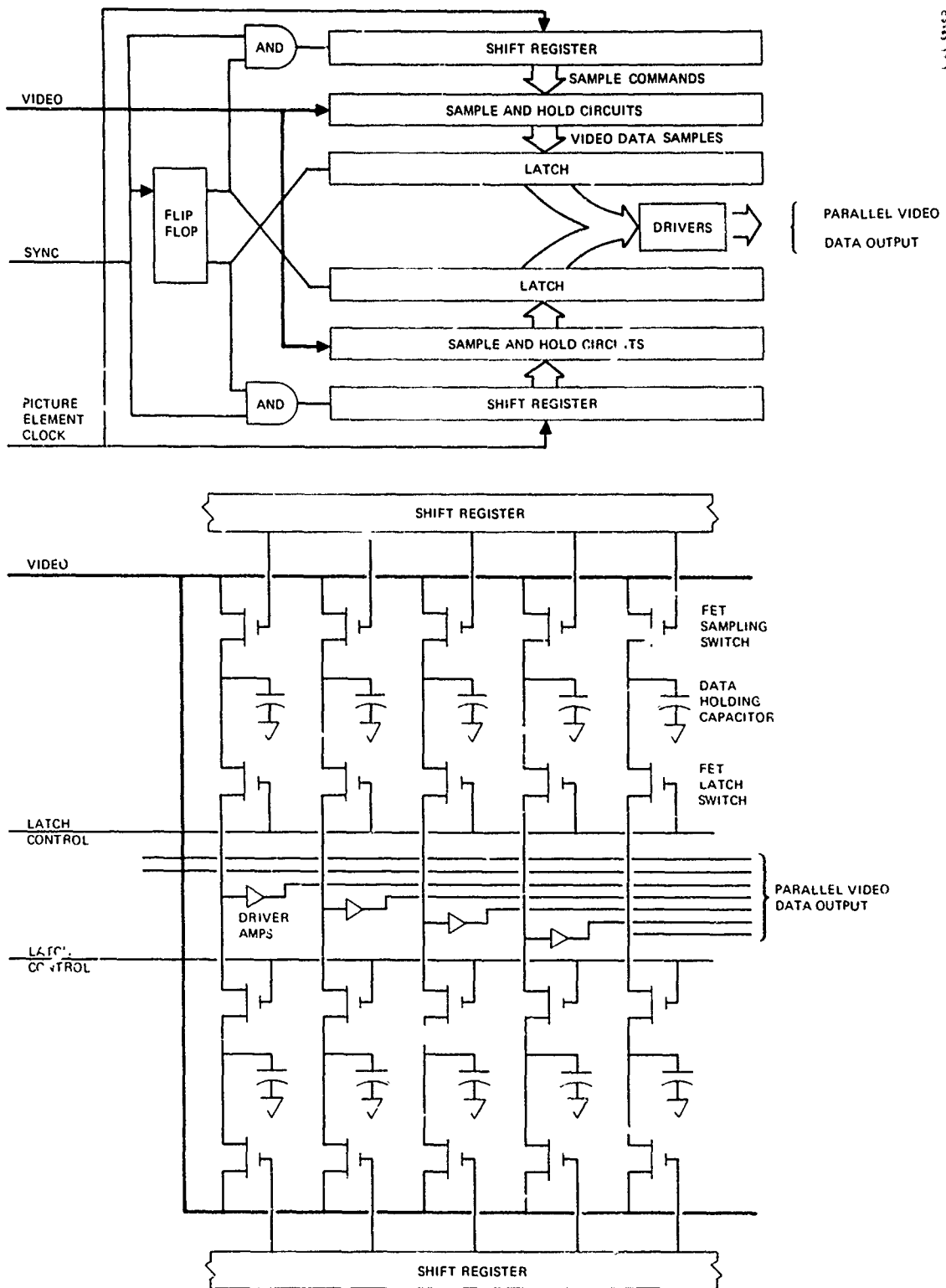


Figure 16. Typical serial/parallel video converter.

number of pixels is 100, presented in 2:1 interlace on a square format, from a 4:3 aspect television raster resulting in the following:

$$\text{Active Line Time} = 3/4 \times 50 = 37.5 \text{ microseconds}$$

Therefore, the shift register data rate for the read or load operation of 100 pixels is $1/0.375 \times 10^6$, or 2.7 MHz. This is well within the state of the art for the MSI circuits that are presently used for that function.

Video Circuits - Feasibility Analysis

The requirements for the proposed SAR display call for a 1024 x 1024 pixel image that is refreshed at a 30-Hz rate, resulting in a 32-MHz data rate that is beyond the present art for LSI semiconductor analog circuits. A sensible way of reducing this rate is through the use of 16 parallel video input channels each having a bandwidth of 2 MHz and each having a dual serial/parallel analog converter. In this manner, LSI semiconductor circuits can be used for the output circuits in the SAR digital scan converter and for the serial/parallel analog converters in the display input channels. It is anticipated that, using LSI techniques, 16 video channels, each with a 2-MHz data rate, can be implemented more economically than a single channel which would require an advanced development program to obtain a converter that would operate at 32 MHz. A single channel converter would entail considerable development risk and would probably require the use of discrete components. On the other hand, each of the 16 video channels requires a dual serial/parallel video converter of the type previously described, and is well within the capabilities of LSI techniques.

SAR Implementation. A block diagram of a 16 channel serial/parallel video converter is shown in Figure 17. The purpose of this converter is to interface between the 16 output lines of the SAR digital scan converter and the 1024 input lines of the display. Each of the 16 video channels, therefore, provides video data for 64 columns of the display. The scan converter is organized to maintain circuit simplicity. Video voltages are separated by 64-bit positions along a line during a single time interval. Thus, in 64 time intervals, one complete line is produced from the scan converter. For

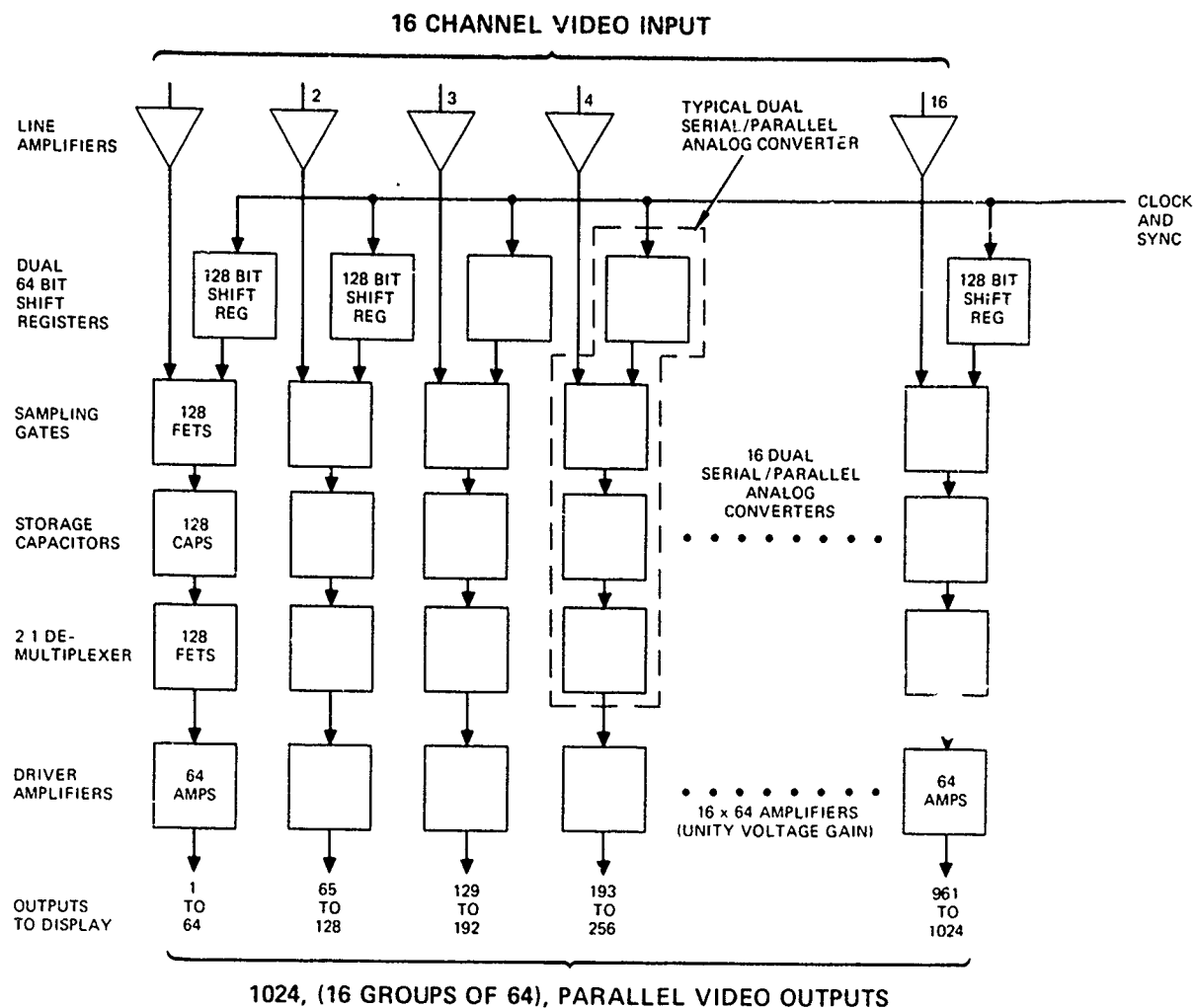


Figure 17. Sixteen channel serial/parallel video converter.

example, in the first time interval, the video element at the extreme left of the line appears on channel 1, the 65th element from the left on channel 2, the 129th on channel 3, and so on. In the second time interval, the 2nd element from the left appears on line 1, the 66th on line 2, the 130th on line 3, and so on. Each of these voltages is stored on individual monolithic capacitors, and, at the 64th interval, the 2:1 demultiplexer switches each capacitor to its respective column bus on the display module. By using the demultiplexer, adjacent lines can be stored on each bank of capacitors, with one line being stored while the preceding line is transferring data (charge) to the display module. This portion of the video converter is a 2048-channel analog memory with a retention time equivalent to two line scan periods (approximately 65 microseconds).

Ability of Circuits to Meet Required Performance. A more detailed diagram showing one video channel of the video converter appears in Figure 18. The video input is amplified to provide the required voltage gain to drive the liquid crystal display. The full-scale video range on the amplifier output is approximately 25 volts. Because the input video is transmitted on 16 parallel channels, the slew rate for these amplifiers is

$$\frac{64 \text{ elements}}{32 \text{ microsec}} \times \frac{25 \text{ v peak}}{\text{element}} = \frac{50 \text{ volts}}{\text{microsec}}$$

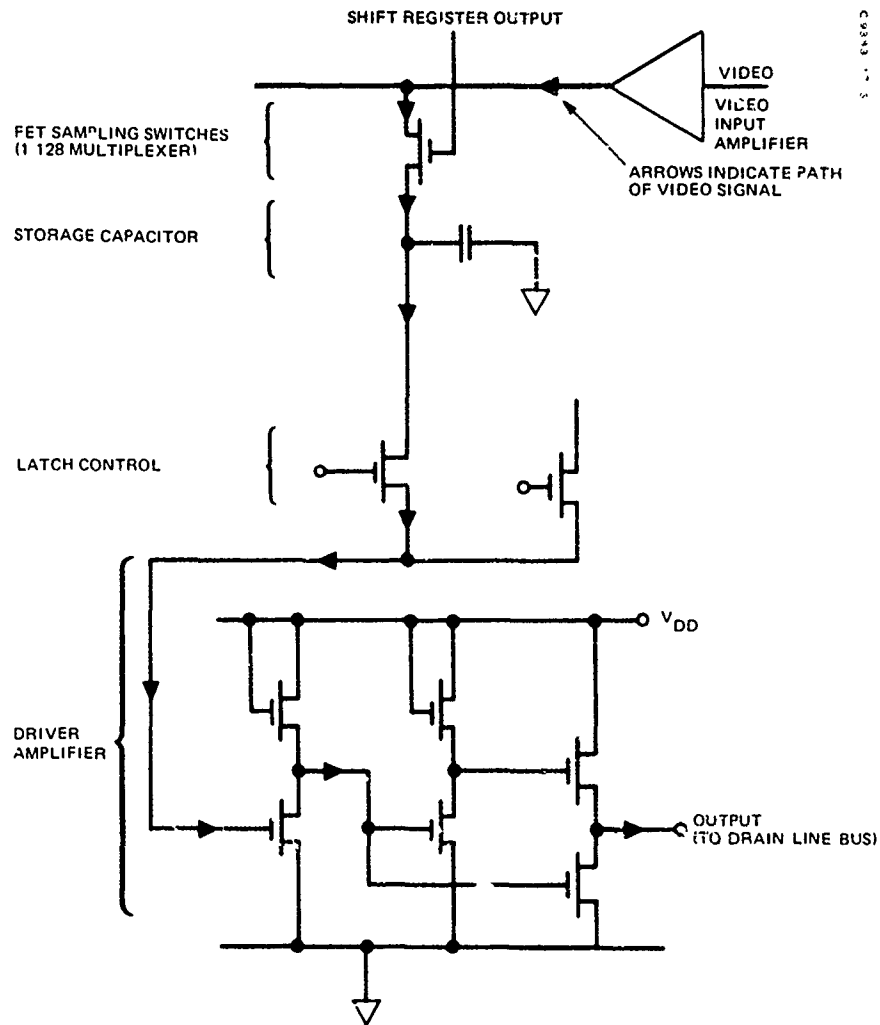


Figure 18. Schematic diagram of video driver amplifier.

In a general-purpose amplifier, this could be a moderately stringent requirement; however, in this instance, the amplifier load is integrated on the LSI wafer in proximity to the amplifier and consists essentially of a load capacitance of approximately 4 picofarads on the load side of the 1:128 multiplexer. The amplifier design thus does not involve any significant problem.

The FET devices in the 1:128 multiplexer must commute in 0.5 microsecond and must provide a resistance low enough to charge the 4-picofarad capacitance within that time. If a time constant of 0.1 microsecond is chosen (such that the capacitance should charge 99 percent of its final value), the FET resistance in the conducting state can be as high as 25K ohms, which is a very practical value for this kind of device. The series FET's commute at the television line rate: 32 microseconds ON and 32 microseconds OFF which is an easy requirement.

The line driver amplifier serves to buffer the amplifier and thereby prohibits the 4-picofarad storage capacitor from being discharged significantly by the capacitance of the column buses. The driver amplifier is a simple source-follower circuit, and can be designed to maintain the slew rate of 10 volts per microsecond required to provide the 3-microsec charging time for the column buses.

Timing Circuits

Timing circuits are required to coordinate the sampling, the transfer of data, and the enabling of row buses on the display. Control of the data to the proper storage capacitor location and transfer of the data to the display is accomplished with two 64-bit, parallel-output, shift registers and a synchronized flip-flop for the output line select function. The clock rate on the shift registers is only 2 MHz, due to the bandwidth reduction allowed by the 16-channel parallel input. In operation, a single control bit is loaded into one shift register at the beginning of a line (triggered by a sync signal from the scan converter) and shifted down the register at the 2-MHz rate. Each of the 64 shift register outputs is amplified to approximately a 30-volt pulse and applied to a FET gate to control the sample switching on the corresponding video channel. As the control bit is clocked through to the end of the shift register, the data from each of the video channels is accumulated in a

form equivalent to a single line on the display. At the end of the data block for each line, a "line-select" flip-flop switches, commanding 1024 FET gates to connect the storage capacitors (in the sample-and-hold circuits having just been addressed) to the buffer amplifiers. The complementary set of 1024 FET's used for the alternate lines are all commanded to disconnect the video voltages corresponding to the elements in the prior line from the buffer amplifier, and a signal is sent to step the sweep shift register by one display line. A single control bit is then loaded into the second 64-bit shift register and clocked along to sample and to hold the succeeding line of video. This process continues, alternating, as the row addressing circuits scan down each of the odd lines of the display until a field on the display module is formed. Then, as in conventional television interlace scanning, the row addressing circuits return to the top of the display and scan down to display each of the even lines of the frame for the interlaced field. This cycle, which produces one frame of data display, is repeated for consecutive frames.

3.2.4 Wafer Fabrication - Feasibility Analysis

An essential part of the baseline design and one without which it could not function, is the fabrication of the electrical circuits and the electrode array on the same semiconductor substrate using compatible LSI techniques. To establish the feasibility of the proposed baseline design, the following areas of the proposed fabrication technique were examined: (1) the state-of-the-art of silicon MOS FET construction and (2) the status of the Hughes experimental LX display developed under the company-sponsored IR&D program.

State-of-the-Art

Silicon MOS FET device art is well established. A wide variety of MOS FET LSI circuits are currently being manufactured in production quantities by Hughes and others, which have demonstrated characteristics equal to those required by the SAR LX display subsystem. Furthermore, industry predictions indicate that MOS LSI Technology will predominate in future semiconductor industry markets. The latter is important, in that tooling and processing techniques, developed in support of MOS FET LSI device production will be available to the LX display program which could not be practically or economically developed for that program alone.

Device Complexity. An estimate of the feasibility of the proposed design can be had by comparing the number of active devices that need to be fabricated on a single chip for the SAR LX display to the number of active devices that are currently being fabricated on a single chip as part of existing LSI designs. The baseline display design initially calls for a module containing 128 by 128 pixels, representing approximately 16,000 total active devices. Examples of relevant existing LSI designs are: (1) a 1024 bit shift register containing approximately 7000 active devices, under routine production at the Hughes MOS facility, Newport Beach, Ca.; (2) A 4096 bit random-access-memory containing approximately 12,000 active devices that is commercially available from American Micro Systems, Inc.; and (3) any of the sophisticated electronic desk calculator computational units containing 10,000 or more active devices which are in volume production in the USA and in Japan. Thus, it is not unreasonable to anticipate that display chips containing approximately 16,000 devices can be fabricated using MOS FET technology with process yields that will permit the limited production of engineering model displays to be practically achieved.

Device Size and Density. An additional estimate of the feasibility of the proposed design can be had by comparing the size and density of the chips for the proposed display with those currently being fabricated. The proposed design initially calls for chip dimensions that are: 1.28 x 1.28 inches (1.6 sq. in.), with 10,000 devices per square inch. This is an easy requirement compared to current LSI production designs which although on very small chips, achieve far higher densities. For instance, the desk calculators utilize the largest chips currently under production, 0.2 x 0.3 inches maximum (0.06 sq. in.), with device densities of approximately 200,000 devices per square inch. A typical large logic chip is 0.130 x 0.130 inches (0.017 sq. in.) with densities of 500,000 devices per square inch, while smaller logic chips have achieved 1,000,000 or more (with charge coupled methods) devices per square inch. The baseline design requires chips that are far larger in area but much lower in density, thus, it is reasonable to anticipate that display chips of the required size and density can be fabricated with adequate yield.

Experimental Display. Hughes Aircraft Company, on a company-sponsored IR&D program, is currently fabricating semiconductor wafers for an experimental 100 x 100 matrix array display. The experience gained in fabricating these wafers is directly applicable toward estimating the feasibility of the baseline design, because the basic circuits are identical. Each of these wafers contain 10,000 individual FETs, capacitors, and electrodes, that have been fabricated using MOS J-SI techniques. At the present time, only a few hundred wafers have been processed; however, an acceptance level of eight percent defects and a yield of approximately three percent have been achieved. This is a very low defect level considering the early stage of the process development. Therefore, it is feasible to anticipate defect levels of a fraction of one percent when mass production of these wafers commences.

3.3 Illumination and Viewing

The electro-optic behavior of a liquid crystal material in a reflective display causes light that is incident to the display to be modulated proportional to the strength of an external electric field. Specular reflection occurs in the absence of the electric field and when the electric field is present diffuse reflection occurs up to a maximum value of 20 percent of the incident light. Shades of gray are directly proportional to the amplitude of the input signal used to create the electric field. Thus, the observer sees the brightness of the display increase as it is driven to scatter more and more of the incident light into diffuse reflection. The foregoing is most useful, when the incident light and the display viewing angle to the observer are carefully arranged to cause the scattering to be pronounced.

For lack of a specific installation requirement at this time, the feasibility analysis is confined to a discussion of generalized illumination and viewing conditions. Final optimization of the scattering effect is highly dependent upon the geometry of specific installations but certain guideline criteria prevail which may be applied to any specific situation. Since the display is reflective and is operated by the modulation of incident light, a sunlight ambient has been assumed for daytime operation and artificial lighting has been assumed for nighttime or adverse weather operations.

The following discussion describes possible configurations of the display for use under natural and artificial lighting. In this context, several possible general configurations of lighting and light traps are introduced and the discussion concludes with a set of guidelines to be observed in the design of particular illumination systems.

3.3.1 Lighting Under Natural Sunlight

Liquid crystal displays have exhibited very high brightness and contrast under conditions in which an intense light is incident on the display surface and a light trap is used to absorb the specular reflections from that source to make the non-excited areas appear dark. Because the position of the sun relative to an aircraft is completely variable, as are any intervening clouds or atmospheric effects, the design becomes one of configuring the display to make maximum use of the sunlight for any aircraft altitude or atmospheric condition.

The first consideration in designing for a specific installation is in the choice of the display surface orientation. Ideal lighting and viewing conditions are illustrated in Figure 19. Here, the display is tilted upward away from the normal, by an angle ϕ that is chosen to provide maximum reception of the light from activated portions of the display.

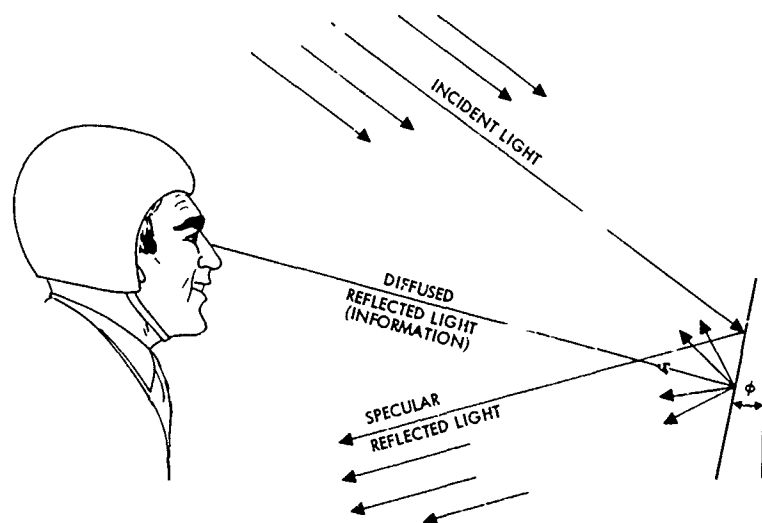


Figure 19. Ideal lighting and viewing.

Orientation alone is not sufficient to provide optimum viewing, as Figure 20 indicates. Here, sunlight incident on the pilot's clothing is scattered diffusely and a significant fraction is scattered forward into the surface of the display where it is redirected to the pilot's eye. The effect is most pronounced when flying toward the sun.

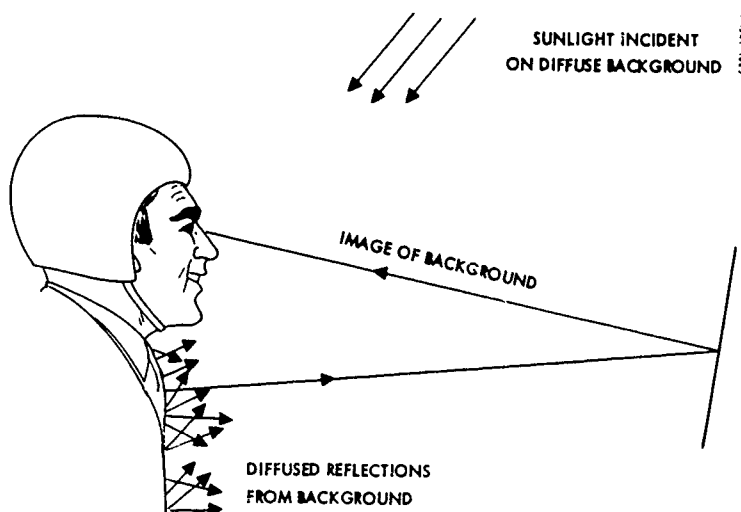


Figure 20. Effect of lighted object in reflected field of view.

This condition is common to other classes of cockpit displays as well, CRTs, alphanumeric readouts, and flight instrument faces, for example. An effective technique for combating this kind of unwanted image for the CRT or other glass covered displays has been to provide an antireflection coating or roughening treatment to the first surface of the display, thus diffusing the unwanted image to a greater extent than the primary one. The primary image is in proximity to the treated surface and hence is largely unaffected. This solution is a good one for a light emitting mechanism like a CRT phosphor, but for the LX display which is reflective, the first surface treatment would interfere with the incident light which the display must operate on.

Increasing the display angle ϕ will help, but as soon as the process is carried far enough to eliminate the unwanted reflection of the pilot an unwanted image of the canopy and sky background will come into view.

A good solution to combat the foregoing, is the light trap. Originally designed for use with the CRT, it is equally applicable here and a practical implementation appears in Figure 21. It is arranged so that the first surface reflection seen by the observer, is always the image of the light trap. The light trap is shown as a thin opaque member with the thin edge on or near the pilot's visual axis to present a minimum aspect of interference with his normal forward vision. An alternate mechanism for providing the required light trap function is shown in Figure 22 where an even greater field of view is provided. This mechanism involves the concept of micro-louvers, which are very closely spaced light baffles in a plastic sheet (manufactured by 3M). They allow light transmission through a controlled angular field. A typical microlouver sheet, which may be 0.020 inch thick, has very thin absorbing or reflecting layers spaced approximately 0.010 inch apart. The angular field through the sheet is therefore restricted to 50 degrees. A sheet of this material with the louvers fabricated at an angle to the surface can be placed in the area requiring a light trap. The louvers are placed at an angle allowing full forward visibility but blocking the direct downward sunlight onto the display, thus preventing it from reflecting into

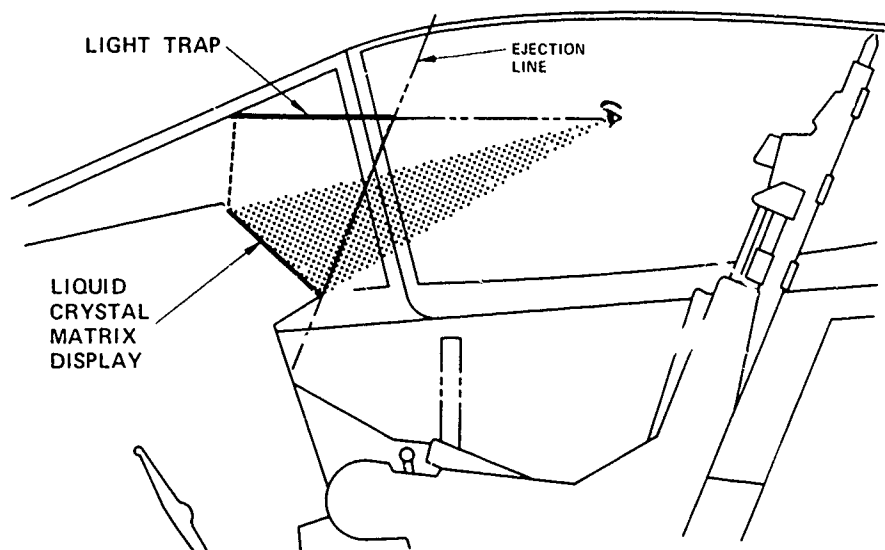


Figure 21. Conceptual idea - cockpit installation using a nonlouvered light trap.

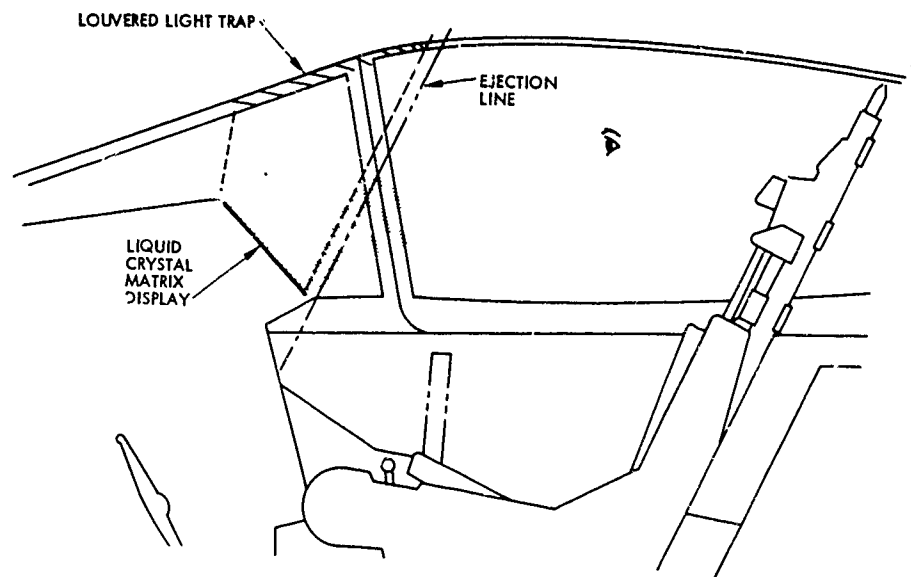


Figure 22. Conceptual idea - cockpit installation using overhead louvered light trap.

the observer's eye. This orientation allows viewing of the display under daylight conditions with the sun in a wide range of relative positions to the side, overhead, aft, and slightly forward.

Utilization of solar illumination may also be enhanced by tilting the display downward and modifying the light trap and light entrances. Figure 23 shows a possible orientation of the display surface with a light trap design using a microlouver filter similar to that used in the tilt-up design. In this instance, the louvers are angled upward by approximately the depression angle of the line-of-sight. Incident light or reflected scattered rays may pass through the louvered sheet if they fall within the designed acceptance cone of the sheet. However, the spectral reflection off the display surface strikes the absorbing (black) microlouver area and is not seen. A circular polarizer may be used in this application to absorb the unwanted specular reflections. In addition, a microlouver sheet with reflective louvers is included above the display surface to reflect sunlight when facing the sun. Some degree of diffusion may be desirable to provide more uniform illumination on the display surface or it may be determined that a simple diffuser is adequate. Specific design constraints established by particular cockpit installations are required before more definitive details are included.

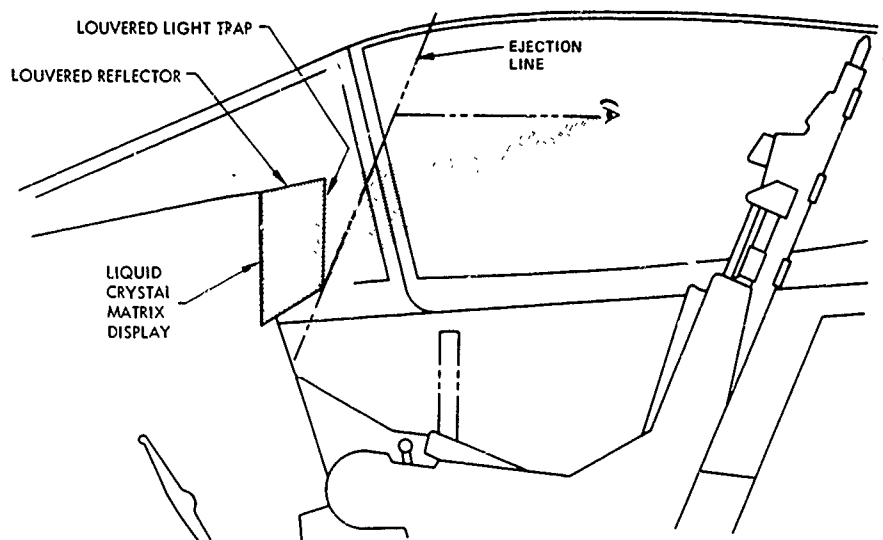


Figure 23. Conceptual idea - cockpit installation using front louvered light trap.

In installation, the display may use sunlight for display illumination only during most daytime operations with artificial lighting required for general, full-time utilization.

3.3.2 Artificial Lighting of the Display

It has been established that under unfavorable natural lighting conditions, artificial lighting is required. The worst condition - that of a completely shadowed display surface observed under high sky brightness with accommodated eyes - is experienced when flying into the sun in a clear sky. The required lighting to reinstate good display visibility under this condition is estimated at 200 watts. The most likely configurations for this kind of lighting system include (1) an over-the-shoulder projection system, (2) a side console projector and mirror, and (3) an edge-lighted system.

The over-the-shoulder projection provides an optimum method for the liquid crystal light scattering mechanism. High optical efficiency is achieved because light enters the display surface at an angle close to the normal; thus, the peak scattered light intensity pattern is directed back in a direction close to the observer's line of sight. A disadvantage to this configuration is the possible added installation complexity and possible manual interference with the projected light beam; however, it is quite similar to cockpit instrument

flood lighting which has evolved to cope with this kind of illumination requirement very efficiently by providing dual over-the-shoulder sources.

A third method (lighted-edge) represents a possible approach to avoid the complexities of the projection system. It is a somewhat more elegant method, albeit unproved. The edge lighted system, Figure 24, injects a collimated slit of light into the edge of the cover glass at greater than the critical angle to provide total internal reflection at each front surface reflection. Specular reflections from the front surface of the cover glass and from the rear mirrored surface of the liquid crystal cell propagate across the display to illuminate the entire surface nearly uniformly. Light scattered in the region of an activated liquid crystal display element strikes the front surface at less than the critical angle and, upon exit, is viewable. The anticipated problem with this form of lighting is the shadowing caused by several elements scattering light in one area that effectively block the illumination of elements farther along the panel. However, because the panel would be illuminated from both sides and because the light is not collimated along the direction of the slit, this may not be a serious problem. Also, practical implementation of the technique will require multispectral, multi-layer coatings to match the cover glass to the index of the liquid crystal material.

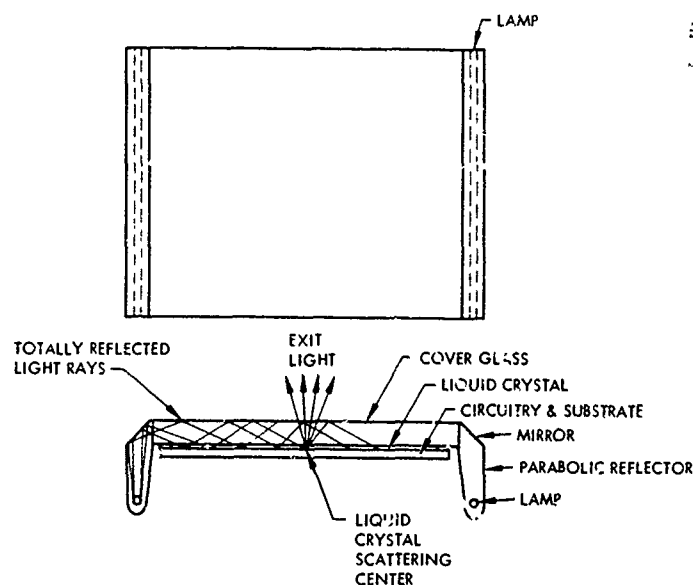


Figure 24. Edge lighting configuration of liquid crystal display.

The lamp itself could be a filament or a long arc lamp with a parabolic cross-section reflector extending the length of the display edge. Such a lamp should be fairly efficient and should occupy only a small volume of panel space. Further effort is required in the determination of scattering properties and viewing angle of this configuration; also, an optimum injection angle will need to be determined. A design tradeoff to be considered is the scattering efficiency for the desired viewing angle (presumably maximized with light striking the front surface at the critical angle) as opposed to minimized shadowing (presumably by injection at shallower angles).

3.3.3 Summary Guidelines

Although a specific design is not suggested at this time, these guidelines have been established to be used in designing display subsystems for specific aircraft installations.

- Display is to be positioned so that observer always sees a specularly reflected image of a dark light trap.
- Optimum illuminating angle is normal to the surface of the display.
- Optimum viewing angle is as close as possible to the angle of reflection of the specular incident illumination.
- Illumination for optimum viewing is a collimated light source.

Artificial illumination is required for night viewing and may be required under certain daytime viewing conditions such as viewing against the sun or under adverse weather.

3.4 Fabrication Costs

In the long term, when large-scale production of LX modules routinely occurs, the LX display approach for SAR should be less expensive than present day CRT indicator subsystems. For the near term, however, such is not the case. With any new approach there are start-up costs associated with tooling and yield factors associated with learning new process techniques that will make the engineering models and those units that are constructed under limited-production more costly than existing SAR displays.

3.4.1 Cost Projection

A meaningful cost projection for devices fabricated in production can be given by analyzing similar previous developments. Once the basic technology is defined and a program plan is established, parallel lines can be drawn to analogous or corresponding projects.

Typical cost development curves are shown in Figure 25 for a bipolar circuit and two MOS LSI circuits. A similar trend for all curves is very obvious. Although only three examples have been selected, they are representative and many more with the same characteristics could be shown. What Figure 25 really shows is that, for example, where a MOS multiplexer initially was sold for \$45.00, three years later it cost about \$10.00, representing a reduction by a factor of more than four in a relatively short time. Such a reduction is mainly due to the technological progress production experience and competition.

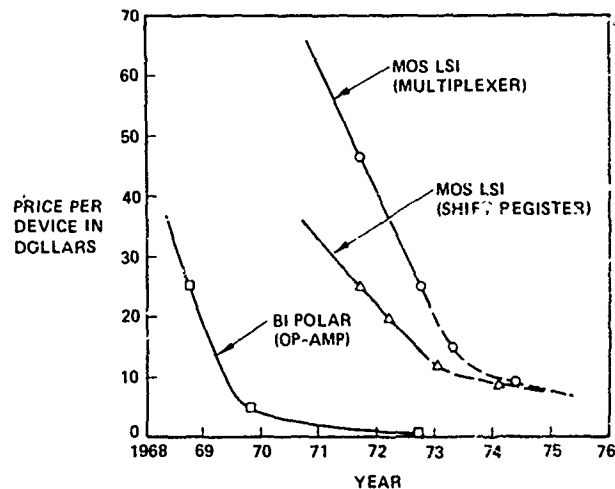


Figure 25. Trends of actual device cost.

Two of the major factors that determine the manufacturing cost of the display are the wafer processing costs and the wafer yield. The yield reflects how many of the processed devices are acceptable; the more there are, the lower the price. Figure 26 shows two processes that are related the closest to the process used for the matrix array. The solid lines represent actual numbers. It is assumed that the matrix array curve has a similar

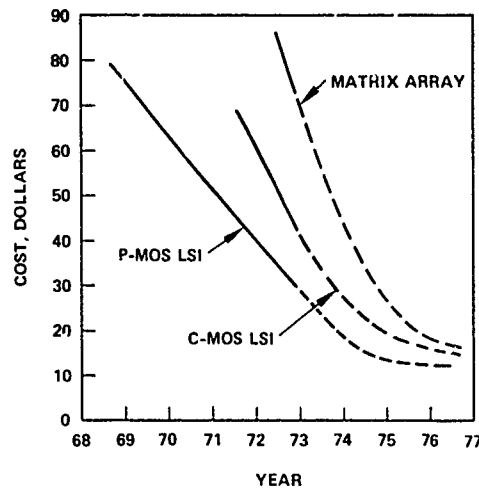


Figure 26. Wafer processing projection.

trend. This assumption is based on the fact that the technologies involved are almost identical and that the project does not rely on future inventions.

3.4.2 Electrode Array Chip Modules

The present wafer processing cost for an electrode array chip (with one chip per wafer) is approximately \$80.00. In three years, the cost will be down to about \$20.00. During the same period, the wafer yield will increase, as shown in Figure 27, where the present yields of a vidicon

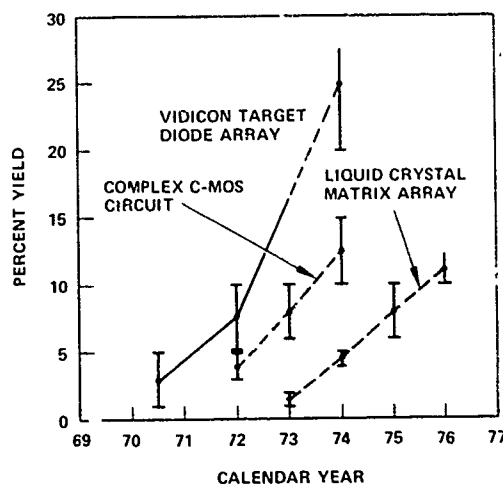


Figure 27. Wafer yield projection of device fabrication costs.

diode array and a complex C-MOS circuit are indicated by the solid lines. These circuits have a close resemblance in complexity to the matrix array. The vidicon target, for example, consists of a whole wafer containing more than 9×10^6 diodes in which a maximum of 5 leaky diodes can be tolerated.

Again, we assume that the yield curve of the matrix array will follow the other two curves. Starting with a very low yield, 1976 should show conservatively a 10 percent increase. In other words, at that time 10 wafers will have to be processed in order to get one good array, getting the cost per good wafer down to approximately \$200.00.

3.4.3 Drive Circuit Chip Modules

The cost of the necessary drive circuits are listed in Table 2 as part of the total display cost. There are two different types of circuits. One type is for the video addressing which consists of a multiplexer, an analog memory and an output amplifier. The other circuit supplies the enable pulses to the gate lines and is basically a shift register with output drivers. Both circuits are larger in area than current state-of-the-art MOS LSI circuits but lower in total device count. The initial costs are therefore higher but the cost development will follow closely the one of the presently manufactured circuits.

Assuming a conservative yield figure, the two circuits will cost in 1976, \$60.00 and \$45.00, respectively. Mounting and connecting is not included in these numbers. For the 500 line array, there are a total of 16 video circuits and a total of 16 gate line circuits necessary (assuming 64 bits per circuit).

3.4.4 Assembly Costs

Assembly costs include providing a mounting surface for physical rigidity, electrical interconnection, filling and sealing the display. These costs are estimated at approximately \$500 for a small display in production; they increase in proportion to the size of the display because the economies of scale are offset by the additional care required in assembling a larger display.

TABLE 2. PRODUCTION COST COMPARISON

	Liquid Crystal Display	CRT Display
500 Lines	Electrode Array Chip Modules (9) Video Drive Chip Modules (16) Sweep Drive Chip Modules (16) Display Assembly Support Equipment \$ 3,000 to \$ 7,000	CRT Video Deflection High Voltage \$ 3,000 to \$ 7,000
1000 Lines	Electrode Array Chip Modules (36) Video Drive Chip Modules (32) Sweep Drive Chip Modules (32) Display Assembly Support Equipment \$10,000 to \$20,000	CRT Video Magnetic Deflection Dynamic Focus High Voltage \$ 5,000 to \$10,000
1500 Lines	Electrode Array Chip Modules (100) Video Drive Chip Modules (48) Sweep Drive Chip Modules (48) Display Assembly Support Equipment \$20,000 to \$30,000	Multibeam CRT Multiple Video Amps Magnetic Deflection Dynamic Focus Dynamic Astigmatism Regulated High Voltage Regulated Low Voltage \$15,000 to \$20,000
NOTES: * A larger electrode array is assumed than is proposed for the experimental baseline design		

3.4.5 Support Equipment

Support equipment includes power supplies, packaging, interface connectors, etc. The cost of the support equipment is not strongly dependent upon display size.

4.0 CONCLUSION

It has been established through analysis and through direct observation of experimental displays that a reflective liquid crystal display can be expected to achieve more of the performance objectives required by a SAR display than currently available CRTs. Furthermore, even though a new concept is involved, it has been established that it is feasible to implement the intended SAR application using a reflective liquid crystal display. Given the above, the questions still to be attacked are: (1) How will a liquid crystal display fit into the overall SAR system? and (2) what are the major developmental steps?

4.1 Recommendations

A SAR system that is configured to utilize the maximum capabilities of a reflective liquid crystal pictorial display will present high resolution synthetic array radar on board an aircraft in real time with improved performance and decreased complexity over systems that utilize CRTs. A liquid crystal pictorial display designed for application to a High Resolution Synthetic Array Radar Digital Processor (HIRSADAP) is shown in Figure 28.

4.1.1 HIRSADAP Radar

The HIRSADAP radar subsystem is a high resolution synthetic array radar incorporating digital processing. The data for the HIRSADAP system is accumulated using a radar antenna that is squinted at a fixed angle to the flight path. The radar video is stored and correlated in a special processor to improve the angular resolution over that which can be obtained from a

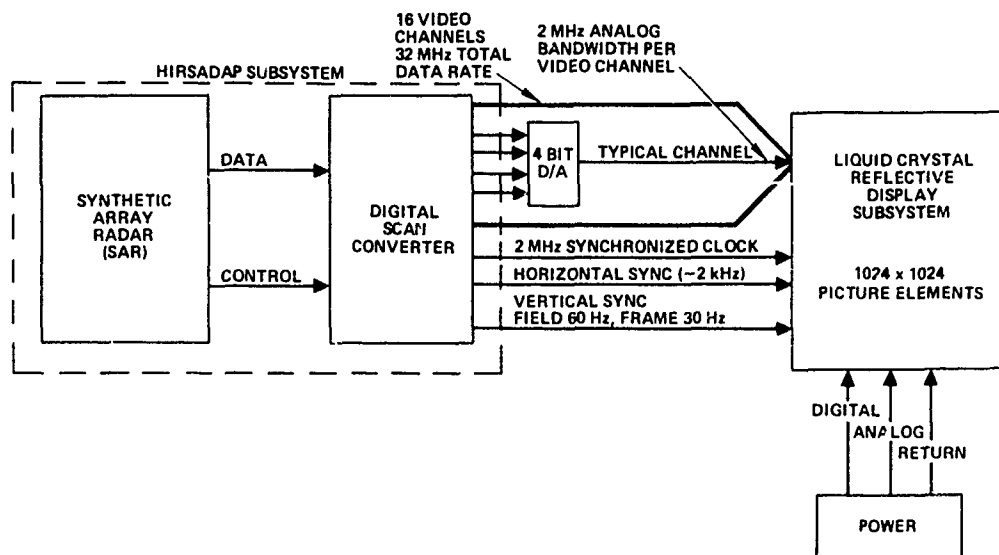


Figure 28. Block diagram of radar system.

conventional radar sensor. The data is accumulated and processed in a manner designed for display as a strip map ground segment in one of several modes. One mode presents the data as a ground map that is continuously moving down the display screen at a speed that is a function of the aircraft ground speed and the selected map scale. A snap shot or freeze mode presents the data as a ground map that is fixed relative to some specific ground coordinates and a "telescope" mode provides a zoom capability.

The single most significant item in the cost of a HIRSADAP subsystem is the data memory. The slow rate at which the data is accumulated along the ground track makes it necessary to provide storage for at least one entire frame of radar imagery. The exact size of the memory is dependent upon the resolution requirements but typically several million bits are required. The sixteen video channel interface recommended for the LX display subsystem, as shown in Figure 28, can significantly reduce the cost of this memory, for the following reasons.

The cost of a memory system, in terms of price and power consumption, is dependent upon size and speed. The use of multiple video channels reduces the speed at which the memories of the HIRSADAP system must be accessed. When several video channels are used, several sections of the

memory are read out simultaneously, thus leading to the same overall display update rate but a reduced data rate for each channel. Cost savings are possible because at the data rates involved, typically 10^7 million bits per second, the cost goes down more rapidly due to speed reductions than it increases due to circuit duplication. Moreover, further cost reductions may be possible because the use of 16 video channels, (as opposed to the limited number used with multibeam CRT displays), brings the data rate down to a level that can feasibly be implemented using LSI semiconductor circuits. The implication is that further system integration using increased numbers of LSI semiconductor circuits leads to lower costs through higher reliability, lower power, and smaller size.

4.1.2 Display

The recommended system shown in Figure 28 calls for a ten inch by ten inch display containing 1024×1024 pixels. The display would be constructed by assembling an array of semiconductor chips as shown in Figure 29. It is recommended that for the early experimental displays that each of the chips in the assembly contain 128×128 pixels; this number can be anticipated to increase to 256×256 pixels for a production display.

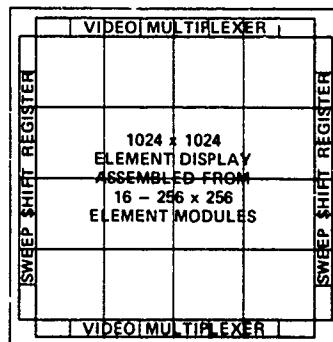


Figure 29. Assembly of LX display from semi-conductor modules.

The liquid crystal pictorial display is different from a CRT in several ways that have significant system implications, among them (1) the LX display functions as a light valve rather than as a light source and hence it must be externally illuminated, and (2) the image on the liquid crystal display is formed using an array of discrete elements.

The light valve action of the liquid crystal display is the main factor in reducing display power consumption. It is no longer necessary to have a display that can produce sufficient light power to compete directly with the sun under conditions of direct illumination; the liquid crystal display controls rather than competes with the illumination of the sun. Artificial illumination is only required when there is inadequate natural lighting as during adverse weather conditions and at night. The amount of lighting power required under these conditions is markedly less than that needed to compete directly with the sun.

The discrete elemental nature of the liquid crystal pictorial display permits a one-to-one correspondence to be established between the data presented by each picture element on the display and the data stored in the data bins of the radar signal processor. When this degree of synchronism is present, the resolution of the system as a whole is determined by the resolution of the sensor; the display does not significantly degrade system resolution.

The discrete elemental nature of the liquid crystal pictorial display furthermore results in a display that has uniform resolution over the entire display surface. The resolution in the corners is every bit as good as in the center. This effectively increases the useful area of the display over that of a CRT display of equal size, because the resolution of the latter deteriorates rapidly towards the edges.

Finally, the discrete elemental nature of the liquid crystal pictorial display results in excellent positional stability. The location of a picture element on the display is determined only by physical dimensions; it is unaffected by magnetic fields, component value drift, or power supply voltages.

4.2 Program Plans for Future Development

Schedules and plans for the orderly development of the liquid crystal pictorial display have been formulated. The intended application is as a display for a high-resolution airborne synthetic array radar system. These schedules and plans have been conceived to attack each of the major risk items in logical steps. It is suggested that the display development be continued in the phases shown on the program plan in Figure 30.

TASK/PHASE	1/2 YEAR	YEAR 1	YEAR 2	YEAR 4
CONCEPT DEMONSTRATION Demonstrate Single Wafer Display				
DETAILED DESIGN AND EVALUATION Demonstrate 3 x 3 Wafer Display				
COMPONENT FABRICATION Demonstrate 10 x 10 Inch Display				
DISPLAY REFINEMENT Flight Test Demonstration				

Figure 30. Program plan for liquid crystal pictorial display developments.

4.2.1 Concept Demonstration

The purpose of demonstrating the liquid crystal display concept is to show that it can achieve the required functional performance objectives. A concept demonstration involves building up a single wafer liquid crystal display with external discrete medium-scale-integrated (MSI) drive circuits. The concept demonstrator provides an example of the method by which the large image is formed and the performance that will be achieved.

The concept demonstration will also eliminate as a major risk area the uncertainty as to whether the liquid crystal pictorial display can meet the operational requirements of brightness, contrast, and shades of gray rendition.

4.2.2 Detailed Design and Evaluation

The detailed design and evaluation phase would be concerned with the detail design, preliminary fabrication and evaluation of the components from which the large display will be assembled. The drive circuits, previously constructed using MSI components, will have to be modified for LSI packaging. The layout of the electrode array previously demonstrated on a single chip will have to be modified for the interconnections between chips. The techniques for interconnecting chips will have to be refined to be compatible with the constraints of the liquid crystal display. Integrated spacers to insure uniform spacing between the electrode array chips and the cover electrode will need to be designed and evaluated. The detail design and evaluation phase should conclude with the demonstration of a three by three chip display. This demonstration will eliminate as major risk areas those problems associated with feeding signals to a display module that is completely surrounded by other modules.

4.2.3 Component Fabrication and Assembly

Component fabrication and assembly will be concerned with the fabrication of the required number of semiconductor chips, the acquisition of a suitable liquid crystal material, and the assembly of all components into a display. It can be anticipated that over 1000 wafers will have to be processed to obtain 96 operating chips of the three basic types that are called for by the baseline design for the 1024 x 1024 display. The acquisition of a suitable liquid crystal material will require evaluation of materials developed for other applications, analysis of the findings on parallel liquid crystal material development programs and formulation of the required quantities. Assembly of the display will be concerned with the mechanical assembly of the chips into the larger array in a manner that assures flatness and mechanical rigidity, and filling and sealing in a manner that prevents voids and contamination. The end of the component fabrication and assembly phase should be marked by the demonstration of an operational experimental 1024 x 1024 pixel, ten by ten inch, liquid crystal pictorial display.

This demonstration will eliminate as a major risk area the uncertainty connected with the ability to produce the semiconductor circuits with an adequate yield, and the uncertainty connected with the search for a suitable liquid crystal material.

4.2.4 Display Refinement

Display refinement is required to take the experimental liquid crystal pictorial display and modify it to meet the mechanical requirements for a flight test. An environment testing program will be required to ascertain the effects of pressure and vibration upon the display. A flight safety design review and inspection will be required to insure compliance with personnel and aircraft safety. Interface hardware compatible with on board signal sources will have to be built and tested. The program should conclude with a flight test demonstration of an advanced development model of a liquid crystal pictorial display. This flight test demonstration will eliminate as a major risk the uncertainty of the display meeting the required military environmental performance.

APPENDIX A. TECHNICAL FACTORS PERTAINING TO LIQUID CRYSTALS IN DISPLAY APPLICATIONS

A.1 INTRODUCTION

When some organic substances are melted, instead of becoming a clear liquid, they pass through a turbid liquid state which was termed the mesomorphic state or a "liquid crystal." The liquid crystalline state has more order in the arrangement of its molecules than the liquid state but less than the solid state.

The three principal types of LX's are nematic, cholesteric, and smectic. While the cholesteric LX's are optically active modules, the nematic and smectic LX's are generally optically inactive, (i.e., they do not rotate polarized light).

Nematic LX's consist of molecules that are parallel, resembling matches in a box. Each molecule can rotate only around its long axis and has some freedom of movement from side to side or up and down (Figure 31a). The smectic LX's have a layered arrangement. The layers can slide over one another, because the molecules in each layer can move from side to side or forward and backward but not up and down. Within each layer, molecules may be ordered in ranks (Figure 31b) or randomly distributed. The cholesteric LX's consist of layers, as smectic LX's do. Within each layer, however, the molecules are parallel, as are the nematic molecules. Molecules in one layer exert an influence on the layers above and below, so that the long axes of the molecules in these layers is displaced slightly and a helical pattern forms from layer to layer (Figure 31c).

A very important intrinsic property of LX molecules is the dielectric anisotropy, ϵ_a , which is equal to the dielectric constant ($\epsilon_{||}$) in a direction parallel to the long molecular axis minus the dielectric constant ($\epsilon_{\perp}$) at right angles to the molecular axis.

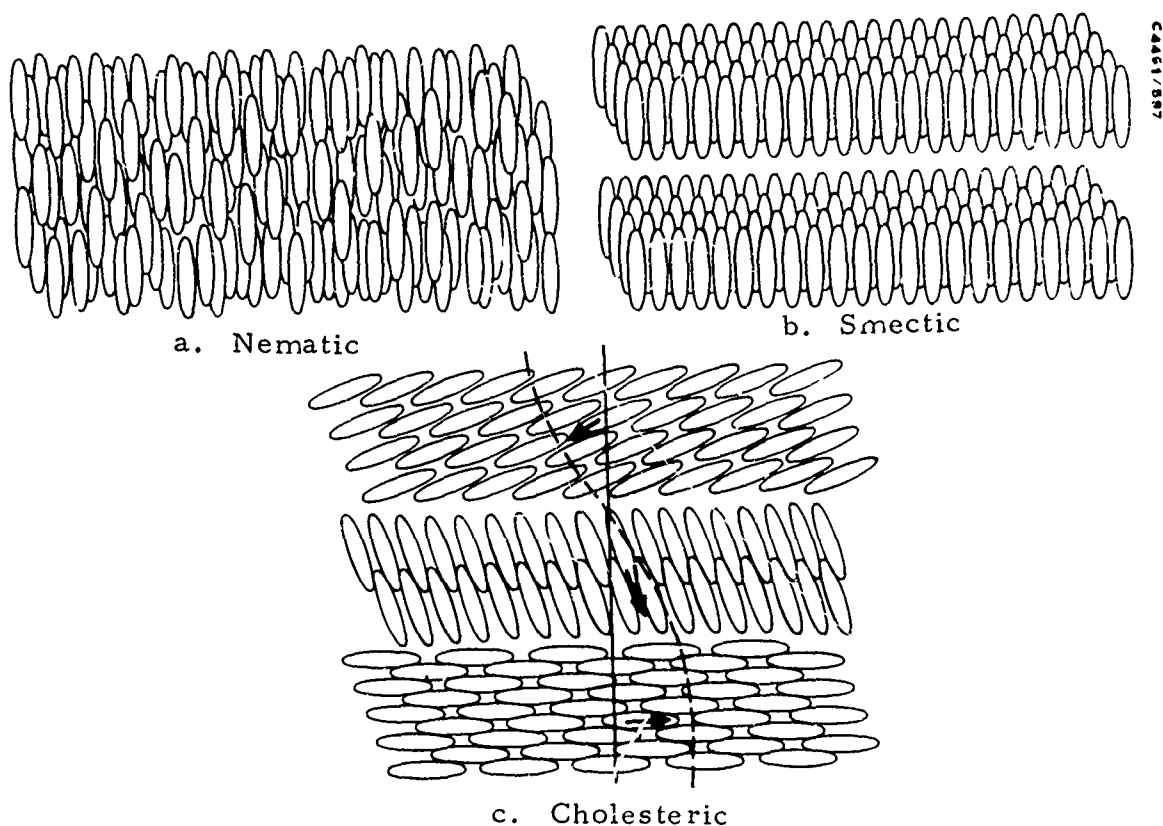
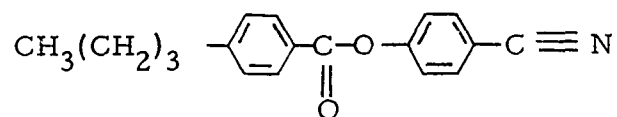


Figure 31. Diagrams of packing effects in liquid crystals.

$$\epsilon_a = \epsilon_{11} - \epsilon_1$$

When ϵ_a is positive, the molecular axis will align roughly in the direction of an electric or magnetic field, whereas when ϵ_a is negative, the molecules will orient themselves at some angle roughly perpendicular to the field. The dielectric anisotropy is a function of the vector sum of the dipolar groups in the molecule. To prepare a LX with a strongly positive ϵ_a , for example, it is conventional to introduce the strongly dipolar nitrile group at the end of the long axis of the molecule, as in



Individual properties of each of the types of LXs have been taken advantage of in making displays:

NEMATICS:	Dynamic scattering Field effects (1) Twisted Nematic (2) Birefringent color switch (3) Nematic dichroic dye interaction
CHOLESTERICs:	Reflective color displays (1) Temperature sensitive (2) Pressure sensitive (3) Chemical vapor sensitive (4) Electric field sensitive
SMECTICS:	Thermo-optic storage display
HYBRIDS:	Thermo-optic Cholesteric-nematic phase change

A.2 NEMATICS

A.2.1 Dynamic Scattering Mode (DSM)

Briefly, DSM may be characterized by electrical current - field induced hydrodynamic motion. Nematic LX's are optically anisotropic (i.e., they have different refractive indices parallel to and perpendicular to the long axes of the molecules.) The effect of applying a voltage to and passing a current through a typical LX cell is to disrupt the normally uniform molecular orientation in favor of a large number of small regions (domains) whose molecular orientation is different from those of their neighboring domains. This appears to the light passing through the cell as closely spaced refractive index boundaries. These index boundaries cause the light to be refracted at various angles (i.e., scattered). Thus, we have a system that, when no voltage is applied, appears optically homogeneous and transparent, and when voltage is applied, appears highly diffusing or scattering.

DSM can be activated by either AC or DC signals. Typically, AC frequencies less than 1 KHz are used.

A.2.2 Field Effects

Twisted Nematics

Another way to take advantage of the sympathetic alignment and the optical anisotropy of nematics is the twisted nematic configuration. The design of the twisted nematic cell is the same as for the DSM, except that the cell walls are treated to induce the LX's to align with their long axes parallel to the plane of the cell wall. Thus, on each of the cell walls the LX molecules have their long axes parallel to each other as well as parallel to the plane of the cell wall. The cell is assembled in such a way that there is an angle of 90° between the direction of the long axes of the LX's on one wall and the corresponding direction on the other wall. Calculations have shown that the orientation of the long axes of the molecules varies smoothly across the cell thickness from one orientation to the other. Hence, the name twisted nematic.

If light incident on the cell is plane polarized either along the direction parallel to the long molecular axis or perpendicular to it, the plane of polarization of the light is rotated 90° upon emerging from the other side of the LX cell. If this emergent light is viewed through an analyzer oriented parallel to the polarizer, no light is observed to pass through the analyzer. However, if a field of sufficient strength (typically a few volts) is applied to the cell, the molecules in the bulk change their alignment from parallel to perpendicular to the cell walls. As a result, no rotation of the plane of polarization of the light occurs when the field is applied. Since the analyzer is aligned parallel to the polarizer, light is now passed by the analyzer. Thus, by using a linear polarizer and analyzer in conjunction with a twisted nematic configuration, the intensity of the transmitted (polarized) light can be modulated with an electric field.

Birefringent Color-Switch

A birefringent color-switch (BCS) cell is very similar to the twisted nematic cell except that it is usually made without the 90° angle between the orientation of the long axes of the molecules. That is, the long axes of the LX molecules are aligned parallel to the cell walls and uniformly pointed in one direction throughout the cell. However, the polarizer is set so that the incident light is not polarized in the planes either parallel or perpendicular to the long axes of the molecules. The wavelength of the light passed by the analyzer is determined by the angle with respect to the polarizer and the degree of birefringence. The degree of birefringence, and therefore the color of the transmitted light, can be controlled with an electric field applied across the cell. (The projection of the index ellipsoid is dependent on the orientation of the long axes of the LX molecules.)

A twisted nematic cell can also be used as a BCS by simply reorienting the polarizer so that the plane of polarization of the incident light is neither parallel nor perpendicular to the long axis of the LX. In this configuration the expected birefringent effect is observed. That is, the plane of polarization of the incident light is rotated by an amount dependent on the wavelength of the light and the degree of birefringence of the LX material.

Guest-Host Dye Alignment

In this type of display, a pleochroic dye (a material that has different optical spectra along different molecular directions is pleochroic) is dissolved in a nematic LX. An electric field is used to control the orientation of the LX and the orientation of the dye which follows it. Hence, the name guest-host alignment.

Initially the LX and the dye are aligned parallel to the electrodes. Plane polarized light is passed through the cell with the plane of the light oriented parallel to the long axes of the dye molecules. Viewed in this manner the dye has a high absorbance. Upon application of a field the LX and its dye guest are reoriented perpendicular to the electrodes. This is accomplished by a dramatic increase in the amount of light transmitted.

A.2.3 Thermo-Optic Display

A thermo-optic display with nematic LX's has also been reported. The effect depends on thermal hysteresis. The rate of cooling from the isotropic state to the solid state determines the degree of light scattering. However, the device stores the recorded information and is not directly relevant to the requirement for dynamic detector.

A.3 CHOLESTERIC

A.3.1 Reflective Color Displays

The iridescent colors reflected from Cholesteric LX are quite striking. These colors are due to Bragg type reflections from the layers of the LX helix. The periodicity of these layers, or the pitch, determines the wavelength of the reflected light at a given viewing angle. Fundamentally, all of the cholesteric color displays operate on the same principle — change the pitch and you change the color.

Displays have been made whereby the pitch of the cholesteric LX is altered by temperature, pressure, and electric field. In addition, the pitch of the cholesteric is also sensitive to certain chemical vapors. These vapors essentially dissolve in the cholesteric and dilute it, thus changing the pitch length.

A.3.2 Thermo-Optic Storage Display

A non-colored application of Cholesteric LX's to displays can be obtained by constraining (by surface preparation) the axis of the helical structure to be perpendicular to the cell walls thus obtaining an optically clear cell. Upon heating to the isotropic phase (with an IR laser) and subsequent relaxation back to the LX phase, a light scattering state is obtained in the irradiated regions. The degree of scattering is dependent upon the rate of cooling back to the meso phase. That is, the amount of disorder "frozen in" is dependent on the rate of "freezing." The molecules relax very slowly from the disordered state (random focal conic texture) to the transparent state (Grandjean texture). This relaxation time may be reduced by the application of a high audio frequency signal (typically a few kilo-hertz).

A.4 SMECTICS

Until recently, smectics have enjoyed little but academic interest. Recently, however, smectic LX have been used in a display.

The display employs the normal light scattering properties of the smectic state. To change the appearance, the LX is heated with an IR laser, above its isotropic transition temperature. The isotropic liquid is clear (optically transparent) as expected.

A.5 HYBRID TYPES

Nematic LXs have been doped with Cholesteric materials to provide a new dimension to DSM — storage. Dissolving cholesterics in nematics produces a device that, after the DSM producing voltage is removed, has a solution with a very long relaxation time back to the normal transparent state. This relaxation rate is a function of both Cholesteric concentrates and Cholesteric structure, as well as temperature.

Nematic LX molecules initially align themselves in a helical arrangement typical of Cholesteric LX's. The pitch of the helix is determined Cholesteric concentration and structure. Upon application of a voltage suitable for DSM (DC or low frequency AC, e.g. <1kHz) hydrodynamic turbulence ensues and optical scattering is effected. After removal of the writing signal, small independently oriented domains of helical structure are formed. This is called a random focal conic structure. Again, the number and size of these helical domains is dependent on the Cholesteric concentration and structure. It should be noted here that due to their independent orientation these domains form a light scattering state.

This state is governed by the rate of coalescing of these domains to eventually form a single domain. Application of a high frequency signal (frequency greater than a few kilohertz) decreases the time for this coalescing to take place.

The time scale for relaxation from DSM back to transparent state, without a high frequency erasing signal, can be from fractions of a second to months. However, the application of an erasing signal can convert these time scales to a matter of a few tens of milliseconds to a few seconds.

APPENDIX B. ELEMENTAL ADDRESSING CIRCUITS COMPUTER SIMULATION AND ANALYSIS OF FEASIBILITY

B.1 BACKGROUND

A matrix array for a flat-panel liquid crystal display incorporates a circuit diagram similar to that shown in Figure 32, where multiple video signals are presented on each of the columns. The image is formed by sequentially loading the video information into rows 1, 3, 5, 7, . . . , then rows 2, 4, 6, 8, . . . , a row at a time with the whole process being repeated at 30 Hertz.

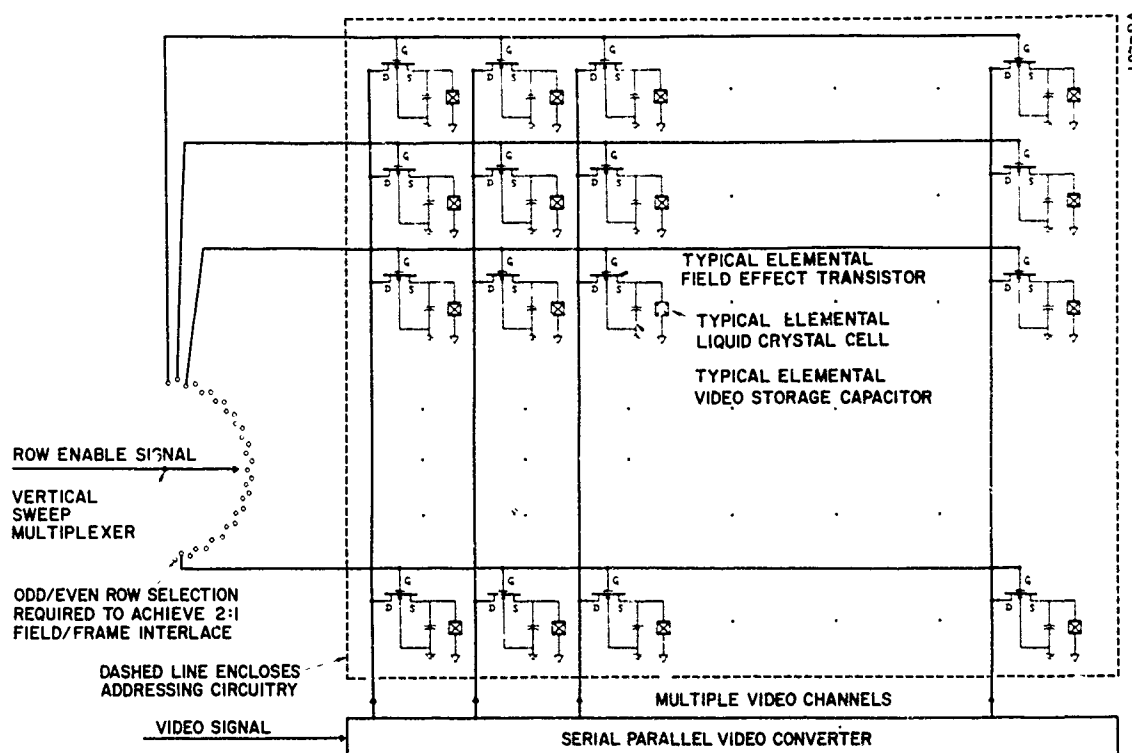


Figure 32. Schematic diagram of line-at-a-time addressing circuit.

Associated with each element is a field-effect transistor to serve as a switch, and a capacitor to serve as intermediate storage of the video signal level; together, they provide a sample-and-hold circuit at the intersection of each row and column. The FET switch is used to sample the level of the video signal during the time interval in which the line is enabled, and the capacitor holds the value till the liquid crystal material reacts to the change in applied potential. The ON resistance of the transistor switch determines the speed with which the potential on the capacitor can be changed. The OFF resistance determines the length of time for which this potential can be maintained. The OFF/ON resistance ratio determines the crosstalk between the elements — and therefore the maximum contrast — that can be achieved in a display.

B. 1. 1 Approach

The problem was attacked by approximating the electrical circuit of the elemental liquid crystal cell with an equivalent circuit and by approximating the electro-optical response of the liquid crystal as a linear flow problem.

The basic technique for solving problems of this type on a digital computer is by using the state-space approach. The applicable differential equations are expressed in finite-difference form, and then the computer performs a summation. For example, in the method used to compute the potential on the capacitor shown in Figure 33 as a function of time after the switch is closed, the differential equation that describes the circuit is

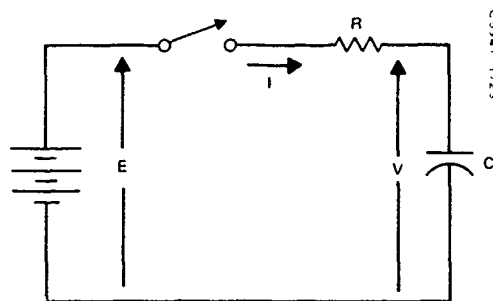


Figure 33. Schematic diagram of capacitor charging circuit.

$$I = \frac{dQ}{dt} = C \frac{dV}{dt} = \left(\frac{E-V}{R} \right)$$

or

$$\frac{dV}{dt} = \frac{1}{RC} (E-V)$$

This equation expressed in finite-difference form is then

$$\Delta V = [(E-V)/RC] \Delta t$$

and the voltage across the capacitor therefore becomes

$$V = \int_{\tau} \left[\frac{dV}{dt} \right] dt = \sum_{\tau} \Delta V = \sum_{\tau} [(E-V)/RC] \Delta t$$

B. 2 SIMULATION

This simulation required that assumptions be made with respect to the data input mechanization, the number of resolution elements, the FET source-to-drain resistance, and the electro-optical transfer characteristics of the liquid crystal material. The simulation looked at the contrast between two adjacent elements, one of which is addressed when the video signal is maximum, or white, and the other when the video signal is minimum, or black (see Figure 34). For each set of initial conditions, the relative voltages across the elemental liquid crystal cells were computed as a function of time. These, in turn, were used to compute the relative numbers of scattering centers formed by the liquid crystal material, which permitted determination of the contrast. The equivalent circuit used in the computation is shown in Figure 35.

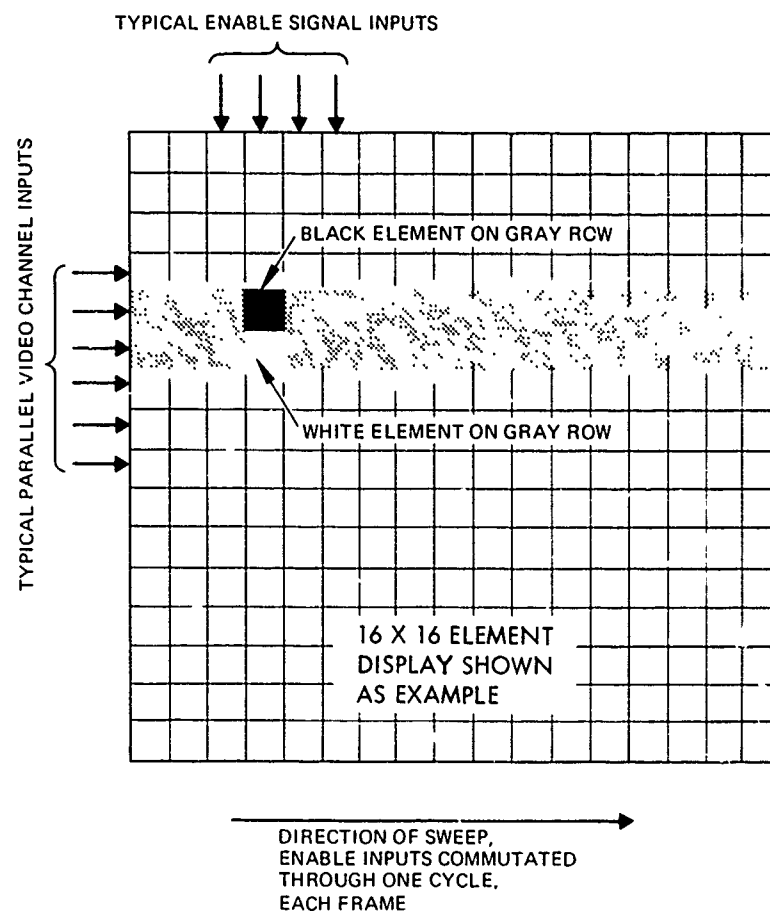
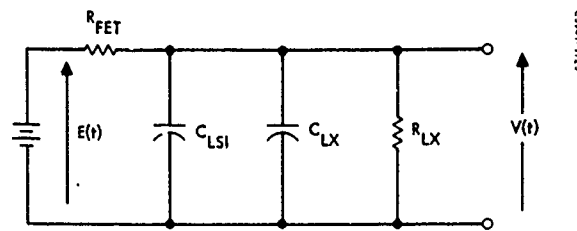
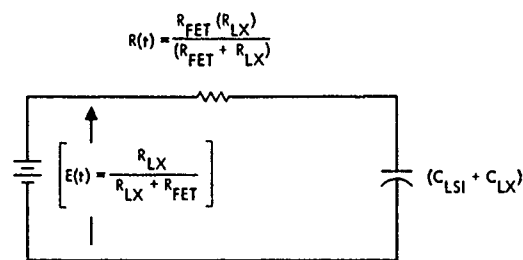


Figure 34. Formulation of contrast equation.



a) BASIC COMPONENTS



b) LUMPED EQUIVALENT CIRCUIT

Figure 35. Equivalent circuits of elemental cell.

The resistance of the FET is time dependent, and R_{FET} is taken as R_{ON} during the ON portion of the cycle, and as R_{OFF} during the OFF portion of the cycle. Likewise, the applied voltage, $E(t)$, changes between the ON and OFF portions of the cycle.

The video signal for the white element was assumed to be equal to 1.0 when the FET was ON and 0.5 when the FET was OFF. A video signal of 0.5 volts approximates the average video signal for an image with a random intensity distribution. The black case was not computed because it is merely the complement of the white case. In the first instance, the elemental capacitor is charged from a potential source equal to 1.0 volt through a resistance of R_{ON} for period of t_{ON} and is discharged toward 0.5 volts through a resistance of R_{OFF} for the period of $(P - t_{ON})$, where P is the frame period. The parameter t_{ON} was assumed to be equal to $1/1000^{th}$ of P , which is consistent with the goal of a 1000-line, line-at-a-time addressed display.

The iteration step size, Δt , was chosen to be short compared to the time constant of the circuits. The values chosen were $\Delta t = P \times 10^{-6}$ during the ON interval, $\Delta t = P \times 10^{-4}$ during the time interval from $0.001 \times P$ to $0.01 \times P$, and $\Delta t = P \times 10^{-2}$ during the balance of the period. This step size was found to give results consistent to three significant figures. At each step, the voltage on the capacitor was computed using the equation derived in the earlier example, except that E and R were charged periodically to reflect the changes in circuit parameter during the ON and OFF cycles. R_{OFF} was assumed to be 10^{10} ohms.

The number of scattering centers formed in the liquid crystal material was computed by numerical integration of the differential equation

$$\frac{dN}{dt} = SV - \frac{N}{T_0}$$

where:

N = density of scattering centers

S = sensitivity factor

V = applied voltage

T_0 = decay constant

This expression describes a process in which scattering centers form and disappear by an unspecified linear mechanism. It assumes (1) that the rate at which the centers are formed is proportional to the product of a sensitivity factor and the applied voltage and (2) that the rate at which they disappear is proportional to the density of scattering centers that are present divided by some decay constant. It has been found that this equation generally predicts the experimentally observed results except for scattering-center densities below the threshold value and above the saturation value. Although it was unnecessary for this simulation, the equation can be modified to include these effects. In the simulation, the sensitivity was defined to be unity and the decay time, T_0 , was 1/30 second. The sensitivity can be chosen arbitrarily when all scattering-center densities are expressed as a normalized ratio.

The solutions of these equations are plotted in Figure 36. The plot of the potential across the elemental capacitor oscillates back and forth as it gradually approaches the steady-state condition; also, the plot of the density of scattering centers has a similar shape. However, its variations are smaller and have a longer time response. The contrast between the two hypothetical cells was computed for various combinations of variables, OFF/ON resistance ratio, and RC time constant using the equation:

$$\left(\frac{\text{scattering density in ON cell} - \text{scattering density in OFF cell}}{\text{scattering density in OFF cell}} \right)$$

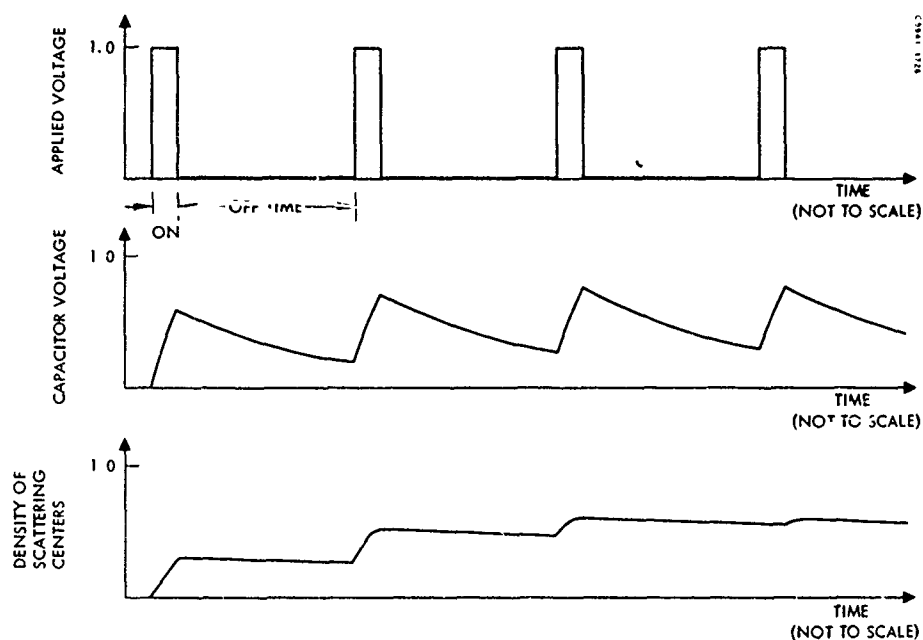


Figure 36. Graphical presentation of equation solutions as functions of time.

B.3 RESULTS

Data obtained from a series of computational runs are plotted in Figure 37. The contrast predicted for the postulated model is plotted as a function of the charging time constant, normalized to the length of the

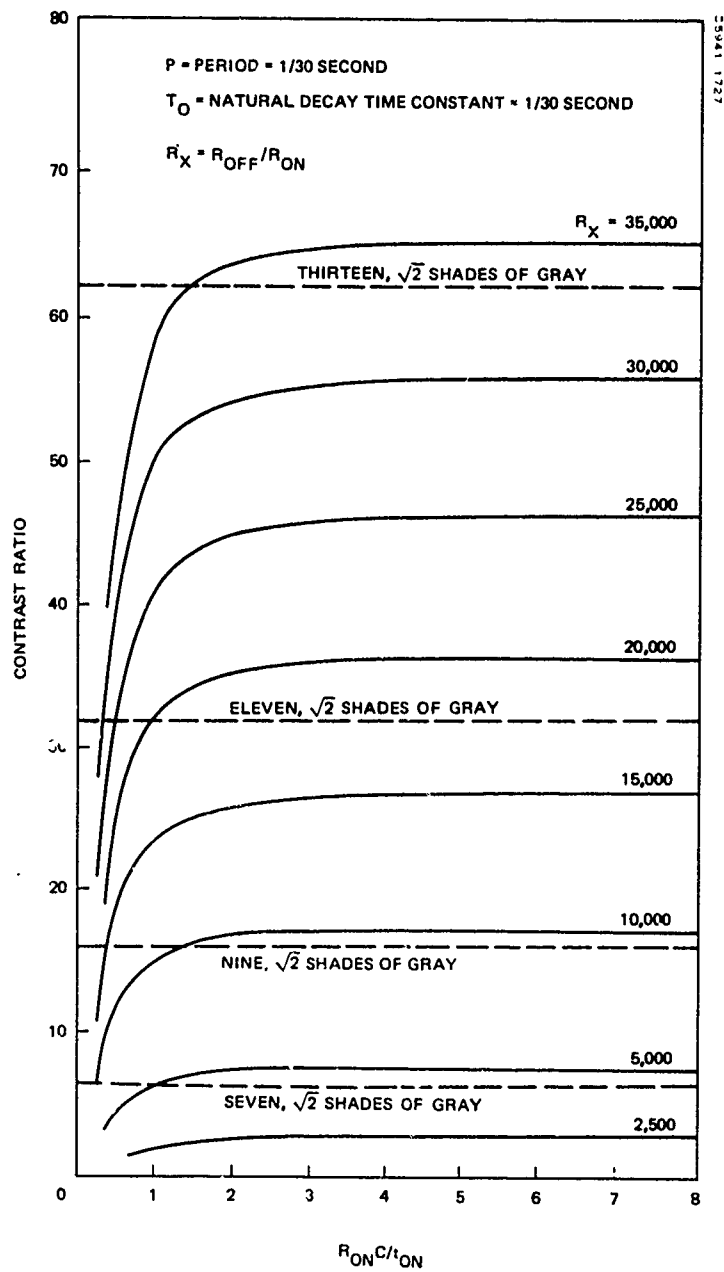


Figure 37. Contrast as a function of OFF/ON ratio.

Thus, in as much as OFF/ON resistance ratios of greater than 10^4 can routinely be achieved using silicon LSI technology, and that a capacitor of greater than 8 pfd can be routinely fabricated in the available space using the same technology, it is concluded that it is feasible to anticipate that the required electrical performance can be achieved from the proposed baseline design.

Thus, in as much as OFF/ON resistance ratios of greater than 10^4 can routinely be achieved using silicon LSI technology, and that a capacitor of greater than 8 pfd can be routinely fabricated in the available space using the same technology, it is concluded that it is feasible to anticipate that the required electrical performance can be achieved from the proposed baseline design.

UNCLASSIFIED

Security Classification

DOCUMENT CONTROL DATA - R & D

(Security Classification of title, body of abstract and indexing annotation must be entered when the overall report is classified)

1. ORIGINATING ACTIVITY (Corporate author)		2a. REPORT SECURITY CLASSIFICATION Unclassified
		2b. GROUP -
3. REPORT TITLE A Study of the Application of Reflective Displays to Synthetic Array Radar		
4. DESCRIPTIVE NOTES (Type of report and inclusive date) Final Report April 1972 - April 1973		
5. AUTHOR(S) (First name, middle initial, last name) Ernstoff, M.N. Winner, R.N.		
6. REPORT DATE April 1973	7a. TOTAL NO. OF PAGES 78	7b. NO. OF REFS
8a. CONTRACT OR GRANT NO. F33615-72-C-1415	9a. ORIGINATOR'S REPORT NUMBER(S) AFAL-TR-73-155-	
b. PROJECT NO 7662	9b. OTHER REPORT NO(S) (Any other numbers that may be assigned this report) P73-156R HAC Ref. No. C5941	
c.		
d.		
10. DISTRIBUTION STATEMENT Distribution limited to U.S. Government agencies only; test and evaluation; April 1973. Other requests for this document must be referred to AFAL/NVT, Wright-Patterson AFB, OH		
11. SUPPLEMENTARY NOTES		12. SPONSORING MILITARY ACTIVITY Air Force Avionics Laboratory, Air Force Systems Command, Wright-Patterson Air Force Base, Ohio
13. ABSTRACT The purpose of this study was to establish the performance requirements for an airborne synthetic-array-radar (SAR) display and investigate the feasibility of meeting these requirements with a reflective display mechanization. A reflective liquid crystal display was chosen as the baseline mechanization to be evaluated with respect to its operational performance, fabrication feasibility and cost effectiveness. A set of performance requirements were established from psycho-physical considerations that would provide for the transfer of the maximum amount of information that can be realistically used in the named application. They are: size, 10 by 10 inches; resolution, 1024 by 1024 pixels; contrast ratio, 64 to 1 under 10,000 ft. C. ambient (13 shades of gray); reflectance, 20 percent of lambertian surface. The baseline liquid crystal display is fabricated by sandwiching a thin layer of liquid crystal material between a transparent planar conductive electrode and a large semiconductor wafer. Prior to assembly, an X-Y addressed matrix array of transistor-controlled reflective-electrodes is formed in and on the surface of the semiconductor wafer. An image is formed on the display by programming the brightness of each picture element in an appropriate manner. Picture element brightness is dependent upon the reflective characteristics of the dynamic scattering liquid crystal material in contact with the elemental electrode and the ambient illumination. A SAR display system mechanization is recommended that is built around the capabilities of a reflective liquid crystal pictorial display. Such a system could present high-resolution synthetic-array radar on board an aircraft in real-time with improved performance and decreased complexity over systems that utilize CRTs.		

Security Classification

UNCLASSIFIED
Security Classification

Security Classification