MEMS Gate Structures for Electric Propulsion Applications

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A MEMS gate prototype is under development to extract and accelerate charged particles for use with field emission cathodes and the nanoparticle field extraction thruster at the University of Michigan. Preliminary simulations suggest the desirability of a unity aspect ratio in the emission channel design to achieve electric field uniformity. Low emission threshold cubic boron nitride films have been grown, and gated testing with these films along with carbon nanotubes is in progress.

Nomenclature

A	=	aspect ratio	J	=	current density
A_{FN}, B_{FN}	=	Fowler-Nordheim coefficients	R	=	emitter radius
D	=	gap distance	R_c	=	grid opening radius
$D_{\mathrm{gate\text{-}tip}}$	=	gate-tip gap distance	t_c	=	grid thickness
$D_{\mathrm{gate\text{-}gate2}}$	=	distance between gates of dual gate system	V	=	grid voltage
D_{sheath}	=	sheath thickness	V_a	=	anode voltage
E	=	electric field	V_{emitter}	=	emitter voltage
E_s	=	emission surface electric field	V_{gate}	=	gate voltage
I	=	emission current	V_{sheath}	=	sheath voltage

I. INTRODUCTION

ELECTRIC propulsion (EP) technologies incorporating the use of microelectromechanical (MEMS) gated structures for the extraction and acceleration of charged particles are under development. Unlike metal screens, which have tens to hundreds of microns for gap spacing, micron-scale or smaller gap distances can be achieved with MEMS structures. Large electric fields may be generated at modest bias voltages, which saves power and simplifies spacecraft power bus design, thus making the gated structures attractive for field emission applications. MEMS gates can also be used to build miniaturized, integrated propulsion systems that can be used for micro- to high-power spacecraft and easily scaled to systems in between, thus providing mission designers with greater flexibility. Finally, the use of mature microfabrication techniques that are routinely used in the semiconductor and MEMS industries, along with the economies of scale associated with mass production, make MEMS gates potentially economically attractive.

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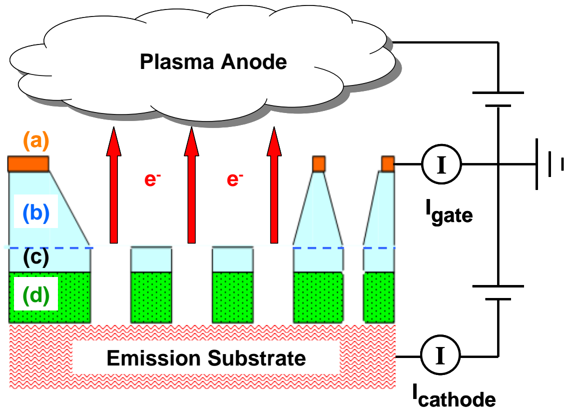

Figure 1. Cross-section view (not to scale) of MEMS-gated FEC emitting into ambient plasma. *(a) Electrical contact pad to gate; (b) ~500-µm bulk silicon structural layer; (c) sub-micron conductive gate layer; (d) ~2-µm dielectric spacer.*

At Michigan, a MEMS gated structure prototype has been designed and fabricated. This structure is currently undergoing characterization and integrated testing with various electron field emission substrates, including carbon nanotubes (CNTs) and cubic boron nitride (c-BN), to form novel electron field emission cathodes (FECs). Such FEC materials, which do not require heaters or propellants, emit electrons from the conduction band via quantum mechanical tunneling. FECs are thus of particular interest for miniaturized, low-power EP systems as replacements for hollow cathodes, which consume a disproportionate amount of propellant and power as the thruster is scaled down in size.[1] A variant of these MEMS gates is also intended to be used as the means of extracting and accelerating charged nanoparticles for the nanoparticle field extraction thruster (nanoFET).[2,3]

This paper describes the design rationale for the MEMS gates along with their fabrication process. Integrated test plans with carbon nanotube substrates are discussed, along with MEMS gates' applications in c-BN FECs and nanoFETs. This paper concludes with a discussion on using MEMS gates for dual-grid electron field emission applications.

II. Gate Design

As schematically depicted in Figure 1, which is a notional cross section of a FEC, each MEMS gate consists of a conductive layer placed over a dielectric spacer with channels arrayed throughout the structure to permit passage of charged particles. A voltage bias applied between the conductive layer and the emission medium under the dielectric spacer generates the electric fields needed to extract and accelerate charged particles. The thinner the dielectric spacer is, the lower the bias voltage needed to generate the necessary electric fields; the limit is imposed by the breakdown strength of the dielectric material and the structural integrity of the overall gate. Both the conductive and dielectric gate layers are structurally supported in bulk silicon, and viewing windows are etched in the bulk silicon to expose the emission channels.

As charged particles are emitted through the channels, some of the particles impact either the conductive layer or the dielectric spacer due to nonuniformities in the electric field or space charge spreading of the particle beam. This collected gate current is an efficiency loss for the system, so a good gate design seeks to minimize gate current.

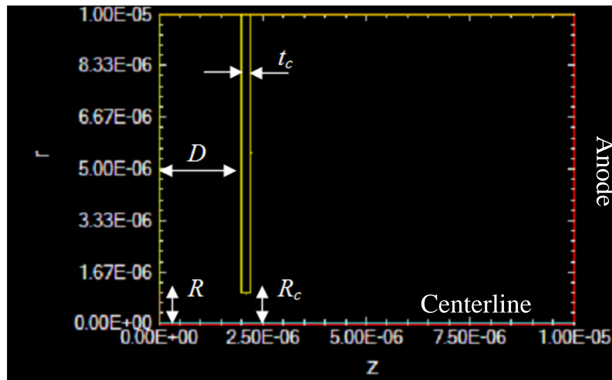

Figure 2. Baseline simulation space configuration for single grid opening. *The domain is axisymmetric, and the spatial units are in meters.*

A. Gate Currents in Screen Grids

Certain FECs such as CNT field emitters use metal screen grids suspended above the emission substrate to extract and accelerate electrons. Following upon previous studies at Michigan using ion optics simulations, particle-in-cell (PIC) simulations were performed at the scale of the individual grid openings for spatial scales achievable in the MEMS gate design. Using PIC simulations permits the examination of space charge effects that are neglected in simple ion optics studies. For FECs in which the emission sites are not well ordered (e.g., CNT cathodes), electron emission is not uniform across the entire substrate.[4] Emission could be dominated by a small number of favorable emission sites, reinforcing the importance of examining space charge effects.

PIC simulations were performed with OOPIC (Object-Oriented Particle-in-Cell Code),[5] a 2.5D (two spatial and three velocity dimensions) code developed

Parameter	Value
Emitter radius, R [μm]	1
Gap distance, D [μm]	2
Grid opening radius, R_c [μm]	1
Grid thickness, t_c [μm]	0.2
Grid voltage, V [V]	200
Anode voltage, V_a [V]	200
Emission current, I [mA]	1
Time step [fs]	10
Spatial cell size [nm]	100

Table 1. Baseline parameters for PIC simulations for a single grid opening. *Baseline configuration has a unity aspect ratio.*

by the Plasma Theory and Simulation Group at the University of California at Berkeley and distributed by Tech-X Corporation. For each run, the electrostatic solver iterated until the system reached steady state. Parameters of interest such as the gate current and electric field magnitudes were obtained from either existing or user-defined diagnostics within OOPIC.

Figure 2 shows the baseline simulation space configuration in OOPIC for a single grid opening. The simulated domain is axisymmetric with the axis of symmetry along the centerline of a grid opening. An electron source of radius R is located on the left boundary and separated from the conductive grid (at a radius R_c from the centerline and t_c in thickness) by a gap distance D. This simplified electron source produces cold electrons at 0.026 eV (room temperature) that are then accelerated from the planar emission surface by the electric field generated by the grid, which is biased at voltage V above ground. The entire left boundary is grounded, while the right boundary is a collection anode that is biased at voltage V_a above ground. A dielectric wall with free space permittivity closes the upper boundary of the simulated space and is placed far enough away from the centerline so no interaction between divergent beam particles and the wall takes place.

Table 1 shows the baseline simulation parameters for a single grid opening. Both the time step and the spatial cell size were determined via convergence studies. To ensure an adequate number of particles in the simulation space, an emission current of 1 mA was used. This current level may seem high when considering that a 1-cm^2 device may have millions of emission channels, but it may be treated as a worst case scenario when considering emission nonuniformity from a small number of favorable emission sites on the substrate. Moreover, this PIC study was intended to identify general trends in gate current collection rather than as a high fidelity model for a specific cathode device.

The aspect ratio of the screen grid is defined as

$$\mathrm{A} \equiv \frac{D}{2R}. \tag{1}$$

A unity aspect ratio is used for the baseline configuration. In the PIC simulations, the aspect ratio parameter was varied by changing the gap distance while keeping the emitter radius constant at 1 μm.

Note that field emission devices obey the Fowler-Nordheim (F-N) relation,

$$J = A_{\mathrm{FN}} E_s^{\,2} \exp\left(-\frac{B_{\mathrm{FN}}}{E_s} \right), \tag{2}$$

where J is the current density, E_s is the electric field at the emission surface, and A_{FN} and B_{FN} are the Fowler-Nordheim coefficients that depend on the emission material and surface geometry. Since to first order, the emission surface electric field is approximately the gap electric field

$$E_s \approx \frac{V}{D}, \tag{3}$$

the grid bias was scaled linearly with the gap distance in order for the field emission device to maintain a constant baseline electric field (100 V/μm) and emission current.

Figure 3 shows the PIC simulation results. The gate current collection reaches a minimum for aspect ratios in the range of 1 to 1.5. This result supports the initial assumption that the baseline configuration minimizes gate current. At low aspect ratios, the electric field at the emission surface is not uniform and has a significant radial component that contributes to the high gate current. At very high aspect ratios, gate current is high because of beam spreading before the beam passes the gate.

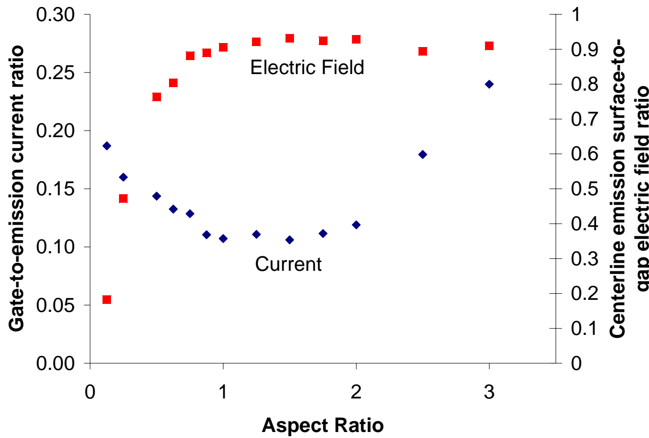

Figure 3. Steady-state gate current and centerline emission surface electric field variation with aspect ratio. *Simulations were performed at 1-mA emission current and 100-V/µm gap electric field and no longer represent a field emission device at aspect ratios less than 0.75.*

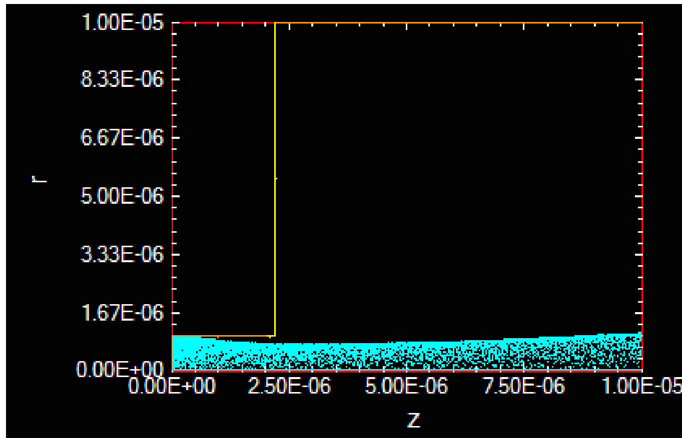

Figure 4. Beam focusing by MEMS gates at steady-state conditions. *Particle impingement can result in charge build-up on the dielectric walls and deflect charged particles toward the channel's centerline.*

This simulation holds the emission current constant, an approximation that is valid as long as the electric field at the emission surface is also constant. Due to radial symmetry, the electric field at the center of the emission surface only has an axial component. At aspect ratios above 0.75, this steady-state electric field levels off versus aspect ratio and is only reduced by about 10% from the baseline gap electric field due to space charge effects. As the aspect ratio is decreased below 0.75, however, the steady-state electric field rapidly falls due to decreased surface field uniformity at low aspect ratios. Consequently, the simulation no longer represents a constant-current field emission device at aspect ratios less than 0.75; in practice, the reduced field strength at the surface would generate less than 1 mA of current.

Gate current variation with other geometric parameters was also examined. As the grid thickness increases relative to the gap distance, gate current increases due to the increased current collection area. An increase in gate current is also seen for constrictions of the grid opening with respect to the baseline value ($R_c < R$).

B. Focusing Effect of Dielectric Walls

The actual MEMS gate differs from the screen grid in that the conductive gate layer is separated from the emission surface by a dielectric spacer. As charged particles impinge upon the dielectric, the channel walls can build up charge depending on its conductivity. The resulting electric field acts to oppose the movement of charged particles to the walls and causes a focusing of the charged particle beam within the emission channel. Therefore, gate current may be significantly reduced once steady-state operation is reached. This effect is depicted in Figure 4. Additional effects due to charge migration along the dielectric surface are being investigated.

III. MEMS Gate Fabrication

MEMS gates are built using microfabrication techniques commonly used in the semiconductor and MEMS industries. This approach improves the reliability of the fabrication process by making use of the expertise built up in these related fields. The present MEMS gate design, designated the Beta prototype, incorporates lessons learned from the initial Alpha prototype. Both prototype versions are described below. Future design work includes additional modifications to ensure that the gates will survive the likely application environments, including such detrimental effects as ion sputtering and atomic oxygen decay.

A. Alpha Gate Prototype

The Alpha gate's fabrication process is shown in Figure 5.[6] Highly doped (greater than 10^{20} cm^{-3} boron) polysilicon serves as the conductive layer, while a triple stack silicon oxide-nitride-oxide serves as the 2-µm

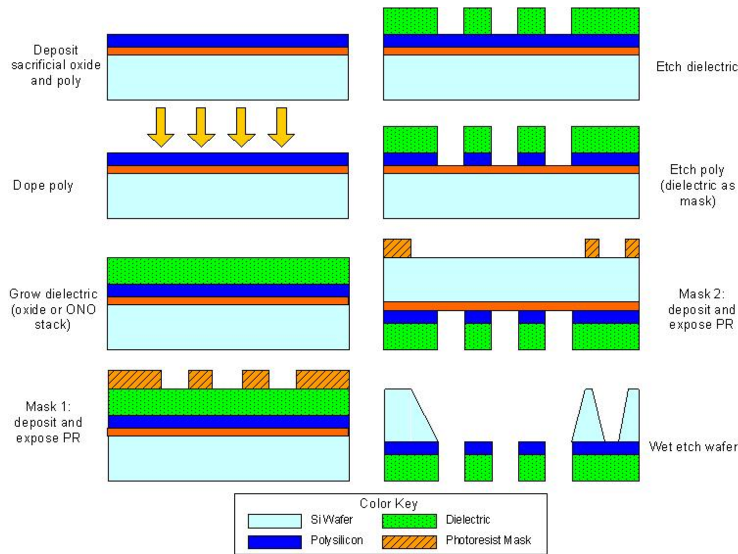

Figure 5. Alpha gate fabrication process (Reference 6). *Individual gates chips are separated via mechanical dicing.*

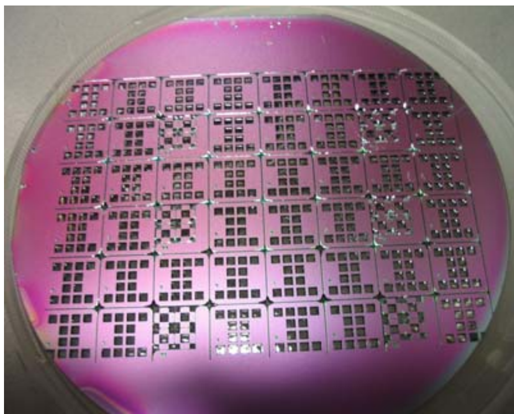

Figure 6. Alpha gates on 4-in diameter silicon wafer prior to dicing. *Array includes test chips to investigate alternative geometric configurations.*

dielectric spacer. Both of these layers are deposited using low pressure chemical vapor deposition with a surface roughness on the order of tens of nanometers or less. This surface roughness is comparable to that of the emission substrate to ensure proper alignment during mounting. After the layers are deposited, the emission channels are formed using reactive ion etching. These emission channels are exposed by etching away, via a dissolved wafer process using ethylene diamine pyrocatechol, viewing windows in the bulk silicon that act as structural support members.

Figure 6 shows a wafer of completed Alpha gate structures. An individual gate structure is approximately 1 cm^2 in area with 11 viewing windows for particle emission. Each viewing window contains about 4×10^4 emission channels that are 2-μm in diameter with a center-to-center spacing of 5 μm, for a 12.6% grid transparency. The last viewing window does not contain emission channels but serves as a contact pad to enable wire bonding via colloidal silver and silver epoxy to the polysilicon conductive layer.

B. Beta Gate Improvements

Despite the inclusion of a contact pad area for wire bonding in the Alpha gate design, testing revealed the difficulty of achieving a reliable electrical contact with the conductive polysilicon layer. These difficulties were due to the presence of a silicon oxide surface layer and the risk of rupturing the gate membrane layers by exerting pressure on the contact pad. In the Beta gate design, this electrical connectivity issue is resolved by utilizing a gold contact surface on the bulk silicon and replacing the polysilicon conductive layer in the Alpha design by a ~0.5-μm-thick, ion-implanted layer (4×10^{16} cm^{-2} boron). Using ion-implantation retains a thin, single-crystal conductive layer, and by replacing the polysilicon layer, the Beta prototype increases gate membrane resistance to rupture during handling and assembly. To ensure good conductance between the gold contact surface and the ion-implanted layer, doped bulk silicon (1-20 Ω-cm) is used.

The dielectric layer for the Beta gate structure is low-stress silicon nitride rather than the triple stack in the Alpha design. Low-stress silicon nitride provides a slight tensile stress, like the oxide-nitride-oxide triple layer, to keep the gate membrane from flexing but enables a more streamlined fabrication process. The dielectric strength for silicon nitride is also higher than that for the triple stack, thus permitting higher voltages to be applied to the gate structure during testing.

The Alpha gate structures had low yields during their fabrication run, with one of the reasons being the need to use a dice saw to separate the gate structures from each other after fabrication. This mechanical dicing generated particulate contamination and also led to rupturing of the gate membrane layers. In the Beta design, this problem is resolved by incorporating scribe lanes into the fabrication process. During the deep reactive ion and wet etch to open up the viewing windows, the scribe lanes are also etched, thus permitting self-dicing of the gate structures as the final step in the fabrication process. To improve yield for the Beta gate structures, test chips are included in the

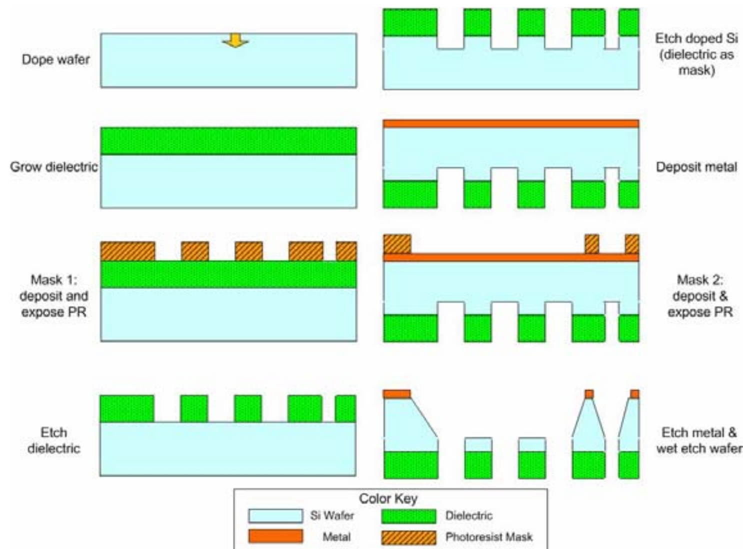

Figure 7. Beta gate fabrication process (Reference 7). *Individual gates are separated via self-dicing during fabrication.*

fabrication run to monitor each process step. These test chips verify the presence of emission channels and the conductive ion-implanted layer following fabrication. The test chips also provide an indication of spatial variability during the fabrication process. Figure 7 shows the fabrication process for the Beta gate structure.[7]

IV. Gated Testing with Carbon Nanotubes

To determine the functionality of these MEMS gate prototypes, they were integrated with carbon nanotube (CNT) substrates from Applied Nanotech to form functional FECs. Emission testing on these field emitters is being conducted to determine the emission threshold voltage for the gated FECs. The gate is expected to lower the threshold voltage because of its closer spacing for a given bias voltage. Current collected by the gates are tracked to verify the proper design of the gate structures, seen in Figure 8.

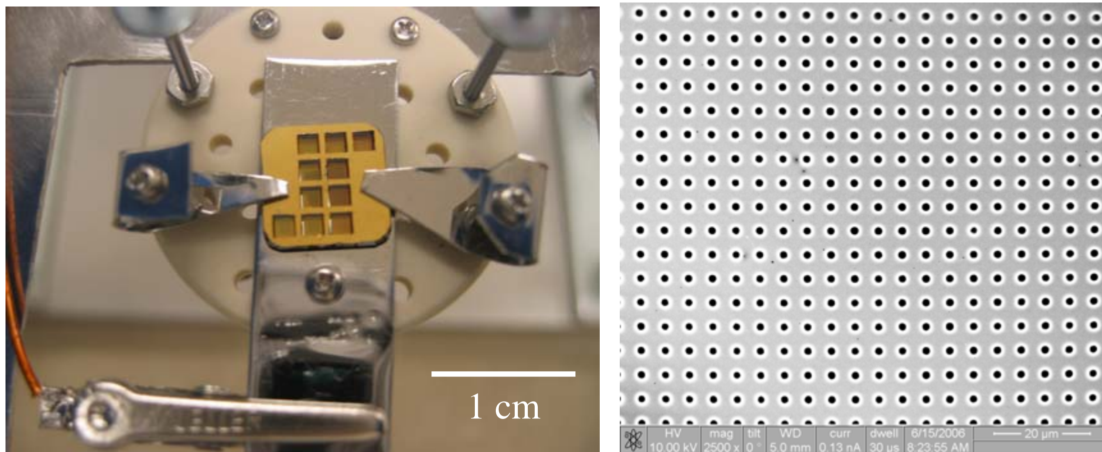

Figure 8. Beta gate design. *1-cm^2 chip shown during preparation for integrated testing (left). Array of emission channels 2 μm in diameter with 5-μm center-to-center spacing seen under a scanning electron microscope (right).*

CNT films, 5-10 µm in thickness and grown on n-type silicon substrates, are being used for the gated tests. Electrical contact is made to a CNT film by pressing the doped silicon substrate of the CNT sample against a stainless steel electrode by clamps. Planar alignment is enforced between the CNT sample and the mounted MEMS gate by utilizing an indium tin oxide (ITO) coated microscope slide as the collection anode, offset from the MEMS gate by kapton film spacers. The entire assembly can then be sandwiched between microscope slides using adjustable spring clamps. Separate Keithley sourcemeters are used to bias the gate and the collection anode relative to the CNT sample. These sourcemeters also monitor the emission and anode currents, with the gate current of the FEC monitored by a separate Keithley multimeter. Gated CNT tests are currently in progress.

V. Cubic Boron Nitride FEC

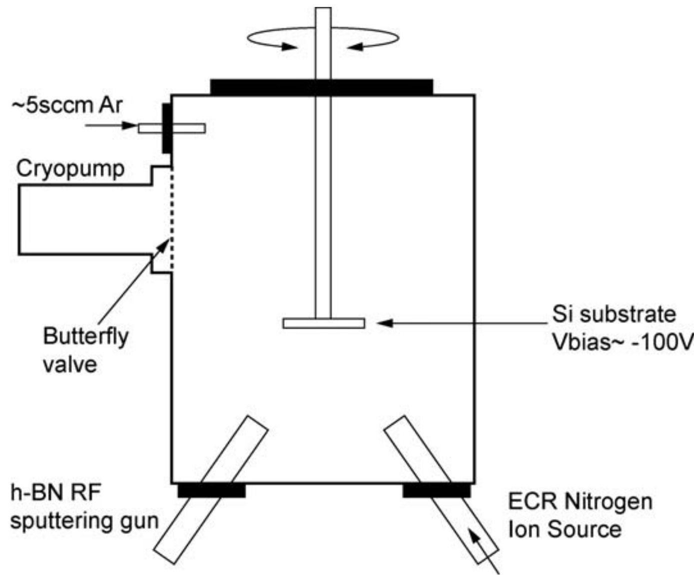

Figure 9. c-BN growth chamber setup. *Samples are rotated during growth to promote film uniformity.*

Poor sputter resistance and reactive surfaces severely lower the lifetime of state-of-the-art FECs and can limit their use in a micro-EP system plasma environment, where ion bombardment of the array would readily degrade the array tips and their performance.[8] For CNTs, a similar lifetime concern exists regarding atomic oxygen reactions for low Earth orbit (LEO) applications.[9] Recently, cubic boron nitride (c-BN) has emerged as a candidate material that could make practical FECs realizable in EP and LEO environments. With physical properties that resemble diamond, c-BN is a large band-gap, metastable material with high thermal conductivity, high mechanical strength, and good chemical stability.[10] c-BN thus is thought to have excellent sputter resistance and to form a less reactive surface than current field emission materials. Its toughness should lower ion bombardment damage and inhibit the formation and migration of emitter surface nanoprotrusions that could otherwise lead to destructive arcing of the array. c-BN's chemical inertness should also make it more tolerant than other prospective emitter materials to atomic oxygen and other contaminants present in a micro-EP system's operational environment. As an additional benefit, c-BN has a low work function that enables lower operating voltages to decrease potential sputtering damage.

A. c-BN Growth Process

c-BN films were grown using a method developed by Kidner[11] on Si (001) substrates (p-type doped with a resistivity of 1-20 Ω-cm) in a vacuum environment. Prior to growth, the substrate's oxide layer was removed by thermal desorption at 1,000 ºC for 10 minutes. A hot pressed boron nitride target (4N) in the hexagonal phase (h-BN) was sputtered in a RF magnetron sputtering gun. To promote the nucleation of the cubic phase, an electron cyclotron resonance nitrogen ion source was used. The kinetic energy of the incident nitrogen ions was controlled using a negative bias applied to the substrate. Since both cubic and hexagonal phases nucleate simultaneously, the bias also favored the selective etching of the softer h-BN while leaving the c-BN material intact. During deposition, argon was bled into the growth chamber along with the flow from the nitrogen ion source, resulting in an operational pressure less than 3 mTorr.

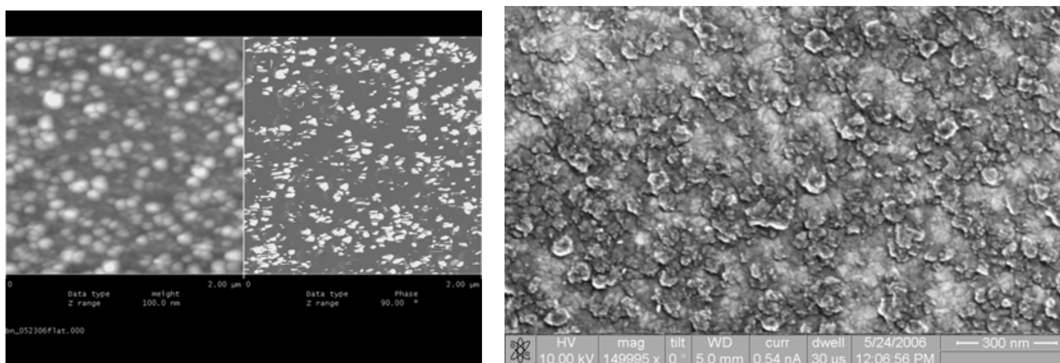

Figure 10. c-BN samples imaged with atomic force (left) and scanning electron (right) microscopy. *Surface features for this sample (left) are ~100 nm in height. Sharp edges on "islands" (right) represent favorable emission sites.*

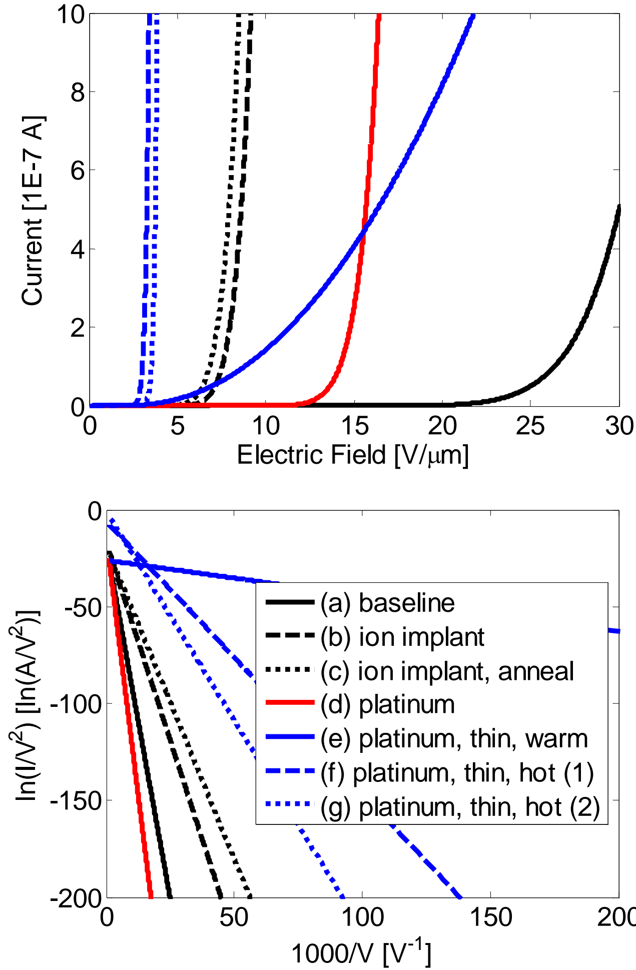

Figure 11. Averaged c-BN emission profiles (top) and corresponding F-N plots (bottom). *Each curve represents an average of all I-V emission profiles for a given sample. Emission area is ~1 cm^2 for each sample. BN samples are: (a) baseline thick (over 100 nm) film grown at ~950 ºC on bare Si, (b) baseline film with carbon implantation, (c) baseline film with carbon implantation and annealing, (d) thick film grown on Si wafers with Pt backing, (e) thin (less than 100 nm) film grown on Pt-coated wafers at ~700 ºC ("warm"), (f) thin film grown on Pt-coated wafers at ~950 ºC ("hot"), and (g) same growth conditions as (f).*

voltage (I-V) behavior on a Fowler-Nordheim (F-N) plot (1000V^{-1} versus ln(I/V^2)). Each I-V sweep can thus be reduced to two parameters: the slope and the intercept of the F-N plot. For each functional emitter, the averaged F-N parameters for all emission tests were determined, and they are shown in Figure 11, along with I-V curves resulting from these averaged parameters. Table 2 shows the threshold electric field, defined as the gap electric field needed to achieve a 100-nA emission current. This threshold current value was chosen because it lies an order of magnitude above the current measurement noise floor. A low electric field threshold is desired because it enables low operating voltages, thus

A growth rate of ~20 nm/hour was achieved, and the substrate temperature was monitored using an optical pyrometer. To improve the film uniformity, the substrate was rotated during the deposition process. Because of the high strain in the film, the samples were gradually cooled over 20 minutes to minimize delamination. Fourier transform infrared spectroscopy was used to evaluate the composition of the film. Figure 10 shows microscopy images of the grown c-BN samples.

B. Emissions Testing

c-BN emission testing was performed in a vacuum environment in the mid- to low 10^{-8} Torr. Earlier samples were grown on bare silicon substrates, which necessitated the formation of indium contact pads on the substrate backsides for wire bonds. Later samples were grown on silicon substrates whose backsides already had a deposited platinum layer. Not only did the platinum layer improve the heating uniformity of the samples during growth, but it also facilitated making electrical contact to the c-BN substrate. For initial tests, the c-BN film was offset, using kapton film spacers, from an ITO-coated microscope slide that served as the collection anode. This kapton mask around the edges of the c-BN sample helped to reduce edge effects and provided ~1 cm^2 of emission area. The entire setup was sandwiched and clamped between two microscope slides to enforce planar alignment. A voltage bias was applied between the c-BN and the ITO slide using a Keithley sourcemeter, which also monitored the emission current.

The emission performance of a c-BN sample was analyzed by plotting the sample current-

Sample	Threshold Electric Field [V/μm]
(a) Baseline	26.3 ± 3.3
(b) Ion implant	7.6 ± 0.1
(c) Ion implant, anneal	6.8 ± 0.5
(d) Platinum	14.6 ± 2.2
(e) Platinum, thin, warm	9.3 ± 2.7
(f) Platinum, thin, hot (1)	3.0 ± 0.1
(g) Platinum, thin, hot (2)	4.2 ± 1.2

Table 2. Averaged threshold electric field for c-BN emission. *The threshold is defined for when the gap electric field causes 100 nA of emission current. Emission area is ~1 cm^2 for each sample.*

simplifying electrical system design and reducing sputtering damage.[12]

The baseline c-BN sample is a thick (over 100 nm) film grown at ~950 ºC on bare silicon. Upon doping via carbon implantation at 10^{13} ions per square centimeter concentration at 40 keV, the threshold electric field decreases by over a factor of three. Upon annealing the ion-implanted sample at 900 ºC for 20 minutes, a slight decrease in the threshold electric field is achieved.

Samples grown on silicon wafers whose backsides were coated with platinum result in a decrease in the threshold electric field by about a factor of two from the baseline sample. This performance improvement corresponds with the platinum layer providing more uniform substrate heating during the growth process, resulting in more uniform films.

Atomic force microscopy images indicate that thinner c-BN samples (less than 100 nm) have greater surface roughness than thicker films. For these thin films, the boron nitride composition is a mixture, with c-BN nucleation on a wetting layer of amorphous and hexagonal boron nitride.[13] These "islands" of c-BN nucleation sites have not yet coalesced, and their sharp edges are promising candidates for field emission sites. Thus, thin samples are suggested to provide improved field emission performance. Moreover, the growth temperature affects the surface mobility, which also appears to have a significant effect. The best emission performance is from two thin samples grown at essentially the same growth conditions (~950 ºC) on platinum-backed silicon wafers. The performance of these two samples are quite similar, and further emission and lifetime testing, both gated and ungated, are planned.

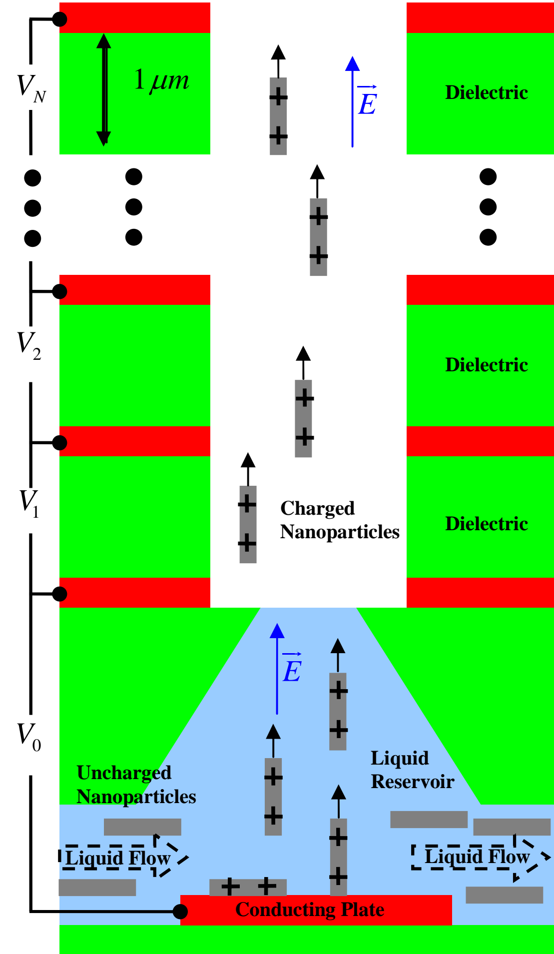

Figure 12. Single emitter element of a multi-grid, nanoparticle thruster using a dielectric liquid. *Charge neutralization can be accomplished by other emitter elements in the nanoFET array operating with opposite polarity.*

VI. nanoFET Application

In addition to FEC applications, MEMS gates may also be applicable for Michigan's nanoFET (nanoparticle field extraction thruster) design, schematically depicted in Figure 12 in the dielectric liquid configuration (see AIAA-2006-4335 and AIAA-2006-4803). A series of stacked MEMS gates can be used to provide the electric field necessary to charge conductive nanoparticles, whose diameters must be smaller than the emission channel diameter, and to transport them to the liquid surface. There, the electric field imposed by the gate structures would extract the nanoparticles from the liquid surface and accelerate them to generate propulsive thrust. Using MEMS gates would permit lower operational voltages due to their close spacing than would be possible with other gridded structures.

To achieve high specific impulse operation, large potential differences are needed to accelerate the charged nanoparticles to high exhaust velocities. However, the high electric fields associated with these potential differences over small length scales tend to promote liquid surface instability by exciting electrohydrodynamic waves. Such liquid surface instability may lead to Taylor cone formation and the generation of colloids, whose size and charge variability would offset the precise thrust controllability afforded by the nanoparticles. A stacked gate design would help avoid conditions of instability by decoupling the particle extraction (moderate potential) and acceleration (high potential) stages.

By using a stacked gate design, large acceleration potentials may be applied without exceeding the breakdown strength of the separate dielectric layers. In addition, preliminary charged particle trajectory simulations suggest that a stacked gate design improves beam collimation; such reduction in the beam divergence caused by space charge effects would result in improved efficiency and lifetime for the nanoFET system. More refined simulations are in progress.

VII. Dual Grid Electron Field Emission

Similar to the multi-layer, stacked gate structures that are needed for the nanoFET system, a dual layer MEMS gate can provide significant benefits for certain electron field emission applications.[14] The total power cost for electron emission is determined by the final energy of the electron beam leaving the spacecraft. This final energy is controlled by the outer gate of an emission system as well as the bias of the spacecraft with respect to the ambient plasma. With a dual gate structure, the electric field required for electron extraction can be decoupled from the final beam energy. A high voltage can be applied to the inner gate to extract electrons, while a lower voltage on the outer gate can limit the overall emission energy to a level that is only just above what is required to avoid space-charge limit reflection of the beam. This configuration, schematically shown in Figure 13, can result in a significant power savings for existing emission systems where the current level is low enough that the extraction field requirements far exceed the space-charge limit requirements.

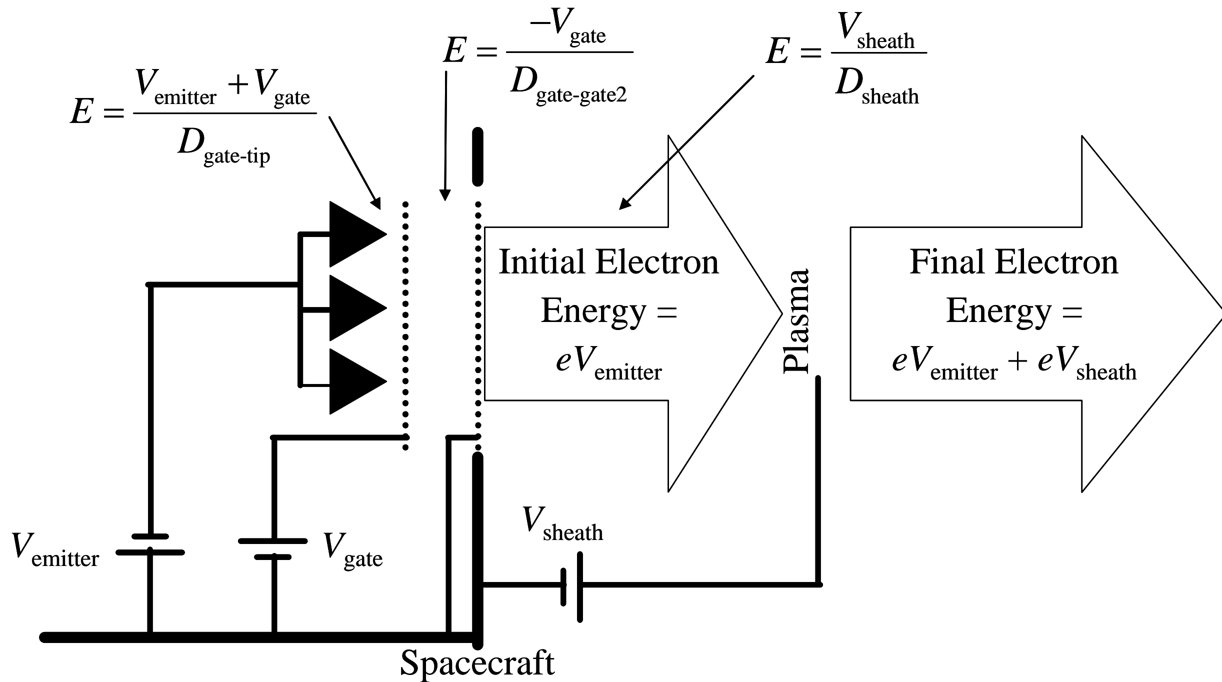

Figure 13. Emission with dual power supplies and dual gates (Reference 14). *The electric field used for emission is isolated from that providing the final acceleration of the electrons. Electrons accelerate in the extraction field towards the first gate but then decelerate between the first and second gates, thus leaving with only the energy supplied by the emitter power supply. In the sheath, the electrons are further decelerated, and only the emitter power is spent in the absence of gate current. The outer gate shields the extraction gate from the surrounding plasma, thus minimizing the impact of the emitter on spacecraft operations and the plasma.*

Alternately this setup can permit the use of a wider range of potentially more robust emitter materials that previously could not be considered due to prohibitively high extraction field requirements. By incorporating a dual gate directly into a MEMS structure, the power savings is expected to be accomplished easily and efficiently, with minimal additional system cost or impact. By holding the outer gate at the spacecraft potential, the electron emission system should not disturb the local plasma or worsen space-charge limits by creating a larger sheath. Experimental demonstration of this technique is planned for the next generation of dual MEMS gates.

VIII. Conclusion and Future Work

A MEMS gate prototype design has been fabricated and is currently undergoing integrated testing with CNTs to determine the gate design's functionality. With the demonstration of c-BN films with low emission electric field thresholds, plans for testing integrated c-BN FECs are also proceeding. Work continues to improve the c-BN films' emission characteristics, including emission threshold, current density, and emission stability. This work includes

using heavy n-type doping of the films via ion implantation, surface morphology studies immediately following c-BN nucleation, and emission in AC rather than DC mode.

More refined PIC simulations are planned to optimize the MEMS gate design, and more advanced microfabrication techniques are being considered to reduce the dielectric spacing and increase the film transparency. Alternative configurations are also being explored, including a dual gate design that decouples the extraction and acceleration stages for FECs and the nanoFET system. Of particular interest is a design in which the gate layers are built directly onto the c-BN films. Using electron beam lithography rather than optical lithography for these gates would permit smaller feature sizes and an order of magnitude stronger electric fields for the same applied gate voltage.

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