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1. REPORT DATE (DD-MM-YYYY) 18-02-2016		2. REPORT TYPE Final Report		3. DATES COVERED (From - To) 24-Sep-2009 - 24-Sep-2011	
4. TITLE AND SUBTITLE Ultra Low Noise Infrared Detector Amplifier for Next Generation Standoff Detector			5a. CONTRACT NUMBER		
			5b. GRANT NUMBER W911NF-09-C-0095		
			5c. PROGRAM ELEMENT NUMBER 665502		
6. AUTHORS Hari Vemuri, Angelo Scotty Gilmore			5d. PROJECT NUMBER		
			5e. TASK NUMBER		
			5f. WORK UNIT NUMBER		
7. PERFORMING ORGANIZATION NAMES AND ADDRESSES EPIR Technologies Inc 590 Territorial Drive Suite B Bolingbrook, IL 60440 -4881			8. PERFORMING ORGANIZATION REPORT NUMBER		
9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS (ES) U.S. Army Research Office P.O. Box 12211 Research Triangle Park, NC 27709-2211			10. SPONSOR/MONITOR'S ACRONYM(S) ARO		
			11. SPONSOR/MONITOR'S REPORT NUMBER(S) 55204-EL-ST2.1		
12. DISTRIBUTION AVAILABILITY STATEMENT Approved for Public Release; Distribution Unlimited					
13. SUPPLEMENTARY NOTES The views, opinions and/or findings contained in this report are those of the author(s) and should not be construed as an official Department of the Army position, policy or decision, unless so designated by other documentation.					
14. ABSTRACT Report developed under topic #A08-T017, contract W911NF-09-C-0095. A wideband ultralow-noise amplifier (LNA) for standoff detection applications employing a commercial 0.15 μ m PHEMT active device and a feedforward noise cancellation technique has been developed. The technology used is based on the 0.15- μ m pHEMT 3MI TriQuint power process. The amplifier has a die surface of 1 mm by 2 mm and a gain that exceeds 17 dB between 200 MHz and 2.25 GHz. The matching at both input and output is better than					
15. SUBJECT TERMS LWIR, HgCdTe, MHEMT, Noise Figure, Noise Cancellations, STTR Report					
16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT UU	15. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON Don Rafol
a. REPORT UU	b. ABSTRACT UU	c. THIS PAGE UU			19b. TELEPHONE NUMBER 630-771-0204

Report Title

Ultra Low Noise Infrared Detector Amplifier for Next Generation Standoff Detector

ABSTRACT

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Sub Contractors (DD882)

1 a. Illinois Institute of Technology

1 b. Room 301, Main Building

3300 South Federal Street

Chicago

IL

60616

Sub Contractor Numbers (c): 0095-SIIT-09-0001

Patent Clause Number (d-1): 52.227-11

Patent Date (d-2): 12/1/07 12:00AM

Work Description (e): Under the direction of Yang Xu, Ph.D. the IIT team will provide consultation for the noise

Sub Contract Award Date (f-1): 9/24/09 12:00AM

Sub Contract Est Completion Date(f-2): 8/24/11 12:00AM

Inventions (DD882)

Scientific Progress

Technology Transfer

Ultralow-noise Amplifier for Next Generation Standoff Detector

Abstract: A wideband ultralow-noise amplifier (LNA) for standoff detection applications employing a commercial 0.15 μm PHEMT active device and a feedforward noise cancellation technique has been developed. The technology used is based on the 0.15- μm pHEMT 3MI TriQuint power process. The amplifier has a die surface of 1 mm by 2 mm and a gain that exceeds 17 dB between 200 MHz and 2.25 GHz. The matching at both input and output is better than -10 dB. The measured noise figure at room temperature is 1.1 dB at 700 MHz and 1.2 dB at 1.5 GHz. The measured $P_{1\text{dB}}$ and P_{sat} at room temperature are about 7 dBm and 10 dBm, respectively. At room temperature, the LNA draws 37 mA at 3 V voltage. We further characterized the LNA at cryogenic temperatures in terms of gain, input/output match and noise figure. The measured results showed an improvement of approximately 0.9 dB in noise figure across the band. At cryogenic temperatures, the gain variation is approximately 1.5 dB, while the input/output match fluctuated without any disruption in the LNA behavior. This LNA is intended for use in applications requiring a combination of low noise and low operating temperatures.

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Glossary

ADS – Advanced Design System

DUT – Device Under Test

FET – Field Effect Transistor

G-S-G – Ground-Signal-Ground

HEMT – High Electron Mobility Transistor

ISS – Impedance Standard Substrate

LNA – Low Noise Amplifier

LCC – Leaded Chip Carrier

MMIC – Monolithic Microwave Integrated Circuit

pHEMT – Pseudomorphic High Electron Mobility Transistor

S-Parameter – Scattering Parameters

SOLT – Short-Open-Line-Thru

VNA – Vector Network Analyzer

1. Project Summary

This final report for the Phase II STTR program “Ultralow-Noise Amplifier for Next Generation Standoff Detector” summarizes the Phase II milestones and findings and also discusses potential applications for the demonstrated prototype. The objectives of Phase II were to build, fabricate and test a low-noise infrared detector amplifier with a noise figure less than 1 dB and bandwidth of 1 GHz. In the first part of the project, low-noise GaAs mHEMT (metamorphic High Electron Mobility Transistor) and CMOS-based amplifiers employing thermal noise cancellation were demonstrated through simulations. In the subsequent part, an ultralow-noise amplifier employing the feedforward noise cancellation technique was designed, fabricated and tested using the 0.15 μm pHEMT (pseudomorphic High Electron Mobility Transistor) process from TriQuint. A packaged LNA prototype was also developed and tested.

2. Brief Summary of Phase II Effort

An ultralow-noise amplifier was designed, fabricated, tested and packaged. The major source of internally generated broadband noise is the thermal noise in the channel of the active device. We introduced feed-forward noise cancellation schemes into the amplifier circuit to reduce this thermal noise and improve the noise performance. Our noise cancellation technique was validated by comparing the simulation results for the amplifier with and without noise cancellation. The amplifier demonstrated excellent noise performance and wide bandwidth. A noise figure of 1.1 dB at 1 GHz and a gain of 18 dB have been measured on a pHEMT-based amplifier at room temperature. At a temperature of 120 K, the noise figure dropped to 0.2 dB without significant change in return-loss and gain at a much lower DC power dissipation. A prototype LNA was also built and characterized. Figure 1 (left) is a picture of the bare die. Figure 1(right) shows the topology of our amplifier. In Figure 2, the measured small-signal gain, return loss and noise figure of our LNA are shown.

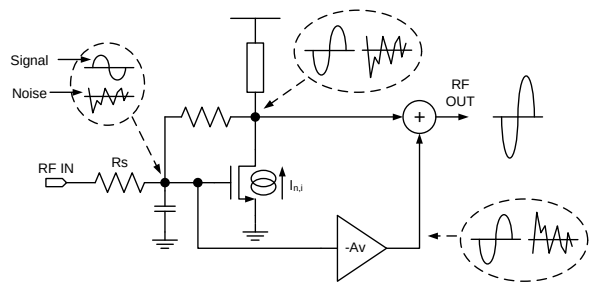
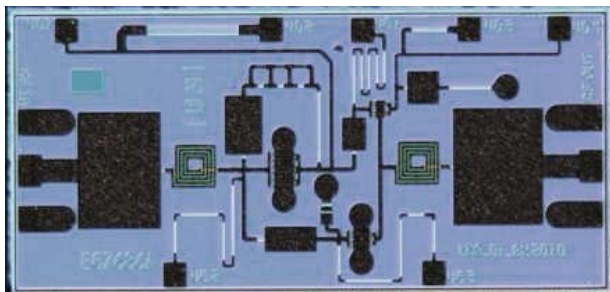


Figure 1: (left) LNA bare die and (right) noise cancellation topology

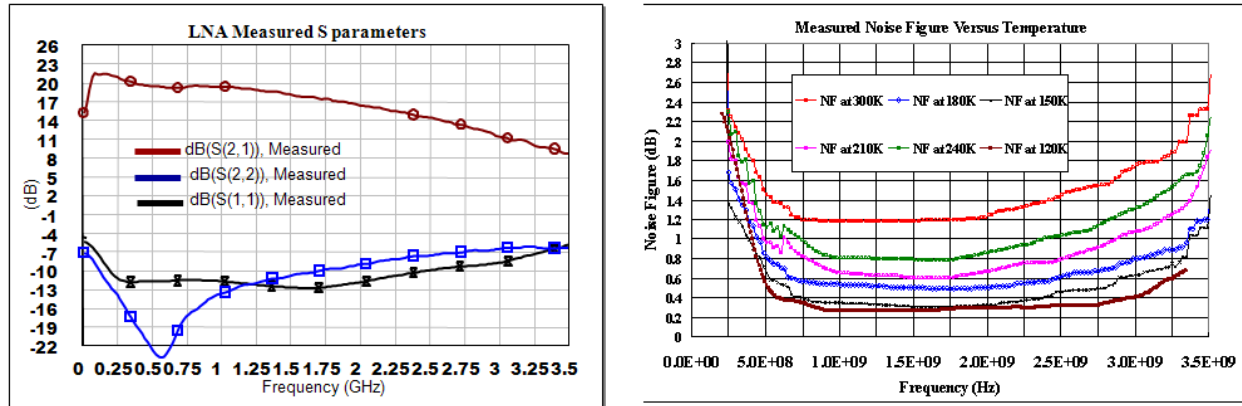


Figure 2:(left) measured gain and return loss and (right) noise figure

In parallel, cryogenic small signal models of pHEMT devices fabricated using the 0.15 μm pHEMT process were also developed for the purpose of examining and analyzing the low-temperature behavior of the TriQuint 3MI process. While the low-noise preamplifier developed is primarily intended to be integrated with photoconductive infrared detectors, a number of direct commercial applications also exist for the LNA.

3.0 Technical Background

3.1 Standoff Detection: Heterodyning for Improved SNR

The detection sensitivity of standoff detection can be significantly improved by heterodyning. The infrared radiation incident on the detector from the scene is mixed with radiation from an infrared laser. The scene is often a vapor plume being sensed remotely for standoff detection. Figure 3 below illustrates a block diagram of heterodyne infrared detection. The infrared radiation from the scene passes through a focusing lens and a limiting aperture. This radiation is then reflected internally and passes through a beam splitter where it is spatially mixed with collimated infrared radiation from a CO₂ laser operating at a single frequency.

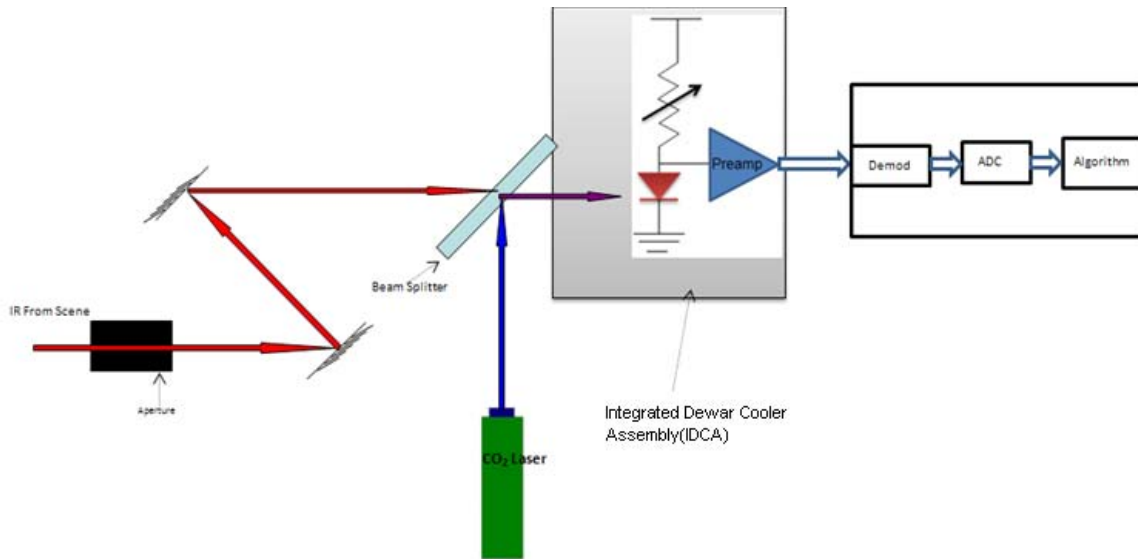


Figure 3: Heterodyne infrared detection

Assuming that the incident beams have frequencies ω_1 and ω_2 and amplitudes E_1 and E_2 , the total electric field incident on the detector is given by:

$$E = E_1 \cos \omega_1 t + E_2 \cos \omega_2 t \quad (1)$$

The detector response is proportional to the intensity of the radiation or to the square of the electric field. The detector response is given by:

$$r \propto [(E_1^2 \cos^2 \omega_1 t + E_2^2 \cos^2 \omega_2 t + E_1(1) E_2(2) \cos(\omega_1 - \omega_2)t + E_1(1) E_2(2) \cos(\omega_1 + \omega_2)t] \quad (2)$$

However, the detector has a limited bandwidth, so that only the DC and difference signal components ($\omega_1 - \omega_2$) can be detected.

The resultant radiation is focused onto a cooled HgCdTe infrared detector which is housed inside an infrared Dewar assembly. One implementation of the detector/amplifier unit is the integration of the amplifier with the detector, with cooling to the same temperature. The cooling results in a reduction of thermal noise in the amplifier, and incorporating the noise cancellation circuit can potentially decrease the noise figure of the detector/amplifier unit. This application makes the diode function essentially as a mixer and is tuned to detect signals whose frequency is the difference between that of the laser and the radiation from the source.

The overall bandwidth of the system is determined by the bandwidths of the detector and the preamplifier. The noise floor of the system electronics limits system performance. The smallest electrical signal from the detector is equal in magnitude to the total noise of the detector. If the signal detected by the detector is less than the input referred noise of the amplifier, the threshold of detection will be higher and significant information is lost. In this situation the preamplifier

sets the noise floor. Therefore, it is important to realize that the noise at the 1st stage of the signal flow chain must be smaller than the noise generated at the detector.

3.2 Preamplifier Noise

For high-speed standoff detection systems such as the one described above, the preamplifier noise can limit the sensitivity of the FTIR system, especially at low photon fluxes and high speeds of operation. The issue for the latter is more serious because the duration of signal integration is extremely short, making the noise bandwidth large and the integrated signal small. If the integrated signal is less than the self-generated noise of the amplifier, significant information will be lost. This is the situation in which the preamplifier sets the noise floor. If, on the other hand, the detector noise is greater than the input referred noise of the amplifier, the detector sets the limit of performance. The smallest signal coming from the detector is equal in magnitude to the noise of the detector. In this condition the signal-to-noise ratio (SNR) is equal to one.

Figure 4 below is a noise model of the detector-preamplifier unit. The detector is modeled as a current source (I_d) representing the generated photocurrent. The detector has a resistance R_d and a shunt capacitance C_d . The thermal noise arising from the detector's finite resistance and the shot noise are the dominant sources of noise in the detector when no flux is incident on it. The equivalent noise current arising from these factors has a spectral density $\overline{i_{nd}^2}$. When the detector responds to the background flux, it generates shot noise with spectral density $\overline{i_{nb}^2}$. It is assumed that this shot noise sets the noise floor of the detector.

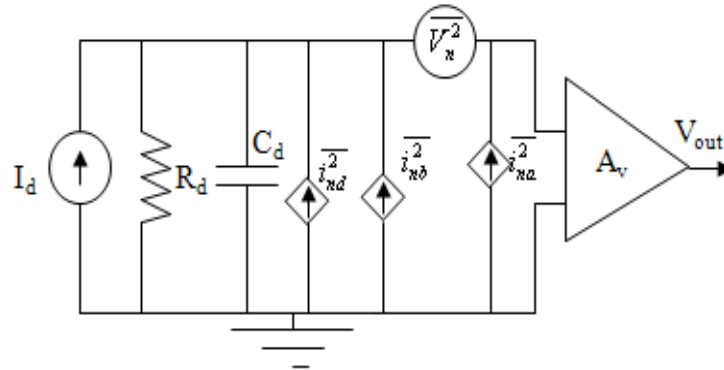


Figure 4: Noise model of preamplifier-detector circuit

The amplifier has a gain A_v and its noise is modeled in terms of its equivalent input noise current and voltage generators (which are uncorrelated) and represented by $\overline{i_{na}^2}$ and $\overline{v_n^2}$, respectively.

Assuming background limited infrared photodetector (BLIP) operation, the total noise spectral density at the input of the amplifier is:

$$e_{ni}^2 = (i_{nb}^2 R_d^2) + v_n^2 + (i_{na}^2 R_d^2) \quad (3)$$

An important parameter characterizing the noise performance of the preamplifier is its noise figure F_{dB} , which is the ratio of the noise contribution from the preamplifier to the total noise from the cooled detector inside the integrated Dewar cooler assembly (IDCA), which encloses and cools the detector-preamplifier assembly:

$$F_{dB} = 10 \log \left[\frac{i_{nb}^2 R_d^2 + v_n^2 + i_n^2 R_d^2}{i_{nb}^2 R_d^2} \right] \quad (4)$$

This equation demonstrates that when the detector noise becomes much larger than the amplifier noise, F_{dB} approaches zero. Similarly, decreasing the equivalent input noise of the amplifier can also decrease the noise figure. This is the ideal situation and it implies that the effect of the amplifier noise is insignificant. However, when the detector noise is weaker, the current and voltage noise of the preamplifier must be minimized and kept below the noise value of the detector.

For instance, consider a HgCdTe infrared detector with an area of 30 μm by 30 μm , operating at 77 K and seeing a background at a temperature of 300 K. The photon flux on the detector is 3.57×10^{16} ph/cm²/sec when using f/2 optics. The approximate photocurrent output from the detector is 41 nA. The detector is assumed background limited already. Since the detector is operated at cryogenic temperatures, thermal noise and dark current noise are neglected and it is assumed that the noise floor is established by the detector shot noise alone, which is calculated to be 1.1413×10^{-13} A/ $\sqrt{\text{Hz}}$.

Assuming that the noise spectrum is flat for an amplifier with a noise figure of 1 dB and gain of 10 dB, the required input referred noise current of the amplifier is 0.0537 pA/ $\sqrt{\text{Hz}}$. This is the minimum detectable signal of the amplifier, and corresponds to a SNR equal to 1.

4.0 Approach

4.1 Device Technology for Low-noise, High-frequency Preamplifiers

Low noise, linearity and bandwidth are the major factors influencing the design of preamplifiers for optical detectors. The designer not only has to use suitable circuit topologies, but also design a circuit that can meet the noise and frequency requirements. The cutoff frequency of a transistor depends on its electron mobility. In general, the higher the electron mobility, the higher the cutoff frequency and the higher the speed of operation will be. While CMOS has been the workhorse for analog IC development, GaAs-based devices are preferable, especially at higher frequencies due to higher electron mobilities and lower noise. In an n-channel MOSFET device, an electron channel is formed between the source and the drain when a positive voltage is applied to the gate terminal. However, electron-phonon and electron/charged-impurity scattering

in this channel limit the carrier mobility. As a result, the speed of operation of Si-based CMOS technology is significantly limited. On the other hand, the motion of electrons is confined to a thin two-dimensional channel in a GaAs-based HEMT, giving rise to a higher mobility.

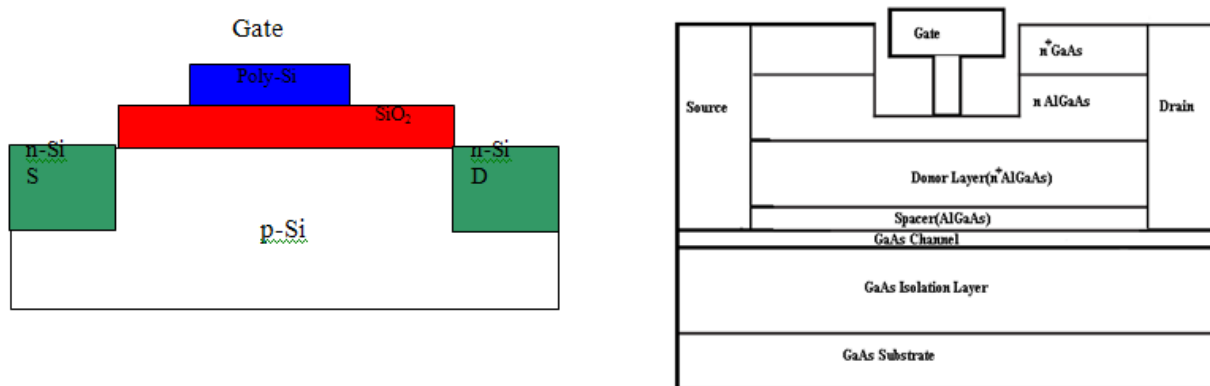


Figure 5: Cross Section of a Si-NMOS (left) and a GaAs HEMT(right)

The HEMT illustrated in Figure 5 has a p-doped GaAs buffer layer grown on a GaAs substrate to prevent electrons from entering the substrate. On top of this buffer layer is an undoped GaAs channel. In between the channel and the donor layer is a spacer layer that prevents the diffusing electrons from returning to the donor layer. The channel layer consists of highly doped AlGaAs. On top of the donor layer is an n-doped AlGaAs layer to which the source and drain terminals are formed. A highly doped GaAs layer is grown above the AlGaAs layer in order to realize low resistance Ohmic contacts. The high electron mobility results from the fact that the electrons' motion is confined to a thin sheet away from the dopant atoms that would otherwise cause scattering. In addition, the substrate is non-conducting (unlike silicon), which leads to lower losses. The higher electron mobility also means lower parasitic drain and source resistances, leading to lower thermal noise.

The basic HEMT structure is being optimized by different variations of the device in several commercial foundries to produce higher cutoff frequencies and improved noise performance. A pHEMT uses a thin InGaAs channel layer with lattice constant greater than that of the underlying GaAs substrate. An InP HEMT uses an InAlAs channel over a lattice matched InP substrate. In a metamorphic HEMT (or mHEMT), the lattice structure of the channel is buffered using epitaxial layers to gradually adjust the lattice constant so it lines up with the donor layer. An InAlAs buffer layer is used between the GaAs substrate and the InGaAs channel. mHEMT devices can offer superior performance to pHEMT ones due to their higher indium content in the channel, which leads to lower channel resistances and thermal noise.

While lattice matched InP HEMTs currently offer the lowest noise figures, mHEMTs are attractive due to their economic advantages and because of the maturity of GaAs technology over that of InP. For example, low cost 4- or 6-inch GaAs substrates are much more easily available than InP substrates.

4.2 Feed-forward Noise Cancellation

While n-channel HEMT devices already offer better noise performance, the thermal noise in these devices can be further reduced by using noise-reduction techniques, especially when the dominant noise source is the thermal noise from the input stage. Consider a basic common-source amplifier, for which the signal and noise paths are shown in Figure 4. The amplifier is fed a voltage V_s through a series resistor R_s . Two different amplification paths are considered. The circuit on the left shows the noise flow path alone and that on the right shows the signal flow path alone. Both noise and signal from the source are amplified by the input transistor (M_1). The thermal noise current ($I_{n,i}$) generated in the channel of transistor M_1 would give rise to noise voltages V_{xn} and V_{yn} at nodes X and Y, respectively. Similarly, the signal input to the transistor is represented by V_x and is amplified at node Y (represented as V_y). The signals at node Y (V_y) and node X (V_x) are opposite in phase due to the phase shift provided by the common source amplifier. However, the noise voltages V_{xn} and V_{yn} at nodes X and Y are in phase with each other.

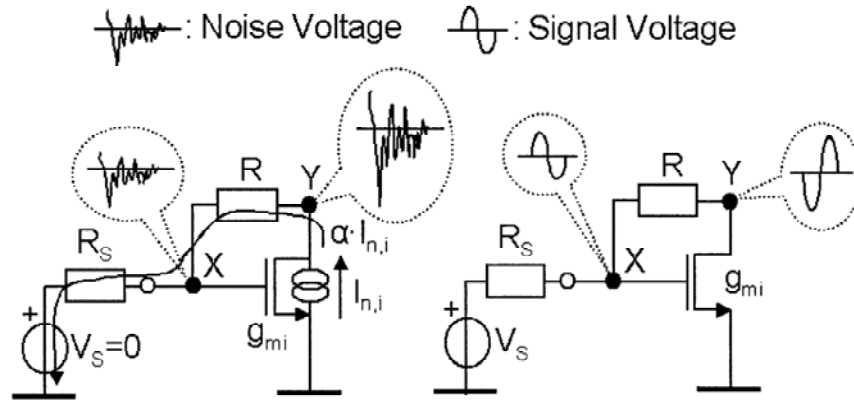


Figure 6: Noise (left) and signal (right) flow paths in a common source amplifier with resistive feedback [1]

If the noise voltages V_{xn} and V_{yn} can somehow be combined in such a way that their net sum is zero, we can cancel the thermal noise from the amplifying transistor M_1 . An auxiliary amplifier can be used to combine the noise voltages V_{xn} and V_{yn} destructively. This auxiliary amplifier stage will consist of a source follower stage as shown in Figure 4. The noise and signal voltages at node X are amplified and shifted in phase by 180° by the lower transistor, which has transconductance g_{m2} . On the other hand, the noise and signal voltages at node Y will appear at the output of the amplifier with no change in amplitude or phase because the upper transistor (which has transconductance g_{m3}) acts as a source follower that simply translates the input at its gate to output at its source without amplification. At the output stage, the signal voltage V_y gets added to a scaled version of voltage V_x , whereas a scaled version of noise voltage V_{xn} is subtracted from V_{yn} . Proper scaling of V_{xn} is needed to make noise cancellation possible. Ignoring the body effect of the transistors, the ideal condition for noise cancellation for the circuit in Figure 6 is

$$\frac{g_{m2}}{g_{m3}} = 1 + \frac{R}{R_s} \quad (5)$$

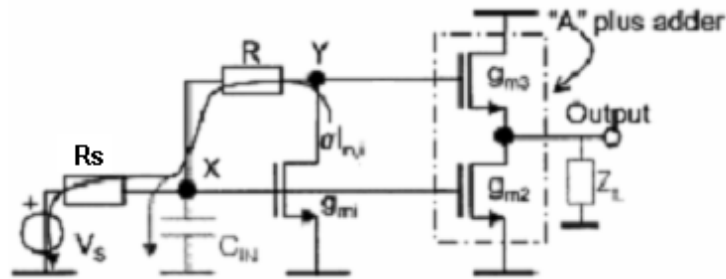


Figure 7: Single-stage common-source amplifier with an auxiliary amplifier for noise cancellation.

5. Phase II Tasks

The ultimate objective of this STTR project was to design, fabricate and test a low-noise infrared-detector amplifier with a noise figure less than 1 dB and a gain of 10 dB, with a bandwidth of 1 GHz. At the end of the Phase II effort, a monolithic low-noise preamplifier was fabricated, tested and prototyped. This section discusses in detail the Phase II objectives, tasks and milestones of the project.

5.1 Task 1: Design and Simulation of the Low Noise Amplifier

The feedforward noise cancellation technique was demonstrated in both 0.18 μm CMOS and 0.15 μm mHEMT technologies through simulations in Phase I. Thermal noise reductions of up to 30% were estimated. In Phase II, a full fledged circuit design was done.

Figure 88 shows the design flow chart for the Phase II effort. Microwave Office from AWR [2] was used for the design and simulation endeavors. The objective was to design and fabricate a low-noise amplifier that operates with low impedance LWIR HgCdTe detectors and a noise-cancellation circuit. In addition to providing the process-design kit and updating the process-design rules, the TriQuint foundry also provided design support by validating device models and providing custom device models.

A small-signal simulation was first performed in order to estimate the small-signal gain, return loss and noise figure. Large-signal device models are required in order to determine the effects of performance on DC bias and linearity. Biasing circuitry consisting of a resistive divider network was used at the transistor gate terminals in order to provide the optimum V_{GS} . The TriQuint foundry also provided models for interconnects such as microstrip tees, bends and power couplers.

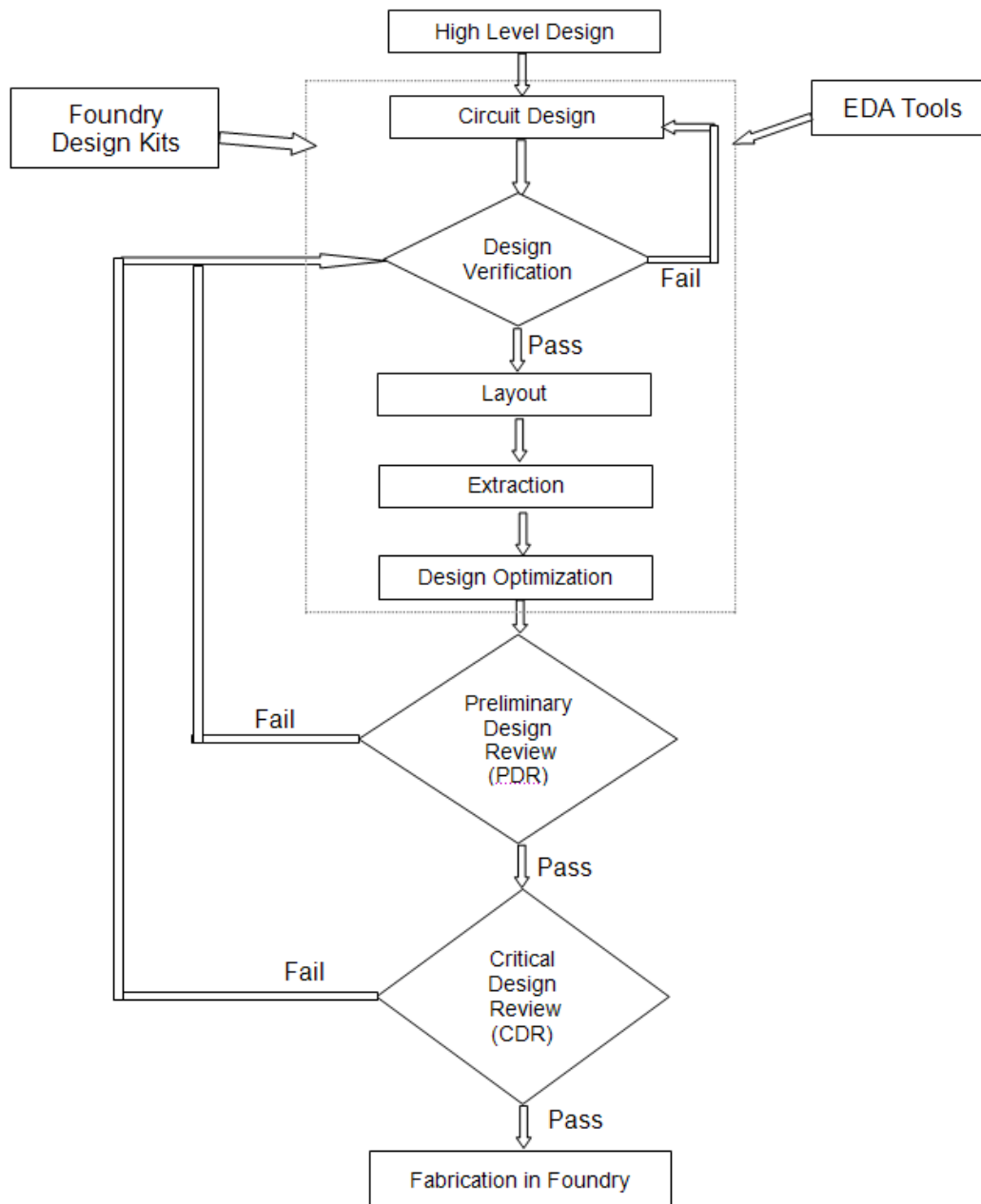


Figure 8: Design process flow

A PDR (preliminary design review) was held on February 17 2010 at the Edgewood Chemical and Biological Center (ECBC). Once the design was approved, the circuit layout was completed and the design underwent a Critical Design Review (CDR) which was held on April 2010. This was followed by submission to the foundry for design-rule checks. The design-rule checker performed physical verification on the width, shape and spacing of different elements in the layout based on the process-dependent parameters. The design rules are a set of guidelines that ensure proper fabrication and function. Some of the categories of these rules are the minimum width, minimum spacing, minimum enclosure. Apart from the parasitics

arising due to interconnect and other passive elements, the transistor layout itself is a major source of parasitic capacitances and resistances that will affect the performance of the circuit. While these parameters are not quite explicit during circuit design, a poor layout can significantly affect the frequency response characteristics, due to the associated parasitics.

5.1.1 Process Technology

The primary requirement for meeting the ultimate goals of this program is the availability of commercial low noise process that can be met at a reasonable budget. Among commercial compound semiconductors device processes, the mHEMT process from TriQuint Semiconductor offers very low noise as well as a high cutoff frequency ($f_T \sim 100$ GHz) while simultaneously offering the benefit of a low cost medium to large scale production. This process was initially chosen for our design.

The TriQuint process supports three metal layers that can be used for interconnects or for realizing capacitors. In addition, there is another low resistance metal layer for realizing vias. The TriQuint 3MI Process allows 3 metal layers in addition to tantalum nitride (TaN). This enables the simultaneous properties of good resistivity, uniformity and a low temperature coefficient of resistivity [3]. Table 1 below summarizes the performance parameters of a typical TriQuint 0.15 μ m mHEMT process.

Table 1: Typical characteristics of the TriQuint 3MI process incorporating a 0.15 μ m mHEMT

Element	Parameter	Designed Values
FET	I_{dss}	225 mA/mm
	G_m	800 mS/mm
	V_{bd}	-3 V
	F_t	135 GHz
Capacitors	Density	240 pF/mm ²
Resistors	Sheet Resistance	50 Ω /sq
GaAs Substrate	Thickness	100 μ m

The TriQuint foundry provided circuit models for the mHEMT devices based on measured parameters for the device. The small-signal and large-signal parameters for each element fabricated in the process formed the basis for creating a behavioral model for each device fabricated by the process. Figure9 below shows a small-signal model of the mHEMT device. A similar model was used in the S-parameter simulations of our circuit. The noise in the device is modeled in terms of the equivalent noise current (i_n) in the channel and the equivalent noise voltage source (v_n).

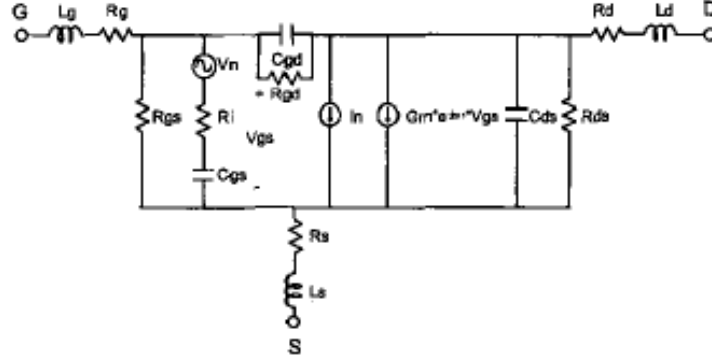


Figure 9: Small-signal model of the mHEMT [4]

Device models are offered for FET's of two different pitch sizes. The mHEMT device model itself is based on the standard EEHEMT model provided by Agilent Technologies. The device parameters such as the gate source capacitance (C_{gs}), drain-source capacitance (C_{ds}) and transconductance (G_m) vary with device scaling. However, the device models are valid only at fixed DC bias conditions. Table 2 below summarizes the properties of the mHEMT devices offered by TriQuint.

Table 2: mHEMT models available in the TriQuint design kit

Gate Pitch (μm)	Number of Gate Fingers	FET Size (μm)(Width)
12 by 18	4	40, 50, 100, 200, 300
20 by 20	4	100, 200

The noise performance of the device model was validated with the foundry. It was determined that the mHEMT device with a 20 μm by 20 μm pitch offers a more accurate noise model than the device with a 12 μm by 18 μm pitch. Therefore, the device with 20 μm by 20 μm pitch was used for all the Phase II design efforts.

An accurate noise model is critical for ultralow-noise amplifier design. While some attempts have been made to develop analytical models, the most commonly used models provided by commercial foundries come in two different flavors: A noisy linear two-port model and a semiempirical small-signal model. In a linear two-port model, the noise source is simply added at the input or output network of the HEMT (as shown in Figure). Noise parameters such as the minimum noise temperature (T_{min}), optimum input impedance match (Z_{opt}) and equivalent noise resistor (R_n) can be determined from the measurement of the noise temperature as a function of input match. However, this method is prone to errors arising from source matching. On the other hand, the semiempirical noise model uses experimentally determined fitting parameters to represent complex physical processes to produce an equivalent noise circuit. The TriQuint foundry provides HEMT devices with two different gate and drain finger spacings: 18 μm and 20 μm . However, only the HEMT devices with 20 μm spacings have an empirical noise model. Therefore, in our design, we used these models. Besides, the TriQuint foundry does not incorporate temperature-dependent characteristics into its device model. Thus, the cryogenic behavior of the LNA could not be estimated prior to tapeout.

5.1.2 LNA Topology

Several topologies for wideband LNAs exist such as cascode, series peaking, and common gate. Our LNA is based on the shunt feedback topology. The shunt feedback gives the best tradeoff between the noise figure and the input matching. A shunt feedback topology with a feedforward noise cancellation stage is shown in Figure 20. The mHEMT device M_1 forms the first amplification stage. The R-C shunt feedback network improves the stability as well as the bandwidth. In addition, the R-C shunt feedback network improves the impedance matching at the input. Transistors M_2 and M_3 form the auxiliary amplifier stage. This is essentially a common-source, source-follower combination and is intended to simultaneously cancel the thermal noise flowing through the channel of M_1 and add the signal voltages occurring at the drain and gate terminals of M_1 , as described in reference [1].

The amplifier was presented with an impedance of $100\ \Omega$ at the input and $50\ \Omega$ at the output. This design was intended to serve as a voltage mode preamplifier for an LWIR HgCdTe infrared detector of impedance $100\ \Omega$. However, the planned input impedance was subsequently changed to $50\ \Omega$ after the PDR. The mHEMT devices were based on large signal EEHEMT models with gate pitch $20\ \mu\text{m}$ by $20\ \mu\text{m}$. The models allow the use of scaling rules and rebasing. The number of fingers in each device is fixed at 4, whereas the width of fingers can be changed to optimize the device dimensions.

Interconnects play a major role in the amplifier performance, especially at microwave frequencies. The simulation results previously provided did not take into account the effect of interconnects. As a result, much of the calculated noise contribution was from the active device alone, and noise from interconnects was largely neglected. Table 3 below lists the electrical properties of the GaAs substrate on which the microstrip lines were fabricated. These characteristics were used for simulating the LNA layout.

Table 3: Electrical properties of the GaAs substrate used for modeling interconnects

Parameter	Value
ϵ_r (relative dielectric constant)	12.9
H (substrate thickness)	$100\ \mu\text{m}$
T (strip line height)	$6.77\ \mu\text{m}$
Rho	1.2
TanD (loss tangent)	0.0004

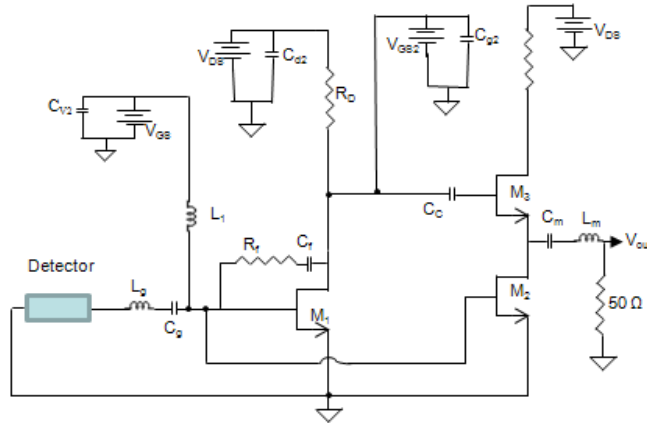


Figure 20: Circuit schematic showing device biasing networks.

The detector was modeled as a $100\ \Omega$ photoconductive device based on the specifications of the HiSpec detector [5]. In order to be able to optimize the bias of each device independently, each was provided with an independent bias supply for V_{DS} and V_{GS} . The bias supply to each device was intended to be provided through bond pads. Shunt capacitors were provided at the bond pads in order to provide isolation from DC power to ground.

S-parameter analysis was performed on the circuit design. All the device models in the circuit are based on large-signal EEHEMT models. The circuit design was optimized by adjusting the matching networks. Figure 31 below plots the noise figures, S_{21} , S_{11} and S_{22} of the amplifier from 100 MHz to 2 GHz. 2.5 dB gain flatness could be achieved between 200 MHz and 1.2 GHz. The noise figure within this band is less than 0.5 dB. While the output return loss is less than 10 dB over this band, the input return is higher at the higher edge of the band. These results are summarized in Table 4.

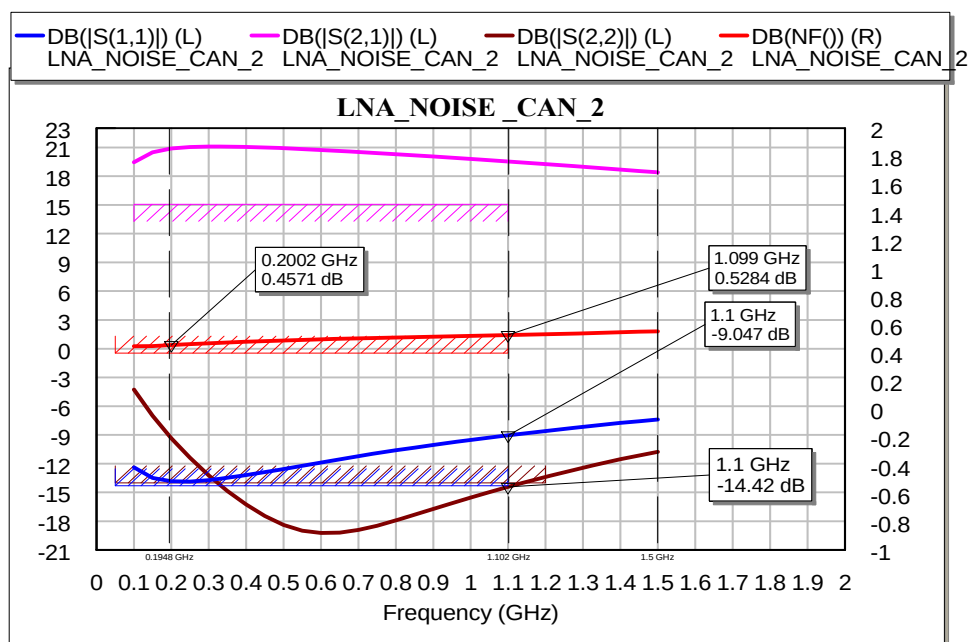


Figure 31: Wide band low noise amplifier design NF and S-parameters using foundry-modeled devices and interconnects

Table 4: Simulated preamplifier characteristics of LNA with 100 Ω input match, 50 Ω output match

Parameter	Value
Frequency	0.1 to 1.1 GHz
Gain	19 dB
Input/Output Return Loss	9 dB
Noise Figure	< 0.6 dB
Drain Voltage	5 Volts
Drain Current	32 mA
Input/Output Impedance	100/50 Ω

A series L-C network was used for matching the detector with the amplifier input. The input return loss was improved by optimizing the series inductor at the input. A major challenge that we encountered in this process was the limited number of discrete inductors provided by the TriQuint foundry for our design. There is no model for the large inductor required for our input matching network. While a series inductor can be realized using a shorted transmission line, [6], the line must be quite long at the frequency of interest (1 GHz). A 4-turn foundry-modeled spiral inductor was used. Also, the FET size and the feedback network were optimized for obtaining an input return loss of less than 10 dB.

While our design targeted an LWIR detector for chemical/biological detection, several commercial applications for the design also exist. The LNA has a remarkably low noise figure, especially for the broad operating frequency range of 100 MHz to 1.2 GHz. Several communication front ends operate in this frequency range (UHF), including GPS receivers, TV tuners, and mobile phones, for which the signal attenuation in the UHF range is more than in the VHF range. All these applications require ultralow-noise front ends in which the LNA is directly connected to the receiving antenna (which usually has a 50 Ω impedance). This implies that the LNA would be matched to the antenna impedance.

During the PDR, the LNA design was validated with our sponsors. A discussion on potential applications of the LNA was held. Based on our sponsor's input, we decided to optimize the design towards commercial applications requiring LNAs with input and output impedances matched to 50 Ω . A discussion of this design and the simulation results follows in Section 5.1.3.

5.1.3 LNA matched to 50 Ω input and output impedances

Taking into account our sponsor's input, an LNA matched to 50 Ω at the input and output was designed. The circuit topology was the same as that in Figure 20. The input matching was optimized to 50 Ω by optimizing the R-C feedback network across M_1 . Figure 42 below is the circuit schematic of the LNA. The design was optimized to improve the input and output return loss to less than 10 dB across the entire frequency band.

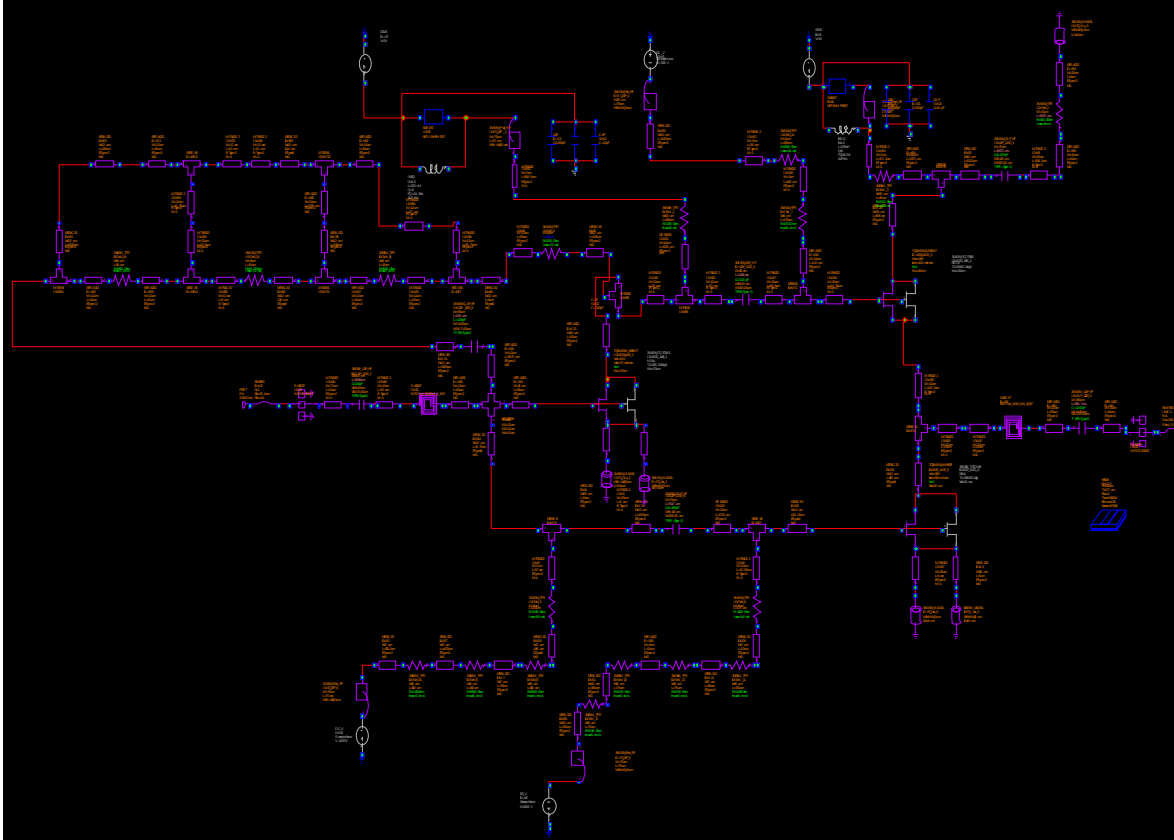


Figure 42: Circuit Schematic of the LNA with input and output terminated with 50 Ω impedances. The feedback in the first stage was implemented as a pi-network.

The nominal operating point for the device is 1 V (V_{DS}) and 100 mA/mm (I_{DS}). Table 5 below summarizes the DC operating point of the mHEMT devices used in the circuit. Since much of the LNA gain was provided by the first-stage transistor M_1 (shown in Figure 20), the size of M_1 was increased. This increased the thermal noise from M_1 . However, the thermal noise current arising from M_1 is cancelled by the auxiliary amplifier stage consisting of M_2 and M_3 .

Table 5: Operating points for the device terminated with 50 Ω impedance inputs and outputs.

Devices	M1	M2	M3
Channel Width (μm)	280	80	160
V_{GS} (Volts)	-0.2	0.8	-0.2
V_{DS} (Volts)	1	0.8	0.8
I_{DS} (mA)	21	8	8

Figure 53 is the layout for the LNA. The layout measures 2 mm by 1 mm. The input and output of the amplifier are connected to G-S-G pads with 150 μm pitch. It was observed that the readily

available foundry-modeled inductors will suffice for the design. 75 μm bond pads were provided at the drain, gate and drain of M_1 , the gates of M_2 and M_3 and the drain of M_3 . The bond-pad size was a tradeoff between the desired bandwidth and return loss and the minimum surface area required for the formation of an ultrasonic ball bond. While a larger bond pad area was favorable from a bonding standpoint, it increased the parasitic capacitance to ground which in turn reduced the bandwidth.

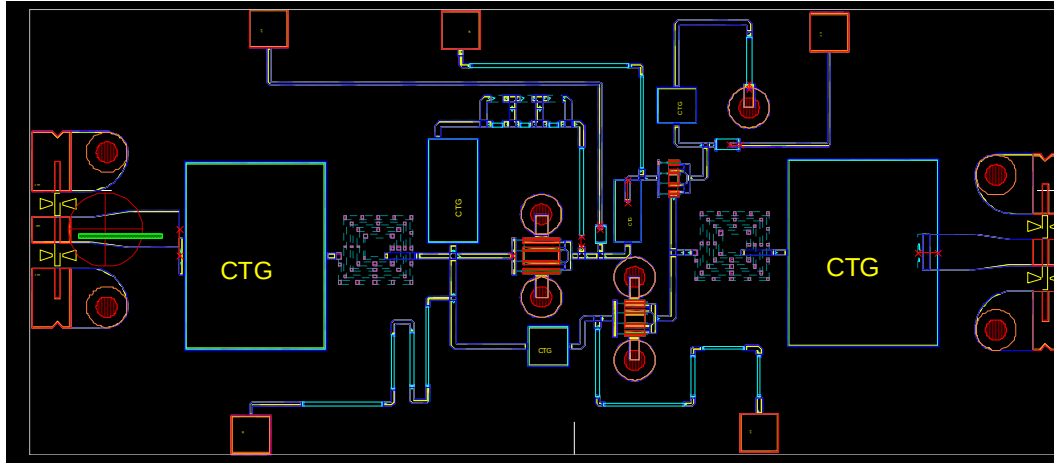


Figure 53: Layout of the mHEMT-based LNA

The circuit requires external biasing networks at the drain terminals of M_1 and M_2 . The biasing network consists primarily of a series inductor and shunt capacitors. Figure 64 below shows the schematic for the bias networks.

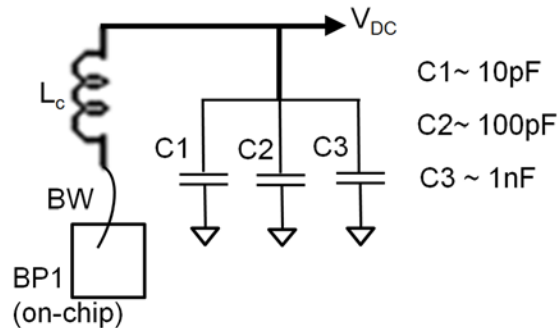


Figure 64: DC biasing network at the drains of M_2 and M_1

In Figure 64, the inductor L_c acts as the RF choke. The inductance of the bond wire was not taken into account for this simulation. Since the operating frequency is below 3 GHz, the inductor L_c is large. On-chip realization of L_c not only requires large real estate, but also causes resistive losses. Such large inductors are not recommended for the 3MI process. Therefore, L_c is realized off-chip and is wirebonded to the LNA MMIC. The inductance of the bond wire is negligible compared to L_c . The capacitors C_1 , C_2 and C_3 filter out any AC from entering the DC power supply at the drain.

5.1.3.1 Small-signal Simulation Results on the mHEMT LNA

Small-signal simulations were performed, followed by large-signal simulations. The simulated small-signal gain was 19 dB from 100 MHz to 1.4 GHz. The input and output of the amplifier were terminated and matched to the 50 Ω source and load impedances, respectively. Figure 75 below is the plot of the simulated small-signal input and output return losses vs frequency. Figure 86 is a plot of the simulated small-signal gain, and Figure 97 is a plot of the small-signal noise figure. The simulated input and output return losses were less than 11 dB from 100 MHz to 1.1 GHz. The simulated small-signal noise figure was less than 0.7 dB over this band.

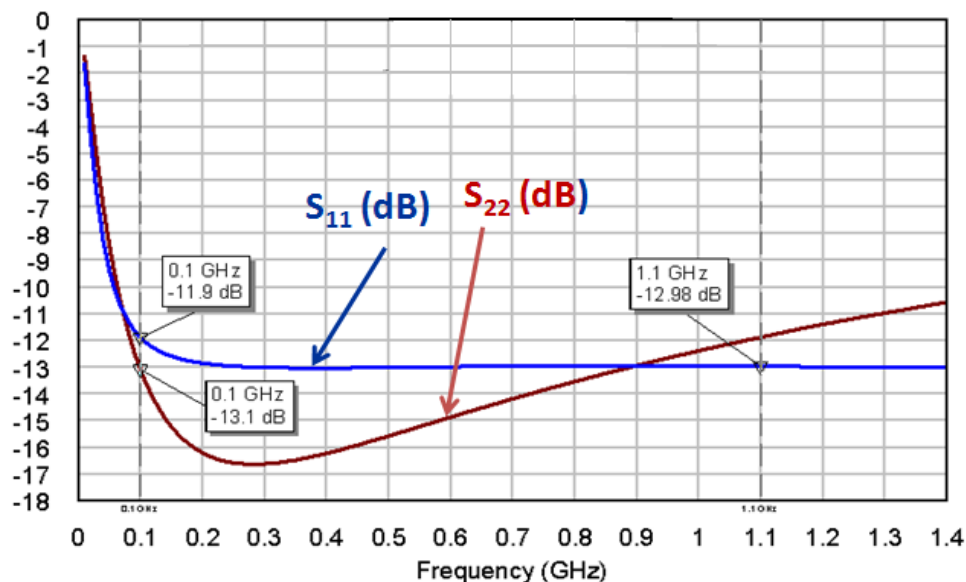


Figure 75: Simulated input (red) and output (blue) return losses in dB for the mHEMT-based LNA with 50 Ω matches at the input and output

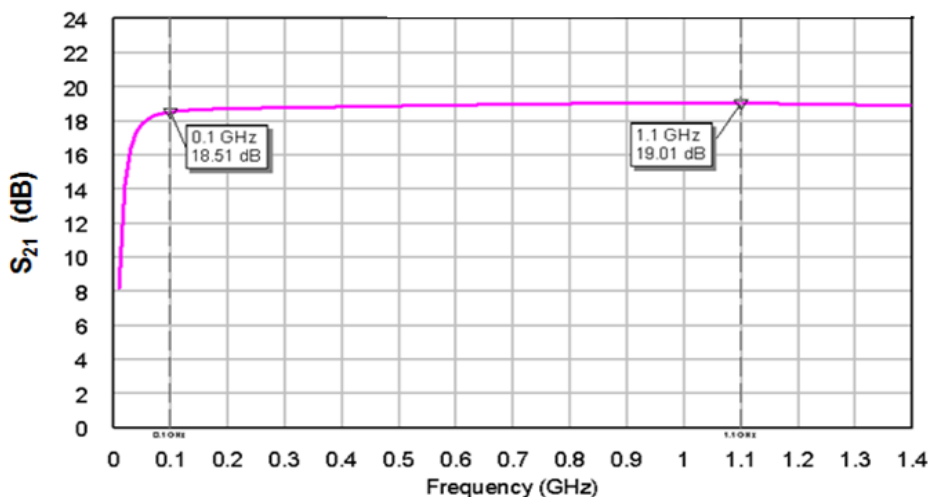


Figure 86: Simulated small-signal gain (S_{21} , dB) with 50 Ω match at the input and output

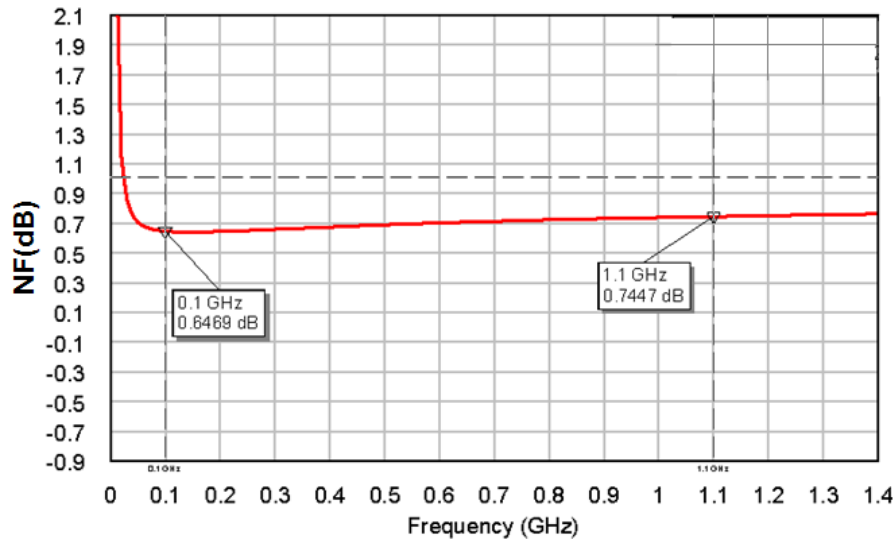


Figure 97: Simulated small-signal noise figure (dB) with 50 Ω match at the input and output

5.1.3.2 Large-Signal Simulation Results on the mHEMT LNA Matched to 50 Ω Impedances

The TOM 3(TriQuint's Own Model) nonlinear model was used for performing large-signal simulations on the LNA. The simulated large-signal gain was close to the simulated small signal gain. Figure 108 below is a plot of the simulated large-signal S-parameters (large signal gain and return loss) and Figure 1919 is a plot of the simulated large-signal noise figure.

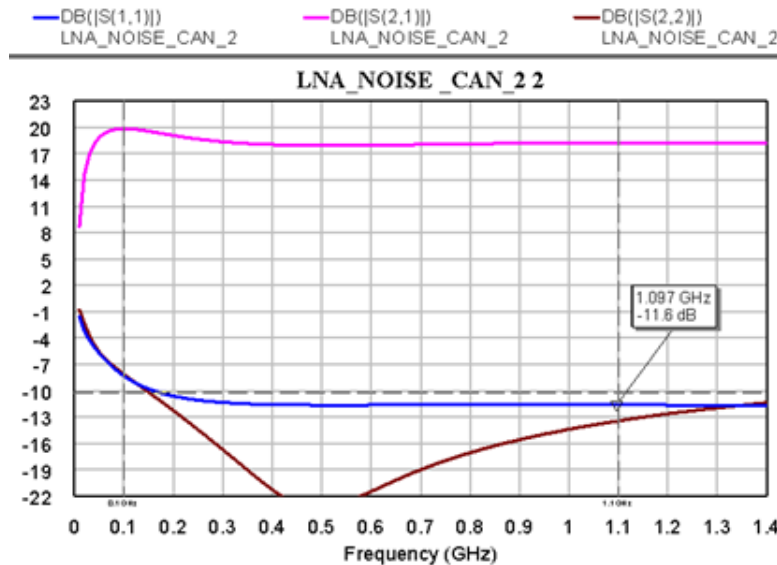


Figure 108: Simulated large-signal gain(S21, dB, pink), large-signal input return loss (S11, dB, blue) and output return loss (S22, dB, brown)

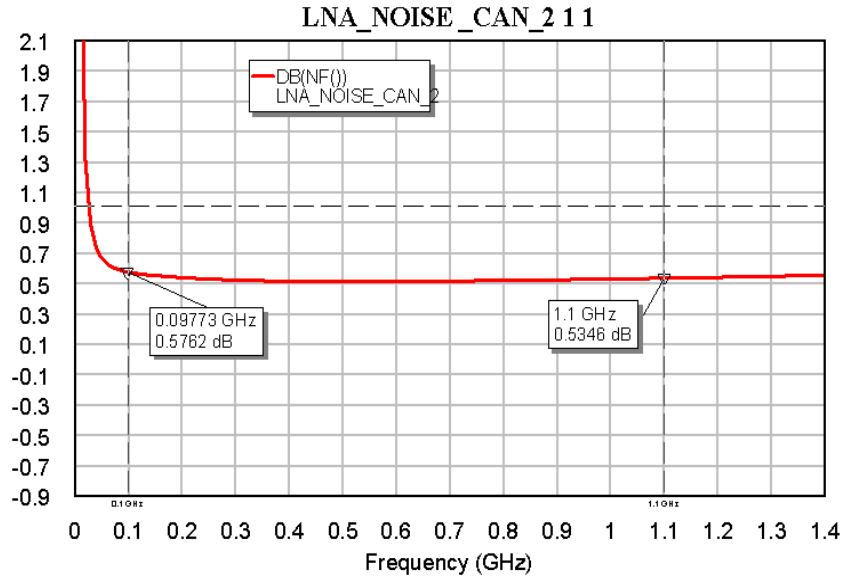


Figure 19: Simulated Large Signal Noise Figure

Harmonic-balance analysis was performed to determine the 1-dB gain compression point and the third-order intercept point. For simulating the gain compression, the input power to the LNA was swept from -100 dBm to 0 dBm. The simulated amplifier gain was found to drop by 1 dB at an input power of -7 dBm. This simulation was performed by simultaneously sweeping the input frequency from 100 MHz to 1.1 GHz. Figure 110 below is a plot of the simulation gain and output power with respect to input power.

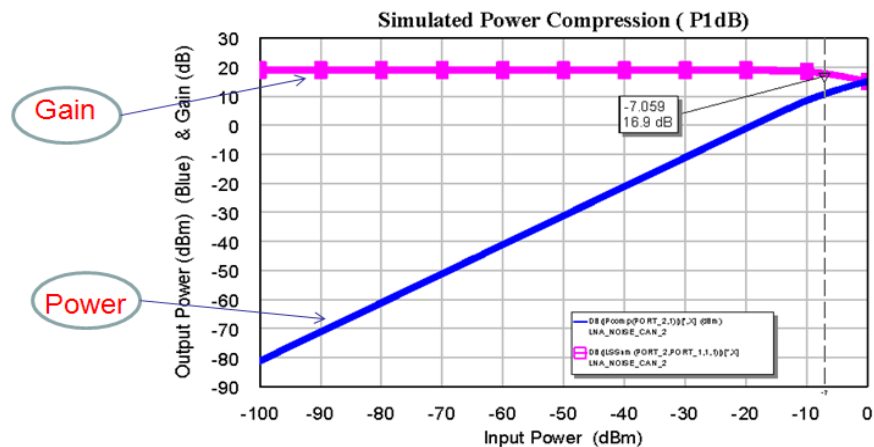


Figure 110: Simulated gain compression point of the mHEMT LNA

In order to simulate harmonic distortion, the amplifier was simulated using a two-tone input signal with frequency separation 10 MHz. The two-tone signals were swept from 100 MHz to 1.1 GHz and the output third-order intercept point was calculated from the equation

$$OIP_3(dBm) = 0.5 \times (3 \times \text{Output Power}(dBm)(\text{fundamental frequency}) - \text{Output Power}(\text{intermodulation frequency})(dBm)) \quad (6)$$

Figure 121 below is a plot of the simulated output third-order intercept point vs. frequency at -30 dBm input power, and Table 6 summarizes the simulated performance of the LNA.

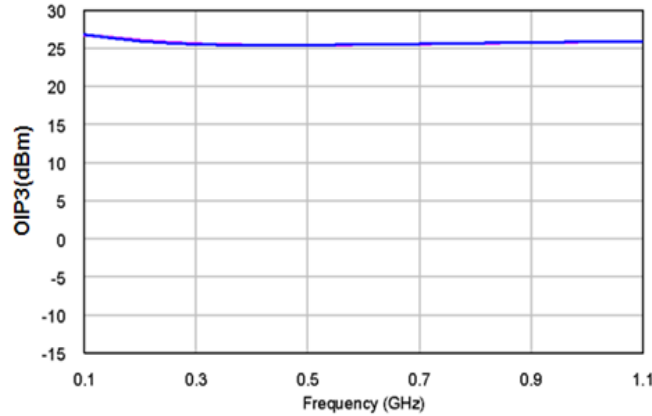


Figure 121: Simulated OIP3 (dBm) vs. frequency of the mHEMT LNA

Table 6: Summary of simulated performance of the mHEMT LNA matched to 50 Ω at input and output

Parameter	Value
Frequency Range (GHz)	0.1 to 1.1
Gain (dB)	19
Input Return Loss (dB)	<-11
Output Return Loss (dB)	<-12
Noise Figure (dB)	< 0.7
Power Supply Voltage (V)	3
DC Current (mA)	32
Stability Factor (K)	>1
Output Third order intercept point (dBm)	25

5.1.3.3 Effect of Feedback Resistor

Shunt feedback was used to increase the bandwidth. It was implemented using the R-C network shown in Figure 132 consisting of resistor R_2 and DC blocking Capacitor C_4 . Decreasing R_2 will

decrease the feedback gain and improve the bandwidth in addition to the input return loss. However, it will degrade the noise figure. On the other hand, increasing the feedback resistance will reduce the noise figure but degrade the input return loss. A thin film TaN resistor was used for the feedback resistor. In the layout a series-shunt combination of 3 tuning resistors was used for this resistance. The tuning is in steps of $100\ \Omega$ and can be activated by laser trimming the bridge. Figure 132 shows the layout of the tuning resistors. Figure 143 plots the changes in gain and input return loss with frequency, and Figure 154 plots the change in the noise figure with increasing feedback resistance.

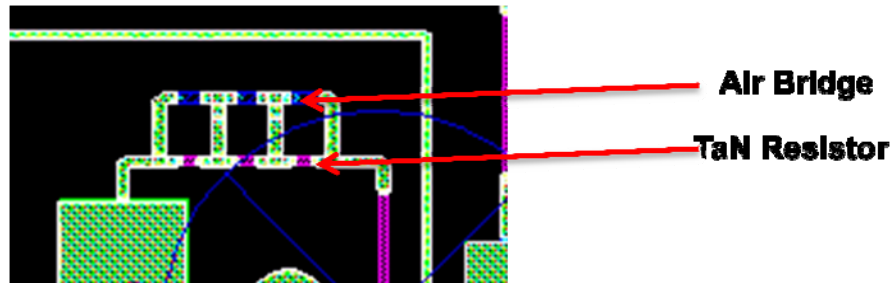


Figure 132: Implementation of feedback resistance

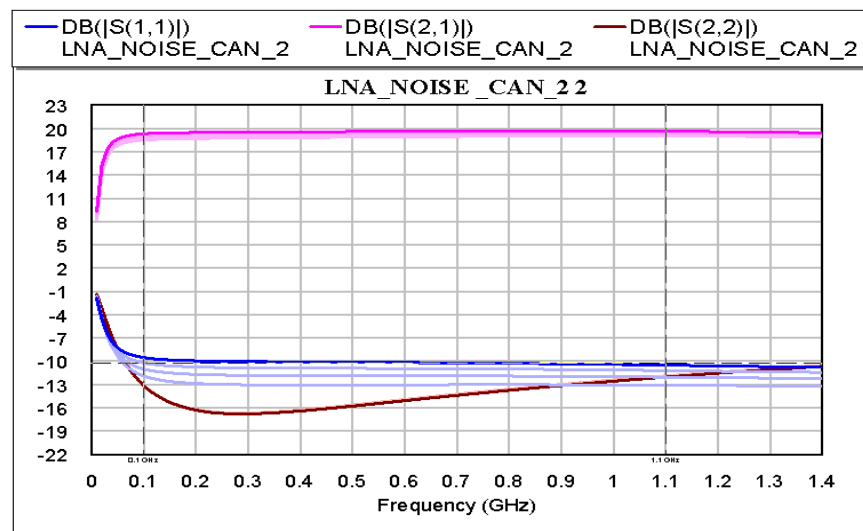


Figure 143: Gain(S21, pink (dB)) and input return loss (S11, dB, blue) and output return loss (S22, dB, brown) vs. frequency. Gain drops as the feedback resistance is reduced. Input return loss improves as the feedback resistance is reduced.

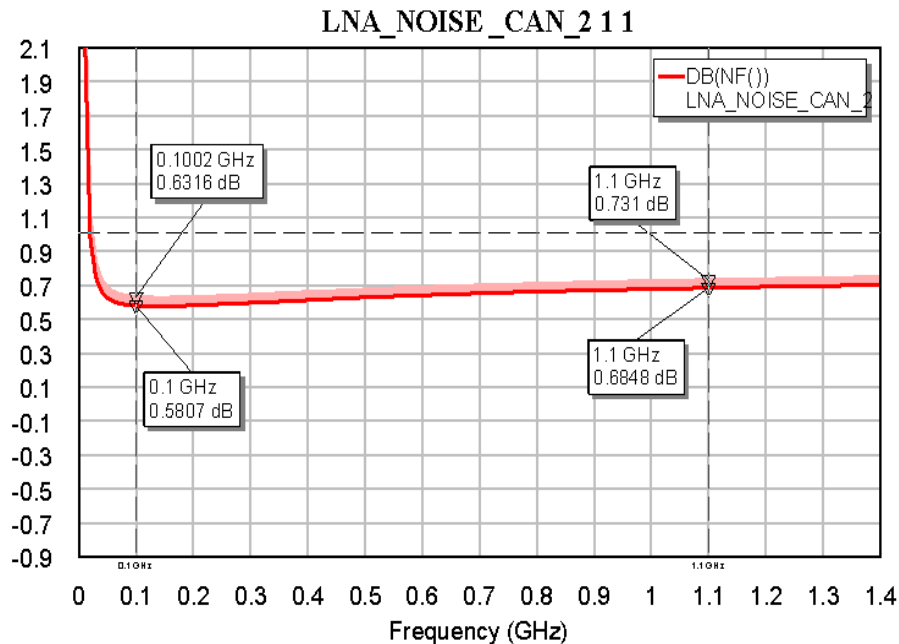


Figure 154: Noise Figure Vs frequency of mHEMT LNA. Noise Figure decreases as feedback resistance increases

Figure 165 shows the layout of the mHEMT low-noise amplifier. The primary method of biasing the LNA is through the L-C network shown in Figure 64. However, our design also incorporates additional resistors at the drain terminal in the event of the nonavailability of inductors. This feature is especially useful when the MMIC LNA must be integrated with the rest of the signal flow electronics such as a down converter or a filter. It is intended to provide DC bias to the drain pads through off-chip circuitry. As shown in Figure 14, we have also provided for on-chip bias networks that can override the off chip network. This is done using the “test pads” as shown in Figure 165. These pads are connected to the drain of Q_1 and Q_2 through on-chip resistors.

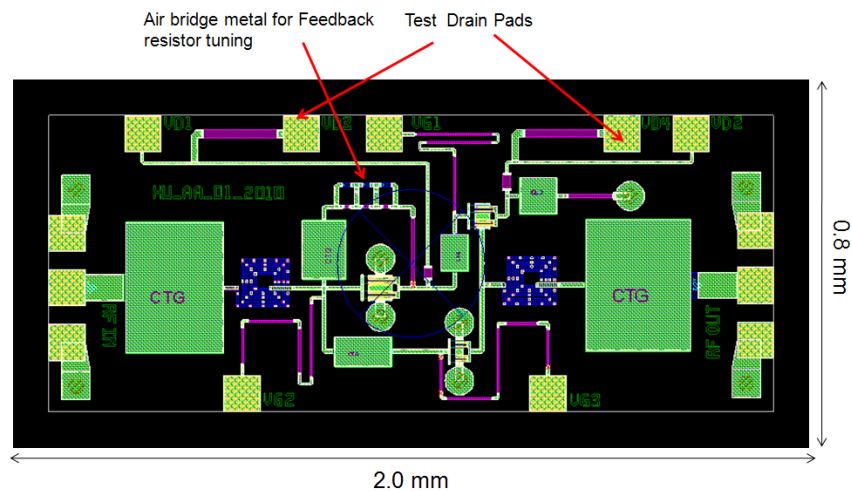


Figure 165: Final layout of the mHEMT-based LNA.

The ultimate goal of the program is to develop an LNA suitable for cryogenic operations. However, the foundry does not provide temperature dependent models for active or passive

devices. Therefore, it is necessary to develop device models for 77 K operation in the event that the chip fabricated in the first foundry run fails. For this purpose, we have also added test structures to the layout. The test structures are as follows:

1. Active Devices: mHEMT devices of the same dimensions as Q₁, Q₂ and Q₃.
2. Passive Devices: 3MI inductor, TaN resistor and MIM capacitor

Figure 176 below shows the layout of the test structures.

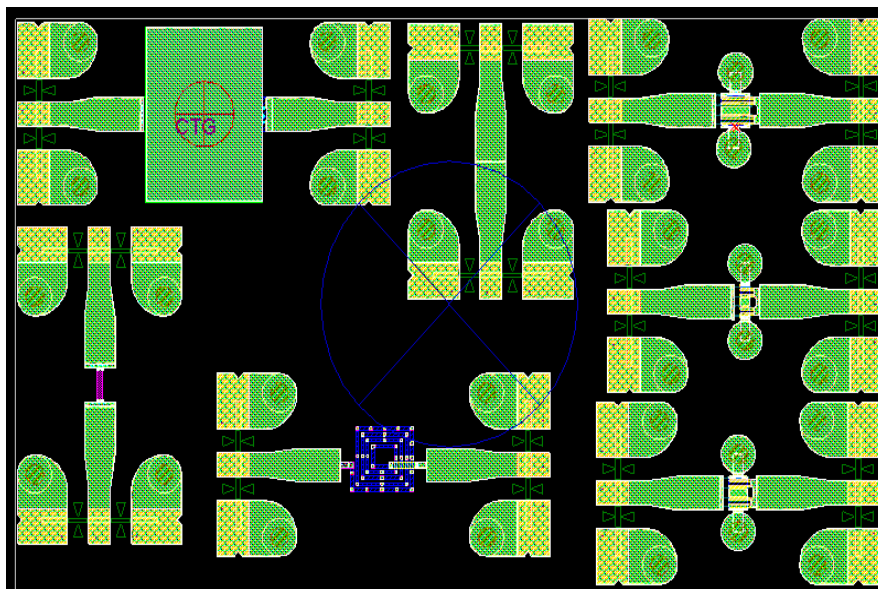


Figure 176: Structures for characterization of devices at cryogenic temperatures

5.2 Migration to 0.15 μ m PWR pHEMT Process

The mHEMT based LNA design was submitted to the TriQuint foundry on April 30th, 2010 for fabrication. The design passed the online DRCs (Design Rule Checks). Two foundry iterations were initially proposed for the LNA fabrication. However, the TriQuint foundry phased out the mHEMT process. As a result we redirected our design efforts towards a pHEMT based design. The closest possible feature size was selected for the PHEMT process from TriQuint. The 0.15 μ m PWR PHEMT process was selected to replace the mHEMT process.

The various layers in a HEMT structure are typically grown by epitaxy. Molecular beam epitaxy usually results in the highest quality growth only when all layers are lattice-matched. However, pHEMT growth can permit some mismatches. The formation of a heterojunction for the channel entails creating a sufficient degree of difference between the bandgap of the donor and channel layers. In the original GaAs/AlGaAs HEMT structure, this bandgap difference was increased by increasing the mole fraction of aluminum. This, however, results in the creation of electron traps that reduce the channel conductivity. Another option is to grow an alloy of GaAs with narrow bandgap materials such as InGaAs over the channel layer. Such a layer is extremely thin, so the

lattice constant of this layer expands to form a lattice matched GaAs/InGaAs interface. This structure allows materials with different lattice constants to be incorporated into the device, and therefore gives us more freedom of selection of materials to obtain the desired large bandgap difference. Larger bandgap differences produce higher carrier densities, higher electron mobilities and higher output conductance.

Figure 187 below is a plot of NF_{min} versus frequency for a 400 μm pHEMT device. The NF_{min} for the 3MI pHEMT is approximately 0.7 dB at 12GHz. While both the processes have several features in common, the pHEMT process offers a much higher power density and can operate up to a 6V drain voltage.

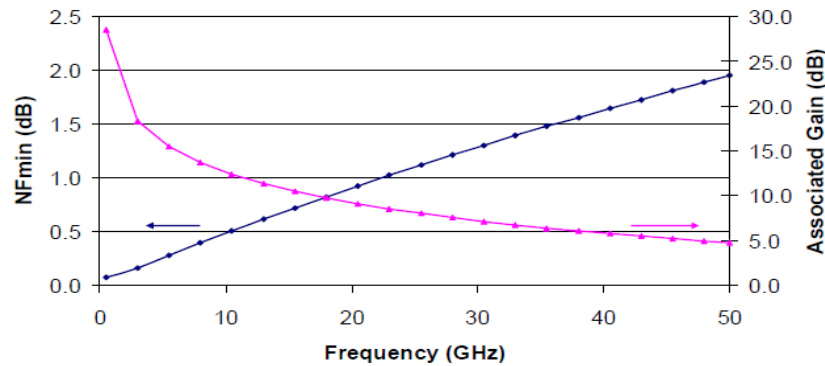


Figure 187: NF_{min} Vs Frequency for a 0.15 μm pHEMT device of channel width 400 μm at 6V, 30mA

5.2.1 Design and Simulation of an LNA based on the 0.15 μm pHEMT Process

A pHEMT-based LNA was designed using a similar topology, as described in Section 5.1.3. Microwave Office from AWR Corp. was used for our design and the simulation endeavors. In order to obtain similar performance, the device size had to be made larger. Table 7 below summarizes the DC operating points of the devices in the LNA. Figure 198 shows an AWR screen capture of the LNA.

Table 7: DC operating points of the devices in the PHEMT LNA

Devices	Q1	Q2	Q3
Area (μm)	360	200	100
Vgs (Volts)	-0.63	-0.834	-0.776
Vds (Volts)	3	1.5	1.5
Ids (mA/mm)	75	50	100

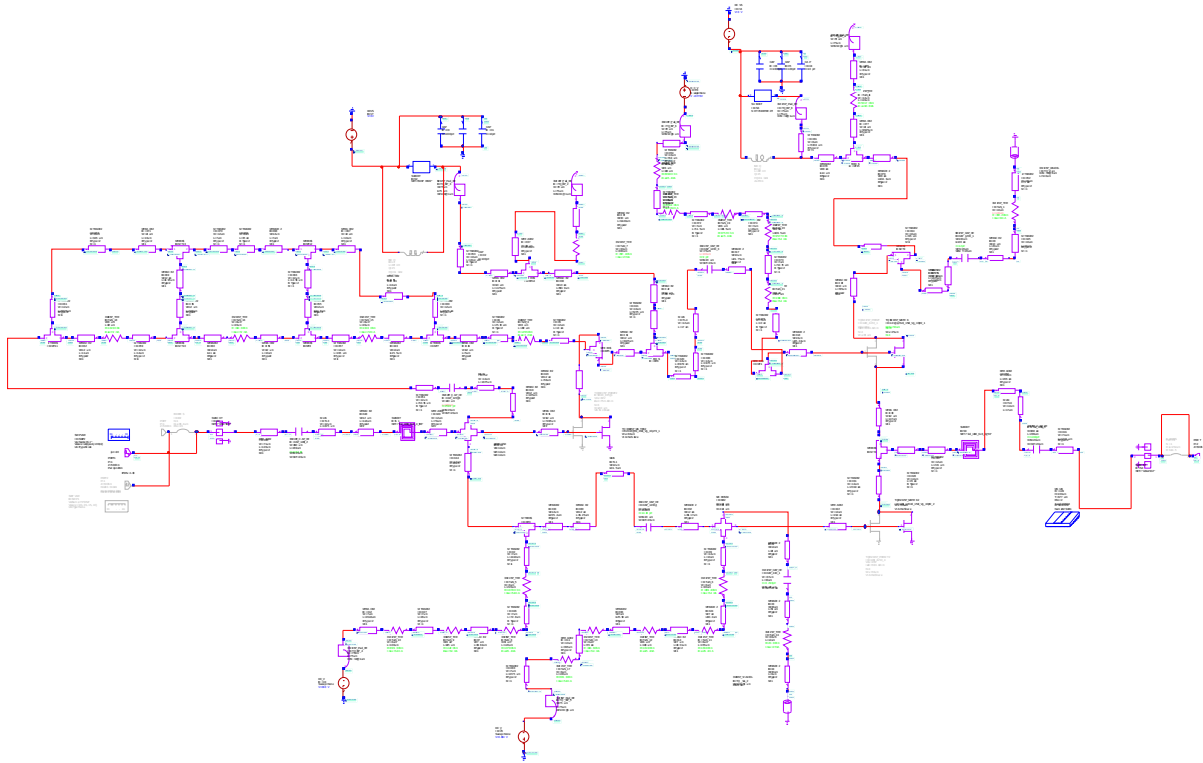


Figure 198: AWR screen capture of the LNA

5.2.2 Simulation Results

Small-signal simulations were performed followed by large-signal simulations. The simulated small-signal gain was 19dB from 100MHz to 1.4GHz. The input and output of the amplifier were terminated with 50 Ω source and load impedances. Figure 29 below plots the simulated small-signal input and output return loss vs. frequency. Figure 200 plots the simulated small signal gain, and Figure 211 plots the small-signal noise figure. The simulated input and output return losses were less than 11 dB from 100MHz to 1.1GHz. The simulated small-signal noise figure was less than 0.7 dB over this band.

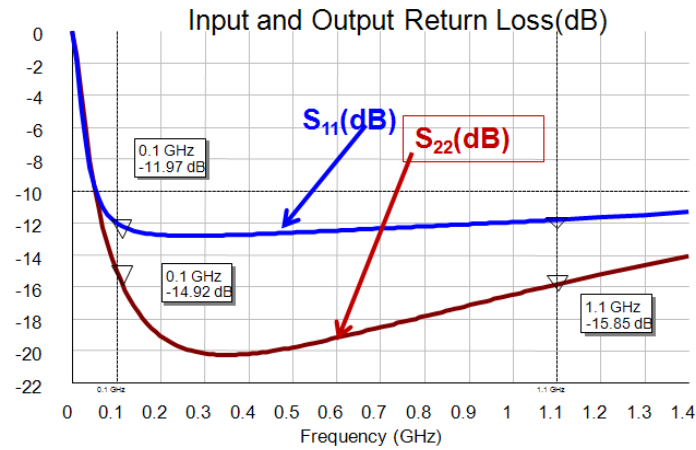


Figure 29: Simulated input (red) and output (blue) return losses in dB for the pHEMT-based LNA

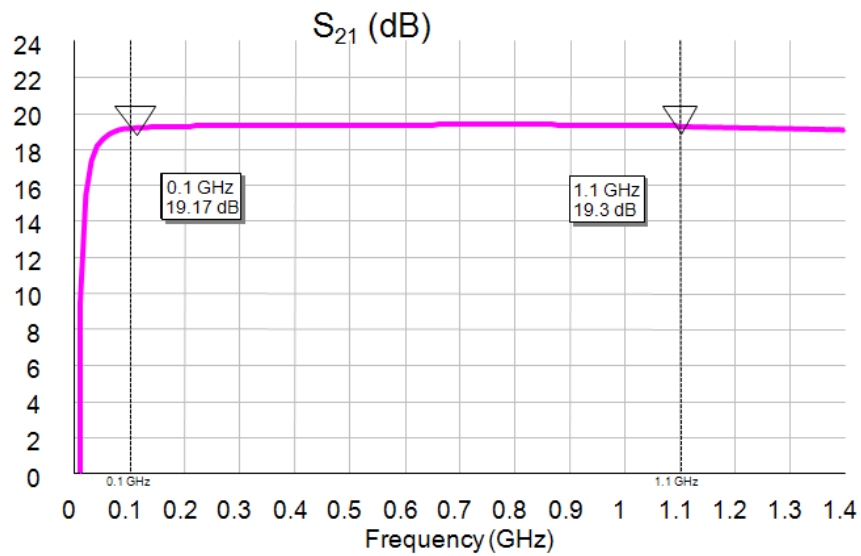


Figure 200: Simulated small-signal gain (S_{21} , dB)

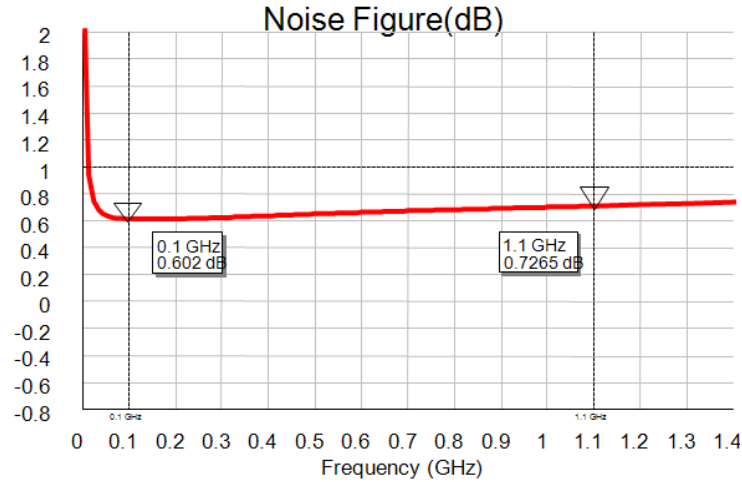


Figure 211: Simulated small-signal noise figure(dB)

Table 8 below summarizes the simulated performance of the LNA designed using the 0.15 μ m PHEMT process.

Table 8: Summary of simulated performance of the LNA-based on the 0.15 μ m pHEMT process

Parameter	Value
Frequency Range (GHz)	0.1 to 1.4
Drain Voltage (V)	3
Total Current (mA)	38
Gain (dB)	19 .3
Input Return Loss (dB)	<-11
Output Return Loss (dB)	<-12
Noise Figure (dB)	$0.6 < NF < 0.73$ (dB)
Power Supply Voltage (V)	3
DC Current (mA)	32
Stability Factor (K)	>1 up to 50GHz
Output Third order intercept point (dBm)	25

5.3: Foundry Tapeout and Test Board Design

5.3.1 Final Layout

After submission to the foundry, Design Rule Checks (DRC) were performed, and the design was modified to satisfy the foundry design rules. Figure 222 below shows the layout of the MMIC LNA designed using the 0.15 μm PHEHT process. The DC bond pads are 75 μm by 75 μm . These bond pads are wirebonded to a circuit board. In addition to the LNA, test structures were also submitted to the foundry for fabrication in order to determine the cryogenic performance of the process. Figure 233 shows the test structure layout.

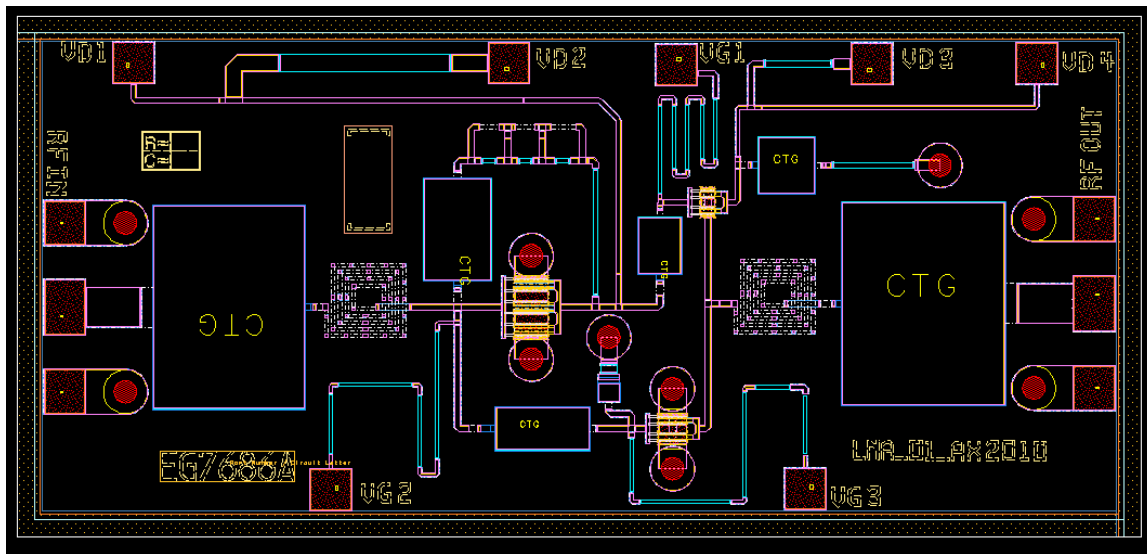


Figure 222: Finalized layout of the MMIC LNA

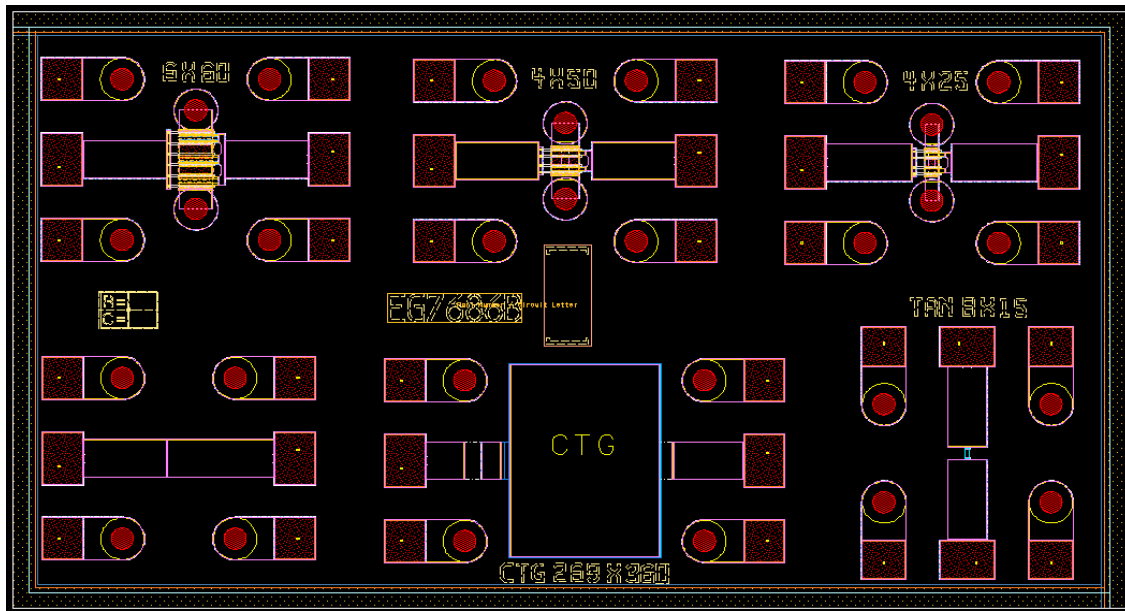


Figure 233: Finalized layout of the test structures.

The MMIC design was taped out in May, 2010. The fabricated bare die was shipped from TriQuint in August, 2011. During the foundry fabrication stage, a test fixture was designed for the MMIC. The test fixture is used for providing DC bias to the MMIC, holds the off-chip inductors and bypass capacitors.

5.3.2. Complete LNA Assembly

Figure 244 below shows the schematic of the LNA. Inductors L1 and L3 act as the RF Choke (RFC) required for high-frequency gain by providing a high impedance path for the RF to the ground. In addition to the RFC, a bank of shunt capacitors is required at the drain terminal of the pHEMT devices EEHEMT_1 and EEHEMT_2. This bank of capacitors acts to eliminate oscillations induced due to the inductance of the DC probes. The DC probes are used to provide the bias as well as to act as a DC bypass cap. Fabricating these passives on-chip consumes a huge amount of real estate. Therefore, they must be realized off-chip. Additional off-chip DC bypass capacitors may also be used at gate terminals if there are oscillations. Therefore, the LNA is a hybrid circuit consisting of an MMIC core and passives for biasing.

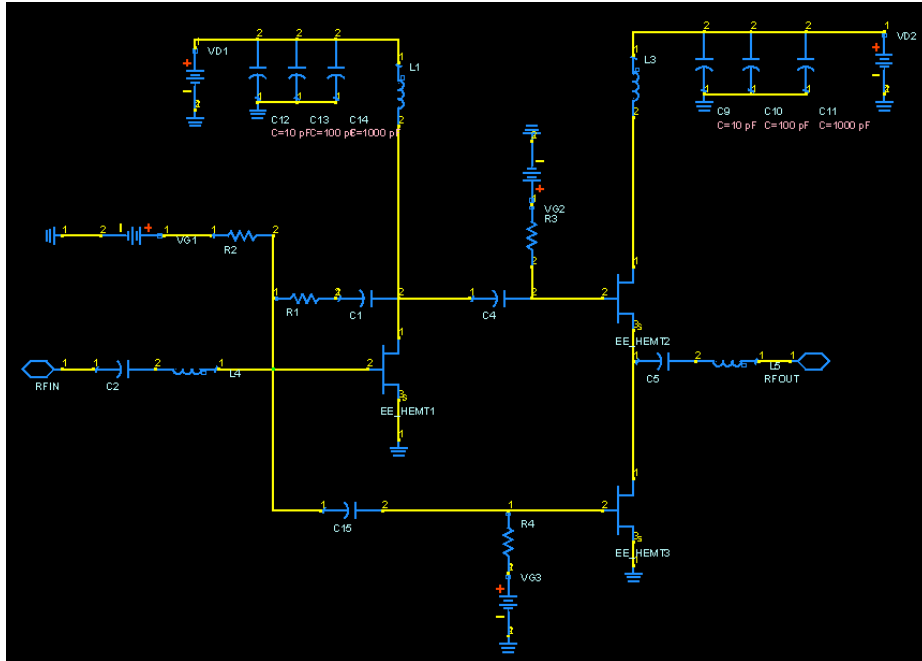


Figure 244: Topology of the LNA assembly showing the biasing circuits

Table 9: Off-chip components used for biasing the LNA MMIC

Component	Function	Dimensions (mm * mm)	Quantity per Board
Capacitor SMT 10 pF, 100 V, $\pm 10\%$ tolerance	Bypass Cap	0.6 * 0.6	5
Capacitor SMT 100 pF, $\pm 15\%$ tolerance, 50 V	Bypass Cap	0.6 * 0.6	5
Capacitor SMT 1000 pF, $\pm 15\%$ tolerance, 16 V	Bypass Cap	2.7 * 2.7	5
Wirewound inductor, ceramic core 470 nH, $\pm 15\%$ tolerance	RFC	1.12 * 0.55	2

The passives and the MMICs were assembled on a circuit board. A two-layer board was designed using ADS. The bottom layer is copper and provides the ground for the MMIC. The top layer contains the traces connecting the different components. The MMIC is placed in the center of the board and the MMIC bond bands are wirebonded to the traces. The bottom side of the MMIC is conducting and contains an 8 μm thick gold backing that provides the RF ground. The RF ground and the DC ground are connected through the traces. The MMIC is mounted on the board using electrically conductive epoxy. Cryogenic performance was a criterion for the

selection of the epoxy. Specifically, EPOTEK H20E was used. Figure 255 below shows the layout of the circuit board. The MMIC was mounted in the center of the board, as shown in Figure 266. The trace width was 100 μm , which is the minimum allowable width for the process. The vias connecting the top-layer ground pads and the bottom layer of the board are 250 μm in diameter.

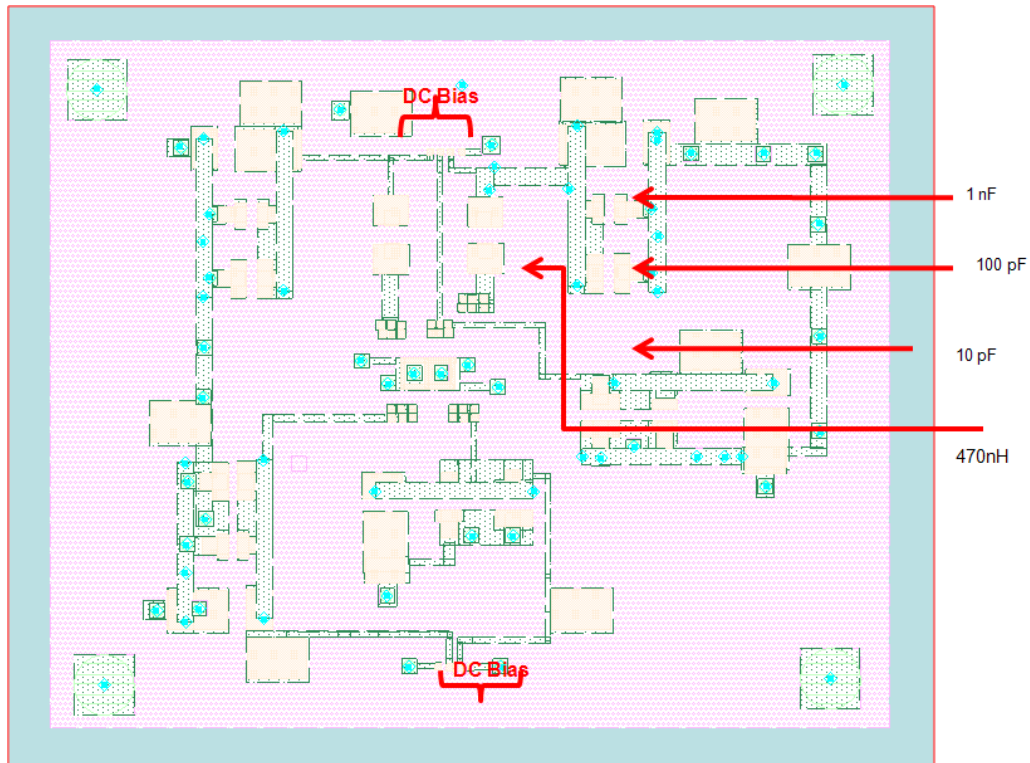


Figure 255: Board layout showing the location of the passive components

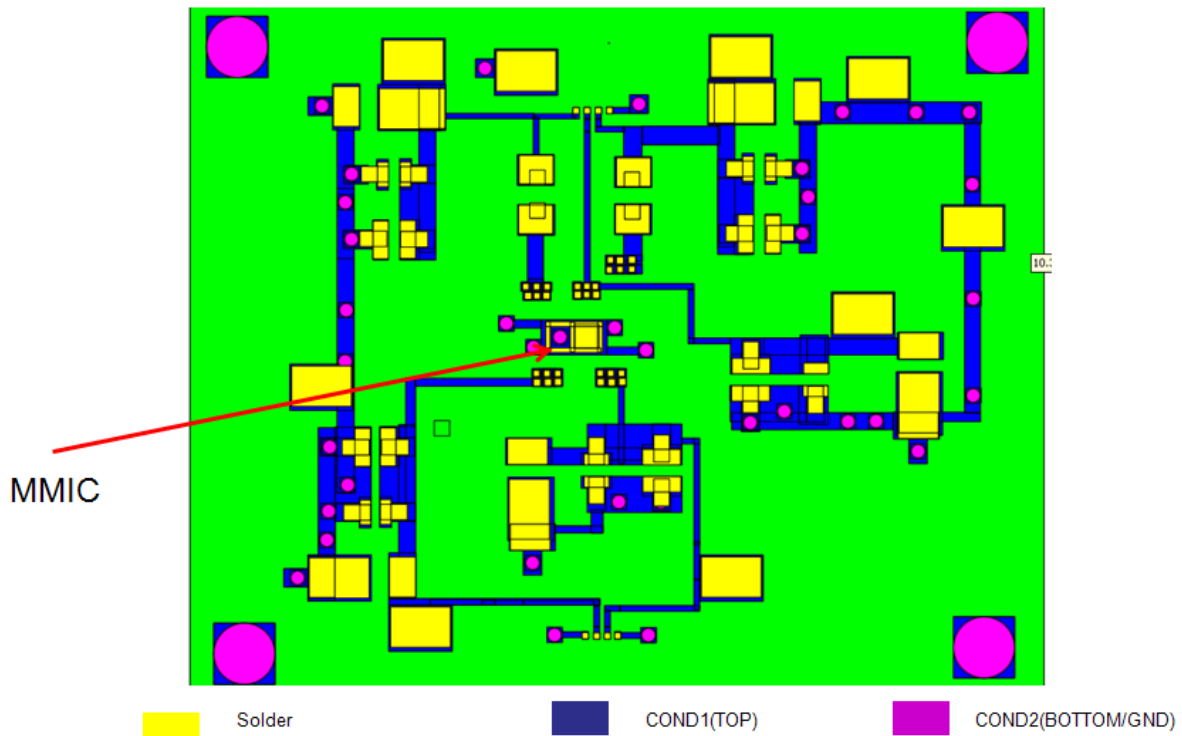


Figure 266: AutoCAD Drawing of the two-layer board

Where the passive elements are to be mounted, a solder mask was coated with tin/silver to help solder the passives. However, the passives were mounted on the board using electrically conductive epoxy as the initial results of soldering small structures were not encouraging. The bond pads on the MMIC were then wirebonded to the board using 0.75 mil gold wire. Figure 277 below is a photograph of the MMIC wirebonded to the board.

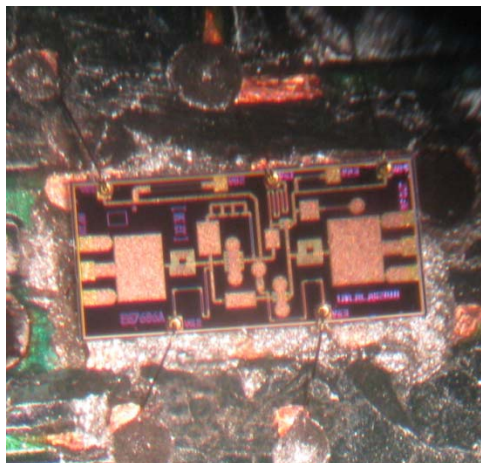


Figure 277: Photo of a MMIC wirebonded to a custom circuit board as described in Figure 255

The DC bias to the MMIC is applied through the board whereas the RF probing for the LNA was done by directly probing the MMIC through the G-S-G probes. Figure 288 below shows the assembled board.

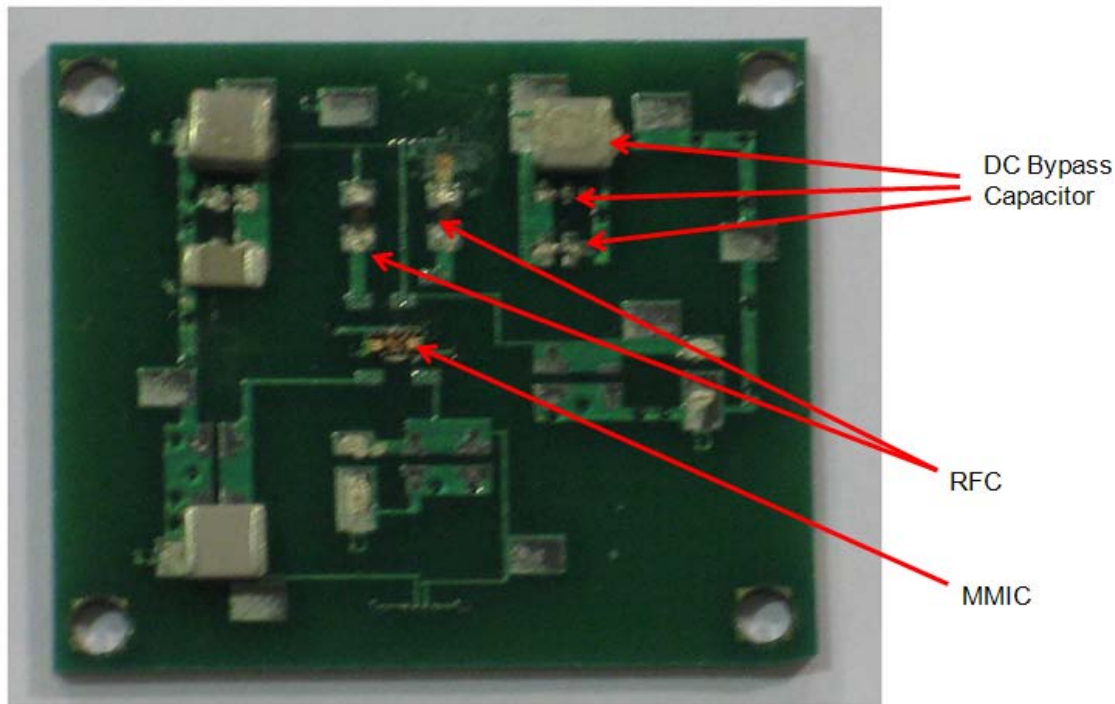


Figure 28: Assembled circuit board

5.4. Measurements on MMIC LNA: Ambient Temperature

5.4.1 Small-signal S-parameters at aAmbient Temperature (300K)

Small-signal S-parameter measurements were performed using the Agilent E8362C PNA (programmable network analyzer). Specifically, the amplifier gains (S_{21}), input return loss (S_{11}) and output return loss (S_{22}) were measured. These measurements were performed under various DC biasing conditions. The network analyzer was calibrated using the CS-5 impedance standard substrate [8]. Table 10 below lists the DC biasing conditions at which the LNA was tested. Figure 39 below shows a plot of the measured small-signal gain (S_{21}) in dB under different biasing conditions. The measured gain was close to 20 dB between 100 MHz and 1.1 GHz at bias point 1, which is closest to the simulated DC operating point. Figure 290 plots the measured input reflection coefficient (S_{11}) in dB under different biasing conditions. The S_{11} is less than -10 dB at bias point 1 between 100 MHz and 1.1 GHz, the frequency band of interest. Figure 301 plots the measured output reflection coefficient (S_{22}) in dB under different biasing conditions. The measured S_{22} is less than -10 dB across the frequency band of interest at bias point 1.

Table 10: Biasing Conditions for the MMIC LNA (at 300K)

Biasing Point	V_{G1} (V)	V_{D1} (V)	I_{D1} (mA)	V_{G2} (V)	V_{G3} (V)	V_{D2} (V)	I_{D2} (mA)
1	-0.53	3	25	0.8	-0.54	3	12
2	-0.63	3	14	0.8	-0.54	3	12
3	-0.54	3	28	0.8	-0.54	3	12
4	-0.53	3.5	27	0.8	-0.54	3	12
5	-0.53	3	25	0.9	-0.54	3	13

As the DC current in the input stage increases, the gain increases. This can be observed by the drop in gain (as shown in Figure 39) between bias point 2 and bias point 3, at which the DC current in the input stage has nearly doubled. This corresponds to an increase in gain of ~ 1.5 dB at a frequency of 1.5 GHz. Similarly, the input return loss improves as the DC current through the input stage increases (as shown in Figure 40).

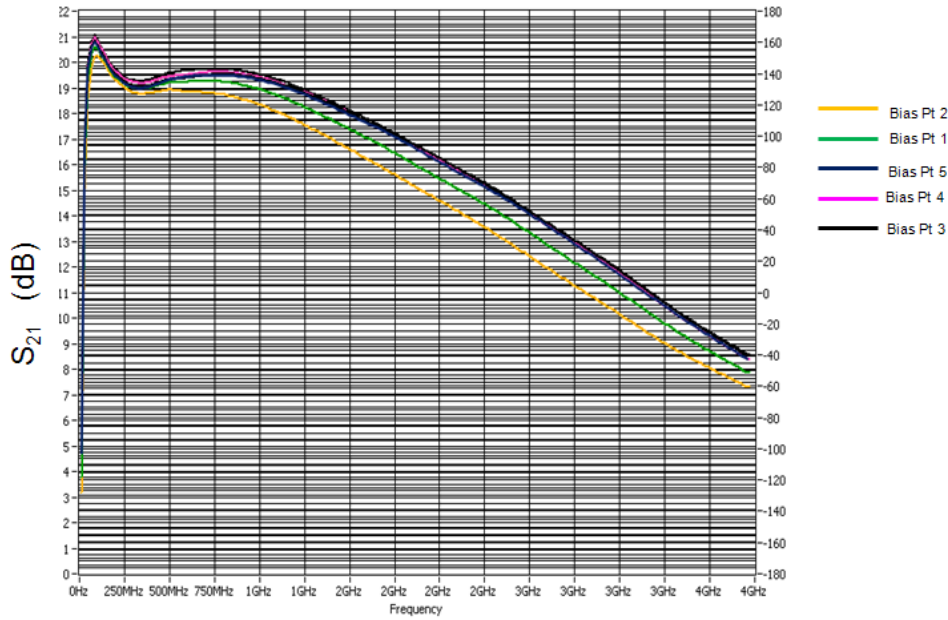


Figure 39: Measured gain (S_{21} in dB) under different bias conditions at 300 K. The gain increases with the DC current flowing through the input and the auxiliary amplifier stage.

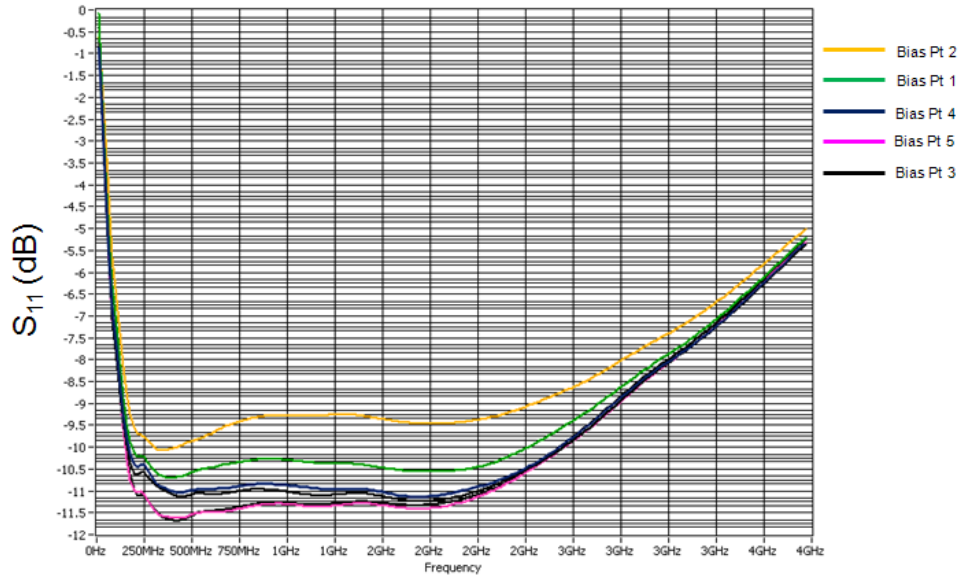


Figure 290: Measured input return loss (S_{11} in dB) under different bias conditions at 300 K.

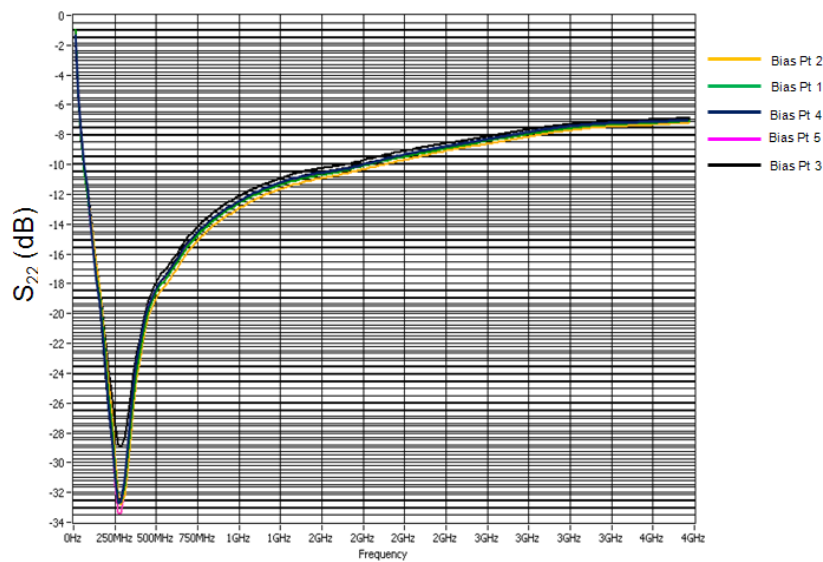


Figure 301: Measured output return loss (S_{22} in dB) under different bias conditions at 300 K.

5.4.2 Amplifier nonlinearity measurements

The input power to the LNA was increased from -24 dBm to 6 dBm in steps of 3 dBm, and the gain was measured for each input power level. The amplifier tends to saturate at high input power levels, thereby causing the gain to drop. Figure 312 below plots the measured gain at different input power levels.

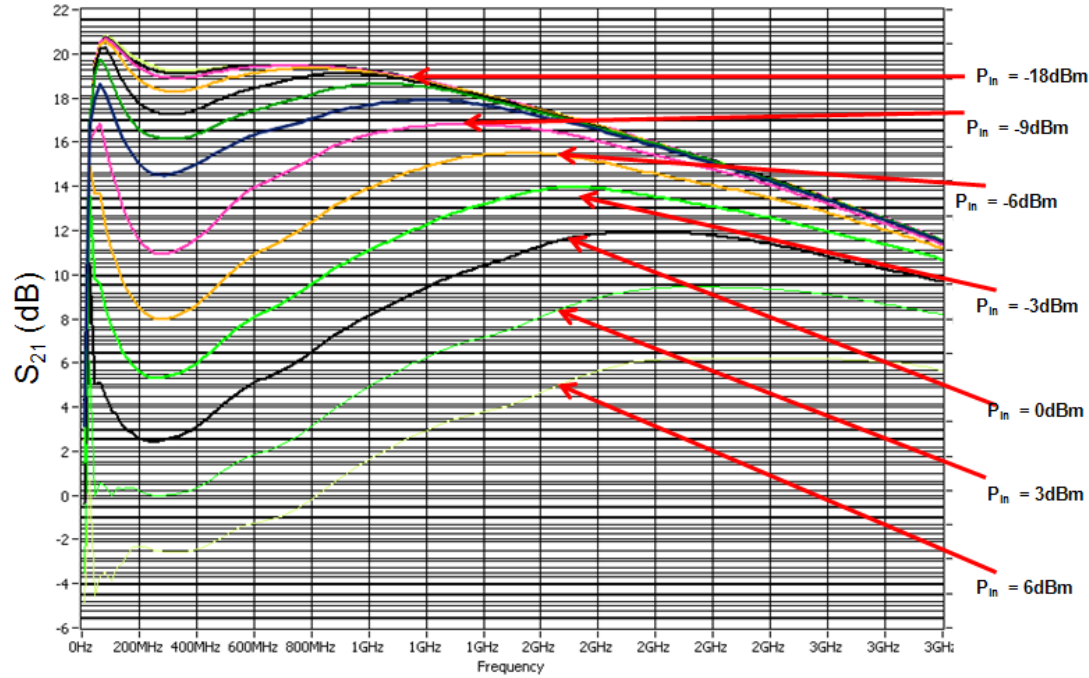


Figure 312: Measured gain at different input power levels at 300 K. The input power was stepped by 3 dBm from -24 dBm to +6 dBm. As the input power increased, the amplifier tends to become nonlinear, thereby causing the gain to decrease. The topmost curve corresponds to an input power of -24 dBm. The bottommost curve corresponds to an input power of +6 dBm.

5.4.3 Noise Figure measurements: Before Loss Compensation

The Y-Factor [7] measurement technique was used for measuring the noise figure of the LNA. The noise source was first calibrated using a 50 Ω through line. Then the noise source was connected to the LNA input, and the LNA output was connected to the noise figure meter, or spectrum analyzer. Then the noise level at the output of the LNA was initially measured with the noise source turned off, and then again with the noise source turned on.

Assuming that the temperature of the noise source when turned off is T_c , and its temperature when turned on is T_h , the output noise from the noise source, which is represented by the excess noise ratio (ENR), is defined as

$$ENR_{dB} = 10 \log \left(\frac{T_h - T_c}{T_0} \right), \quad (7)$$

where T_0 is the ambient temperature, which is assumed to be 290 K. If the output noise power from the LNA with the noise source turned on is N_1 , and that when it is turned off is N_2 , then the ratio of these noise powers is the Y-factor, which is defined as:

$$Y = \left(\frac{N_2}{N_1} \right) \quad (8)$$

Then the input referred noise level (N_i) of the LNA is:

$$N_i = kT_0B \left(\frac{ENR}{Y-1} - 1 \right) \quad (9)$$

Where B is the bandwidth, ENR is the excess noise factor as defined in Equation 7 and Y is the noise factor as defined in Equation 8. From the input referred noise, the noise figure can be calculated if the gain is known. The spectrum analyzer measures the gain of the LNA, allowing the noise figure to be calculated.

The noise figure was measured using the Agilent MXA 9020A Signal Analyzer and Agilent N4002A noise source. The noise source was first calibrated using a through-line on the impedance substrate. This was followed by insertion of the LNA between the noise source and the MXA signal analyzer. The noise figure was measured at the different biasing conditions listed in Table 10. The measured noise figure was found to be significantly higher than the simulated one. However, since other measured small-signal parameters seem to be in accordance with the corresponding simulated values, the high-noise figure can be attributed to the ENR of the noise source. The ENR of the noise source N4002A is 15 dB. Based on the information in reference [8], a low ENR noise source such as N4000A is recommended when measuring ultralow-noise figures.

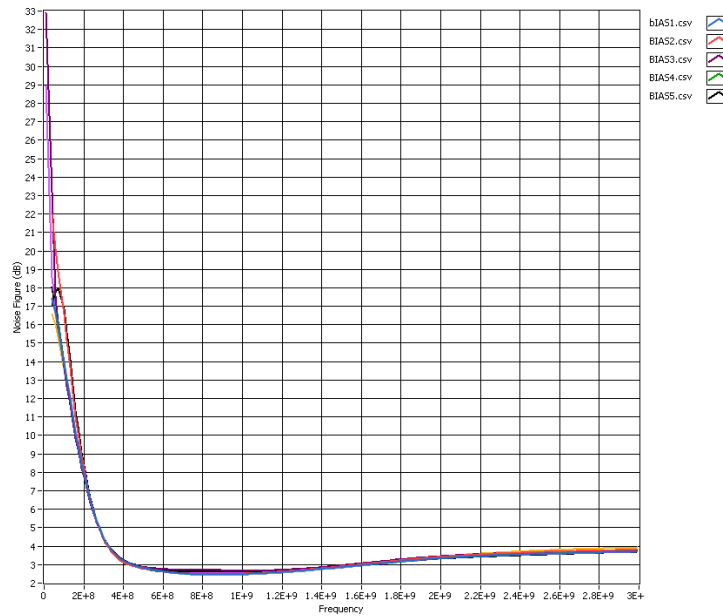


Figure 323: Measured noise figure (dB) at 300 K under different biasing conditions.

5.5 Measurements on MMIC LNA: Low Temperature

Cryogenic small-signal S-parameter and noise-figure measurements were performed after cooling the LNA board down to 77 K. These measurements were done using the JANIS ST500 cryostat. Table 11 below lists the DC biasing conditions at which the LNA was tested cryogenically. Figure 334 and Figure 345 plot the measured input and output return losses, respectively, performed at 77 K under various biasing conditions. Figure 356 plots the measured small-signal gain at 77K under various bias conditions.

Table 11: DC Bias conditions for cryogenic testing of the LNA.

Biasing Point	V _{G1} (V)	V _{D1} (V)	I _{D1} (mA)	V _{G2} (V)	V _{G3} (V)	V _{D2} (V)	I _{D2} (mA)
1	-0.5	3	18	0.8	-0.58	3	6
2	-0.45	3	26	0.8	-0.5	3	9
3	-0.45	3	26	0.8	-0.48	3	10
4	-0.43	3	29	0.8	-0.43	3	13
5	-0.43	3	29	0.9	-0.43	3	13

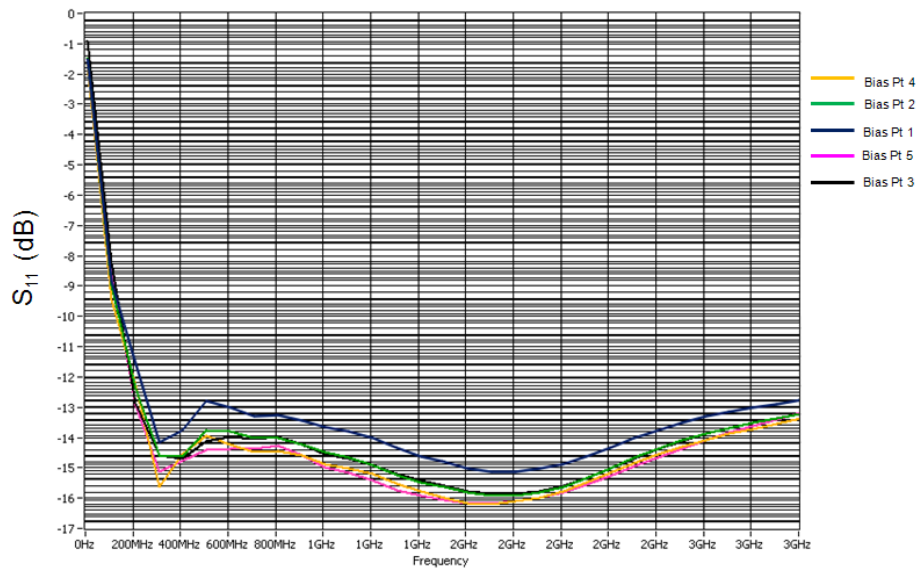


Figure 334: Measured input return loss (S_{11} in dB) at 77 K under different bias conditions.

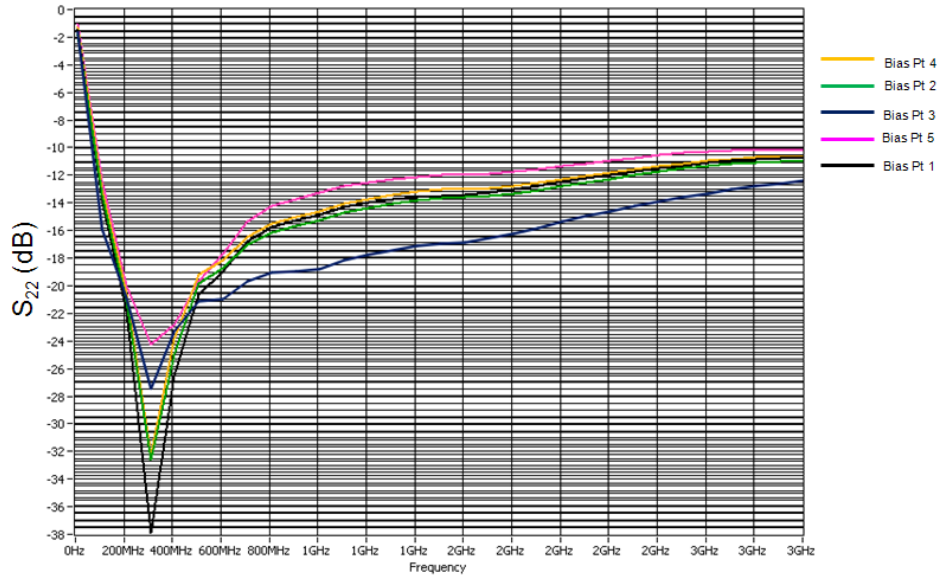


Figure 345: Measured output return loss (S_{22} in dB) at 77 K under different bias conditions.

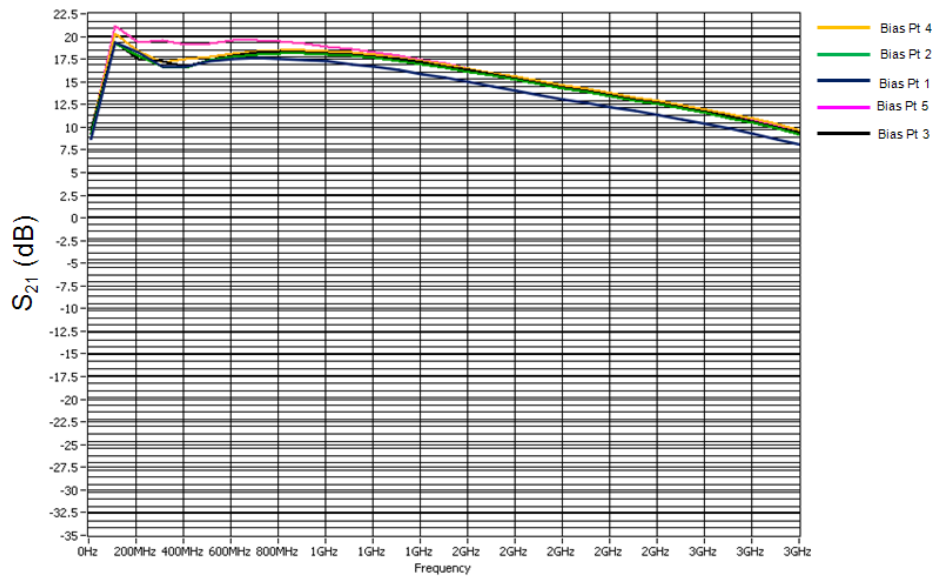


Figure 356: Measured small signal gain (S_{21} in dB) at 77 K under different bias conditions.

Keeping the gate and drain voltages fixed, small-signal gain and return loss measurements were performed on the LNA at different temperatures ranging from, 300K down to 77K in 40K steps. It was observed that the drain currents decreased as the LNA is cooled down. However, no significant degradation of the return loss was noticed. Besides, the gain variation during this entire temperature range was less than 2dB across the band of interest. Figure 367 and Figure 378 plot the variation of input return loss and gain of the LNA at $V_{G1} = -0.5V$, $V_{D1} = 3V$, $V_{G2} = -0.58V$, $V_{D2} = 3V$.

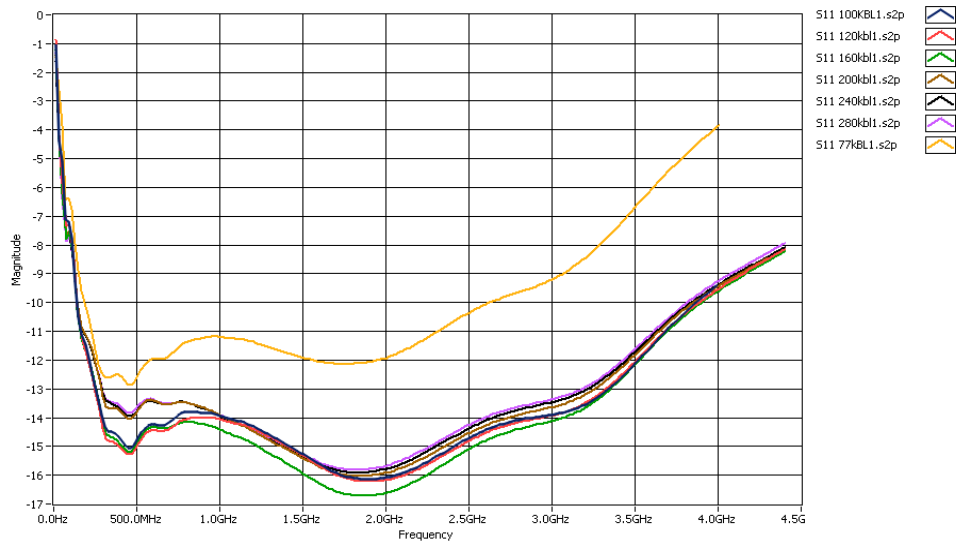


Figure 367: Variation of the measured input return loss (S11, dB) vs. temperature

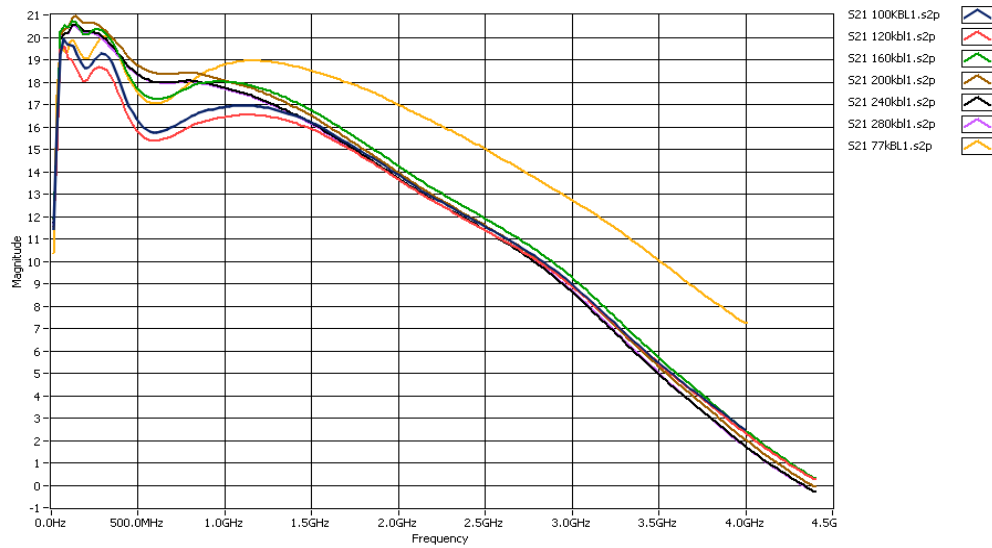


Figure 378: Variation of the measured gain (S21, dB) vs. temperature

The noise figure was also measured at 77 K when the DC current through the input stage was 26 mA and the DC current through the auxiliary amplifier stage was 10 mA. Figure 49 below compares the noise figure at 77 K with the noise figure at 300 K under the same DC bias condition.

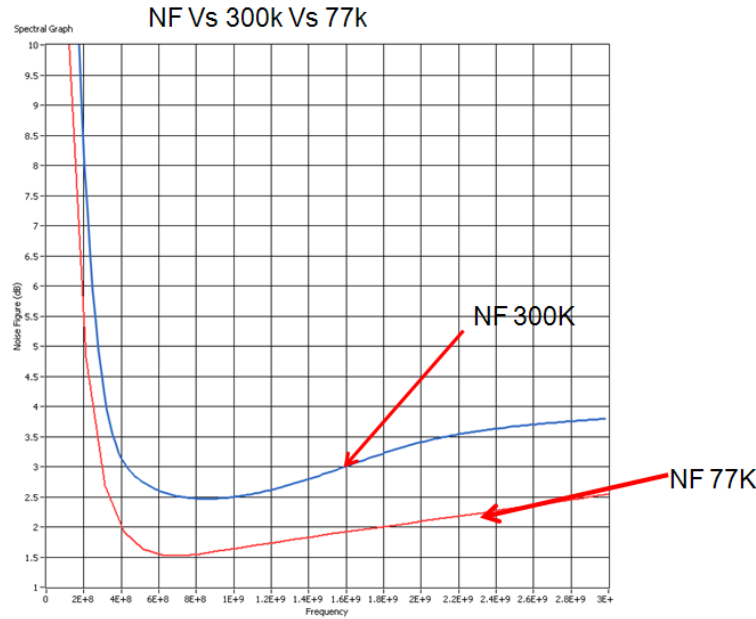


Figure 49: Measured noise figure in dB at 300 K (blue) and 77 K (red) for the LNA (measured on the PC board).

The measured noise figure dropped by approximately 1 dB when cooled from 300 K to 77 K.

Table 12: Measured vs. simulated parameters for the LNA.

Parameter	Simulated (300 K)	Measured ¹ (300 K)	Measured ² (77 K)
S ₁₁ (dB) (0.1 GHz-1.1 GHz)	<-11	<-10	<-12
S ₂₂ (dB) (0.1 GHz-1.1 GHz)	<-10	<-10	<-12
S ₂₁ (dB) (0.1 GHz-1.1 GHz)	18	19	19
Bandwidth (GHz) (1 dB gain flatness)	100 MHz-1.7 GHz	100 MHz-1.4 GHz	100 MHz-1.3 GHz
DC Current (mA)	37	35	35

¹I_{D1}= 26mA, I_{D2}= 12mA

²I_{D1} = 25mA, I_{D2}= 10mA

5.6: Noise Figure Measurements: Loss Compensation

The insertion losses of the probe tips and cabling losses were not properly compensated during the noise figure measurements. This section discusses in detail various techniques that have been employed to calibrate the cabling losses. To measure the noise figure, the LNA was first placed inside a cryogenic probe station. The noise of the LNA bare die was probed using G-S-G probe tips. At the input end, there is a 24-inch semirigid cable within the probe station that connects the

probe tip to the noise source. At the output end, there is another 24-inch cable within the probe station which in turn is connected to the spectrum analyzer using a 36-inch flexible cable. Figure 380 below is a block diagram of the noise-figure measurement setup. A step-by-step approach to noise figure measurement with cabling losses follows.

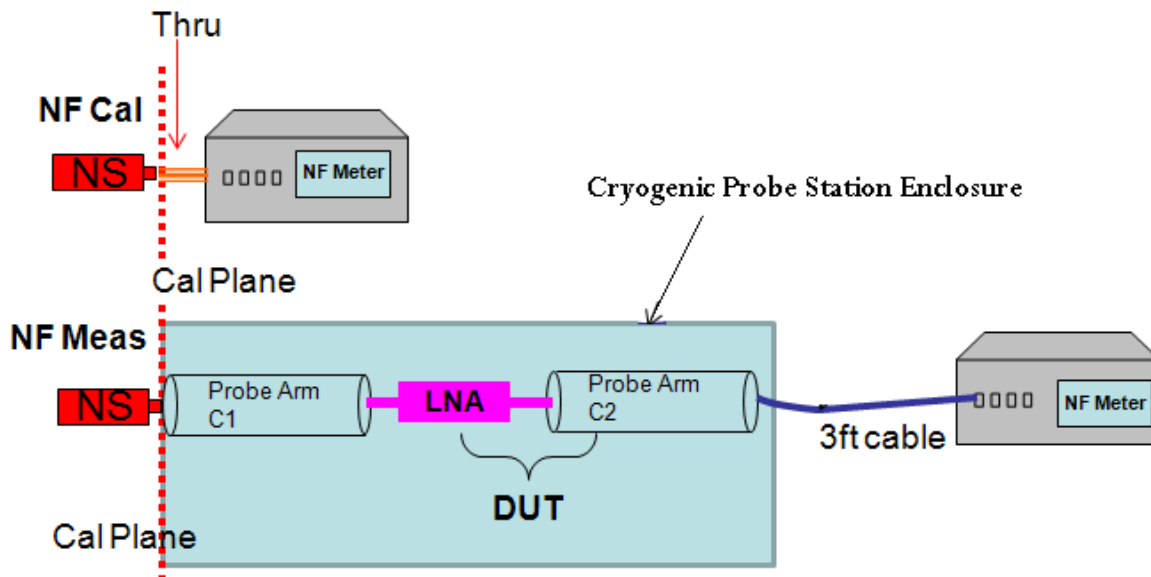


Figure 380: Block diagram of cryogenic noise-figure measurement of the LNA.

The probe-arm cable used to connect the output of the noise source to the LNA input does contribute to the overall noise figure since it is at the input of the amplifier, yet is not part of the calibration loop. Therefore, the noise figure of this cable must be measured first and its noise subtracted out later. After this initial calibration step, the DUT (device under test) is the cable. Figure 39 is a block diagram of this configuration and Figure 51 is a plot of the measured noise performance of this cable. The cable noise figure at 1 GHz was found to be ~ 0.6 dB, which is significant compared to the LNA noise figure.

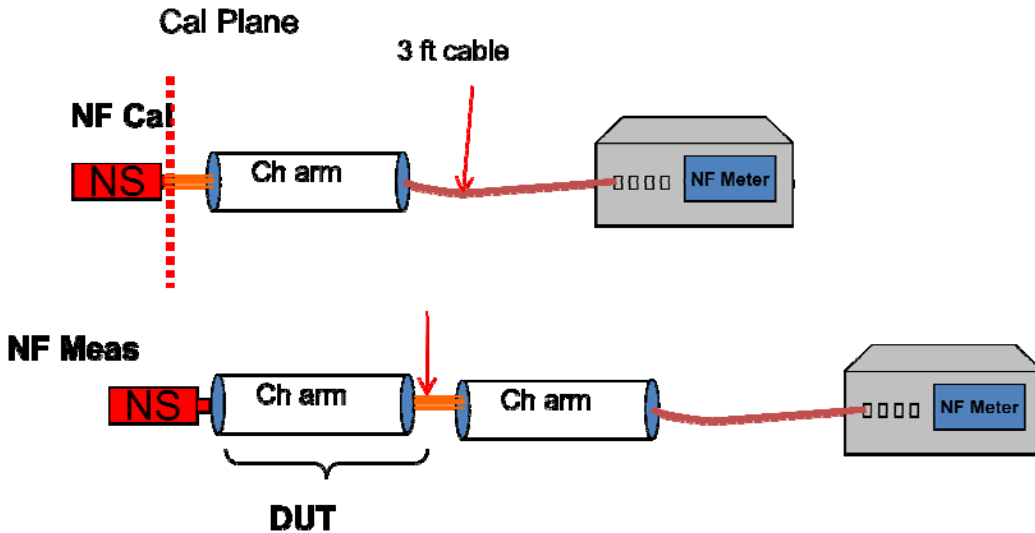


Figure 391: Setup for measuring the cable noise figure for later removal from the LNA noise figure measurements.

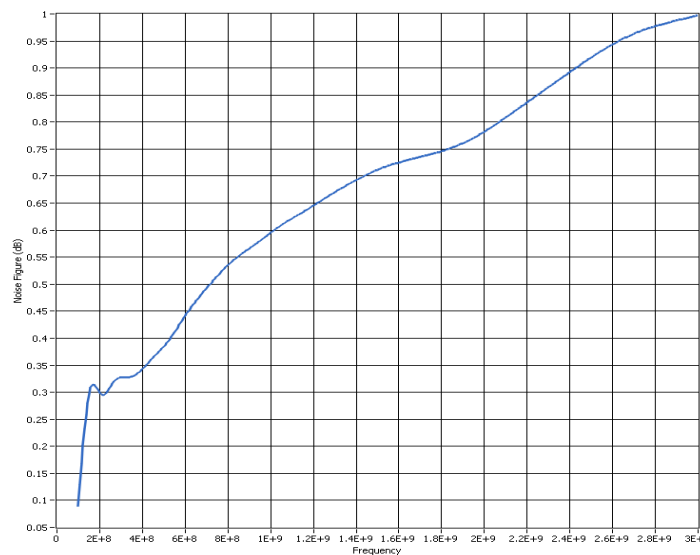


Figure 402: Input cable noise figure at 300 K, measured with the setup shown in Figure 39.

After measuring the noise figure of the input cable, the LNA was placed inside the probe station and the noise figure was measured. This time, calibration of the noise source was performed after including the input probe arm in the calibration loop. However, none of the cabling after the LNA was compensated. Figure 413 below shows an equivalent setup and Figure 424 shows the measured noise figure of this combination.

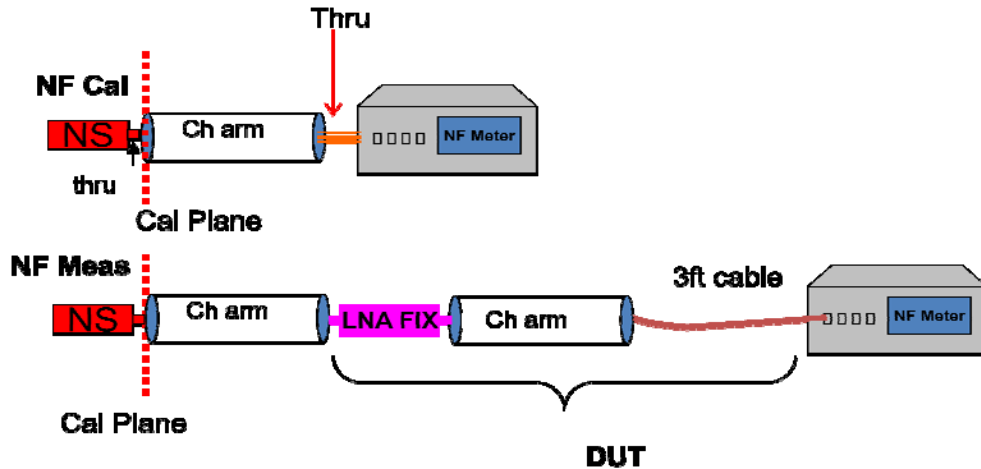


Figure 413: Setup for measuring the noise figure of the LNA and output cable combination.

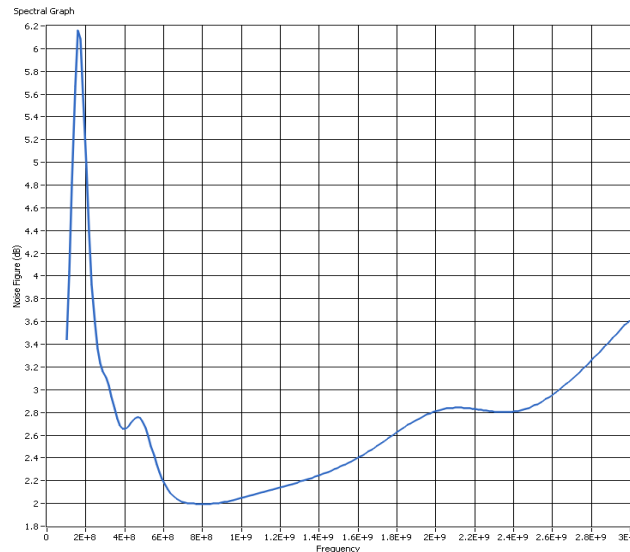


Figure 424: Measured noise figure for the LNA and output cable setup shown in Figure 53.

It can be observed that the noise figure is higher than that in the case in which the LNA output is directly connected to the analyzer. Therefore, it can be inferred that the losses arising from the cabling between the output of the LNA and the probe station were not properly compensated during the calibration.

Based on these results, it can be inferred that the cabling losses are too high to be ignored and have not been properly compensated in the above measurements. An accurate noise figure measurement depends on the selection of the right reference plane. It is desirable to place the DUT as close as possible to the noise source. Any passive network losses, such as cables and adapters at the input and output, must be eliminated to ensure accurate measurements. However, since this is not possible in a cryogenic measurement system, the different cabling losses have to be accounted for separately.

5.6.1: Estimation of the Noise Figure of a Passive Network

To estimate the noise figure of the RF before the LNA input, the cable must be modeled using lumped elements. For analysis purposes, the cable can be assumed to be equivalent to a lossy passive network with an attenuation A_c , as shown in Figure 435.

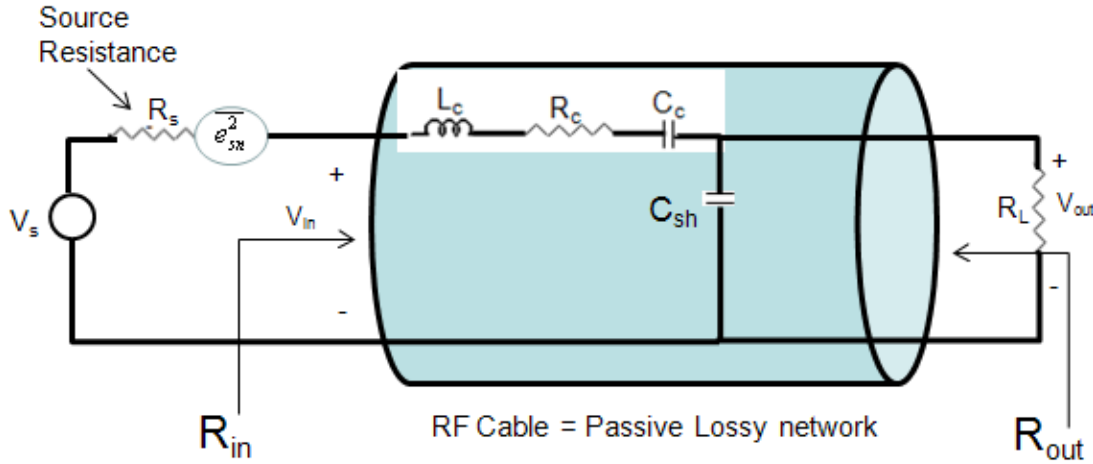


Figure 435: Schematic of the RF cable as a passive network.

The noise from the RF cable (passive network) was modeled in terms of its equivalent noise generator R_{eq} and attenuation A_c . Figure 446 below shows the circuit model with R_{out} representing all the noise from the cable.

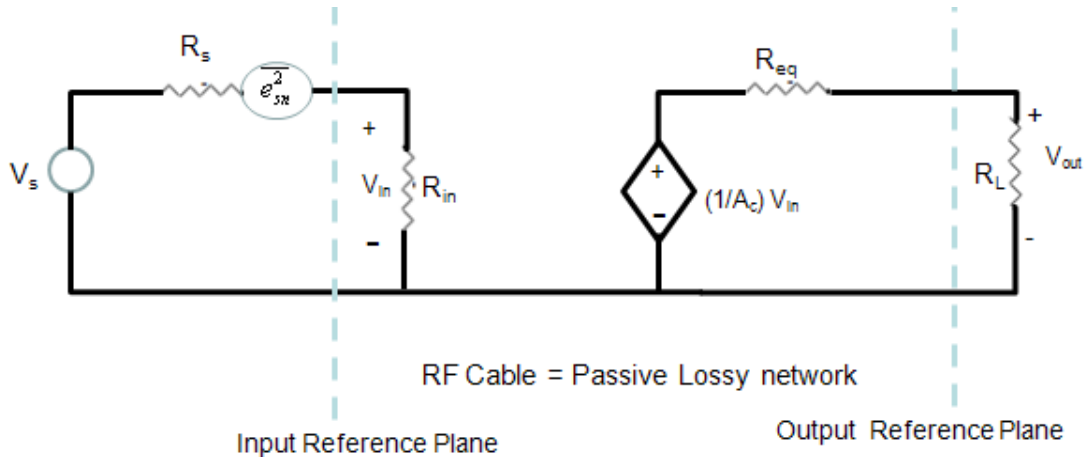


Figure 446: Equivalent circuit for determination of the noise figure of the cable.

The total noise at the output due to noise contributions from the noise source and the cable losses is given by

$$\overline{v_{nout_tot}^2} = 4kTR_{eq} \left(\frac{R_L}{R_L + R_{eq}} \right)^2. \quad (10)$$

The attenuation of the network (from source to load) is given by

$$A_{tot} = \frac{R_s}{R_{eq}} \left(\frac{R_{in}}{R_s + R_{in}} \right)^2 \left(\frac{1}{A_c} \right)^2 \quad (11)$$

The noise at the output due to the source resistance alone is given by

$$\overline{v_{nout_s}^2} = 4kTR_s \left(\frac{R_{in}}{R_s + R_{in}} \right)^2 \left(\frac{1}{A_c^2} \right) \left(\frac{R_L}{R_L + R_{eq}} \right)^2 \quad (12)$$

From Equations 11 and 12, the noise factor will be equal to the total attenuation. Therefore, the noise figure of the cable is equal to its loss. Since the cable appears before the DUT, it is critical to accurately determine the cable losses and compensate for these losses while measuring the DUT noise figure.

We acquired the Agilent 85052D Calibration Kit in order to measure the insertion loss of the cables before and after the DUT (LNA). Figure 457 below shows the measured insertion loss of the RF cable at the input of the LNA (probe arm cable C1 as shown in Figure 50). Figure 458 plots the measured insertion loss of the RF cable (50 Ω characteristic impedance) at the output of the LNA (probe arm cable C2 as shown in Figure 53 and the 36 inch cable with 50 Ω characteristic impedance connecting the probe arm to the spectrum analyzer).

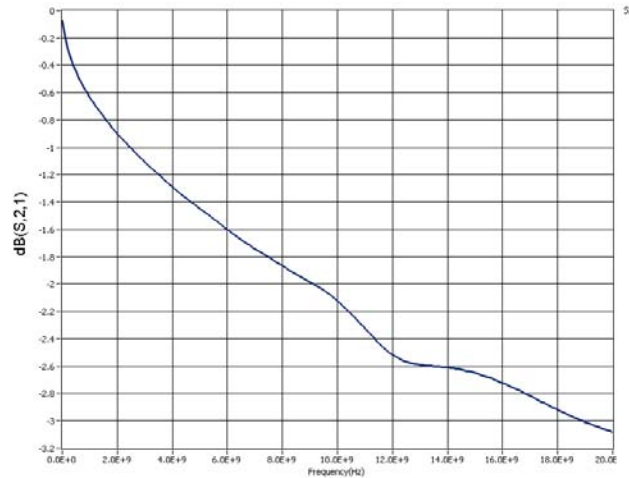


Figure 457: Measured loss of the RF cable before the LNA (probe arm C1).



Figure 468: Measured loss of the RF cable after the LNA (probe arm C2 plus 36 inch cable).

In addition to the cabling losses, the insertion loss of the probe tips was also considered for performing die level measurements. Figure 59 plots the probe-tip insertion losses.

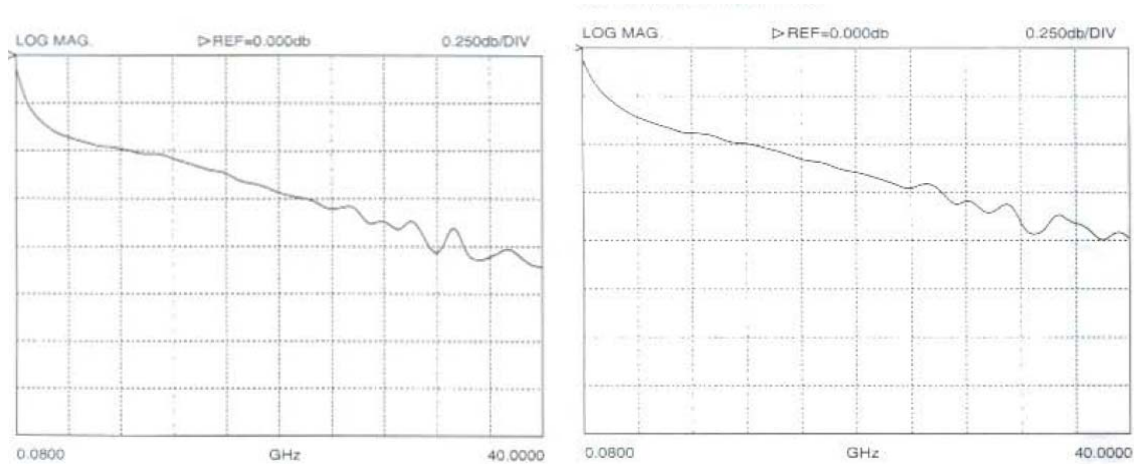


Figure 59: The insertion loss of the probe tip at the LNA input (left) and the insertion loss of the probe tip at the LNA output (right).

5.6.2 Noise-figure Measurement with Cable-loss Compensation

The MXA spectrum analyzer was programmed to perform loss compensation for the noise-figure measurement. Die-level noise-figure measurements were performed on the MMIC. The circuit board assembly that houses the MMIC and other passives was placed inside the cryogenic probe station and the noise figure was measured at temperatures ranging from 300 K (ambient) down to 120 K. Figure 470 plots the measured noise figure of the LNA at different temperatures. With the correct compensation of the passive losses due to the cable and probe station, the noise figure has dropped as expected.

Maintaining the same DC biasing voltage, the LNA chip was cooled down. Figure 481 plots the variation of gain vs. temperature. The loss compensation discussed above was employed for

taking into account the losses from the RF cables and probe tips in the measurement path. At 120K, an ultralow noise figure of 0.3 dB was obtained.

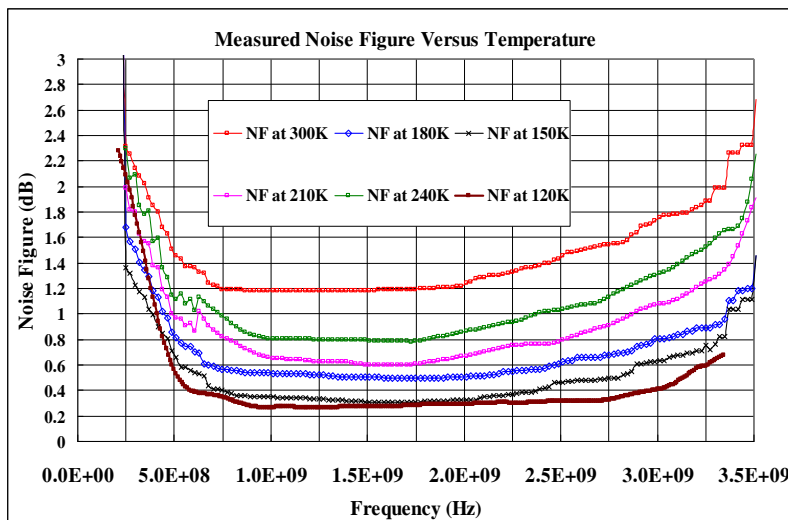


Figure 470: LNA noise figure vs. temperature

It is important to mention that during the design and optimization stages only a room-temperature device model was available to us. However, as expected, low-temperature measurements show a noise performance improvement of ~ 0.9 dB across the band when the LNA is cooled down to 120K. Also as expected, the gain slightly changed as the temperature went down, this variation (~ 1.5 dB) was not detrimental to the LNA behavior. Similar observations apply to the input and output return losses. Figure 481 below plots the variation of the gain with temperature.

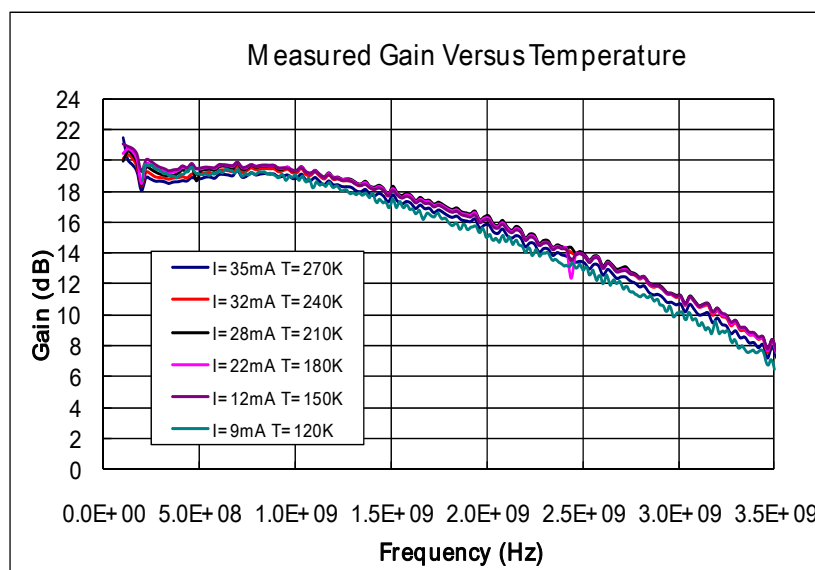


Figure 481: Measured gain figures of the LNA (die level) at various temperatures for the setup shown in Figure 53.

It is interesting to note that as the LNA is cooled down, the DC power consumption also drops. This is due to the fact that the FET DC current drops with temperature. Our LNA has also demonstrated lower power consumption. This is an especially useful feature because it shows that the load on the cooling system can be reduced. Table 13 below summarizes the low temperature characteristics of this LNA.

Table 13: Summary of Low Temperature Characteristics of the LNA

Temperature (K)	Freq. (GHz)	NF(dB)/T(K)	DC Power
270	0.7-2.5	<1.5/120	102mW
240	0.7-2.5	<0.8/59	93mW
180	0.7-2.5	<0.5/35	66mW
150	0.7-2.5	<0.3/21	36mW
120	0.7-2.5	<0.3/21	32mW

At 300K after loss compensation the noise figure is 1.2 dB, which is close to the case in which the test fixture output is directly connected to the analyzer input (Figure 1), suggesting a correct compensation procedure. As the temperature decreases, a monotonic drop in the noise figure was observed. At 150 K, the noise figure was less than 0.5 dB. These exciting results will be published in the upcoming IEEE MWCL 2012 journal.

5.7 Device DC Characteristics vs. Temperature

Test structures consisting of active and passive devices based on TriQuint's 0.15 μ m pHEMT process were fabricated during the last foundry run. The pHEMT devices are of the same dimensions as those used in the amplifier designs. The test structure bare die is shown in Figure 492.

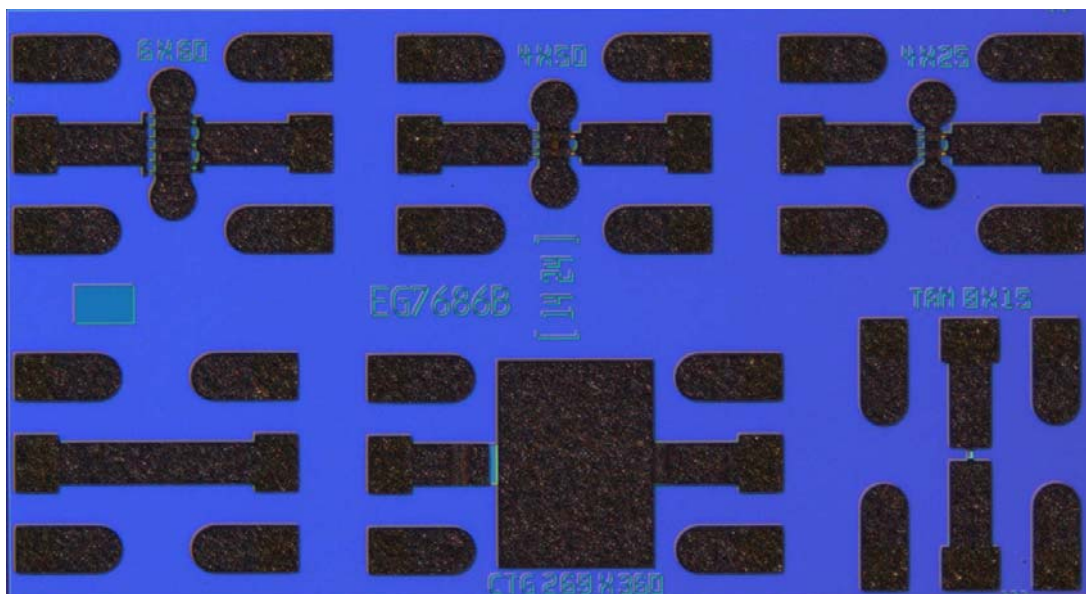


Figure 492: Bare die of the test devices

The test structure has pHEMT devices of the same dimensions as those used in the LNA, and has a 5pF capacitor and a TaN resistor. The purpose of the test structure is to develop a temperature dependent small-signal model for the pHEMT devices. It is important to note that the FET models provided by the foundry are not temperature dependent. Table 14 shows the pHEMT devices used in the LNA circuit and their nominal DC biasing conditions.

Table 14: Locations of the FETs in the LNA

Device Size (μm)	Location on the LNA	V_{DS} (V)	I_{DS} (mA)	V_{GS} (V)
360	Input Stage	3	27	-0.6
200	Auxiliary Amplifier(top)	1.5	45	-0.7
100	Auxiliary Amplifier(bottom)	3.14	16	-0.65

I-V characterization of these FET test structures was performed at various temperatures using the Keithley 4200 Parameter Analyzer. The test-structure die was mounted on a test fixture, which in turn was placed inside a JANIS ST500 cryogenic chamber. Figure 503 gives a block diagram of the DC characterization setup for the test structures.

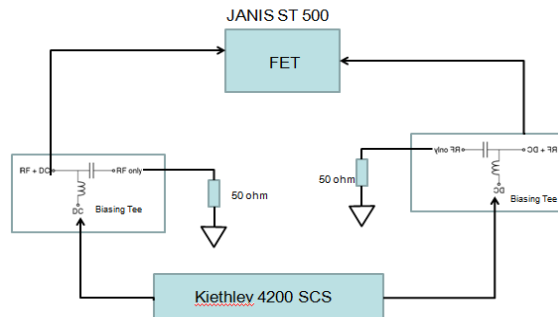


Figure 503: Setup for DC Characterization of the FETs

While performing the parametric analysis, it is essential to connect the devices properly in order to prevent untoward oscillations. Proper isolation of the RF and DC signals was required. For this purpose, a biasing tee was used for connecting the SMU (Source Measure Unit) cable of the biasing tee to the probe arm of the probe station. The RF terminal of the biasing tee was terminated with 50 Ω impedances. In this way, the RF was properly terminated, allowing only DC to pass through the devices. Our initial I-V measurements without the biasing tee showed a decrease in the drain current with increase in gate voltage, which is contrary to the behavior of the HEMT device.

The drain current (I_{DS}) of each device was measured by sweeping the drain voltage (V_{DS}) and stepping the gate voltage (V_{GS}). V_{GS} was stepped from -1 V to 0 V and V_{DS} was swept from 0 V to 3 V. The DC transconductance (g_m) was determined from these measurements. Ambient temperature measurements were performed first. All of the devices were pinched off at a V_{GS} of -1 V at a temperature of 300K. This was followed by temperature dependent measurements (77K-ambient). Figure 514 below shows the I-V characteristic for the 100 μ m pHEMT at 300K and 77K. The gate voltage (V_{GS}) was swept from -1 V to 0 V in 0.2 V increments).

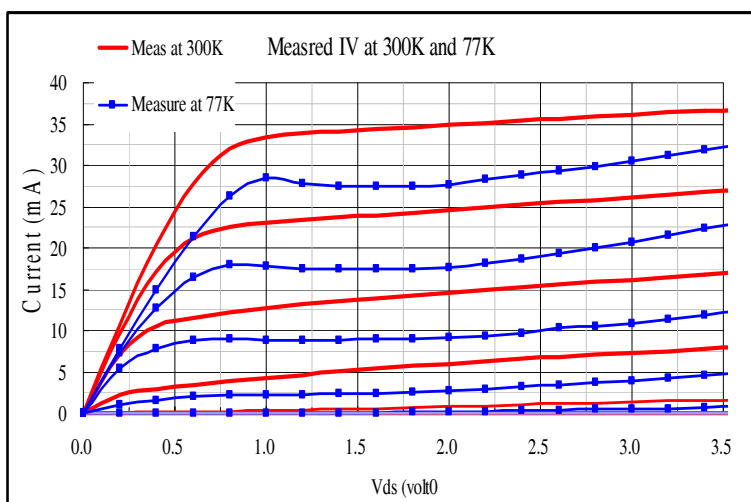


Figure 514: I_{DS} (A) vs. V_{DS} (V) characteristics of the 100 μ m pHEMT device at 300K and 77K

Figure 51 below shows the I-V characteristics of the 200 μm pHEMT at 300K, 110K and 77K. The gate voltage (V_{GS}) was swept from -1 V to 0 V in 0.2 V increments). Figure 52 shows the I-V characteristic of the 360 μm pHEMT devices at $V_{GS} = -0.6\text{V}$, which is the nominal DC bias condition at ambient temperature.

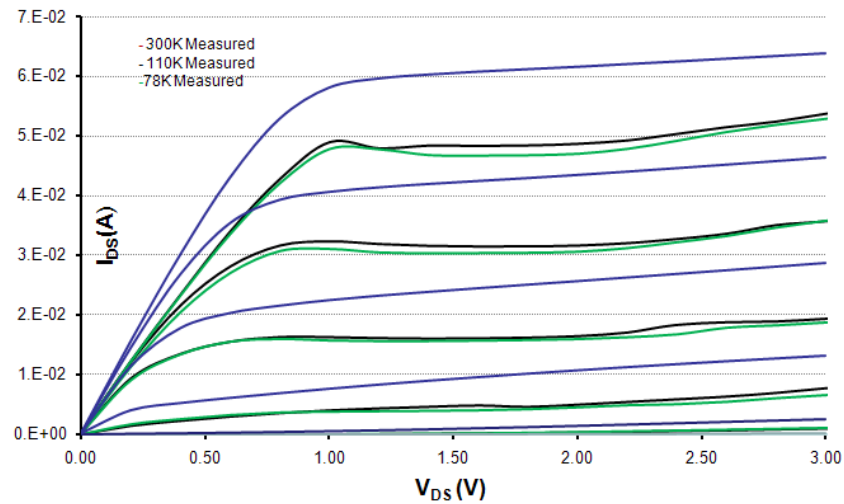


Figure 525: $I_{DS}(A)$ vs. $V_{DS}(V)$ characteristics of 200 μm pHEMT device at 300K, 110K, 77K

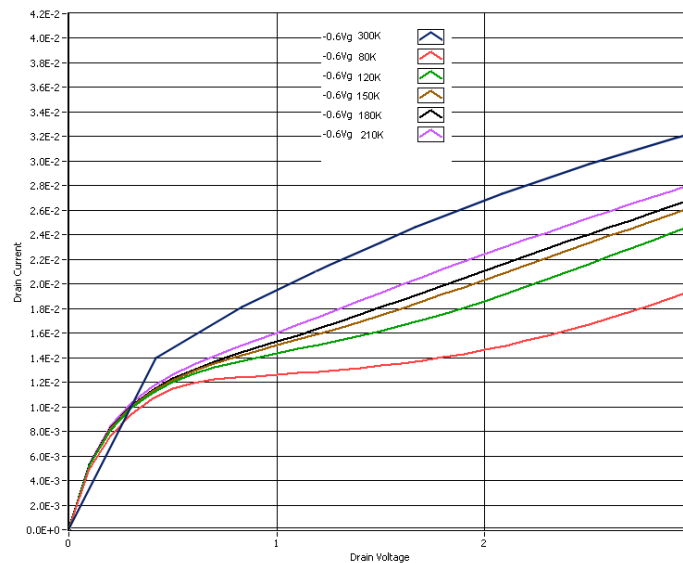


Figure 536: $I_{DS}(A)$ vs. $V_{DS}(V)$ characteristics of 360 μm PHEMT device from 300K to 80K for $V_{GS} = -0.6\text{V}$.

In addition to the pHEMTs, the test structure also contains a 100 Ω resistor and a capacitor. The TriQuint 3MI process provides TaN resistors that have a very low temperature coefficient. The I-V characteristics of the resistor were also measured at different temperatures. Figure 547 below plots the I-V characteristics of this resistor at three temperatures. The variation in resistance from 300 K to 110 K was less than 10%. The measured resistance at 0 V bias was 117 Ω at 300K and 128 Ω at 110 K.

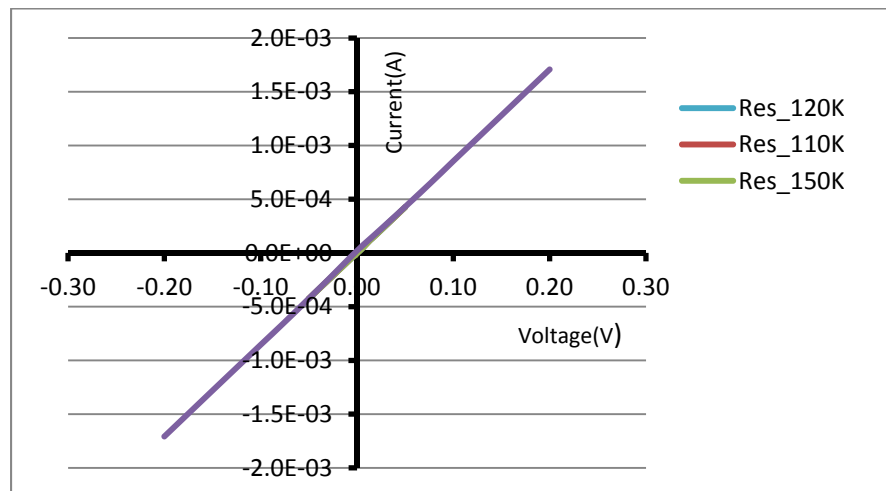


Figure 547: Variation of Resistance with Temperature

5.8 Cryogenic Device Measurements: Device Small-signal Characteristics

Small-signal S-parameter measurements were performed on the pHEMT devices under different biasing conditions. The purpose of these measurements is to enable the development of a temperature-dependent small-signal model. The measured S-parameters at 300 K were close to the simulated results. For the simulation, transmission lines and pads were added at the input and output of the devices in order to mimic the test-structure devices. Specifically, 150 μm pitch G-S-G pads were added at the drain and the gate terminals, and 100 μm transmission lines and tapers were added at the drain and gate-feed networks.

Figures 68-70 show the measured and simulated S-parameters of the different pHEMT devices (360, 200 and 100 μm devices) at 300 K. The measured values match the simulated values quite well in all cases.

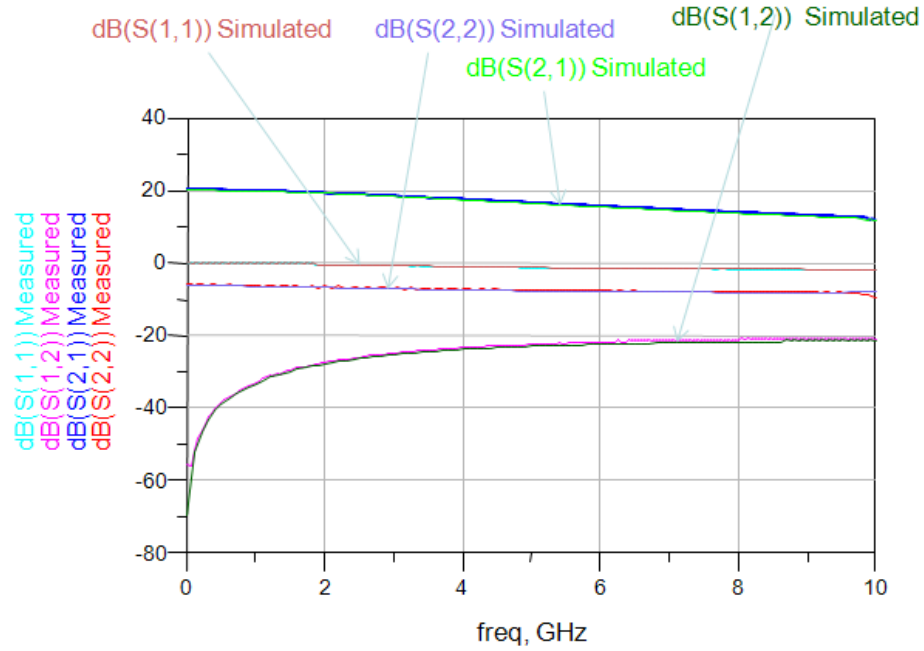


Figure 55: Measured and simulated S-parameters vs. frequency for the 360 μm pHEMT at 300 K ($V_{DS} = 3$ V, $I_{DS} = 75$ mA/mm).

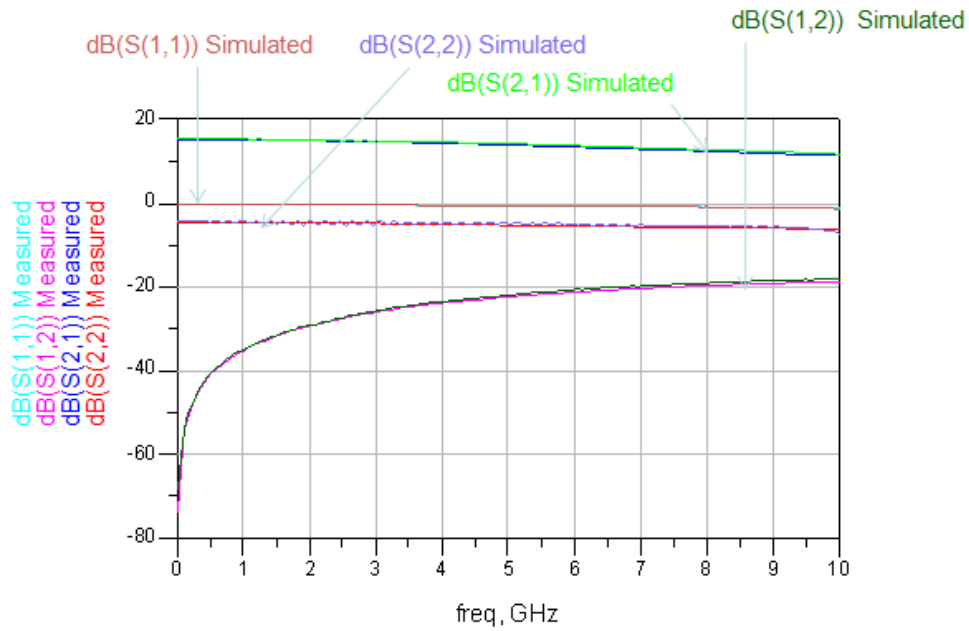


Figure 69: Measured and simulated S-parameters vs. frequency for the 200 μm pHEMT at 300 K ($V_{DS} = 1.5$ V, $I_{DS} = 50$ mA/mm).

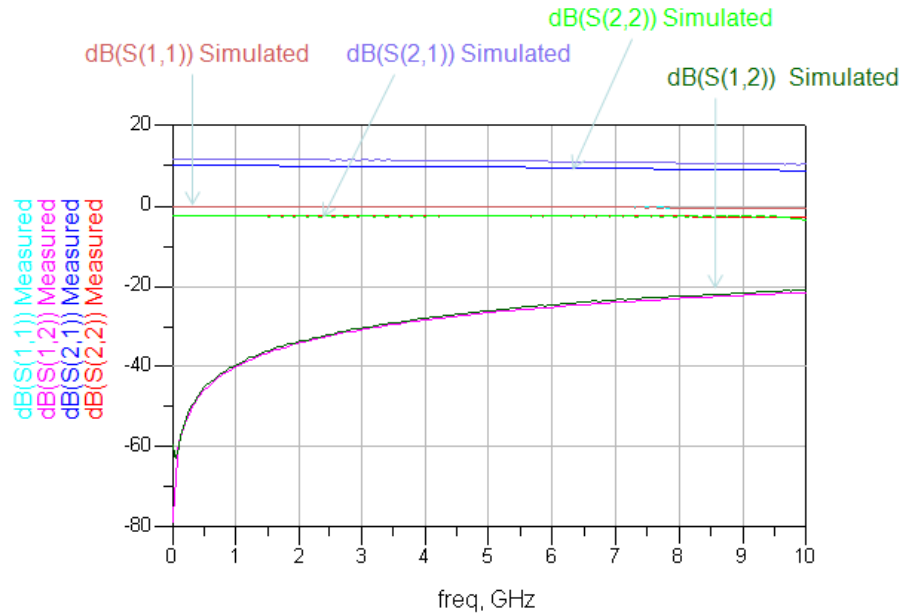


Figure 560: Measured and simulated S-parameters vs. frequency for the 100 μm pHEMT at 300 K ($V_{\text{DS}}=1.5\text{V}$, $I_{\text{DS}}=100\text{mA/mm}$).

5.8.1 Bias dependence of device small-signal gain

Small-signal S-parameters for the FETs were measured at different biasing conditions. Keeping the drain voltage fixed, the gate voltage was adjusted to increase the DC current. The S-parameters were measured at different DC currents. As expected, the device gain increased with increase in DC current. Figure 571 shows the variation of device gain with DC current for the input device.

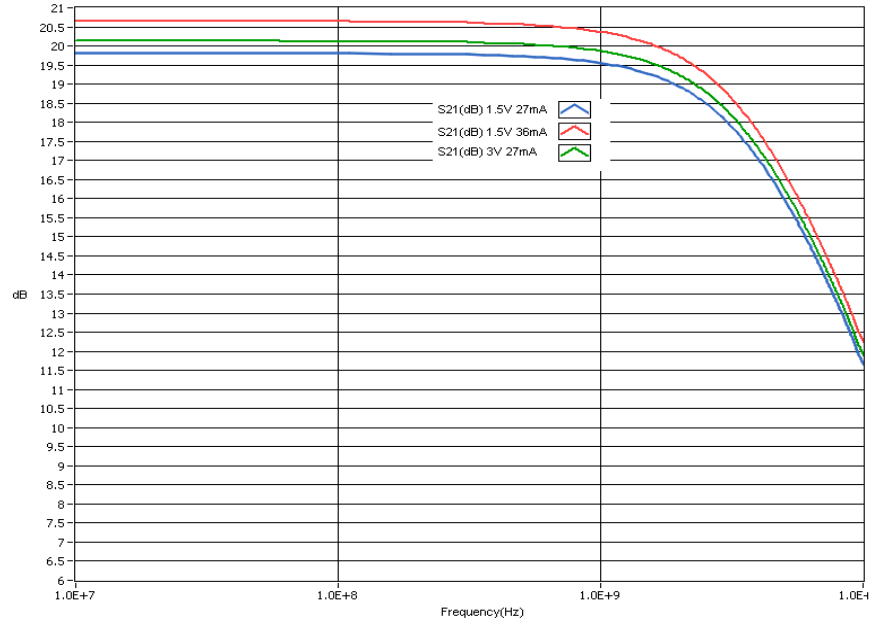


Figure 571: Measured S_{21} (dB) vs. frequency at various bias conditions for the 360 μm pHEMT at 300 K. The frequency is on a log scale.

5.8.2 Temperature dependence of device small-signal gain

As discussed before, small-signal measurements on the FETs were performed at different temperatures. Keeping the drain and gate voltages fixed at their nominal values at 300K, the test structure was cooled down to 80K and the drain currents were allowed to drop. The S-parameters were measured at different temperatures. As expected, the device gain increased with increasing DC current. Figures 72-74 show the variation of device gain with temperature for each of the devices in the LNA. It was observed that the larger the FET size, the more sensitive the gain is to temperature variations.

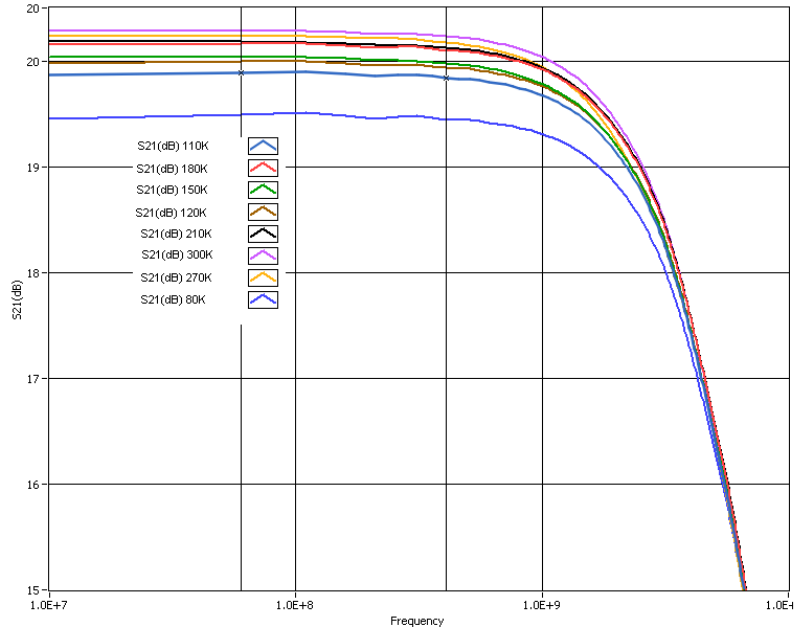


Figure 582: Measured S21 (dB) vs. frequency at various temperatures for the 360 μm pHEMT at 300 K. The frequency is on a log scale.

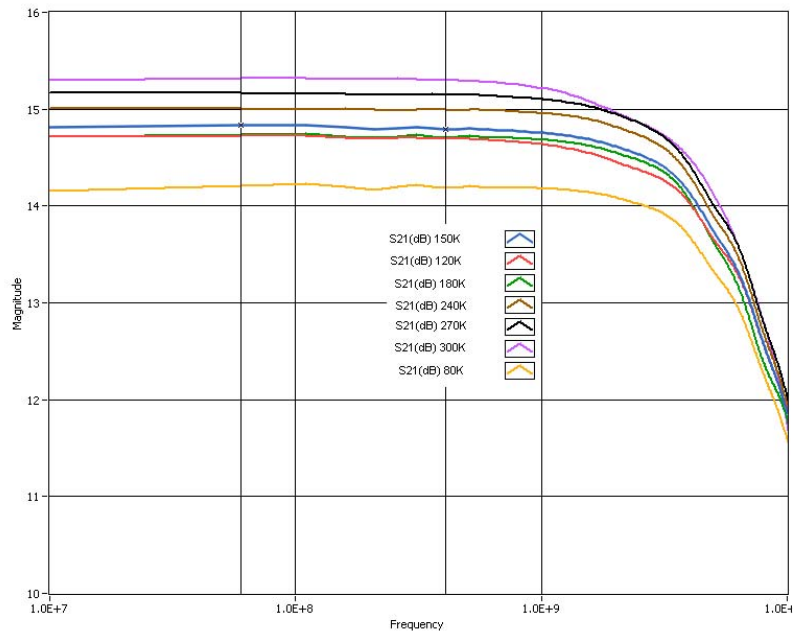


Figure 593: Measured S21 (dB) vs. frequency at various temperatures for the 200 μm pHEMT at 300 K. The frequency is on a log scale.

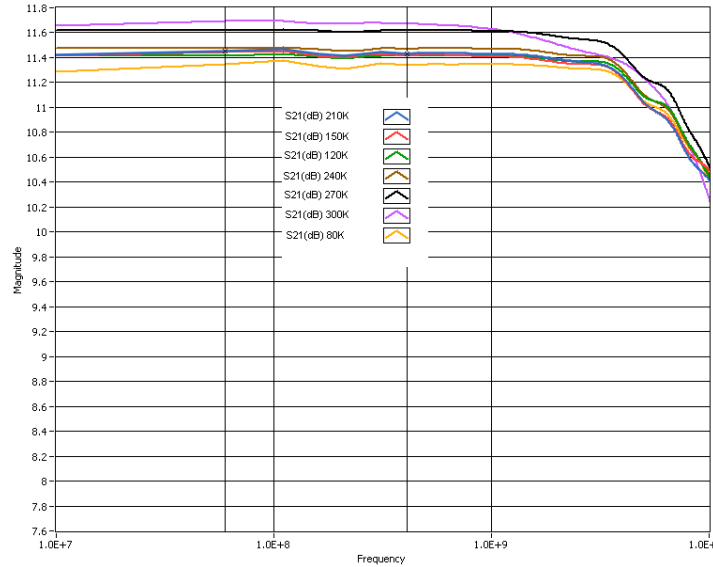


Figure 604: Measured S21(dB) versus frequency at various temperatures for 100 μm pHEMT at 300 K. The frequency is on a log scale.

Besides small-signal measurements, large signal measurements were also performed on the LNA.

6.0 Prototyping

For prototyping the amplifier, we used open-cavity circuit-packaging techniques in which the amplifier input and output pads (in addition to the DC pads) were wirebonded to a ceramic package. The amplifier can have SMA input and output pins. These pins were then wirebonded to 50 Ω microstrip lines, which in turn were bonded to the LNA RFIN and RFOUT pads.

The package is essentially a test fixture consisting of 50 Ω coplanar lines with SMA terminations to provide RF input and RF output to the LNA. The LNA MMIC has G-S-G pads for RFIN and RFOUT that are wirebonded to the coplanar line. The DC bias is provided through leads. The test fixture also has provisions for mounting other discrete components such as the bypass capacitors and inductors. Figure 615 below shows the layout of the test fixture, and Figure 626 is a picture of the actual test fixture.

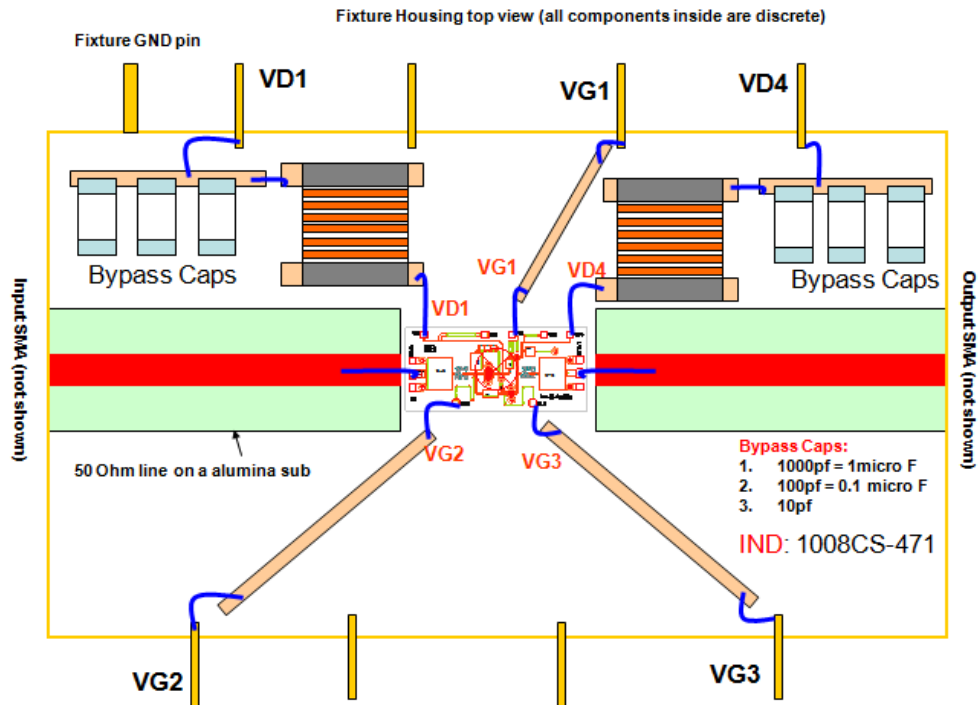


Figure 615: LNA package layout

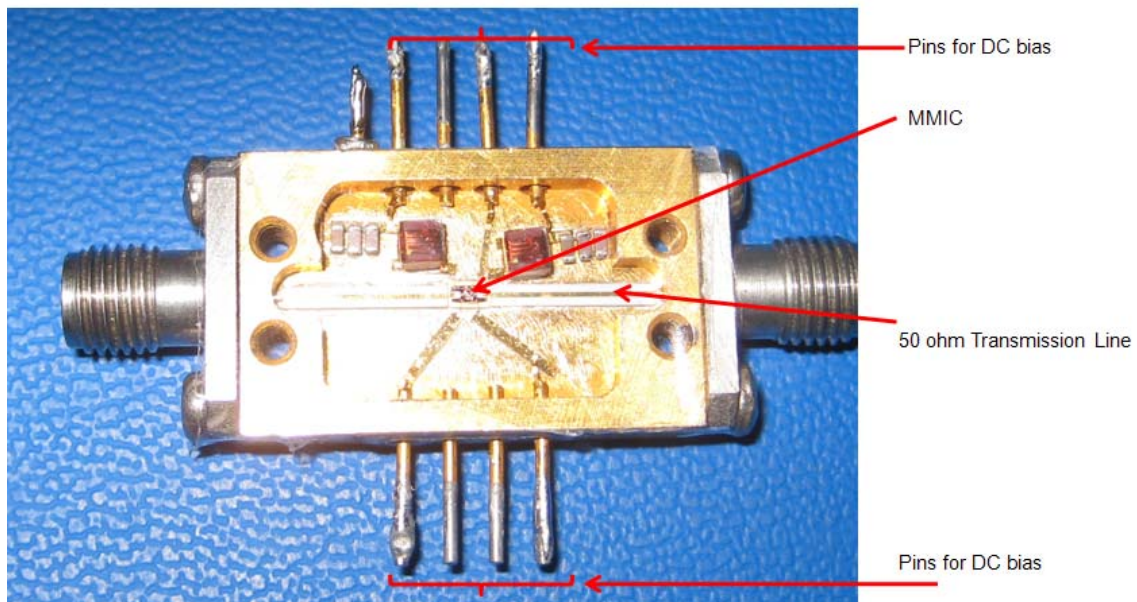


Figure 626: Packaged LNA with connectorized input and output

6.1: Small-signal Measurements on the Package

Small-signal measurements were performed using the Agilent E8362C network analyzer. The network analyzer was calibrated using the Agilent 85052D calibration kit. Short-Open-Load-Through (SOLT) calibration was performed. Figure 637 below plots the measured small-signal S-parameter return losses and gain vs. frequency at 300 K, measured at EPIR. Figure 648 shows the results of in-fixture small-signal S-parameter measurements of return loss and gain vs. frequency at 300 K, measured by our collaborator, IIT. Table 15 below lists the biasing points for this measurement. A comparison of Figure 63 and 77 reveals that these measurement results are repeatable and verifiable at separate test facilities.

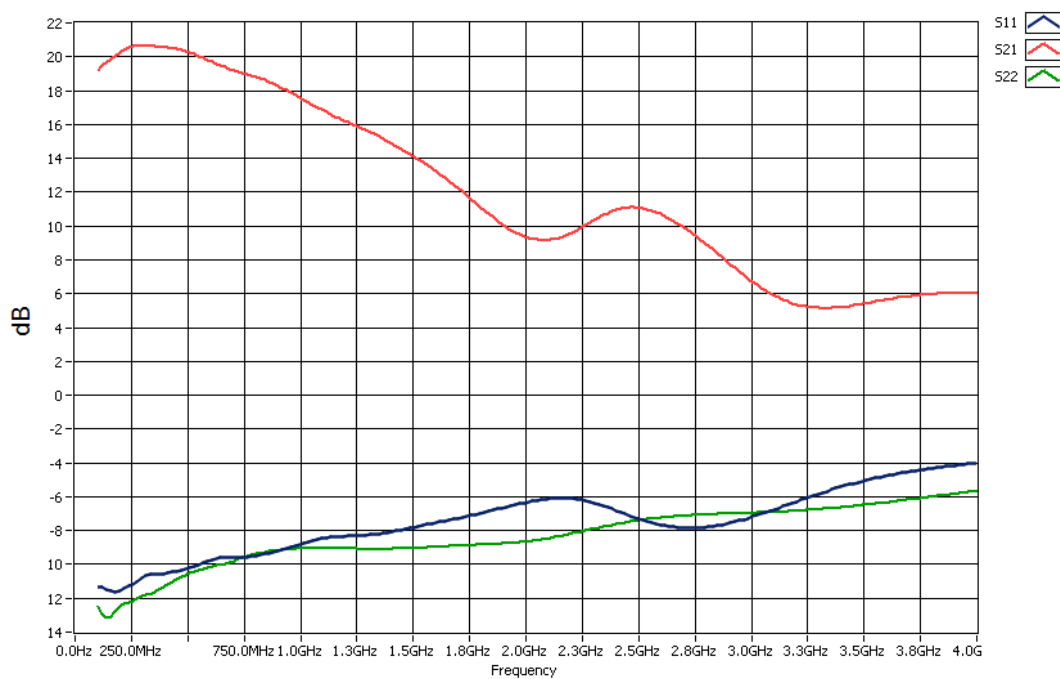


Figure 637: In-fixture measured small-signal S-Parameters vs. frequency at 300 K, measured at EPIR.

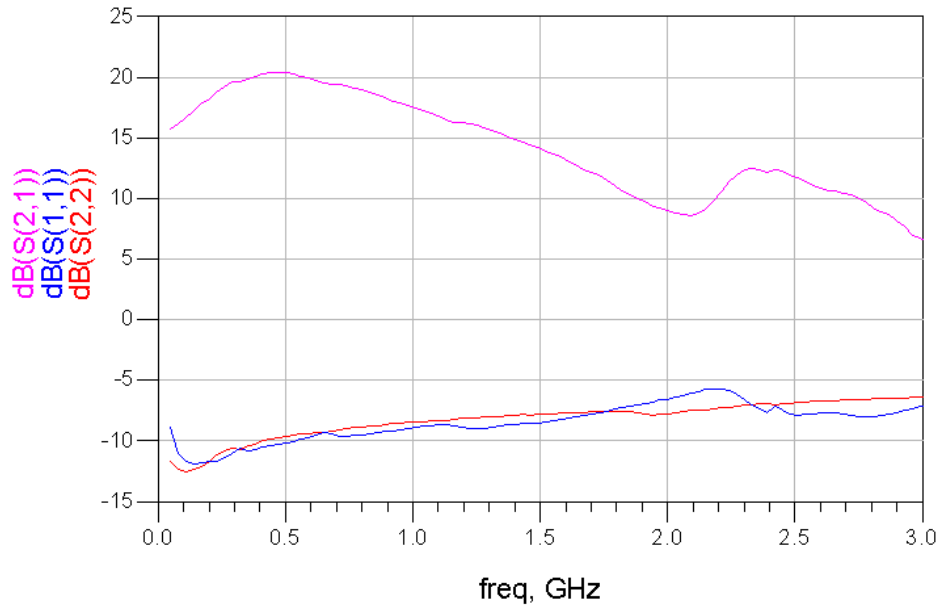


Figure 648: In-fixture small-signal S-Parameter measurements vs frequency at 300 K, measured by our STTR collaborator, IIT.

Table 15: DC Operating Points of the packaged LNA (300K)

V_{G1} (V)	V_{D1} (V)	I_{D1} (mA)	V_{G2} (V)	V_{G3} (V)	V_{D2} (V)	I_{D2} (mA)
-0.53	3.0	26	0.8	-0.55	3.0	10

Figure 79 below plots the measured noise figure when the DC current through the input stage was 27 mA and through the auxiliary amplifier stage was 10 mA. The measured noise figure was 1.1 dB at 1 GHz. These measurements were performed using a noise source with an ENR of 6 dB.

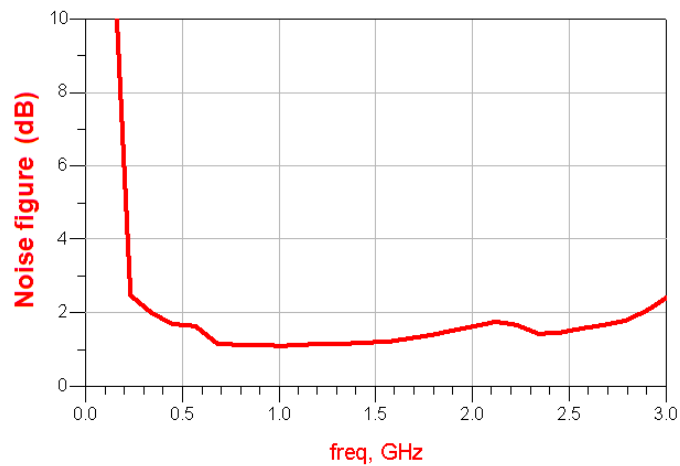


Figure 79: Measured small signal noise figure (test fixture based measurement) at 300 K

6.2 Large Signal measurements

The 1 dB gain compression point for the LNA was measured by sweeping the input power to the LNA keeping the frequency constant. This process was repeated for different frequencies. Figure 650 below plots the measured gain vs. input power at various frequencies across the band. It can be observed from Figure 80 that at a frequency of 1 GHz, the gain drops by 1 dB at an input power of -10.5 dBm. Therefore, the extracted 1 dB gain compression point (P_{out1dB}) is 7.5 dBm.

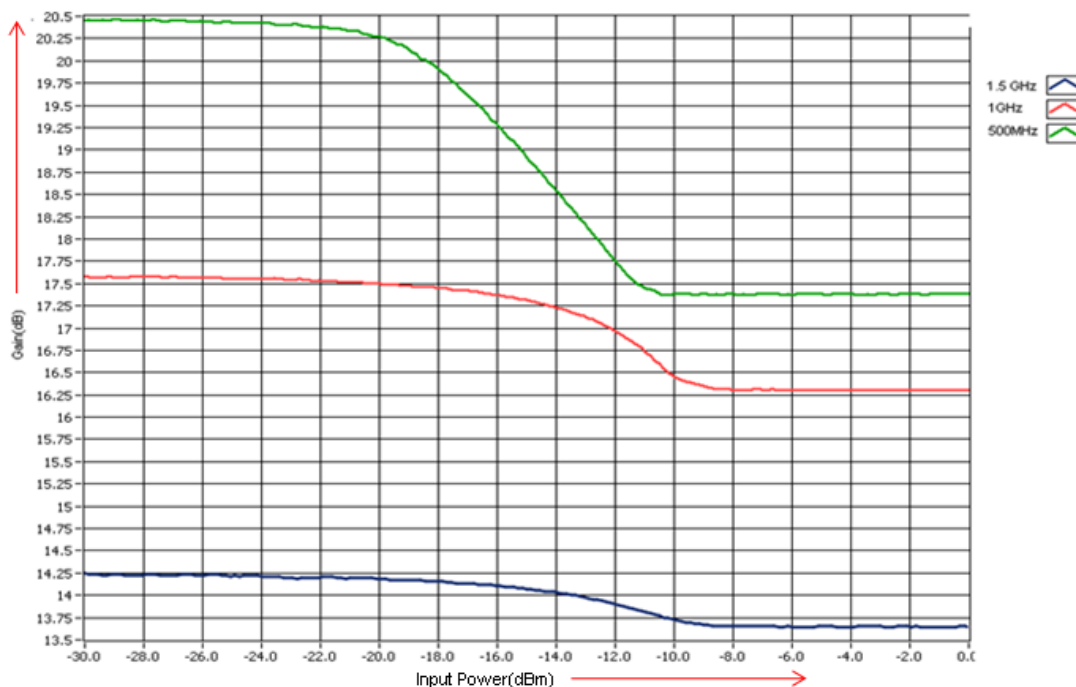


Figure 650: In-fixture measured gain (dB) versus input power (dBm) at 300 K.

P_{1dB} also was measured over a wide range of frequencies (instead of a finite number of frequencies). This was done by incorporating a LabView routine into the Vector Network Analyzer to sweep both input power and frequency. Figure 651 below plots the variation of the measured P_{in1dB} between 100MHz and 3GHz.

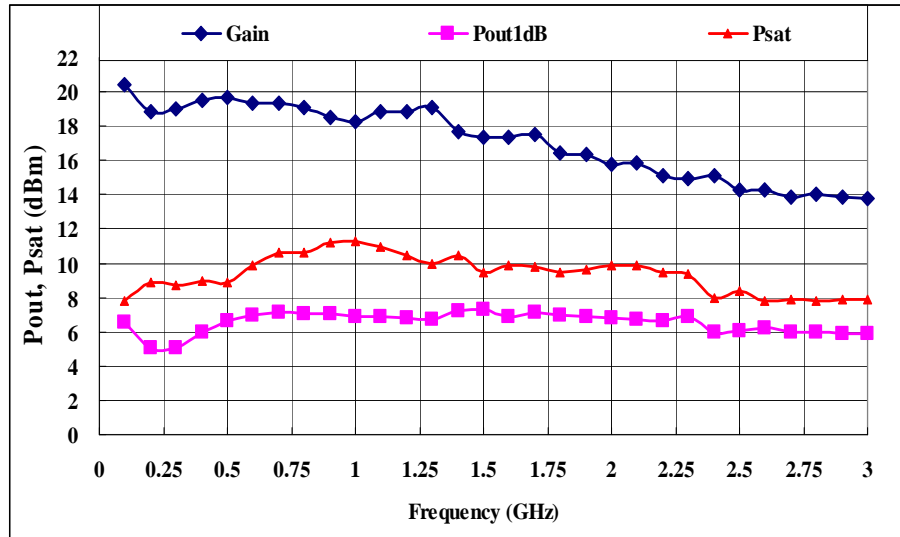


Figure 661: Measured large-signal characteristics as a function of frequency showing large signal gain (blue), the output power at 1dB gain compression point (pink) and the saturated output power (red)

7.0 Conclusion and Future Plans

An ultralow-noise broadband amplifier with feedforward noise cancellation has been implemented using 0.15 μm PHEMT technology. The amplifier is unconditionally stable at cryogenic temperatures and is suitable for cryogenic operation. Through the combination of feedforward noise cancellation and the pHEMT device, sub-1dB noise figures are possible. In this effort, a wideband LNA using a standard GaAs pHEMT process was realized. The gain and input/output return loss varied only slightly with temperature and the overall functionality of the LNA was maintained over a wide temperature range.

The amplifier has a die surface of 1 mm by 2 mm, and a gain that exceeds 17 dB between 200 MHz and 2.25 GHz. The matching at both input and output is better than -10 dB. The measured noise figure at room temperature is 1.1 dB at 700 MHz and 1.2 dB at 1.5 GHz. The measured results showed an improvement of approximately 0.9 dB in noise figure across the band. An ultralow-noise figure of 0.3 dB was measured at 120K. At cryogenic temperatures, the gain variation is approximately 1.5 dB, while the input/output match fluctuated without any disruption of the LNA behavior. The measured $P_{1\text{dB}}$ and P_{sat} are about 7 dBm and 10 dBm, respectively. At room temperature, the LNA draws 37 mA at a 3 V voltage. All the milestones of Phase II of this contract have been met. This Section compares our LNA with existing commercial LNAs available on the market and also discusses possible future enhancements to the LNA.

7.1 Commercialization Plans and Future Enhancements

7.1.1 Further Testing

All the tests on the prototype done so far have been performed at ambient temperatures. The behavior of the package at cryogenic temperatures must be examined by actual measurements. A major challenge is the placement of the temperature sensor on the package. Besides, the configuration of our cryogenic probe station for performing tests on connectorized devices needs to be established.

Once the probe station can be reconfigured for connectorized devices, the measurement technique will be similar to that used for die-level measurements. An SOLT calibration can be performed at ambient temperature using the 85052D calibration kit. Then the LNA package can be fixtured inside the cryoprober chamber and can be cooled down. For accurate temperature measurements, the LNA package will be modified for mounting a Lakeshore DT670 temperature diode.

Similarly, the LNA package will be tested at temperatures greater than the ambient (up to 60C).

7.1.2 Single Supply Biasing

While our MMIC has excellent small-signal characteristics, a single-supply biasing option can simplify system integration by reducing the number of required biasing lines. Our LNA can be used as a standalone amplifier.

If the MMIC needs to be integrated into an existing receiver system such as an L-band receiver, the peripheral biasing circuit must be optimized. Our MMIC LNA uses via ground for source terminals to maximize the high-frequency performance. While the gate-source junction requires a negative bias, the drain terminal is always biased at a positive voltage. In our MMIC, the gate voltages (for both the input stage and the noise-cancellation stage) are biased at the same negative voltage of -0.5 V. The drain voltage of both the stages is 3 V. Biasing these devices requires both a negative and a positive supply and sequential biasing of the gate and drain terminals. For the hybrid designer, this type of MMIC may be difficult to use as a direct replacement for MMIC modules due to single-supply restrictions.

The number of power supply lines can be reduced by isolating the RF and DC grounds. Specifically, if the source terminal is referenced to a fixed positive voltage and the gate terminal is left unbiased, a negative V_{GS} can be obtained. This can be achieved without modifying the circuit design (and without requiring foundry iteration).

One such configuration is shown in Figure 82 below. The MMIC LNA can be mounted on a silicon metal oxide (MOS) capacitor, thereby isolating the ground from dc.

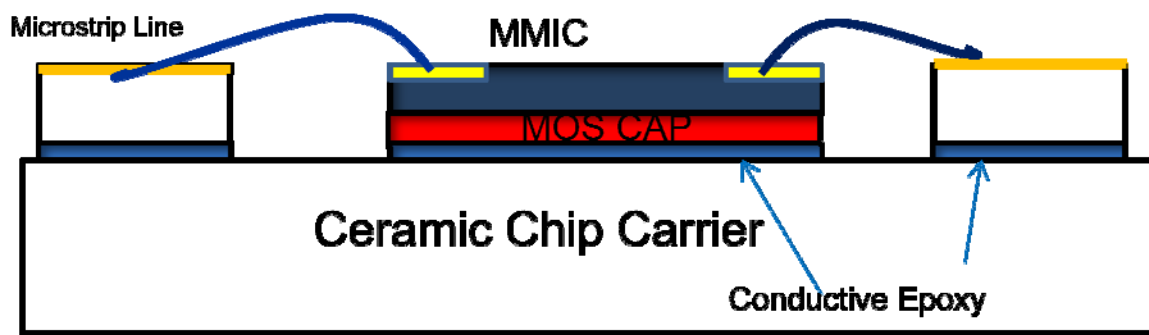


Figure 672: Mounting of MMIC for isolation of DC and RF ground

The FET source can be floated from ground at DC through the MOS capacitor.

In addition to the MOS capacitor, a resistance at the source terminal can be used to maintain a positive bias at the source. The gate terminal can be biased at 0V. Since the input to the LNA is at the gate terminal and the RF input is always referenced to ground, a negative V_{GS} will be automatically created. Figure 683 shows one such configuration.

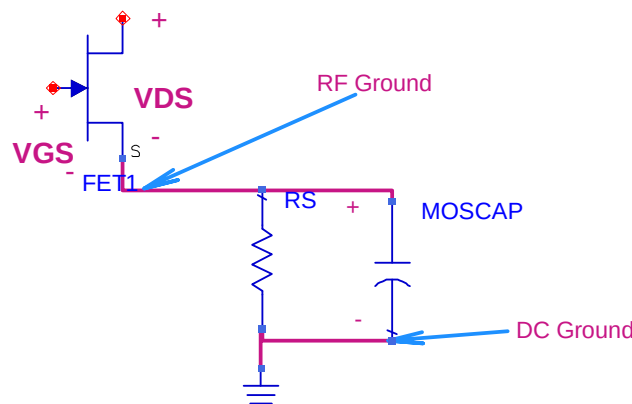


Figure 683: Circuit for generation of a negative V_{GS} by isolating the RF and DC grounds [10]

Current flows through the resistor R_s causing a gate-to-source voltage drop, $V_{GS} = -I_D R_s$. The operating current is obtained from the square-law transfer equation

$$I_{DS} = I_{DSS} [1 - (V_{GS}/V_p)]^2$$

By combining these equations, one can solve for R_s . In our case, $V_{GS} = -0.5$ V, $I_{DS} = 27$ mA for the input stage. The pinch-off voltage V_p is approximately -1V. Therefore, R_s will be 18 Ω . One potential issue is the feedback generated by R_s . However, if the underlying MOS capacitor is large enough, any RF signal at the source terminal will be grounded and the source feedback can be negated. The MMIC will only require commercial off-the-shelf resistors for biasing. Commercial MOS capacitors such as Skyworks SC99906068 [9] can be used.

7.2 Potential Commercial Applications

While the Phase II efforts have been focused on a heterodyne detection application, a number of other commercial applications exist for our LNA. The operating frequency of our LNA falls under the L-Band. The peak gain of our LNA is centered at 900MHz. The LNA can be used in front-end electronics or as an IFA (intermediate frequency amplifier). Both commercial radio and navigation systems use the L-band (1-2GHz). These applications require a low-noise front end. Noise-figure performance is the key parameter in receiver systems, and describes the capability for the reception of low-level signals. Table 16 below compares our LNA with existing commercial LNA s in this band.

Table 16: Comparison of our LNA with commercial L-Band LNAs

Vendor	Catalog No	Technology	Operable Freq. Span/Center Freq (GHz)	Gain	Noise Figure (300K, 1GHz)	Operating Temp.(K)	DC power	P1dB (output)
TriQuint	TQP369182	InGaP/InGaAs HBT	DC-6	21	3.9	220-420	202.5	27.6
Freescall	MBC13916	SiGe	0.2-2.5	19	1.9	233-358	100	22
Freescall	MML09211	pHEMT	0.9	20	0.5	208-423	900	20
Skyworks	SKY67101	GaAs pHEMT	0.4-1.2	17.5	0.6	208-423	200	18
Hittie Microwave	HMC636ST	GaAs pHEMT	0.2-4	13	2.2	233-423	800	22
RFMD	SGL0622Z	SiGe HBT	0.1-3	25	1.6	233-423	32	5.3
<i>This LNA</i>		<i>0.15μm pHEMT</i>	<i>0.1-3.5</i>	<i>20</i>	<i>1.1</i>	<i>77-300¹</i>	<i>100</i>	<i>8</i>

¹ LNA has not been tested above 300K

The main market driver in this band is cellular telephony, followed by CA-TV. There is need for a wideband low-noise amplifier with high IP₃. For satellite uplink receivers, a wide operating temperature also is a requirement. Our LNA has demonstrated operability over a wide temperature range. Besides, the ultralow-noise figure of our LNA at low temperatures can improve detection thresholds in satellite communications.

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