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Somnath Chattopadhyay

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California State University - Northridge
18111 Nordhoff Street

Northridge, CA 91330 -8232

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14. ABSTRACT

During 2012-2013, some analytical models have been developed and the results were inputted to the Synopsys Sentaurus TCAD. The device structure and dimension were optimized and the device performance was tested for conductive substrate and semi-insulating substrate. The wafer specification and mask layout were prepared by the combination of Synopsys Sentaurus TCAD and analytical modeling. In 2014, high quality oxide development has been obtained by the combination of thermal oxidation and sputtering oxide deposition and the research work has outstanding merit as indicated by two peer reviewed publications in reputed journals. In 2015, the impurity profile

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Report Title

Final Report: SiC/GaN Based Optically Triggered MESFET for High Power Efficiency and High Radiation Resistance Solid State Switch Application for Actuator System

ABSTRACT

During 2012-2013, some analytical models have been developed and the results were inputted to the Synopsys Sentaurus TCAD. The device structure and dimension were optimized and the device performance was tested for conductive substrate and semi-insulating substrate. The wafer specification and mask layout were prepared by the combination of Synopsys Sentaurus TCAD and analytical modeling. In 2014, high quality oxide development has been obtained by the combination of thermal oxidation and sputtering oxide deposition and the research work has outstanding merit as indicated by two peer reviewed publications in reputed journals. In 2015, the impurity profile for source and drain and junction depth has been designed and nitrogen ion implantation has been performed followed by high temperature annealing. In 2016, the device electrical isolation has been performed using high energy Argon with high ion dose to create high resistivity amorphous barrier surrounding the active device area. Ohmic contact by nickel deposition and ITO Schottky contact by bi-layer lift-off process has been established. I-V characteristics of the fabricated SiC MESFET have been obtained by curve tracer showing clear indication of linear and non-linear properties with DIBL effects and process induced defects. Threshold voltage, transconductance and pinch-off voltage have been determined.

Enter List of papers submitted or published that acknowledge ARO support from the start of the project to the date of this printing. List the papers, including journal references, in the following categories:

(a) Papers published in peer-reviewed journals (N/A for none)

Received		Paper
04/13/2016	4.00	Somnath Chattopadhyay, Subba Kodigala, Charles Overton, Ira Ardoin. Fowler–Nordheim electron tunneling mechanism in Ni/SiO2/n-4H SiC MOS devices, Solid-State Electronics, (12 2015): 104. doi: 10.1016/j.sse.2015.08.017
09/09/2015	2.00	Subba Kodigala, Somnath Chattopadhyay, Charles Overton, Ira Ardoin, BJ Gordon, D Johnstone, D Roy, D Barone. Growth and surface analysis of SiO2on 4H-SiC for MOS devices, Applied Surface Science, (03 2015): 465. doi:
TOTAL:	**2**	

Number of Papers published in peer-reviewed journals:

(b) Papers published in non-peer-reviewed journals (N/A for none)

Received		Paper
TOTAL:		

Number of Papers published in non peer-reviewed journals:

(c) Presentations

Number of Presentations: 0.00

Non Peer-Reviewed Conference Proceeding publications (other than abstracts):

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TOTAL:

Number of Non Peer-Reviewed Conference Proceeding publications (other than abstracts):

Peer-Reviewed Conference Proceeding publications (other than abstracts):

Received	Paper

TOTAL:

Number of Peer-Reviewed Conference Proceeding publications (other than abstracts):

(d) Manuscripts

Received	Paper	
08/29/2014	1.00	Charles Overton, Ira Ardoin, Dragana Barone, Subba Kodigala, Somnath Chattopadhyay. Growth and Surface Analysis of SiO2 on 4H-SiC, Applied Surface Science (08 2014)
09/09/2015	3.00	Subba Kodigala, Somnath Chattopadhyay, Charles Overton, Ira Ardoin. Fowler-Nordheim electron tunneling mechanism in Ni/SiO2/n-4H SiC MOSdevices, Solid State Electronics (07 2015)

TOTAL: **2**

Number of Manuscripts:

Books

Received Book

TOTAL:

Received Book Chapter

TOTAL:

Patents Submitted

Patents Awarded

Awards

Graduate Students

NAME	PERCENT_SUPPORTED	Discipline
Ira Ardoin	0.50	
FTE Equivalent:	**0.50**	
Total Number:	**1**	

Names of Post Doctorates

NAME	PERCENT_SUPPORTED
Subba Kodigala	0.50
FTE Equivalent:	**0.50**
Total Number:	**1**

Names of Faculty Supported

NAME	PERCENT_SUPPORTED	National Academy Member
Somnath Chattopadhyay	0.50	
FTE Equivalent:	**0.50**	
Total Number:	**1**	

Names of Under Graduate students supported

NAME	PERCENT_SUPPORTED
FTE Equivalent:	
Total Number:	

Student Metrics

This section only applies to graduating undergraduates supported by this agreement in this reporting period

The number of undergraduates funded by this agreement who graduated during this period:	0.00
The number of undergraduates funded by this agreement who graduated during this period with a degree in science, mathematics, engineering, or technology fields:.....	0.00
The number of undergraduates funded by your agreement who graduated during this period and will continue to pursue a graduate or Ph.D. degree in science, mathematics, engineering, or technology fields:.....	0.00
Number of graduating undergraduates who achieved a 3.5 GPA to 4.0 (4.0 max scale):.....	0.00
Number of graduating undergraduates funded by a DoD funded Center of Excellence grant for Education, Research and Engineering:.....	0.00
The number of undergraduates funded by your agreement who graduated during this period and intend to work for the Department of Defense	0.00
The number of undergraduates funded by your agreement who graduated during this period and will receive scholarships or fellowships for further studies in science, mathematics, engineering or technology fields:	0.00

Names of Personnel receiving masters degrees

NAME
Gandhi Dipakbhai
Shrotin Hendre
Aditya Naidu
Bhavik Patel
Praneeth Thota
Jimit Gandhi
Sushma Malku
Swaroop Jallipeta
Sai Nikitha Rudraraju
Anish Vemulapalli
Dileep Reddy Goda
Total Number: **11**

Names of personnel receiving PHDs

NAME
Total Number:

Names of other research staff

NAME	PERCENT_SUPPORTED
FTE Equivalent:	
Total Number:	

Sub Contractors (DD882)

Inventions (DD882)

Scientific Progress

See attachment below.

Technology Transfer

Scientific Progress and Accomplishments

During 2012-2013, the research work was focused on optimization of SiC and GaN MESFET device structure by using Synopsys Sentaurus TCAD and mask design for photolithography process. SiO_2 contributes an important role for device fabrication serving as process masking, electrode isolation, device isolation, etc. In 2014, the research effort was conducted to produce high quality and low interface trap density SiO_2 layer formation onto SiC material recognized through peer reviewed publication in the journal. The research was focused on the process for maximizing the quality SiO_2 formation and minimizing the interface trap density on SiC materials by the combination of thermal oxide growth at very specific temperature ≈ 1175^{o}C followed by nitradation and oxide film deposition by plasma sputtering physical vapor deposition (PVD). The SiO_2 layers were grown onto C-face and Si-face 4H-SiC substrates by different techniques such as wet/dry thermal oxide process and sputtering. The SiO_2 formation onto SiC is initiated by the thermal oxidation followed by high temperature nitradation and sputtering deposition. The growth effects of SiO_2 on the C-face and Si-face 4H-SiC substrates are thoroughly investigated by AFM analysis.

During 2015-2016, a detailed research work on developing the 4H-SiC MESFET was conducted by different front-end and back-end wafer processing (i) forming the source and drain contact by ion implantation, (ii) the rapid thermal annealing processing, (iii) device isolation by using ion implantation process, (iv) optimization of nickel film for ohmic contact, (v) Lift-off process and indium tin oxide deposition for Schottky gate contact and (v) electrical characterization and described chronologically.

(i) **Source-drain Formation:** Ion implantation service for drain and source formation has been conducted in the Cutting Edge Ions, LLC with the following parameters.

(a) Ion Dose: $2x10^{15}cm^{-2}$
(b)Ion Energy: 80KeV
(c) Ion Species: Nitrogen
(d)In-situ Temperature during ion implantation: 500^{o}C
(e)Tilt Angle: 0^{o}

(ii) **Rapid Thermal Annealing (RTA) Processing:** RTA processing is required to cure the wafer from amorphous to single crystal and also to electrically activate ion dopant species. In order to conduct the high temperature annealing in the temperature range of 1700^{o}C to 1800^{o}C, a detailed search for different Universities and federal laboratories has been continuously conducted for three months. A response was received from the Naval Research Lab for high temperature annealing of SiC sample of 5mm x 5mm and the laboratory has no facility to offer the high temperature annealing service of 3 inch ion implanted SiC wafer. Another response was received a German company and the high temperature annealing for SiC was quoted in the range of $5000 to $7000 per annealing service. In this situation, the planning for high temperature annealing has been diverted

from the facility search to equipment procurement. A detailed study on different high temperature annealing capable furnaces has been studied and finally, a US made furnace produced by Micropyretics Heaters International of Cincinnati, OH has been procured and finally installed in our laboratory. This furnace was extremely suitable for high temperature furnace annealing having a rise-time at 1600^{o}C with ramp 10^{o}C per minutes and ramp down 20^{o}C/minutes depending on the argon flow and the main annealing time was scheduled for only 10 minutes. The minimum time and maximum temperature were optimized to complete the entire temperature cycle with a short duration at 1600^{o}C (under 10 minutes) for three hours. In order to avoid the sublimation of silicon from SiC wafer, the SiC wafer was coated with AlN film with a thickness of 700Å. AlN film thickness of about 700Å has been deposited by sputtering PVD system. This process involved a 3inch 99.9% AlN sputter target sourced from Angstrom Sciences, Inc. of Duquesne, PA. RF sputtering occurred at 2.5mTorr with 99.999% Argon and Nitrogen at a ratio of 100:1 as the sputtering gas. RF power was 125 watts for 25minutes. The ion implanted SiC wafer was annealed in the furnace for three hours in argon ambient. AlN film on SiC was found to be extremely difficult to etch by KOH, NaOH and HF. The characteristic analysis of surface morphology has been performed by Atomic Force Microscopy (AFM), Bruker in Santa Barbara, CA. AFM analytical characterization has been conducted to study the surface and detailed micrograph of AFM has been depicted in Figure 1 and 2.

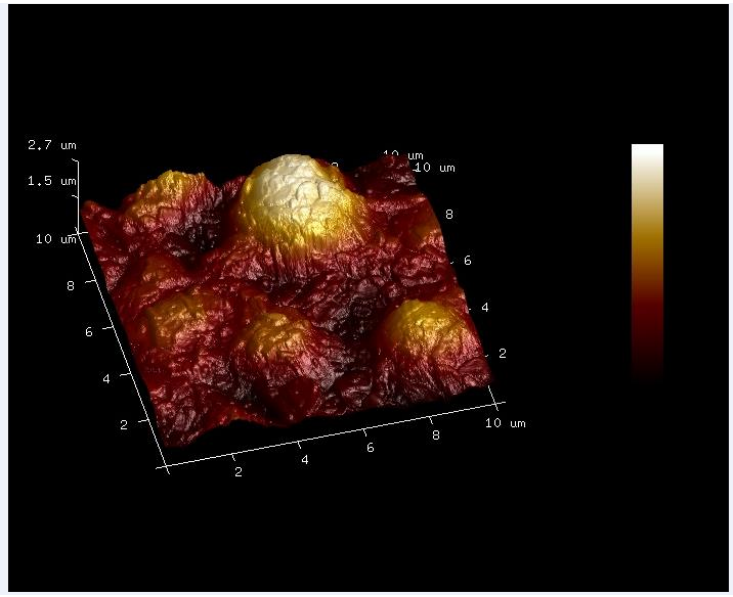

Figure 1: AFM micrograph showing the transformation of AlN to Al_2O_3

Figure 1 presents the AFM characterization showing the surface roughness due to the AlN and its transformation to Al_2O_3 with peak height range from 1.5µm to 2.5 µm. The phase transformation of AlN to Al_2O_3 covers 90% of the surface.

Dr. Somnath Chattopadhyay
CSU Northridge, 18111 Nordhoff St. Northridge, CA 91330
somnath.chattopadhyay@csun.edu
1-818-677-7197

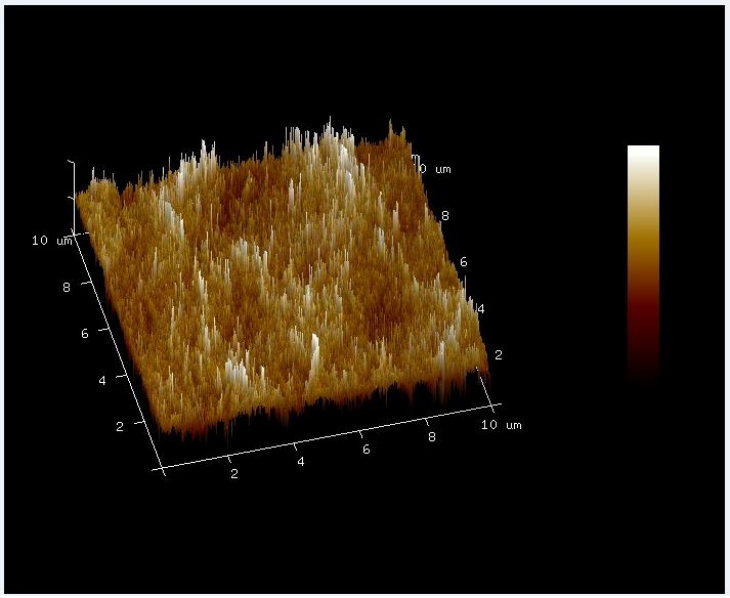

Figure 2: AFM Micrograph showing the roughness due to the AlN and Al_2O_3

The Figure 2 displays the AFM micrograph showing clearly surface roughness due to AlN film and Al_2O_3 growth at high temperature of 1600^{o}C. For annealing with pressures of argon at the temperature of 1600°C, the surface of AlN layers became rough because of the Al_2O_3 decomposition from the interface of the AlN layer on SiC surface. In order to get complete picture of AlN film and high temperature phase transformation of the Al_2O_3 film which was causing a shielding effect preventing proper etching, an Auger study has been conducted at the Seal Laboratory at Los Angeles.

Dr. Somnath Chattopadhyay
CSU Northridge, 18111 Nordhoff St. Northridge, CA 91330
somnath.chattopadhyay@csun.edu
1-818-677-7197

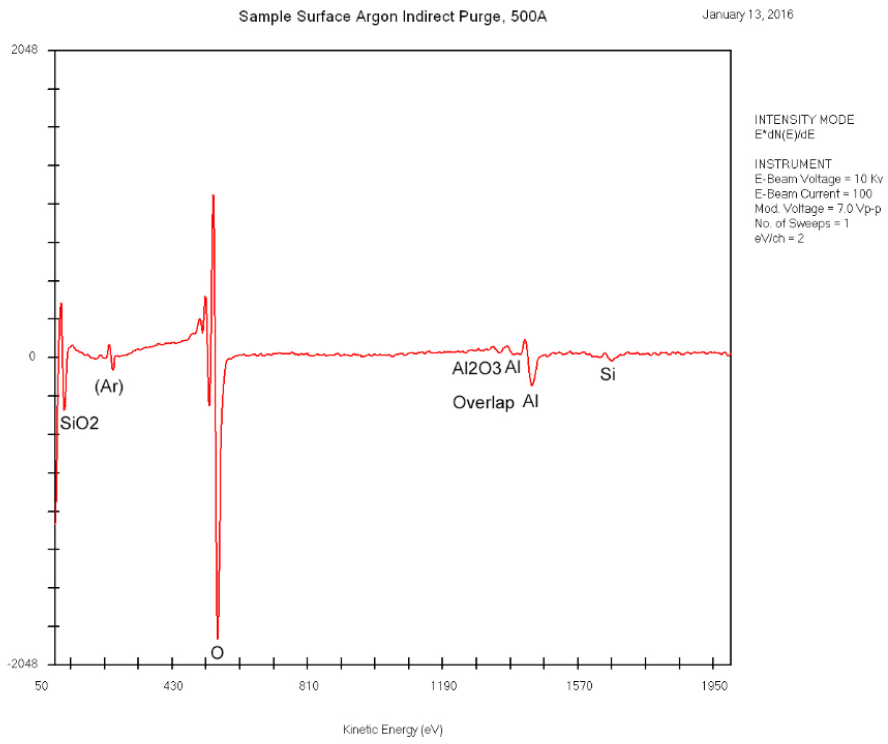

Figure 3: Surface morphology study using Augerscope

Figure 3 shows the surface morphology study of high temperature annealed AlN film. The Auger study shows the trace of SiO_2, Argon, Al_2O_3, Al and silicon. The study shows that some silicon has been sublimated and trapped in the Al_2O_3. Hence Al_2O_3 acts as a barrier layer to prevent any sublimation of Si at high temperature. The trace of Al contain confirms the escape of nitrogen contain for conversion of Al_2O_3 formation. This study confirms the cause of hard shielding against etching by KOH due to the layer of SiO_2 and Al_2O_3. The sample was initially etched by dilute HF to remove the oxide layer. The sample was again dip in the hot KOH at 70^{o}C followed by NaOH dipping at 70^{o}C and the Al_2O_3 film was removed.

(iii)**Device isolation by using ion implantation process:** The device isolation is important process step to electrically isolate the active area of the transistor from other device in the wafer. The trench formation and oxide filling is generally conducted for device isolation in silicon carbide is extremely tedious work because most of plasma etching to date for trench formation has been performed by the reactive ion etching (RIE) of silicon carbide in fluorinated-gas (CHF_3, $CBrF_3$, CF_4, SF_6 and NF_3) plasma and inductively coupled plasma (ICP) etchings. One attribute of this technique is the high energy (typically > 200eV), which is useful in breaking the bonds in the SiC. However a downside to high ion energies during RIE and ICP is mask erosion, residual lattice damage in the SiC and surface damage causing potential degradation of the electrical performance of the device. Ion implantation allows electrical isolation, which is used in several state-of-the-art semiconductor device

processing. The use of ion implantation for selective area doping and isolation is a critical requirement for advancement of GaN and SiC device technology. To date there has been little work in this area, and generally implantation has been used to introduce impurities for study of their optical properties. In order to avoid the RIE and ICP etching technique for device isolation, an innovative process of device electrical isolation by ion implantation has been developed by using argon (Ar) ion species of ion dose of $1x10^{15}/cm^2$, ion energy of 350KeV implant range parameter of 2329Å and straggle parameter of 410Å to achieve a junction depth of 0.425µm which are calculated by the SRIM simulator and MatLab to isolate the active areas of the device in wafer level shown in Figure 4. The photolithography process was performed to keep the oxide layer of 400Å for selective ion implantation and photoresist (S1813) thickness of 1.5 µm for masking the ion species.

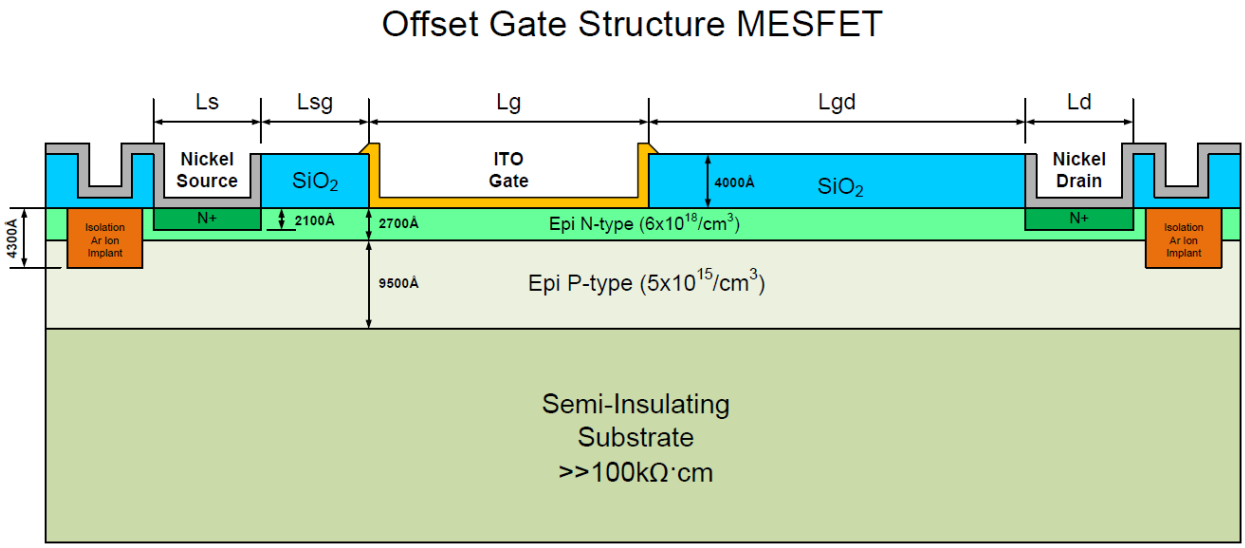

Figure 4: Isolation of active areas by using ion implantation

The Ar impurity distribution and the junction depth in both PMMA and SiC have been investigated to study any leakage of argon ions through the PMMA. The required ion energy and, ion dose of SiC and PMMA have been optimized from SRIM and Matlab and the result has been depicted in the following Tables 1 and 2.

Ion Energy	dE/dx Electron	dE/dx Nuclear	Projected Range	Lateral straggling	Junction depth
200 KeV	2.791E+00	1.559E+00	1675Å	314 Å	0.308µm
275 KeV	2.879E+00	1.489E+00	1839 Å	338 Å	0.335µm
300 KeV	2.963E+00	1.426E+00	2003 Å	363 Å	0.362µm
350 KeV	3.124E+00	1.318E+00	2329 Å	410 Å	0.425 µm
375KeV	3.203E+00	1.271E+00	2492 Å	433 Å	0.441 µm

Dr. Somnath Chattopadhyay
CSU Northridge, 18111 Nordhoff St. Northridge, CA 91330
somnath.chattopadhyay@csun.edu
1-818-677-7197

Table 1: Simulated result of projected range and straggle parameters and junction depths for different argon ion doses and ion energies for Argon implantation into SiC.

Ion Energy	dE/dx Electron	dE/dx Nuclear	Projected Range	Lateral straggling	Junction depth
200 KeV	3.226E+00	2.324E+00	2934Å	414 Å	0.477µm
275 KeV	3.592E+00	1.991E+00	4026Å	537Å	0.638µm
300 KeV	3.704E+00	1.903E+00	4389Å	576 Å	0.690µm
350 KeV	3.919E+00	1.753E+00	5112 Å	652 Å	0.794µm
375KeV	4.022E+00	1.687E+00	5471 Å	689 Å	0.845µm

Table 2: simulated results of projected range and straggle parameters and junction depths for different argon ion doses and ion energies for Argon implantation into PMMA.

In order to achieve the effective device isolation, the resultant junction depth of 0.425µm was kept to penetrate up to epitaxy p-buffer layer. Ar+ ion implantation is not only an excellent electrical isolation method but also a good technique to remove the leakage paths by maintaining planar surface after the device isolation process. Generally, Ar-implantation leads to produce the resistivity of 10^{10}ohm-cm at room temperature because the crystal structure becomes amorphous, because Ar prefers to stay at an interstitial position.

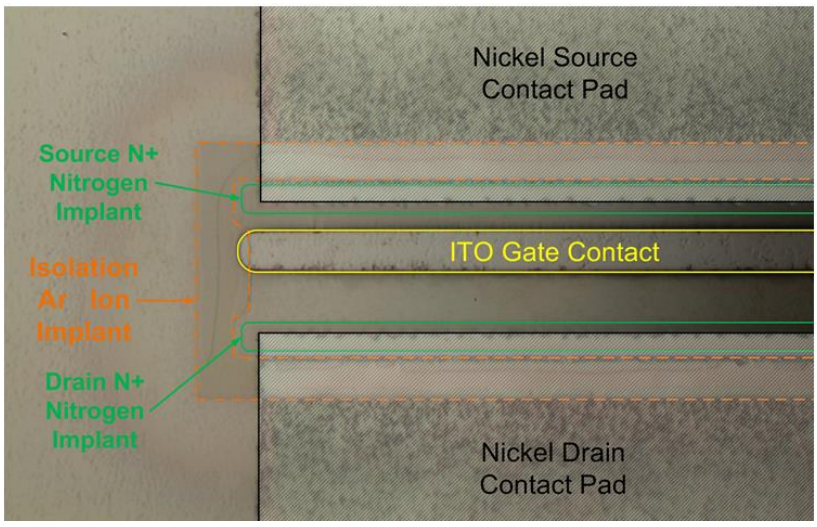

Figure 5: Photograph of patterns for Ar isolation, ITO gate and source/drain contact pad.

Figure 5 shows the pattern of argon ion implant isolation, source and drain nickel contact pads and indium tin oxide (ITO) gate contact. The device isolation needs extremely careful selection of the ion energy and resultant ion beam current, because high ion beam current generates excessive heat, cooking the photoresist causing it to carbonize, which is extremely hard to

Dr. Somnath Chattopadhyay
CSU Northridge, 18111 Nordhoff St. Northridge, CA 91330
somnath.chattopadhyay@csun.edu
1-818-677-7197

clean/etch. Excessively hard-baked photoresist can usually be dissolved in piranha etching solution. 48 hours of piranha etching worked for all but the hardest carbonized portions of photoresist. Followed by the piranha etch, the wafer was further cleaned in an oxygen rich plasma cleaning process, using our plasma sputtering system. Due to a lack of a dedicated ashing (high pressure oxygen plasma cleaning) system, we adapted the sputtering system for the maximum oxygen content at the highest process pressure the system would allow. Typical ashing systems use up to a 500 watt RF plasma in a 100mTorr oxygen environment. For our process, 18mTorr with argon to oxygen mix ratio of 5:3 was used. 75 watts RF power for 25minutes was sufficient with minimal collateral damage to the wafer features. Figures 6 and 7 illustrate the problem and progress at each step.

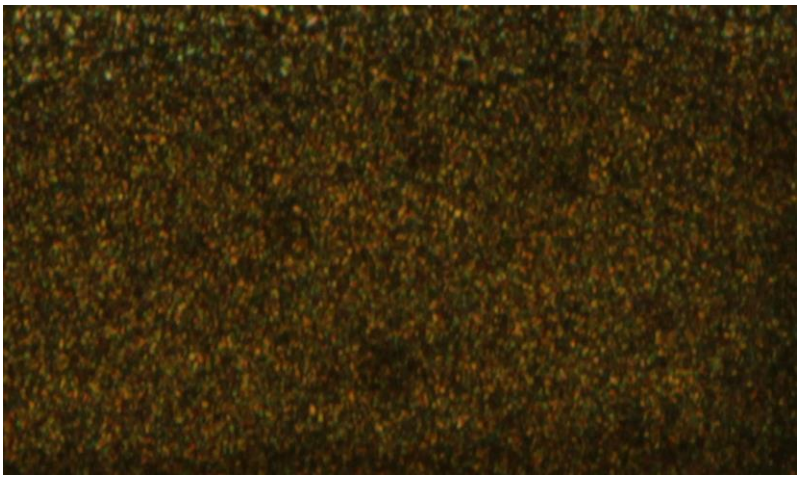

Figure 6: Extreme charring of the photoresist (PR) due to heating of the wafer during Ar ion implantation for isolation is shown. The PR started to undergo carbonization.

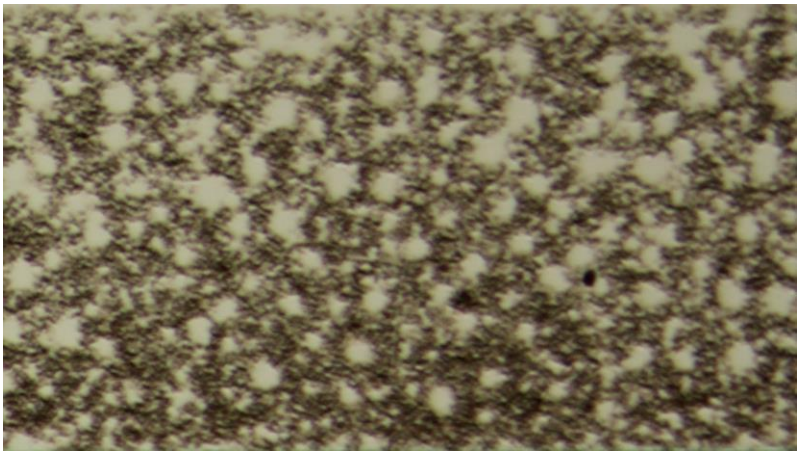

Figure 7: Piranha solution has been used as an aggressive cleaning etchant for organic residue. The worst of the carbonized PR has not been removed even after 48 hours of exposure to the piranha solution.

Dr. Somnath Chattopadhyay
CSU Northridge, 18111 Nordhoff St. Northridge, CA 91330
somnath.chattopadhyay@csun.edu
1-818-677-7197

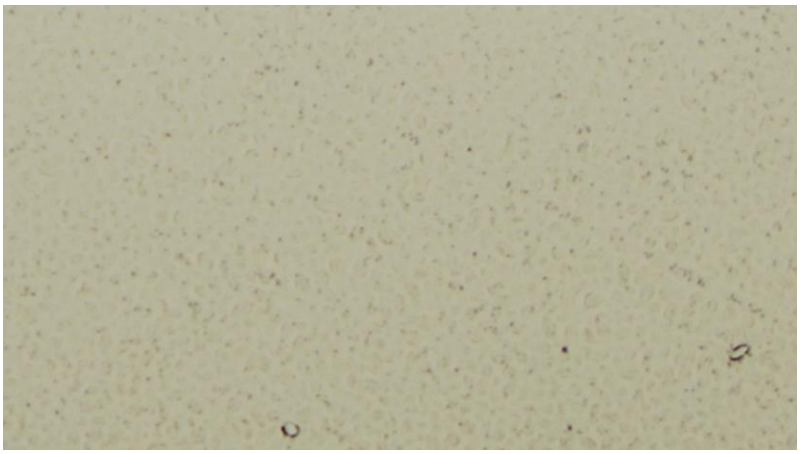

Figure 8: The wafer was further cleaned in a oxygen rich plasm clean step. 18mTorr with Argon to Oxygen ratio of 5:3 is used with RF power set to 75 watts for 25 minutes.

(iv) Optimization of nickel film for ohmic contact: Nickel, being a metal and a good conductor is relatively easy to sputter. However, due to the magnetic properties of the pure nickel metal, the plasma concentrating function of the magnetron on a conventional sputter gun is somewhat subdued. In order to minimize this problem, a thinner (0.125 inch, rather than 0.250 inch) target is used. Several samples of nickel sputtering at various pressures and power levels were iteratively tested on glass blanks in order to test conductivity and deposition rates. Additionally, nickel is prone to excessive film stress, which can cause cracking and peeling after deposition. Additional study into the optimum parameters for minimizing film stress was conducted. Ultimately a process of 2.8mTorr Argon at 250 watts for 15 minutes results in a nickel deposition of about 1500Å with a bulk resistivity of about 7.1μΩ·cm, without need for follow-up annealing or 'sintering' was chosen.

(v) Lift-off process and indium tin oxide (ITO) deposition for Schottky gate contact: Due to the difficulty of pattering ITO via selective etching, without damaging the other features on the wafer, it was decided to use a bi-layer lift-off photolithography process for the ITO patterning. The process involves use of our standard photoresist (PR), Shipley S1813, however an additional non-photosensitive (PMGI SF6) layer is first applied vie spin coating, before the PR. The PMGI is spin coated onto the freshly cleaned and dried wafer at 3000RPM, then soft-baked at 180ºC for 120 seconds. This gives a PMGI layer of about 0.4μm. Then the PR is spin coated onto the wafer at about 4000RPM and soft baked at 115ºC for 90seconds, resulting in a PR layer about 1.3μm thick. The wafer is then exposed to 360nm UV, through the ITO pattern mask for 22 seconds. After exposer, the wafer is then developed by immersion and stirring in CD-26 developer for 50 seconds. The wafer is then rinsed thoroughly with de-ionized water for 120 seconds, and dried with nitrogen. After inspection to verify the quality of the pattern and the presence of the undercut (see illustration), the wafer is then hard-baked at 125ºC for 180 seconds. If everything looks good, the wafer is then loaded into the plasma sputtering system for ITO deposition. The ITO film thickness of about 800Å has been deposited by sputtering PVD

system. This process involved a 2000 seconds deposition; 125 Watts RF Power; 18cm working distance; 75mm target diameter; In_2O_3/SnO_2, 90/10 wt% target material; 100mm substrate diameter, and 99.999% Argon and Oxygen at a ratio of 100:1 as the sputtering gas. The target is supplied by Kurt Lesker, Inc. of Jefferson Hills, PA. When the deposition is complete the wafer is then cleaned in an ultra-sonic bath of CD-26 which quickly can enter through the gap formed by the undercut, and wash out the PMGI. Follow-up cleaning with acetone and isopropyl alcohol then spin-rinse-drier complete the cleaning, and the wafer is then ready for testing.

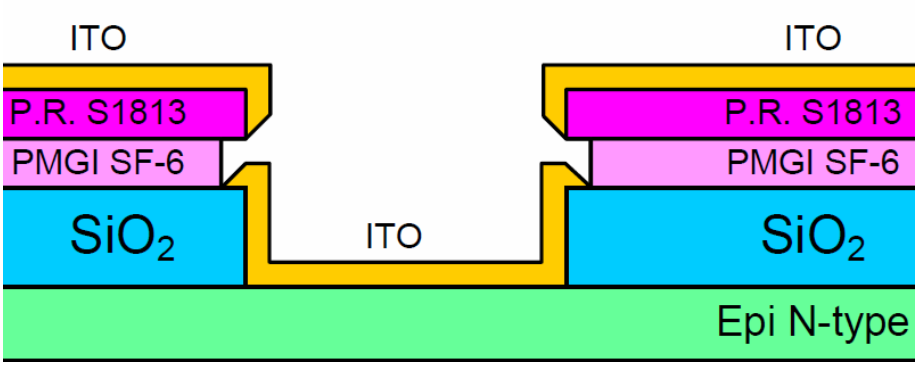

Figure 9: Stack-up of bi-layer lift-off photolithography process is shown (not to scale). The undercut feature where some extra PMGI is washed out by the developer is needed in order that the ITO cannot form a seal on the side wall. This allows for the solvent to attack the PR after the deposition during the "lift-off" step.

(vii) Electrical characterization: The I-V characteristics of fabricated SiC MESFET have been extracted from Tektronix 370A curve tracer. In order to find different I-V characteristics of different gate off-set structures and device widths have been considered to present the result for study the device performances. The gate off-set structure in MESFET is preferred to achieve high power density by avoiding electrical crowding in the bulk. Also, the impurity concentration of the channel of MESFET was intensionally kept higher range compared to conventional MESFET device in order to obtain a higher power density.

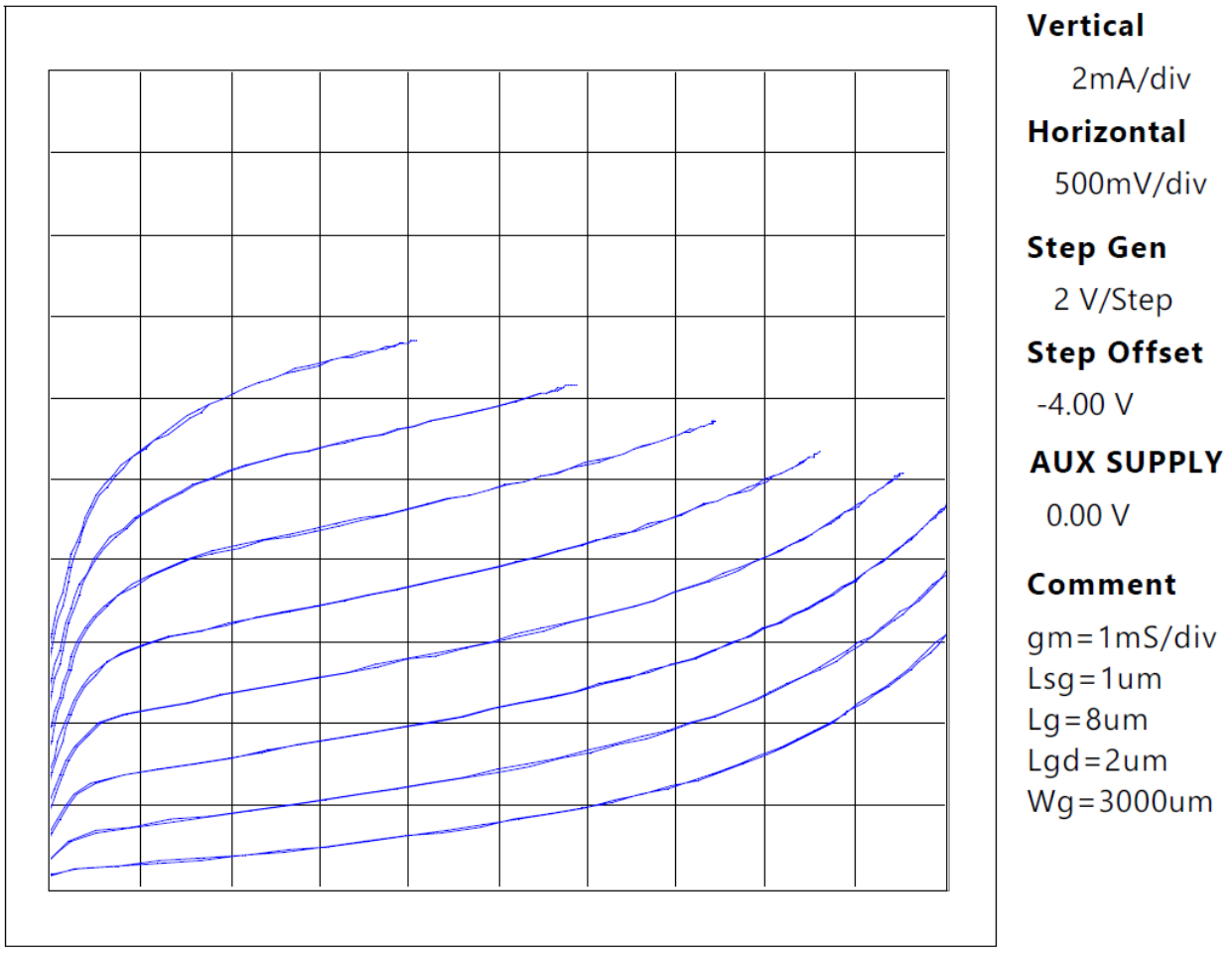

Figure 10: I-V characteristics of SiC MESFET with L_g = 8 µm, L_{sg} = 1µm, L_{gd} =2 µm and W_g = 3000 µm for gate-source voltage (V_{GS}) of 2V with step offset -4V (V_{GS} = -4V, -2V, 0V, 2V, 4V, 6V, 8V and 10V)

Figure 10 shows the I-V characteristics of a fabricated SiC MESFET with off-set gate structure, where the gate length (L_g), separation length between source-gate (L_{sg}) and separation length between gate-drain (L_{gd}) were considered in the order of 8µm, 1 µm and 2µm respectively and device width (W_g) of 3000µm. The maximum dc drain-source current is obtained in the order of ≈13.2mA, which clearly shows linear and non-linear properties for the drain-source voltage (V_{DS}) of 0.5V and 5V respectively. The drain-source current increases at the gate-source voltage (V_{GS}) swing from -4V to +10V. The transconductance has been found in the order of 9mS. The threshold voltage has been estimated in the range of -4V to -5V, which correctly implies the device behavior as a depletion type SiC based MESFET. The threshold shifts obtained from the I-V characteristics is obtained from the effect of drain-induced-barrier-lowering (DIBL). The

Dr. Somnath Chattopadhyay
CSU Northridge, 18111 Nordhoff St. Northridge, CA 91330
somnath.chattopadhyay@csun.edu
1-818-677-7197

pinch-off voltage is in the order of 3V, which agrees well with the active channel depth, having a theoretical pinch off voltage of abuot 4V. The discrepancy can be explained by the DIBL effect.

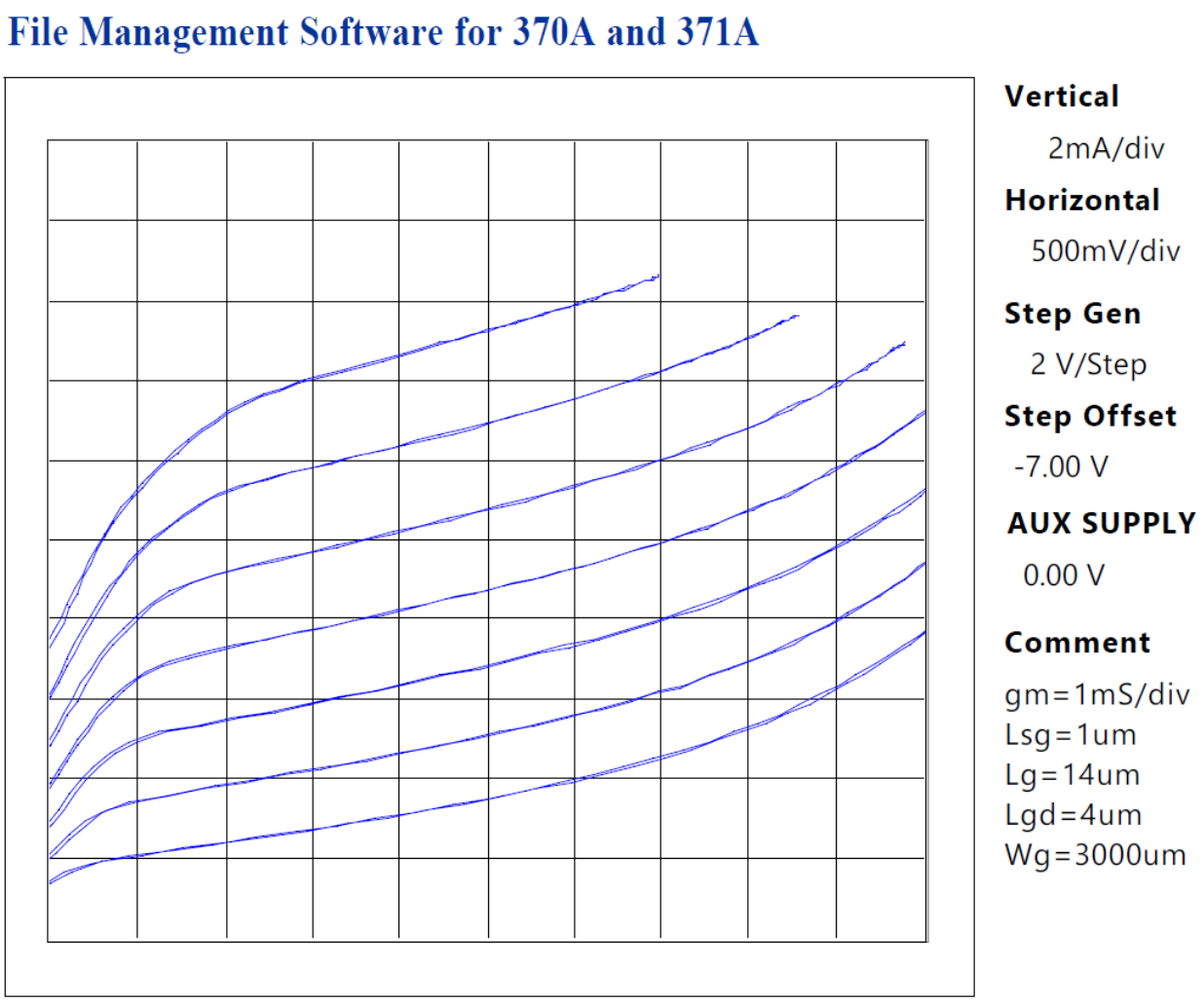

Figure 11: I-V characteristics of SiC MESFET with L_g = 14 µm, L_{sg} = 1µm, L_{gd} =4 µm and W_g = 3000 µm for gate-source voltage (V_{GS}) of 2V with step offset -7V

Figure 11 shows the plot of I-V characteristics generated from Tektronix 370A curve tracer. The drain-source current versus drain-source voltage plot displays the I-V characteristics of fabricated SiC MESFET with the gate length (L_g) of 14µm, separation length between source-gate (L_{sg}) of 1 µm, separation length between gate-drain (L_{gd}) of 4µm and device width (W_g) of 3000µm. The maximum drain-source dc current of ≈ 16.2mA clearly shows linear and non-linear properties up to drain-source voltage (V_{DS}) of 0.5V and 5V respectively. The drain current increases with response of increase of the gate-source voltage (V_{GS}) from -7V to +3.5V. The

threshold voltage has been found in the range of -4V to -5V, which confirm the device behaving as Normally-ON SiC based MESFET. The pinch-off voltage is on the order of 3V.

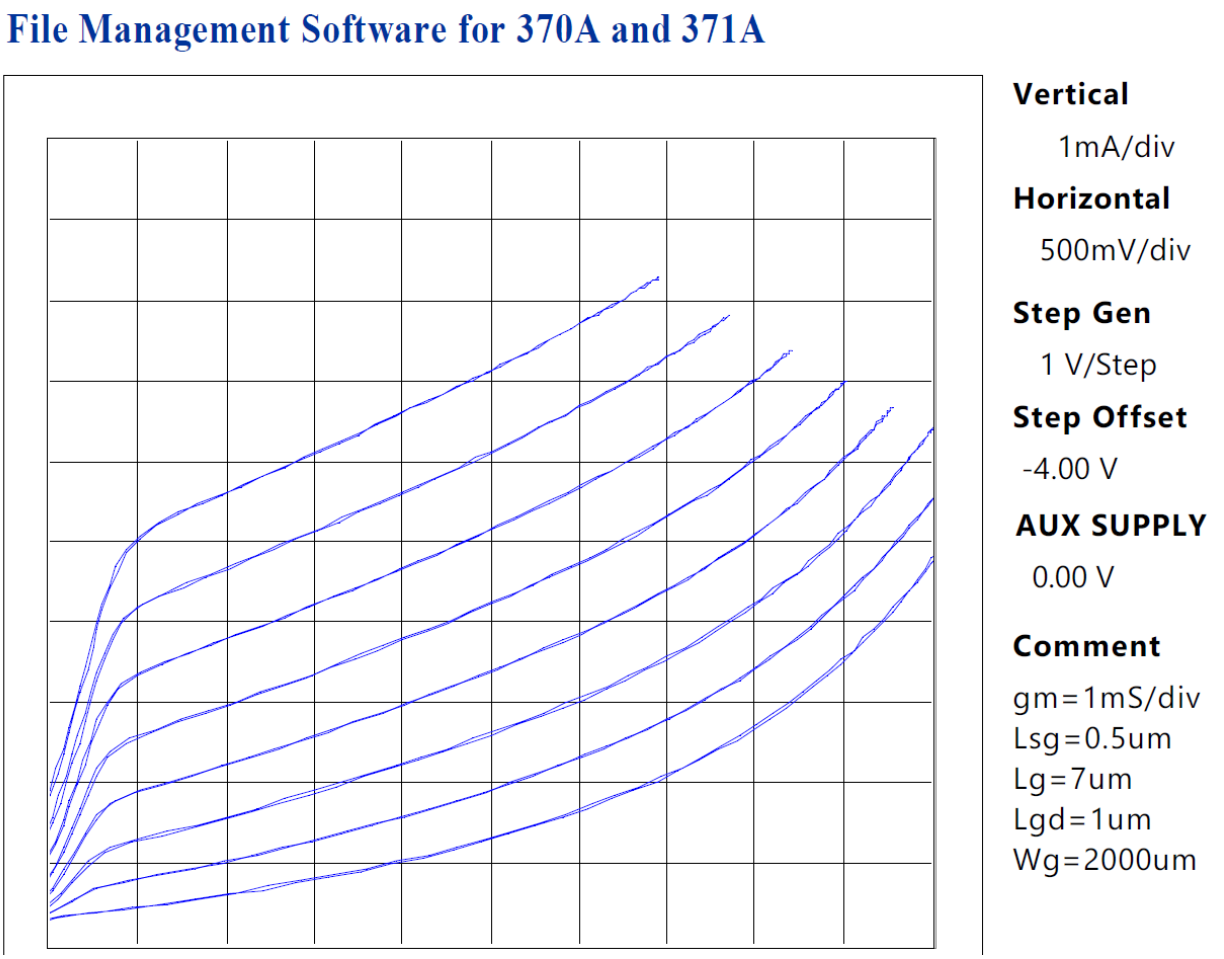

Figure 12: I-V characteristics of SiC MESFET with L_g = 7 µm, L_{sg} = 0.5µm, L_{gd} =1 µm and W_g = 2000 µm for gate-source voltage (V_{GS}) of 1V/step with step offset -4V

Figure 12 shows the I-V characteristics of fabricated SiC MESFET with gate length (L_g) of 7µm, separation length between source-gate (L_{sg}) of 0.5µm, separation length between gate-drain (L_{gd}) of 1µm and device width (W_g) of 2000µm. The maximum drain-source dc current of ≈ 9.3mA at drain-source voltage (V_{DS}) of 3.5V clearly presents the linear and non-linear properties at the drain-source voltage (V_{DS}) of 0.5V and 5V respectively. The maximum drain-source dc current of ≈ 9.3mA at the drain-source voltage (V_{DS}) of 3.5V is low compared to the previous devices exhibited in Figure 8 and 9, because of the ratio of device width and gate length. The drain-source current increases when gate-source voltage (V_{GS}) increases from -4V to +3.0V for 1V/step increment. The threshold voltage has been found on the order of -4V, which

Dr. Somnath Chattopadhyay
CSU Northridge, 18111 Nordhoff St. Northridge, CA 91330
somnath.chattopadhyay@csun.edu
1-818-677-7197

corresponds to the depletion type SiC based MESFET. The pinch-off voltage is obtained in the order of 3.0V, which agrees well with the other devices.

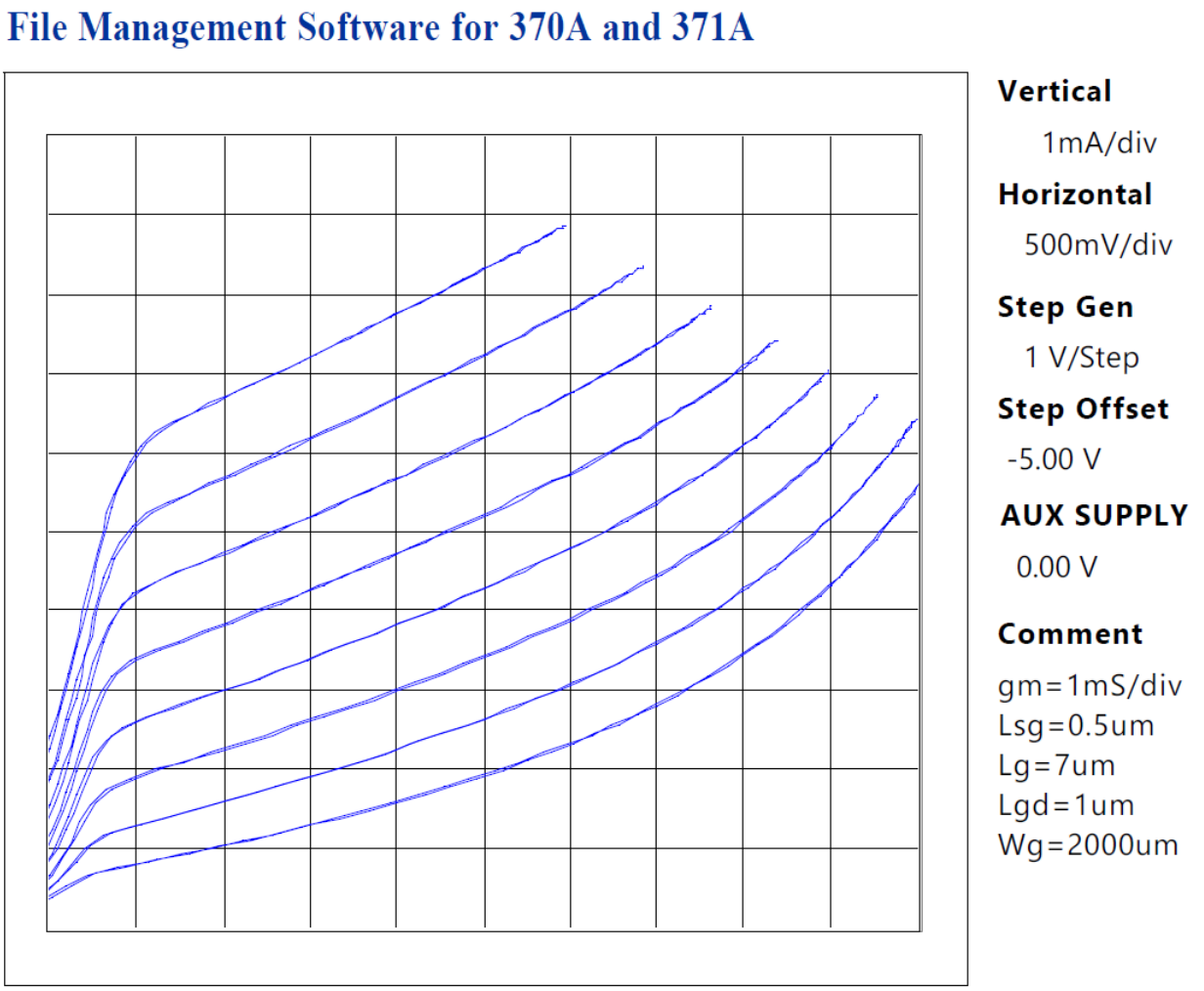

Figure 13: I-V characteristics of SiC MESFET with L_g = 7 µm, L_{sg} = 0.5µm, L_{gd} =1 µm and W_g = 2000 µm for gate-source voltage (V_{GS}) of 1V/step with step offset -4V

Figure 13 presents the I-V characteristics of fabricated SiC MESFET with gate length (L_g) of 7µm, separation length between source-gate (L_{sg}) of 0.5µm, separation length between gate-drain (L_{gd}) of 1µm and device width (W_g) of 2000µm and this plot has been extracted from Tektronix 370A curve tracer. The maximum drain-source dc current of ≈ 9.8mA at drain-source voltage (V_{DS}) of 3.0V clearly presents linear and non-linear properties for drain-source voltage (V_{DS}) of 0.5V and 5V respectively. The drain-source current increases when the gate-source potential (V_{GS}) changes from -5V to +2V. The threshold voltage has been obtained in order of -4V, which

Dr. Somnath Chattopadhyay
CSU Northridge, 18111 Nordhoff St. Northridge, CA 91330
somnath.chattopadhyay@csun.edu
1-818-677-7197

is a reasonable typical value for a normally-on SiC based MESFET. The pinch-off voltage is on the order of 3V.

All fabricated SiC MESFET device were exposed to 365nm UV light and the increase of drain current has been initially observed. However, the drain current remains same after the next successive UV exposure. The constant drain current concludes that large number of defects serving as recombination center captures the photogenerated carrier produced in the Schottky junction. I-V characteristics presented in above figures show the effects of drain-induced-barrier-lowering (DIBL). The DIBL effect is an electrostatic effect that can change the channel from a state of pinch-off to conduction and result in a substantial leakage current. DIBL also shifts the threshold voltage and renders the gate ineffective in controlling the channel. In the transition of linear to non-linear regimes of I-V characteristics, it has been observed that the gate control has been lost in the saturation regions. Another reason for DIBL can be attributed to contamination and defects generated by the fabrication process causing surface leakage currents. Several studies have reported the DIBL effect in GaAs and silicon on insulator MESFETs. However, to date no similar results for SiC MESFET have been reported.

SiC MESFETs are typically designed for high power and high frequency applications, and as such, will have short gate length, and are subject to large drain bias voltage, both of which will enhance the undesirable DIBL effect. In order to improve the high frequency performance, short gate length is preferred, and consequently, thinner channel layer should be selected to maintain a large gate length (Lg)/active channel depth (a) ratio and reduce the DIBL effect. This necessitates a higher channel doping for our fabricated device in order to obtain high output power density. Therefore, the DIBL effect has been enhanced by higher channel doping. However, the high channel concentration, thin active channel depth, geometrical pattern of gate and contamination and process induced defects is the source of DIBL effect of our device. Further studies of this and future fabricated devices will require more sophisticated analysis via extensive use of AFM, SEM and Augerscope, in order to extract the most valuable data from the samples.

(viii) Conclusion: This research work to develop the optically triggered SiC MESFET has been extremely challenging, on many levels. This is a most pioneering device design in terms of device structure, process development, potential optical quantum efficiency, material properties and device failure analysis, etc. The entire process development for optically triggered SiC MESFET has deviated from conventional SiC MESFET device fabrication, significantly. In order to work with transparent high band-gap materials such as SiC for device research and development, updated characterization tools such as AFM, Augerscope and SEM are needed to study the materials properties involved in the process steps, monitoring different materials' etching layers, etching rate and etching damage, doping dimensions and junction depth, and other failure analysis for material and device levels. The SiC wafer is transparent like glass. In order to perform multiple photolithography process steps with flexibility and accuracy, a better more modern system than the early 1980's era Karl Süss MA 56 is needed.

The older machine has a poor optical system compared to newer machines which makes contrast visibility with feeble alignment marks on transparent substrates very difficult. See Figure 14 and Figure 15 for illustration of this issue. Additionally, newer machines which are designed for the research lab, are more flexible to handle the various wafer sizes, or even wafer chips, unlike the Karl Süss MA 56, which was originally designed exclusively for 100mm silicon wafers. A retrofit adapter was designed, fabricated and installed to allow processing of 76mm wafers. In this present work, in order to improve the visibility of the alignment marks, the wafer was processed for backside nickel metallization each time an alignment step was planned. In cases where there was some alignment failure or other process problem which required the alignment step to be repeated, often the wafer back side had to be re-coated with nickel. At least a total of 14 back side depositions were performed in order to complete the 6 mask steps.

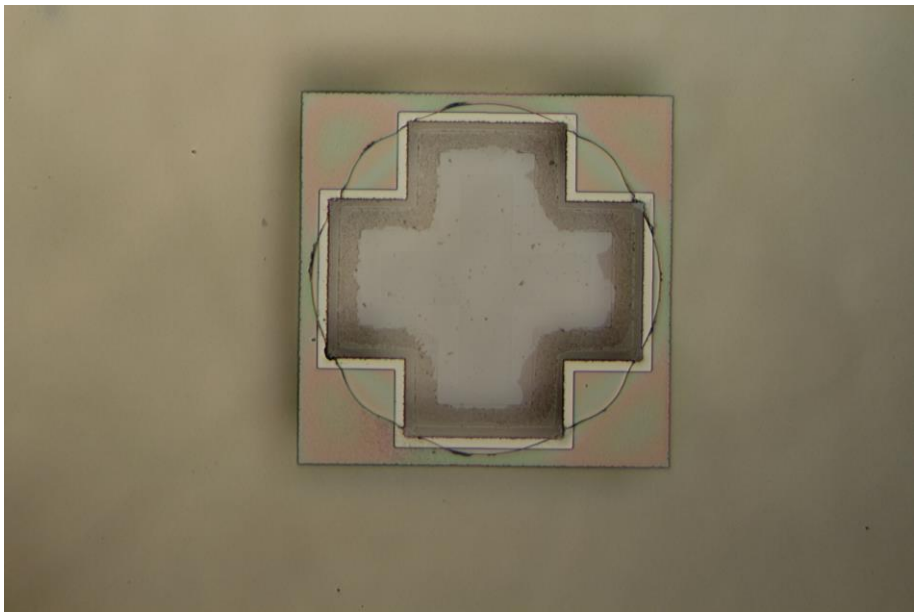

Figure 14: Typical view of a good/clear alignment mark step which was relatively easy to align to. Note that the inner pattern and the outer pattern (with uniform light colored gap around entire circumference) is clear. Uniformity of the light colored gap is indicative of a good alignment.

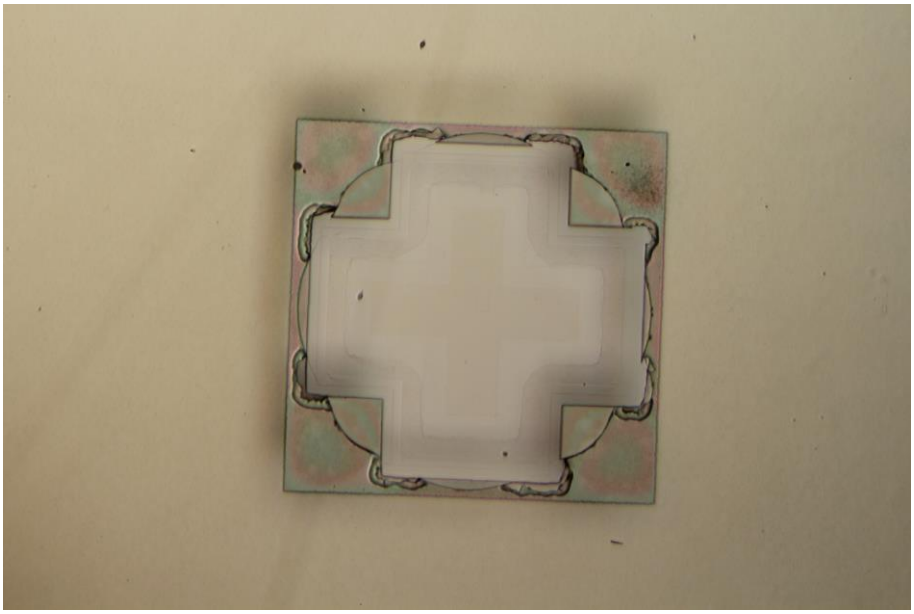

Figure 15: Typical view of a feeble alignment mark where the aligning step was extra difficult. Note the outer pattern is aligned to the very faint inner pattern.

However, the extracted result of SiC MESFET device with 1um gate length clearly indicates the I-V characteristics with linear and non-linear regimes with drain-induced-barrier lowering due to short channeling effects. The low breakdown voltage shows significant contamination and process induced defects due to several fabrication process stresses, which could have been minimized, if the proper characterization tools were available. However, it is remarkable to note that the researchers were able to bring an effective success from the first processed wafer by their experimental knowledge and hands-on-experience of practical device fabrication and the solutions of many critical issues related to the device electrical isolation, alternative method of method of materials' etching, critical photolithography process for SiC wafers, etc. Lastly, it can be concluded that this is a most pioneering research work for the first time development of an optically triggered SiC MESFET, indicating the great potential and competence for successful development of other wide band-gap MESFETs, optically triggered MESFETs and HEMT devices.