A 205GHz Amplifier in 90nm CMOS Technology

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Abstract: *This paper presents a 205GHz amplifier drawing 43.4mA from a 0.9V power supply with 10.5dB power gain, P_{sat} of -1.6dBm, and $P_{1dB} \approx$ -5.8dBm in a standard 90nm CMOS process. Moreover, the design employs internal (layout-based) /external (using passive embedding around the transistor) neutralization techniques for improving performance and yield of the overall system while canceling the effect of internal parasitic capacitors. The fabricated amplifier has the highest operation frequency among all reported amplifiers in 90nm and greater CMOS technologies.*

Keywords: Amplifier, neutralization, parasitic, P_{sat}, P_{1dB}.

Introduction

Millimeter-wave and sub-mm-wave (THz band) ranges offer many considerable applications, such as chip-to-chip communication with extremely high bandwidth, vehicular radar, and medical imaging [1]-[5]. According to ITRS prediction, by scaling down the dimensions of CMOS transistors, $f_{max\ and}$ $f_{T\ should}$ benefit [6]. However, recent studies based on the measurement data demonstrate the f_{max} is almost constant by CMOS scaling [7].

Aside from this potential, CMOS processes offer other advantages, such as low-cost, reliability, and mixed-mode analog/digital chips, intensifying its usage in the mm-wave band [5]. CMOS has several disadvantages at the higher frequency range with the worst case scenario happening when the device operates near its f_{max}. This is chiefly due to maximum achievable gain (G_{acc}) being lower than required [5]. For instance, a systematic methodology with the aim of operating CMOS near its f_{max} is reported in [2]. In this paper, two neutralization techniques, internal and external approaches, have been implemented to achieve higher power gain (boosting G_{acc} to near G_{max}) while the circuit operates near the f_{max}. The transistors' *Round-Table* structure [8] has been chosen for boosting the f_{max} (increasing Mason's invariant function (U) and G_{acc}). This technique is briefly discussed and another ameliorative technique for boosting the performance of transistors is external neutralization. The rest of the paper has been organized as follows: section II covers the utilized techniques in this design; Section III is devoted to designing a mm-wave amplifier based on the mentioned techniques in section II.

mm-Wave Device Optimization

Layout-Based Neutralization

So much research has been conducted on the improvement of layout to reduce parasitic [9]. Since U is nearly constant under any 4-port linear, lossless, and reciprocal embedding, this function has been chosen as a Figure of Merit (*FoM*) for comparing the effect of parasitics and the successfulness of the proposed layout. As shown in Figure 1., U is more dependent on C_{gd} compare to C_{gs}. Therefore, optimization is focused on the aim of lowering C_{gd}. A round table structure is used in reducing the value of undesired parasitics realizing multi path connections between unit cells.

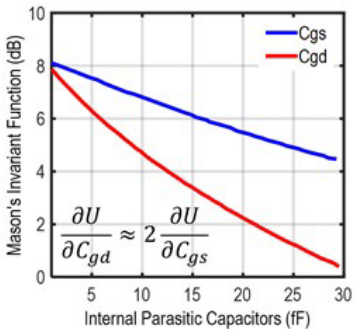

Figure 1. U's sensitivity to dominant internal parasitic capacitors

Figure 2. shows the simulated G_{acc}, G_{max}, and U of a *round-table* NMOS with W=48μm. While f_T remains almost constant (around 106GHz), the simulated f_{max} is boosted to near 300GHz as shown in Fig. 2. This achievement enables the usage of the neutralized transistors in the band of interest. As shown in Figure 2. , Mason's invariant function is improved around 5.8dB, proving the feasibility of the proposed structure. The dominant internal parasitic capacitors, C_{gs}/C_{gd}, changed from 42.85/25.57fF to 68.48/20.61fF, respectively. As calculations show, C_{gs} is increased as a price of using this structure. As a result, the practical solution presented in this letter is employing external cancellation (resonating) this parasitic capacitance (C_{gs}) using CPWs-based inductors.

External Neutralization

As shown in Figure 2. , there is a significant difference between maximum achievable gain (G_{acc}) and G_{max}. This has fueled many circuit innovations with the aim of boosting G_{acc} to reach G_{max}. As reported in [5], the technique boosts up G_{acc} with the aid of passive embedding around the device in order to control the signal conditions of the transistor Figure 3. shows a simplified schematic of each stage of the proposed amplifier [9].

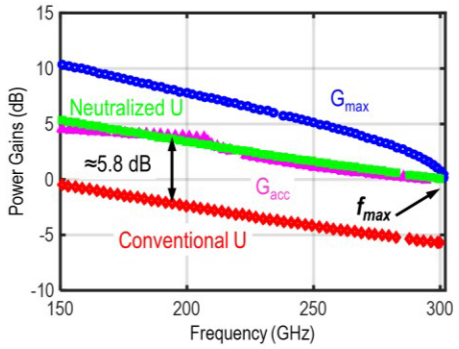

Figure 2. Simulated maximum achievable gain (G_{acc}), Mason's invariant function (U) and maximum available gain (G_{max}) with conventional and *round-table* NMOS layouts of a W=48μm transistor in a 90nm CMOS process.

In order to tune A and □ and optimize them (A_{opt} and □$_{opt}$), T_3 is inserted between gate and drain of the transistor. Since the gate of a CMOS transistor has high loss in ultra- high frequencies, it can be compensated by injecting part of the generated output power of each stage (transistor) to its input port (gate) utilizing T_3 in conjunction with T_1 and T_2.

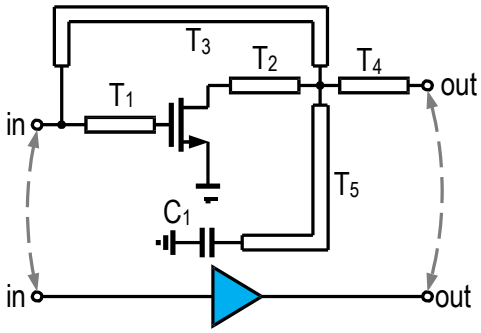

Figure 3. Simplified schematic of one stage of the proposed amplifier.

A 205GHz Amplifier

Figure 4. is the simplified schematic of the designed amplifier, which is constructed from 5 stages as shown in Figure 3. Two parallel *round-table* transistors with a total W=48μm with 4 fingers per unit cell are utilized with the aim of increasing the operation frequency of the proposed amplifier. T_3 and T_5 are designed to have around λ/2 and λ/3 electrical lengths near the operation frequency. Moreover, the inter-stage matching networks per stage are constructed from T_4, T_5, and C_1.

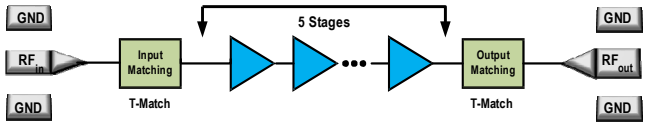

Figure 4. Simplified schematic of the proposed 5 stage 205GHz amplifier.

The quality factor of implemented coplanar waveguide-based transmission lines (inductors) are around 14 at 205GHz. Simulations show 2.6dB/stage power gain, which is almost 8dB more power gain compared with conventional amplifiers with 1dB/stage operating with similar operation frequencies of the proposed amplifier. Using the systematic methodology in [2], the simulated signal conditions, A and □, in the proposed amplifier are 1.68 and 153°, respectively.

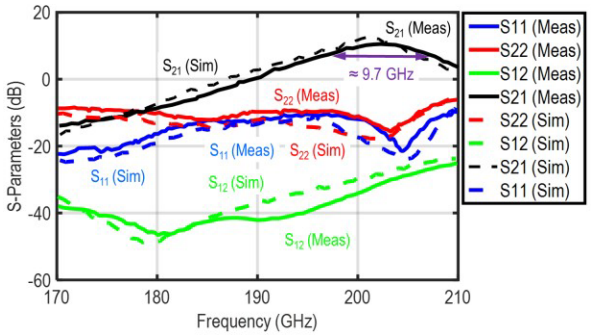

Figure 5. Simulated/Measured small-signal *S-parameters* of 205GHz amplifier.

These values are very close to optimized signal conditions, A_{opt}=1.69 and □$_{opt}$=145°. This guaranteed that G_{acc} of the transistor is boosted up to almost G_{max}, excluding the effects of passive elements losses. Fig. 5 plots the simulated/measured *S-parameters* of the fabricated 205GHz amplifier.

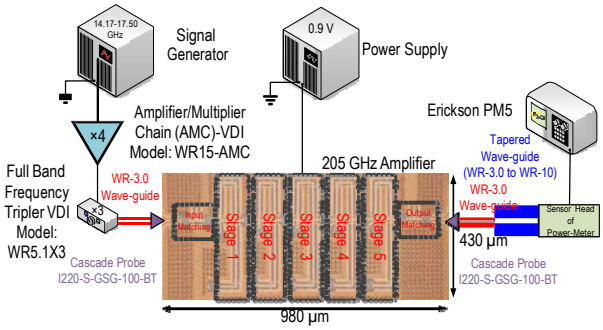

Figure 6. Die photo of the proposed 205GHz amplifier along with test setup for power measurement.

Table I: Comparison with other state of the art work

Reference	This Work	[9]	[10]	[11]	[12]	[13]	[14]
Tech. (nm)	90 CMOS	65 CMOS	40 CMOS	65 CMOS	250 InP (HBT)	50 GaAs MHEMT	250 InP DHBT
Freq. (GHz)	205	260	210	190	301	183	210-315
Gain (dB)	10.5	9.2	10.5	16.3	13.4	19	12.5
P_{Diss} (mW)	39.1	27.6	42.3	33.4	-	-	-
P_{sat} (dBm)	-1.6	-3.9	-3.2	-	13.5	-	5.5
P_{1dB} (dBm)	-5.8	-5.5	-7.2	-	13.2	-	-
V_{DD} (V)	0.9	0.8	0.8	2	4.5	-	-
f_{max}(GHz)	300	350	275	-	700	-	600

Fig. 6 shows the equipment setup for measurements. The active area of the fabricated chip excluding pads is around 0.42mm^2. The comparison with other state-of-arts is listed in Table I.

Conclusion

Millimeter wave communications holds the future of high data rate and high bandwidth based applications. Hence, a 205 GHz amplifier has been implemented and fabricated in 90nm CMOS technology. The proposed amplifier attained a gain of 10.5 dB whilst consuming a dc power consumption of 39.1 mW. Such a high standard of performance is realized by employing external neutralization techniques such as transmission line theory and power compensation techniques. This enabled to boost G_{acc} to almost reach G_{max}. The proposed CMOS mm-wave amplifier demonstrates the potential of employing CMOS technology at such high frequencies.

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