STAR Performance with SPEAR
(Signal Processing Electronic Attack RFIC)

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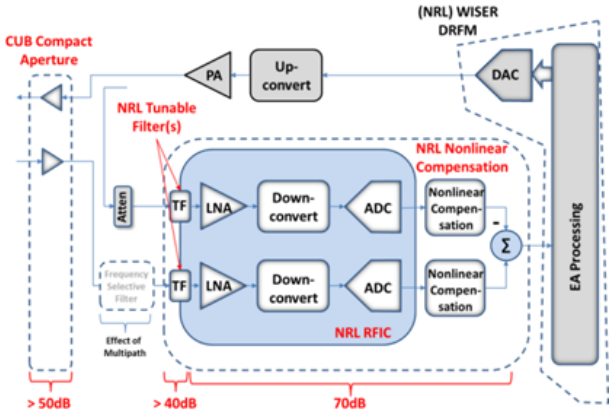

Figure 1: The Signal Processing Electronic Attack RFIC (SPEAR) system.

Abstract: *The Signal Processing Electronic Attack RFIC (SPEAR) is a simultaneous transmit and receive (STAR) system capable of STAR operation in the presence of 1 kW EIRP power, independently of the choice of transmitter in use. The paper reports on the status of the SPEAR project that started 2 years ago with the support of the Office of Naval Research, Code 31. Preliminary measurements based on a COTS-based receiver prototype will be presented. To the authors' knowledge, the measured results from the prototype already demonstrate state-of-the-art STAR performance and provide a solid base for the integration of the complete system.*

Keywords: Simultaneous Transmit And Receive; STAR; Full Duplex; Digital Signal Processing; DSP; Transmitter; Receiver; Multipath.

Full duplex challenges

Simultaneous transmit and receive (STAR) systems – or full duplex systems as they are also widely known – have received strong attention from researchers and commercial interests. Indeed, full duplex systems are inherently doubling the system's channel capacity – a fact that wireless service providers find extremely attractive when considering a very expensive and scarce spectrum. Full duplex, relatively narrow band (~ 100 MHz) communication systems have been demonstrated on-chip at mm-wave frequencies [1]. Broad bandwidth (>> 100 MHz) and large tunability are challenges that military systems have to face in additions to the basic issue of isolation between transmitter and receiver chains. Further, EW applications must be capable of discriminating any type of incoming signal in the presence of self-generated high power interferers.

SPEAR is an innovative approach to the full duplex challenge that meets the high demands of military systems. The program the SPEAR program is funded by the Office of Naval Research, Code 31, and kicked off 2 years ago [2]. This abstract will highlight some key results and provide an update of the status of the program.

The SPEAR System

The SPEAR system is sketched out in Fig. 1 and consists of 3 key sub-systems: (1) high performance antennas; (2) RFIC system-on-a-chip; and (3) digital signal processing. A high performance, multi-layer board will host the RFIC die and interface with the DSP sub-system. The design effort also includes a transmitter composed of off-the-shelf components because the SPEAR system is agnostic to the type of transmitter in use. The ultimate goal of the SPEAR program is to demonstrate the operational use of the receiver system beyond a lab environment.

The SPEAR dual-receiver is designed to tune a 1 GHz bandwidth over the 0.5-45.0 GHz range with 4 overlapping channels. Each channel shares the same architecture in order to maximize on-chip circuit reuse. High isolation between transmitter and receiver chains (~ 120 dB) is achieved by enhancing the isolation of the system's constituents. The antennas, designed by the University of Colorado, Boulder, are discussed separately at this Conference and contribute with 50 dB of isolation or more.

The SPEAR prototype receiver

A 2.0-7.0 GHz SPEAR receiver has been assembled after careful selection of the off-the-shelf components and it is shown in Fig. 2. The main objective of the prototype is to guarantee high linearity with a IMD >> 50 dB at full power at the input of the receiver. The RX chains consist of an up-conversion to 23.5 GHz followed by a down-conversion to

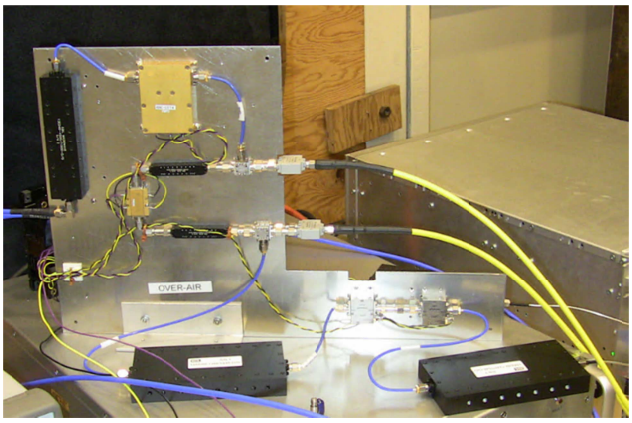

Figure 2: The SPEAR receiver prototype. The other channel receiver is assembled on the other side of the metal plate.

a fixed 2 GHz IF frequency. Careful frequency planning has been performed to minimize harmonics within the 1 GHz bandwidth of interest. In addition, NRL Code 6851 has designed and manufactured a microstrip absorptive low pass filter up to 100 GHz and tested up to 67 GHz. This filter is inserted after a standard comb-line resonator-based commercial filter centered at 23.5 GHz which shapes up the spectrum before the second conversion. The combination of the 2 filters yields >> 50 dB of non-reflective suppression. Additional filtering is provided before an analog-to-digital converter digitizes the analog signal. DSP algorithms have been developed at NRL Code 5734, along with a suitable Graphic User Interface. The algorithms will not be discussed at this venue.

Testing of the prototype receiver has been performed at NRL under diverse conditions. Fig. 3 shows the results achieved with adaptive cancellation in the presence of multi-paths in a controlled environment: the SPEAR system demonstrates 120 dB cancellation and it is able to detect both a communication signal and a chirp signal within the band-width of interest.

SPEAR Integration

The prototype results demonstrate that the NRL approach is capable of delivering STAR performance. The DSP algorithm shows that cancellation can be achieved under challenging conditions, including multi-path and high harmonic generation by the transmitter. The prototype is an important project milestone which gives confidence in the NRL approach. However, some limitations are inherent with the limited COTS choice. For example, the SPEAR prototype cannot adjust to amplitude variations of the signals of interest nor has the target 1 GHz bandwidth been enabled by the off-the-shelf ADC. The next steps are aiming at designing and demonstrating SPEAR performance under all conditions.

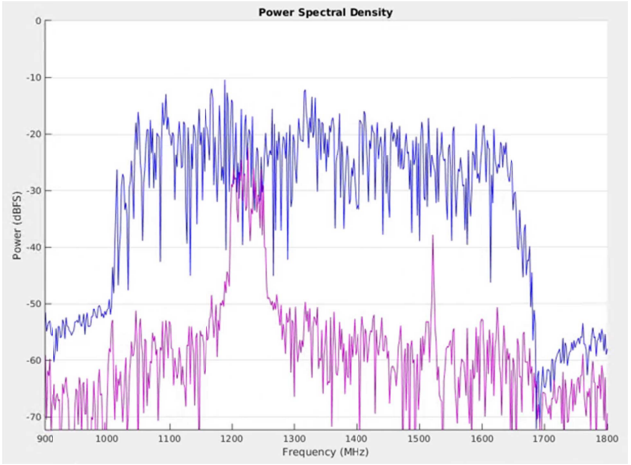

Figure 3: Time snapshot results with adaptive cancellation: a communication signal and a chirp signal (in purple) are clearly detected despite the simultaneous transmission (in blue) over a 700 MHz bandwidth.

NRL has been leading a RFIC design effort to manufacture a complete system-on-a-chip that replaces the whole off-the-shelf prototype with a Silicon based integrated circuit. The die will be taped out in November 2016 as part of a scheduled MOSIS multi-project wafer ITAR run in Global Foundry 8HP SiGe BiCMOS technology. The die will include (i) a complete 2.0 – 7.0 GHz dual-channel receiver chain; (ii) gain control; (iii) an on-chip 2 GHz filter; (iv) an analog-to-digital converter; and (v) a serial-to-parallel interface. The die dimensions are about 6 x 7 $(mm)^2$ including the ADC. The RF chains duplicate the same up/down conversion architecture implemented by the prototype with some notable differences. A low noise amplifier receives the single-ended signal from the antenna and delivers it differentially to the first mixer stage over the complete 2.0 – 7.0 GHz channel range. The LNA's gain is fixed to facilitate the trade-off between noise figure and linearity even under the presence of a strong interferer along with the signal of interest.

The first mixer stage includes (i) a on-chip balun to drive the differential LO driver; (ii) a micro-mixer to address the linearity performance requirements; (iii) variable gain high-IF amplifiers at fixed 23.5 GHz with 1 GHz bandwidth; and (iv) an on-chip balun to drive the off-chip IF filter. The external 23.5 GHz filter performs a similar task as in the prototype case. However, the design has been modified to be fabricated as a surface mounted component by an external vendor.

A second mixer stage receives the filtered signal trough an on-chip balun and feeds a Gilbert cell mixer. The mixer down-converts the signal to 2.0 GHz. The IF signal is boosted by a series of variable gain amplifiers. A 2 GHz anti-aliasing on-chip differential filter is embedded in the amplifier chain to shape the signal before the ADC conversion. The filter makes use of lumped components to avoid introducing additional harmonics in the proximity of the ADC. The area is approximately 1 x 1 $(mm)^2$.

The on-chip time-interleaved analog-to-digital converter is designed by Ohio State University and features 12 bits and delivers 2.7 Gsps. A board on which the chip is flipped is also being designed to interface the receiver with a commercial FPGA. Initial characterization of the SPEAR card is scheduled in late Spring 2017.

Conclusions

This abstract reports the state-of-the-art STAR results of the prototype SPEAR receiver and describes the upcoming integrated system and its high performance card.

Acknowledgment

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