



AFRL-RY-WP-TR-2018-0012

**FREQUENCY DISCRIMINATOR BASED PHASED NOISE
FILTER (PNF) FOR ULTRA-CLEAN LOCAL
OSCILLATOR (LO)/CLOCK, EVOLVING AT
COMMERCIAL TIMESCALES**

Jane Gu

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**APRIL 2018
Final Report**

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REPORT DOCUMENTATION PAGE				Form Approved OMB No. 0704-0188	
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1. REPORT DATE (DD-MM-YY) April 2018		2. REPORT TYPE Final		3. DATES COVERED (From - To) 11 March 2014 – 11 December 2017	
4. TITLE AND SUBTITLE FREQUENCY DISCRIMINATOR BASED PHASED NOISE FILTER (PNF) FOR ULTRA-CLEAN LOCAL OSCILLATOR (LO)/CLOCK, EVOLVING AT COMMERCIAL TIMESCALES				5a. CONTRACT NUMBER FA8650-14-1-7415	
				5b. GRANT NUMBER	
				5c. PROGRAM ELEMENT NUMBER 61101E/62716E	
6. AUTHOR(S) Jane Gu				5d. PROJECT NUMBER 1000	
				5e. TASK NUMBER N/A	
				5f. WORK UNIT NUMBER Y0YS	
7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES) University of California, Davis 1850 Research Park Drive, Suite 300 Davis, CA 95618				8. PERFORMING ORGANIZATION REPORT NUMBER	
9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES) Air Force Research Laboratory Sensors Directorate Wright-Patterson Air Force Base, OH 45433-7320 Air Force Materiel Command United States Air Force				10. SPONSORING/MONITORING AGENCY ACRONYM(S) AFRL/Rydi	
				11. SPONSORING/MONITORING AGENCY REPORT NUMBER(S) AFRL-RY-WP-TR-2018-0012	
12. DISTRIBUTION/AVAILABILITY STATEMENT Approved for public release; distribution is unlimited.					
13. SUPPLEMENTARY NOTES This report is the result of contracted fundamental research deemed exempt from public affairs security and policy review in accordance with SAF/AQR memorandum dated 10 Dec 08 and AFRL/CA policy clarification memorandum dated 16 Jan 09. This material is based on research sponsored by Air Force Research Laboratory (AFRL) and the Defense Advanced Research Agency (DARPA) under agreement number FA8650-14-1-7415. The U.S. Government is authorized to reproduce and distribute reprints for Governmental purposes notwithstanding any copyright notation herein. The views and conclusions contained herein are those of the authors and should not be interpreted as necessarily representing the official policies of endorsements, either expressed or implied, of AFRL and DARPA or the U.S. Government. Report contains color.					
14. ABSTRACT University of California, Davis investigated a fully integratable phase noise filter (PNF) to achieve ultra-low noise across a wide band for common modules and array systems, which has the capability to evolve at commercial timescales. Different phase noise cancellation techniques have been investigated and realized in analog and digital domains. Two PNF categories were examined and developed: linear PNF and nonlinear PNF. Within each category, the university demonstrated different versions by continuously improving the phase noise.					
15. SUBJECT TERMS phase noise filter, linear, nonlinear, local oscillator					
16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT: SAR	18. NUMBER OF PAGES 70	19a. NAME OF RESPONSIBLE PERSON (Monitor) Tony Quach 19b. TELEPHONE NUMBER (Include Area Code) N/A
a. REPORT Unclassified	b. ABSTRACT Unclassified	c. THIS PAGE Unclassified			

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1. First Category: Linear Phased Noise Filter

1.1 1st Version Linear Phase Noise Filter

Local oscillator (LO) phase noise is critical for many electronic systems. It constrains the performance of the bit-error-rate (BER) and error vector magnitude (EVM) of the radio frequency (RF) system, resolution of the analog-to-digital converter (ADC)/digital-to-analog converter (DAC), and the detection dynamic range of the radar [1-4]. Therefore, the LO phase noise improvement technique is an active research topic and has been explored widely [5-20]. One research trend is to use new techniques in the frequency synthesizers or phase-locked loops (PLLs) to improve the phase noise [5-10]. However, this structure relies on a superior reference clock. Another option is to improve the phase noise by a general function unit [11-20]. This method uses a frequency discriminator (FD) to extract the phase noise and convert it to a voltage signal. It is used by feedback or feed-forward schemes to cancel the phase noise through a phase shifter. Different phase noise cancellation techniques have been investigated and realized in analog and digital domains.

1.1.1 Architecture

1. Phase Noise Cancellation in Analog Domain: In [12] and [13], the phase noise of the oscillator is extracted by a high quality factor (high-Q) resonator based FD and cancelled in the negative feedback loop by adjusting the phase of the oscillator in the analog domain, as shown in Figure 1(a). This approach achieves good phase noise, but the input LO bandwidth is quite limited by the high-Q resonator. For example, [12] demonstrates ultra-low phase noise of -141 dBc/Hz at 1 MHz offset for a 1.5 GHz clock, but with less than 5 MHz input LO bandwidth. Figure 1(b) shows another phase noise cancellation method used by a ring oscillator based PLL [11]. The phase noise is detected by an active delay line (DL) based FD and cancelled in the feed-forward scheme. The phase noise is -105 dBc/Hz at 1 MHz offset with a 5 GHz carrier, which is greatly constrained by the active DL. In addition, the feed-forward cancellation approach requires good matching between the main path and the cancellation path, which is challenging in the complex electronic systems.
2. Phase Noise Cancellation in Digital Domain: As shown in Figure 1(c), the LO phase noise is extracted by the FD and then cancelled by the digital signal processing in the baseband [20]. This method is inherently stable because it does not have any analog or RF feedback in the system. However, the ultimate LO phase noise performance is affected by the sampling clock jitter. [21] Shows another method to reduce the clock jitter for the ADC as shown in Figure 1(d). The jitter cancellation capability of this method is limited by the time-to-digital converter (TDC) resolution.

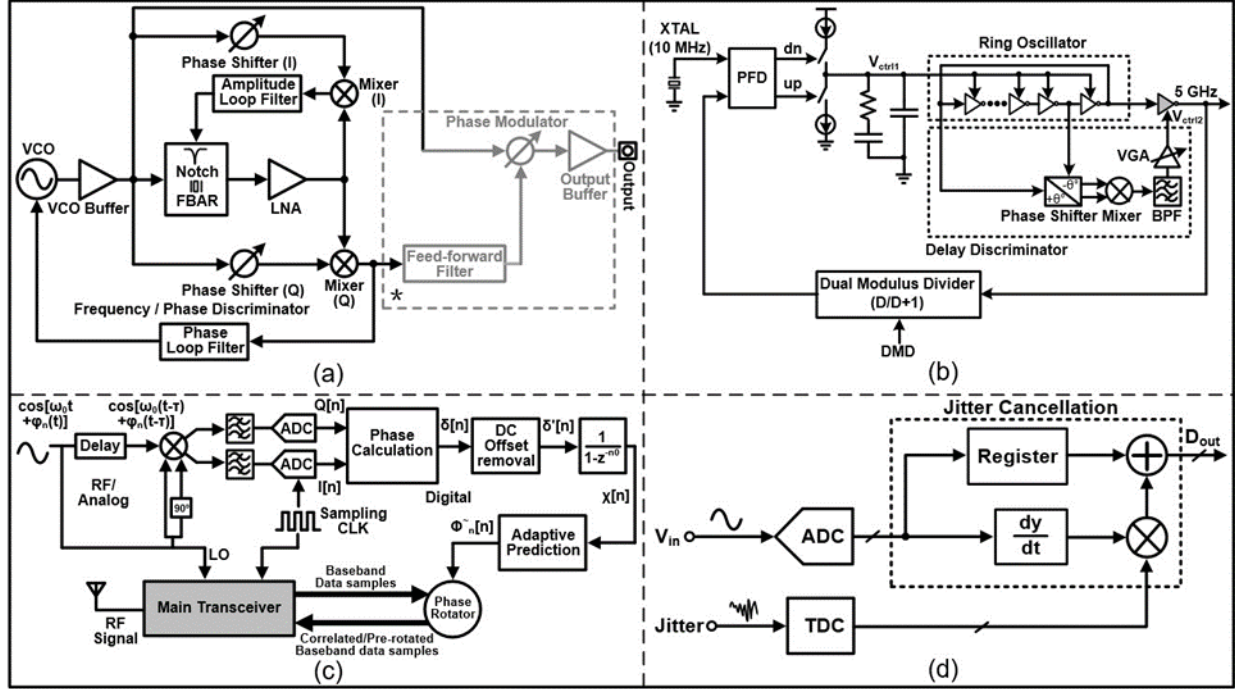


Figure 1: (a) Phase Noise Reduction System for the Oscillator in the Analog Domain [12], (b) Phase Noise Cancellation for the Ring Oscillator based PLL in the Analog Domain [11], (c) Phase Noise Cancellation for the Transceiver in the Digital Domain [20], and (d) Jitter Cancellation for the ADC in the Digital Domain [21]

To mitigate the issues of the existing phase noise cancellation techniques, we propose a passive DL based feedback type phase noise filter (PNF) to suppress the input clock phase noise in the analog domain [22]. It is enabled by the passive DL and phase detector (PD)/charge pump (CP) based FD.

Figure 2 shows the block diagram of the proposed PNF. The PNF consists of a voltage controlled phase shifter (VCPS), a divider, an FD and a baseband (BB) circuit. The 10 GHz input LO is converted to a 1.25 GHz signal by the divide-by-8 divider to alleviate the design challenges of the subsequent circuits. The FD converts the phase noise information into a low frequency voltage, which is further amplified and filtered by the analog baseband circuit to get the desired control voltage (V_{ctrl}). V_{ctrl} controls the VCPS in a negative feedback loop to generate the required phase shift to suppress the phase error caused by the phase noise. The suppression offset frequency range, f_1 - f_2 , is determined by the loop frequency response.

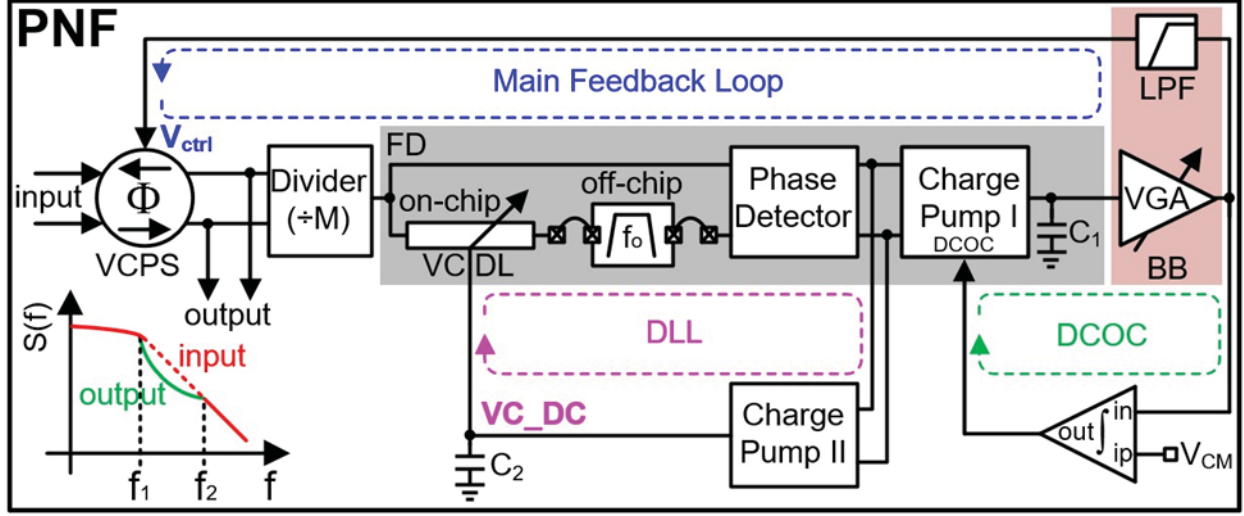


Figure 2: Block Diagram of the Proposed PNF

The FD is the key unit of the PNF because it determines the phase noise sensitivity, suppression bandwidth and input frequency range [27-29]. Figure 3 shows the simplified block diagram of the FD, which is composed of two parts: DL and phase extractor.

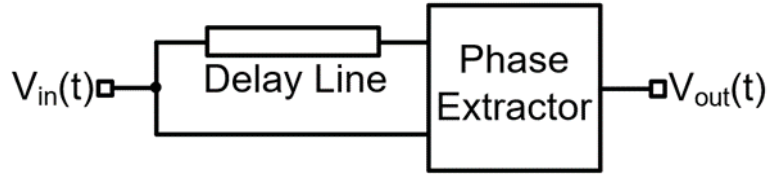


Figure 3: Block Diagram of the FD

The DL converts the absolute phase noise into relative timing jitter; the phase extractor detects the relative timing jitter and converts it to the voltage. The input LO with phase noise and its delayed counterpart can be represented as

$$V_{in}(t) = V_p \cos(2\pi f_{in}t + \phi_n \cos(2\pi f_m t)) \quad (1)$$

$$V_{in}(t - \tau) = V_p \cos(2\pi f_{in}(t - \tau) + \phi_n \cos(2\pi f_m(t - \tau))) \quad (2)$$

where V_p is the input signal amplitude, f_{in} is the input LO frequency, τ is the delay time of the DL. $\phi_n \cos(2\pi f_m t)$ represents the phase error caused by the phase noise with the maximum phase error ϕ_n at f_m offset frequency. The output voltage of the FD is approximated as

$$V_{out}(t) \approx 2\pi\tau \cdot K_{PE} \cdot \phi_n \cdot \sin(2\pi f_m(t - \tau/2)) \cdot f_m \quad (3)$$

where K_{PE} is the phase extractor gain in V/rad. The output voltage is proportional to the maximum phase error ϕ_n , which indicates the phase noise level of the input LO.

Based on (3), a large delay time leads to a large FD transfer gain, which helps achieve large phase noise suppression and good phase noise sensitivity. Delay time, phase noise and bandwidth are three important specifications to characterize a DL. Table 1 compares the performance of the passive DL, the high-Q resonator and the active DL. The high-Q resonator based DL achieves large delay time but with very small bandwidth due to the limited phase adjustability. The active DL achieves large bandwidth but with poor phase noise because of the active circuit's noise contribution. Therefore, we propose to use a passive on-chip voltage controlled DL (VCDL) cascaded with an off-chip surface acoustic wave (SAW) filter to achieve the balance of delay time, bandwidth and phase noise.

Table 1. Delay Line Performance Comparison

Delay Line Type	Passive Delay Line	High-Q Resonator	Active Delay Line
Delay Time	medium	large	medium
Phase Noise	good	good	poor
Bandwidth	medium	very small	large

The PD and CP (PD/CP) combination is adopted as the phase extractor in this design instead of a mixer, because PD/CP is insensitive to the amplitude noise and coupling noise due to the in-phase requirement for the input signals [29], [30]. In addition, a delay-locked loop (DLL) is adopted in the PD/CP type FD to automatically align the phase of the two input signals. In the mixer based designs, [11] adopts G_m -C polyphase filter, [27] uses phase adjustment loop and [12] need manual phase adjustment to ensure the quadrature phase requirement. The phase extractor implementation methods are summarized and compared in Table 2.

Table 2. Phase Extractor Method Comparison

Phase Extractor	PD/CP	Mixer
Input Phase Requirement	in-phase	quadrature-phase
Calibration	delay-locked loop	phase adjustment loop [27]
Coupling Noise	insensitive	sensitive
Amplitude Noise	insensitive	sensitive

Since the PNF deals with the phase noise, which is an ultra-small quantity by nature, any circuit mismatch or non-ideal factors may greatly deteriorate the phase noise extraction and cancellation. Therefore, a DLL and a direct current offset cancellation (DCOC) loop are embedded into the system to make the PNF calibrate automatically, thus making the PNF immune to the non-ideal factors.

1.1.2 Circuits

1.1.2.1 VCPS

VCPS is a key block in the PNF with the requirement of a large drivability. The conventional passive phase shifters are not preferred due to the large loss [31]. The active vector combining based approach is hard to achieve accurate gain control and fine phase adjustment [32]. To simplify the design and provide large drivability, an amplifier with cross-coupled pair is implemented as the VCPS as shown in Figure 4. The phase of the output signal is shifted by adjusting the resonant frequency of the tank, which is composed of an inductor, a 5-bit capacitor array, and a varactor. The phase of the tank impedance is expressed as

$$\phi(Z_{in}) = \arctan [R(1 - \omega^2 LC) / \omega L] \quad (4)$$

where L, C, and R are the parallel tank component values. At the center frequency, ω_c , the phase of the tank impedance is zero. If the tank capacitance is changed by $\pm\Delta C$, the phase shift is calculated as

$$\Delta\phi(Z_m) = \mp R \cdot \Delta C / \sqrt{LC} \quad (5)$$

Figure 5 (a) shows the phase response of the tank impedance in the frequency domain with different resonant frequencies by adjusting the capacitance. If the resonant frequency f_{reso} is larger than the center frequency f_c , the output signal phase will lead and vice versa. Figure 5(b) shows the VCPS output transient waveforms with different varactor control voltage V_{ctrl} , showing consistent results from the frequency domain analysis. Figure 6 depicts the phase shift versus the V_{ctrl} . The phase changes linearly in the range of 0.5-1 V, with the slope as the phase adjustability of the VCPS, named as K_{VCPS} .

The cross-coupled pair (M5 and M6) is used as a Q booster to enhance the parallel tank resistance and generate a large output [33]. Besides the large output, the phase shift is also enhanced based on (5) due to the large parallel resistance, thus leading to a large K_{VCPS} . However, the inserted cross-coupled pair may degrade the phase noise due to its own noise contribution. Figure 7 shows the VCPS phase adjustability and phase noise at 1 MHz offset versus the input frequency in two cases: with and without the Q booster. With the Q booster, the K_{VCPS} increases from 0.54 rad/V to 1.47 rad/V and the output amplitude is enhanced from 0.43 V to 1.52 V. The 2 dB phase noise degradation is negligible because the VCPS is not the main noise contributor in the PNF as will be discussed in Section 1.4.

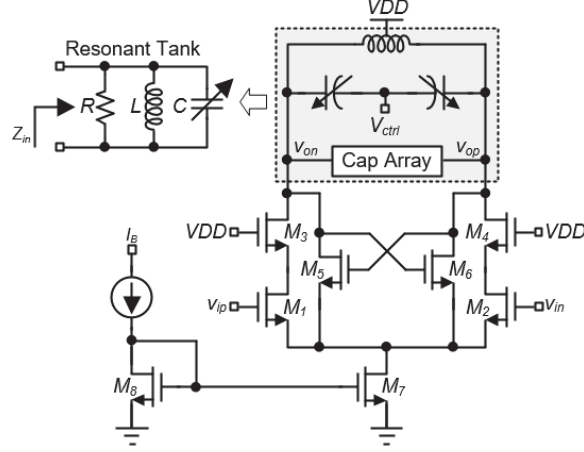


Figure 4: Schematic of the VCPS

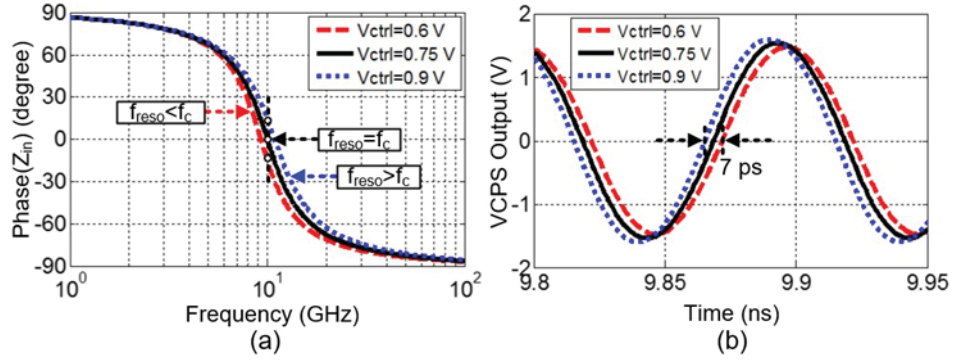


Figure 5: VCPS Phase Shift in the (a) Frequency Domain and (b) Time Domain

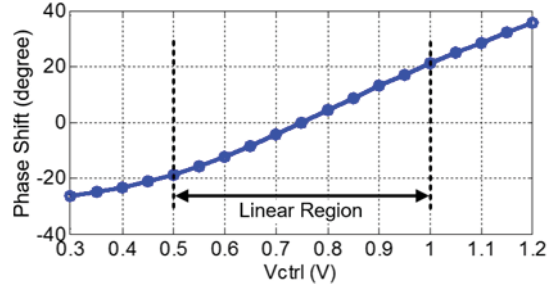


Figure 6: VCPS Phase Shift vs. the Varactor Control Voltage V_{ctrl}

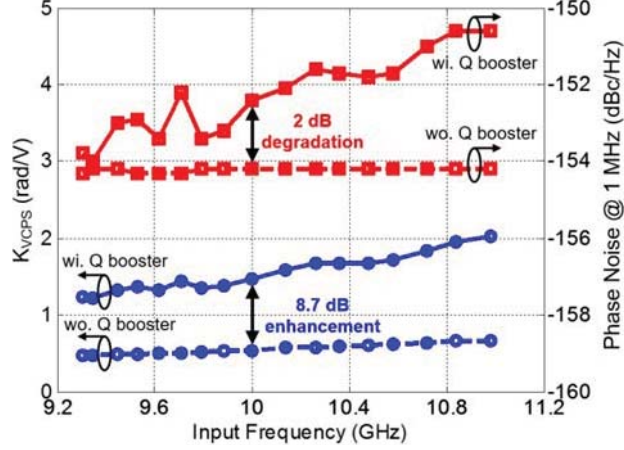


Figure 7: VCPS Phase Adjustability and Phase Noise at 1 MHz Offset vs. the Input Frequency with and without the Q Booster

1.1.2.2 DLL

The DLL is adopted to align the PD's input phase, which ensures that the phase error detected by the PD is only caused by the phase noise instead of the large dc component. Figure 8 shows the block diagram of the DLL. The on-chip VCDL is a four cascaded stages LC type transmission line [29]. The coarse and fine delay adjustment are realized by a 4-bit switchable capacitor array and a varactor, respectively. The frequency locking range of the VCDL continuously covers over 0.95-1.4 GHz, which corresponds to 0.71-1.05 ns delay time. To further increase the delay time, an off-chip SAW filter with about 20 ns group delay and 25 MHz bandwidth centered at 1.25 GHz is adopted.

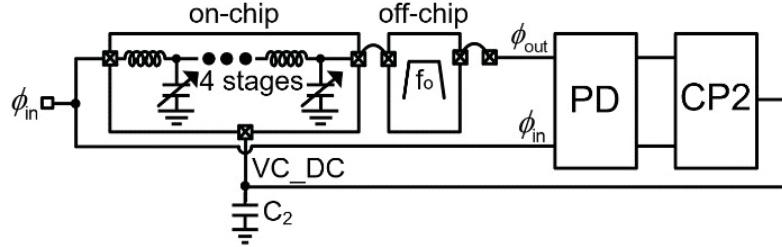


Figure 8: Block Diagram of the DLL

The DL transfer function is derived as [34]

$$H_{DL} = \frac{\Delta\phi}{\phi_m} = \frac{s/\omega_{p1}}{1 + s/\omega_{p1}} \cdot (1 - e^{-\tau s}) \approx H_{HPF} \cdot \tau s, \quad \omega_{p1} = \frac{I_{CP2} K_{DL}}{2\pi C_2} \quad (6)$$

where K_{DL} is the tuning gain of the DL in rad/V, I_{CP2} is the CP2 current in the DLL, and C_2 is the capacitor at the CP2 output. When f is much smaller than $1/\tau$, $1 - e^{-\tau s}$ can be simplified as τs . Therefore, the DL transfer gain is proportional to the delay time. Large delay time leads to a large DL transfer gain. In addition, the DLL performs the high pass characteristic with the corner frequency f_{p1} . The corner frequency f_{p1} should be designed small enough not to affect the low

frequency boundary of the phase noise suppression. In this design, f_{pl} is 1.5 kHz with $10 \mu\text{A}$ I_{CP2} , 0.13 rad/V K_{DL} , and 22 pF C_2 .

1.1.2.3 DCOC Loop

Any mismatch from the PD, CP, and variable gain amplifier (VGA) will cause large direct current (DC) offset at the VGA input, which blocks the desired phase noise signal. The DC offset may come from different mechanisms, such as the VGA DC offset, CP current mismatch, PD input phase mismatch, UP/DN rising and falling time difference. Therefore, a DCOC loop as shown in Figure 9 is adopted [34]. The output of VGA is continuously extracted by the integrator and compares with the common mode (CM) voltage V_{CM} . Then, the integrator output adjusts part of the discharging current source until the VGA output CM voltage settles to V_{CM} , which indicates the dc offset cancellation. A differential CP shown in Figure 9 is used in the PNF. Op Amps A1 and A2 are adopted to reduce the charging and discharging current mismatch [35].

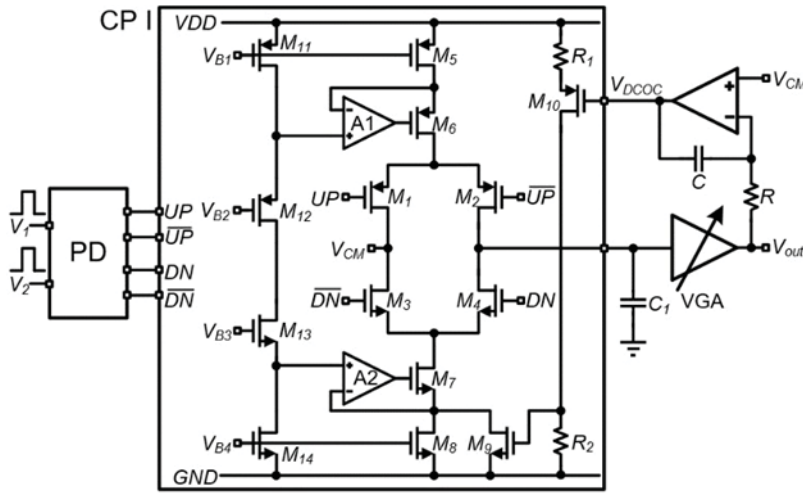


Figure 9: Block Diagram of the DCOC Loop

To maintain the DCOC loop stability, the dominant pole is minimized by choosing a large R (12.4 MΩ) and C (56 pF). Furthermore, the ratio of the adjustable and fixed discharging current source device size is proportional to the loop gain. Large ratio increases the current adjustability but degrades the phase margin. The ratio is 1:3 in this design as a trade-off between the DCOC capability and the loop stability. The simulated phase margin is 60° in the high gain mode.

DCOC capability is evaluated in two ways. First, a Monte Carlo simulation is performed on the transient of the VGA output including the device mismatch and process variation. Both the mean and standard deviation of the VGA output CM voltage indicate the good settling to the targeted 0.75 V as depicted in Figure 10. Second, all the mismatch from the circuits can be converted to the UP/DN phase mismatch in another point of view. Therefore, the maximum tolerable UP/DN phase mismatch is an important specification to characterize the DCOC capability. Transient simulations show that the DCOC loop can tolerate up to 45% phase mismatch, which indicates the successful dc offset cancellation with large mismatches [22].

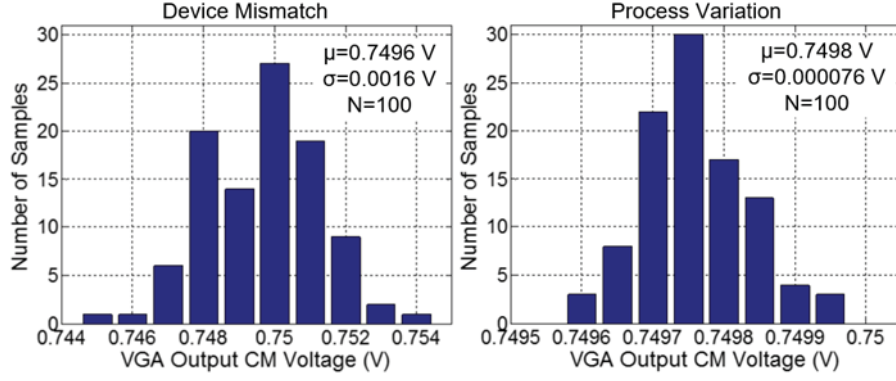


Figure 10: Monte Carlo Simulation Results of the VGA Output CM Voltage including the Device Mismatch and Process Variation

1.1.2.4 Other Circuit Blocks

A divider with a division ratio of 8 is adopted in the PNF to alleviate the speed requirement of the PD/CP. It is composed of three cascaded divide-by-2 circuits. Current mode logic (CML) divide-by-2 circuits are used in the first and second stages to meet the high speed requirement. The last divider is a true single-phase clocking (TSPC) type to reduce the power consumption and area.

A delay flip-flop (DFF) based phase frequency detector (PFD) is used as the PD. The VGA is realized in a non-inverting configuration to provide high impedance for the CP. It achieves 50 and 100 gain in the low and high gain mode, respectively. A passive low pass filter (LPF) is adopted with zero power consumption and good noise performance.

1.1.3 System Analysis

Phase noise suppression and phase noise sensitivity are two key specifications to characterize the PNF performance. They are closely related to the loop parameters.

1.1.3.1 Phase Noise Suppression

The amplitude of the PNF closed-loop phase noise transfer gain indicates the phase noise suppression level. Using the PNF phase domain model shown in Figure 11, the closed-loop phase noise transfer gain is calculated as

$$H_{close} = \frac{1}{\underbrace{1 + K_{VCPS} \cdot \frac{1}{M} \cdot H_{HPF} (1 - e^{-\tau s}) \cdot \frac{I_{CP1}}{2\pi} \left(R_{CP1} \parallel \frac{1}{sC_1} \right) \cdot G \cdot H_{LPF}}_{H_{open}}} \quad (7)$$

where K_{VCPS} is the VCPS phase adjustability in rad/V, M is the division ratio, τ is the delay time of the DL, I_{CP1} is the CP1 current, R_{CP1} is the output impedance of the CP1, C_1 is the capacitor at the CP1 output, G is the VGA gain, and H_{LPF} is the LPF transfer function. Based on (7), a large open loop gain leads to a large phase noise suppression. Therefore, a VGA is adopted to

maximize the open loop gain in a stable loop condition. Figure 12 shows the simulated phase noise transfer gain with 10.7 dB and 15.3 dB suppression at 1 MHz offset in low and high gain mode, respectively.

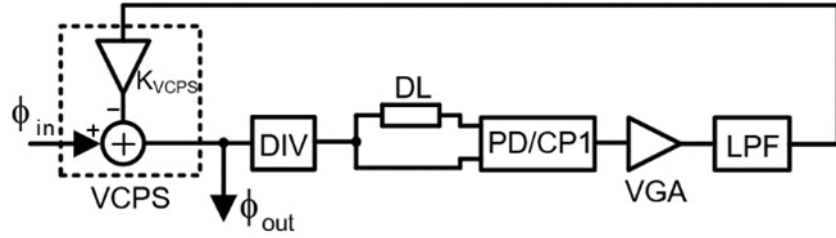


Figure 11: PNF Phase Domain Model

The suppression offset frequency range is about 100 kHz-12 MHz. The high frequency boundary of the phase noise suppression is determined by the LPF corner frequency f_{LPF} , which also affects the phase margin. A 2 MHz f_{LPF} is set as a trade-off between the suppression bandwidth and the loop stability. The low frequency boundary is determined by the CP1 corner frequency f_{CP1} (R_{CP1} and C_1) as long as the high pass corner frequency f_{p1} from the DL is much smaller than f_{CP1} . The low frequency boundary will be reduced with larger R_{CP1} as shown in Figure 12. However, a larger R_{CP1} requires a smaller I_{CP1} , which degrades the phase noise sensitivity as discussed in Section 1.1.2.

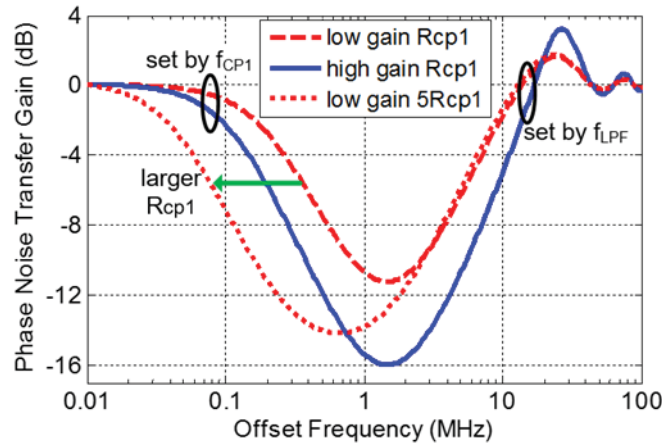


Figure 12: Simulated Phase Noise Transfer Gain in Low and High Gain Mode

1.1.3.2 Phase Noise Sensitivity

Phase noise sensitivity determines the best phase noise the PNF can achieve, which is calculated as

$$PN_{sensitivity} = 10 \log \left(\frac{1}{2} \sum |H_{n,each_block}|^2 \cdot \theta_{n,each_block}^2 \right) \quad (8)$$

where $H_{n,each_block}$ is the noise transfer function (NTF) from each block's output to the PNF output, $\theta_{n,each_block}^2$ is the output noise of each block. The NTF is derived according to the linear ac noise model as shown in Figure 13. Based on the NTF and simulated output noise of each

block, the phase noise sensitivity and each block's noise contribution are depicted in Figure 14. It clearly presents that the PD/CP1 contributes most of the noise. Therefore, PD/CP1 noise contribution reduction is the key to improve the phase noise sensitivity. The noise contribution from the PD/CP1 is calculated as

$$Noise_{PD/CP1} \approx \left| \frac{M}{2\pi f \cdot (I_{CP1}/2\pi)} \right|^2 \cdot \left(\frac{T_{on}}{T_s} \right)^2 \left(\frac{4kT\gamma \cdot 2I_{CP1}}{|V_{GSN} - V_{TN}|} + \frac{4kT\gamma \cdot 2I_{CP1}}{|V_{GSP} - V_{TP}|} \right) \quad (9)$$

where T_{on} is the on-time of the PMOS and NMOS in CP1 to avoid the “dead zone” and T_s is the UP/DN signal period. (9) clearly shows that a large CP current and a long DL reduce the noise contribution from the PD/CP1. The practical design trade-offs are discussed in part C and D. In this design, we optimize the CP current to be 1.28 mA and adopt the 20.8 ns DL (0.8 ns on-chip DL + 20 ns off-chip DL). At 1 MHz offset, the PNF achieves -116.6 dBc/Hz phase noise sensitivity.

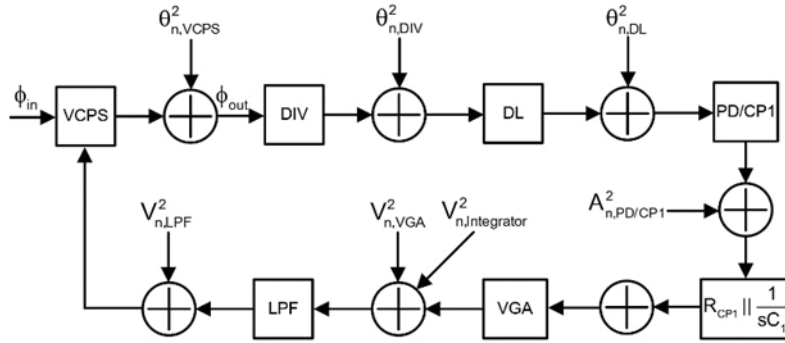


Figure 13: Linear ac Noise Model of the PNF

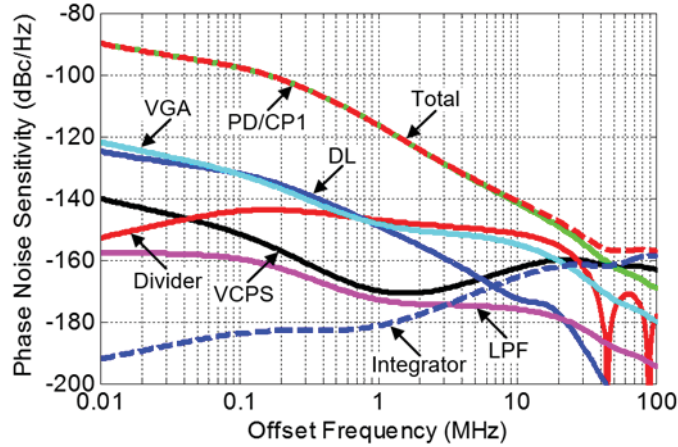


Figure 14: PNF Phase Noise Sensitivity and Noise Contribution from each Circuit Block

1.1.3.3 CP Current Effect

A large CP current is preferred to reduce the PD/CP1 noise contribution based on (9). However, the output impedance of the CP will decrease with larger CP current, which increases the low frequency boundary and reduces the phase noise suppression at low offset. In addition, the power consumption also increases. To find the optimum CP current, the phase noise sensitivity and low frequency boundary with different CP current are simulated and plotted in Figure 15. The optimum CP current is around 1.28 mA.

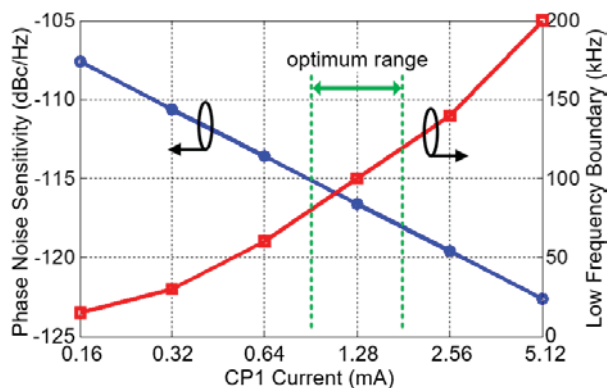


Figure 15: Phase Noise Sensitivity and Low Frequency Boundary vs. the different CP1 Current

1.1.3.4 DL Effect

The DL is an important component for the PNF because it determines the PNF performance in three ways. First, a long DL benefits the phase noise sensitivity because it reduces the noise of all following circuits including the PD/CP1. Ideally, the phase noise sensitivity improves by about 6 dB when the delay time doubles based on (9). However, a longer DL may introduce a larger loss that reduces the amplitude of the PD input. Smaller PD input degrades the PD/CP1 noise performance because of the smaller input transition slope. Figure 16 shows the simulated PD/CP1 output current noise with different loss. The noise degrades by about 8 dB with 20 dB loss at 1 MHz offset. Therefore, the phase noise improvement is less than 6 dB with the doubled delay time especially with a large DL loss. Second, a long DL increases the phase noise suppression level by increasing the loop gain, which however need to consider the system stability requirement. Third, a long DL may reduce the suppression bandwidth. In the DL transfer function of (6), $1 - e^{-\tau s}$ performs a periodic response with a period of $1/\tau$ and its amplitude is zero when the offset frequency is $1/\tau$, which sets the maximum suppression offset frequency.

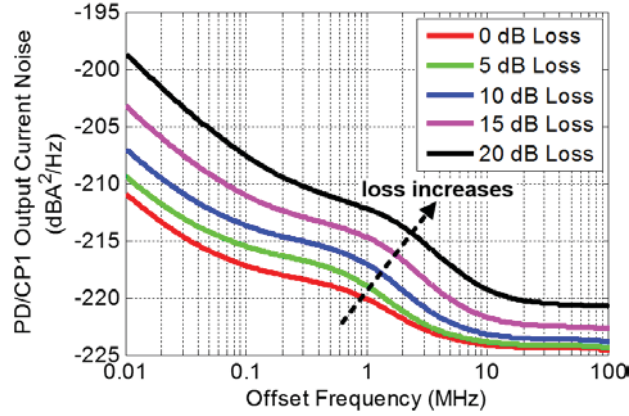


Figure 16: PD/CP1 Output Current Noise with different Loss Assumption from the DL

Figure 17 shows the simulated phase noise sensitivity, phase noise suppression at 1 MHz offset and suppression bandwidth versus the delay time with the assumption of 2 dB DL loss per 20 ns delay. When the delay time is larger than 80 ns, the phase noise sensitivity improvement rate drops significantly due to the dramatically degraded PD/CP1 noise caused by the large DL loss. In addition, the suppression bandwidth is limited to only 4 MHz when the delay time is 160 ns. It is worth to mention that the analysis is based on the 2 dB loss per 20 ns delay. If a DL with smaller loss is adopted, the phase noise performance will be better.

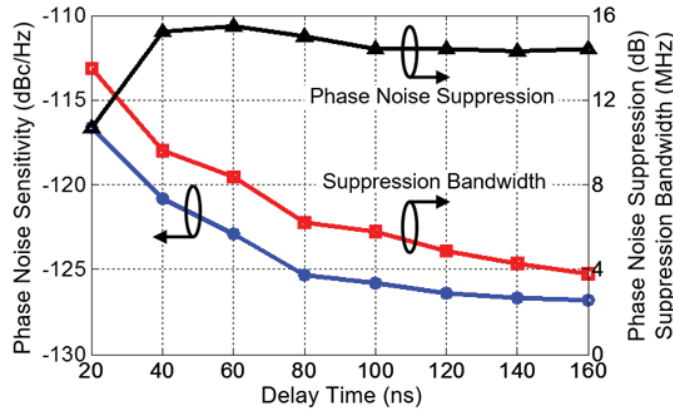


Figure 17: Simulated Phase Noise Sensitivity, Phase Noise Suppression at 1 MHz Offset, and Suppression Bandwidth vs. the Delay Time

1.1.4 Measurement Results

The proposed 10 GHz PNF is fabricated in a 65 nm complementary metal-oxide-semiconductor (CMOS) process and the chip area is 1.68 mm × 1.5 mm. Figure 18(a) shows the die photo. The chip is mounted to an FR4 printed circuit board (PCB) for test. It consumes 102 mW power and Figure 18(b) shows the power consumption breakdown. Buffers before and after the DL consumes 81% total power to drive the off-chip SAW filter.

Two testing methods are used to evaluate the PNF's phase noise suppression and phase noise sensitivity. One method is the single tone (ST) frequency modulated (FM) signal test and the other one is the LO with wideband noise test. As shown in Figure 19, the signal generator

generates a signal as the PNF input and the PNF output is measured by a signal analyzer. The feedback control signals from the DLL and main PNF loop are monitored by the oscilloscope.

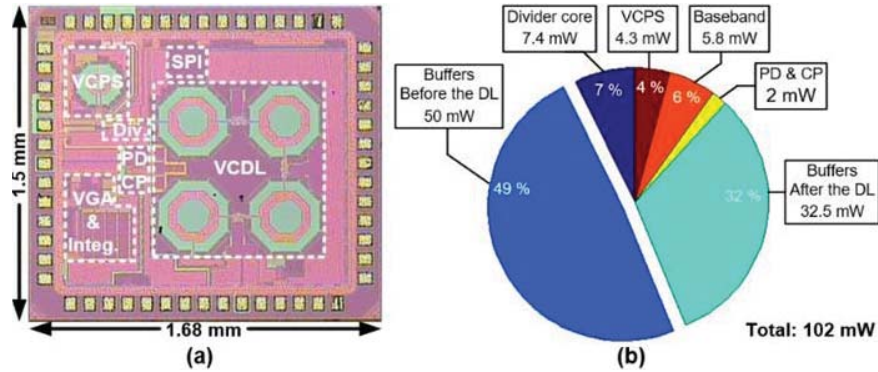


Figure 18: (a) PNF Die Photo and (b) Power Consumption Breakdown

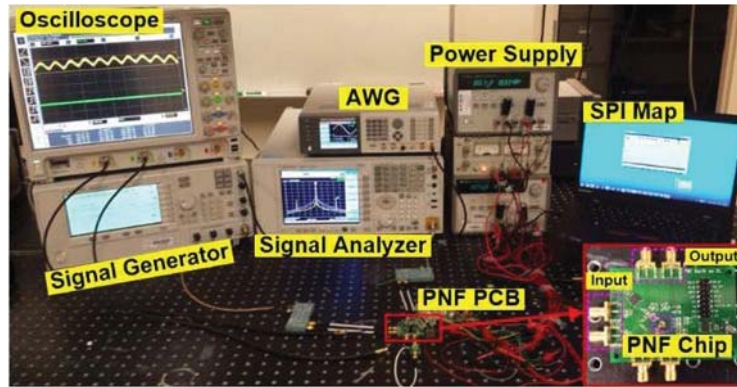


Figure 19: Test Setup for the PNF

1.1.4.1 Single Tone FM Signal Test

To measure the phase noise suppression level, a ST FM signal is applied first to emulate the LO with phase noise at a given offset frequency (equal to the FM rate). Figure 20(a) shows the 10 GHz input and output spectra of the PNF with 1 MHz FM rate. It indicates that the phase noise suppression level is 10.6/15 dB in the low/high gain mode respectively for a 10 GHz LO at 1 MHz offset. The input is generated by a high fidelity signal generator, which has superior noise performance. That is why the input noise floor is lower than the output noise floor, which is determined by the circuit noise. The stable DL control voltage VC_DC and 1 MHz V_{ctrl} with 747.1 mV CM voltage are plotted in Figure 20(b), which indicate the good loop working condition.

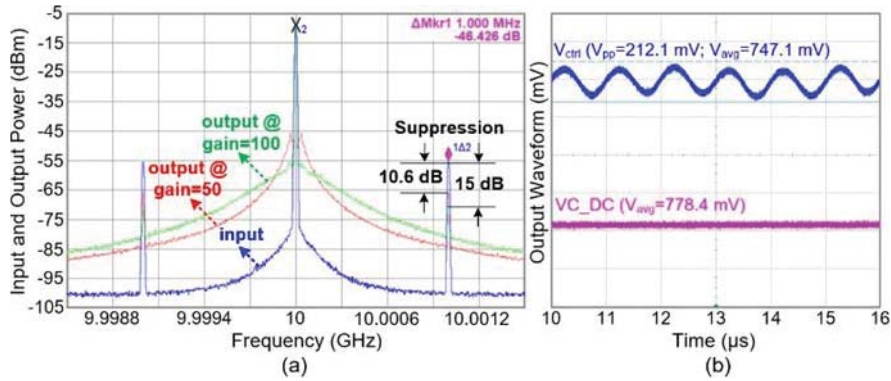


Figure 20: (a) Input and Output Spectra of the PNF in the ST FM Test and (b) Measured V_{ctrl} and V_{C_DC} Waveforms

By sweeping the FM rate, the phase noise suppression level versus the offset frequency at the two different gain modes are measured and plotted in Figure 21(a). The suppression bandwidth is from 100 kHz to 12 MHz and the maximum suppression level is 10.6/15.5 dB in the low/high gain mode, respectively. These results are close to the simulation results. Figure 21(b) shows the phase noise suppression at 1 MHz offset in low gain mode versus the input frequency. The input frequency range is 9.97-10.087 GHz with almost constant phase noise suppression. Out of this range, the phase noise suppression drops dramatically due to the unlocked DLL.

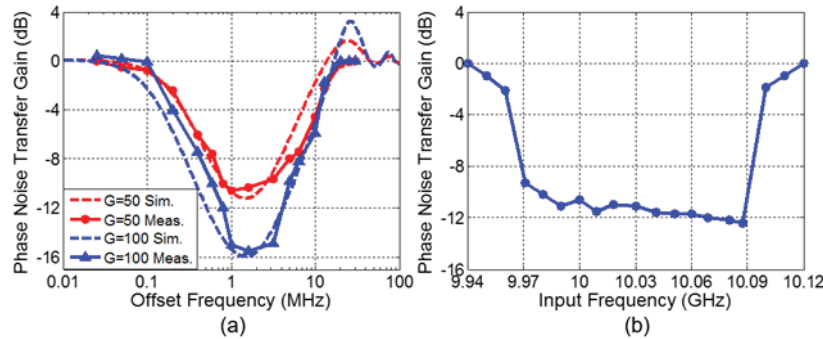


Figure 21: (a) Simulated and Measured Phase Noise Suppression Level in Low and High Gain Mode and (b) Phase Noise Suppression at 1 MHz Offset in Low Gain Mode vs. the Input Frequency with 20 ns DL

Figure 22 shows the simulated and measured phase noise sensitivity in low and high gain mode. Measured phase noise sensitivity is obtained by averaging the ST sensitivity over the resolution bandwidth (RBW). ST sensitivity is the output level which corresponds to no suppression for the input. The measured phase noise sensitivity is -116/-114.9 dBc/Hz at 1 MHz offset in low/high gain mode, respectively. They are also close to the simulation results. At the higher offset frequencies, the simulated phase noise sensitivity is 5-8 dB better than the measurement results. The possible reason is that the signal analyzer's noise floor limits the measurement accuracy.

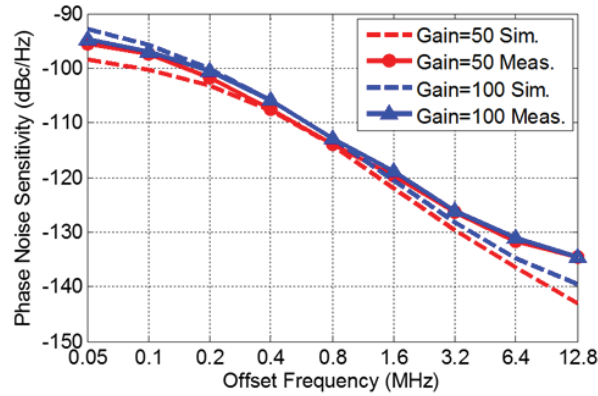


Figure 22: Simulated and Measured Phase Noise Sensitivity in Low and High Gain Mode with 20 ns DL

1.1.4.2 LO with Wideband Noise Test

To further evaluate the PNF performance, a signal with wideband noise modulation is used as the input. It is generated by the signal analyzer with FM function in noise modulation mode. Because the E8257D signal generator can only generate noise modulation up to 1 MHz, the maximum measurable phase noise offset frequency is limited to 1 MHz.

Figure 23 shows the input and output phase noise curves with a 10 GHz carrier in low and high gain mode. The noise suppression is 9.9/14.8 dB with -116.6/-114.9 dBc/Hz phase noise sensitivity at 1 MHz offset in low/high gain mode, respectively. The low frequency boundary is about 100 kHz. The results are consistent with the ST FM testing results.

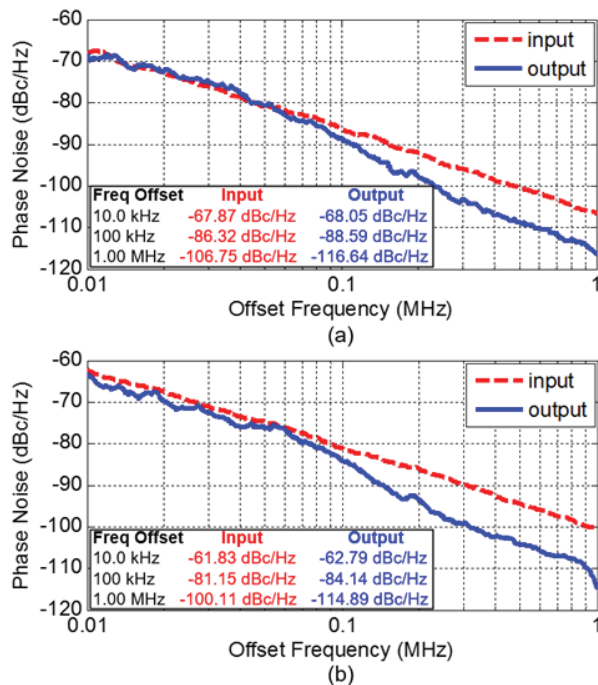


Figure 23: LO with Wideband Noise Test using 20 ns DL in (a) Low Gain Mode and (b) High Gain Mode

1.1.4.3 PNF Performance with Different Delay Time

The PNF performance with 2 and 4 cascaded SAW filters (~ 40 ns and 80 ns delay time) are measured and summarized in Table 3. The phase noise sensitivity is improved from -116.6 dBc/Hz to -119.9 dBc/Hz and -123.4 dBc/Hz at 1 MHz offset as shown in Figure 24 with the 40 ns and 80 ns DLs, respectively. The phase noise is measured by the signal analyzer with a 10 GHz clean input LO. The integrated jitter from 10 kHz to 100 MHz decreases from 176.0 fs to 111.0 fs and 85.5 fs when the delay time increases from 20 ns to 40 ns and 80 ns, correspondingly. The phase noise suppression is maintained at about 15 dB due to the loop stability requirement. The suppression bandwidth drops to 7 MHz when the delay time increases to 80 ns. The measured results match well with the simulated results in Figure 17. As for the input frequency range, it decreases from 117 MHz to 67 MHz and 31 MHz with the 40 ns and 80 ns DLs, which is caused by the limited tuning range of the VCDL. Figure 25 (a) and (b) show the LO with wideband noise testing results with 40 ns and 80 ns DLs, respectively. They achieve -119.9/-123.4 dBc/Hz phase noise sensitivity with 15.7/15 dB phase noise suppression at 1 MHz offset.

Table 3. PNF Performance Summary with Different Delay Time

Delay Time	20 ns	40 ns	80 ns
PN Sensitivity @ 1 MHz (dBc/Hz)	-116.6	-119.9	-123.4
PN Suppression @ 1 MHz (dB)	10.6	15	15.3
Integrated Jitter (fs) (10 kHz - 100 MHz)	176.0	111.0	85.5
Suppression Offset Freq. Range (MHz)	0.1 – 12	0.08 – 10	0.06 – 7
Input Frequency Range (GHz)	9.97 - 10.087 (117 MHz)	9.954 - 10.021 (67 MHz)	10.019 - 10.05 (31 MHz)

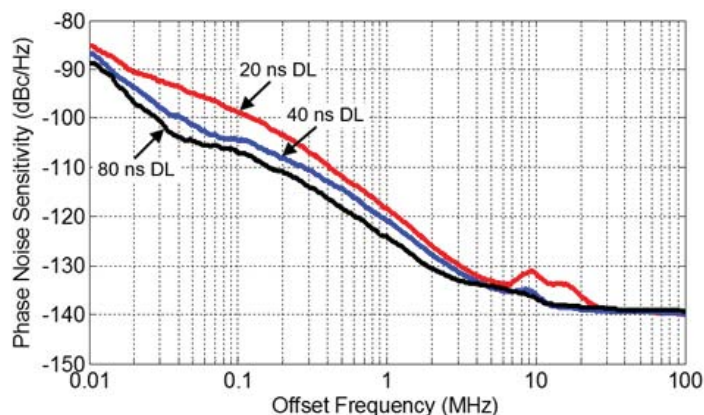


Figure 24: PNF Phase Noise Sensitivity with 20 ns, 40 ns, and 80 ns DLs

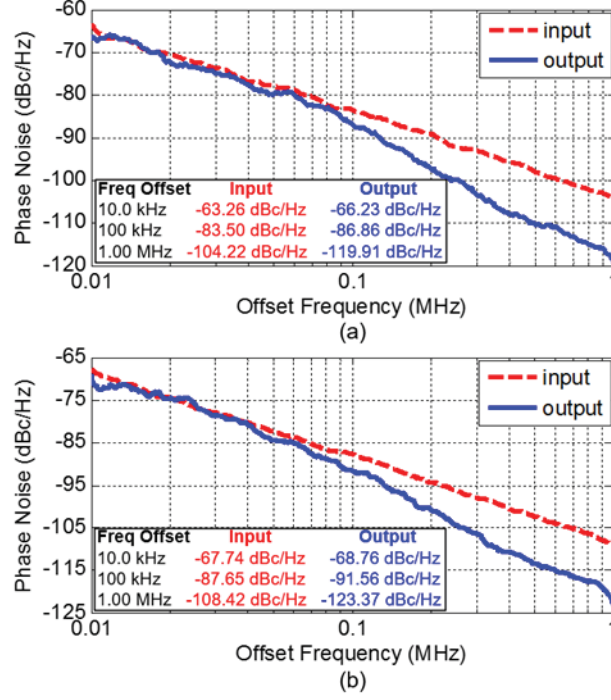


Figure 25: LO with Wideband Noise Test Using (a) 40 ns DL and (b) 80 ns DL

Table 4 summarizes the performance of the proposed PNF and compares with the published state-of-the-arts (SOAs) of the phase noise reduction systems and PLLs in similar CMOS technologies [7-9, 11-12, 19]. The PNF achieves better phase noise and integrated jitter than SOAs except [12]. To make a complete comparison, a commonly used figure of merit (FOM) for PLLs is adopted [36]. It is defined as $10\log [(\sigma_i/1s)^2 \cdot (P/1mW)]$, where σ_i is the integrated jitter and P is the power consumption. The PNF achieves -235.0 dB FOM with a 20 ns DL, which is better than other SOAs except [12]. With an 80 ns DL, the enhanced FOM of -241.3 dB is better than all the SOAs. [12]'s excellent phase noise performance relies on the high-Q film bulk acoustic resonator (FBAR) based DL, which however constrains the tuning range less than 5 MHz. Although the PNF's 117 MHz tuning range is smaller than SOAs except [12], it can be increased by using wideband DLs with large tunability. As summarized in Table 4, the PNF achieves better phase noise at low offset frequencies which can be utilized by reducing the low frequency boundary and adopting a longer DL.

Table 4. Performance Summary and Comparison with SOAs

Ref.	JSSC'10 [7]	TCAS II'16 [8]	TMTT'16 [9]	JSSC'13 [11]	TMTT'15 [12]	VLSI'16 [19]	This work
Design Type	All digital PLL	Fractional-N PLL	Fractional-N PLL	PLL with PN Suppression	PN Suppression System	Fractional-N PLL with PNF	PNF
Technology	90 nm CMOS	130 nm CMOS	130 nm CMOS	90 nm CMOS	130 nm CMOS	65 nm CMOS	65 nm CMOS
Chip Size (mm ²)	0.97 × 0.93	1.2 × 2.5 ^a	0.6 × 0.55 ^a	0.32 × 0.38 ^a	2 × 3	0.75 × 0.8 ^a	1.5 × 1.68
Delay Line Type	N/A	N/A	N/A	On-chip active inverter	Off-chip high-Q FBAR	On-chip active inverter	On-chip DL & off-chip SAW filter
Phase Extractor	N/A	N/A	N/A	Mixer	Mixer	Phase Averager	PD/CP
Sensitive to Amplitude Noise	N/A	N/A	N/A	YES	YES	N/A	NO
Suppress LO PN	NO	NO	NO	YES	YES	YES	YES
Carrier Frequency	10 GHz	10 GHz	1.76 GHz	5 GHz	1.5 GHz	1.152 GHz	10 GHz
Tuning Range	9.75 – 10.17 GHz	0.047 – 10 GHz	1.6 – 1.8 GHz	3.5 – 7.1 GHz	< 5 MHz ^b	N/A	117 MHz
Phase Noise (dBc/Hz)	-80 @ 100 kHz -100 @ 1 MHz -119.6 @ 10 MHz	-85 @ 50 kHz -100 @ 1 MHz -112 @ 3 MHz	-101 @ 100 kHz -108 @ 1 MHz -135 @ 10 MHz	-78 @ 100 kHz -105 @ 1 MHz -121 @ 10 MHz	-137 @ 100 kHz -141 @ 1 MHz -150 @ 10 MHz	-99 @ 100 kHz -109.4 @ 1 MHz -134.8 @ 10 MHz	-98.7 @ 100 kHz -116.6 @ 1 MHz -132.0 @ 10 MHz
Phase Noise ^c (dBc/Hz)	-80 @ 100 kHz -100 @ 1 MHz -119.6 @ 10 MHz	-85 @ 50 kHz -100 @ 1 MHz -112 @ 3 MHz	-86 @ 100 kHz -93 @ 1 MHz -120 @ 10 MHz	-72 @ 100 kHz -99 @ 1 MHz -115 @ 10 MHz	-120.5 @ 100 kHz -124.5 @ 1 MHz -133.5 @ 10 MHz	-80.2 @ 100 kHz -90.6 @ 1 MHz -116 @ 10 MHz	-98.7 @ 100 kHz -116.6 @ 1 MHz -132.0 @ 10 MHz
Integrated Jitter	1.1 ps (50k – 80MHz)	1.44 ps ^d (BW: N/A)	1.18 ps ^e (30k – 10MHz)	3.8 ps (10k – 10MHz)	76 fs ^e (10k – 40MHz)	1.48 ps (100k – 100MHz)	176 fs (10k – 100MHz)
Power (mW)	7.1	80	8.3	29.6	350	19.8	102
FOM (dB)	-230.7	-217.8	-229.4	-213.7	-236.9	-223.6	-235.0 ^f

a. Core area excluding the pads. b. Estimated from the S-parameters of FBAR. c. Convert to 10 GHz with the 20 dB/decade trend. d. Calculated from the RMS phase error. e. Estimated from the phase noise. f. -239.0/-241.3 with the 40/80 ns DL respectively.

1.2 2nd Version: 1st Time-Amplifier Enhanced Linear PNF

1.2.1 1st Time-Amplifier Enhanced PNF Architecture

1.2.1.1 Time-Amplifier Enhanced PNF System Description

The proposed time amplifier enhanced PNF (TAPNF) block diagram is shown in Figure 26, which consists of a VCPS, a divider, a DL, a resettable low noise time amplifier (LNTA), charge pump 1 (CP1), C_1 and BB circuits. The DL converts the phase noise (PN) into relative timing jitter. The resettable LNTA detects the relative timing jitter, amplifies it and then converts it to a low frequency voltage with the help of CP1 and C_1 . The low frequency voltage is further amplified and filtered by the BB circuits to get the desired V_{ctrl} . The V_{ctrl} controls the VCPS in a negative feedback loop to generate the required phase shifting to contradict the phase changed by the PN, which achieves PN suppression for the input LO. A divide-by-8 divider is used to alleviate the speed requirement of LNTA and CP1. In addition, a cascaded of off-chip SAW and on-chip VCDL is used as the DL to provide both long delay and tunability [3]. Different from [3], this proposed TAPNF replaces the linear PD with a resettable LNTA to enhance the PN performance as discussed in the next section.

Since the TAPNF deals with the PN, any circuit mismatch may deteriorate the PN extraction and cancellation. Therefore, a DLL is adopted to align the PD input phase [3]. The DLL is unconditionally stable because it's a one pole system. In addition, a DCOC loop is realized to cancel the mismatch from the PD, CP and VGA and set the CM voltage of the CP1 output to a fixed value V_{CM} . The transient of VGA output can settle to V_{CM} in both Monte Carlo simulation and up to 45% UP/DN timing/current mismatch conditions, which indicates successful DC offset cancellation [3].

To simulate the phase noise suppression, a ST FM signal is applied to the input to emulate the LO with phase noise. Figure 27(a) shows the 10 GHz output spectrum with ST FM input of 1 MHz modulation frequency and 0.1 index (-26 dBc), which shows 13.5 dB suppression at 1 MHz offset with output of -39.5 dBc.

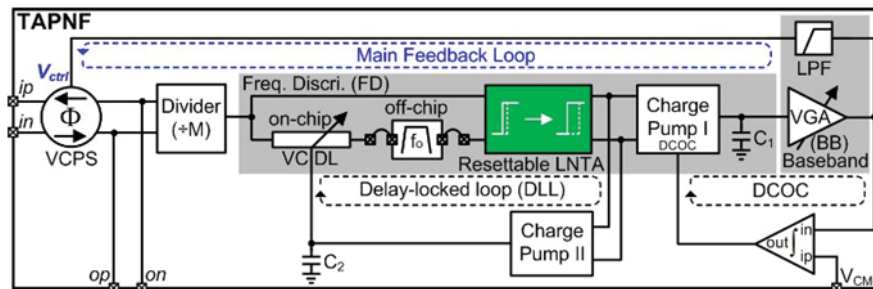


Figure 26: Block Diagram of the proposed TAPNF

1.2.1.2 PN Improvement by LNTA

For the PNF without time amplifier (TA), the main noise contributor is the CP1, whose noise contribution is calculated as the division of the output current noise and the gain of the preceding stages [3]. The larger the preceding gain is, the smaller the CP1 noise contribution is. Therefore, we propose to use a LNTA as the preceding stage of the CP1 to suppress its noise. After using the LNTA, the output noise of the TAPNF is calculated as

$$Noise_{wiLNTA} \approx \left| \frac{M}{2\pi f \cdot \tau} \right|^2 \cdot \left(N_{LNTA_input} + \frac{N_{CP1_input}}{A_{LNTA}^2} \right) \quad (11)$$

where M is the division ratio, τ is the DL delay time, I_{CP1} is the CP1 current and A_{LNTA} is the gain of the LNTA. Because the interface of these two blocks are on chip without matching requirement, the noise equation doesn't have the impedance transformation. To enhance the PN sensitivity, large A_{LNTA} and low N_{LNTA_input} are required based on (a). In addition, large τ reduces both the CP1 and the LNTA noise contributions.

To show the PN improvement effect from the LNTA, the PN sensitivity and major noise contributors without and with the LNTA is simulated and plotted in Figure 27(b). Figure 27(b) clearly shows that the major noise contributor becomes the LNTA instead of the CP1 after adopting the LNTA and the simulated PN sensitivity improves from -116 dBc/Hz to -126 dBc/Hz at 1 MHz offset with a 10 GHz carrier, whose 10 dB improvement is attributed by the LNTA.

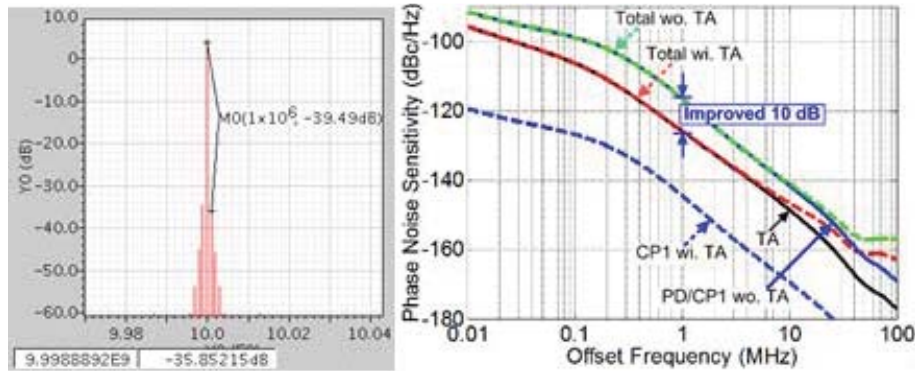


Figure 27: (a) Simulated 10 GHz Output Spectrum with ST FM Input of 1 MHz Modulation Frequency and 0.1 index (-26 dBc) and (b) PNF's PN Sensitivity and Major Noise Contributors without and with the LNTA

1.2.2 Resettable LNTA Design

The core schematic of the LNTA is shown in Figure 28(a) [4]. At the arrival of a fast rising edge at the gate of M_1 , a current impulse travels from the drain of M_1 to the drain of M_2 whereby a certain amount of negative charge is injected from C_2 to C_1 . Then, upon the arrival of another edge at the gate of M_3 , another negative charge is injected from the drain of M_4 to the drain of M_3 . However, the second charge injection is smaller. A high-speed comparator detects its input

polarity inversion to obtain the desired output. The input and output waveforms of the LNTA are depicted in Figure 28(c), which indicates the gain of A_{LNTA} . For the typical TA without the reset path, the overlap time of the outputs is large. Therefore, the TA can't drive the CP directly due to the induced large CP1 noise. By adding the reset path, the TA outputs' overlap time reduces dramatically compared with the typical TA as shown in Figure 28(c), which removes the need of PD. The simulated current noise of resettable TA+CP1 is the same as the normal TA+PD+CP1. Therefore, the resettable TA is applicable.

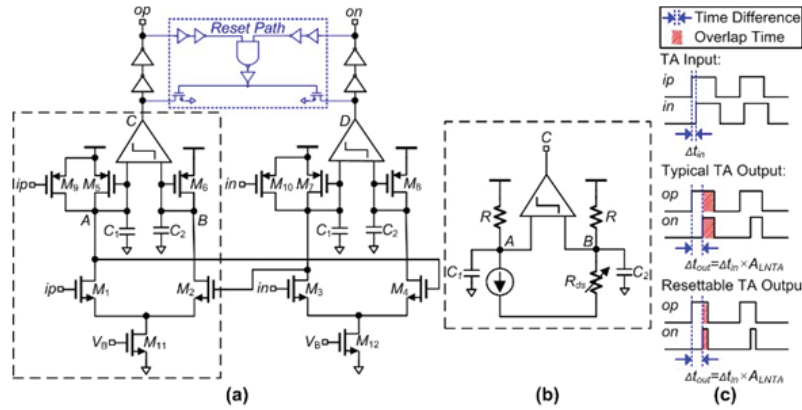


Figure 28: (a) Schematic of the LNTA, (b) Model for the Left Side of the LNTA, and (c) Input and Output Waveforms of the LNTA

1.2.2.1 Phase Noise

To evaluate the noise performance of the TA, a simplified model for the left side of LNTA is adopted as shown in Figure 28(b). M_1 is modeled as a current source, and M_2 is modeled as a linear resistance R_{ds} . The overall PN at node C is proportional to the PN at node A and B, which are approximated as [4]

$$S_A(f) \propto C_1(\eta W + C_1)/W^3, S_B(f) \propto C_2(\eta W + C_2)/W^3 \quad (12)$$

where W represents the channel width of the transistors M_1 - M_4 , C_1 and C_2 represent the load capacitors. (2) indicates that the TA favors large W and small C_1 and C_2 . However, a large W increases the load capacitance for the input buffer, which consumes more power and degrades the buffer PN. To find the optimum W , the PN and buffer power consumption with different W are simulated and plotted in Figure 29(a). The optimum W is 100 μm with -135 dBc/Hz PN at 1 MHz offset and medium buffer power consumption. The PN improvement rate drops with larger W due to the buffer PN degradation.

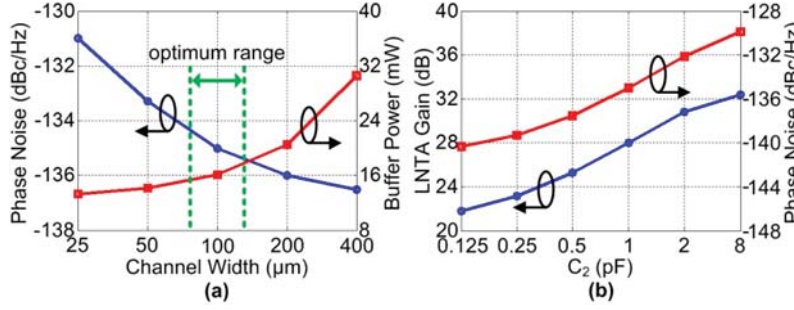


Figure 29: (a) PN and Buffer Power Consumption vs. different Channel Width and (b) LNTA Gain and PN vs. different C₂

1.2.2.2 Gain

A large gain of LNTA is desired to suppress the noise contribution from CP. Based on the current transmission procedure, the gain is calculated as

$$A_{LNTA} = k \cdot W \cdot (C_2/C_1) \quad (13)$$

where k is the coefficient to indicate the charge transfer rate. Small C_1 and big C_2 are preferred. However, a large load capacitor increases the PN based on (2). In this design, C_1 is minimized and realized by the parasitic capacitance at node A. Figure 29(b) shows the gain and PN versus different C_2 , which validates the analytical result. 1 pF C_2 is chosen as a tradeoff of gain and area. In addition, a larger W leads to a higher LNTA gain, because more charge is transferred due to the small equivalent resistance of the current transmission transistor. The optimized resettable LNTA achieves 28 dB gain and -135 dBc/Hz PN at 1 MHz offset with 8.9 mW power consumption.

1.2.3 Measurement Results

The proposed 10 GHz TAPNF is fabricated in a 65-nm CMOS process and occupies 1.4 mm × 1.6 mm chip area. It consumes 94.6 mW power. The die photo is shown in Figure 30(a).

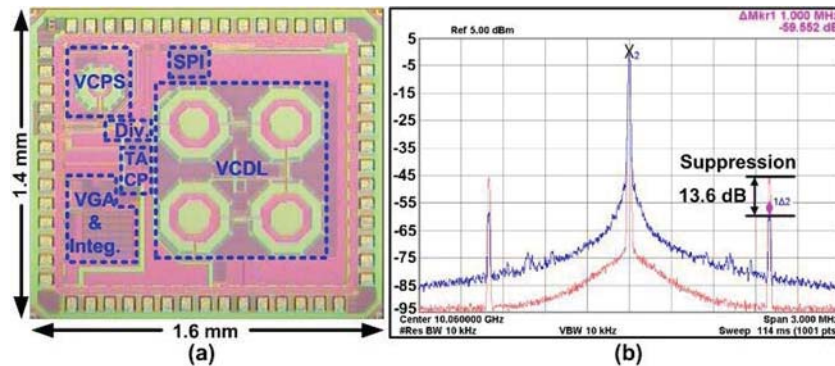


Figure 30: (a) TAPNF Die Photo and (b) ST FM Test with 20 ns DL

The TAPNF is measured with the 20/40/80 ns DLs in terms of the PN suppression level, input frequency range, PN sensitivity and LO with wideband noise test. First, PN suppression is evaluated by injecting a ST FM signal emulating the LO with PN at an offset frequency (equal to FM rate). Figure 30(b) shows the input and output spectra for the TAPNF with the 20 ns DL, achieving 13.6 dB PN suppression for a 10 GHz LO at 1 MHz offset. By sweeping the FM rate, the PN suppression level versus the offset frequency with 20/40/80 ns DLs are measured and plotted in Figure 31(a), which demonstrates 90k-11MHz/50k-10MHz/30k-8MHz suppression bandwidth with 13.6/13.4/14.4 dB maximum PN suppression. Figure 31(b) shows the respective 100/50/24 MHz input frequency range.

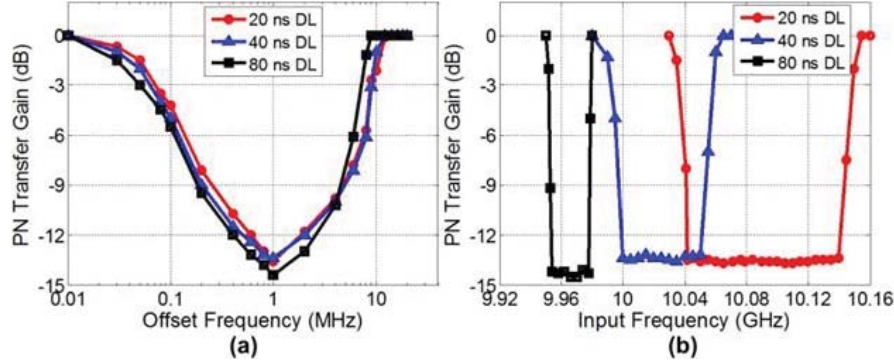


Figure 31: (a) PN Suppression Level and (b) Input Frequency Range

PN sensitivity is measured by the signal analyzer with a clean input from the signal generator. Figure 32(a) shows the PN sensitivity with the 20/40/80 ns DLs, which achieve -125/-129/-132 dBc/Hz PN sensitivity at 1 MHz offset, and 70/52/34 fs integrated jitter from 10 kHz to 100 MHz, respectively. To verify the PN sensitivity and suppression at the same time, an input LO with wideband noise modulation is generated as the TAPNF input. Figure 32(b) shows 14.3 dB PN suppression with -132.1 dBc/Hz sensitivity with 80 ns DL, which matches well with the measured ST and PN sensitivity results. The maximum measurable PN offset frequency is limited to 1 MHz because the E8257D can only generate noise modulation up to 1 MHz.

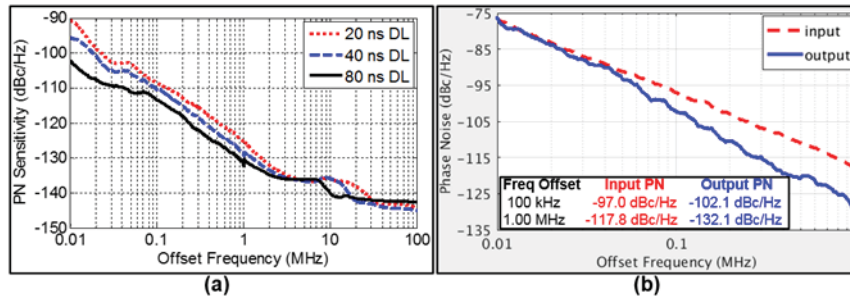


Figure 32: (a) TAPNF PN Sensitivity with different DLs and (b) Input LO with Wideband Noise Modulation Test with 80 ns DL

Table 5 summarizes the performance of the TAPNF and compares to the published state-of-the-arts (SOAs). The achieved -125/-129/-132 dBc/Hz PN sensitivity for a 10 GHz carrier are the best of all. In addition, a commonly used FOM defined as $10\log [(\sigma_t/1s)^2 \cdot (P/1 \text{ mW})]$ for PLLs is adopted, where σ_t is the integrated jitter and P is the power consumption. The TAPNF

achieves -243.3/-245.9/-249.6 dB FOM, which are the best. Based on the authors' best knowledge, this PNF achieves the best PN and FOM compared to other PLLs and PNFs with similar technologies and carrier frequencies. Therefore, the TAPNF provides a new approach to further enhance the clock PN.

Table 5. Performance Summary and Comparison with SOAs

Ref.	JSSC'13 [1]	TMTT'15 [2]	TMTT'17 [3]	TCAS II'16 [6]	VLSI'16 [7]	This work
Design Type	PLL w/ PNF	VCO w/ PNF	Linear PD PNF	PLL	PLL w/ PNF	TAPNF
Technology	90 nm CMOS	130 nm CMOS	65 nm CMOS	130 nm CMOS	65 nm CMOS	65 nm CMOS
Chip Size (mm ²)	0.32 × 0.38 ¹	2 × 3	1.5 × 1.68	1.2 × 2.5 ¹	0.75 × 0.8 ¹	1.4 × 1.6
Carrier Freq.	5 GHz	1.5 GHz	10 GHz	10 GHz	1.152 GHz	10 GHz
Tuning Range	3.5 – 7.1 GHz	< 5 MHz ²	117 MHz	0.047-10 GHz	N/A	100/50/24 MHz ³
PN Suppress.	12.5 dB	N/A	10.6 dB ⁴	N/A	N/A	13.6/13.4/14.4 dB
Phase Noise (dBc/Hz)	-78 @ 100 kHz -105 @ 1 MHz	-137 @ 100 kHz -141 @ 1 MHz	-98.7 @ 100 kHz -116 @ 1 MHz	-85 @ 50 kHz -100 @ 1 MHz	-99 @ 100 kHz -109.4 @ 1 MHz	-108.5/-110.5/-113.4 @ 100 kHz -125.7/-129.3/-132.3 @ 1 MHz
Phase Noise ⁵ (dBc/Hz)	-72 @ 100 kHz -99 @ 1 MHz	-120.5 @ 100 kHz -124.5 @ 1 MHz	-98.7 @ 100 kHz -116 @ 1 MHz	-85 @ 50 kHz -100 @ 1 MHz	-80.2 @ 100 kHz -90.6 @ 1 MHz	-108.5/-110.5/-113.4 @ 100 kHz -125.7/-129.3/-132.3 @ 1 MHz
Integrated Jitter	3.8 ps (10k – 10MHz)	76 fs ^{6,7} (10k – 40MHz)	176 fs ⁶ (10k – 100MHz)	1.44 ps (BW: N/A)	1.48 ps (100k – 100MHz)	70/52/34 fs (10k – 100MHz)
Power (mW)	29.6	350	102	8.3	19.8	94.6
FOM (dB)	-213.7	-236.9	-235.0	-229.4	-223.6	-243.3/-245.9/-249.6

1. Core area excluding the pads. 2. Estimated from the S-parameters of FBAR. 3. With 20/40/80 ns DLs respectively.

4. Low gain mode with better phase noise. 5. Convert to 10 GHz with the 20dB/decade trend. 6. Estimated from the PN.

7. Jitter is degraded by the phase noise hump in the offset frequency range of 500 kHz-10 MHz.

1.3 3rd Version: 2nd Time-Amplifier Enhanced Linear PNF

1.3.1 2nd Version Time-Amplifier Enhanced PNF Architecture

The proposed TAPNF block diagram is shown in Figure 33, which consists of a VCPS, a divider, a FD, and BB circuits. The FD converts the PN information into low V_{ctrl} . The V_{ctrl} controls the VCPS in a negative feedback loop to generate the required phase shifting to contradict the phase changed by the PN, which achieves PN suppression for the input LO.

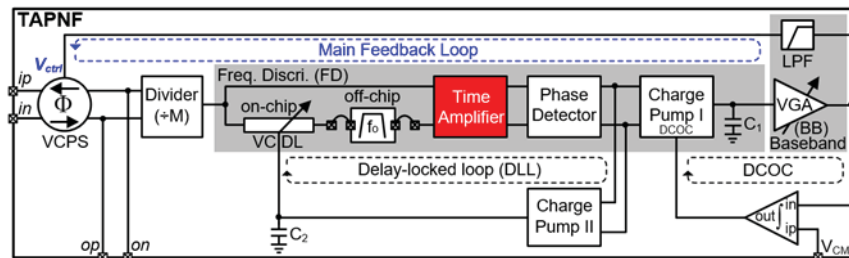


Figure 33: Block Diagram of the proposed 2nd Version TAPNF

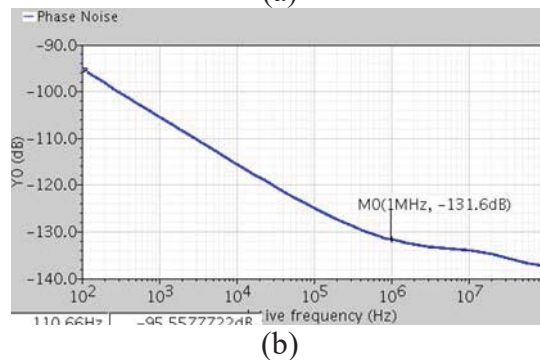
1.3.2 Low Noise 2nd Version TA Design

To save the power and area, the inverter-type TA is adopted in this design as shown in Figure 34(a) [5]. The drain of M4 and M9 are initially pre-charged to VDD when the two inputs are low. When the rising edge of the inputs arrives, the drain nodes of M4 and M9 will be discharged through two paths: input inverter path and a dependent M5 and M10 path. Because the discharging strength of the second transition is determined by the discharging status of the first

$$Gain = \frac{W_{3N} + W_{5N}}{W_{3N}} \quad (14)$$

PN performance is critical for the TA. By using the similar PN analysis method of inverter, the PN of the TA is approximated as

where C_L represents the load capacitance. (15) indicates that TA favors large channel width and small load capacitance. Large channel width also leads to large TA gain as shown in (2). However, the large channel width increases the load capacitance for the preceding stage (input buffers), which consumes more power. In this design, the W_{3N} and W_{5N} are optimized to be $2\text{ }\mu\text{m}$ and $7\text{ }\mu\text{m}$. The cascaded three-stage TA achieves -131.6 dBc/Hz PN at 1 MHz offset as shown in Figure 34(b) and 39 dB gain with 0.8 mW power consumption.



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1.3.3 Power Consumption Reduction

For other PNFs, the major power is consumed by the buffers before and after the DLs as shown in Figure 35(a). The boosted swing at the PD/CP1 input benefits the noise performance. In this design, by carefully choosing the value of the alternating current (AC) coupling capacitor and resistor of the self-biased inverter, the matching resistor R can be removed to increase the input swing. In addition, the good PN performance of the TA also relaxes the input swing requirement. Therefore, the buffers before and after the DLs are greatly optimized and the power consumption is reduced by about 52 mW. The new power consumption distribution is shown in Figure 35(b).

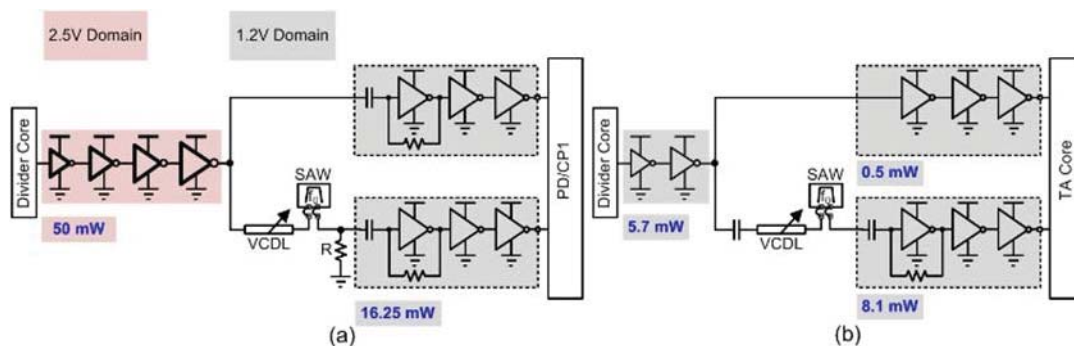


Figure 35: (a) Major Power Consumption Distribution of other PNFs and (b) Optimized Power Consumption of TAPNF

1.3.4 Measurement Results

The proposed 10 GHz TAPNF is fabricated in a 65 nm CMOS process and occupies $1.4 \text{ mm} \times 1.6 \text{ mm}$ chip area. It consumes 50 mW power. The die photo is shown in Figure 36(a).

First, TAPNF's PN suppression is measured by injecting a single tone (ST) frequency modulated (FM) signal emulating the LO with PN at an offset frequency (equal to FM rate). Figure 36(b) shows the input and output spectra with 1 MHz FM rate, which achieve 8 dB PN suppression for a 9.64 GHz LO at 1 MHz offset. By sweeping the FM rate, the PN suppression level versus the offset frequency is measured and plotted in Figure 37(a). The suppression bandwidth is 40k-8MHz with the 8 dB maximum suppression level. In addition, it achieves about 60 MHz input frequency range as shown in Figure 37(b).

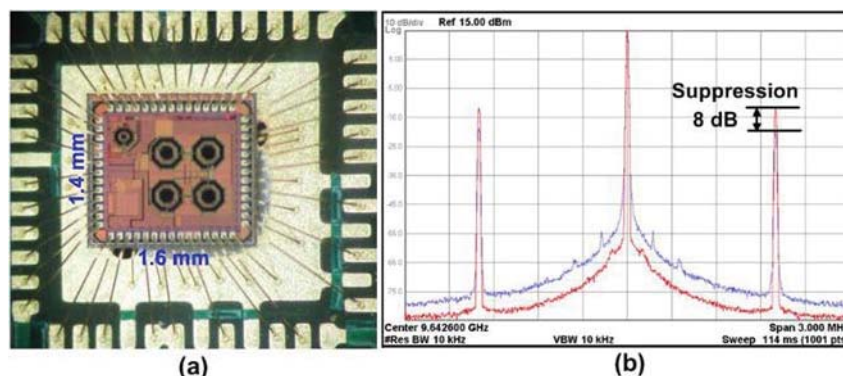


Figure 36: (a) TAPNF Die Photo and (b) ST FM Test Spectra

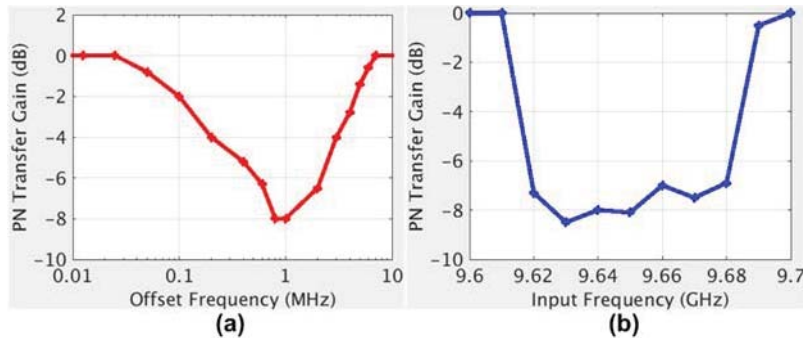


Figure 37: (a) PN Suppression Level and (b) Input Frequency Range

PN sensitivity is measured by the signal analyzer as shown in Figure 38, achieving -133 dBc/Hz at 1 MHz offset. The integrated jitter from 10 kHz to 100 MHz is 52 fs. To verify the PN sensitivity and suppression at the same time, an input LO with wideband noise modulation is generated as the TAPNF input. Figure 39 shows the input and output PN curves and it achieves 8 dB PN suppression with -133 dBc/Hz sensitivity, which matches well with previous results. The maximum measurable PN offset frequency is limited to 1 MHz because the E8257D can only generate noise modulation up to 1 MHz.

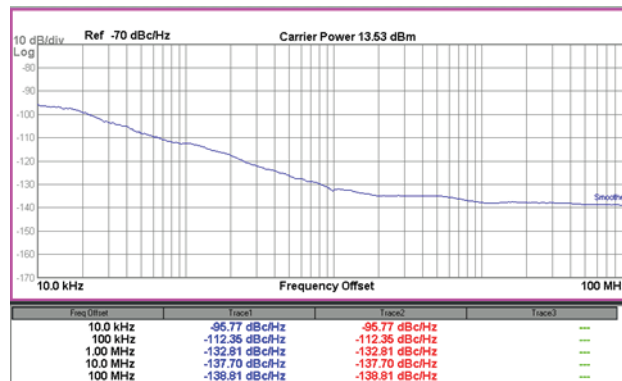


Figure 38: TAPNF PN Sensitivity

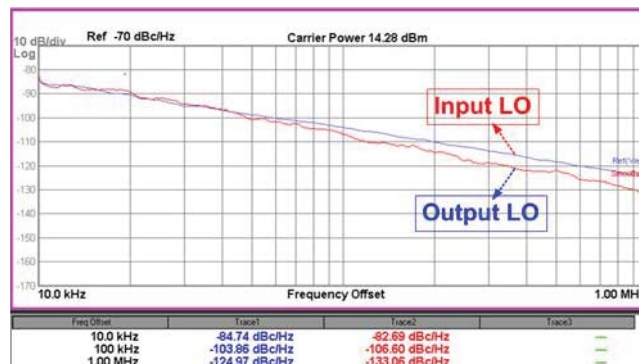


Figure 39: Input LO with Wideband Noise Modulation Test

Table 6 summarizes the performance of the TAPNF and compares to the published SOAs. The achieved -133 dBc/Hz PN sensitivity for a 10 GHz carrier is the best of all. The 50 mW power consumption is also the smallest among [2-4]. A commonly used FOM defined as $10\log[(\sigma_t/1s)^2 \cdot (P/1mW)]$ for PLLs is adopted to evaluate the performance in a comprehensive way, where σ_t is the integrated jitter and P is the power consumption. This TAPNF achieves the best FOM, -248.7 dB. Therefore, the TAPNF provides a new approach to further enhance the clock generator's PN.

Table 6. Performance Summary and Comparison with SOAs

Ref.	JSSC'13 [1]	TMTT'15 [2]	IMS'16 [3]	IMS'17 [4]	This work
Design Type	PLL wi. PNF	VCO wi. PNF	Linear PD PNF	BBPD PNF	TAPNF
Technology	90 nm CMOS	130 nm CMOS	65 nm CMOS	65 nm CMOS	65 nm CMOS
Chip Size (mm²)	0.32 × 0.38 ¹	2 × 3	1.5 × 1.68	1.48 × 1.77	1.4 × 1.6
Carrier Freq.	5 GHz	1.5 GHz	10 GHz	10 GHz	10 GHz
Tuning Range	3.5 – 7.1 GHz	< 5 MHz ²	117 MHz	100 MHz	60 MHz
PN Suppress.	12.5 dB	N/A	10.6 dB	15 dB	8 dB
Phase Noise (dBc/Hz)	-78 @ 100 kHz -105 @ 1 MHz	-137 @ 100 kHz -141 @ 1 MHz	-98.7 @ 100 kHz -116 @ 1 MHz	-98.4 @ 100 kHz -120.3 @ 1 MHz	-112 @ 100 kHz -133 @ 1 MHz
Phase Noise ³ (dBc/Hz)	-72 @ 100 kHz -99 @ 1 MHz	-120.5 @ 100 kHz -124.5 @ 1 MHz	-98.7 @ 100 kHz -116 @ 1 MHz	-100 @ 100 kHz -117.2 @ 1 MHz	-112 @ 100 kHz -133 @ 1 MHz
Integrated Jitter	3.8 ps (10k – 10MHz)	76 fs ^{4,5} (10k – 40MHz)	135.7 fs ⁴ (50k – 12.8MHz)	81.2 fs (100k – 10MHz)	52 fs (10k – 100MHz)
Power (mW)	29.6	350	102	98	50
FOM (dB)	-213.7	-236.9	-237.3	-241.9	-248.7

1. Core area excluding the pads. 2. Estimated from the S-parameters of FBAR

3. Convert to 10 GHz with the 20dB/decade trend. 4. Estimated from the PN.

5. Jitter is degraded by the phase noise hump in the offset frequency range of 500 kHz-10 MHz.

2. Second Category: Non-linear Phased Noise Filter

2.1 1st Version: BBPD based Non-linear PNF

2.1.1 Architecture

In this part, we propose a bang-bang detector (BBPD) and delay line FD based PNF to mitigate the above issues. Compared to the other FDs, this design replaces the mixer and linear PFD with a BBPD. This choice leads to in-phase input requirement and a better PNF noise floor, since the BBPD with extremely high gain suppresses the CP noise. This PNF acts as a general function unit to improve the clock phase noise without the need of a superior reference.

To overcome the disadvantages of the methods mentioned above, we employ a BBPD based FD, as shown in Figure 40. It is composed of a long delay line, a VCDL, a BBPD, a voting machine and a CP, and works in a similar way to the linear PFD/CP based FD. The difference is the use of a binary phase detector, which provides only an indication of the phase difference between the two inputs in a binary form. This inevitably pushes the phase detector gain to an extremely high level, thus suppressing the CP induced noise to a negligible value [11]. This approach also enables in-phase inputs, which is adjusted by the VCDL. We employ this BBPD based FD in the proposed PNF in Figure 41.

This PNF consists of a VCPS, a divider, a FD, and a baseband circuit. The 10 GHz input LO is converted to a 1.25 GHz signal by the divide-by-8 divider to alleviate the design challenges of the subsequent circuits. The FD converts the phase noise information into a low frequency voltage and is further filtered to get the desired V_{ctrl} . The V_{ctrl} controls the VCPS in a negative feedback loop to achieve the required phase shifting in order to compensate the input phase error. As mentioned before, the FD is the key unit of this system because it determines the phase noise floor, suppression bandwidth and input frequency range.

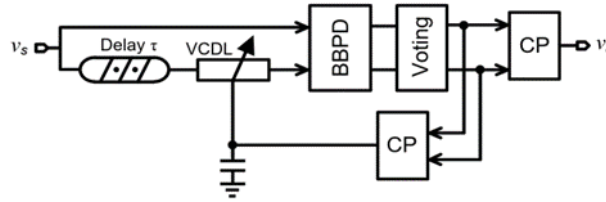


Figure 40: Block Diagram of the Proposed BBPD based FD

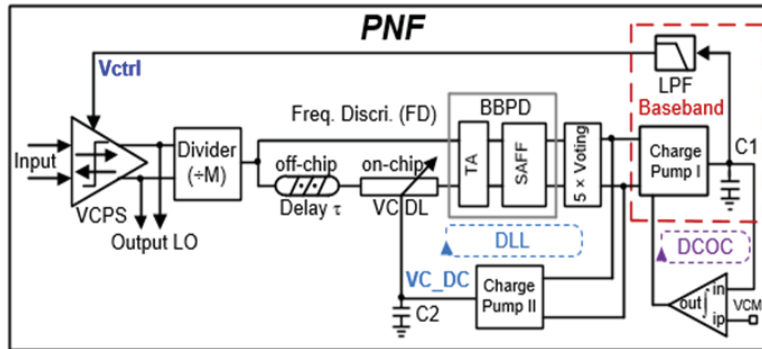


Figure 41: Block Diagram of the Proposed BBPD based PNF

The off-chip passive delay line is used to reach a long delay time τ with low noise, while the tunable on-chip VCDL with 250 ps tunable range is only employed to adjust the BBPD input phase relations. The adoption of a $5 \times$ voting scheme improves the BBPD noise performance by minimizing its error decisions, as will be discussed in the following section. Two local feedback loops are embedded into the PNF for calibration.

Since the proposed BBPD based PNF is based on a multiple-loop structure, the interaction among the loops should be considered. The main loop is made much faster than the DLL and DCOC loop to avoid interference. The DLL is used only to remove low frequency contents, including the DC component, thus having negligible effects to the main loop. With a 2 uA CP2 current and 80 pF C2, the DLL tracking bandwidth is close to 100 kHz. The same design strategy also applies to the DCOC loop. Its loop bandwidth needs to be significantly lower than the target phase noise suppression band to avoid interfering with the main loop. Consequently, DCOC only determine the DC level of the feedback voltage V_{ctrl} . Its simulated 3 dB bandwidth is about 10 Hz.

2.1.2 Limit Cycle Regime and Random Noise Regime Analysis

The distinct feature of the BBPD based PNF is the nonlinearity brought in the loop, invalidating the traditional Laplace domain analysis used in linear systems. Analogous to any quantized systems, like DPLL, the fundamental aspect of BBPD based PNF is the presence of limit cycles when there is no random noise [12]. It is well known that the limit cycles will degrade the phase noise floor of the system. Therefore, we analyze the limit cycle regime of this PNF in the first step.

2.1.2.1 Limit Cycle Regime

For the sake of simplicity, we assume the PNF has no divider, no voting machine. Figure 42 shows the block diagram of this simplified discrete PNF model. BBPD compares the rising edges of the D input (whose time instants is referred to as t_d) with those of the C input (whose time instants can be referred to as $t_{d,D1}$). The binary output ε of BBPD is mapped to a numerical value +1 if the D input leads the C input, otherwise it is mapped to -1 [13]. We can write:

$$\varepsilon = \text{sgn}(\Delta t), \quad \Delta t = t_d - t_{d,D1} - D_1 \cdot T_o \quad (16)$$

where Δt shows the time difference between the BBPD two inputs, D_1 represents the number of clock delays, T_o indicates the clock period. By subtracting the $D_1 T_o$, time instants of the D rising edge t_d and the C rising edge $t_{d,D1}$ will arrive at the same time if assuming no jitter. Note that α represents the CP gain coefficient and Ψ indicates the integration character of the capacitor that follows the CP. The other blocks, such as the LPF, are modeled by βz^{-D2} to express the gain and loop latency effects.

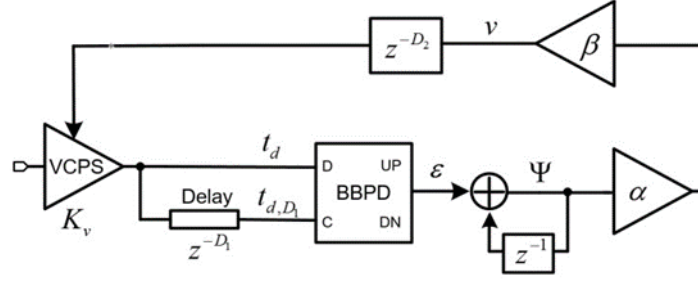


Figure 42: Block Diagram of the Simplified Discrete PNF Model

The VCPS is modeled as a linear block that provides the time shift of T_v depending on the feedback voltage v , which is given by:

$$T_v = -K_v \cdot v \quad (17)$$

where K_v is the time shift gain constant. In this model, we assume the response of the VCPS to a change of v is immediate without any transient behavior.

At the k -th clock cycle, the time occurrence t_d is adjusted by the time shift T_v in VCPS, according to the following:

$$t_d[k] = k \cdot T_o + T_v[k] \quad (18)$$

By combining the results so far achieved, the dynamics of the BBPD based PNF in Figure 43 can be described by the following set of equations (k indicates the k -th clock cycle in the PNF model):

$$\begin{cases} \Delta t[k] = t_d[k] - t_d[k - D_1] - D_1 \cdot T_o \\ \varepsilon[k] = \text{sgn}(\Delta t[k]) \\ \Psi[k] = \Psi[k - 1] + \varepsilon[k] \\ v[k] = \alpha \beta \cdot \Psi[k] \\ T_v[k] = K_v \cdot v[k - D_2] \\ t_d[k + 1] = t_d[k] - T_v[k] + T_v[k + 1] + T_o \end{cases} \quad (19)$$

By adding the last equation in (19) for D_1 times, then substituting it in (19), the dynamics above can be simplified to:

$$\begin{cases} \Delta t[k + D_1] = -\alpha\beta K_v \cdot (\Psi[k + D_1 - D_2] - \Psi[k - D_2]) \\ \Psi[k] = \sum_{x=0}^k \text{sgn}(\Delta t[x]) \end{cases} \quad (20)$$

The definition of the following quantity:

$$\lambda \triangleq \frac{\Delta t}{\alpha\beta K_v} \quad (21)$$

allows the set of equations to be rewritten in the form:

$$\lambda[k + D_1] = - \sum_{x=k+1}^{k+D_1} \text{sgn}(\lambda[x - D_2]) \quad (22)$$

The evolution of the system in time is dominated by the above nonlinear map. $\alpha\beta K_v$ is the quantization step of the VCPS, λ is the time difference Δt normalized to this quantization step.

In this system, we are interested in deriving the expression of the limit cycle period and the associated jitter. Indeed, once the operation trajectory of (22) is known, both properties can be evaluated. This will give insights into the nonlinear dynamics. Eq. (22) is discrete, and is hard to solve for directly. However, an observation of (22) reveals that the trajectory of $\lambda[x]$ will move in integer steps in either the positive or negative direction. $\lambda[x]$ cannot stay positive or negative all the time since the term $-\text{sgn}(\lambda[x])$ will invert it. Hence, the operation trajectory must be periodic with a cycle period $T\lambda$. However, the simultaneous presence of D_1 and D_2 in the map increases the difficulty of analyzing (22). As such, we decide to consider their effects separately by performing the analysis in three steps. In the first two step, D_1 and D_2 will assume to be equal to one independently, which is already the minimum acceptable value for them in (22). Then the third step removes the previous assumption.

First, we just take the case of $D_1 = 1$, thus (22) simplifies to:

$$\lambda[k + 1] = -\text{sgn}(\lambda[k - D_2]) \quad (23)$$

If the trajectory starts with a positive value, with $(1+D_2)$ iterations, the trajectory will reach a negative value. After another $(1+D_2)$ iterates, the trajectory will become positive again. This means that the trajectory is periodic with a period of $2(1+D_2)T_0$.

Similarly, we also consider the case of $D_2 = 1$, and the nonlinear map (22) reduces to:

$$\lambda[k + D_1] = - \sum_{x=k}^{k-1+D_1} \text{sgn}(\lambda[x]) \quad (24)$$

In (24), there are D_1 iterates of $\text{sgn}(\lambda[x])$ for each λ value. The trajectory will eventually reach a steady state. At that time, $\lambda[x]$ must be half positive and half negative within the D_1 iterations. Otherwise, the trajectory will move in one direction, and indefinitely stay in the positive or negative axes. As such, it is fair to assume this trajectory has a period of about $D_1 T_o$.

Lastly, the above results can be combined together, so that the overall orbit period T_λ is affected by D_1 and D_2 simultaneously. Therefore, it is reasonable to predict that T_λ is the sum of two terms. One term $2(1+D_2-1)T_o$ depends only on the loop latency D_2 . The other term $(D_1-1)T_o$ depends on the clock delay D_1 . In both terms, D_1 and D_2 need to minus one independently in order to compensate the effect of being one in (23) and (24). So we get $T_\lambda = (2D_2+D_1-1)T_o$.

To evaluate the validity of the predicted T_λ , we compute (22) with different D_1 and D_2 values based on two assumptions. First, the starting (D_1+D_2) iterations are meaningless, and $\lambda[x]$ will maintain the same value during this time. Therefore, we assume $\text{sgn}(\lambda[x]) = -1$ in the first (D_1+D_2) iterations. Second, $\lambda[x]$ may be equal to 0, so we suppose $\text{sgn}(0) = -1$. Computation results confirm that our prediction $T_\lambda = (2D_2+D_1-1)T_o$ is correct.

In the ideal case, the absolute time jitter is $\Delta t_d[k] = td[k] - k \cdot T_o$. Obtaining the cycle period T_λ is already enough to calculate the peak-to-peak quantization induced jitter ($\Delta t_{d,pp}$) as the difference between the maximum and the minimum values that Δt_d assumes in the orbit. Indeed, Δt_d is a linear response to ε , which is equal to $\text{sgn}(\lambda)$. With a triangular shaped trajectory, a worst-case estimate for the $\Delta t_{d,pp}$, can be derived as:

$$\Delta t_{d,pp} = \frac{T_\lambda}{2} \cdot \alpha\beta K_v = \frac{(2D_2 + D_1 - 1)T_o}{2} \cdot \alpha\beta K_v \quad (25)$$

In (25), $\Delta t_{d,pp}$ is already denormalized by multiplying $\alpha\beta K_v$ on the right hand. This is to evaluate the effects of PNF parameter variations on $\Delta t_{d,pp}$. The standard deviation of the quantization jitter is given by [14]:

$$J_q = \frac{\Delta t_{d,pp}}{\sqrt{12}} = \frac{(2D_2 + D_1 - 1)T_o}{4\sqrt{3}} \cdot \alpha\beta K_v \quad (26)$$

Eq. (26) reveals that the larger VCPS phase granularity ($\alpha\beta K_v$) leads to the larger quantization jitter J_q . Additionally, (26) suggests that quantization jitter increases as the clock delays D_1 , a parameter which cannot be reduced below a certain value for PNF noise sensitivity.

To further illustrate the dynamics of the PNF in limit cycle regime, a FM ST input is applied to simulate the ideal PNF model, which adopts the delay time $D_I T_o$ of about 20 ns. The FM signal is at 1 MHz offset frequency. The simulated CP output is plotted in Figure 43, and presents that BBPD is flipping with a period of about 41 ns.

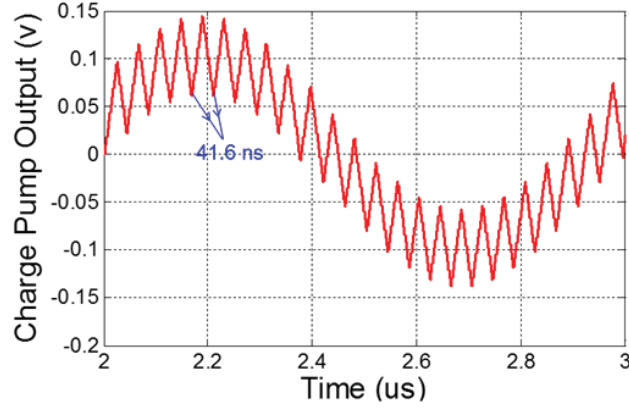


Figure 43: Simulated Waveform of the CP Output in the Ideal PNF Model with 1 MHz FM ST Input

2.1.2.2 Random Noise Regime

We have so far analyzed the BBPD based PNF neglecting the presence of any random noise sources. In practice, when the circuit noise is large enough, it acts as a dithering signal for the BBPD, which can be then linearized. This operation mode is referred to as the random noise regime [12]. The derivation of a linearized model of the BBPD has extensively been discussed in literature. For input signals around its threshold, the BBPD behaves as a linear block given that its averaged output is proportional to its input with a gain of [2]:

$$K_{BPD} \approx \frac{0.8T_{ref}}{2\pi\sigma_t} \quad (27)$$

Comparing with the gain of $(1/2\pi)$ in the conventional three-state PFD, the BBPD has a much larger gain. If assuming the root mean square (RMS) value of input jitter σ_t in the range of 0.5 ps or less, the BBPD gain is four orders of magnitude higher than the conventional PFD gain.

The other blocks in the loop are ideally linear and thus they can be described in the frequency domain. Now, the Laplace analysis can be adopted to get the PNF phase noise transfer function:

$$H_{PNF} = \frac{1}{1 + K_{VCPS} \cdot H_{DLL} \cdot K_{BPD} \cdot H_{BB} / M} \quad (28)$$

where K_{VCPS} is the gain of VCPS; M is the division ratio; H_{DLL} shows the transfer function of the DLL, while H_{BB} represents the transfer function of the baseband circuit blocks including the CP1, C1, and LPF. The CP1 current is adjustable to achieve different gain modes for H_{PNF} . The input and output signals of (13) are $\varphi_{n,in}$ and $\varphi_{n,out}$ respectively, which have been marked in

Figure 45. As mentioned earlier, HDLL has a high pass response, calculated as [23]:

$$H_{DLL} = \tau s \cdot \frac{s/\omega_p}{1 + s/\omega_p} \quad (29)$$

In (29), ω_p is a low frequency pole determined by the DLL tracking bandwidth, τ is the delay time. The input and output signals of (29) are $\varphi_{n_DIV, out}$ and $\varphi_{n_DLL, out}$ respectively. Together with the low pass filtering feature of the PNF main loop, the overall PNF open loop demonstrates a band-pass characteristic. Hence, the PNF close loop is able to suppress the input phase error within the band, as shown in Figure 44. The lower frequency boundary is determined by the DLL while the higher frequency corner comes from the LPF. A wider suppression band requires a higher corner frequency of the LPF. However, this may lead to a limited phase margin in the open loop. So the LPF must be designed carefully to guarantee both the suppression bandwidth and loop stability.

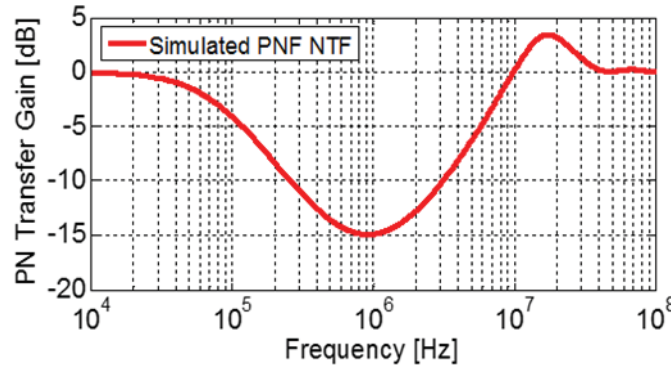


Figure 44: Simulated PNF Phase Noise Transfer Function

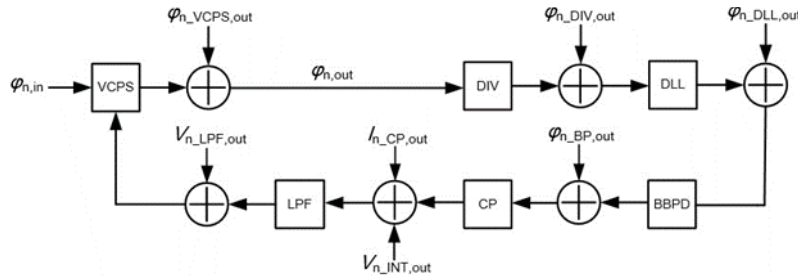


Figure 45: Linear Noise Model for PNF

The same method can now be applied to calculate the phase noise floor in the PNF with a linear noise model, as shown in Figure 45. It is one of the most important specifications, because it determines the best phase noise the PNF can achieve. Based on the derived noise transfer functions and the simulated output noise of each block, the PNF phase noise floor and major noise contributions are shown in Figure 46. It clearly presents that the BBPD contributes most of the noise. This makes sense because all noise sources after the BBPD can be minimized to a negligible level due to its large gain. Besides, through simulation, the VCPS, divider and delay line they all have very good phase noise. As a consequence, BBPD itself becomes the dominant noise source.

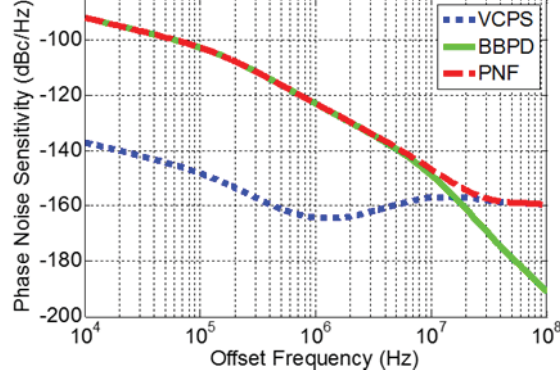


Figure 46: PNF Phase Noise Floor and Major Noise Contributions

The BBPD noise induced jitter is:

$$J_r \approx \frac{T_{ref}}{2\pi} \cdot \sqrt{2 \int_0^{\infty} \frac{S_{BPD}(f)}{|H_{DLL}(f)/M|^2} df} \quad (30)$$

where S_{BPD} represents the BBPD input noise power spectral density (PSD). Figure 46 leads us to the conclusion that a worthy effort in the PNF design is to minimize the BBPD noise so as to enhance the PNF noise sensitivity. This will be discussed in the next section.

In reality, the total output jitter J_o follows the sum of the two noise contributions, the quantization induced jitter and the random noise induced jitter [12], and can be expressed below under the premise that $\tau = D_1 T_o$:

$$J_o \approx \frac{T_{ref}}{2\pi} \cdot \sqrt{2 \int_0^{\infty} \frac{S_{BPD}(f)}{|2\pi f D_1 T_o / M|^2} df} + \frac{(2D_2 + D_1 - 1)T_o \cdot \alpha\beta K_v}{4\sqrt{3}} \quad (31)$$

Eq. (31) provides a few key observations. While the quantization induced jitter J_q grows as the number of clock delays D_1 , the noise induced jitter J_r decreases as D_1 . As such, the total jitter given by (31) can exhibit a minimum value. The optimum D_1 is found when the two terms on the right hand side of (31) are equal, or in other words when the jitter induced by quantization equals the jitter induced by random noise. In addition, a compromise must be made between the noise sensitivity and noise suppression, as noise sensitivity prefers a small VCPS phase granularity $\alpha\beta K_v$ while noise suppression prefers a large one. Besides, the loop latency D_2 should be kept small in order to minimize the quantization jitter.

2.1.2.3 BBPD PNF Implementation

2.1.2.3.1 Voting Machine

In last section, we already demonstrate that in the ideal case with no random noise, BBPD will flip with a constant cycle period so that the CP output has a saw-tooth shaped waveform. However, with the presence of random noise at the BBPD input, the saw-tooth waveform may be corrupted since undetermined decisions may appear at the BBPD output.

The working scheme of a BBPD is similar to that of a comparator. Consider a comparator with a certain input referred noise, denoted by its standard deviation σ_{input} . Due to this noise, the comparator has a certain output probability function, which logically means that the comparator makes error decisions when the input signal is close to σ_{input} . [15] indicates that when the same comparator is used several times to repeat the same decision, a majority voting logic can be applied on the obtained output samples to decide the final output. Using more samples increases the possibility that the majority decision is correct. In view of this, majority voting helps to scale down the comparator noise. Obviously, this approach can also be adopted to reduce the BBPD noise. However, it is hard to directly apply the technique in [15] to our PNF by using the BBPD several times to repeat the same decision, because the BBPD input is not a voltage signal, but a time difference signal. Currently, it is still challenging and power consuming to hold a time difference signal in circuit.

Fortunately, the unique feature of our PNF allows the employment of majority voting by holding previous BBPD decisions. In the ideal case, BBPD will maintain the same decision for the half cycle period, which is about 20 ns. Given the 1.25 GHz input frequency, BBPD can hold the same decision for at least 25 consecutive periods. This feature implies that one could minimize error by performing majority voting for several consecutive decisions. To better illustrate this working mechanism, a $5 \times$ voting scheme is taken as an example and is shown in Figure 47. The $(n+1)$ -th to $(n+4)$ -th decisions are all one (green signal), and the error bit zero (red signal) at the $(n+5)$ -th decision can be corrected by majority voting for the recent 5 decisions. The amount of noise reduction can be varied by applying different number of samples used to determine the majority decision. To intuitively present the effect on equivalent noise for different number of samples, Figure 48(a) illustrates the transfer curves of a transistor-level BBPD with different samples. This figure also indicates the statistical results of the equivalent noise in different voting scheme, as shown in Figure 48(b).

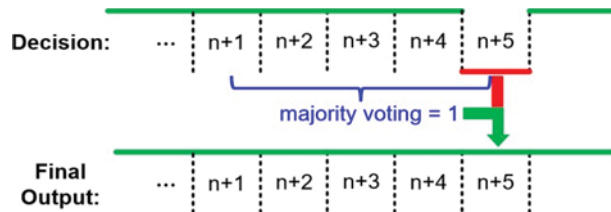


Figure 47: Work Diagram for a $5 \times$ Voting Scheme

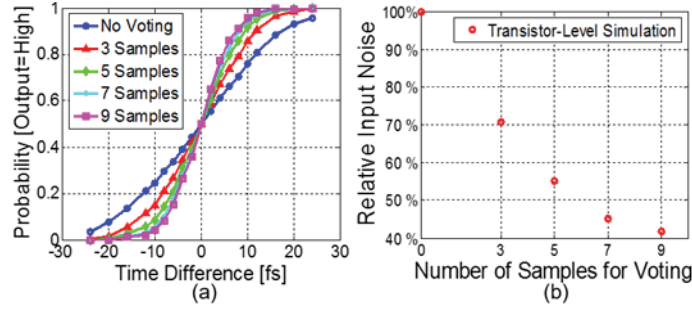


Figure 48: (a) Probability of BBPD Output as High vs. Input in different Voting Schemes and (b) Relative BBPD Equivalent Input Referred Noise vs. Number of Samples in the Voting Scheme

It presents that voting on 5 samples reduces the effective noise to about 55% of the original value. With more samples, the equivalent noise improvement slope is reduced. In addition, more samples also cause larger loop latency. As mentioned previously, large loop latency D_2 degrades the quantization induced jitter. Finally, we choose to use the $5 \times$ voting scheme as the optimum option, as shown in Figure 49. Four registers are employed to hold the previous 4 BBPD decisions, together with the latest one. All 5 samples are fed into the majority voting logic to decide the final output.

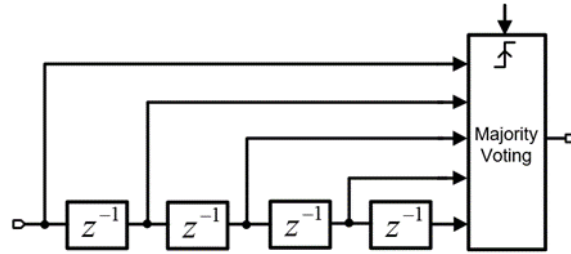


Figure 49: Block Diagram of the proposed $5 \times$ Voting Machine

If we deliberately add some small noise to the PNF model, the original saw-tooth like CP output will be corrupted. The top waveform in Figure 50 plots the simulated CP output in the noisy model without voting, while the bottom waveform in Figure 50 plots the CP output with the $5 \times$ voting scheme. It is clear that the corrupted saw-tooth waveform is partly recovered by the majority voting because of the reduced equivalent BBPD noise.

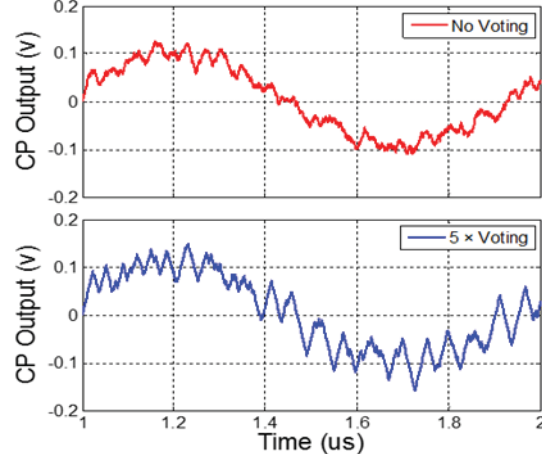


Figure 50: Simulated CP Output in the Noisy PNF Model without and with the $5 \times$ Voting Scheme

2.1.2.3.2 TA in BBPD

In order to further reduce the BBPD noise, the BBPD itself also requires careful design. Researchers typically adopt a DFF as BBPD. However, in high frequency applications, DFF may experience metastability and hysteresis effects, thereby generating undetermined outputs [16], and increasing the BBPD noise. So, to address this issue, a TA is included in the BBPD to enlarge the time difference to make the DFF work away from these regions. Figure 51(a) shows the schematic of the TA [17]. Over the years, many techniques have been published about TA with the focus on linearity [18][19], because TA is often employed in TDC to enhance its resolution by amplifying the time residue. Its accurate amplification gain is a key factor in this application. However, in our PNF, the design consideration for the TA was optimizing its noise performance, since extra noise in the BBPD is undesirable. In addition, there is no strict requirement for TA in terms of linearity since the proposed PNF is already a nonlinear system. In other words, our proposed design sacrifices the other performances, such as gain and linearity, to achieve a low noise TA for the PNF.

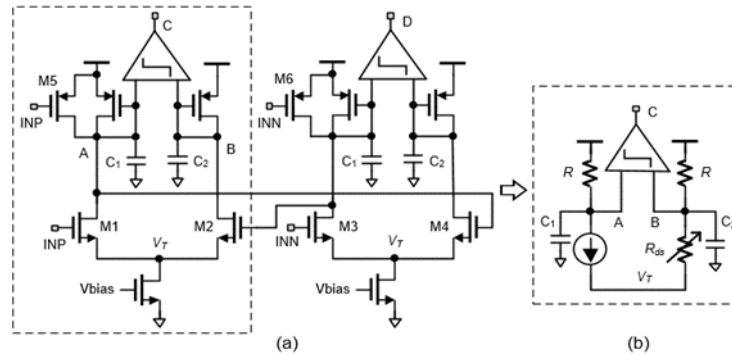


Figure 51: (a) Schematic of the TA and (b) Equivalent Model for the Left Side of the TA

The transient behavior of this TA is that upon the arrival of a rising edge at M1, a current impulse travels from the drain of M1 to the drain of M2. The comparator detects its input phase inversion [17]. To reset the TA every period, M5-M6 are employed. The circuit operation for the

left side of the TA can be approximated by the model depicted in Figure 51(b). Here, M1 is modeled as a current source, whereas M2 is modeled as a linear resistance R_{ds} . Also, the biasing current source is neglected since it is assumed that the traveled current impulse is larger than the tail current. For the sake of simplicity, our design applies the method in [20] to analyze the phase noise of node C in order to guide the low noise TA design.

The next simplifying assumption is that M1 operates in a similar way to the NMOS transistor in an inverter on the falling edge at the output. Moreover, as illustrated in Figure 51(b), the diode-connected PMOS transistor acts as a resistor, producing noise across C_1 . Hence, according to [20], the phase noise on the falling edge at node A is equal to:

$$S_A \approx \left\{ \frac{\pi^2}{s_r^2 C_1^2} [\Delta T f_{in} S_I(f) + \Delta T^2 f_{in}^2 S_{1/f}(f)] \right\} + \frac{\pi^2 f_{in}^2 \cdot 4kTR}{s_r^2} \quad (32)$$

where the first item on the right evaluates the M1 contributed phase noise, and the second item denotes the resistor induced phase noise from the diode-connected PMOS. Note that s_r presents the slew rate, ΔT denotes the duration time for the node transition, C_1 is the output load capacitance, $S_I(f)$ shows the active device thermal noise, $S_{1/f}(f)$ indicates the active device flicker noise and R is resistance of the diode-connected PMOS.

Similarly, the phase noise on the rising edge at node B is given by [20]:

$$S_B \approx \left\{ \frac{\pi^2}{s_r^2 C_2^2} [\Delta T f_{in} S_I(f) + \Delta T^2 f_{in}^2 S_{1/f}(f)] \right\} + \frac{\pi^2 f_{in}^2}{s_r^2} \cdot \frac{kT}{C_2 f_{in}} + \frac{\pi^2 f_{in}^2 \cdot 4kTR}{s_r^2} \quad (33)$$

where the second item on the right hand denotes the kT/C_2 noise from the resistor R_{ds} [20], and C_2 represents the load capacitance.

With the analysis developed above, we now seek to optimize the TA design for low noise. As can be seen from the ΔT in (32) and (33), the phase noise rises in proportion to the transition time ΔT . Therefore, the channel length of NMOS transistors must be the smallest since the longer channel inevitably raises transition time ΔT . Then we make several approximations: (a) device thermal noise spectrum $S_I(f) = 4kT\gamma g_m$, where $g_m = 2I_D/(V_{GS} - V_{th})$, I_D is the drain current and we have $I_D \propto W$ at the point of interest, where W represents the channel width of the transistor. So we get $S_I(f) \propto W$. Similarly, $S_{1/f}(f) = g_m^2 K/(C_{ox} W L f) \propto W$. (b) The slew rate $s_r \propto I_D/C_L \propto W/C_L$, where C_L represents the load capacitance. (c) The transition time window width, ΔT , is proportional to $1/s_r \approx C_L/W$ [20].

If assuming an ideal comparator, the overall phase noise of node C is proportional to the phase noise in node A and B, which are now rewritten as:

$$S_A(f) \propto \frac{C_1(\eta W + C_1)}{W^3}, \quad S_B(f) \propto \frac{C_2(\eta W + C_2)}{W^3} \quad (34)$$

An important point emerging from the above derivation is that low noise design of TA favors wide channel width NMOS transistors and small load capacitance. On the other hand, the PMOS and tail current have little effect on the TA noise. They only affect the DC operating point. However, enlarging the NMOS channel widths too much is not favorable, not only for the reason of power consumption but also due to the loading effect. Large load capacitance caused by the NMOS transistors would inevitably degrade the buffer phase noise.

To simulate the TA input referred phase noise, we embed the TA with a PFD/CP to run a Pnoise analysis, and deduce the phase noise from the CP output noise, as shown in Figure 52(a). To further illustrate the DFF noise reduction by the TA, transient noise simulations are also performed to compare the transition curves of TA + DFF and DFF, as illustrated in Figure 52(b). It is clear that the application of TA shrinks the DFF transition region because of the reduced equivalent noise.

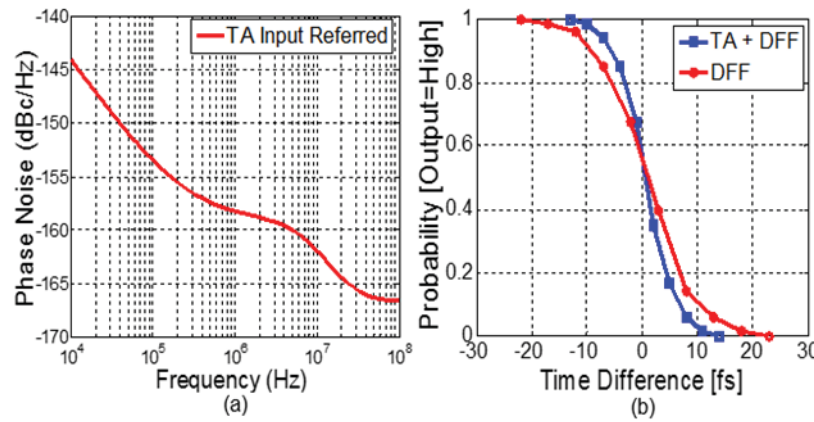


Figure 52: (a) Simulated Input Referred Phase Noise of TA and (b) Probability of TA + DFF and DFF Outputs as High vs. Input Time Difference

2.1.2.3.3 SAFF in BBPD

A sense-amplifier-flip-flop (SAFF) is chosen to realize the DFF in BBPD because it exhibits a good metastability among DFFs [21]. However, the conventional SAFF also suffers from hysteresis effect because any master-slave registers have a tendency to exhibit memory effect in the sampling process, thus negatively influencing the jitter performance [22]. As for the conventional SAFF, as shown in Figure 53(a), there is kickback effect from the SR latch in the slave stage to the master stage, leading to bad hysteresis. Therefore, to reduce the hysteresis of the conventional SAFF, modification can be made by inserting isolation between the two stages, as shown in Figure 53(b). The master stage is still a sense amplifier, but the slave stage changes from a SR latch to a cross coupled latch with an isolated stage. Clock for the slave stage is also delayed compared with the master stage.

To evaluate the hysteresis of the above SAFFs, transient noise simulations are also performed. The results are shown in Figure 54. It exhibits the conventional SAFF has hysteresis of about 90 fs, but hysteresis of the modified SAFF drops to 7 fs.

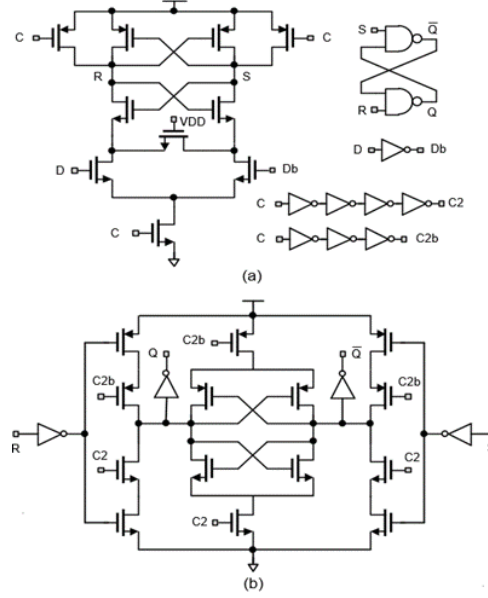


Figure 53: (a) Schematic of the Conventional SAFF and (b) Modified Slave Stage in the SAFF

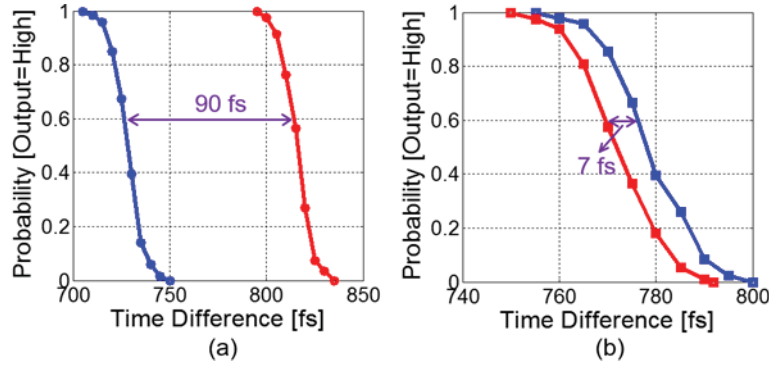


Figure 54: Transient Noise Simulation Results showing the Hysteresis of the (a) Conventional SAFF and (b) Modified SAFF

2.1.2.3.4 Voltage Controlled Phase Shifter

VCPS is a key block in PNF. The conventional passive phase shifters are not applicable in this design, because of the large insertion loss. For this reason, an active type VCPS with a cross-coupled pair is implemented [8], as shown in Figure 55. The phase of output voltage is shifted by adjusting the resonant frequency of the tank. The resonant tank is composed by an inductor, a 5-bit capacitor array and a varactor.

This resonant tank can be represented by a parallel of an inductor L , a capacitor C , and a resistor R . Its phase shift is realized by changing the capacitor value of the varactor or cap array. If the tank capacitor changed by $\pm\Delta C$, the tank impedance phase shift is calculated as

$$\Delta\phi(Z_{in}) = \mp R \cdot \Delta C / \sqrt{LC} \quad (35)$$

As can be seen from (35), the phase shift is proportional to the capacitor change. The cross-coupled pair (M1 and M2) is used as a Q booster to enhance the parallel tank resistance to generate large output.

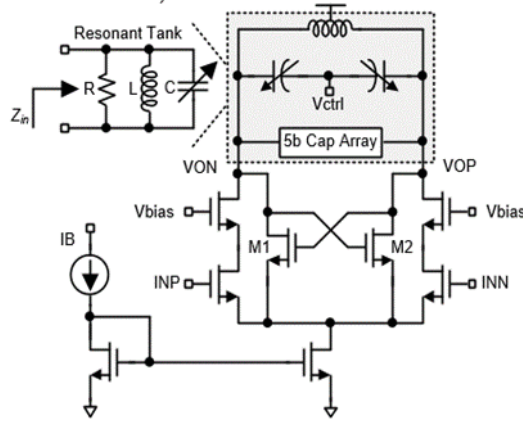


Figure 55: Schematic of the VCPS

2.1.2.4 Measurement Results

The proposed BBPD based PNF was fabricated in a 65 nm CMOS technology and the chip area is $1.77 \text{ mm} \times 1.48 \text{ mm}$. Figure 56(a) shows the die photo. A 20 ns off-chip delay line is adopted in the measurement. We have used two methods to test the noise suppression and noise sensitivity based on two input signals, one is the FM ST input, and the other one is the wideband noise input. Both PNF input signals are generated by the signal generator E8257D. After that, signal analyzer measures the PNF output spectrum. The feedback voltage (V_{ctrl}) to the VCPS is monitored by the oscilloscope. Figure 56(b) shows the power breakdown. Buffers before and after the DL consume 72% total power to drive the delay line.

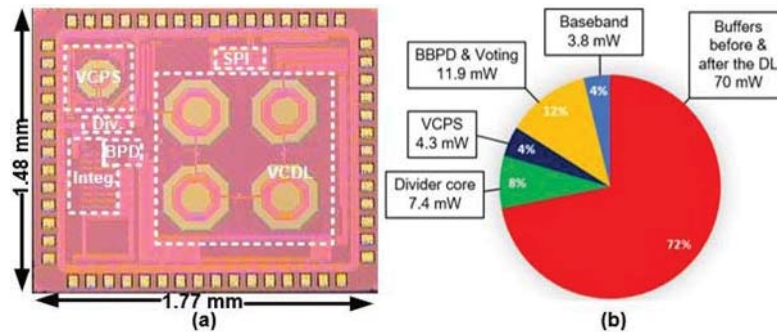


Figure 56: (a) Die Photo and (b) Power Breakdown

2.1.2.4.1 FM Input Measurement

A FM ST signal is applied to emulate the LO with phase noise at a given offset frequency. We first measure FM signal at 1 MHz offset. Figure 57 shows the 10.06 GHz FM input (red curve) and output (blue curve) spectra of PNF. It presents that the small and large phase noise suppression level is 15/23 dB respectively for the 10.06 GHz carrier at 1 MHz offset.

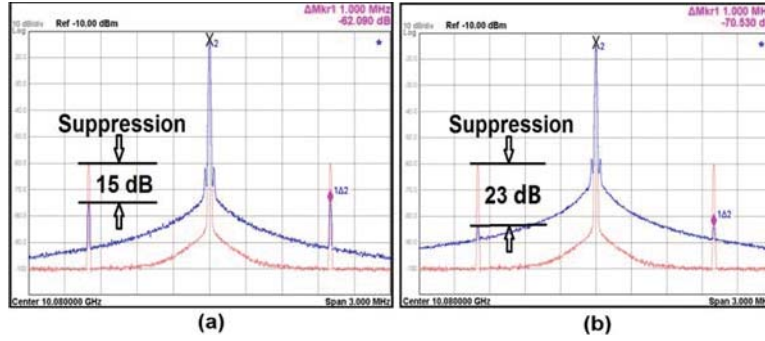


Figure 57: Input and Output Spectra of the PNF with the FM ST Input with (a) Small Suppression and (b) Large Suppression

The input signal is generated by the signal generator, which is of extremely good noise floor. The uplifted noise floor at PNF output is due to its own circuit noise. This illustrates that PNF's noise floor determines the best sensitivity it can achieve. If the input phase noise is already better than PNF's noise floor, there will be no noise suppression. In this case, input phase noise is only suppressed at 1 MHz offset frequency.

By sweeping the FM rate, we get the noise suppression bandwidth. Figure 58(a) plots the noise suppression level versus offset frequency at the two different gain modes. The suppression offset frequency is from 100 kHz to 8 MHz and the suppression level is 15/23 dB in the low/high gain mode at around 1 MHz offset, respectively. Figure 58(b) shows the noise suppression versus the input frequency at 1 MHz offset in low gain mode. Within the input frequency range of 10-10.1 GHz, the PNF has similar noise suppression level. Once out of the range, PNF will have no suppression for the reason that the DLL cannot lock anymore. This is limited by the tunability of VCDL. The blue waveform (V_{ctrl}) shown in Figure 59 indicates the 1 MHz FM information has been successfully extracted and feedback to VCPS. The purple waveform (VC_DC) in Figure 59 is almost constant, demonstrating the slow response of DLL.

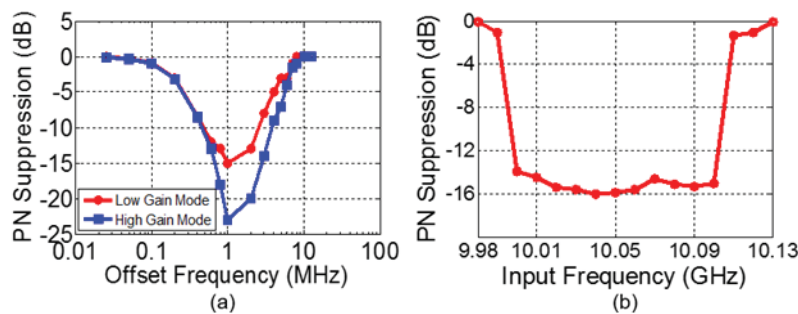


Figure 58: (a) Phase Noise Suppression vs. Offset Frequency in Low/High Gain Mode and (b) Phase Noise Suppression vs. Input Frequency

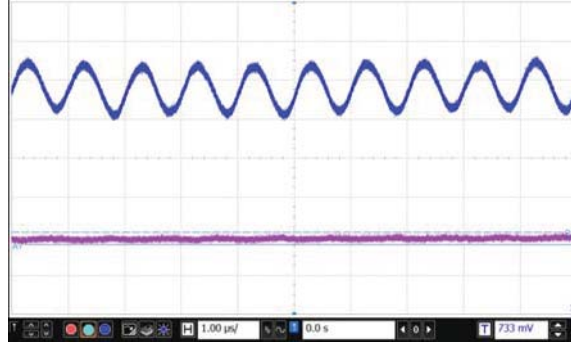
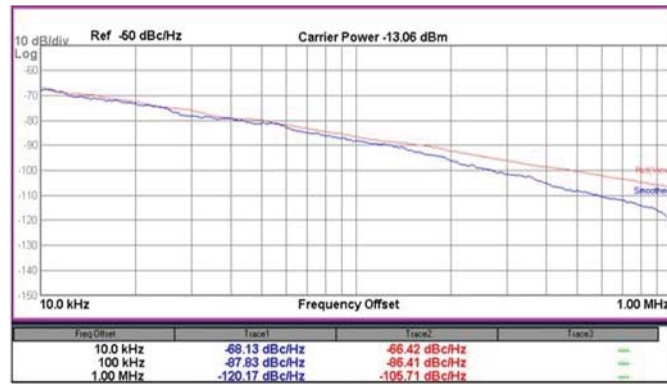


Figure 59: Measured V_{ctrl} and VC_DC waveform

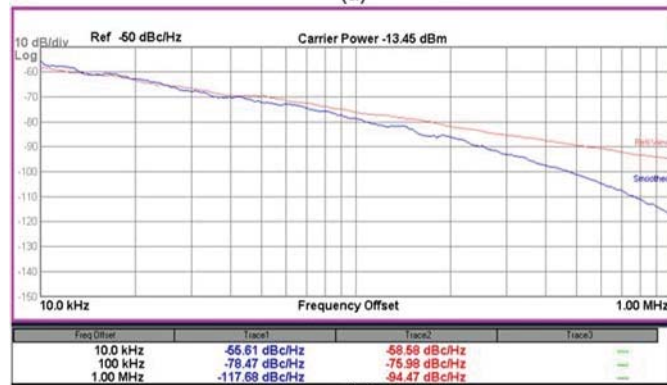
2.1.2.4.2 Wideband Noise Input Measurement

To further evaluate the PNF performance, the wideband noise input is also generated by the signal generator E8257D to test the noise suppression and sensitivity for the PNF. E8257D can only generate the wideband noise up to 1 MHz, which limits the highest offset frequency in the measurement.

Figure 60 shows the input and output phase noise curves in the low/high gain modes. Red curve represents the input phase noise while blue curve represents the output phase noise. In the low gain mode, PNF can suppress the input phase noise down to -120.2 dBc/Hz at 1 MHz offset with 14.5 dB noise suppression. In the high gain mode, PNF has a larger suppression of 23.2 dB at 1 MHz offset, but can only suppress the input down to -117.7 dBc/Hz. Although a larger CP current is adopted in the high gain mode to improve the noise suppression, this is at the cost of a worse noise floor. As can be seen from (28), a larger CP current in the main loop contributes to a smaller $|H_{PNF}|$. On the other hand, as illustrated in (31), larger CP gain coefficient α will also degrade the total output jitter due to the enlarged quantization induced jitter. It is known that the gain of BBPD may vary as the input phase noise profile varies. Hence, a measurement result with a large input noise in high mode is also given in Figure 61. This suppression is 3 dB smaller than that of Figure 60(b) due to the reduced BBPD gain.



(a)



(b)

Figure 60: Input and Output Spectra of the PNF with the Wideband Noise Input in (a) Low Gain Mode and (b) High Gain Mode

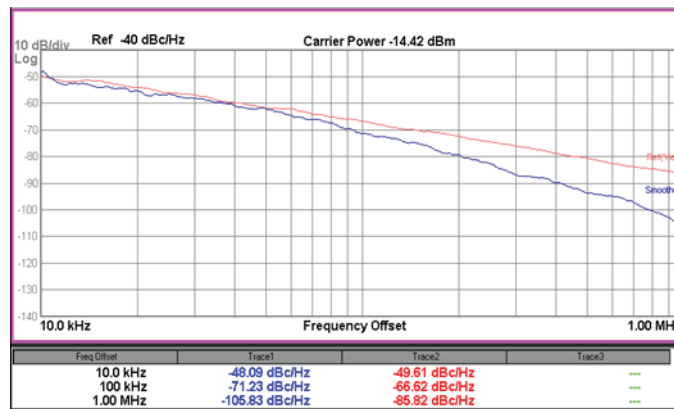


Figure 61: Input and Output Spectra of the PNF with a Large Wideband Noise Input in High Gain Mode

As mentioned, if injecting a clean carrier signal to the PNF, we can get the PNF noise floor from its output. Figure 62 illustrates the noise floor in low gain mode. The measured phase noise floor is -120 dBc/Hz at 1 MHz offset. This also explains why we cannot achieve better output phase noise in Figure 60. The integrated jitter in the suppression band (100 kHz – 10 MHz) is 81 fs.

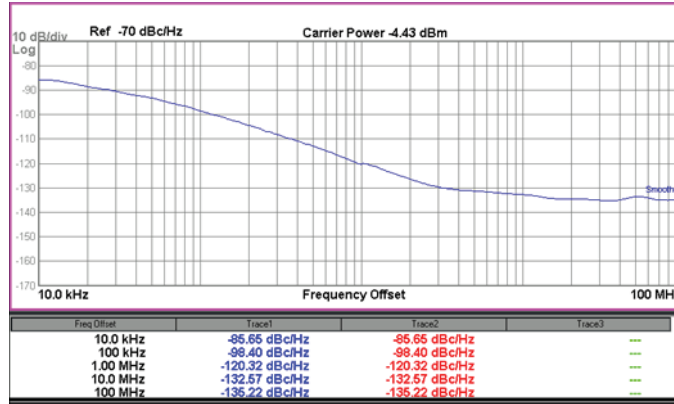


Figure 62: Phase Noise Floor of the PNF in Low Gain Mode

Table 7 summarizes the performance of the proposed PNF and compares with SOAs. Even though the -120 dBc/Hz at 1 MHz phase noise floor is a little worse than [6], the 100 MHz input bandwidth is much wider than that work. This work also exhibits the largest suppression among all works. Therefore, this PNF can be used as an individual block to suppress the phase noise of the LOs for performance boosting.

Table 7. Performance Summary and Comparison with SOAs

	[6] TMTT 2015	[5] RFIC 2012	[8] IMS 2016	This work
Center Frequency	1.5 GHz	5 GHz	10 GHz	10 GHz
Delay Line	Off-chip high Q FBAR	On-chip active inverter	On-chip delay line+ off-chip SAW filter	On-chip delay line+ off-chip SAW filter
Phase Detector	Mixer	Mixer	PFD	BBPD
Input Bandwidth	< 5 MHz ^a	3.1-7.5 GHz	117 MHz	100 MHz
Need Reference Clock	no	yes	no	no
PN @ 1 MHz (Convert to 10 GHz)	-124 dBc/Hz	-99 dBc/Hz	-116 dBc/Hz	-120/-118 dBc/Hz ^b
PN Suppression @ 1 MHz	n/a	12.5 dB	10.6 dB	15/23 dB ^b
Power Consumption	350 mW	29.6 mW	102 mW	98 mW
Technology	0.13 um	90 nm	65 nm	65 nm

a. estimated from paper

b. with low/high gain mode

4.2f

2.1.3 2nd Version: Digital PNF

2.1.3.1 Architecture

Figure 63 depicts the block diagram of the digital phase noise filter (DPNF), which consists of a digital-controlled-phase-shifter (DCPS), a divider, a TA-TDC type FD and baseband digital blocks. The delay line in FD converts the absolute phase noise into the relative phase difference. Then the TA-TDC detects the phase difference and drives its digital output into a digital loop filter (DLF). Finally, the DLF output Dctrl controls the DCPS in a negative feedback loop to achieve the required phase shifting.

2.1.3.1.1 Delay-Locked Loop

An off-chip SAW filter is used to provide a long delay time about 20 ns, while the tunable on-chip VCDL is employed in a DLL to align the two TA-TDC inputs. Unlike the conventional DLLs, the output of this DLL is the phase difference in front of TA-TDC. It is worth noting that this DLL requires a very small tracking bandwidth, which ensures any sudden jitter of the input clock appears at this DLL output before the loop reacts and reaches a new steady state. That is, this DLL is a first-order high-pass system. Figure 63 also shows the overall DPNF phase noise transfer function. The lower suppression boundary f_1 is determined by the DLL while the high boundary f_2 comes from the LPF in DCPS.

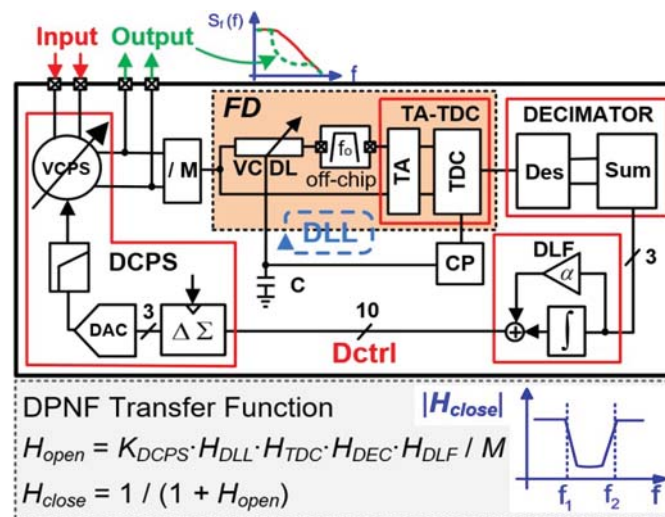


Figure 63: DPNF Block Diagram and Phase Noise Suppression Concept

2.1.3.1.2 Proportional Path in Feedback Loop

By using the TA-TDC in place of a PFD/CP or a mixer, the CP noise or mixer noise that limits the FD sensitivity is eliminated. Furthermore, the limit cycle behavior that constrains the quantized system is greatly suppressed by the TA-TDC. However, when the input phase noise is too small, the TA-TDC still work similarly as a DFF and brings limit cycles. For this reason, the DLF is optimized to minimize the limit cycle effect in this condition. In conventional phase noise cancellation systems [1, 2, 3], the phase detector output is integrated first, and then fed into the phase shifter to compensate the input phase noise. This introduces a long delay in the integration path. To reduce the cycle period for a small quantization jitter, a proportional path is proposed to combine with the integration path. In the proportional path, the TA-TDC output directly transmits to the DCPS, thereby increasing the DFF flip rate. In other words, the integration path behaves as a main loop to generate the feedback signal for the DCPS. The proportional path acts as a supplementary loop, delivering a small portion of the TA-TDC output to the DCPS earlier to reduce the cycle period, thus reducing the quantization induced jitter. Figure 64 presents the simplified DPNF model in this condition. For the sake of simplicity, we assume there is no divider. D_1 represents the number of clock delays in the delay line, D_2 denotes the loop latency equivalent delay, and T_o indicates the clock period. Based on the loop dynamics, the cycle period with the integration path only is $T_i = (2D_2 + D_1 - 1) \cdot T_o$ and the cycle period with the proportional

path only is $T_p = (D_2 + D_1 - 1) \cdot T_o$. The behavior model simulation reveals that cycle period T_λ can reduce from 60 ns to 40 ns if combined with the proportional path, as shown by the DLF output in Figure 64.

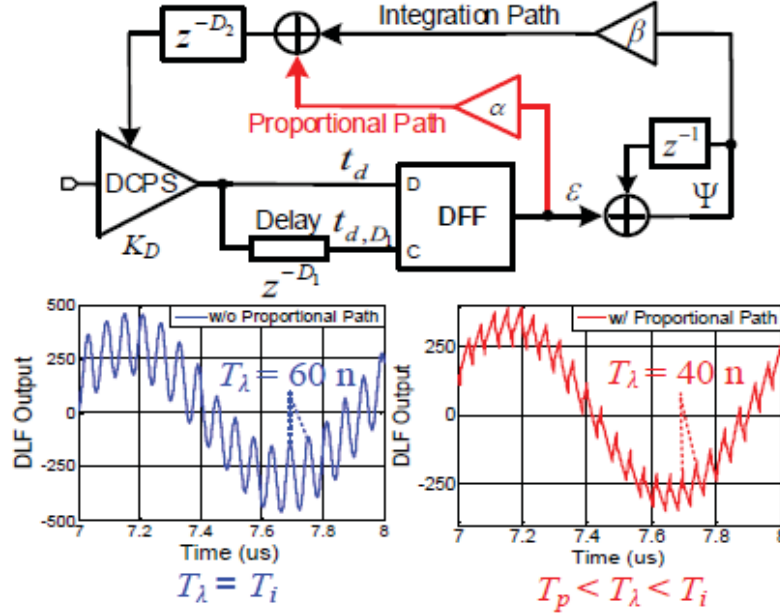


Figure 64: Simplified DPNF Model and DLF Outputs without and with the Marked Proportional Path

2.1.3.2 Circuit Implementation

2.1.3.2.1 TA-TDC

The TA-TDC shown in Figure 65(b) is implemented by using a TA that amplifies the input time difference with a gain of K_{TA} and a sub-gate delay TDC that digitizes the TA output into 2 bits. The DFF is realized by a sense-amplifier-flip-flop because it exhibits a small metastability. The required resolution of TDC is below the gate delay supported by the 65 nm process, thus does not allow implementing the TDC as a cascaded delay line. To achieve the sub-gate resolution, switchable capacitors are added at the output of each buffer to linearly scale the delay of each buffer from $(\tau_0 + \Delta\tau)$ to $(\tau_0 + 3\Delta\tau)$, where $\Delta\tau$ is the TDC resolution (about 3 ps in this design). The resolution for the entire TA-TDC equals to $\Delta\tau / K_{TA}$. The TDC quantization noise is also suppressed by its gain factor K_{TA} . The TA shown in Figure 65(a) is similar to the $2 \times$ gain stage reported in [4]. Different from the TA employed in [4] to amplify the time residue, whose key factor is the accurate gain. The key TA design consideration in this work is the noise performance, because the TA noise is one determine factor of the DPNF phase noise sensitivity. The total phase noise of TA is given by the sum of node A, B phase noise and inverter phase noise. If evaluated for only the rising edge at the output, the TA phase noise is governed by the expression [5]:

$$S_{\phi}(f) \propto \frac{2C_L(W_{1N} + C_L)}{W_{1N}^3} + \frac{C_L(W_{2N} + C_L)}{W_{2N}^3} + \frac{2C_L}{W_{1P}^3} \quad (36)$$

where W_{1N} , W_{2N} and W_{1P} represent path1 nch width, path2 nch width and path1 pch width respectively. C_L is the load capacitance of node A and B. Based on the expression, the optimum nch channel width ratio between path 1 and path 2 is about 1.25 : 1. Device actual size choice is subject to the power consumption budget due to its linear proportional relation to the device width.

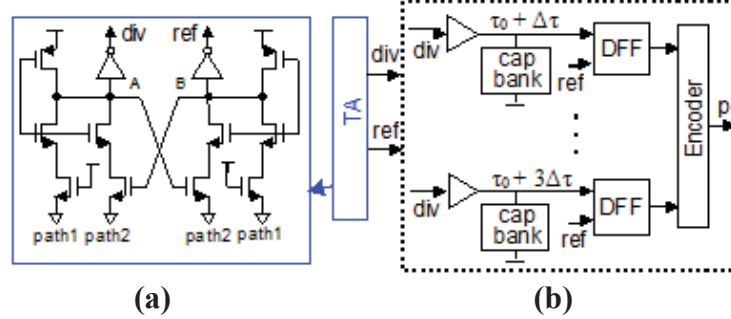


Figure 65: (a) Schematic of the TA and (b) TA-TDC Block Diagram which consists of a TA and a Sub-gate TDC

2.1.3.2.2 DLF and DCPS

The digital integrator in the conventional DLF usually comes with a large gain in the low frequencies. However, enormous DLF gain would greatly amplify the TA noise and thus degrade the DPNF noise floor at low offset frequencies.

For this reason, top 4 bits are deliberately subtracted from the integrator feedback loop to maintain a flat gain at the low frequencies, as shown in Figure 66(a). Therefore, the integration path gain is changed to:

$$H_{NT} = \frac{Z^{-1}}{1 - (1 - 2^{-7}) \cdot Z^{-1}} \quad (37)$$

4 bits is optimized to achieve both low offset frequencies gain and sufficient 1 MHz frequency gain. Figure 66(b) compares the integration path gain with and without the feedback loop subtraction.

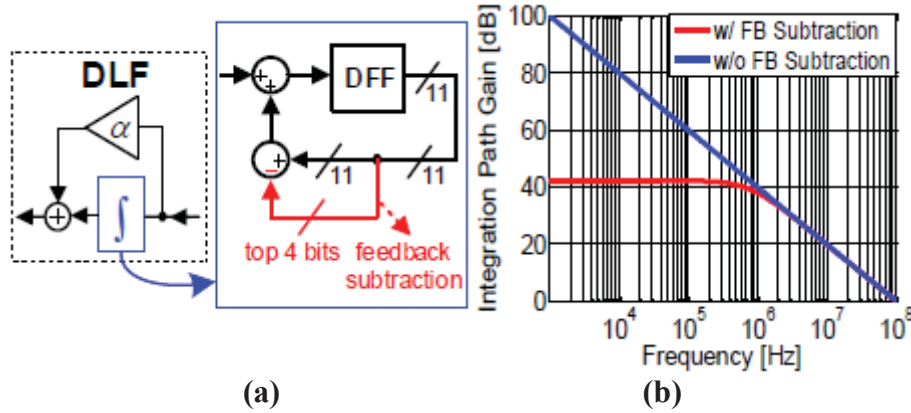
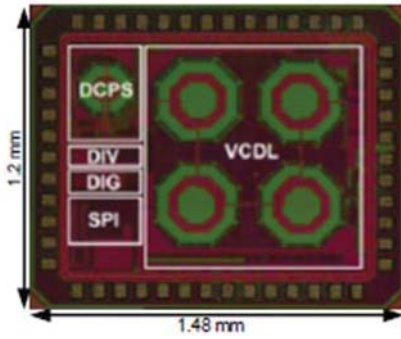


Figure 66: (a) Integration Path with the Feedback Subtraction inside the DLF and (b) Integration Path Gain Comparison with and without the Feedback Subtraction

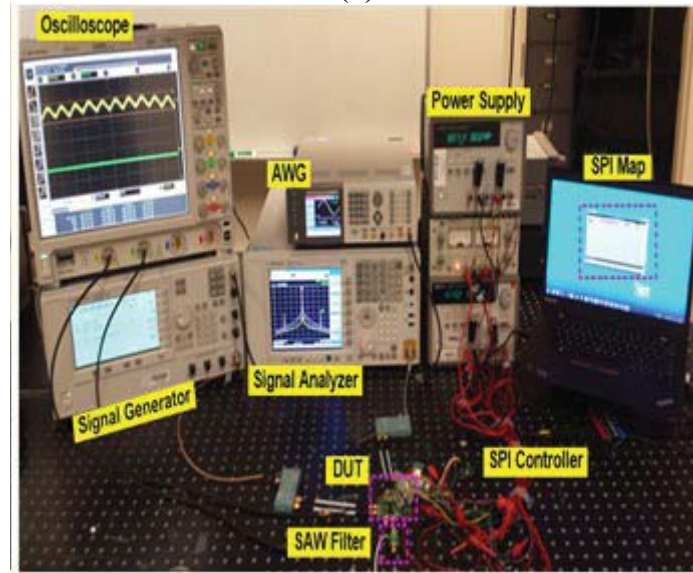
The DCPS also presents its own design challenges in achieving low quantization noise. In this work, we exploit a hybrid DCPS approach which combines a DAC and a VCPS [3]. A first order $\Delta\Sigma$ modulator truncates the 10 bit word to control the 3 bit thermometer coded DAC, whose output passes through a low pass filter before reaching the VCPS. Fortunately, the modulator dynamic range requirement is much looser compared to the ones applied in DPLL. This is because the phase noise cancellation in VCPS does not need a large bias voltage, especially in the case of dealing with low phase noise inputs. Accordingly, the full scale modulator output is optimized to 100 mV to minimize its quantization noise. This guarantees both negligible noise contribution to the DPNF output and sufficient phase noise suppression, about 30 dB by model simulation.

2.1.3.3 Measurement Results

Figure 67 shows the die photo and test bench photo. To measure the phase noise suppression of the DPNF versus offset frequency, a single-tone FM signal is injected as the DPNF input. For example, a 1 MHz modulated single-tone signal is applied as DPNF input to emulate the LO with phase noise at 1 MHz offset frequency. The signal analyzer panel in Figure 68(a) presents the input (red curve) and output (blue curve) spectra of the DPNF. The noise suppression is 14/22 dB in the low/high gain mode respectively. The uplifted noise floor at DPNF output is due to its own noise, which is higher than the ultra-clean spectrum analyzer N9020A noise floor. By sweeping the FM rate of the input, we measured the noise suppression bandwidth, 40 kHz to 8 MHz, as shown in Figure 68(b).



(a)



(b)

Figure 67: (a) Die Photo and (b) Test Bench Photo

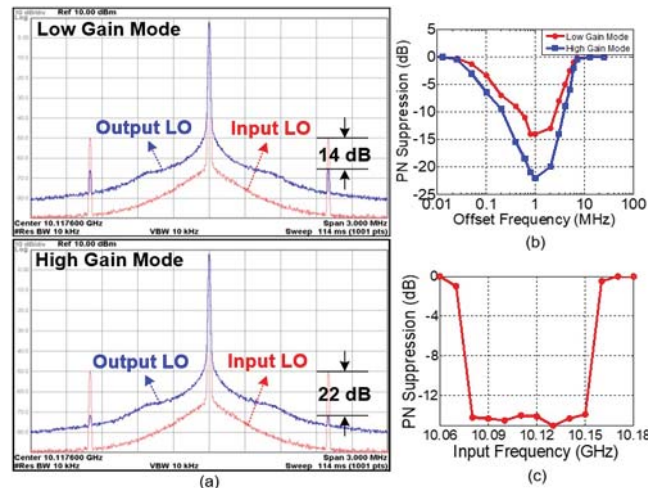
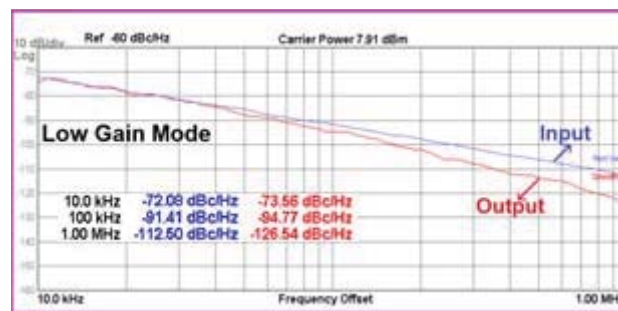


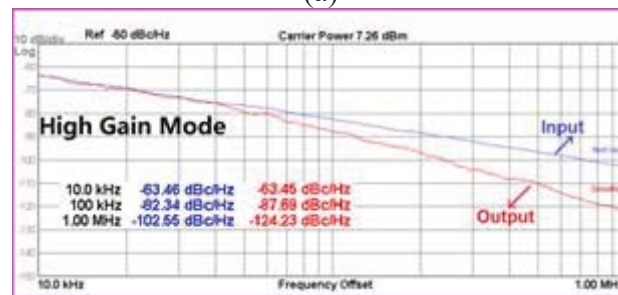
Figure 68: (a) Input and Output Spectra of the DPNTF with the 1 MHz Modulation Input in Low/High Gain Mode, (b) Phase Noise Suppression vs. Offset Frequency in Low/High Gain Mode, and (c) Phase Noise Suppression vs. Input Frequency

Within the input range of 10.07 – 10.15 GHz, the DPNF has similar noise suppression levels. To further evaluate the DPNF performance, a signal with wideband noise is also generated by the signal generator E8257D as the input. But E8257D only generates noise up to 1 MHz, which consequently sets the limit of the highest measureable offset frequency.

Figure 69 shows the input (blue curve) and output (red curve) phase noises of the DPNF in the low/high gain mode. The suppression band starts from 40 kHz, consistent with the single-tone FM measurement in Figure 68. In the low gain mode, the input phase noise of -112.5 dBc/Hz is suppressed down to -126.5 dBc/Hz with 14 dB suppression. In the high gain mode, DPNF has a larger suppression of 22 dB. Figure 70 also illustrates the DPNF noise floor by injecting a clean LO. The measured phase noise floor is -127 dBc/Hz at 1 MHz offset. This explains why the input phase noise of -112.5 dBc/Hz in Figure 69(a) cannot be suppressed to a lower level. The integrated jitter (10 kHz – 100 MHz) is 81 fs.



(a)



(b)

Figure 69: Input and Output Phase Noise of the DPNF with the Wideband Noise Input in (a) Low Gain Mode and (b) High Gain Mode



Figure 70: Phase Noise Floor of the DPNF

Table 8 presents the performance comparison with SOAs. The noise sensitivity of -127 dBc/Hz at 1 MHz offset for a 10.1 GHz clock is better than existing CMOS phase noise suppression systems based on the authors' best knowledge. Compared with FBAR based approach [1], the work demonstrates a much wider input bandwidth with a fractional power consumption.

Table 8. Performance Summary and Comparison with SOAs

	JSSC 2010 [7]	TMTT 2015 [1]	JSSC 2013 [2]	TMTT 2017 [3]	JSSC 2017 [6]	This work
Design Type	All Digital PLL	PN Suppression System	PLL with PN Suppression	PN Suppression System	PLL + PN Suppression	PN Suppression System
Center Frequency	10 GHz	1.5 GHz	5 GHz	10 GHz	1.2 GHz	10.1 GHz
Delay Line	n/a	Off-chip high Q FBAR	On-chip active inverter	On-chip delay line+ off-chip delay line	On-chip active inverter	On-chip delay line+ off-chip delay line
Phase Detector	n/a	Mixer	Mixer	PFD/CP	Phase Aver	TDC
Tuning Range	9.8 – 1.2 GHz	< 5 MHz ^a	3.1-7.5 GHz	117 MHz	n/a	80 MHz
Need Reference Clock	yes	no	yes	no	yes	no
PN @ 1 MHz (10 GHz)	-100 dBc/Hz	-124 dBc/Hz	-99 dBc/Hz	-116 dBc/Hz	-96 dBc/Hz	-127/-124 dBc/Hz ^b
PN Suppression @ 1MHz	n/a	n/a	12.5 dB	10.6 dB	5 dB	14/22 dB ^b
Integrated Jitter	1.1 ps (50 kHz – 80 MHz)	76 fs (10 kHz – 40 MHz)	3.8 ps (10 kHz – 10 MHz)	176 fs (10 kHz – 100 MHz)	1.48 ps (100 kHz – 100 MHz)	81 fs (10 kHz – 100 MHz)
FOM^c (dB)	-237	-236.9	-213.7	-235	-223.6	-245
Core Area (mm²)	0.97 * 0.93	2 * 3	0.32 * 0.38	1.5 * 1.68	0.6	1.2 * 1.48
Power Consumption	7.1 mW	350 mW	29.6 mW	102 mW	19.8 mW	53 mW
Technology	90 nm	0.13 um	90 nm	65 nm	65 nm	65 nm

a. estimated from paper b. with low/high gain mode c. FOM = 20log(Integrated Jitter) + 10log(Power/1mW)

3. References

3.1 References for First Category: Linear PNF

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List of Acronyms, Abbreviations, and Symbols

ACRONYM	DESCRIPTION
AC	alternating current
ADC	analog-to-digital converter
BB	baseband
BBPD	bang-bang phase detector
BER	bit-error-rate
CM	common mode
CML	current mode logic
CMOS	complementary metal-oxide-semiconductor
CP	charge pump
DAC	digital-to-analog converter
DC	direct current
DCOC	direct current offset cancellation
DCPS	digital-controlled-phase-shifter
DFF	delay flip-flop
DL	delay line
DLF	digital loop filter
DLL	delay-locked loop
DPNF	digital phase noise filter
EVM	error vector magnitude
FBAR	film bulk acoustic resonator
FD	frequency discriminator
FM	frequency modulated
FOM	figure of merit
high-Q	high quality factor
LNTA	low noise time amplifier
LO	local oscillator
LPF	low pass filter
NTF	noise transfer function
PCB	printed circuit board
PD	phase detector
PFD	phase frequency detector
PLL	phase-locked loop
PN	phase noise
PNF	phase noise filter
PSD	power spectral density
RBW	resolution bandwidth
RF	radio frequency
RMS	root mean square
SAFF	sense-amplifier-flip-flop
SAW	surface acoustic wave
SOA	state-of-the-art
ST	single tone
TA	time amplifier

ACRONYM	DESCRIPTION
TAPNF	time amplifier enhanced phase noise filter
TDC	time-to-digital converter
TSPC	true single-phase clocking
VCDL	voltage controlled delay line
VCPS	voltage controlled phase shifter
V_{ctrl}	control voltage
VGA	variable gain amplifier