CHARACTERIZATION FOR THE DEVELOPMENT OF THE HYBRID MULTI-JUNCTION SILICON GERMANIUM SOLAR CELL

THESIS

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Abstract

Based on the previous development of the hybrid multi-junction silicon (HMJ-Si) solar cell, this work characterized the preceding design for the development of the hybrid multi-junction silicon germanium (HMJ-SiGe) solar cell. Seven focus areas were investigated: diffraction pattern generation, photon propagation, silicon diffusion processing, ohmic contacts, the distributed Bragg reflector (DBR), the Fresnel zone plate (FZP), and the germanium/germanium telluride (Ge/GeTe) pn-junction Diffraction patterns were theoretically examined, and contact grating design characterization for reflectance and transmittance properties was modeled using rigorous coupled wave analysis. An improved silicon diffusion process follower was developed, and theoretical study and experimental assessment were accomplished for appropriate ohmic contacts, the DBR, the FZP, and the Ge/GeTe pn-junction for incorporation into the HMJ-SiGe solar cell architecture. Results showed that minima locations are nonexistent, the ratio between the metal width and electrical contact spacing is vital, an interfacial layer is required for Fermi level de-pinning, the DBR can reject detrimental wavelengths, the FZP excessively prevents transmittance, and p-type GeTe can form a pn-junction on n-type germanium. With an average efficiency of 1.27%, the HMJ-SiGe solar cell demonstrated a capstone requirement of charging a capacitor to 2.5 VDC in 11 minutes to illuminate a light emitting diode.

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A	Area	k	Boltzmann constant
α	Absorption coefficient	λ	Wavelength
c	Speed of light	λ_0	Target wavelength
°C	Degrees Celsius	ln	Natural logarithm
cm	Centimeter	L_n	Diffusion length minority carrier electrons
d_{ARC}	Thickness of anti-reflective coating	L_p	Diffusion length minority carrier holes
D_n	Diffusion coefficient of minority carrier electrons	m	Ideality factor
D_p	Diffusion coefficient of minority carrier holes	m^2	Meters squared
eV	Electron-volts	M_{pp}	Maximum power point
E_c	Conduction band energy level	n_{AIR}	Refractive index of air
E_f	Fermi energy level	n_{ARC}	Refractive index of ARC
E_g	Band gap energy level	n_H	High refractive index
E_{ph}	Photon energy	n_i	Intrinsic carrier concentration
E_0	Vacuum energy level	n_L	Low refractive index
E_v	Valence band energy level	nm	Nanometer
FF	Fill factor	n_{semi}	Refractive index of semiconductor
h	Planck's constant	N_A	Acceptor concentration
I	Current	Nc	Effective density of states for the conduction band
I_s	Saturation current	N_D	Donor concentration

I_{sc}	Short-circuit current	N_V	Effective density of states for the valence band
Ω	Ohm	T	Temperature
Ω/□	Ohms per square	τ_n	minority carrier lifetime of electrons
P_{in}	Input power	τ_p	Minority carrier lifetime of holes
ϕ_B	Barrier height	V	Volts
ϕ_M	Metal work function	V_{oc}	Open-circuit voltage
ϕ_S	Semiconductor work function	V_T	Thermal voltage
q	Electron charge	x_p	Penetration depth
R_{pad}	Metal pad resistance	χ_s	Semiconductor electron affinity
R_{semi}	Semiconductor resistance	W/m^2	Watts per meter squared
ρ_c	Contact resistivity		

List of Acronyms

AFIT	Air Force Institute of Technology
a-GeTe	Amorphous germanium telluride
Al_2O_3	Aluminum Oxide
AM	Air mass
ARC	Anti-reflective coating
a-Si	Amorphous silicon
BSF	Back surface field
c-GeTe	Crystalline germanium telluride
DBR	Distributed Bragg reflector
E-beam	Electron beam
EBSF	Enhanced back surface field
EHP	Electron-hole pair
FZP	Fresnel zone plate
$GaInP_2$/GaAs/Ge	Gallium indium phosphide/gallium arsenide/germanium
Ge/GeTe	Germanium/germanium telluride
GPIB	General purpose interface bus
HMJ-Si	Hybrid multi-junction silicon
HMJ-SiGe	Hybrid multi-junction silicon germanium
I-V	Current-voltage
LIGA	Lithographie, Galvanoformung, and Abformung
MEMS	Microelectromechanical system

MS	Metal-to-semiconductor
NREL	National Renewable Energy Laboratory
P_2O_5	Phosphorus pentoxide
PECVD	Plasma enhanced chemical vapor deposition
$POCl_3$	Phosphorus tricloride oxide
PV	Photovoltaic
RCWA	Rigorous coupled-wave analysis
RF	Radio frequency
Si_3N_4	Silicon nitride
SiO_2	Silicon dioxide
TMM	Transfer matrix method
UV	Ultraviolet
VI	Virtual instrument

I. INTRODUCTION

1.1 The Need and Response of Solar Cells

It is common knowledge that non-renewable resources, like crude oil, natural gas, and coal, are finite resources, and the nations of this world will desperately need to turn to alternative sources to satisfy and sustain their requirements for energy consumption. In fact, it is apparent that as national economies increase so does their need for energy, and this positive trend is forecasted to increase quickly into the foreseeable future- "…the total world consumption of marketed energy is projected to increase by 44% from 2006 to 2030…" [1]. Therefore, it is critical that the leading economies of the world need to accelerate development of reliable and efficient alternative (or at the very least supplemental) energy resources.

The answer to this unavoidable global calamity is to invest, focus, and develop effective technologies that utilize renewable and virtually unlimited energy resources. Photovoltaics is one such promising technology that use a minuscule fraction of the vast amounts of energy provided to the Earth by the Sun. Sunlight is a nearly limitless resource that far exceeds the energy needs of the entire world. Authors Steven Hegedus and Antonio Luque conveyed it this way:

> *As matter of fact the amount of energy arriving on Earth from the Sun is gigantic: in the range of 10000 times the current energy consumption of the human species... Using photovoltaics with an efficiency of 10%, solar energy can be converted directly into enough electricity to provide 1000 times the current global consumption. Restricting solar collection to the*

earth's solid surface (one quarter of the total surface area), we still have the potential of 250 times the current consumption. This means that using 0.4% of the land area could produce all the energy (electricity plus heat plus transportation) currently demanded. [2]

Fortunately, solar cell technology research, development, and manufacturing have substantially increased over the years. Since early 2000 "the total installed capacity of solar based electricity generation capacity has increased to more than 40 GW by the end of 2010 from almost negligible capacity in the early nineties" [3]. In the 2012 SunShot Vision Study executive summary based on specific target pricing, the Department of Energy projected U.S. installations of 302 gigawatts of photovoltaics by the year 2030 and 632 gigawatts by the year 2050 [4]. These statistics are a testament to the academic vigor in the study and advancement of photovoltaic technologies. In fact, in a journal article of *Renewable Energy*, corresponding author Francesco Rizzi stated that out of the 5 renewable energy source categories researched (biomass, geothermal, hydro, solar, and wind), it was solar that yielded the most number of publications contributing to scientific knowledge, which is most likely due to the use of this technology worldwide [5].

1.2 Solar Cell Efficiency

One of the driving factors of continual research and production decision-making for mass manufacturing is the efficiency of the solar cell, which directly affects the overall cost. It is obvious that any cost-conscience consumer wants more

"bang for the buck." Therefore, scientists and engineers have a strong desire to increase the solar cell efficiency has much as possible while developing fabrication and manufacturing methods that can lower the cost of production as much as possible. There are many technological recipes (e.g. single-junction, multi-junction, thin-film, organic, etc.) that can be employed to produce a solar cell, and each promising technique has its potential for increasing the efficiency of solar-to-current conversion. According to a line graph chart entitled "Best Research-Cell Efficiencies" from the National Renewable Energy Laboratory (NREL) website for the National Center for Photovoltaics, the current record for the solar cell technology having the best research-cell efficiency is a 2 terminal, monolithic four-junction cell with a concentrator- 46.0% [6]. This is a dramatic leap from the average best research-cell efficiencies in various listed crystalline silicon cell techniques of about 24% [6].

Although silicon has been the traditional semiconductor of choice for solar cell design, germanium has become increasingly popular. Some of its attractive properties include absorption in the infrared region [7, 8, 9] and increased mechanical strength over gallium arsenide [10]. Germanium is typically used in triple-junction space solar cell applications, but efforts have been made to cost-effectively manufacture them for terrestrial use with expected post-production efficiencies close to 40% [11].

However, these percentages represent record results accomplished in a lab setting and may be expected to negatively if put to mass production. Nevertheless,

the NREL chart illustrates the potential and promising field of solar cell technology as a viable alternative and/or supplemental energy resource.

At the engineering level, solar cell efficiency is dictated by considerations and compromises between the many design factors that influence the photovoltaic effect. Parameters such as substrate material, substrate thickness, reflection management, electrical contacts, etc., directly influence the resulting solar cell efficiency of the end product. In order to achieve a desired efficiency rating, careful planning must be accomplished and incorporated into the solar cell fabrication process.

1.3 Hybrid Multi-Junction Silicon (HMJ-Si) Solar Cell

The HMJ-Si device is a novel approach to solar cell architecture that was designed and developed at the Air Force Institute of Technology. The design, shown in Figure 1, consisted of two silicon wafers, one stacked on top of the other with a 385μm air gap in between, to capitalize on photon absorption and decrease thermal degradation effects while minimizing fabrication costs from complex processing or materials [12].

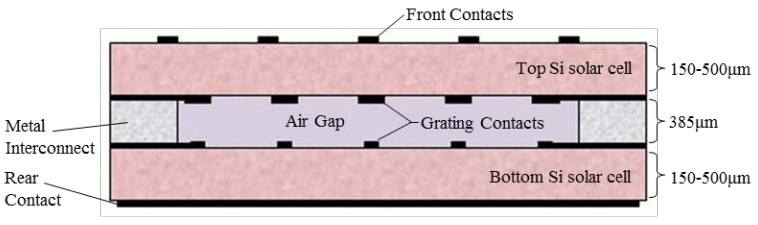

Figure 1. Cross-section of the HMJ-Si solar cell [12].

The architectural objective was to achieve multiple opportunities of photon absorption by exploiting characteristics of the interference pattern generated from the bottom metal contact grating of the top silicon wafer. After many iterations of testing with several configurations, the final overall efficiency obtained for the architecture design depicted in Figure 1 was 5.45% [12]. This was a relatively low efficiency, on par with organic solar cells developed in the early 2000 [6].

1.4 Research Objective

The primary objective of this thesis was to characterize the architectural design of the HMJ-Si solar cell and then improve upon it for the development of the hybrid multi-junction silicon germanium (HMJ-SiGe) solar cell.

1.5 Focus Areas

The following questions became the basis for research:

1. *Was the diffraction grating architecture effective in the appropriate wavelength and angle of incidence range?*
2. *Can spectral filtering of the grating contact design be optimized, subject to fabrication constraints?*
3. *Did the previous HMJ-Si solar cell diffusion process contain flawed fabrication steps?*
4. *Are there more appropriate metal-to-semiconductor interfaces in forming ohmic contacts?*
5. *Would replacing the bottom wafer with germanium improve performance of the architecture ?*
6. *Is it recommended for a Fresnel zone plate and distributed Bragg reflector be added for improvement to the architecture?*

1. Was the diffraction grating architecture effective in the appropriate wavelength and angle of incidence range? This questioned the intended performance of the

electrical contact design with regards to the resulting diffraction pattern formed on the surface of the bottom wafer.

2. Can spectral filtering of the grating contact design be optimized, subject to fabrication constraints? This questioned the interactions of photons at certain wavelengths to understand what the architecture of the electrical contact grating design was doing. For the case of an HMJ-Si solar cell, the electrical contact grating would ideally accept as many photons as possible of a desired wavelength and spectrally filter those of an undesired wavelength.

3. Did the previous HMJ-Si solar cell diffusion process contain flawed fabrication steps? This questioned the process used to form the pn-junction and the back surface fields on the silicon wafer.

4. Are there more appropriate metal-to-semiconductor interfaces in forming ohmic contacts? This questioned the electrical contacts at a solid state physics level.

5. Would replacing the bottom wafer with germanium improve performance of the architecture? This questioned the possibility of utilizing previous research conducted on germanium telluride [13] and its integration with an n-type germanium wafer to form a pn-junction for improved photon absorption in the near infra-red region.

6. Is it recommended for a Fresnel zone plate and distributed Bragg reflector be added for improvement to the architecture? This questioned the feasibility of adding features to the architecture that would concentrate a collection of photons towards the bottom wafer and enhance the selectivity of desired wavelengths without significant heat escalation to the silicon lattice.

These questions became the basis to study, characterize, and understand the HMJ-Si solar cell architectural design. The work presented here includes studying, testing, and analyzing seven focus areas: diffraction pattern generation, photon propagation, silicon diffusion processing, ohmic contacts, the distributed Bragg reflector, the Fresnel zone plate, and the germanium/germanium telluride (Ge/GeTe) pn-junction. While the first four focus areas investigated the architecture of the HMJ-Si solar cell, the remaining focus areas were examined for the development of the HMJ-SiGe solar cell. Specifically, the use of GeTe to form a pn-junction on a germanium substrate, utilization of a distributed Bragg reflector for rejection of undesired wavelengths, and the incorporation of a Fresnel zone plate for enhanced photon management were researched and tested . The culminating point was the assembly and testing of the Hybrid Multi-Junction Silicon Germanium (HMJ-SiGe) solar cell and a capstone demonstration of an external device performing under the sole power delivered by the HMJ-SiGe solar cell with a low-voltage power controller.

1.6 Summary

This chapter presented a brief overview of solar cells today, the genesis of this thesis, and the questions that spawned the search for the necessary theory and background needed to develop the methodology, obtain test results, and evaluate relevant data points for conclusive observations and future recommendations of this project.

II. BACKGROUND

2.1 Solar Cell Fundamentals

In general the fundamental process to a solar cell is the photovoltaic effect, which generates electrical current when light energy from an illuminated source like sunlight strikes the solar cell surface. This electrical current generation can then be acquired for delivery to an external load to accomplish work. However, to further understand what is occurring sub-surface of the solar cell, consideration must be given to the interactions that occur between photons, electrons and holes (absence of electrons) of the semiconductor.

2.1.1 Photon Energy

The photon is the primary source for injecting energy into a solar cell for conversion into electricity. However, the photon must have enough energy to begin the process. This energy can be described by equation (1) [14]

$$E_{\text{ph}} = \frac{hc}{\lambda} \tag{1}$$

where, E_{ph} is the photon energy in electron-volts (eV), h is the Planck's constant (6.6 x 10^{-34} J s), c is the speed of light (3 x 10^{8} m/s), and λ is the wavelength in a vacuum (m). The energy of a specific photon varies inversely by the wavelength of that photon. Therefore, photons with longer wavelengths have smaller energies than photons with shorter wavelengths which have higher energies.

Figure 2 shows the spectral irradiance across the solar spectrum above the earth's atmosphere, called Air Mass 0, and at sea level, called Air Mass 1.5. Air Mass is the "length of the [sunlight] path through the atmosphere in relation to the shortest length if the sun was in the apex" [15]. Therefore, Air Mass (AM) 0 represents the solar spectrum just outside the atmosphere and normal to the Earth's surface, whereas AM1.5 represents the solar spectrum at sea level on a 37° tilted surface [15]. The solar spectral irradiance depicted illustrates the power density at a particular wavelength that can be used by solar cells.

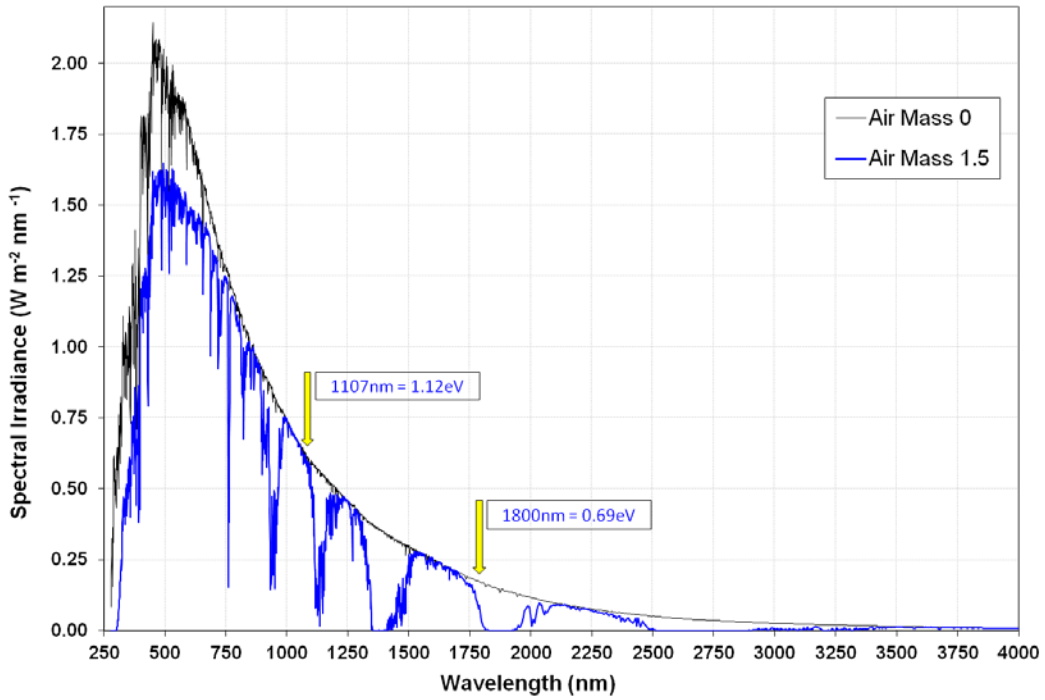

Figure 2. Spectral irradiance of solar spectrum. Air Mass 0 is the solar spectrum received above the Earth's atmosphere, and Air Mass 1.5 is the solar spectrum received on Earth at sea level [16, 15].

Using equation (1) the photon energy can be calculated for a specific wavelength. The boxed examples given in the graph of Figure 2 show the calculated values of 1.12eV and 0.69eV which represent the bandgap energies of silicon and

germanium, respectively. As will be explained later in this chapter, the bandgap energies are a demarcation between the usable, lower wavelengths and the non-usable higher wavelengths of the solar spectrum. In other words, a silicon solar cell can only convert portions of the spectral irradiance lower than 1107nm, whereas a germanium solar cell can convert portions of the spectral irradiance lower than 1800nm.

2.1.2 Energy Bands

Energy bands represent discrete levels of energy for electrons to occupy [17]. They are discrete in that electrons can only "jump" from one level to the next; this is not a gradual event but rather instantaneous. Therefore, the level of occupancy is determined by the amount of electron energy acquired by the electron via absorption from another source, like a photon. There are two energy bands that are important- the valence band, which is the highest band occupied by electrons, and the conduction band, which is the first unoccupied band above the valence band [17]. A forbidden zone, also known as the band gap, separates the valence band from the conduction band. Figure 3 illustrates these three elements:

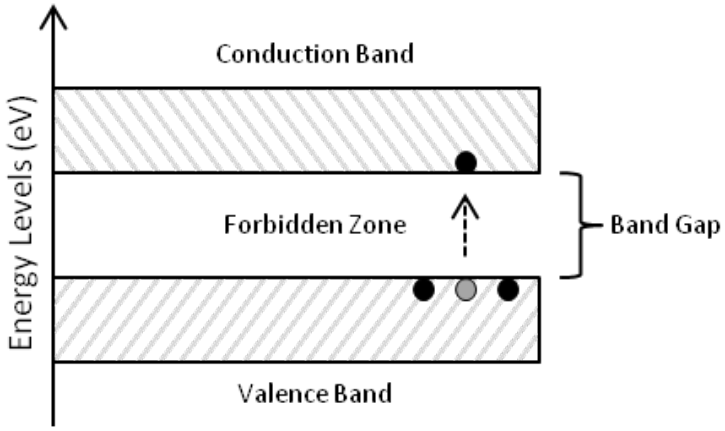

Figure 3. Conduction band, forbidden zone, and valence band. The electron leaves a hole behind when it acquires sufficient amount of energy to "jump" over the band gap [17].

For the semiconductor to generate electricity, electrons from the valence band must acquire enough energy to overcome the band gap and “jump” to the conduction band [17]. This also leaves behind a hole in the valence band which is just an absence of an electron. Together these are called an electron-hole pair (EHP).

The band gap is a unique characteristic for all materials, whether it is a metal, insulator, or semiconductor. Because insulators are non-conductive materials, their band gap is typically very large- greater than 3eV [17]. On the opposite end, metals are very conductive, so their band gaps are essentially zero. In fact, their valence and conduction bands overlap [17]. However, semiconductors, like silicon and germanium, have bandgaps that are less than 3eV. Figure 4 illustrates these concepts [17]:

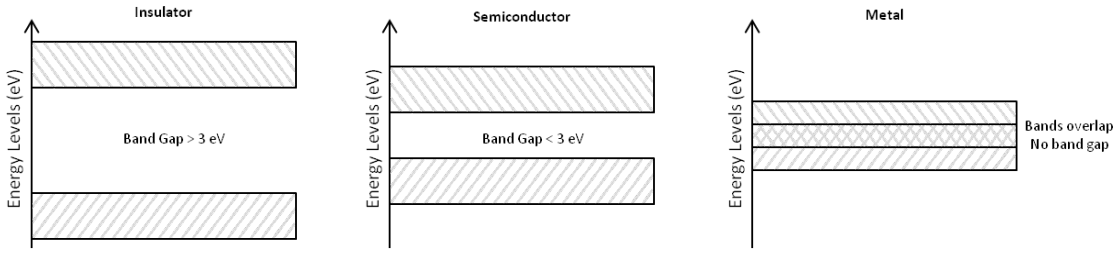

Figure 4. Differences in band gaps of an insulator, semiconductor, and metal [17].

2.1.3 Absorption

In order for photon absorption to occur for EHP generation, the incoming photon must have an amount of energy at least equivalent to the bandgap of the semiconductor. The absorption coefficient, denoted as α, is a measure of the ability for a semiconductor to absorb photons and is strongly related to the photon and bandgap energies [18]. Figure 5 shows the absorption coefficient for several semiconductors across a portion of the spectrum.

In the case of a silicon semiconductor, when a photon enters into the lattice, there are three possibilities for interaction with an electron in reference to the silicon band gap energy: 1) the photon energy is greater than the band gap, 2) the photon energy is equal to the band gap, and 3) the photon energy is less than the band gap. When the photonic energy is greater than or equal to the silicon band gap energy (1 & 2), then an EHP is created. In these two scenarios, an electron from the valence band jumps to the conduction band. However, in scenario 1, the electron jumps to a level much higher than the conduction band edge and the excess energy is dissipated as heat in the lattice [18, 19]. In fact, because the absorption coefficient is greater at higher energies (shorter wavelengths), the chances for a photon to be

absorbed are much greater than at lower energies (longer wavelengths). However, when the photon energy is less than the silicon band gap energy, electrons are not given enough energy to jump to the conduction band, resulting in negligible absorption. The photons then pass through the semiconductor, as if the material "appears to be transparent" to the photon [18].

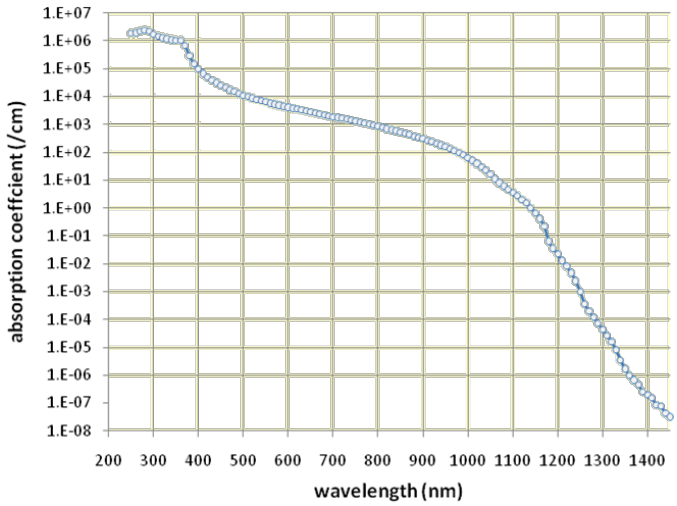

Figure 5. Absorption coefficient of silicon [20].

Furthermore, the absorption coefficient can also give a sense of how far photons can penetrate into a semiconductor's lattice before being absorbed which can be viewed inversely as the penetration depth x_p [17] in equation (2) and illustrated in Figure 6.

$$x_p = \frac{1}{\alpha} \tag{2}$$

where, α is the absorption coefficient.

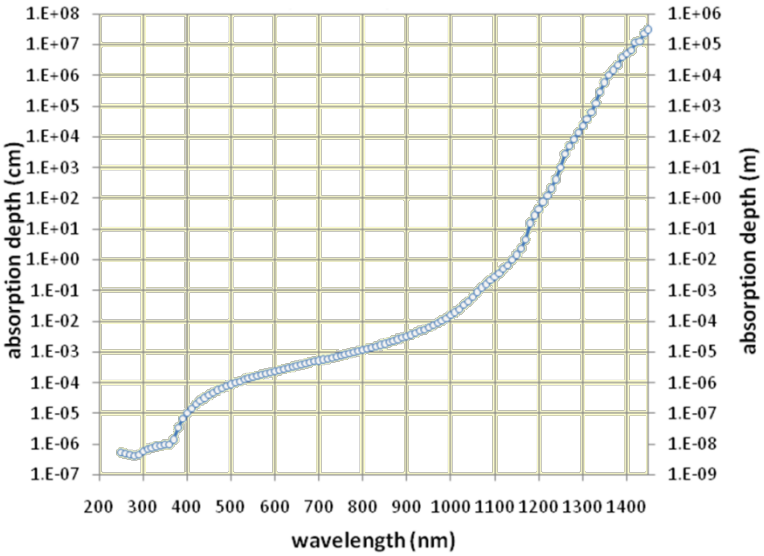

Figure 6. Absorption depth in silicon [20].

2.1.4 The PN Junction

Conventional solar cells are manufactured on silicon substrates for a number of reasons. First, silicon is a highly abundant resource and quite easy to extract and process, and therefore, it is very economical to manufacture for a variety of uses. Second, the electrical properties of silicon are very well known and quite predicTable for mass production, which is the key to keeping the cost of solar cells and technologies as low as possible. However, although this natural element is considered a semiconductor, silicon alone is not very useful. Doping, which is the introduction of impurities in a semiconductor, must be accomplished to exploit the desired electrical characteristics for the ultimate goal of generating electricity.

Because silicon is in the Group IV column of the periodic Table, a silicon atom's four valence electrons will covalently bond (or share valence electrons) with three other silicon atoms, forming a lattice structure as illustrated in Figure 7.

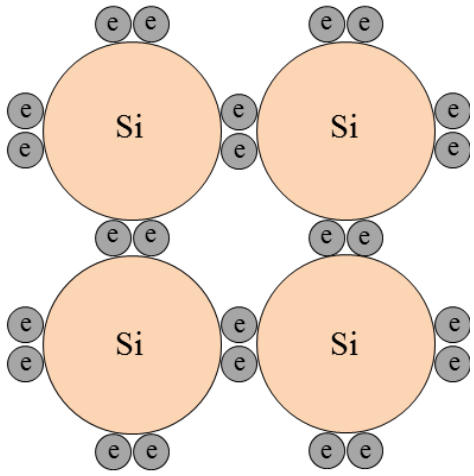

Figure 7. Covalently bonded silicon atoms [21].

However, in its elemental form, silicon by itself is not very useful as solar cells or any other fundamental electronic component. Dopants from other elements must be added to the silicon lattice structure to change and exploit the useful electrical characteristics of silicon, like resistivity. As Mazer stated, "…if a sample of pure single-crystal silicon is doped with a small concentration of phosphorus, say one atom for every hundred thousand atoms of silicon, the resistivity of the crystal lattice decreases from 230,000 Ω cm to about 0.03 Ω cm" [21]. This is usually accomplished by doping a wafer of crystalline silicon with elements that have more or less valence electrons, like boron and phosphorus (Figure 8).

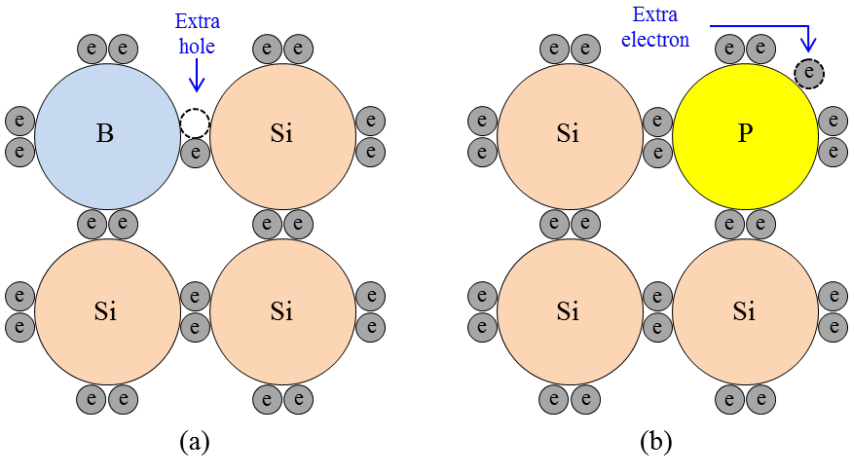

Figure 8. Doping of silicon. Doping silicon with boron adds extra holes (a) making it p-type, and doping silicon with phosphorus adds extra electrons (b) making it n-type [21].

Because boron is a Group III element, it lacks a valence electron to covalently bond with an available silicon valence electron. Instead, the silicon electron will leave its valence band and stay with the boron atom, leaving a hole in the silicon lattice structure; making this doped silicon material a p-type semiconductor (Figure 8a). Likewise, because phosphorus is a Group V element, its fifth valence electron that does not have an available silicon atom to covalently bond with resides in the conduction band of silicon; making this doped silicon material an n-type semiconductor. (Figure 8b) [21].

When a p-type semiconductor (concentration of holes) comes in contact with an n-type semiconductor (concentration of electrons), a pn-junction is formed, which is an important aspect in a solar cell's photovoltaic process. Because of these concentration gradients, a diffusion current occurs where a number of electrons from the n-type semiconductor diffuse across the pn-junction into the p-type

semiconductor to recombine with holes, and a number of holes from the p-type semiconductor diffuse across the pn-junction into the n-type semiconductor to recombine with electrons [17, 19]. This recombination of electrons and holes results in annihilation of each other and is a lost opportunity of capturing them to accomplish work [19]. However, an electric field develops around the pn-junction, because electrons that diffuse across the pn-junction leave behind uncompensated donor ions (fixed positive charges), and the holes that diffuse across the pn-junction leave behind uncompensated acceptor ions (fixed negative charges) [17, 19]. Because of these fixed positive and negative charges, the generated electric field tends to keep the electron and hole majority carriers in their dopant-type sides (i.e. electrons in the n-type region and holes in the p-type region) [22]. At equilibrium the diffusion and drifting forces equalize, and the resulting electrical potential difference that developed is known as the space charge region [17] (Figure 9), where this area is depleted of majority carriers.

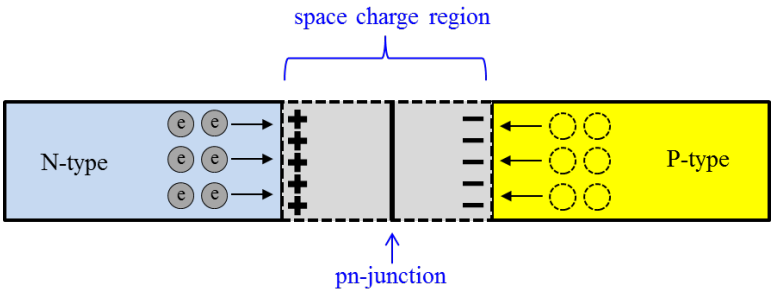

Figure 9. PN-Junction and space charge region [17].

2.1.5 Solar Cell Operation

As mentioned above, electron energy can change through absorption from another source, like photons from the sun in a solar cell. Silicon has a bandgap of 1.12eV, which is equivalent to 1107nm in wavelength. So, when photons, whose wavelengths are less than or equal to 1107nm, enter into the silicon solar cell and interact with electrons, EHPs are created. Likewise, because the band gap of germanium is 0.69 eV, when photons whose wavelengths are less than or equal to 1797nm enter into a germanium solar cell and strike electrons, EHPs are created.

The pn-junction is a significant component to the photovoltaic process in that it helps to keep majority carriers on their respective sides, and it helps to sweep minority carriers to their respective sides. This effect on the majority and minority carriers is due to the electric field in the space charge region. If an incoming photon is absorbed within the space charge region, then the generated EHP is forced to their respective sides and can be collected by the metal contacts to perform work on an external load. If an incoming photon is absorbed beyond the space charge region, then as long as the generated minority carrier of the EHP (i.e. electron in a p-type silicon substrate or a hole in a n-type silicon substrate) is within its diffusion length of the space charge region, then there is a relatively high chance that it will be swept to its respective side for collection by the metal contacts [17] to accomplish work on an external load. Figure 10 illustrates the photovoltaic effect delivering power to an external load to accomplish work.

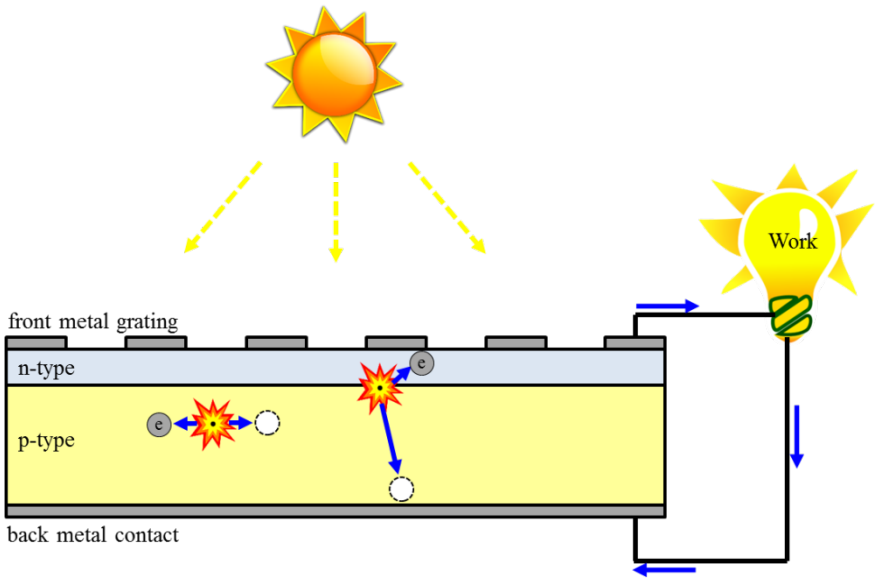

Figure 10. Typical solar cell operation. Incident photons with energies at least greater than the silicon bandgap enter into the semiconductor lattice and create EHPs. The EHPs are separated by the electric field and then collected by metal contacts to accomplish work, like illuminating a light bulb.

2.1.6 Solar Cell Fabrication

The three main processes for solar cell fabrication are diffusion, light trapping methods, and metal contact application [17]. Doping is the process for introducing impurities (see 2.1.4) into the silicon substrate in order to create the pn-junction. This can be accomplished by several methods, like by ion implantation or by a high-temperature diffusion furnace which is the prevailing and well-established technology [23]. Diffusion furnaces require substrates to be heated to temperatures of 800-900°C [17] or more, depending on the dopant source and diffusion profile (see 2.2.3). For silicon substrates boron (p-type) and phosphorous (n-type) are typical dopant sources [24, 25, 26]. Two common forms of dopant sources are solid planar (Figure 11) and liquid (see 2.2.3).

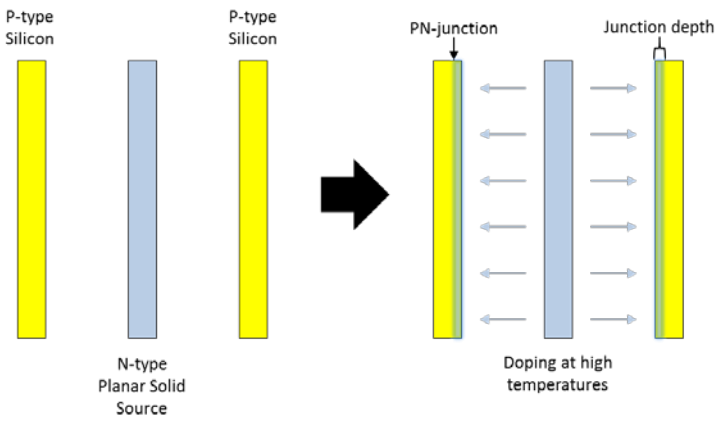

Figure 11. Solid planar source diffusion. By placing the silicon wafers side-by-side next to a solid planar source, doping is accomplished in high-temperature furnaces [27].

In the case of solid planar sources, the silicon wafers and sources are arranged very closely to each other in a quartz boat. Depending on the temperature and time, a concentration of dopant impurities diffuse into the silicon wafer. The dopant concentration is a gradient, as it decreases with distance into the substrate. The distance measured from the surface to the point where the dopant concentration ends is the junction depth, and it is at this location where the pn-junction is identified.

For germanium substrates bulk doping can be accomplished by other Group III and Group V elements, such as gallium (p-type) and antimony (n-type). However, germanium is typically used in high efficient multi-junction configurations for space photovoltaic applications, such as the gallium indium phosphide/gallium arsenide/germanium ($GaInP_2$/GaAs/Ge) tandem junction solar cell [28]. More complex than silicon solar cell fabrication, these multiple junction solar cells require

multiple layer growth via the metal-organic chemical vapor deposition process which results in a lower yield throughput [21].

Light trapping methods include texturizing of the substrate surface and application of an anti-reflection coating. These techniques improve solar cell performance by reducing the reflections of photons from the silicon surface [21]. The process of wet chemical texturing, typically accomplished before the formation of the pn-junction, creates a rough surface of pyramid shapes by using a solution of potassium [17, 21]. This helps by increasing the chances of multiple reflections back into the silicon bulk [29]. Anti-reflection coatings, usually applied after the pn-junction formation, are accomplished by a thin layer of a dielectric material, like silicon nitride, which takes advantage of destructive interference to prevent reflections from the surface [21, 30]. Further details of the ARC is discussed in 2.1.9.

Metal contacts are required to collect as many EHPs as possible for accomplishing work. However, any metal on the semiconductor becomes an obstruction to the incident photons and results in shading the surface directly beneath. To fabricate the metal contact grating, the solar cell industry uses a conductive silver paste in a screen printing process which has advantages in low cost and high throughput but has its disadvantages in contact width broadening and the consequential increased metal shading onto the silicon surface [21]. However, there are other ways that metal can deposited for contact forming on the surface of the silicon wafer, like electron beam (e-beam) evaporation and sputtering.

Before the silicon wafer can have metal deposited, the surface must be prepared with a pattern that would enable for the metal to adhere to the areas

desired. This process is called photolithography, which is basically the transfer of features from a mask to a substrate [31]. Photoresist, a sacrificial material sensitive to ultraviolet (UV) light, must be applied to the surface first. Then, a UV-light is illuminated through a patterned mask. Depending on the type of photoresist, the exposed areas will either develop away or stay on the surface. If a positive photoresist is used, then the areas exposed by the UV-light will be chemically changed and become more soluble in developer. If negative photoresist is used, then the areas exposed by the UV-light will be chemically changed and become more polymerized and resistant to developer [31]. After the desired pattern has been transferred to the substrate surface, metal deposition can be accomplished in a number of ways.

In the case of e-beam evaporation, the photoresist-patterned silicon wafer is mounted in a rotating holder above the metal source. Small nuggets of metal like gold, silver or titanium are placed in a graphite crucible where it is vaporized by a high energy electron beam generated from a filament [32]. The vaporized metal atoms travel in straight vertical lines from the crucible to the suspended wafer and adheres to silicon surface and the photoresist, which is a UV-sensitive material used in photolithography. Sputtering is a physical deposition technique that utilizes a planar target of a desired metal or dielectric. In a process of a ballistic exchange in momentum, a plasma of charged ions bombard the target material at high energy, resulting in the ejection of atoms from the target onto the substrate surface [33]. The metal covered photoresist is then removed by a process which uses acetone or another remover solution to dissolve the photoresist and lift away the metal.

2.1.7 MEMS Fabrication

Some of the process steps utilized in solar cell fabrication are also used in the fabrication of microelectromechanical systems (MEMS) devices. Using photolithography MEMS structures, like cantilevers, can be fabricated to microscopic dimensions.

There are three main techniques for fabricating MEMS devices- bulk micromachining, surface micromachining, and high-aspect ratio fabrication (Figure 12).

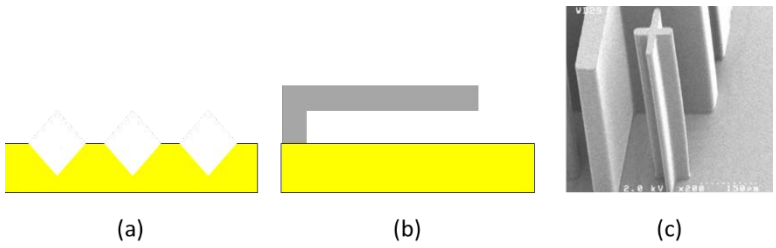

Figure 12. Main techniques of MEMS fabrication. Bulk micromachining (a) is a subtractive process that etches away bulk material. Surface micromachining (b) is an additive process that utilizes structural and sacrificial layers. High-aspect ratio fabrication enables construction of very tall devices [34, 35].

Bulk micromachining (Figure 12(a)), which is the oldest technique [36], is a subtractive process that builds devices into the substrate by etching away the unwanted portions of material. Etching of the bulk can be accomplished by isotropic wet etching, anisotropic wet etching, or by dry etching [37].

Surface micromachining (Figure 12(b)) is an additive process that builds up devices on the surface of the substrate by depositing thin structural layers of polysilicon and thin sacrificial layers of oxide. Some of the reasons for its popularity

are the simplicity in process and the ability for the precise control in the structural build up [38].

As the name implies, high-aspect ratio fabrication is a process that enables the creation of MEMS devices with very high aspect ratios (Figure 12(c)). This has been enabled by advances in microfabrication technology, like deep reactive ion etching [36]. LIGA, or Lithographie, Galvanoformung, and Abformung, is a process for making high aspect ratio devices [35] using an x-ray source, a polymer mold, and electroplating bath [36].

2.1.8 Solar Cell Testing

Efficiency is basically a ratio of the power generated by the solar cell over the power input from the light source. However, because many solar cell technologies exist, a standard test condition must be utilized to enable consistent comparison of individual performances: 1) full sun radiation of $1000W/m^2$, 2) solar module temperature of 25^0C, and 3) light spectrum AM1.5 [17]. To determine the power generated by the solar cell, three aspects are measured and calculated: open-circuit voltage (V_{oc}), short circuit current (I_{sc}), and fill factor (FF). V_{oc} is determined by measuring the voltage across the solar cell without a connected load. I_{sc} is determined by measuring the current without a connected load. The FF is calculated from V_{oc}, I_{sc}, and the product of the voltages and currents measured across various resistive loads. Essentially, the FF helps determine the actual maximum power point (M_{pp}) and is defined as the ratio of the solar cell's actual M_{pp} to the product of V_{oc} and I_{sc} [39], as shown in equation (3) [17]:

$$FF = \frac{V_{oc} \times I_{sc}}{V \times I} \tag{3}$$

V_{oc}, I_{sc}, and the FF can be plotted in a graph to visually see the "squareness" of a solar cell's performance. Figure 13 shows a comparison of an ideal M_{pp} (dashed line) to the actual M_{pp} (solid line) calculated across various resistive loads. The more efficient a solar cell is, the more square the solid curve becomes, and the closer the actual M_{pp} and ideal M_{pp} become.

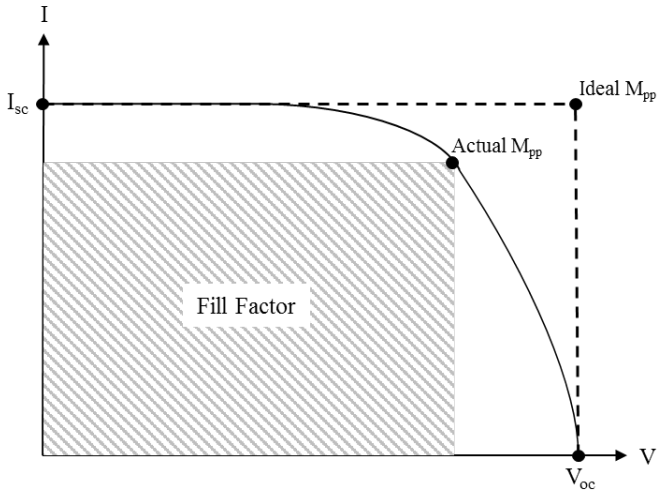

Figure 13. Graphical depiction of V_{oc}, I_{sc}, and the M_{pp}. The fill factor is the expression of the relationship between the actual (solid line) and the ideal (dashed line) maximum power points [17].

The result of these parameters are used in conjunction with the input power to calculate the efficiency η [17]:

$$\eta = \frac{FF \times V_{oc} \times I_{sc}}{P_{in}} \quad (4)$$

where, *FF* is the fill factor, V_{oc} is the open-circuit voltage (volts), I_{sc} is the short-circuit current (amps), and P_{in} is the input power (watts) from an illuminated source. P_{in} is calculated by the product of the irradiance (W/m^2) and the area (m^2) [17].

Automated software can be used to test solar cells extensively. Because unwanted heat from excessive photonic energies and continuous solar illumination can plague the efficiency of the photovoltaic process, long duration testing is desired data point for performance characterization. The National Instruments software LabVIEW is a graphical programming environment that enables communication and control with electronic equipment for test, measurement, and data acquisition [40]. If the test equipment has a communication interface, like a general purpose interface bus (GPIB) [41], then its manufacturer should be able to provide the necessary virtual instrument (VI) driver files [42]. The VI file developed by the vendor allows for a particular function to be accomplished from a LabVIEW front panel (Figure 14) which is the graphical user interface to control and acquire data from the actual test equipment [43].

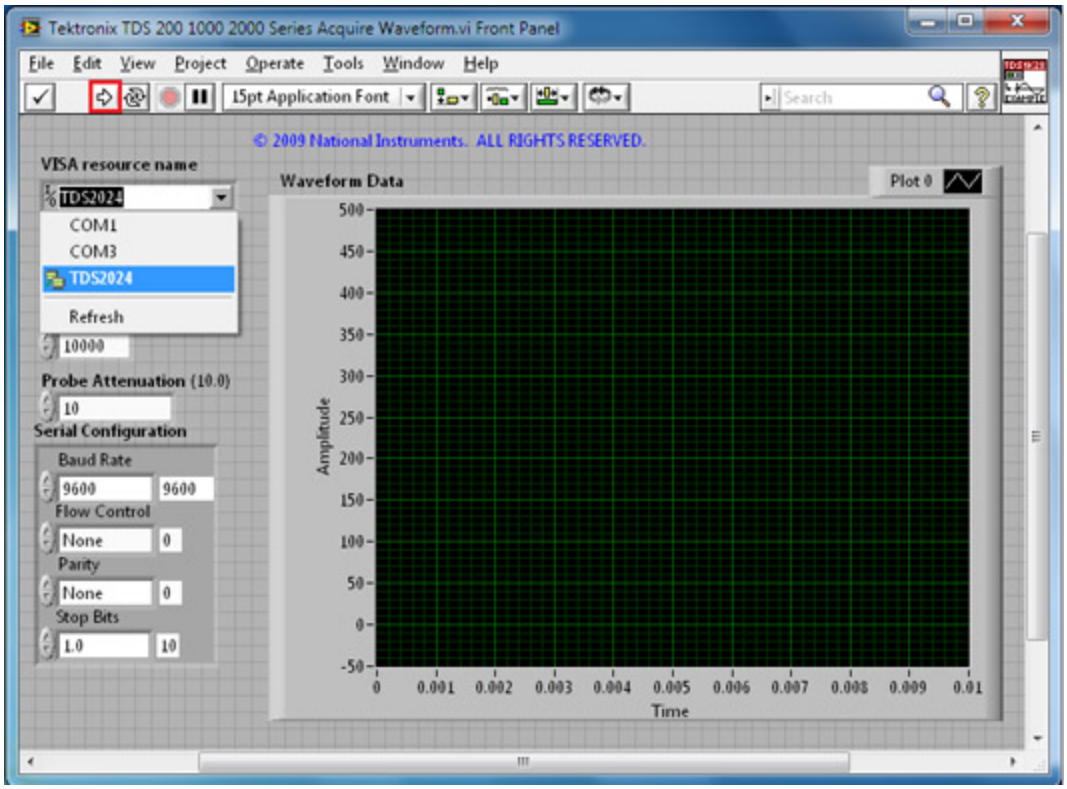

Figure 14. LabVIEW front panel example. Front panels are the user interface to the virtual instrument [42].

The VI file is also accessible for modification. Because the front panel is controlled by a graphical source code (Figure 15), programming test equipment to accomplish automated tasks like long duration solar testing is possible.

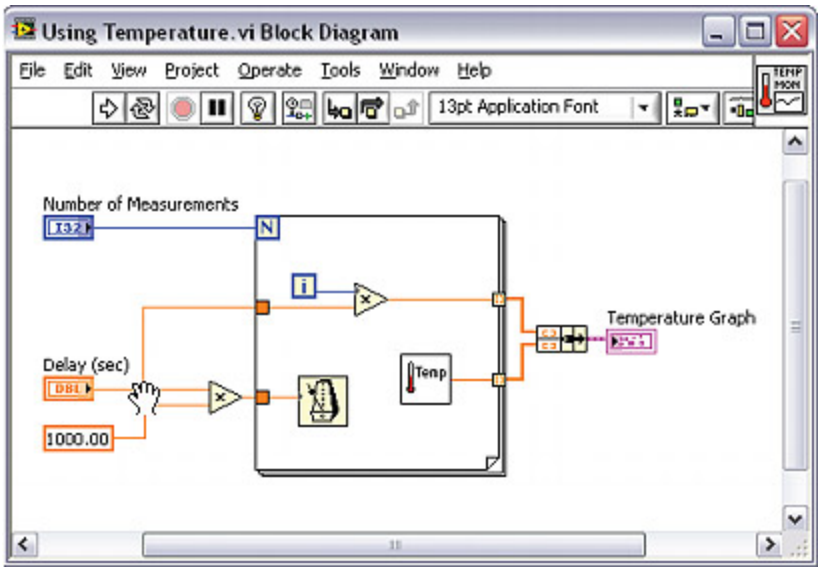

Figure 15. LabVIEW graphical source code example. Operation of the virtual instrument can be modified by changing the graphical source code in the block diagram.

The primary goal of any solar cell is to deliver the necessary power to a load to accomplish work, like charging a battery or capacitor. However, if the power-delivering capability of a solar cell is substantial, a power controller is needed to prevent damage to the batteries from overcharging them [44]. For low power solar cells that have a V_{oc} of at least 250mV, then a boost converter like the LTC3105 by Linear Technology [45] would be required. This integrated circuit utilizes maximum power point control and step-up voltage converter to deliver the maximum charging capability to a connected battery. Then, the charged battery can be used to power an external circuit like the illumination of a light-emitting diode (LED).

2.1.9 Influences on Efficiency

Solar cell efficiency, which is the ratio of the power generated by the solar cell to the power input from incident light, is influenced by many parameters, like recombination, light trapping schemes, an anti-reflection coating, bulk sheet resistivity, temperature, etc [46].

High temperatures can plague the photovoltaic efficiency of a solar cell, because open-circuit voltage, which is a metric in determining its performance, drops significantly with increase in temperature. In fact, there is a domino effect that can be seen from the following equations, beginning with the intrinsic carrier concentration n_i [47]:

$$n_i^2 = N_c N_v \mathrm{e}^{(-\mathrm{E_{g/kT}})} \tag{5}$$

where, N_c and N_v are the effective density of states for the conduction and valence bands, respectively, E_g is the bandgap energy (eV), k is the Boltzmann constant ($8.62\text{x}10^{-5}$ eV/K), and T the is temperature (K).

Temperature begins its influence with the semiconductor's intrinsic carrier concentration. This strong association is furthered conveyed by Muller that the intrinsic carrier concentration for silicon "doubles for every 8 degree Celsius in temperature near room temperature" [47]. Then, the carrier concentration affects the saturation current I_s, as shown in equation (6) [48]:

$$I_s = Aqn_i^2 \left(\frac{1}{N_a} \sqrt{\frac{D_n}{\tau_n}} + \frac{1}{N_d} \sqrt{\frac{D_p}{\tau_p}} \right) \quad (6)$$

where, A is the area (m^2); q is the electron charge (1.602×10^{-19} C [47]); N_a and N_d are the acceptor and donor concentrations, respectively; D_n and D_p are the diffusion coefficients for minority carrier electrons and holes, respectively; and τ_n and τ_p are the minority carrier lifetimes of electrons and holes, respectively. Furthermore, it can be seen that the diffusion coefficients, which lead to the diffusion lengths L_n and L_p, are also affected by temperature [47]:

$$D_n = \frac{kT}{\mu_n} \quad and \quad D_p = \frac{kT}{\mu_p} \quad (7)$$

where, μ_n and μ_p are the mobility of electrons and holes, respectively.

$$L_n = \sqrt{D_n \tau_n} \quad and \quad L_p = \sqrt{D_p \tau_p} \quad (8)$$

Substituting equations (7) and (8) into equation (6) gives a clearer depiction of the impact to the saturation current I_s by temperature [47]:

$$I_s = Aqn_i^2 \left(\frac{D_n}{N_a L_n} + \frac{D_p}{N_d L_p} \right) \quad (9)$$

Finally, the domino effect stops with open-circuit voltage V_{oc}, which is one metric that contributes to solar cell efficiency [17]:

$$V_{oc} = m \times V_T \times \ln\left(\frac{I_{sc}}{I_s}\right) \quad (10)$$

where, m is the ideality factor, which is a measurement of similarity to the ideal doped equation [49], and V_T is the thermal voltage (26 mV at 300K). Together, the product of V_{oc} and I_{sc} gives the ideal power output point of the solar cell. Although the saturation current increases slightly with respect to an increase in temperature, the open-circuit voltage sharply decreases and, thus, significantly affects the output power to the load. In fact, for every 10° C change in temperature, the power of a silicon solar cell drops around 5% [17]. Therefore, it can be seen that high temperatures are a problem to the performance of a solar cell.

Light trapping helps to increase the efficiency by decreasing reflectance. Silicon can reflect 34% to 54% of incident light depending on the wavelength of the solar spectrum [21], whereas germanium can reflect at least 37% of incident light [50]. In addition to decreasing the reflection, light trapping techniques help by increasing the chances of photon absorption to create as many EHPs as possible within the solar cell. Depositing an anti-reflective coating (ARC) on the top surface of the solar cell is a commonly used method. An ARC works by taking advantage of the destructive interference (see 2.2.2) at multiple interfaces of dielectric materials. Silicon nitride (Si_3N_4), considered the standard material for solar cells, yields less than 1% of reflection at the 600nm wavelength for just 74nm in thickness [17]. The

thickness d_{ARC} is determined by one-quarter of the target wavelength and the refractive index of the material [51]:

$$d_{ARC} = \frac{\lambda_0}{4n_{ARC}} \tag{11}$$

where, λ_0 is the target wavelength, and n_{ARC} is the ARC refractive index. The reflection factor R is given by [17]:

$$R = \frac{n_{ARC}^2 - (n_{air} \times n_{semi})}{n_{ARC}^2 + (n_{air} \times n_{semi})} \tag{12}$$

where, n_{air} and n_{semi} are the refractive index of air and the semiconductor, respectively. For a single ARC layer, the necessary thickness is readily defined by equations (11) and (12).

Creating a back surface field (BSF) in the lower region of a solar cell can also help increase the solar cell efficiency by mitigating recombination that can occur at the bottom interface between the metal and silicon. The BSF is accomplished by highly doping the bottom silicon surface with the same substrate doping type (i.e. p+ or n+). Like the pn-junction of opposite dopant types, the BSF is basically another built-in electric field that acts like a mirror to the minority carriers (Figure 16) and redirects them back toward the space charge region [17].

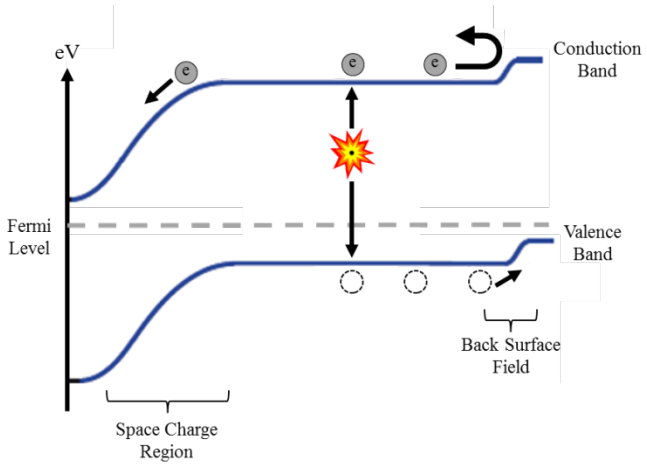

Figure 16. Back surface field illustration. The back surface field acts like a mirror, having a built-in electric field that redirects minority carriers back toward the space charge region [17].

The HMJ-Si solar cell employed an enhanced back surface field (EBSF). The EBSF was formed by doping the bottom of the silicon substrate twice, such that the second dopant concentration is higher than the first to ensure a step potential in the energy diagram. In other words and in relation to Figure 16, an energy diagram depicting the EBSF would have a second step potential on the right side of the figure.

2.2 Focus Areas

In addition to the background information of solar cell fundamentals presented above, further background information was acquired through research and investigation into seven focus areas: diffraction pattern generation, photon propagation, silicon diffusion processing, ohmic contacts, the distributed Bragg reflector, the Fresnel zone plate, and the Ge/GeTe pn-junction.

2.2.1 Diffraction Pattern Generation

Diffraction is the change of wave direction due to passing around a barrier or through an opening [52]. This definition is applicable to a light, since it is a self-sustaining propagating transverse wave. Therefore, a diffraction pattern is the visible result of this behavior, like the example pictured in Figure 17.

Figure 17. Diffraction pattern of light through single narrow slit [53].

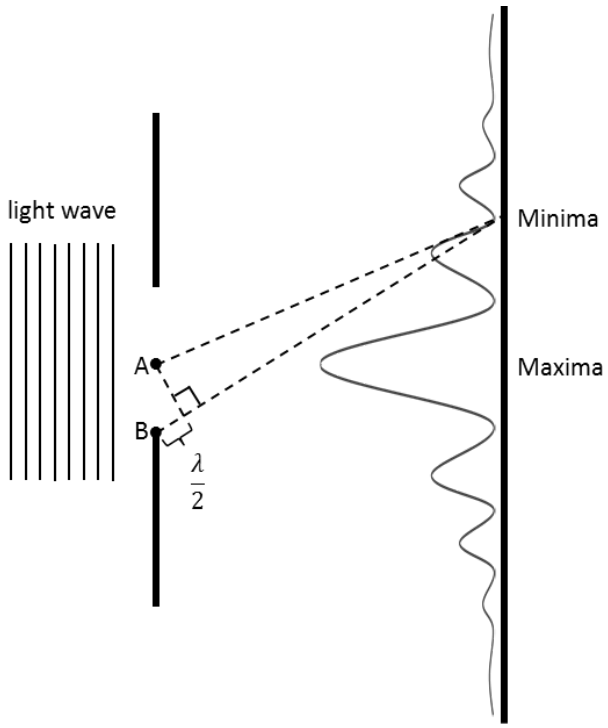

Figure 18. Diffraction pattern generation. The minima areas are formed by destructive interference when light waves travel at a difference of a half-wavelength from any two points within the slit space [54].

The right side of Figure 18 illustrates a generated diffraction pattern, having peaks (maxima) and valleys (minima) of intensity. The maxima are the result of constructive interference, and the minima are the result of destructive interference [55]. Constructive interference is the result of two waves summing together to form a larger wave in amplitude (bright spots), and destructive interference is the result of two waves summing together to form no wave at all (dark spots) [56]. Waves that are in phase by multiples of the free space wavelength will add together constructively, and two waves that are out of phase by multiples of half-wavelengths will negate each other totally.

When a light wave at normal incidence passes through a slit, as seen in Figure 18, any point region within the slit space can be treated as a "point source from which new waves spread out" [54]. For example, light waves from point A and point B travel from the slit and meet at the minima. However, it is because that the light wave from point B must travel a longer path distance (by a half-wavelength, and thus 180° out of phase) that the two destructively interfere at the minima. If this path difference was a multiple of a wavelength, then the waves would constructively interfere and form a maximum. The interference pattern generated is based on normal incidence of the incoming light wave. However, if the incident wave is at oblique angles of incidence, then the maxima and minima will shift accordingly [57].

A diffraction grating, as illustrated in Figure 19, can be regarded as many multiples of single objects or slits. When a monochromatic light wave passes through a diffraction grating of slits at normal incidence, then there are more contributions to the maxima and minima regions of the diffraction pattern. This results in a diffraction pattern where the minima regions at a small distance from the maxima destructively interfere greatly, and the maxima regions constructively interfere greatly, resulting in the peaks being extremely narrow (Figure 22) [58].

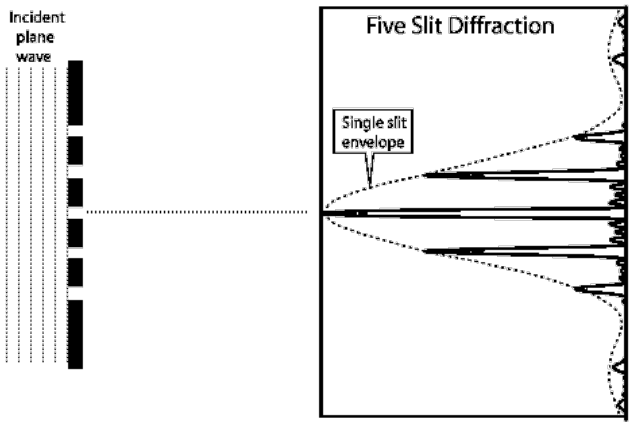

Figure 19. Diffraction grating example. This has multiple slits that generate interference patterns with extremely narrow and intense maxima [59].

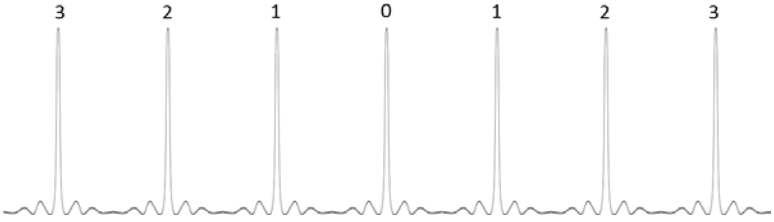

Figure 20. Maxima orders in a diffraction grating [60].

The numbers above the maxima peaks in Figure 20 are referred to as the order [61]. The maxima and minima can be expressed using equations 13 and 14, respectively [62]:

$$\sin\theta = \frac{\mathrm{n}\lambda}{d}, n = 0, n = \pm 1, \pm 2, \ldots \tag{13}$$

where, n is the order number, and d is the spacing in between the slit centers.

$$\sin\theta = \frac{\mathrm{n}\lambda}{Nd}, n = 0, n = \pm 1, \pm 2, \ldots \tag{14}$$

where, N is the total number of slits in the diffraction grating. Also, the locations of the maxima can be determined by the following equation [63]:

$$\tan\theta = \frac{\mathrm{y}}{D} \tag{15}$$

where, y is the distance from the center maximum to the maxima of interest, and D is the distance from the diffraction grating to the plane with the generated diffraction pattern.

2.2.2 Photon Propagation

Rigorous coupled wave analysis (RCWA) is a method used to study and model diffraction of electromagnetic waves from periodic grating structures [64, 65]. A periodic grating structure is simply a structure with a repeating pattern, or a unit cell [66].

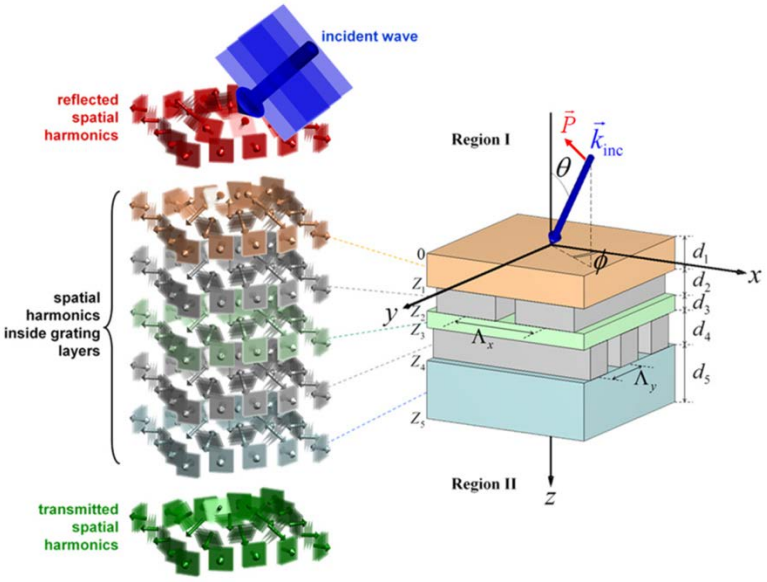

Figure 21. Numerical mechanism in rigorous coupled wave analysis [67].

A constraint to RCWA is that a unit cell must be uniform in one of the directions and can be inhomogeneous in the other two directions. Therefore, a grating structure can be complex in design in two dimensions, or say x-y direction, but the pattern must be uniform in the z-direction. Figure 21 illustrates a multi-layer periodic structure on the right side where variations in the grating structure changes in the x-y direction but is homogenous in the z-direction. In fact, RCWA is a semi-analytical approach for solving scattering investigations in that the cross-section of a unit cell (x-y direction) is solved numerically and an analytical solution

is accomplished in the uniform direction [66]. The unit cell can have multiple layers in the non-periodic direction, and RCWA will use the solutions computed of the electromagnetic waves and match boundary conditions at each layer to provide an overall understanding of the propagation through the entire unit cell. RCWA is based on the transfer matrix method (TMM) to calculate a matrix wave equation, which is then used to formulate scattering matrices for determining the reflection and transmission scattering parameters. Interestingly, because the TMM treats all electromagnetic power as forward propagating waves, a later-developed RCWA method solves the numerical instability found in TMM by incorporating a technique called the enhanced transmittance matrix approach to preempt this instability [66, 65]. A significant advantage of using RCWA over other scattering analysis simulation methods is speed [66].

The propagation of photons through a solar cell can be used with RCWA.

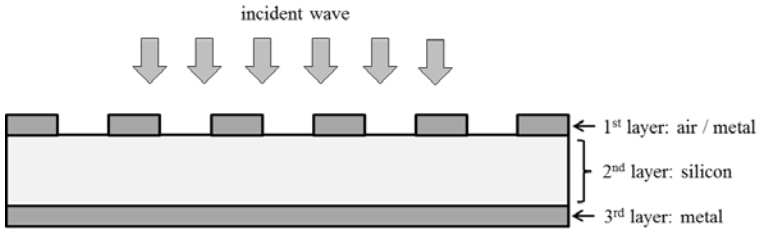

Figure 22. Period grating structure can be divided up into individual layers.

The metal electrical contact grating pictured in Figure 22 can thought as a periodic structure that is inhomogeneous in the x-y direction but homogenous in the z-direction. The same convention can be applied to the silicon and metal layers

beneath. Therefore, resultant solutions of the reflection and transmission scattering parameters can be determined by simulation of the solar cell periodic grating structured layers while varying certain parameters, like width of the grating fingers, thickness of the layers, etc.

2.2.3 Silicon Diffusion Processing

Diffusion is a process used to dope silicon wafers to form features like a pn-junction or a BSF (see 2.1.9). This can be accomplished in a diffusion furnace, where multiple wafers sit vertically side-by-side in a quartz boat, and are exposed to impurities by liquid or solid dopant sources [68]. Given enough thermal energy (around 800-1000°C), these dopant impurities can work their way into the silicon lattice typically through point defect vacancies and interstitially [47]. As can be seen from Figure 23, while the vacancy point defect is self-explanatory, the interstitial point defect is characterized by a dopant atom residing within a void between the silicon atoms [14].

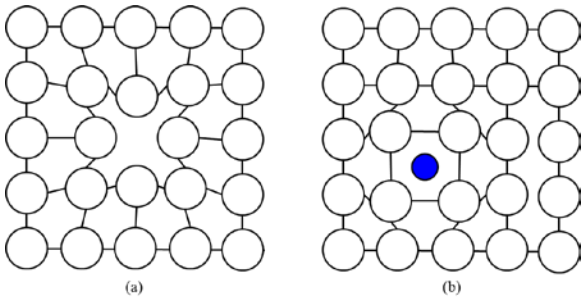

Figure 23. Vacancy (a) and interstitial (b) point defects [19].

Phosphorus tricloride oxide ($POCl_3$) is a common liquid dopant, usually in a bubbler flask, that is used as an n-type dopant. A carrier gas such as nitrogen is used to bubble through the flask. This enables the gas to become saturated with the dopant impurities. When the saturated carrier gas mixes with oxygen and flowed over the wafers in the quartz boat, the $POCl_3$ becomes oxidized to form a glass called phosphorus pentoxide (P_2O_5) [21].

The growth of P_2O_5 on the silicon surface is actually when the diffusion of the dopants begin. Known as predeposition, this newly formed glass layer is highly concentrated with a very shallow junction depth into the silicon bulk [21]. If a shallow diffusion profile is desired, then the carrier gas can be shut off, wafers removed from the furnace, and the glass can be removed by submersion into a "10% HF solution for about a minute" [21]. If a deeper junction depth is desired, a drive-in step is typically accomplished in which silicon wafers remain in the furnace at higher temperatures, resulting in a lower surface dopant concentration [21].

A typical sequence of a diffusion process is: push, ramp up, stabilize, source, purge, ramp down, and pull [69]. These steps are defined by the time and temperatures desired for the target diffusion profile, which is typically driven by a target sheet resistance. The push and pull steps refer to the transiting of the wafers in and out of the furnace, whereas the ramping steps refer to the target temperature. The source time and temperature can be determined by referencing a target sheet resistance from a dopant manufacturer datasheet chart like the one illustrated in Figure 24 by Air Products and Chemicals, Inc.

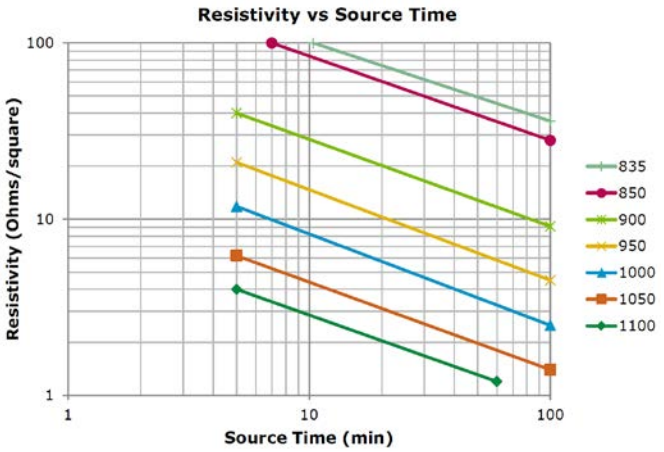

Figure 24. Sample target sheet resistivity chart. Desired target is determined by the deposition time and temperature of the liquid source being used [70].

For example if a sheet resistance of 10 Ω/□ is the target, then the source step time and temperature can be set for 7 mins at 1000°C, ~20 minutes at 950°C, or ~80 minutes at 900°C. However, this diffusion profile will change if a drive-in is accomplished afterwards.

Although the sheet resistance in Ω/□ is typically given for determining the appropriate temperature and time for a particular diffusion profile, it can be useful to calculate the sheet resistivity, also known as bulk resistivity [71], to find the surface dopant concentration using online resources like [72]. If the sheet resistance and the thickness of the material is known, then the sheet resistivity can be calculated simply by the product of the sheet resistance and material thickness [71].

Although a low sheet resistivity from a high surface dopant concentration is desired for creating an ohmic metal contact, this also creates high surface recombination [21]. The best of both worlds can be achieved by etching back the

silicon surface in between the metal contacts to lower the dopant concentration but keep this concentration the same underneath the metal contacts [21, 73, 74].

Some manufacturers provide a useful chart on obtaining a particular junction depth depending on the deposition time (Figure 25). However, charts like those assume no drive-in following deposition.

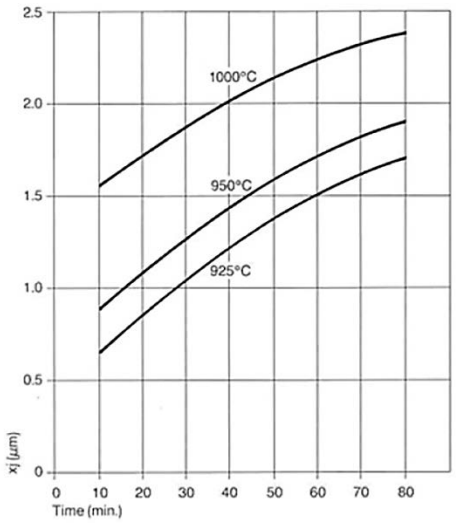

Figure 25. Sample junction depth vs. deposition time from solid source [75].

Furthermore, there are useful online calculators that help determine an estimate junction depth and sheet resistance depending on the substrate doping and diffusion profiles provided as input data. The online website PV Lighthouse [76] is a good resource to use in determining the appropriate diffusion profile by the desired pn-junction and sheet resistivity for solar cell design.

During the process of diffusion, the pn-junction and the BSF would typically be created by different dopant types- either boron (p-type) or phosphorus (n-type). However, because both sides of the wafer is exposed inside a diffusion furnace, it is

necessary to protect the side that should not receive the deposition. This can be accomplished by thermally growing a sufficiently thick oxide layer. A thickness that is sufficient is dependent on time and temperature the dopant deposition profile, as can be seen in Figure 26.

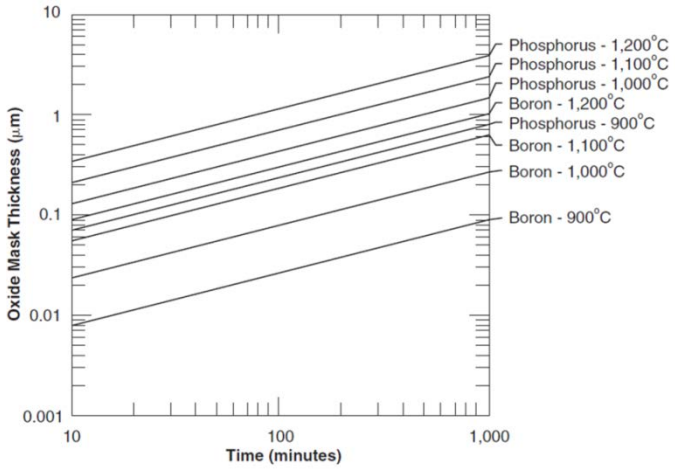

Figure 26. Chart to determine protective oxide thickness [77].

During the diffusion process of fabricating a solar cell, the edges of the substrate may contain dopant concentrations. This creates a shunting issue which "accounts for 80% of the total loss mechanism" [78]. In other words, because the emitter is very conductive, the top side contacts are electrically connected to the bottom side contacts via the edge of the substrate [79]. Therefore, it is critical that a method is employed to electrically isolate both sides of the substrate from each other.

A common edge isolation process in the solar cell industry is to stack and compress many solar cells on top of each other and plasma etch the edges [80]. Other methods can be employed, such as using an automatic dicing saw [74] or a fiber laser [78].

2.2.4 Ohmic Contacts

The metallization process to produce the electric contacts is very important, since this is how the EHPs are extracted from the solar cell to accomplish work.

When applying metallization to a solar cell, it is important to have a good ohmic contact between the semiconductor and the metal to ensure maximum extraction possible of EHPs generated by the photovoltaic process for delivery to an external circuit. A semiconductor-to-metal contact is considered ohmic when the contact resistance is low and conduction can easily flow back and forth [18]. In other words, the ohmic contact does not obstruct the transport of majority carriers from the semiconductor to the metal (and vice versa); the current is not limited. This is indicative by a linear curve on a current versus voltage (I-V) plot of the junction.

Formation of an ohmic contact is determined by several electronic characteristics of the metal and semiconductor, all of which can be seen in an energy band diagram (Figure 27).

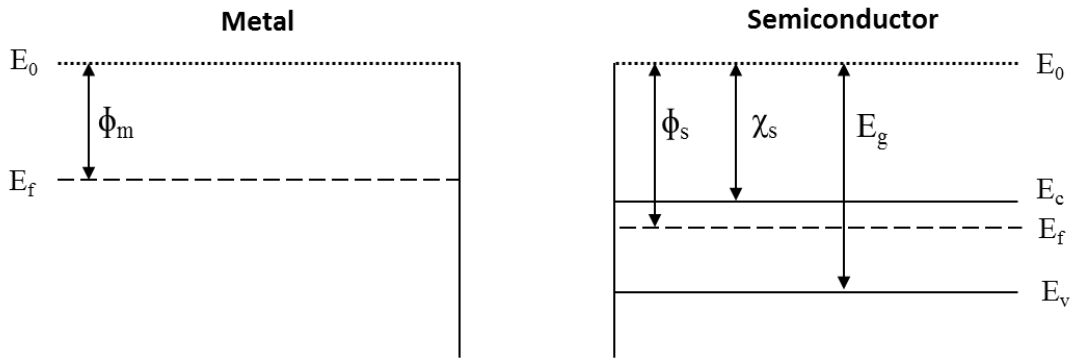

Figure 27. Metal and semiconductor band diagrams before contact [47].

The work function ϕ represents the amount of energy needed to extract an electron from the Fermi level to a vacuum away from the material, whereas the electron affinity χ is amount of energy needed to extract an electron from the conduction band to a vacuum away from the material [19]. The electron affinities for silicon and germanium are 4.01 and 4.13, respectively [18]. Furthermore, it can be seen in Figure 27 that the semiconductor is n-type, since the Fermi level is closer to the conduction band.

To create an ohmic contact between a metal and an n-type semiconductor, the work function of the metal ϕ_m must be less than the work function of the semiconductor ϕ_s, and opposite holds true for a p-type semiconductor- the work function of the metal ϕ_m must be greater than the work function of the semiconductor ϕ_s [19]. A Schottky contact will occur if each of these cases are the opposite. Nevertheless, when the metal and semiconductor materials are brought together in contact, the energy bands of the semiconductor will bend accordingly.

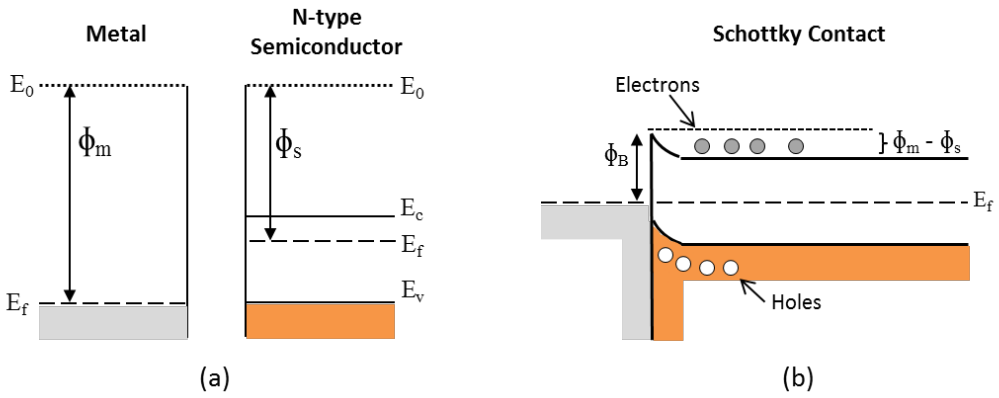

Figure 28. Schottky contact. When a metal with a work function that is greater than the n-type semiconductor work function (a) is physically brought together, a Schottky contact is formed with the n-type semiconductor (b) [47].

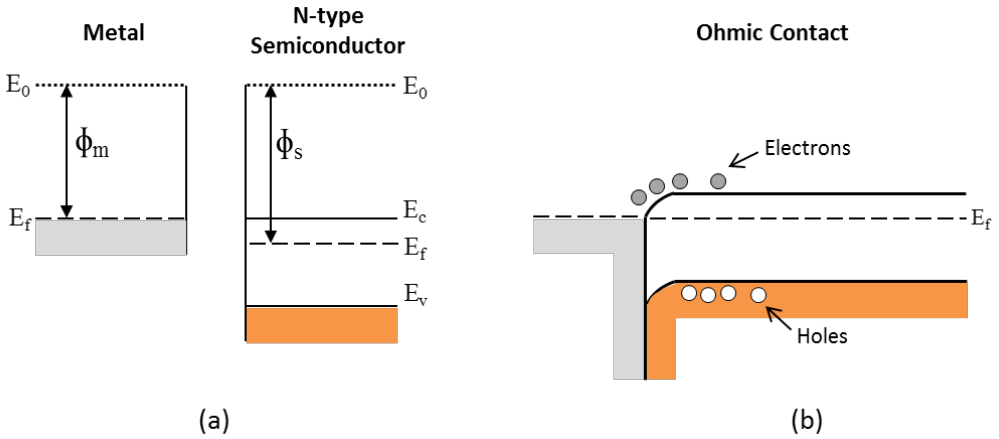

Figure 29. Ohmic contact. When a metal with a work function that is less than the n-type semiconductor work function (a) is physically brought together, an ohmic contact is formed with the n-type semiconductor (b) [47].

As one can see from the illustrations in Figure 28 and Figure 29, the difference between the work functions forms a barrier height at the contact junction. The barrier height ϕ_B can be expressed by [81]:

$$\Phi_B = \phi_m - \chi_s \quad (n-type) \tag{16}$$

$$\Phi_B = \left(E_g + \chi_s\right) - \phi_m \quad (p-type) \tag{17}$$

where, ϕ_m is the metal work function, and χ_s is the semiconductor electron affinity. From equations (16) and (17), it can be seen that for n-type metal-to-semiconductor (MS) junctions, the barrier height will increase as the metal work function increases. The same would happen to p-type MS junctions as the metal work function decreases. Reduction of the barrier height as much as possible is vital to creating an ohmic contact. Therefore, the metal work function should be as small as possible for n-type semiconductors and as large as possible for p-type semiconductors.

In a Schottky contact for an n-type semiconductor (Figure 28), the electrons have a significant barrier height to overcome when moving from the semiconductor side to the metal side. However, the holes have little resistance moving to the metal side. In an ohmic contact for an n-type semiconductor (Figure 29), the electrons can easily move to the metal side, but the holes encounter a significant amount of resistance when moving towards the metal interface. Although not illustrated, the opposite convention holds true for a p-type semiconductor: a Schottky contact is formed when the p-type semiconductor work function is greater than the metal work function, and an ohmic contact is formed when the p-type semiconductor work function is less than the metal work function [47]. Therefore, because creating a pn-junction is part of the solar cell fabrication process, it is pertinent to ensure the correct contact is being made to the correct dopant type of the substrate so that an accurate assessment of a solar cell's performance can be determined.

Furthermore, a semiconductor's work function is influenced by its dopant type and concentration [82]:

$$\Phi_s = \chi_s + \left(\frac{E_g}{2}\right) - \frac{kT}{q}\ln\frac{N_D}{n_i} \quad (n-type) \tag{18}$$

$$\Phi_s = \chi_s + \left(\frac{E_g}{2}\right) + \frac{kT}{q}\ln\frac{N_A}{n_i} \quad (p-type) \tag{19}$$

where, ϕ_s is the semiconductor work function, N_D is the donor concentration in the semiconductor, and N_A is the acceptor concentration in the semiconductor. As one can see from equations (18) and (19), as the doping concentration increases (or decreases), the work function for that specific dopant type will follow accordingly. Table 1 shows a list of common metal work functions.

Table 1. Common metal work functions [18].

Metal	Work Function (eV)
Silver (Ag)	4.26
Aluminum (Al)	4.28
Titanium (Ti)	4.33
Gold (Au)	5.1
Nickel (Ni)	5.15

There are conditions under which finding a metal work function to satisfy the criterion for creating an ohmic contact with an n-type semiconductor becomes nearly impossible. For instance, n-type germanium (n-Ge) substrates are quite difficult to form a low resistance ohmic contact with metal alone. This is due to the Fermi level being pinned to the valence band edge (Figure 30) of the n-type

semiconductor which results in a high Schottky barrier height [83]. However, by inserting a very thin interfacial layer, like Al_2O_3, TiO_2, GeO_2, or even Si_3N_4 [84, 85], in between the metal and n-type germanium, the barrier height is lowered and allows for tunneling across the barrier.

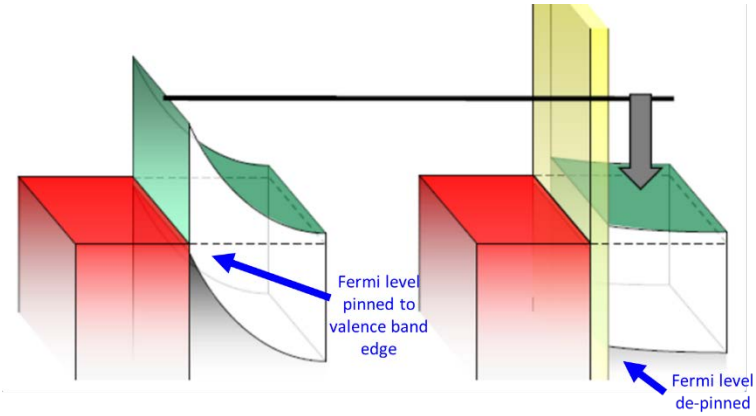

Figure 30. Fermi level de-pinning by insertion of thin interfacial [86].

A common way to compare the effectiveness of ohmic contacts among different variations of MS junctions is to find the contact resistance using the transmission line method (TLM). This can be done by fabricating metal pads of equal dimensions on a substrate of choice where the metal pads are spaced at different lengths [87]. The total resistance R_T between any two metal pads can be thought of as three resistors as depicted in Figure 31 and expressed in Equation (20) .

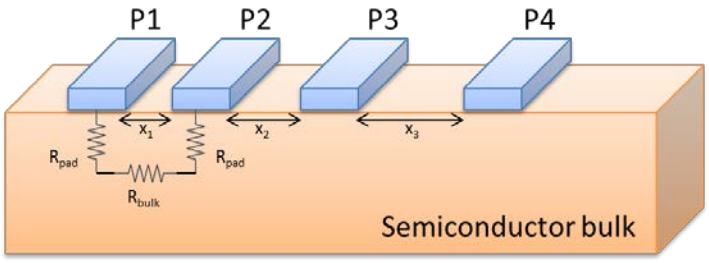

Figure 31. Contact resistance testing structure [87].

$$R_{T(Px-Px)} = R_{pad} + R_{semi} + R_{pad} \tag{20}$$

where, R_{pad} is the resistance between the metal pad and the semiconductor (Ω), and R_{semi} is the resistance through the semiconductor (Ω).

However, contact resistivity ρ_c (Ω·m^2) is the common metric, since this is not dependent upon the size of the metal pad, and it is expressed by [88]:

$$\rho_C = R_{pad} \times A_C \tag{21}$$

where, A_c is the area of the metal pad (m^2).

2.2.5 The Distributed Bragg Reflector

A distributed Bragg reflector (DBR) basically operates as the name implies- like a mirror. Typical DBRs consist of alternating layers of two different dielectric materials with significantly different refractive indices. Like the ARC (see 2.1.5), DBR layers are typically designed with material thicknesses that are one-quarter of the target wavelength [89], as expressed in equation (11). However, rather than

creating an anti-reflection effect, multiple pairs of layers are deposited to create a near 100% reflection of the target wavelength.

DBR stacks can be fabricated by plasma enhanced chemical vapor deposition (PECVD) [90]. Another method is by ion implantation, but some of the benefits of using PECVD include cost-efficiency, "good adhesion, step coverage, and moderate stress" [91]. The dielectric materials available by PECVD at AFIT are amorphous silicon (a-Si), silicon nitride (Si_3N_4), and silicon dioxide (SiO_2). Relative to the target wavelength, the refractive indices of a-Si, Si_3N_4, and SiO_2 can be found by using online databases such as [92] or [93].

Because the DBR is comprised of alternating materials of differing refractive indices, a normal incident light wave will become reflected with a 180^0 phase shift at the interface when it passes from a low refractive index to a high refractive index. No phase shift occurs with the converse- passing from a high refractive index to a low refractive index. In fact, as long as the DBR stack is constructed with the incident light passing from low refractive index to high refractive index at each paired interface, all reflected portions will interfere constructively, thus producing an overall high reflectance effect [94].

The DBR reflectivity *R* can be calculated by [95]:

$$R = \frac{1 - \left(\frac{n_H}{n_L}\right)^{2N} \frac{n_H^2}{n_0 n_s}}{1 + \left(\frac{n_H}{n_L}\right)^{2N} \frac{n_H^2}{n_0 n_s}} \tag{22}$$

where, n_H is the high refractive index, n_L is the low refractive index, n_S is the refractive index of the substrate, n_0 is the refractive index of the initial medium, and N is the number of pairs in the DBR.

If the initial medium that the incident light is coming from is air, then the initial medium refractive index n_0 is 1. Therefore, equation (22) can be reduced to:

$$R = \frac{1 - \left(\frac{n_H}{n_L}\right)^{2N} \frac{n_H^2}{n_s}}{1 + \left(\frac{n_H}{n_L}\right)^{2N} \frac{n_H^2}{n_s}} \tag{23}$$

As can be seen from equation (23), the reflectivity is determined by the refractive indices of the materials that make up the DBR stack. The bandwidth of the DBR stack $\Delta\lambda$ can be determined by [95]:

$$\Delta\lambda = \frac{\pi}{2}\lambda_d \left[\frac{1}{\cos^{-1}\left(\frac{n_H - n_L}{n_H + n_L}\right)} - \frac{1}{\cos^{-1}\left(-\frac{n_H - n_L}{n_H + n_L}\right)}\right] \tag{24}$$

where, λ_d is the DBR target wavelength.

The bandwidth determines how wide of the portion of the spectrum where high reflectivity is desired. Interestingly, the bandwidth is significantly affected by the contrasting differences between the high and low refractive indices. In other words, the larger the gap between these two values the wider the DBR bandwidth becomes [94].

In addition to several resources that provide direct or indirect assistance with simulations of DBRs [50, 96, 97], MATLAB is powerful software program that can simulate and assist in robust designs of DBRs [98].

2.2.6 The Fresnel Zone Plate

A Fresnel zone plate (FZP) is a device that uses constructive interference to focus electromagnetic waves at a desired focal point [99]. FZPs are used in applications where a distant light source needs to be focused [99], like x-ray microscopy, x-ray telescopes, and other imagery purposes [99, 100, 101]. Similar to a diffraction grating that uses slits, the FZP is composed of circular rings that alternate in opaque and transparent regions. Figure 32 shows a simple FZP. The opaque (black) rings are analogous to the blocking areas of a grating structure, and the transparent (white) rings are analogous to the slit openings of a grating structure. Furthermore, each ring is called a zone.

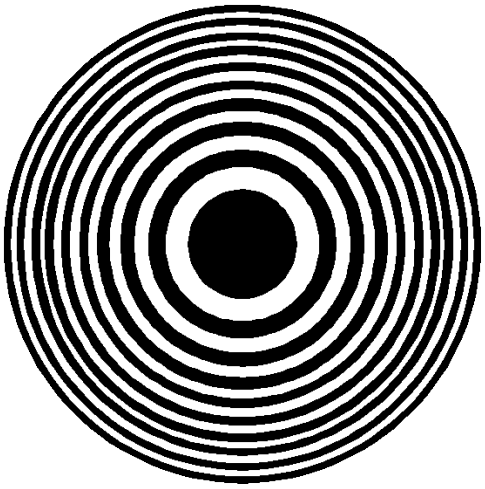

Figure 32. Fresnel zone plate [102].

The boundaries for the zones r_n are defined by [99]:

$$r_n^2 = n\lambda\left(f + \frac{n\lambda}{4}\right) \tag{25}$$

where, n is the zone number, and f is the focal length. Therefore, the width for each zone is determined by the difference in the adjacent radii (Figure 33).

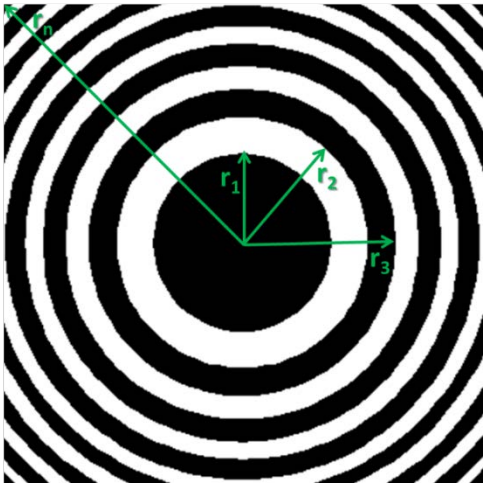

Figure 33. FZP zones are defined by the radii [102].

Because the calculated radii are dependent on the wavelength and the focal length, the focal length will change when the wavelength changes. Therefore, the FZP functions well for one wavelength but acts like a filter for other wavelengths [103].

2.2.7 The Ge/GeTe PN-Junction

GeTe is a p-type semiconductor with phase change properties [13, 104] which has the ability to switch from an amorphous phase (a-GeTe) to a crystalline

phase (c-GeTe) upon heating of the lattice. This heating can be accomplished through various methods, like direct heating on a hotplate [13] or via voltage pulses [105, 13]. A-GeTe is highly resistive and acts like an insulator, but c-GeTe is highly conductive and acts more like a metal. However, c-GeTe "always displays p-type metallic conduction" [104].

Therefore, just as a pn-junction is formed with n-type and p-type doped silicon, p-type c-GeTe can form a pn-junction on an n-type germanium substrate. This can be accomplished using a GeTe target, and depositing a-GeTe via radio frequency (RF) sputtering followed by crystallization into c-GeTe on a hotplate.

2.3 Summary

This chapter presented the necessary theory and background information on solar cell fundamentals and the seven focus areas of diffraction pattern generation, photon propagation, silicon diffusion processing, ohmic contacts, the distributed Bragg reflector, the Fresnel zone plate, the Ge/GeTe pn-junction.

III. METHODOLOGY

3.1 Hybrid Multi-Junction Silicon Germanium (HMJ-SiGe) Solar Cell

It was proposed that an improved architecture be explored. The HMJ-Si solar cell design was based on two silicon wafers stacked on top of each other. This configuration was a multi-junction design, but it centered around the bandgap of silicon only. In this work, a new multi-junction design was explored using a bottom n-type germanium (n-Ge) substrate with a pn-junction formed by a thin film of c-GeTe. Because germanium has a bandgap of 0.69eV, or 1800nm in wavelength, this new HMJ-SiGe solar cell architecture has the potential to convert photons into electricity over a spectral range that is not readily absorbed by silicon, around 1100nm – 1800nm.

3.2 Diffraction Pattern Generation

Diffraction pattern generation had a significant emphasis in the HMJ-Si solar cell. The contact grating designs were designed such that the metal fingers on the top side of the bottom wafer would be placed in between the maxima areas of the interference pattern generated on the surface.

To understand this characteristic, the location of the maxima needed to be identified. Utilizing equations (13) and (14), a spreadsheet was developed to find the distance of five orders of maxima from an arbitrary grating slit location based on the final specifications of the HMJ-Si solar cell. Because the HMJ-Si solar cell was designed around the silicon bandgap of ~1100nm, this evaluation was

accomplished between 900-1200nm. Furthermore, this was accomplished for three different air gap thicknesses of 100um, 385um, and 500um. Simple xy-scatterplots (Figures 43-45) were generated to visually understand the effect of wavelength on multi-order maxima locations.

3.3 Photon Propagation

MATLAB software code [106], was obtained to simulate photon propagation through the HMJ-SiGe solar cell architecture. It was written to implement RCWA with the enhanced transmittance matrix method and solve reflection and transmittance scattering parameters of transverse magnetic (TM) and transverse electric (TE) electromagnetic waves. However, only TM polarization was considered in the simulations, because it was found to possess "higher photoresponsivity than TE" polarization [107]. Although this software program analyzes the scattering of electromagnetic waves through periodic grating structures, the reflection and transmittance solutions do not take into account the absorption of photons in creating EHPs but only internal losses. These solutions are only based on the diffraction of electromagnetic waves as they propagate through a medium.

The RCWA MATLAB software program simulates and analyzes diffraction through a unit cell. A unit cell is the basic pattern of a periodic structure. The layers depicted in Figure 22 (see 2.2.2) can be represented as a repetition of a unit cell composed of 3 layers- a top metal and air layer, a middle silicon layer, and a bottom

metal layer (Figure 34). The resulting reflection and transmittance solutions produced for one unit cell can be represented for the entire layered structure.

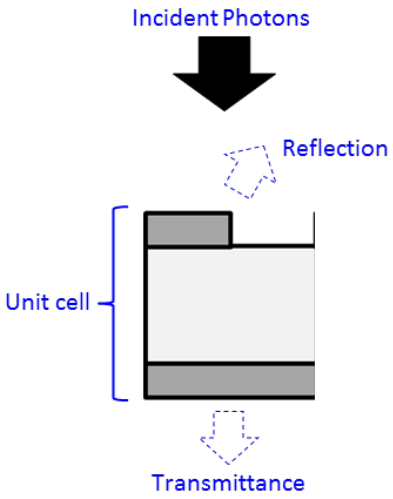

Figure 34. Unit cell illustration. Unit cell is a portion of a periodic structure that can be analyzed for reflection and transmittance solutions.

The objective was to characterize how the metal electrical contact gratings affect propagation through the HMJ-SiGe solar cell architecture at different wavelengths. The goal was to determine the design specifications for maximum possible absorption around the silicon and germanium bandgaps only. The determining criteria for achieving this goal was based on the resulting reflection and transmission solutions solved by the software program. Therefore, the criteria that was developed was: 1) maximum reflection and minimum transmittance from 0.3 – 1.0um, and 2) minimum reflection and maximum transmittance from 1.0 – 1.8um.

The reasoning for this criterion is based on the fact that heat hinders the efficiency of solar cells. Although silicon will absorb photons in the shorter wavelengths well above the silicon bandgap, the excess energies will be absorbed as

unnecessary heat. Although the same principle applies to the germanium substrate, it was anticipated that the air gap in between the two wafers will mitigate the thermal degradation effects by a temperature differential of about 2°C [12].

The architecture layers of the HMJ-SiGe solar cell were divided up into 3 unit cells (Figure 35) for RCWA simulations. The first unit cell configuration was composed of three layers- air/metal layer, silicon layer, and air/metal layer. The second unit cell configuration was composed of two layers- germanium layer and air/metal layer. Finally, the third unit cell configuration was composed of three layers- air/metal layer, air layer, and air/metal layer.

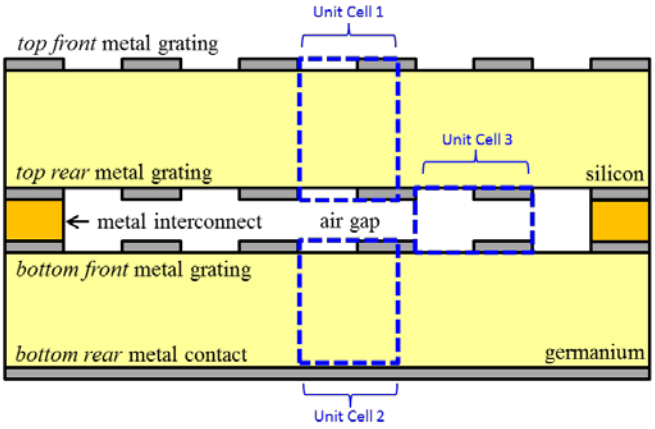

Figure 35. HMJ-SiGe solar cell architecture with three unit cells. These unit cells were defined for rigorous coupled wave analysis simulation.

A number of architectural parameters were varied during simulations of each unit cell configuration depending on the objective, including unit cell width, metal contact width, substrate thickness, metal contact thickness, beginning wavelength, and ending wavelength. Already defined and kept static in the software coding, the tilt of incidence was varied from 0° - 60° for each simulation.

The objective of the first and second unit cells were to determine the configuration of architectural parameters that satisfied the criteria specified above. The objective of the third unit cell was to determine the effect on the metal locations within the air gap of the top and bottom substrates in relation to each other. Figure 36 and Table 2 summarizes the architectural parameters that were varied for each configuration simulated. Furthermore, the column labels in Table 2 are illustrated in Figure 36.

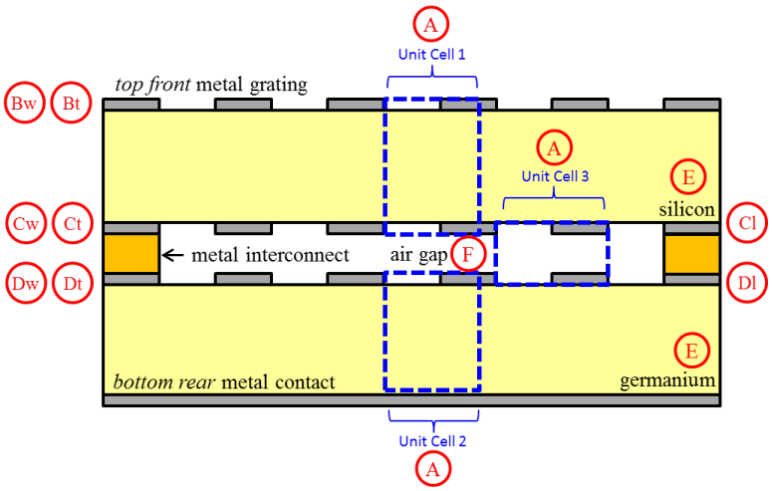

Figure 36. Architectural parameters varied for each configuration simulated. A: unit cell width. Bw, Bt, Cw, Ct, Dw, Dt: respective metal width and metal thickness. Cl, Dl: respective metal locations. E: substrate thickness. F: air gap thickness.

Table 2. Architectural parameters varied in RCWA simulation. For explanation of the column labels, see Figure 36.

Configuration	A	Bw	Bt	Cw	Ct	Cl	Dw	Dt	Dl	E	F
Unit Cell 1	✓	✓	✓	✓	✓					✓	
Unit Cell 2	✓						✓	✓		✓	
Unit Cell 3	✓				✓			✓	✓		✓

As can be seen from Figure 36, the Unit Cell 1 configuration is a 3-layer unit cell that analyzes just the top wafer. Likewise, Unit Cell 2 configuration analyzes just the

bottom wafer. Lastly, Unit Cell 3 configuration analyzes just the air gap region affected by the location of the metal contacts.

3.4 Silicon Diffusion Processing

The ultimate goal for the diffusion study was to create a diffusion profile process follower for n-type and p-type silicon wafers with the intention for utilization of in-house fabrication and for contracting of external fabrication services. Because of a working relationship developed with the faculty members at the Lurie Nanofabrication Facility at the University of Michigan, silicon diffusion processing was purchased and conducted at the university. Using the information presented in the background of this paper, the reasoning for determining the individual process requirements is conveyed. Table 3 summarizes the steps accomplished to develop the diffusion profile process follower for p-type and n-type silicon wafers. The resulting process followers can be found in the appendix of this thesis.

Table 3. Process Follower Development Steps.

#	**Steps to Develop**
1	pn-junction depth
2	emitter sheet resistance
3	emitter temp/time
4	BSF temp/time
5	EBSF time/temp
6	oxide thickness
7	PSG/BSG etch rates
8	oxide etch rates

The target pn-junction depth was chosen with a range of 0.5um – 1.5um. The decision for this was based on the previous design of the HMJ-Si solar cell [12] which was based on a 1.5um depth. Because the original intent was to incorporate a DBR into the final architecture of the HMJ-SiGe solar cell to mitigate unnecessary heat from the much shorter wavelengths, diffusion requirements for industry-standard, shallow junction depths were precluded for a deeper junction depth.

The emitter sheet resistance was chosen to be 50Ω/□, because this sheet resistivity is typical in commercially manufactured solar cells and is a good compromise between dopant surface concentration and providing for low metal contact resistance [74]. Furthermore, this value was chosen with the intent of etching back the emitter surface (see 2.2.3) to about 100Ω/□ [21] in order to reduce surface recombination in between the metal contacts but not the low metal contact resistance.

To accomplish an emitter sheet resistance of 50Ω/□, the temperature and time of the diffusion was referenced from the manufacturing data sheet of the dopant sources to be used. For the p-type wafer, it was known that the liquid phosphorous source $POCl_3$ would be utilized in the thermal furnace. According to Figure 24, the temperature and time required was 850°C for 30 minutes followed by a 10 minute drive-in. The dopant concentration on the surface was calculated and expected to be no less than 3.80×10^{15} cm^{-3}.

The BSF and EBSF diffusion requirements were arbitrarily determined by the required temperatures and times needed to create a step profile. In other words, in the case of the EBSF, the first diffusion needed to be at a lower dopant concentration

than the second diffusion to create a step potential, or basically another electric field that helps keep minority carriers from recombining at the rear surface [108]. Depending on the available dopant source, the sheet resistance of the BSF was expected to be around 8-12 Ω/□, and the EBSF was expected to have a sheet resistance of around 2-5 Ω/□. The temperatures and times to process these diffusion profiles were determined by the manufacturing data sheet. For the case of the BSF, the temperature and time required were 1050°C for 30 minutes of deposition and 10 minutes of drive-in or 1100°C for 30 minutes of deposition and 10 mins of drive-in, depending on the available dopant source. For the case of the EBSF, the temperature and time required were 1100°C for 60 minutes of deposition only or 1150°C for 60 minutes of deposition only, depending on the available dopant source.

The oxide thickness, which is a necessary process step to protect the side of the wafer that should not receive any dopant contamination (i.e. accidental phosphorus n-type dopants on the p-type side), can be determined by Figure 26. Based on the temperatures and times required for the formation of the emitter, BSF, and EBSF, it was determined that 200nm of oxide was sufficient for protection during the diffusion processing.

The oxide etch rates were determined from several online resources [109, 110] that stated the etch rate for standard buffer oxide etch (5:1) to be around 100nm per minute.

Post-diffusion testing of the pre-metallized wafers was accomplished using a four point probe to measure the sheet resistance and then calculated for the surface dopant concentration. Table 4 shows the post-diffusion silicon wafers tested.

Table 4. Post-diffusion testing of processed p-type silicon wafers.

#	Dopant Type	Rear Surface
P15	p-type	BSF
P19	p-type	EBSF

3.5 Ohmic Contacts

The HMJ-SiGe solar cell design is based on a top p-type silicon wafer and an n-type germanium wafer. The silicon wafer contains a pn-junction formed by an n-type emitter, and the germanium wafer contains a rear pn-junction formed by p-type GeTe. Therefore, there were four different metal-semiconductor configurations considered for creating ohmic contacts- 1. metal/n-Si (top), 2. metal/p-Si (bottom) , 3. metal/n-Ge (top), and 4. metal/p-GeTe (bottom). The semiconductor substrates used were a 4-inch, p-type silicon wafer processed according to developed diffusion profile requirements at the University of Michigan Lurie Nanofabrication Facility (see appendix) and a 2-inch, n-type germanium wafer that was single-sided polished and about 350μm in thickness. A four-point probe was used on the first three configurations to measure the sheet resistance, and the respective surface concentrations were calculated using the online calculator [72]. The semiconductor work functions were calculated for each side of the silicon wafer and germanium wafer. Because crystallized p-GeTe is not a dopant to the

germanium lattice, the work function determined from literature [105] was found to be 4.9eV. Based on this data and the metal work functions presented in the background, the appropriate metals that should be used to form ohmic contacts were determined. After the metals were deposited, a 60-second rapid thermal anneal at 250°C of the test pieces were accomplished, with exception to the n-Ge test piece. Table 5 shows these parameters, calculated values, and chosen metal.

Table 5. Calculated Work Functions.

#	Configuration	Sheet Resistance (Ω/□)	Surface Concentration (10^{-3})	Calculated Work Function (eV)	Metal
1	metal/n-Si (top)	30	$6.77x10^{15}$	4.27	Aluminum
2	metal/p-Si (bottom)	2.1	$7.96x10^{17}$	5.07	Gold
3	metal/n-Ge (top)	2.2	$1.94x10^{16}$	4.17	*See Table 3*
4	metal/p-GeTe (bottom)	N/A	N/A	4.9 [105]	Gold

For configuration #3, because all of the metals available exceeded the work function of n-Ge and that n-Ge is known for Fermi level pinning near the valence band edge, an interfacial layer was needed in between the n-Ge and the metal to help lower the Schottky barrier height (see 2.2.4). Table 6 shows the interfacial material and metal chosen for testing.

Table 6. Interfacial layer and metal chosen with n-type germanium

#	Configuration	Interfacial Layer & Thickness (nm)	Metal
3A	metal/n-Ge (top)	Al_2O_3 (3nm)	Aluminum

The contact resistance for each configuration was calculated using TLM. Two contact resistance pad masks were fabricated, and each configuration was patterned with one of these masks using standard lithography techniques.

The first mask contained a series of contact pads (100um x 100um) with distances of 20um, 40um, 60um, 80um, and 100um separation between contiguous pairs of pads. The second mask, a more improved version, contained a series of large contact pads (1000um x 1000um) with distances of 50um, 75um, 100um, 125um, and 150um separation between contiguous pairs of pads.

Using an HP4155A Semiconductor Parameter Analyzer, voltage and current measurements were taken to calculate the total resistance between the pads. Then, a spreadsheet was used create an xy-scatterplot of the calculated total resistances at each spacing distance, like the example depicted in Figure 37. Because the contact resistance is half of the resistance value found at x_0, the spreadsheet trendline function was used to determine $2R_{pad}$.

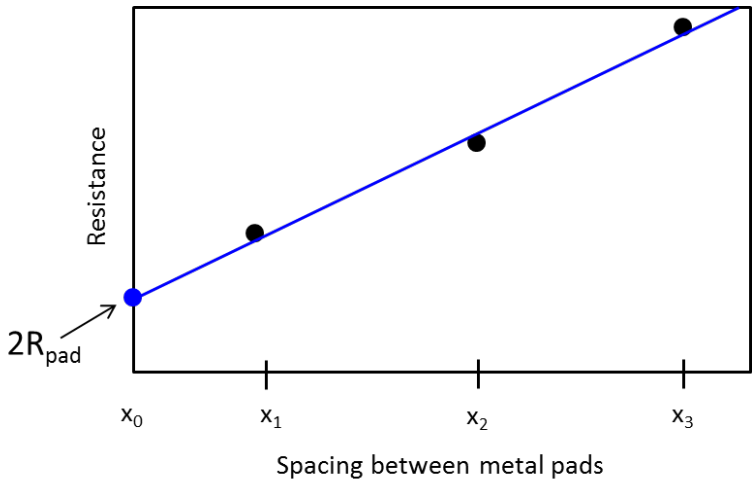

Figure 37. Total resistance between metal pads at various distances [88].

3.6 The Distributed Bragg Reflector

Simulations of DBRs were accomplished using a software program code obtained a MATLAB toolbox posted online [98]. Based on the material refractive indices and target wavelength input parameters, the software program generated line graphs of wavelength versus reflectance (see 4.3.1). The material thicknesses were already defined and kept at one-quarter wavelength for each simulation.

The choices of dielectric material was restricted to what was available in the PECVD at AFIT- a-Si, Si_3N_4, and SiO_2. Then, the refractive indices for each material at their respective wavelengths were attained from an online refractive index database [93]. The target wavelengths chosen were 400-700nm, to reduce the unnecessary heat caused by photon energies far above the bandgap of silicon. Table 7 summarizes the parameters simulated.

Table 7. Distributed Bragg reflector simulations. These simulations were varied by wavelength, material configuration and their refractive index

		Refractive Indices at Target Wavelength		
#	Wavelength (nm)	a-Si / Si_3N_4	a-Si / SiO_2	Si_3N_4 / SiO_2
DBR1	400	4.27/ 2.07	4.27/ 1.49	2.07 / 1.49
DBR2	500	4.47 / 2.03	4.47 / 1.48	2.03 / 1.48
DBR3	600	4.28 / 2.01	4.28 / 1.48	2.01 / 1.48
DBR4	700	4.07 / 2.00	4.07 / 1.47	2.00 / 1.47

After the simulations were accomplished, a 10-layer DBR was fabricated in the PECVD on a 980um-thick, double-sided polished silicon substrate using the dielectrics that provided the best overall coverage of the target spectrum without increasing the reflectance near the silicon band gap. Then, a bare 3mm thick silicon substrate for baseline data and the DBR-layered substrate were individually tested for transmittance and reflectance with the Cary 5000 spectrometer in the spectral range of about 250um-3000um.

3.7 The Fresnel Zone Plate

A Fresnel zone plate (FZP) was originally designed with three intentions: 1) focus longer wavelength photons to the germanium substrate, 2) reflect shorter wavelengths back into the top silicon wafer, and 3) accomplish 1 and 2 while functioning as the top rear contact grating in the HMJ-SiGe solar cell architecture.

Using the design equations, a spreadsheet was created to calculate and graph the specifications of the FZP. A target wavelength of 1200nm was chosen to allow the lower energy photons to pass through and enter the bottom germanium lattice.

The FZP was designed with an outer diameter of 38.1mm (1.5in). Based on these parameters, it was determined by spreadsheet that the maximum number of zones was 30 (Figure 38). The zone radii calculated were used to fabricate an FZP mask. Because the bottom germanium wafer of the HMJ-SiGe solar cell architecture was two inches in diameter, a silicon wafer of the same diameter was used to fabricate the FZP on and for later testing. A pyranometer in conjunction with the solar simulator under standard test conditions were used to measure the resulting solar irradiance transmittance through the FZP silicon wafer, as well as a bare silicon wafer for a baseline reference (Table 8).

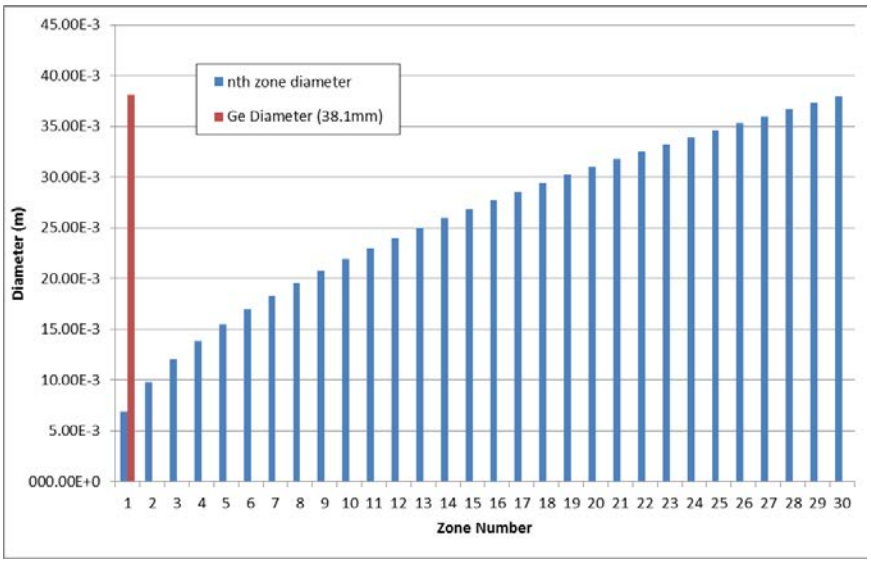

Figure 38. Spreadsheet calculations of Fresnel zone plate design.The number of possible zones and the radius of each zone was determined.

Table 8. Fresnel Zone Plate Test

#	Configuration	Test Data
FZP1	bare silicon	Irradiance transmittance
FZP2	1200nm, silver	Irradiance transmittance

3.8 The Ge/GeTe PN-Junction

Because c-GeTe is a p-type semiconductor, the possibility of using this as a thin film to form a pn-junction with n-Ge was explored. Electrical and optical properties were investigated first, followed by pn-junction formation testing.

The testing was conducted into three phases: 1) transmittance and transitioning properties, 2) pn-junction orientation, and 3) film thickness. The objective the first phase was to determine the temperature at which a-GeTe transitions to c-GeTe relative to various film thicknesses and to measure the transmittance of the various thicknesses of GeTe in the amorphous and crystalline phases. The objective of the second phase was to determine the location of the c-GeTe thin film that results in the best absorption of incident photons. Finally, the objective of the third phase was to determine the best thickness in forming the pn-junction.

1) Transmittance and Transitioning Properties: Because crystalline silicon wafers have high absorption in the wavelengths above 1100nm, quartz wafers were used so that good data could be acquired from the spectrometer measurements. Seven 2cm x 2cm quartz test pieces were made by using a dicing saw. Various a-GeTe thicknesses were deposited by RF sputtering. Before phase transitioning, each a-GeTe test piece was measured for transmittance by using the Cary 5000 spectrometer from 250nm-3000nm. Afterwards, each test piece was placed on the hotplate of the micromanipulator probe station for electrical conductivity measurements as the hotplate surface temperature was incrementally increased.

Resistance and transition temperature data were recorded. After the a-GeTe had transitioned into c-GeTe, each quartz test piece was again measured for transmittance in the spectrometer. Table 9 summarizes the test pieces.

Table 9. Phase 1 of GeTe testing for transitioning and transmittance properties.

#	GeTe thickness (nm)
G1	150
G2	100
G3	50
G4	25
G5	10
G6	5
G7	2

2) PN-Junction Orientation: Four test pieces were created from cleaved n-Ge substrates, unpolished on both sides, and about 500μm in thickness. Two pieces had GeTe deposited on the top side (250nm and 600nm), and the other two pieces had GeTe deposited on the bottom side (250nm and 600nm).

3) Film Thickness: Three test pieces were created from cleaved n-Ge substrates, single-sided polished, and about 350μm in thickness. GeTe was deposited on the bottom side of all three test pieces (50nm, 150nm, and 350nm).

For phases 2 and 3, each test piece was evaluated on the amount of Voc and Isc produced under a solar simulator. Standard test conditions (see 2.1.6) were employed, and temperature control was accomplished a thermoelectric cooler connected to the testing platform. A thermocouple provided temperature measurements, and a power supply connected to the thermoelectric cooler was continually adjusted to maintain the proper temperature during testing.

Furthermore, since each test piece was not identical in shape or size, an aluminum plate with a 6.4mm circular aperture was utilized to ensure same amount of light was provided to each piece.

A layer of a-GeTe was deposited either on the top side or the bottom side via RF sputtering. Then, each test piece was placed on a hotplate for 2 minutes with the temperature set to 300°C to transition the a-GeTe to c-GeTe. Afterwards, a thin amount of S1818 photoresist was applied by a cotton swab to most of the top surface, leaving a thin strip for evaporation of the top gold metal contact. The entire bottom side metal contact was processed with evaporated gold. Table 10 summarizes these test phases.

Table 10. Phases 2 & 3 of GeTe testing for pn-junction orientation and thickness.

#	Test Phase	PN-junction	GeTe (nm)
Ge-A1	Orientation	Top	250
Ge-A2	Orientation	Top	600
Ge-A3	Orientation	Rear	250
Ge-B1	Thickness	-	50
Ge-B2	Thickness	-	150
Ge-B3	Thickness	-	350

3.9 HMJ-SiGe Solar Cell Testing

The top p-type silicon wafer, serialized as P19B, was further processed for metallization and an ARC. However, the silicon wafer was damaged during processing, resulting in about a 21% loss in the photovoltaic surface. The bottom n-type germanium wafer was processed for deposition of p-type c-GeTe to form the

pn-junction and metallization. These additional processing are outlined in process followers, which can be found in the appendix.

Before both wafers were assembled into the HMJ-SiGe solar cell architecture, individual testing was required. The top silicon wafer was tested once under the solar simulator at standard test conditions for V_{oc}, I_{sc}, fill factor, and efficiency. Then after a 30-minute cool off period, the silicon wafer was tested again. Next, the silicon wafer was tested for endurance under continuous solar illumination for two hours without temperature control to briefly simulate a solar cell outdoors in constant sunlight. V_{oc}, I_{sc}, fill factor, and efficiency were measured and calculated once every hour. Likewise, the bottom germanium wafer was tested twice, with a 30-minute cool down period in between, under the solar simulator at standard test conditions recording the same metrics and by the same two-hour endurance test process.

Afterwards, the two semiconductor wafers were assembled in a locally fabricated fixture (Figure 39). Developed by an AFIT graduate student, this device was designed to enable sufficient mechanical contact to the wafer metal contacts during testing, and it provided an efficient solution to portability without separating the architecture. Furthermore, the printed circuit board material that functions as electrical contact layers to the wafers within the fixture also allows for airflow and thermocouple access into the airgap. Each layer contains at least one contact tab to solder a wire to for ease and flexibility in accomplishing electrical connections.

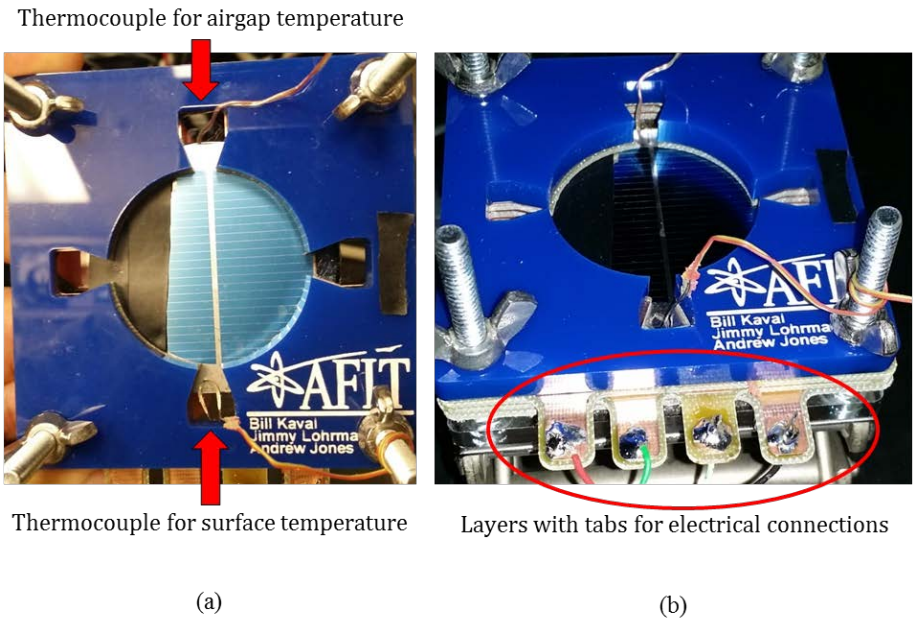

Figure 39. The HMJ-SiGe solar cell fixture. This allowed for thermocouple access, flexibility in electrical connections, and ease in portability of the architecture.

After the HMJ-SiGe solar cell was assembled in the solar cell fixture, it was placed under the solar simulator for setup with the other required test equipment, as illustrated by the schematic in Figure 40. The Agilent E3631A DC Power Supply, Agilent 34410A LXi Digital Multimeter, and Agilent 34401A Digital Multimeter were connected to LabVIEW via a GPIB cable. The 34401A was used to measure the V_{oc}, and the 34410A was used to measure the I_{sc}. The inputs to these multimeters were connected to a 5VDC momentary single-pole, double-throw (SPDT) relay. The DC power supply was used to actuate this relay. Because the two semiconductor wafers are encased by acrylic plates, temperature control at the standard test condition of 25°C was not possible. Then, timed endurance test program (Figure 41) was developed in LabVIEW to control the required individual test equipment and the test duration.

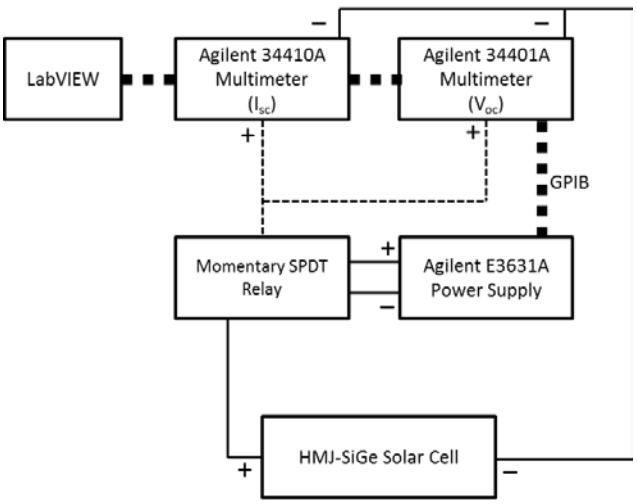

Figure 40. The endurance test setup. LabVIEW was used to communicate with the multimeters and the power supply via the GPIB cable. A momentary single-pole, double-throw (SPDT) relay was actuated by the power supply to allow for the multimeters to measure V_{oc} and I_{sc} from the HMJ-SiGe solar cell.

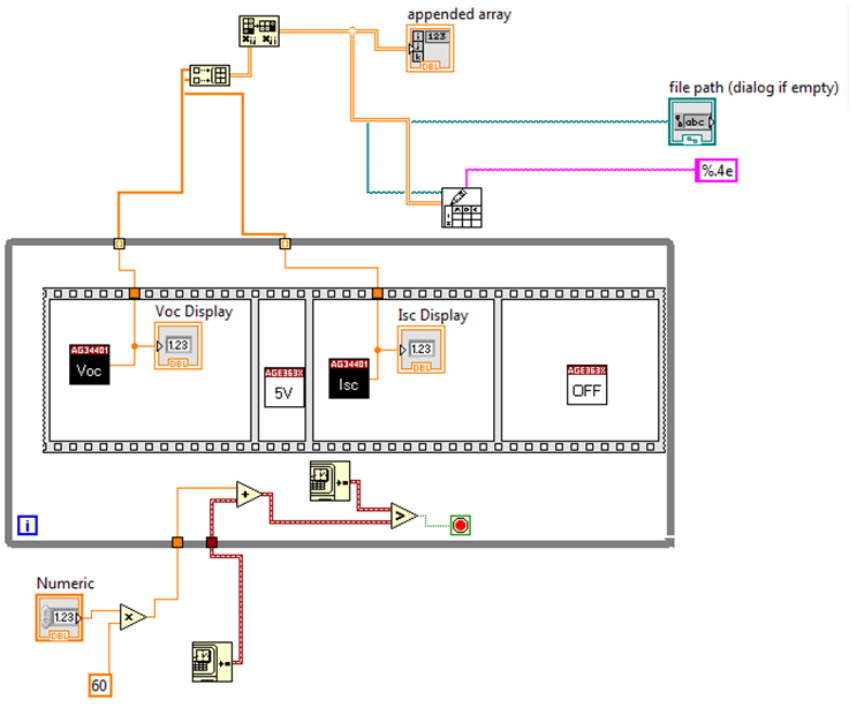

Figure 41. LabVIEW graphic code for timed endurance test. This was programmed to communicate with two multimeters and a power supply to measure V_{oc} and I_{sc} over a specified time in minutes

The operation of this endurance test was conducted as follows: 1) User inputs the time duration of the test in minutes into the LabVIEW program and then runs the program. 2) With the power supply output off, LabVIEW commands the 34401A to read the V_{oc} and records the value to memory. 3) LabVIEW commands the power supply to output 5VDC. 4) The relay actuates 5) LabVIEW commands the 34410A to read the I_{sc} and records the value to memory. 6) LabVIEW commands the power supply output off . The sequence from steps 2 – 6 repeats until the time duration has expired. After the time has expired, all of the V_{oc} and I_{sc} values were written to a text file and saved a folder on the computer.

The HMJ-SiGe solar cell was tested for endurance without temperature control for 60 minutes using the timed endurance test program in LabVIEW. The temperatures of the silicon surface and the air gap were recorded at the beginning of the test and every 15 minutes thereafter.

Finally, as a capstone to the operation and potential of the HMJ-SiGe solar cell, a low-voltage power controller circuit (Figure 42) was connected to the architecture. This external circuit was designed and fabricated to enable the HMJ-SiGe solar cell to charge an in-circuit capacitor and power an on-board, surface-mounted LED. A schematic of the circuit can be found in the appendix. Wires that were soldered to the solar cell fixture were inserted into electrical connectors, observing polarity. The HMJ-SiGe solar cell and the solar cell fixture was placed under the solar simulator to charge the in-circuit capacitor. Charge timing was recorded. Afterwards, the and the on-board switch was turned ON to allow the capacitor to illuminate the LED. As a comparison with other sources of light, the

HMJ-SiGe fixture, the low-voltage power controller, and a handheld Fluke 289 digital multimeter were used to measure the V_{oc}, I_{sc} and charging rate outside of the AFIT building and then under the florescent lighting inside the testing lab.

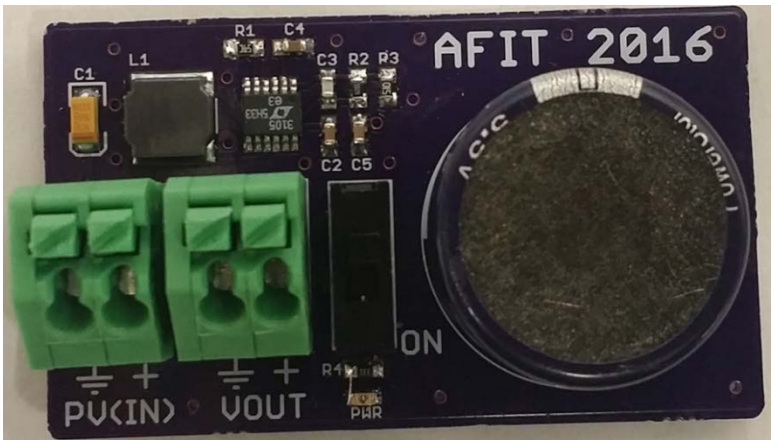

Figure 42. Low-voltage power controller circuit. This circuit was used to charge the capacitor by the HMJ-SiGe solar cell. When the on-board switch is actuated, the energy stored in the capacitor is used to light a surface mount light emitting diode.

3.10 Summary

This chapter presented the methodology employed to the seven focus areas of diffraction pattern generation, photon propagation, silicon diffusion processing, contacts, the distributed Bragg reflector, the Fresnel zone plate, the Ge/GeTe pn-junction.

IV. RESULTS

4.1 Overview

This chapter provides the data and results obtained during testing of the topics studied. The structure of this chapter (4.2 - 4.9) matches the methodology (3.2 - 3.9) and analysis (5.2 - 5.9) chapters of this thesis.

4.2 Diffraction Pattern Generation

The diffraction pattern was a key emphasis in the design of the HMJ-Si solar cell. Equations for finding the locations of several orders of maxima from an arbitrary grating slit were utilized in a spreadsheet to generate a simple xy-scatterplot of the resulting calculations. Results are displayed in Figures 43-45. These figures show the locations of the generated diffraction pattern maxima up to six orders, across a spectral range of 900-1200um and varied by air gap thickness.

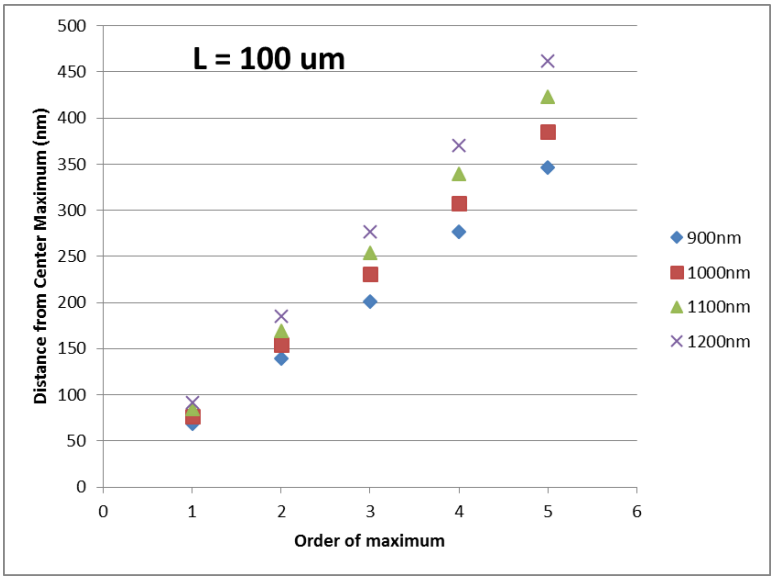

Figure 43. Maxima locations with 100um airgap.

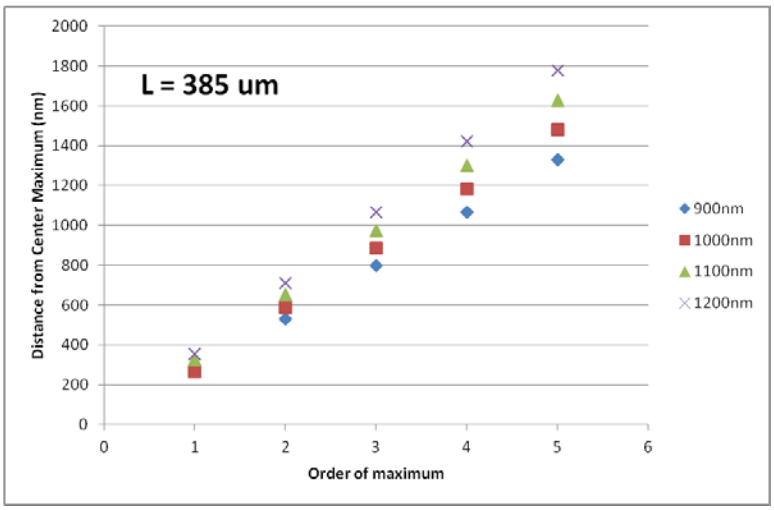

Figure 44. Maxima locations with 385um airgap.

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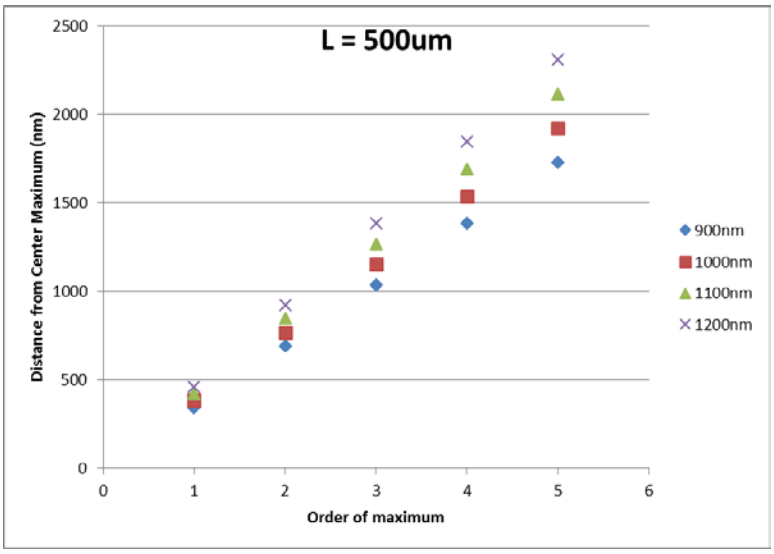

Figure 45. Maxima locations with 500um airgap.

4.3 Photon Propagation

Study of the electrical contact grating utilized in the HMJ-SiGe solar cell architecture was accomplished by RCWA simulation in MATLAB. The reflection and transmittance values were captured across a portion of spectrum for each unit cell configuration. The simulation outputs were written to a text file for identifying the architectural parameters that achieved the criteria specified in 3.3.

Because a large amount of data was generated from these simulations, it was necessary to target logical points of interest for evaluation. In other words, to achieve the intended objective and goals set forth in this study, certain portions of the wavelengths simulated were deemed much more important than others, which will be explained with each configuration below.

In the case of the Unit Cell 1 configuration, which consists of the top silicon substrate, the wavelengths most important are 1.0 to 1.1 um, which is just above the silicon band gap. Therefore, the structural parameters identified for achieving the criteria of maximum transmittance and minimum reflectance served as a basis for evaluation of data points in the other wavelengths

The architectural parameters that achieved maximum transmittance identified in Table 11 were used to observe the transmittance and reflection calculated in the other wavelengths at those same parameters. This was accomplished with the objective of determining whether or not the electrical contact grating design specifications that resulted in maximum transmittance in the 1.0 – 1.8um range would also result in a maximum reflectance in all other regions of

the spectrum. The other wavelengths considered and their respective calculated transmittance and reflections are displayed in Table 12.

Table 11. Unit Cell 1 architectural parameters. Based on maximum transmittance. A: unit cell width. Bw, Bt, Cw, Ct, Dw, Dt: respective metal width and metal thickness. E: substrate thickness. F: air gap thickness.

Wavelength (um)	A	Bw	Bt	Cw	Ct	Dw	Dt	E	F	Max T	Min R
1.0-1.1um	2000	50	0.1	50	0.3	-	-	250	-	0.9676	0.0319

Table 12. Evaluation data points for minimum transmittance. Minimum transmittance required in the shorter-wavelength regions of the spectrum. Maximum transmittance required in the longer-wavlength regions of the spectrum.

Wavelength (um)	Avg T	Avg R
0.3-0.4	0.8871	0.0397
0.5-0.6	0.9585	0.0377
1.3-1.4	0.9606	0.0390
1.7-1.8	0.9633	0.0363

In the case of the Unit Cell 2 configuration, which consists of the bottom germanium substrate, the significant wavelengths are between the silicon band gap and the germanium band gap of 1.0 – 1.8um. The criteria established for this range of wavelengths were for maximum transmittance and minimum reflectance (Table 13).

Table 13. Evaluation data points between silicon and germanium band gaps.

Wavelength (um)	A	Dw	Dt	Max T	Min R
1.0-1.1	3000	150	0.1	0.6379	0.3558
1.1-1.2	4000	150	0.5	0.6384	0.3500
1.2-1.3	2500	100	0.5	0.6453	0.3519
1.3-1.4	3500	150	0.5	0.6491	0.3454
1.4-1.5	3500	150	0.5	0.6453	0.3466
1.5-1.6	3000	150	0.5	0.6479	0.3471
1.6-1.7	4000	150	0.7	0.6530	0.3442
1.7-1.8	4000	150	0.3	0.6552	0.3423

In the case of the Unit Cell 3 configuration, which consists of the top rear metal grating and the bottom front metal grating within the air gap, the intent was to determine how the transmittance and reflectance are affected by the locations of the metal grating within the air gap.

It was decided that the target logical points of interest for Unit Cell 3 configuration were how the location of the bottom metal (Dl) and the thickness of the air gap affected the transmittance and reflectance values for a small unit cell of 2000um and for a large unit cell of 5000um. With the top metal location held in place, the bottom metal location was varied. Tables 14-19 display the values attained in relation to the architectural parameters that were varied.

Table 14. Evaluation data points for small unit cell width. (A). Location of bottom metal (Dl) is varied 100um – 1700um. Air gap thickness (F) is kept constant.

A	Dl	F	Avg T	Avg R
2000	100	100	0.8020	0.1091
2000	300	100	0.7512	0.1826
2000	500	100	0.7595	0.1842
2000	700	100	0.7615	0.1844
2000	900	100	0.7620	0.1846
2000	1100	100	0.7618	0.1848
2000	1300	100	0.7607	0.1852
2000	1500	100	0.7569	0.1859
2000	1700	100	0.7508	0.1857

Table 15. Evaluation data points for small unit cell width. (A). Air gap thickness (F) is varied. Location of bottom metal (Dl) is kept constant near left edge of unit cell.

A	Dl	F	Max T	Max R
2000	100	100	0.8020	0.1091
2000	100	300	0.7971	0.1123
2000	100	500	0.7805	0.1356
2000	100	700	0.7765	0.1485
2000	100	900	0.7728	0.1585

Table 16. Evaluation data points for small unit cell width. (A). Air gap thickness (F) is varied. Location of bottom metal (Dl) is kept constant near right edge of unit cell.

A	Dl	F	Max T	Max R
2000	1700	100	0.7508	0.1857
2000	1700	300	0.7786	0.1618
2000	1700	500	0.8017	0.1422
2000	1700	700	0.7958	0.1429
2000	1700	900	0.7798	0.1564

Table 17. Evaluation data points for large unit cell width. (A). Location of bottom metal (Dl) is varied 100um – 4700um. Air gap thickness (F) is kept constant.

A	Dl	F	Avg T	Avg R
5000	100	100	0.9002	0.0236
5000	300	100	0.8501	0.0263
5000	500	100	0.8404	0.0284
5000	700	100	0.8465	0.0269
5000	900	100	0.8475	0.0261
5000	1100	100	0.8500	0.0274
5000	1300	100	0.8502	0.0274
5000	1500	100	0.8518	0.0277
5000	1700	100	0.8502	0.0272
5000	1900	100	0.8518	0.0277
5000	2100	100	0.8513	0.0274
5000	2300	100	0.8509	0.0275
5000	2500	100	0.8523	0.0276
5000	2700	100	0.8502	0.0273
5000	2900	100	0.8522	0.0277
5000	3100	100	0.8507	0.0273
5000	3300	100	0.8507	0.0276
5000	3500	100	0.8520	0.0275
5000	3700	100	0.8483	0.0273
5000	3900	100	0.8513	0.0278
5000	4100	100	0.8476	0.0271
5000	4300	100	0.8424	0.0278
5000	4500	100	0.8436	0.0276
5000	4700	100	0.8731	0.0260

Table 18. Evaluation data points for large unit cell width. (A). Air gap thickness (F) is varied. Location of bottom metal (Dl) is kept constant near left edge of unit cell.

A	Dl	F	Max T	Max R
5000	100	100	0.9002	0.0236
5000	100	300	0.8831	0.0238
5000	100	500	0.8640	0.0241
5000	100	700	0.8528	0.0256
5000	100	900	0.8475	0.0261

Table 19. Evaluation data points for large unit cell width. (A). Air gap thickness (F) is varied. Location of bottom metal (Dl) is kept constant near right edge of unit cell.

A	Dl	F	Max T	Max R
5000	4700	100	0.8731	0.0260
5000	4700	300	0.8845	0.0256
5000	4700	500	0.8891	0.0247
5000	4700	700	0.8917	0.0247
5000	4700	900	0.8846	0.0249

4.4 Silicon Diffusion Processing

The effectiveness of the pn-junction, emitter, and back surface fields are dependent on the diffusion profile and process followers developed. The significance of the results become more weighted when the diffusion process is contracted to an external service provider, as in this case. Testing the surface dopant concentrations can give insight into whether or not the diffusion requirements were met. Table 20 displays the measured sheet resistances and the calculated surface dopant concentrations after post-diffusion.

Table 20. Measurements of post-diffusion p-type silicon wafers. Sheet resistances were measured using a four-point probe, and the dopant concentrations were calculated.

#	Dopant Type	Rear Surface	Sheet resistance (top)	Dopant Concentration (top)	Sheet resistance (bottom)	Dopant concentration (bottom)
P15	p-type	BSF	41.7 Ω/□	4.62×10^{15}	645 Ω/□	2.72×10^{14}
P19	p-type	EBSF	30 Ω/□	6.61×10^{15}	2.1 Ω/□	5.63×10^{17}

4.5 Ohmic Contacts

Low resistance ohmic contacts are necessary to maximize the collection of EHPs for accomplishing work. As described in the methodology (see 3.5), total resistance between contact pads were calculated and input into a spreadsheet. An xy-scatterplot was generated, as shown in Figure 46, and a trend line function was used to find the summation of the contact resistances for one pair of contact pads. Finally, the actual contact resistivity was calculated for each metal-to-semiconductor interface (Tables 21 and 22).

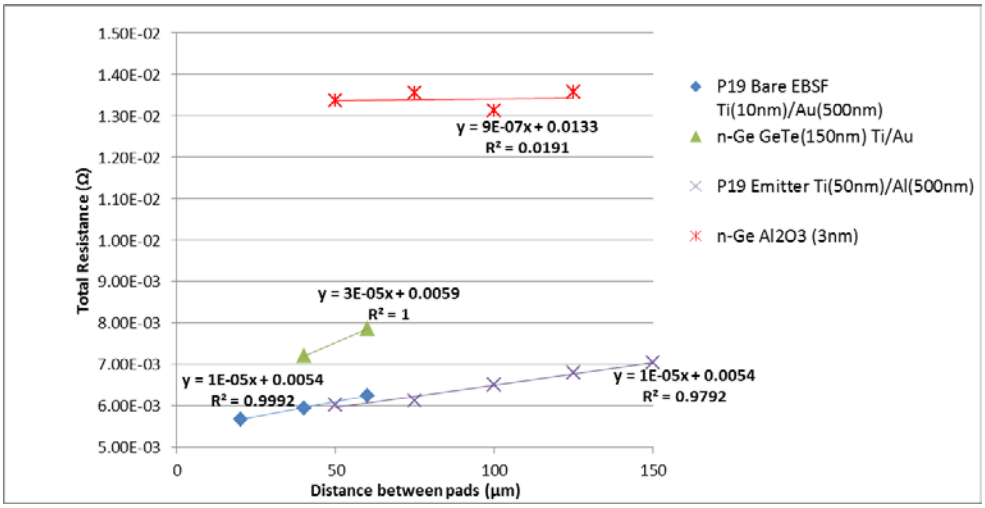

Figure 46. XY-scatterplot of calculated total resistance. The contact resistance was determined from trend line function of the spreadsheet.

Table 21. Calculated contact resistances of metal-semiconductor interfaces.

			Mask 1 Pad Spacing (um) Total Resistance (mΩ)					Mask 2 Pad Spacing (um) Total Resistance (mΩ)					
#	Config	Metal	20	40	60	80	100	50	75	100	125	150	Contact Resistivity ($\mu\Omega \cdot cm^2$)
1	metal/n-Si (top)	Al	-	-	-	-	-	6.02	6.13	6.52	6.79	7.04	27.0
2	metal/p-Si (bottom)	Au	5.68	5.95	6.25	-	-	-	-	-	-	-	38.9
3	metal/n-Ge (top)	*See Table 19*											
4	metal/p-GeTe (bottom)	Au	-	7.20	7.87	-	-	-	-	-	-	-	42.5

Table 22. Interfacial layer test plan for 3nm Al_2O_3 on n-Ge.

				Mask 2 Pad Spacing (um) Total Resistance (mΩ)					
#	Configuration	Interfacial Layer & Thickness (nm)	Metal	50	75	100	125	150	Contact Resistivity ($\mu\Omega \cdot cm^2$)
3A	metal/n-Ge (top)	Al_2O_3 (3nm)	Aluminum	13.4	13.6	13.1	13.6	-	66.5

4.6 The Distributed Bragg Reflector

Based on the input parameters from Table 6, the MATLAB software code generated 12 plots for evaluation of the DBR reflectance on versus wavelength. Two of these plots (Figure 47 and Figure 48) are shown. The remaining plots can be found in the appendix.

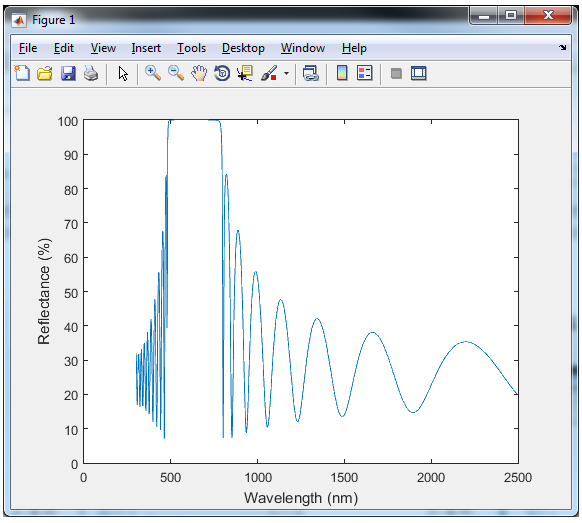

Figure 47. Reflectance of DBR using a-Si and Si3N4 at 600nm.

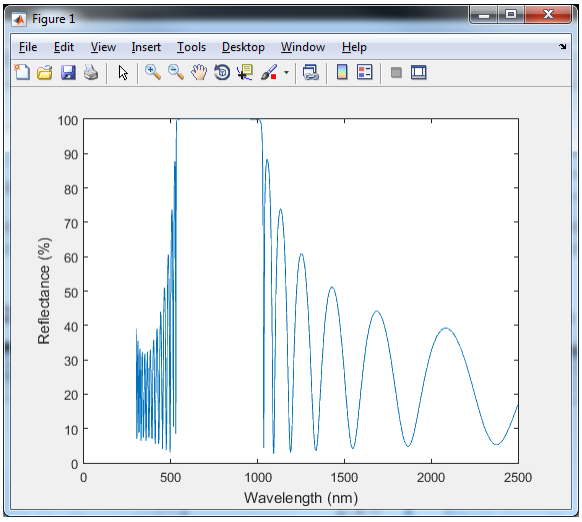

Figure 48. Reflectance of DBR using a-Si and SiO2 at 700nm.

After simulation of the DBRs were accomplished and results observed, a DBR stack of a target wavelength at 600nm was fabricated using 10 layers of alternating a-Si and Si_3N_4. Using the ARC thickness equation (11), the DBR stack was layered as illustrated in Figure 49. Transmittance data (Figure 50) was acquired between 200nm-3000nm using the Cary 5000 Spectrometer. Reflectance data could not be

accomplished, because there was a known issue with reflectance calibration of the spectrometer.

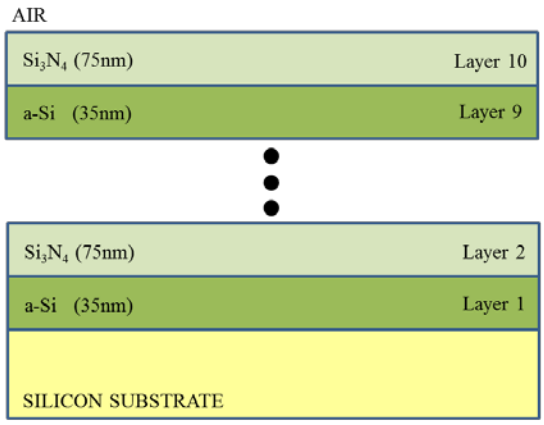

Figure 49. A 10-layer DBR fabricated by PECVD. Alternating layers of a-Si (35nm) and Si_3N_4 (75nm) with a target wavelength at 600nm were deposited on a 980um-thick, double-sided polished silicon substrate.

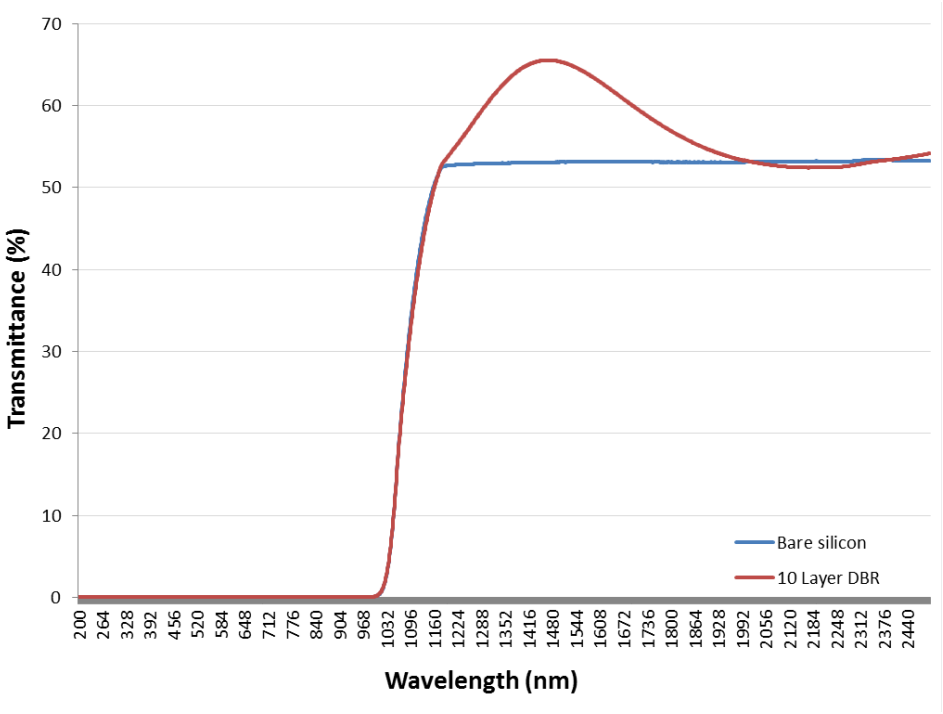

Figure 50. DBR Transmittance measurements. Measurements were accomplished on a bare silicon wafer for a baseline reference and a 10 layer DBR of alternating Si_3N_4 and a-Si material.

4.7 The Fresnel Zone Plate

The intent of the Fresnel zone plate was to focus unabsorbed incoming photons traveling through the silicon substrate and onto the bottom germanium surface. The FZP was designed for a target wavelength of 1200nm. Table 23 displays the solar irradiance measurements recorded for a bare silicon wafer and a silicon wafer with a 1.5in FZP patterned on the surface.

Table 23. Solar irradiance measurements. A bare silicon wafer was measured for baseline and compared with a silicon wafer with a Fresnel zone plate.

#	Configuration	Test Data	
FZP1	bare silicon	pyranometer	104W/m^2
FZP2	1200nm, silver	pyranometer	48W/m^2

4.8 The Ge/GeTe PN-Junction

To understand the pn-junction formed on n-type germanium with p-type c-GeTe, investigating the electrical properties, optical properties, pn-junction location, and film thickness were necessary. Four phases were accomplished, and the results are presented here in Figures 51-53.

Phase 1, Transmittance and Transitioning Properties:

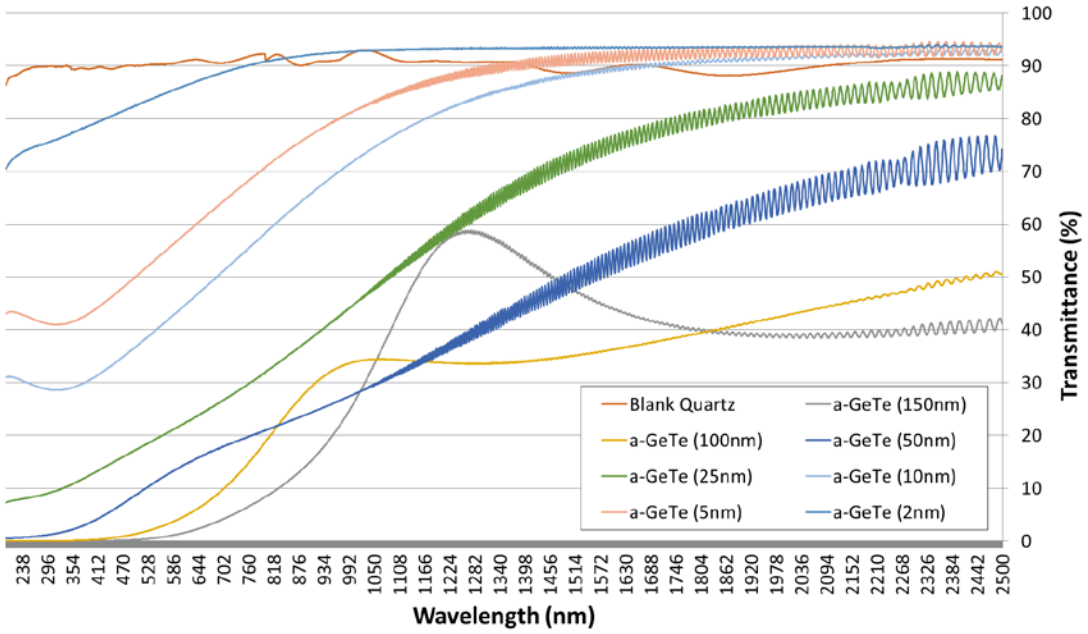

Figure 51. Transmittance of a-GeTe. Various amorphous thicknesses were tested with the Cary 5000 spectrometer.

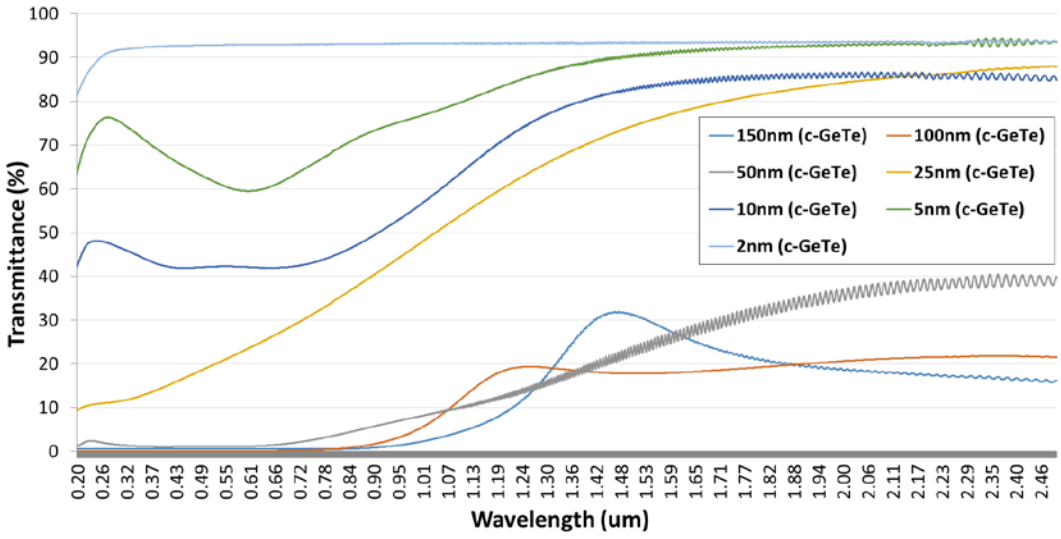

Figure 52. Transmittance of c-GeTe. Various crystalline thicknesses were tested with the Cary 5000 spectrometer.

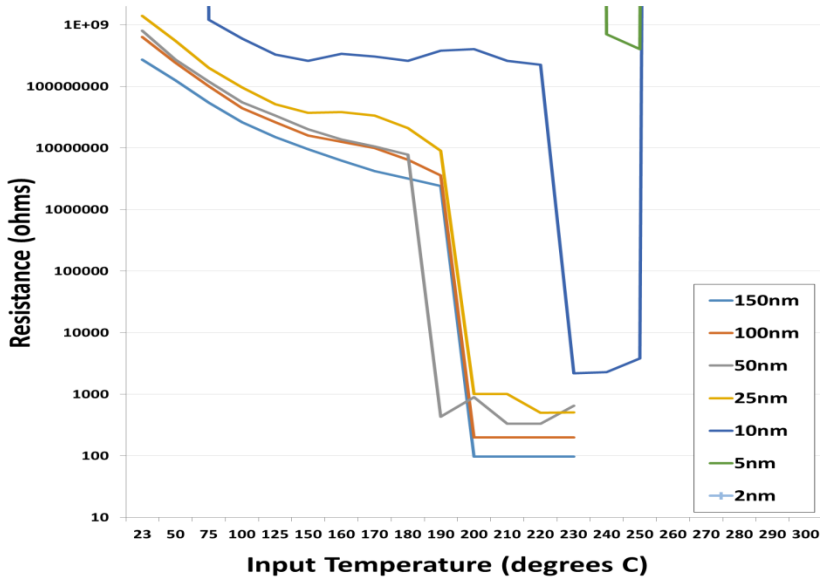

Figure 53. Transition temperatures of a-GeTe to c-GeTe. Phase transition was confirmed by the exponential drop in resistance as measured on the micromanipulator probe station.

Phases 2 and 3, PN-Junction Orientation and Film Thickness: Table 24 displays the V_{oc} and I_{sc} data recorded by a handheld Fluke 289 digital multimeter. These values were used to calculate the power delivered by the test pieces.

Table 24. Germanium pn-junction measured Voc & Isc and calculated power

				Pre-RTA			Post-RTA		
#	Test Phase	PN-junction	GeTe (nm)	Voc (μV)	Isc (μA)	P (pW)	Voc (μV)	Isc (μA)	P (pW)
Ge-A1	Orientation	Top	50	64	2.1	134	58	5.3	307
Ge-A2	Orientation	Top	250	50	-	-	60	3.3	198
Ge-A3	Orientation	Top	600	20	-	-	34	2.2	74.8
Ge-A4	Orientation	Rear	250	230	1	230	305	1.2	366
Ge-B1	Thickness	Rear	50	293	45	13185	-	-	-
Ge-B2	Thickness	Rear	150	128	19	243.2	-	-	-
Ge-B3	Thickness	Rear	350	112	28	3136	-	-	-

4.9 HMJ-SiGe Solar Cell Testing

The individual silicon and germanium wafers were tested under the solar simulator first, then the HMJ-SiGe solar cell was assembled using the solar cell fixture and tested. Data points were entered into a MATLAB software program to generate an I-V graph with calculated values for the voltage at the maximum power point (V_{mpp}), the current at the maximum power point (I_{mpp}), the actual maximum power (P_{max}), the ideal maximum power (P_{ideal}), the fill factor, and the efficiency. Figure 54 illustrates one of the many graphical outputs generated, and the remaining figures can be found in the appendix. Table 25 summarizes the configuration tested and data point values calculated.

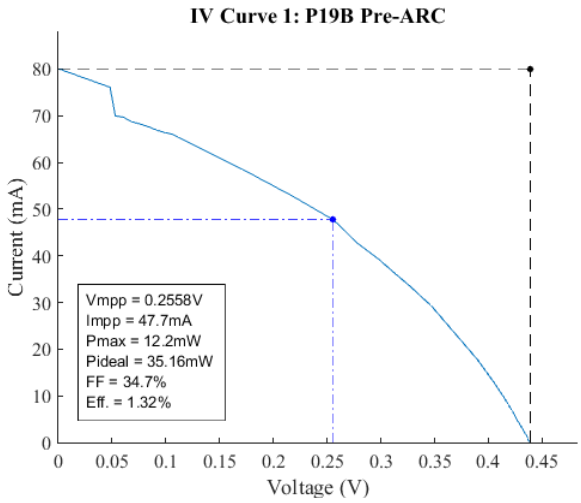

Figure 54. IV curve of P19B wafer before ARC. Although partially damaged during processing, V_{oc} and I_{sc} were measured to calculate the fill factor and efficiency for the p-type silicon wafer P19B using the MATLAB software program.

Table 25. Individual wafer test data. V_{oc}, I_{sc}, and temperatures were measured. Efficiencies were calculated using a MATLAB software program.

Configuration	Test Type	V_{oc} (mV)	I_{sc} (mA)	Temperature	Efficiency (%)	Avg Efficiency (%)
P19B Post RTA & ARC	I-V Curve 1	439.5	122.5	25°C	2.28	2.17
	I-V Curve 2	439.0	120.3		2.22	
	I-V Curve 3	442.6	108.2		2.06	
	I-V Curve 4	443.6	109.8		2.10	
	Endurance 1	417.8	82.5	37.1 - 37.4°C	1.34	1.66
	Endurance 2	416.1	82.9	37.7 - 37.8°C	1.34	
	Endurance 3	429.6	106.7	31.6°C	1.99	
	Endurance 4	429.2	107.0	31.7°C	1.98	
Germanium Wafer	I-V Curve 1	-8.56	-2.76	25°C	0	0
	I-V Curve 2	-8.60	-2.53		0	
	I-V Curve 3	-8.63	-2.76		0	
	Endurance 1	-6.70	-1.28	31.7°C	0	0
	Endurance 2	-6.81	-1.17	31.7°C	0	

Table 26. HMJ-SiGe Solar Cell test data. V_{oc} and I_{sc} were measured. Surface of the top wafer and the airgap temperatures were measured. Efficiencies were calculated using a MATLAB software program

Config	Test Type	V_{oc} (mV)	I_{sc} (mA)	Wafer Temp (°C)	Airgap Temp (°C)	Efficiency (%)	Avg Efficiency (%)
HMJ-SiGe Solar Cell	I-V Curve 1	420.0	75.2	-	-	1.17	1.39
	I-V Curve 2	425.0	83.9	34.4	34.3	1.36	
	I-V Curve 3	433.6	90.1	34.1	32.9	1.52	
	I-V Curve 4	433.2	89.6	34.0	32.8	1.51	
	Endurance 1	416.5	79.5	31.2 - 39.0	30.0-38.2	1.28	1.32
	Endurance 2	420.0	76.7	37.1-37.0	36.4-36.7	1.21	
	Endurance 3	422.0	86.6	38.0	37.2	1.40	
	Endurance 4	420.9	85.9	39.2	38.3	1.39	

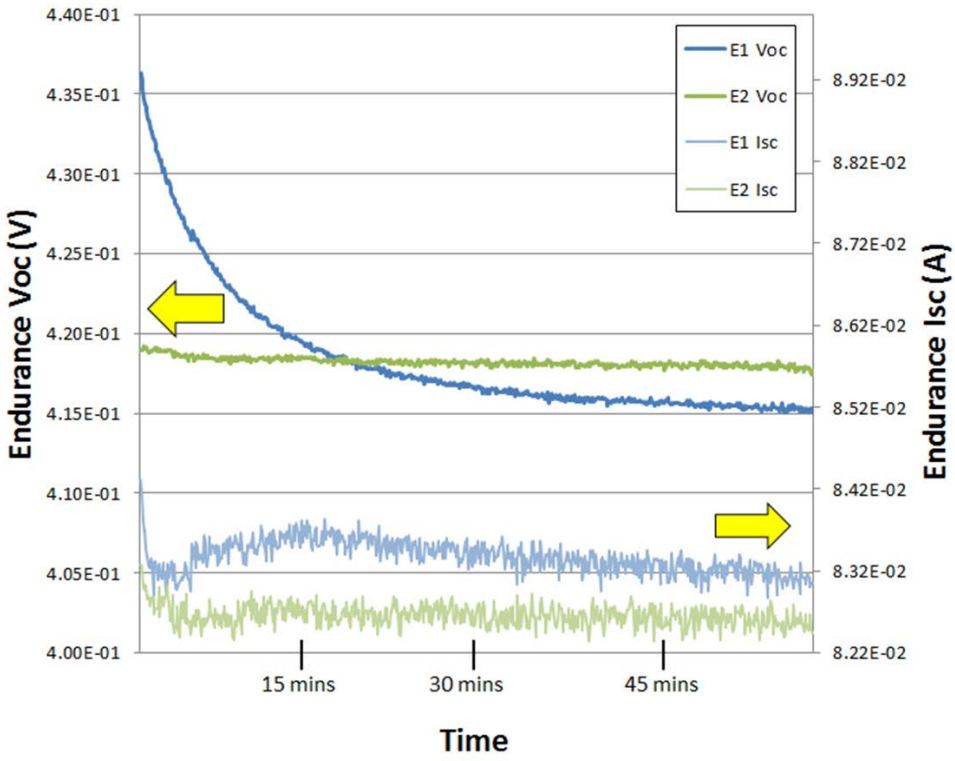

Figure 55. HMJ-SiGe solar cell V_{oc} and I_{sc} trend data. Measurements of V_{oc} and I_{sc} during two endurance tests of the HMJ-SiGe solar cell.

After testing of the HMJ-SiGe solar cell was accomplished, integration and evaluation of the architecture with the low-voltage power controller under different illumination environments was accomplished. V_{oc}, I_{sc}, and charging rate measurements were recorded in Table 26. Figure 56 shows the successful illumination of the on-board LED.

Table 27. HMJ-SiGe capstone test. Using a low-voltage power controller, the charge times were based on fully depleted capacitor to 2.5 VDC

Location	V_{oc} (mV)	I_{sc} (mA)	Estimated Charging Rate (ECR) and Time (ECT)
Solar Simulator	-	-	ECR: 286mV/min ECT: 8.74 mins
Outside @ 1:00pm	374	1.1	ECR: 0.5mV/min ECT: 83.3 hours
Florescent lights in testing room	4.1	0.2	ECR: 150uV/min ECT: 11.6 days

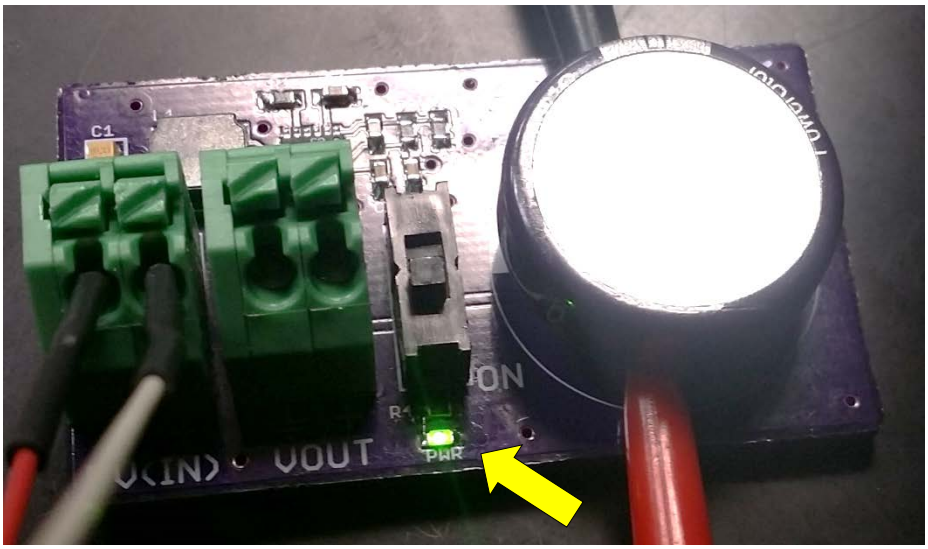

Figure 56. HMJ-SiGe integration with low-voltage power controller. The HMJ-SiGe successfully charged the capacitor for storage of energy and illumination of an LED.

4.10 Summary

This chapter presented the data and results from the testing explained in the methodology of this thesis. Measurements for evaluation in the next chapter were displayed from the seven focus areas of diffraction pattern generation, photon propagation, silicon diffusion processing, ohmic contacts, the distributed Bragg reflector, the Fresnel zone plate, the Ge/GeTe pn-junction Finally, results from the HMJ-SiGe testing were presented.

V. ANALYSIS

5.1 Overview

This chapter presents the analysis, interpretation, and comprehension of the data and results given in Chapter 4. The structure of this chapter (5.2 - 5.9) matches the methodology (3.2 - 3.9) and results (4.2 - 4.9) chapters of this thesis.

5.2 Diffraction Pattern Generation

A key characteristic to the original design of the HMJ-SiGe before the inclusion of the bottom n-type germanium wafer was the utilization of the generated diffraction pattern minima for location of the bottom front contact grating. To understand the importance of this aspect, it was necessary to study how a grating structure forms diffraction patterns.

Based on Figures 43-45, one conclusive observation was noted; the design concept was flawed. Beginning with Figure 43, the maxima points charted are relative to a normal incident plane wave. However, if the plane wave passed through the contact grating at an oblique angle, then the locations of the maxima and minima would shift accordingly. Photons that propagate through a semiconductor lattice and exit out from the surface because of non-absorption are not likely to pass through the contact grating at normal incidence. Therefore, the locations of the generated maxima and minima of a single wavelength would not be static. Furthermore, a solar cell is exposed to many wavelengths of the solar spectrum, and many wavelengths will pass through the electrical contact gratings.

Therefore, as the wavelength changes, the locations of the maxima changes, especially in the higher orders. Also, the angle of incidence prior to entering the grating shifts the maxima and minima locations of the generated diffraction pattern. A metal contact grating designed to be placed in the minima of one wavelength would then be placed in the maxima of another wavelength. Conclusively, there are no minima for the metal contact grating to be placed. The surface of the bottom germanium wafer is effectively a "cloud" of multiple photon plane waves that arrive at the bottom front metal contact grating from various multiple angles and composed of multiple wavelengths. Therefore, design of the contact grating should be based on the balance of shading loss reduction with EHP collection.

5.3 Photon Propagation

To understand how the metal contact grating design affects the incident photons that pass through the metal contact gratings, as well as propagate through the semiconductor lattice, RCWA was accomplished using a MATLAB software program for simulation of periodic structures that make up the layers in the HMJ-SiGe solar cell architecture.

Based on the results for the three Unit Cell configurations (see 4.3), three conclusive observations were made. The first observation was that a metal contact grating design for maximum transmittance in one portion of the solar spectrum cannot also provide significantly minimum transmittance in another portion of the solar spectrum. The second observation was that maximum transmittance occurred when the unit cell width is at the maximum allowed dimension and the metal

contact width is at the minimum allowed dimension. The third observation was that maximum transmittance occurred when the metal contacts of the top rear grating and the bottom front grating were directly underneath each other, and that the average transmittance and reflectance values are relatively constant when the metal contacts are not directly underneath each other.

With regards to the first observation, Table 11 shows the architectural parameters that provided the maximum transmittance (97%) and minimum reflectance (3%) values of the Unit Cell 1 configuration for the range of 1.0-1.1um. This was the basis for evaluating the same parameters simulated in the other portions of the spectrum based on the criteria defined in the methodology (see 3.3), which was maximum transmittance in the range of 1.0-1.8um and maximum reflectance in the range of 0.3-1.0um of the solar spectrum. This criterion was established for the purposes of reducing unnecessary heat to the silicon lattice by reflecting away the short wavelengths above the silicon band gap but allow for the longer wavelengths below the silicon band gap which do not get absorbed by silicon but will contribute to EHP generation in the germanium lattice. Table 12 shows the other portions of the solar spectrum evaluated at the parameters listed in Table 11, and it can be seen that the minimum reflectance values for the spectral ranges of 0.3-0.4um and 0.5-0.6um were very low- at around 4% for both regions. However, the criteria was satisfied in the ranges of 1.3-1.4um and 1.7-1.8um with maximum transmittance values of around 96% for both regions. Similar to the analysis presented on Diffraction Pattern Generation (see 5.2) with regards to the effects of multiple wavelengths passing through a diffraction grating, a metal contact grating

designed for maximum transmittance of one small wavelength region, like 1.0-1.1um, cannot significantly degrade undesired regions of the solar spectrum, like 0.3-0.4um, in prevention of heat absorption to the silicon lattice. It was concluded that in order to achieve this aspect, an external feature must be part of the architectural design. A DBR, as discussed in this thesis, designed to reflect a portion of the solar spectrum higher than the silicon band gap would be the perfect solution.

With regards to the second observation, the contact grating design is both a help for EHP collection and a hindrance due to the shading loss generated by coverage of the silicon surface. The results shown in Table 11 and Table 13 show maximum transmittance and minimum reflectance values which are affected primarily by the unit cell width and metal contact width within the evaluated wavelength range. The periodic structure of a unit cell with a metal contact is analogous to a grating slit opening that allows for photons to pass through (Figure 57). The opening is significantly affected by the unit cell width in relation to the metal contact width.

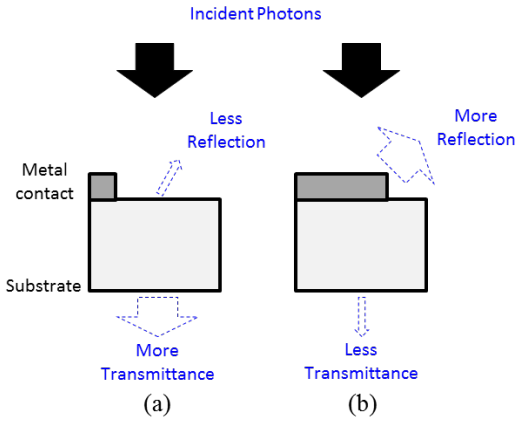

Figure 57. Significance of unit cell width and metal contact ratio. Transmittance and reflectance values are affected by this ratio. More transmittance is achieved (a) by reducing the metal contact width, and more reflection is achieved (b) by increasing the metal contact width.

Based on the unit cell widths and the top front metal contact widths in Tables 11 & 13, the average opening that resulted in the maximum transmittance across all the of the simulated wavelengths was about 96%. In contrast to the previous HMJ-Si solar cell architecture, the top rear metal grating was designed with a unit cell width of 1300um and a metal contact width of 400um, whereas the bottom rear metal grating was designed with a unit cell width of 1300um and a metal contact width of 200um. The openings for these two designs were calculated to be about 69% and 85%, respectively. Because the HMJ-SiGe solar cell architecture is composed of stacked semiconductor wafers, the maximum possible transmittance to the bottom wafer is necessary to maximize the ability for EHP generation within the germanium substrate. Conclusively, the unit cell opening must be maximized but balanced with the spacing of the metal contacts in relation to the diffusion length of the silicon or germanium substrate.

With regards to the third observation, Tables 14-19 show the average transmittance and reflectance values affected by the location of the metal contacts within the air gap. It was observed that the maximum transmittance (80%) occurred when the bottom front metal contact was directly underneath the top real metal contact, as seen in Figure 58(a). As soon as the bottom front metal contact moved to the right of the top rear metal contact, the initial average transmittance value dropped but increased the further that the bottom contact was from the top contact, as seen in Figure 58(b) and Figure 58(c). This was caused by the bottom contact decreasing the exposure of the photons to the germanium surface when it was partially underneath the top contact, followed by the increase in exposure of the photons to the germanium surface when the bottom contact was much further away from the top contact. In fact, the results in Table 14 showed that an average transmittance of 76% was achieved no matter where the bottom front metal contact was located within the unit cell with exceptions at the far left and right ends. On the far right end, as seen in Figure 58(d), the average transmittance was the lowest, because the unit cell opening was essentially decreased in width.

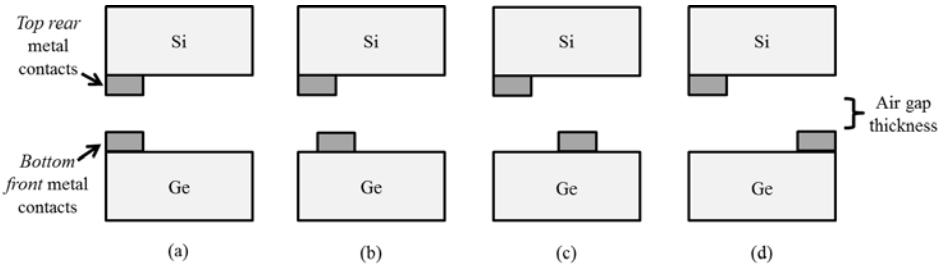

Figure 58. Metal contact location scenarios. Average transmittance was affected by the location of the metal contacts within the air gap. Air gap thickness was kept constant at 100um. Maximum transmittance occurred when the bottom contact was underneath the top contact (a). The average transmittance decrease when the bottom contact was partially underneath (b). As the location of the bottom contact varied across the unit cell width, the average transmittance increased (c). Minimum transmittance occurred when the bottom contact was located at the far right side of the unit cell width (d).

Interestingly, with regards to the results shown in Tables 15 & 16, the air gap thickness has a somewhat opposite effect in relation to the location of the bottom front metal contact at the far left and right ends of the unit cell. With the metal contacts directly underneath each other Figure 58(a)), as the air gap thickness increases, the average transmittance decreases. Conversely, with the metal contacts at opposite ends of the unit cell width (Figure 60(d)), as the air gap thickness increases, the average transmittance initially increases but then decreases. In both cases, because exposure of the photons to the germanium surface is not varied, the average transmittance was more affected by the reflection off of the metal contacts. The same evaluation was accomplished with a larger unit cell width of 5000um (Tables 17-19), and the results showed about the same outcomes. Maximum transmittance of 90% is achieved with the top and bottom contacts directly underneath each other, and the average transmittance of about 85% occurred when the bottom metal contact was anywhere away from the top metal contact.

Interestingly, when the bottom metal contact was at the far right end of the unit cell, the average transmittance increased, which indicated that the larger unit cell opening was less sensitive to metal contact reflection. Nevertheless, for both the small unit cell width and the larger unit cell width, maximum transmittance is the highest when the metal contacts are directly underneath each other but can be negatively affected by the thickness of the air gap. Conclusively, although the air gap is a unique feature of the HMJ-SiGe solar cell architecture for mitigating the degradation effects of heat to the semiconductor lattice, the air gap thickness must be balanced with the desire to achieve maximum transmittance for both the top rear contact grating and the bottom front contact grating. In other words, a big air gap helps keep the solar cell architecture cooler, but it also degrades the average transmittance.

5.4 Silicon Diffusion Processing

The diffusion profile for creating the pn-junction, emitter, and back surface field is quite significant to the performance of the solar cell. The details and location of the diffusion process followers for p-type and n-type silicon wafers can be found in the appendix of this thesis.

Table 20 shows the measured sheet resistance and calculated dopant concentrations of both sides of each p-type silicon. For the most part, the sheet resistance measured were close to the values list in the process follower, with the exception of the bottom side of the wafer labeled P15. According to the requirements given, the bottom side of the single back surface field wafer should

have been 50-80 Ω/□. With a measured sheet resistance of 645 Ω/□, it was apparent that some variability to the processing was introduced, and the exact cause to the resulting decrease in surface dopant concentration is still unknown.

5.5 Ohmic Contacts

Low resistance ohmic contacts in solar cells are essential to maximize the collection of EHPs for accomplishing work. The HMJ-SiGe solar cell architecture has four different metal-to-semiconductor interfaces: metal/p-Si, metal/n-Si, metal/n-Ge, and metal/p-GeTe. It was necessary to understand and test which metals were required for the type of semiconductor.

Based on the results in Table 21, two conclusive observations were made. The first observation was that the appropriate metal for n-type and p-type silicon and for p-GeTe can be determined and proven by comparing the metal work function with the calculated semiconductor work function, as described in 3.5. The second observation was that creating an ohmic contact by metal alone on n-type germanium was extremely difficult and required an interfacial layer.

With regards to the first observation, it can be seen from Table 21 that the contact resistivity for aluminum on n-type Si, gold on p-type Si, and gold on p-type GeTe were calculated in the micro-ohms, which represents the actual resistance between the metal and the semiconductor at the interface.

With regards to the second observation, it can be seen from Table 22 that an interfacial layer on n-type germanium enabled for a much better ohmic contact than metal could do alone. This is due to the reduction of the barrier height by de-

pinning the Fermi level from the edge of the valence in the n-type germanium substrate. However, even though the result presented here is in the micro-ohms, there is potential for the contact resistivity to reach values between 10^{-7} – 10^{-8} with other interfacial layers [111].

5.6 The Distributed Bragg Reflector

Based on the generated plots in Figures 47-48 and the remaining that can be found in the appendix, it can be concluded that the best combination to fabricate a DBR with the available dielectrics in PECVD at AFIT is a-Si and Si_3N_4 with a target wavelength of 600nm (Figure 47). Although there are oscillations that occur near the silicon band gap, the bandwidth of the large reflectance lobe covers a large portion of the shorter wavelengths above the silicon band gap.

Two significant observations can be made from Figure 50, which depicts the transmittance of the DBR from 200nm – 2500nm. The first observation is that the zero transmittance measured between 200nm and around 1000nm is due to the strong absorption of the thick silicon substrate. A quartz or sapphire substrate that does have the same optical response with absorption should have been used instead. Nevertheless, because the reflectance capability of the spectrometer was inoperable, this hypothesis of strong absorption could not be fully confirmed. The second, and probably the most interesting, observation is the increase in transmittance from the DBR between about 1100nm – 2000nm as compared to the bare silicon substrate. Because the DBR is composed of alternating layers of dielectric material, the expected result would be less transmittance compared to a

silicon surface that is bare. Therefore, it is believed that, based on the confirmed issue with the reflectance capability of the spectrometer, there might be a problem with the transmittance portion, too.

5.7 The Fresnel Zone Plate

The intent of the Fresnel zone plate was to concentrate as many photons as possible toward the bottom germanium wafer. Table 23 shows the solar irradiance results between a bare silicon wafer and another silicon wafer with a FZP with aluminum metal. It can be seen that the drop in irradiance was very drastic, at about 54%. Just like the analysis presented on Photonic Propagation (see 5.3), the opaque rings cover too much of the transparent openings. Therefore, more reflectance occurred than transmittance of the incident photons. Maximum possible transmittance is required to allow for the bottom germanium wafer to generate as many EHPs as possible. Conclusively, it was determined that the FZP was not a viable solution to the improvement of the architecture.

5.8 The Ge/GeTe PN-Junction

Because the HMJ-SiGe solar cell utilizes a germanium substrate as the bottom wafer in the architecture, determining the correct pn-junction location and thickness was necessary to ensure successful application of thin film p-type c-GeTe to the n-type germanium surface.

The results presented in Table 24 (see 4.8) conveyed two important observations. The first observation was that the test pieces with the pn-junction

located on the rear performed, resulting in higher calculated power. The second observation was that higher Voc and Isc, and thus higher power, was achieved with thinner film thicknesses of c-GeTe.

With regards to the first observation, placement of the c-GeTe on the rear of the germanium substrate allowed for more incident photons to enter into the lattice and create EHPs. This was confirmed by the transmittance results shown in Figures 51 and 52 for a-GeTe and c-GeTe, respectively. Not only do the thicker films of a-GeTe yield less transmittance, but this transmittance lowers even more when the GeTe is in a crystalline phase. Therefore, significant reflection loss can be prevented and EHP generation can be maximized by depositing the c-GeTe on the rear of the germanium substrate.

With regards to the second observation, it is theorized that 50 nm of c-GeTe performed better by allowing for more minority carriers to become more influenced by the built-in electric field and diffuse across the pn-junction. Because a-GeTe that has transitioned into c-GeTe behaves like a metal electrically, the effectiveness of the purpose of a pn-junction is decreased as the film thickness increases. In other words, thick c-GeTe acts more like an electrical contact.

It can be seen in Figure 53 that a-GeTe transitions into c-GeTe when the surface resistance lowers significantly my orders of magnitude. Furthermore, for films thicker than 10nm, the transition temperatures for each thickness are somewhat close to each other. This information was utilized in the process follower for the n-type germanium wafer processing.

5.9 HMJ-SiGe Solar Cell Testing

The individual wafers and the HMJ-SiGe solar cell assembly were evaluated to assess its performance under standard test conditions and under endurance testing. Table 25 summarizes the measured and calculated values during these types of testing.

It most significant and immediate observation was that the efficiencies calculated are quite low. The top silicon wafer, serialized as P19B, achieved an average efficiency of 2.17% during the standard testing. As expected the efficiencies decreased during the endurance testing, because the addition of heat to the lattice significantly affects V_{oc}.

However, a large difference was noted of the calculated efficiency values between Endurance Tests 1 and 2 with that of Endurance Tests 3 and 4. This was explained by testing variation. Because Endurance Tests 1 and 2 were accomplished separately from Endurance Tests 3 and 4, certain setup steps, like precise wafer placement under the solar simulator, digital multimeter warm-up times, tolerance of irradiance output, etc, most likely were not precisely repeated with every test. Therefore, multiple testing helps with smoothing out this variation.

With regards to low efficiencies it can be seen that the worst performing semiconductor in the HMJ-SiGe solar cell is the n-type germanium wafer. At zero percent efficiency, it was apparent that the silicon wafer was providing all of the performance in the HMJ-SiGe assembly. Many factors may have caused this. First, the reverse polarity of the measured V_{oc} and I_{sc} of the germanium wafer indicate a strong Schottky metal-to-semiconductor contact. During processing of this

germanium wafer, and although the surface resistance of c-GeTe was lowered by orders of magnitude from its amorphous phase measurement, the resistance may have not been lowered enough. Also, because the study and fabrication of ohmic contacts with interfacial layers on n-type germanium is relatively new, unintended variations in processing or worse-than-expected results in the contact formation could have occurred. Furthermore, germanium is quite reflective, with values as high as 51% at 600nm and as low as 38% at 1800nm [50]. Therefore, an ARC should be applied to the surface to prevent reflection losses.

As a capstone to this thesis, the HMJ-SiGe solar cell was connected to the low-voltage power controller to test the charging of the on-board capacitor. Table 26 summarizes the estimated charging rates and times from within three different illumination environment. It was expected that the charging rate and time would be best under the solar simulator due to the intensity of the source, the vertical angle of incidence, and little to no variability in environmental absorbance between the solar cell and the illumination. However, the photovoltaic performance outside was very poor in comparison and even worse under fluorescent lighting. While the solar simulator can generate a controlled irradiance of $1000W/m^2$ to simulate solar light received at sea level, the actual spectral density received could be much different due to atmosphere absorption or environmental variabilities.

5.10 Summary

In this chapter the results were evaluated and interpreted in an effort to present the best explanation for what was observed.

VI. CONCLUSION

6.1 Observations

The primary objective of the work presented here was to characterize the HMJ-Si solar cell architecture and improve on it with the development of the HMJ-SiGe solar cell. The six questions presented at the introduction to this thesis were the basis for research into the seven focus areas: diffraction pattern generation, photon propagation, silicon diffusion processing, ohmic contacts, the distributed Bragg reflector, the Fresnel zone plate, and the Ge/GeTe pn-junction. Nevertheless, those six questions can be answered from the conclusive observations determined in this work.

1. *Was the diffraction grating architecture effective in the appropriate wavelength and angle of incidence range?* It was concluded that there are essentially no shadows to place metal contacts. Because the solar spectrum is composed of many wavelengths that enter into the silicon lattice, any diffraction pattern generated by one wavelength is disturbed by a diffraction pattern generated by another wavelength. Furthermore, the angle of incidence shifts the locations of the maxim and minima of a generated diffraction.
2. *Can spectral filtering of the grating contact design be optimized, subject to fabrication constraints?* It was concluded that grating design cannot spectrally filter a portion of the spectrum- significantly high transmittance in one area but significantly low transmittance in another area. Furthermore,

transmittance is determined by the ratio of the unit cell width to the metal width. The HMJ-Si specifications of the contact grating were more restrictive than should have been. Although based on the premise of an optimized design for diffraction pattern generation, the resulting grating design also decreased the amount of photons allowed to enter and create EHPs.

3. *Did the previous HMJ-Si solar cell diffusion process contain flawed fabrication steps?* It was concluded that the previous diffusion process followers contained to significant flaws- lack of an oxide protection and edge isolation. A protective layer of oxide prevents unintended contamination of the non-target side during. Also, because thermal diffusion can affect the edges of the wafer, electrical isolation is necessary to prevent shunting the top side to the bottom side which hinders efficiency.
4. *Are there more appropriate metal-to-semiconductor interfaces in forming ohmic contacts?* It was concluded that significant improvements can be made by utilizing metals with the appropriate work functions for the desired semiconductor surface. Furthermore, because the HMJ-SiGe solar cell architecture incorporates a bottom n-type germanium wafer, a thin interfacial layer will need to be used to de-pin the Fermi level away from the germanium valence band edge.
5. *Would replacing the bottom wafer with germanium improve performance of the architecture?* It was concluded that germanium has the potential to improve performance, because germanium Because c-GeTe is a p-type semiconductor, a pn-junction with an n-type germanium wafer was formed.

Furthermore, it was found that due to the low transmittance of c-GeTe, placement of the thin film was required to be on the bottom of the substrate to maximize incident photons.

6. *Is it recommended for a Fresnel zone plate and distributed Bragg reflector be added for improvement to the architecture?* While the DBR has a strong potential in mitigating higher energy wavelengths that can add heat to the silicon lattice, the FZP is not a viable solution to concentrate photons towards the bottom germanium wafer due to a significant drop transmittance.

6.2 Recommendations

There are a number of recommendations that can be made regarding this thesis. First, because the germanium wafer is very reflective, a low-temperature ARC should be explored to increase the absorption of photons into its lattice. Second, more research and testing of interfacial layers with n-type germanium ohmic contacts need to be accomplished to ensure the maximum potential of EHP collection from the bottom wafer. Third, thin film passivated contacts should be explored to help with decreasing the surface recombination of both semiconductor wafers. Fourth, because this thesis was based on incorporation of a diffusion-processed p-type silicon semiconductor, an n-type silicon wafer should be tested and incorporated for performance evaluation. Finally, the quest with short-wavelength rejection by a DRB should continue and become incorporated into the HMJ-SiGe solar cell architecture.

6.3 Conclusion

In conclusion, although the performance HMJ-SiGe solar cell did not perform comparably with industry manufactured solar cells, the architectural design is unique and has potential for vast improvement.

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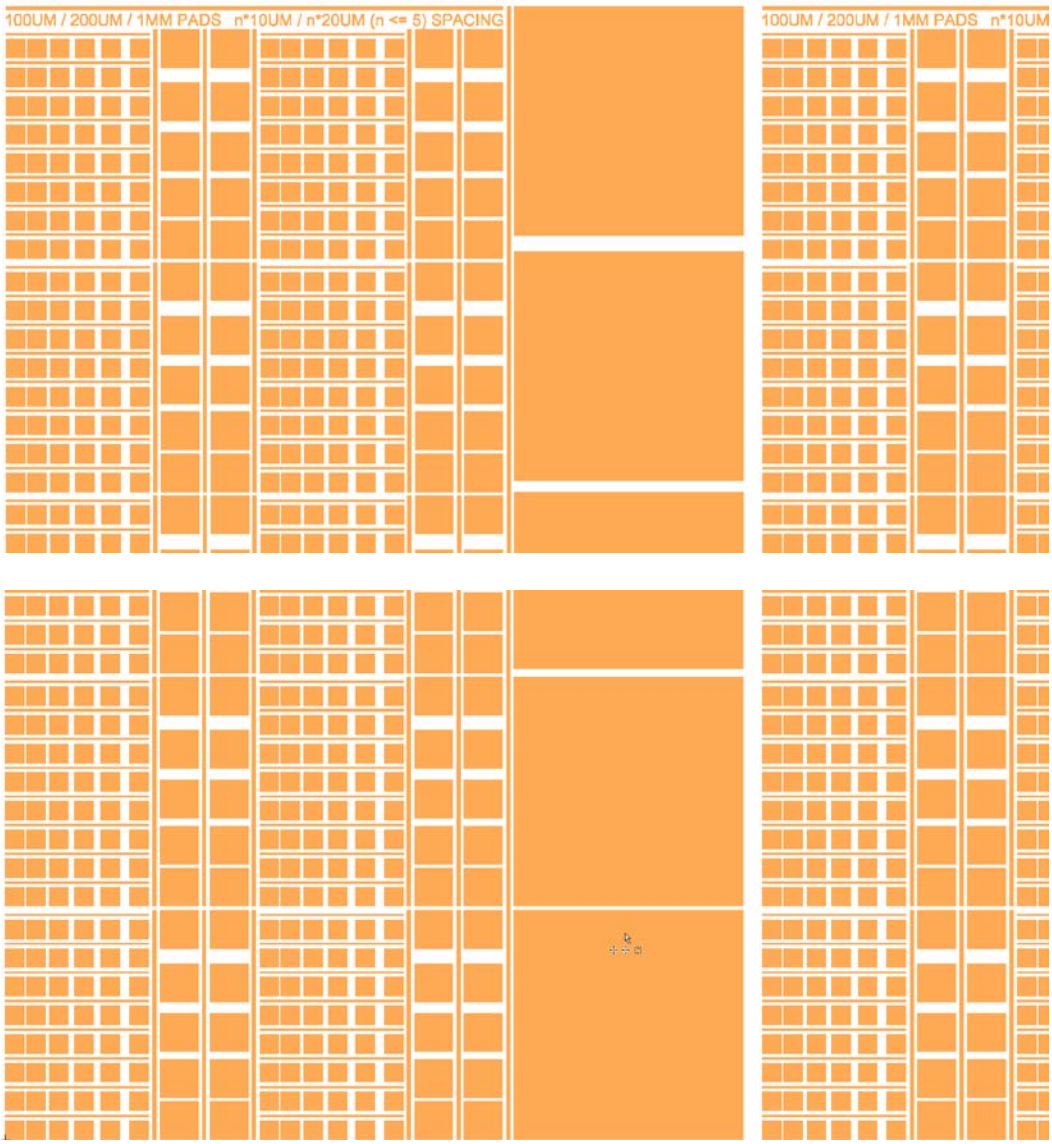
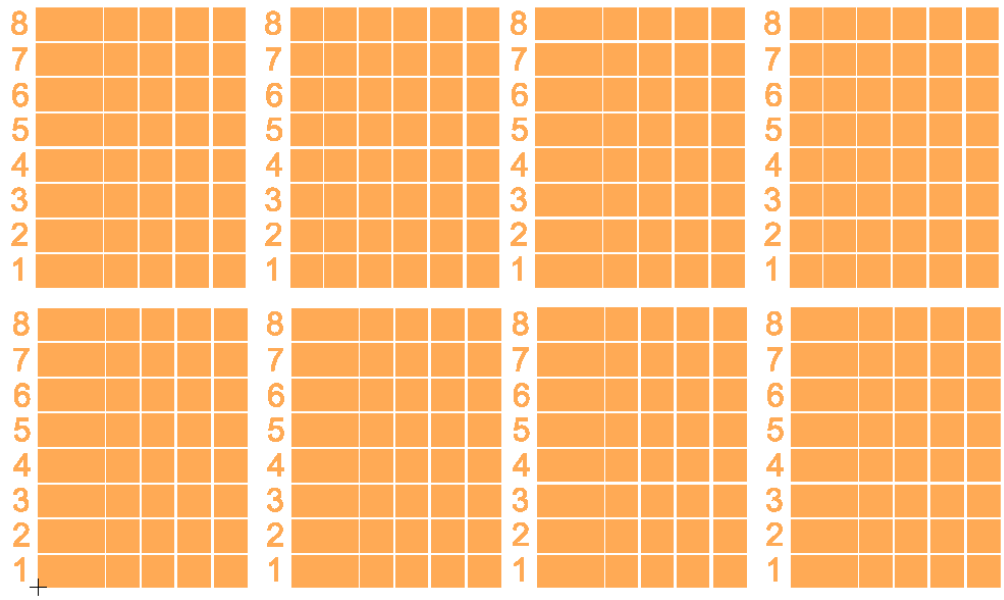
Appendix A: MATLAB Code for DBR Simulations

```
%{
@ 400nm: a-Si = 4.27; Si3N4 = 2.07; SiO2 = 1.49  (Greatest photon
density)
@ 500nm: a-Si = 4.47; Si3N4 = 2.03; SiO2 = 1.48  (Greatest photon
density)
@ 600nm: a-Si = 4.28; Si3N4 = 2.01; SiO2 = 1.48  (Greatest photon
density)
@ 700nm: a-Si = 4.07; Si3N4 = 2.00; SiO2 = 1.47  (Greatest photon
density)
%}


clc;
clear;

na = 1; nb = 3.6; nH = 4.27; nL = 2.07;   % fused silica = 3.6; a-Si =
3.49; SiO2 = 1.44  SiO2 = 1.457, N4Si3 = 2.021, and a-Si = 3.8.
LH = 0.25; LL = 0.25;                     % optical thicknesses = 1/4
unit
la0 = 400;                                % target wavelength units of
nm
rho = (nH-nL)/(nH+nL);                    % reflection coefficient ?
la2 = pi*(LL+LH)*1/acos(rho) * la0;       % right bandedge
la1 = pi*(LL+LH)*1/acos(-rho) * la0;      % left bandedge
Dla = la2-la1;                            % bandwidth
N = 10;                                   % number of bilayers
n = [na, nH, repmat([nL,nH], 1, N), nb]; % indices for the layers
A|H(LH)N|G
L = [LH, repmat([LL,LH], 1, N)];          % lengths of the layers H(LH)N
la = linspace(300,2500,1000);              % plotting range is 950 ? ? ?
1200 nm
Gla = 100*abs(multidiel(n,L,la/la0)).^2; % reflectance as a function of
?
Figure; plot(la,Gla);
xlabel ('Wavelength (nm)');
ylabel ('Reflectance (%)');
```

Appendix B: Contact Mask V1



Appendix C: Contact Mask V2



Appendix D: P-Type Silicon Diffusion Process Follower

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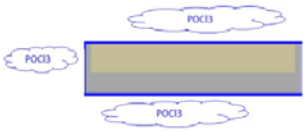
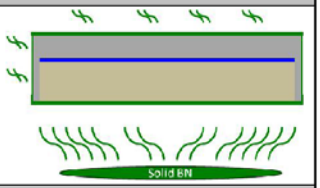
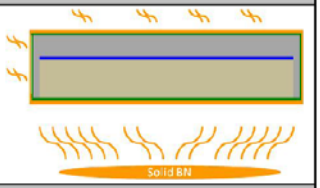
P-type Silicon Substrate n(p)p++ Diffusion Process Follower

Step 1: **Wafer Clean** ***[hand-held, submerge, or spinner @ 500 rpm]***			
	30 sec acetone rinse		
	30 sec methanol rinse		
	30 sec DI water rinse		
	Dry with nitrogen and clean texwipes	*If using spinner, then @ 500 rpm. Place on texwipes and ensure both sides are dry*	
	Hot plate bake for 1 min @ 110°C	*Ensures further drying*	
Step 2: **Oxide (200nm both sides)**			
	Refer to DWD Oxidation Chart for target temp	*Perform steps for temp ramp-up*	
	Perform dry oxidation for 10 mins @ 900°C	*Furnace should be at target temp*	
	Perform wet oxidation. Soak wafers for: p-type = 100 mins @ 900°C n-type = 100 mins @ 900°C		
	Perform dry oxidation for 10 mins @ 900°C		
Step 3: **Photoresist Application (protect back side oxide)**			
	Put wafer on 2" wafer chuck front side up, turn on vacuum, and verify spinner settings. Time: 30 sec; Speed: 4,000 rpm	*Using the spinner in the solvent hood*	
	Spray wafer with nitrogen to cool the wafer and remove any surface contaminants.		
	Apply S1818 positive photoresist onto the wafer, and then start the spinner.	*Bubbles prevent uniform spreading*	
	Once stopped, turn off the vacuum and place the wafer on the 110°C hot plate for 4 min.	*Hot plate sets the resist*	
Step 4: **Oxide Etch (front side)**			
	Prepare 5:1 BOE	*5:1 BOE etches SiO2 around 100nm/min*	
	Submerge wafer in BOE for 2 mins.		
	Remove and rinse with DI water.		
	Verify that all SiO2 has been etched away	*Observe that the film of the DI water wetting or sheeting across the whole surface of the wafer. If the layer of SiO2 has been etched off, the DI water will not adhere to the back, except for a few isolated drops, and the wafer will appear dry and dull gray. This happens because SiO2 is hydrophylic as opposed to silicon which is hydrophobic.*	
	If oxide is not fully etched, repeat BOE immersion for additional 30 secs and recheck		
Step 5: **Photoresist Removal (backside)** ***[hand-held, submerge, or spinner rpm]***			

	Plasma ash with O2 for 5 mins @ 75W		
	Verify photoresist is completely gone, and repeat as necessary		
Step 6: **Diffusion (front side pn-junction)**			
	Refer to previous diffusion runs and SIMS/ECV data	*Choose desired profile, sheet resistance, and junction depth*	
	Target sheet resistance = ~50Ω/□ Target junction depth = 0.5 – 1.5µm	*Create n-type emitter with Phosphorus*	
	POCl3: 850°C @ 30 min dep; 10 min drive-in PH-1000N: 925°C @ 20 min dep; 10 min drive-in	*Accomplish Surface Etch Back process follower after entire wafer diffusion is completed*	
Step 7: **PSG & Oxide Removal**			
	Prepare 10:1 BOE		
	Submerge wafer in BOE	*Removes unreduced glass and oxide layers*	
Step 8: **Thermal Oxide (200nm both sides)**			
	Follow Step 2	*Proceed to Step 13 after completing Step 2*	
Step 9: **Photoresist Application (protect front pn-junction side)**			
	Follow Step 3 for the front side of wafer	*Proceed to Step 14 after completing Step 3*	
Step 10: **Oxide Etch (back side)**			
	Follow Step 4 for the front side of wafer	*Proceed to Step 15 after completing Step 4*	

Step 11: **Photoresist Removal (front side)**			
	Follow Step 5 for the front side of wafer	*Proceed to Step 16 after completing Step 5*	
Step 12a: **Diffusion (BSF)**			
	Refer to previous diffusion runs and SIMS/ECV data	*Choose desired profile, sheet resistance, and junction depth*	
	Target sheet resistance = 50-80Ω/□ Target junction depth = 0.5 – 1.0μm	*p-type wafers: use boron dopant*	
	BN-975: 950°C @ 40min dep; 10min drive-in GS-126: 925°C @ 60min dep; 10min drive-in GS-245: 1050°C @ 30min dep; 10min drive-in GS-278: 1100°C @ 30min dep; 10 min drive-in	*GS-245: ~12Ω/□* *GS-278: ~8Ω/□*	
Step 12b: **Diffusion (EBSF)**			
	Refer to previous diffusion runs and SIMS/ECV data	*Choose desired profile, sheet resistance, and junction depth*	
	Target sheet resistance = 30-50Ω/□ Target junction depth = 0.2 – 0.7μm	*p-type wafers: use boron dopant*	
	BN-975: 1000°C @ 20min dep GS-126: 950°C @ 60min dep GS-245: 1100°C @ 60min dep GS-278: 1150°C @ 60min dep	*GS-245: ~5Ω/□* *GS-278: ~2Ω/□*	
Step 13: **BSG and Oxide Removal**			
	Prepare 10:1 BOE		
	Submerge wafer in BOE for 5 mins.	*Removes unreduced glass and oxide*	

Appendix E: N-type Silicon Diffusion Process Follower

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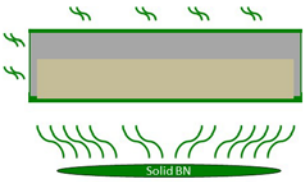
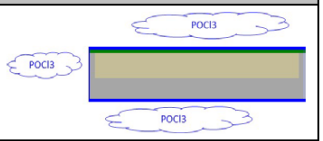
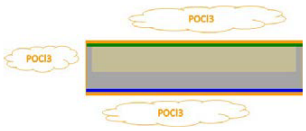
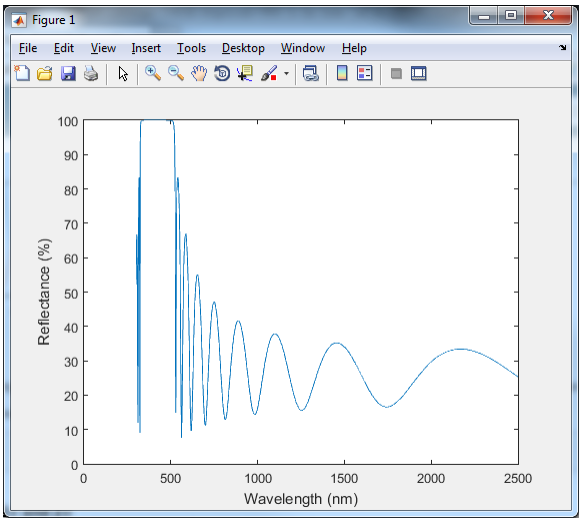
N-type Silicon Substrate p(n)n++ Diffusion Process Follower

Step 1: **Wafer Clean** ***[hand-held, submerge, or spinner @ 500 rpm]***			
	30 sec acetone rinse		
	30 sec methanol rinse		
	30 sec DI water rinse		
	Dry with nitrogen and clean texwipes	*If using spinner, then @ 500 rpm. Place on texwipes and ensure both sides are dry*	
	Hot plate bake for 1 min @ 110°C	*Ensures further drying*	
Step 2: **Oxide (200nm both sides)**			
	Refer to DWD Oxidation Chart for target temp	*Perform steps for temp ramp-up*	
	Perform dry oxidation for 10 mins @ 900°C	*Furnace should be at target temp*	
	Perform wet oxidation. Soak wafers for 100 mins @ 900°C		
	Perform dry oxidation for 10 mins @ 900°C		
Step 3: **Photoresist Application (protect back side oxide)**			
	Put wafer on 2" wafer chuck front side up, turn on vacuum, and verify spinner settings. Time: 30 sec; Speed: 4,000 rpm	*Using the spinner in the solvent hood*	
	Spray wafer with nitrogen to cool the wafer and remove any surface contaminants.		
	Apply S1818 positive photoresist onto the wafer, and then start the spinner.	*Bubbles prevent uniform spreading*	
	Once stopped, turn off the vacuum and place the wafer on the 110°C hot plate for 4 min.	*Hot plate sets the resist*	
Step 4: **Oxide Etch (front side)**			
	Prepare 5:1 BOE	*5:1 BOE etches SiO2 around 100nm/min*	
	Submerge wafer in BOE for 2 mins.		
	Remove and rinse with DI water.		
	Verify that all SiO2 has been etched away	*Observe that the film of the DI water wetting or sheeting across the whole surface of the wafer. If the layer of SiO2 has been etched off, the DI water will not adhere to the back, except for a few isolated drops, and the wafer will appear dry and dull gray. This happens because SiO2 is hydrophylic as opposed to silicon which is hydrophobic.*	
	If oxide is not fully etched, repeat BOE immersion for additional 30 secs and recheck		
Step 5: **Photoresist Removal (backside)** ***[hand-held, submerge, or spinner rpm]***			
	Plasma ash with O2 for 5 mins @ 75W		

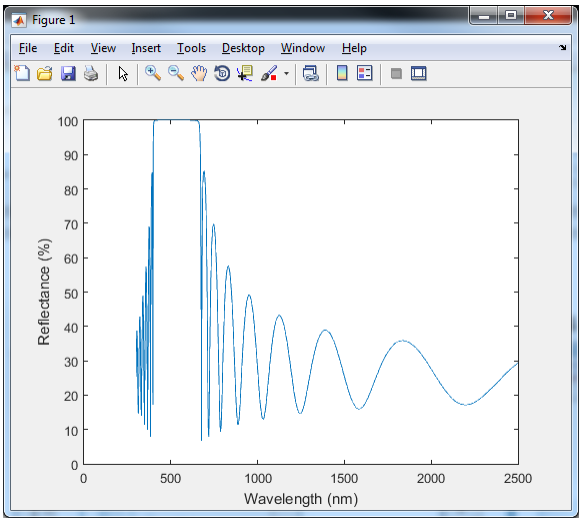
	Verify photoresist is completely gone, and repeat as necessary		
Step 6: **Diffusion (front side pn-junction)**			
	Refer to previous diffusion runs and SIMS/ECV data	*Choose desired profile, sheet resistance, and junction depth*	
	Target sheet resistance = ~50Ω/□ Target junction depth = 0.5 – 1.5µm	*Create p-type emitter with Boron*	
	BN-975: 975°C @ 30min dep; 10 min drive-in GS-126: 950°C @ 30min dep; 10 min drive-in	*GS-245 & GS-278 recommended temperature ranges exceed desired approximate sheet resistivity target* *Accomplish Surface Etch Back process follower after entire wafer diffusion is completed*	
Step 7: **BSG & Oxide Removal**			
	Prepare 10:1 BOE		
	Submerge wafer in BOE	*Removes unreduced glass and oxide layers*	
Step 8: **Thermal Oxide (200nm both sides)**			
	Follow Step 2	*Proceed to Step 13 after completing Step 2*	
Step 9: **Photoresist Application (protect front pn-junction side)**			
	Follow Step 3 for the front side of wafer	*Proceed to Step 14 after completing Step 3*	
Step 10: **Oxide Etch (back side)**			
	Follow Step 4 for the front side of wafer	*Proceed to Step 15 after completing Step 4*	
Step 11: **Photoresist Removal (front side)**			
	Follow Step 5 for the front side of wafer	*Proceed to Step 16 after completing Step 5*	

Step 12a: **Diffusion (BSF)**			
	Refer to previous diffusion runs and SIMS/ECV data	*Choose desired profile, sheet resistance, and junction depth*	
	Target sheet resistance = 50-80Ω/□ Target junction depth = 0.5 – 1.0μm	*p-type wafers: use boron dopant*	
	PH-900: 850°C @ 45min dep; 10min drive-in POCl3: 850°C @ 30min dep; 10min drive-in		
Step 13b: **Diffusion (EBSF)**			
	Refer to previous diffusion runs and SIMS/ECV data	*Choose desired profile, sheet resistance, and junction depth*	
	Target sheet resistance = 30-50Ω/□ Target junction depth = 0.2 – 0.7μm	*p-type wafers: use boron dopant*	
	PH-950: 875°C @ 35 min dep POCl3: 900°C @ 9 min dep		
Step 13: **PSG and Oxide Removal**			
	Prepare 10:1 BOE		
	Submerge wafer in BOE for 2 mins.	*Removes unreduced glass and oxide*	

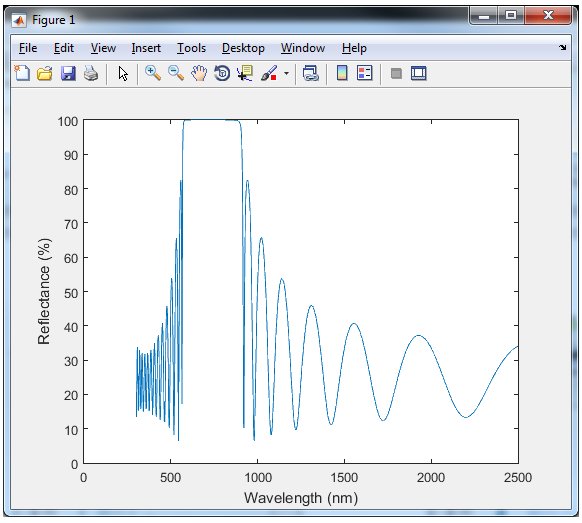
Appendix F: Distributed Bragg Reflector Simulation Outputs



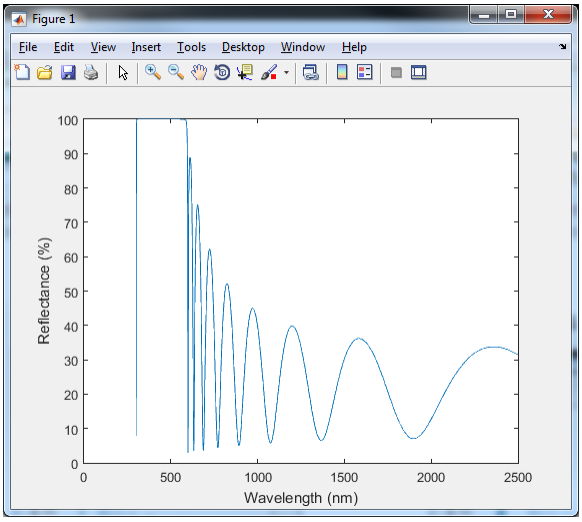
Reflectivity of DBR with a-Si and Si3N4 at 400nm



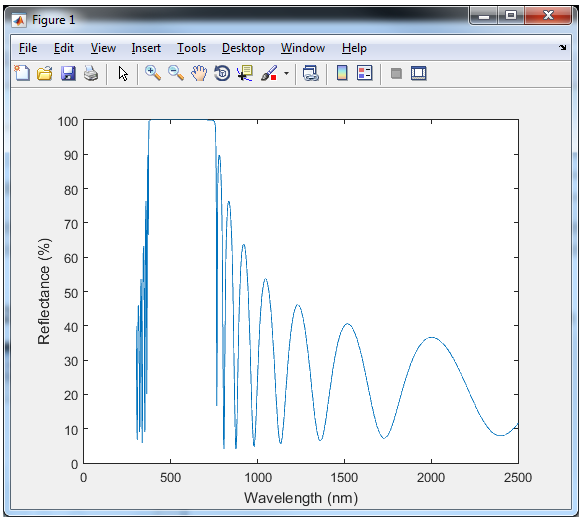
Reflectance of DBR using a-Si and Si3N4 at 500nm



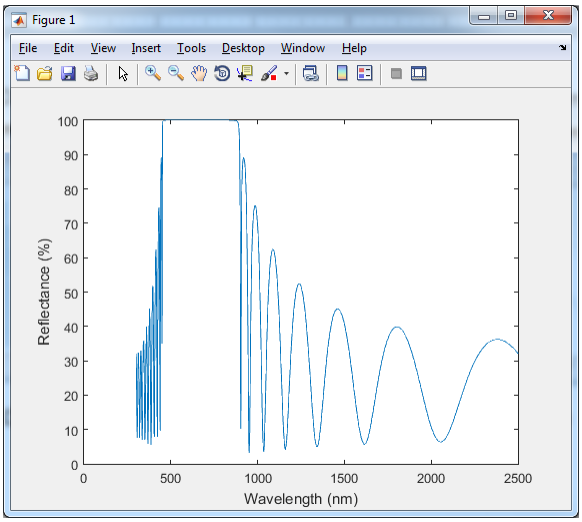
Reflectance of DBR using a-Si and Si3N4 at 700nm



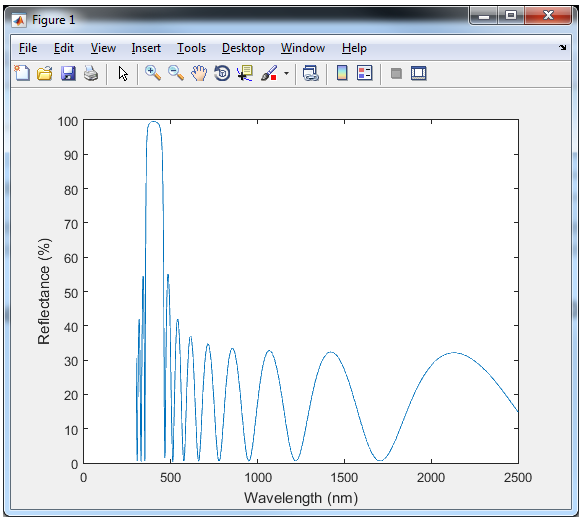
Reflectance of DBR using a-Si and SiO2 at 400nm



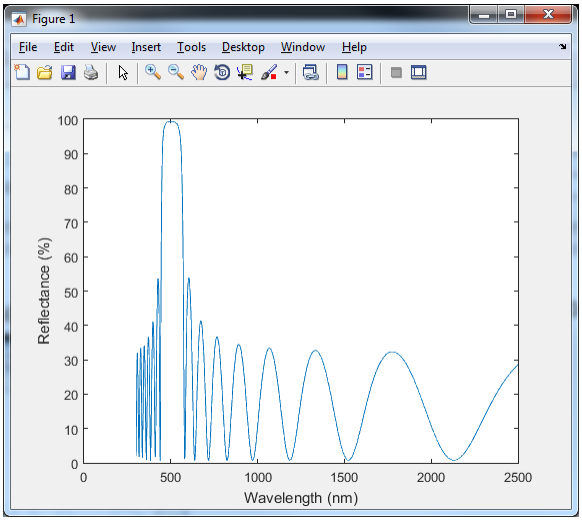
Reflectance of DBR using a-Si and SiO2 at 500nm



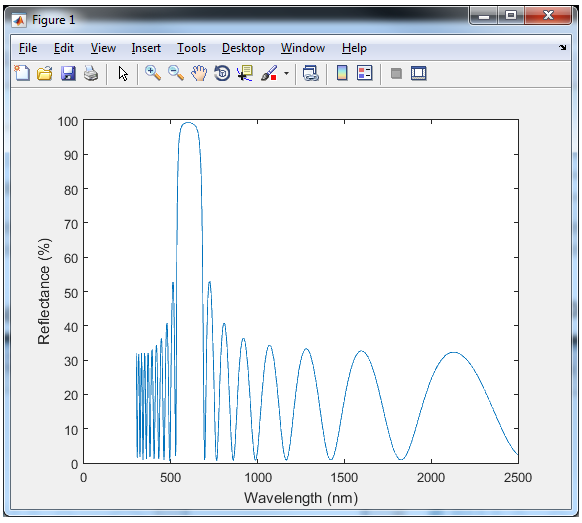
Reflectance of DBR using a-Si and SiO2 at 600nm



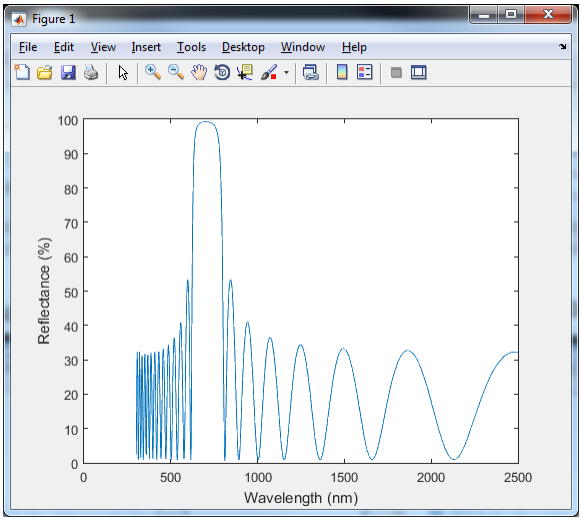
Reflectance of DBR using Si3N4 and SiO2 at 400nm



Reflectance of DBR using Si3N4 and SiO2 at 500nm

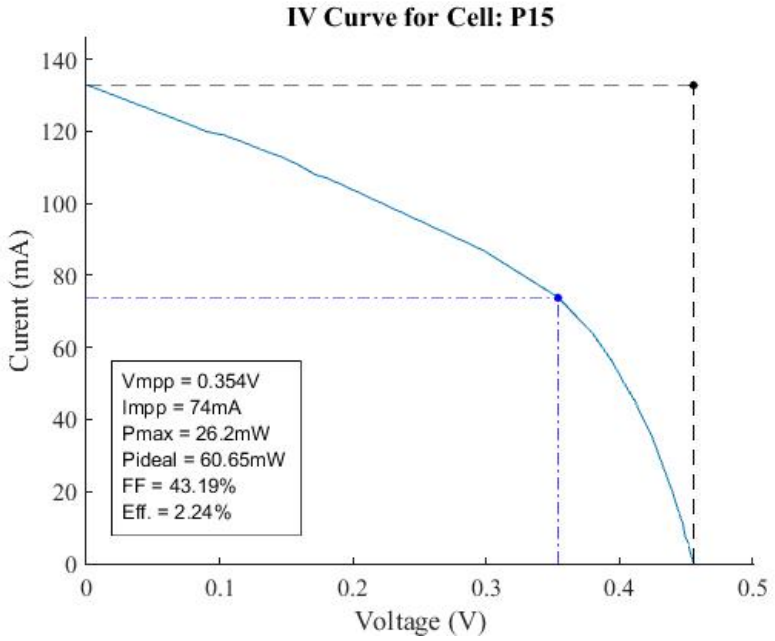


Reflectance of DBR using Si3N4 and SiO2 at 600nm

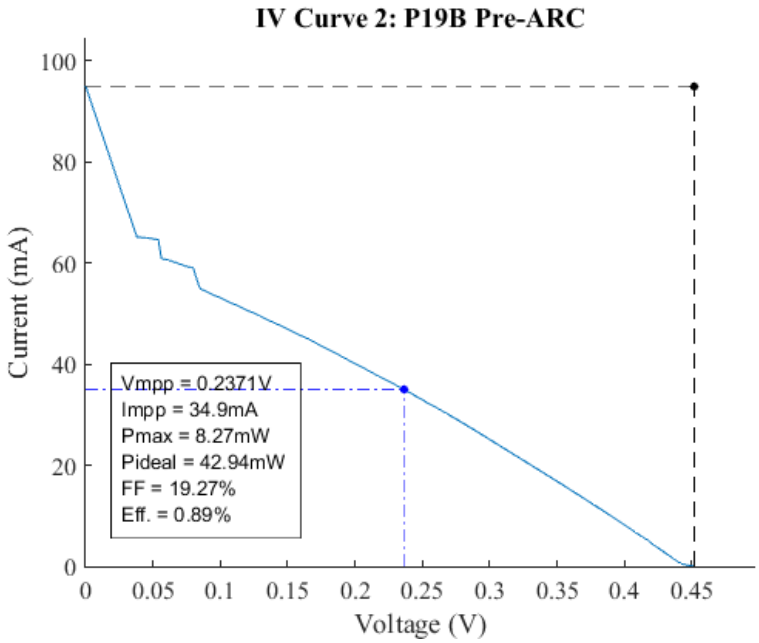


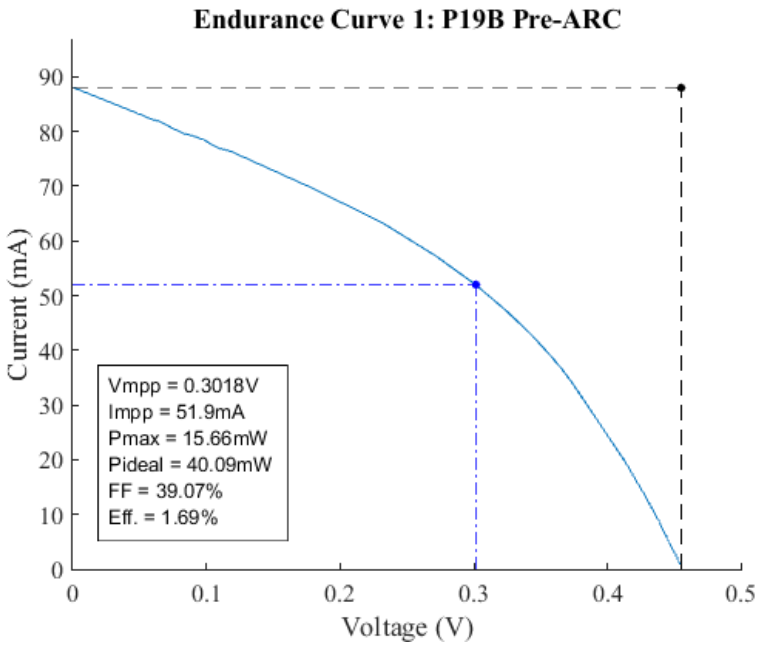
Reflectance of DBR using Si3N4 and SiO2 at 700nm

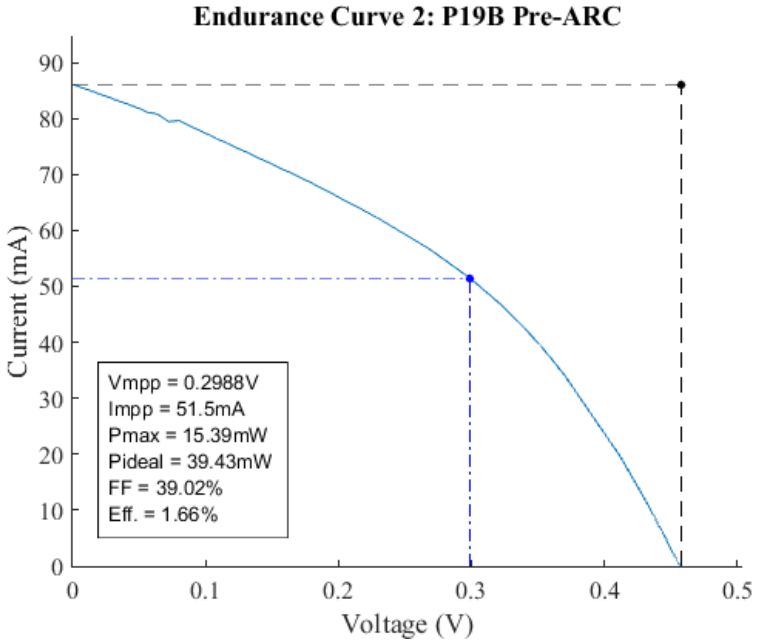
Appendix G: Test Data of Voc, Isc, Fill Factor, and Efficiency

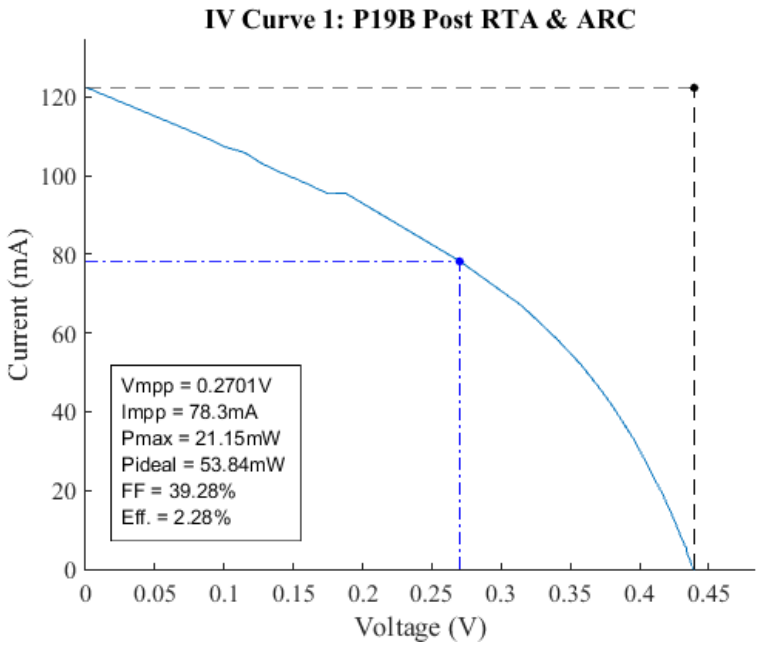


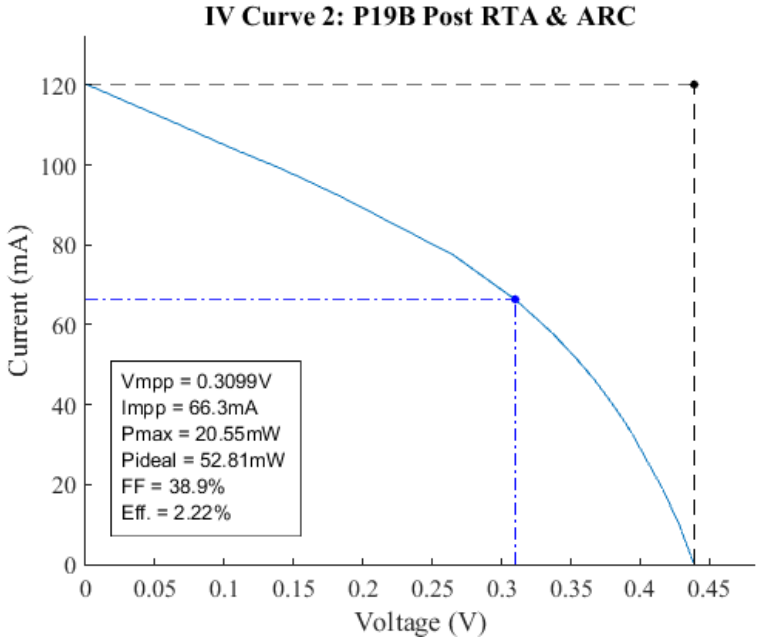
Although damaged during processing, Voc and Isc was measured to calculate the fill factor and efficiency for the p-type silicon wafer P15.

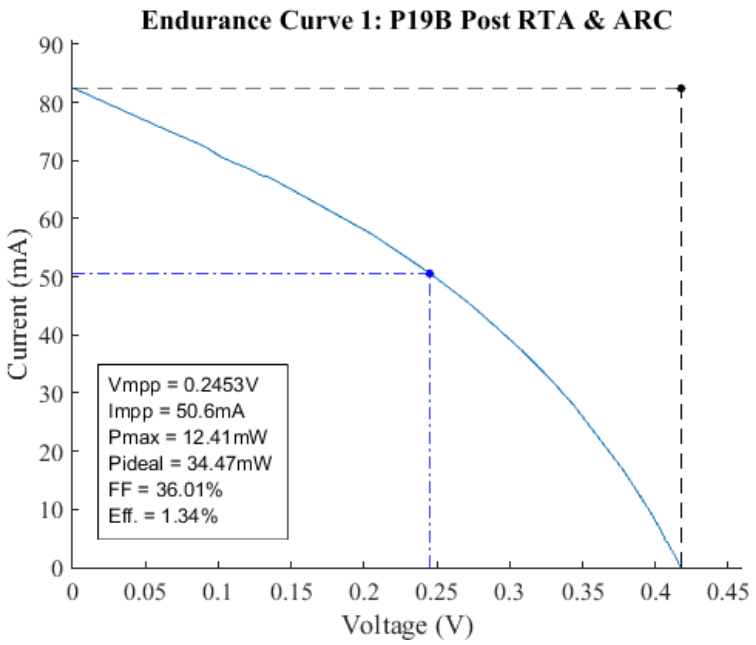


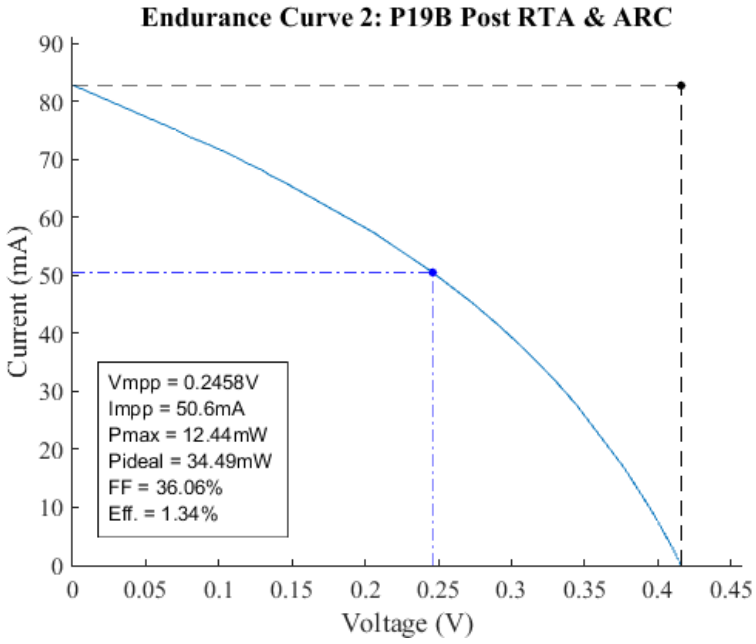

Endurance Curve 1: P19B Pre-ARC
Current (mA)
Voltage (V)
Vmpp = 0.3018V
Impp = 51.9mA
Pmax = 15.66mW
Pideal = 40.09mW
FF = 39.07%
Eff. = 1.69%

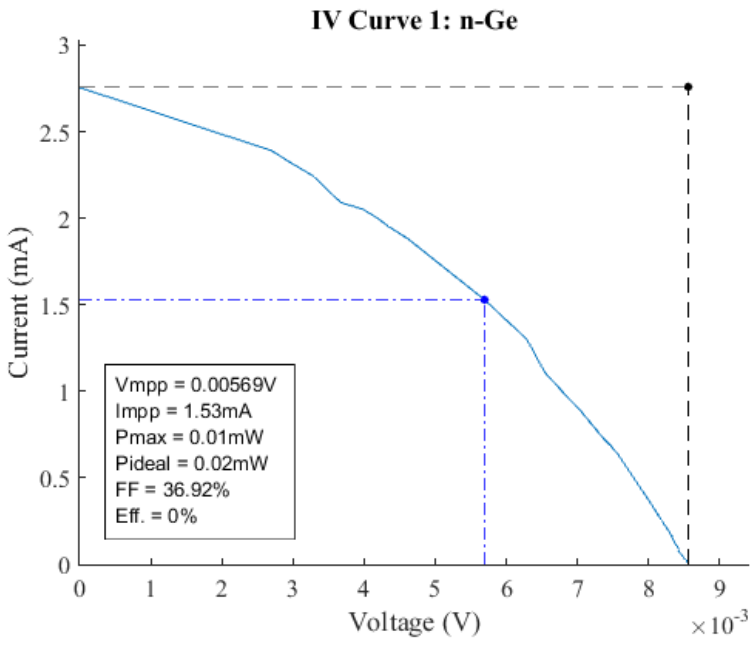

Endurance Curve 2: P19B Pre-ARC
Current (mA)
Voltage (V)
Vmpp = 0.2988V
Impp = 51.5mA
Pmax = 15.39mW
Pideal = 39.43mW
FF = 39.02%
Eff. = 1.66%

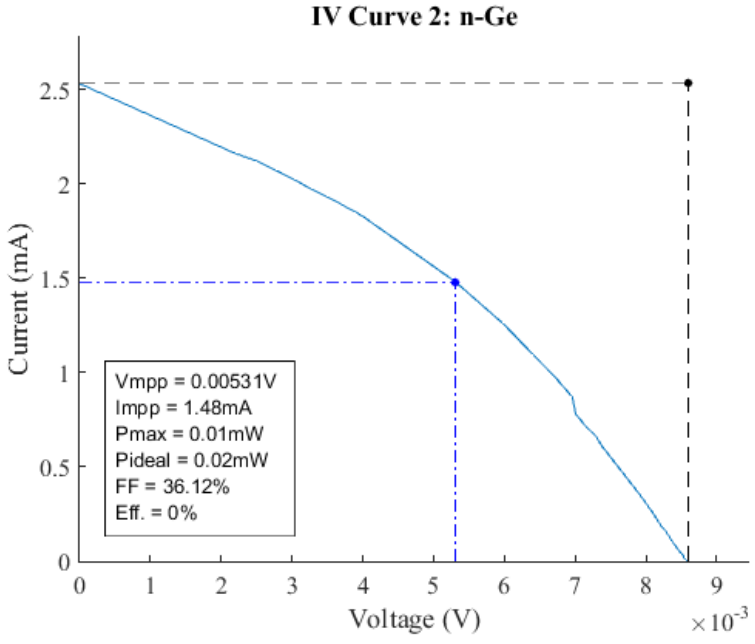

IV Curve 1: P19B Post RTA & ARC
Current (mA)
Voltage (V)
Vmpp = 0.2701V
Impp = 78.3mA
Pmax = 21.15mW
Pideal = 53.84mW
FF = 39.28%
Eff. = 2.28%

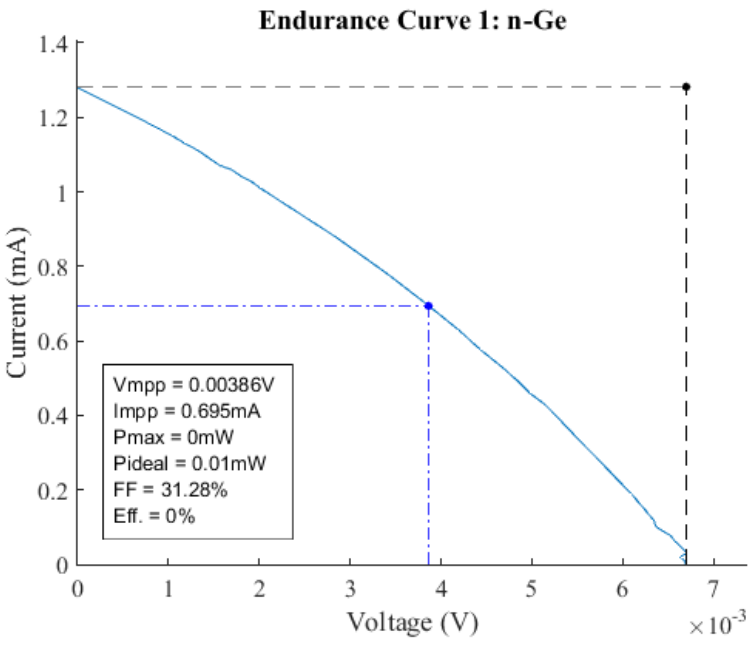

IV Curve 2: P19B Post RTA & ARC
Current (mA)
Voltage (V)
Vmpp = 0.3099V
Impp = 66.3mA
Pmax = 20.55mW
Pideal = 52.81mW
FF = 38.9%
Eff. = 2.22%

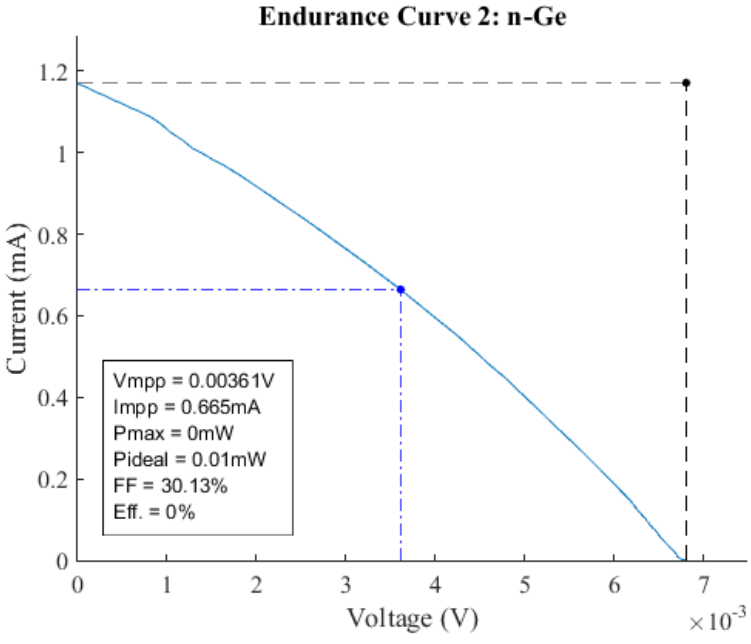

Endurance Curve 1: P19B Post RTA & ARC
Current (mA)
Voltage (V)
Vmpp = 0.2453V
Impp = 50.6mA
Pmax = 12.41mW
Pideal = 34.47mW
FF = 36.01%
Eff. = 1.34%

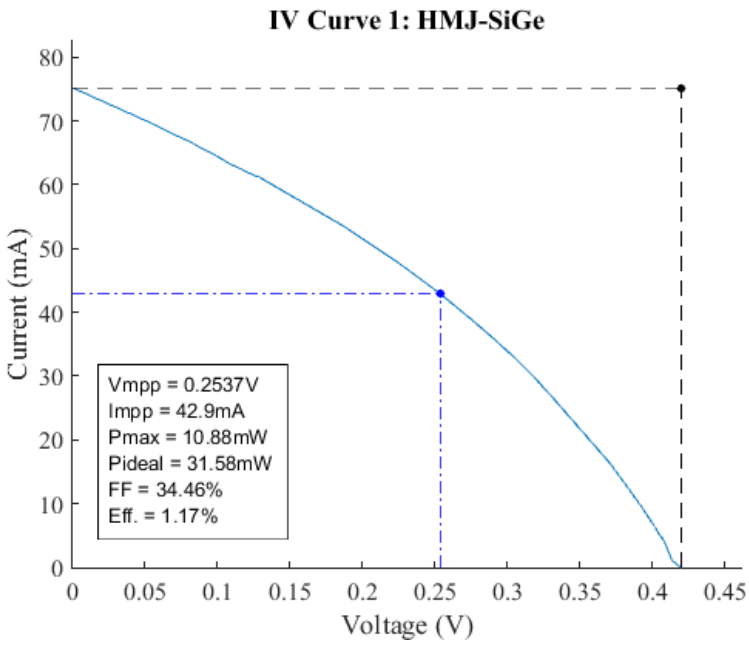

Endurance Curve 2: P19B Post RTA & ARC
Current (mA)
Voltage (V)
Vmpp = 0.2458V
Impp = 50.6mA
Pmax = 12.44mW
Pideal = 34.49mW
FF = 36.06%
Eff. = 1.34%

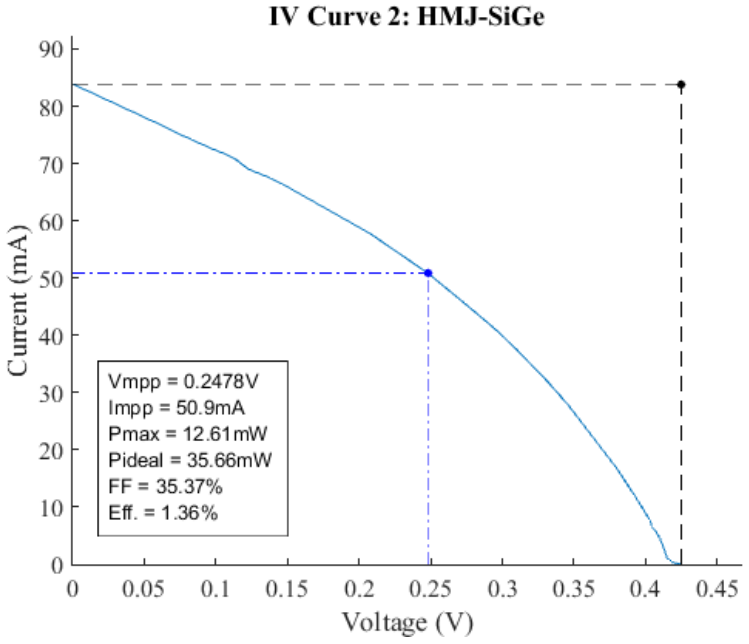

IV Curve 1: n-Ge
Current (mA)
Voltage (V)
×10^-3
Vmpp = 0.00569V
Impp = 1.53mA
Pmax = 0.01mW
Pideal = 0.02mW
FF = 36.92%
Eff. = 0%

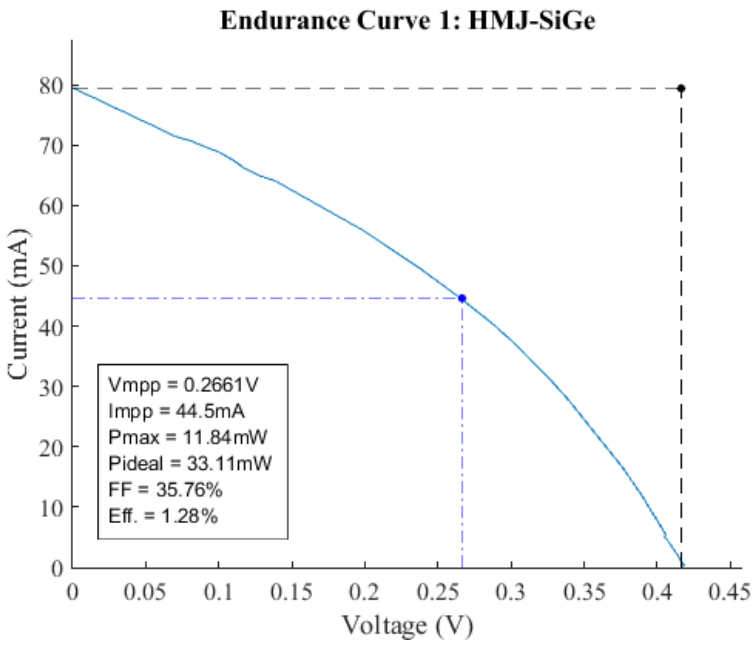

IV Curve 2: n-Ge
Current (mA)
Voltage (V)
×10^-3
Vmpp = 0.00531V
Impp = 1.48mA
Pmax = 0.01mW
Pideal = 0.02mW
FF = 36.12%
Eff. = 0%

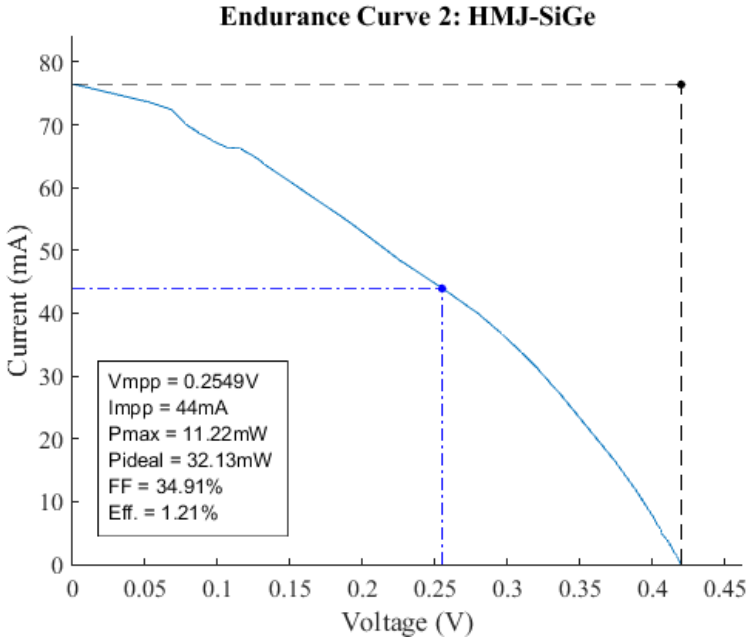

Endurance Curve 1: n-Ge
Current (mA)
Voltage (V)
×10^-3
Vmpp = 0.00386V
Impp = 0.695mA
Pmax = 0mW
Pideal = 0.01mW
FF = 31.28%
Eff. = 0%


Endurance Curve 2: n-Ge
Current (mA)
Voltage (V)
×10^-3
Vmpp = 0.00361V
Impp = 0.665mA
Pmax = 0mW
Pideal = 0.01mW
FF = 30.13%
Eff. = 0%

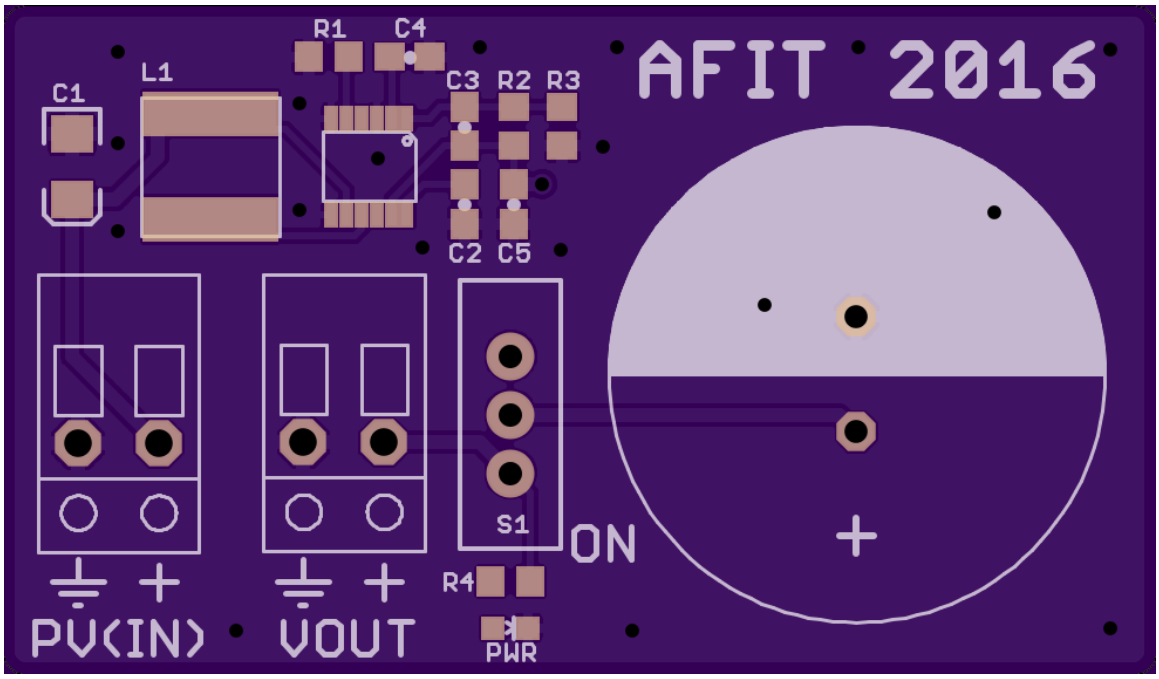

IV Curve 1: HMJ-SiGe
Current (mA)
Voltage (V)
Vmpp = 0.2537V
Impp = 42.9mA
Pmax = 10.88mW
Pideal = 31.58mW
FF = 34.46%
Eff. = 1.17%


IV Curve 2: HMJ-SiGe
Current (mA)
Voltage (V)
Vmpp = 0.2478V
Impp = 50.9mA
Pmax = 12.61mW
Pideal = 35.66mW
FF = 35.37%
Eff. = 1.36%


Endurance Curve 1: HMJ-SiGe
Current (mA)
Voltage (V)
Vmpp = 0.2661V
Impp = 44.5mA
Pmax = 11.84mW
Pideal = 33.11mW
FF = 35.76%
Eff. = 1.28%


Endurance Curve 2: HMJ-SiGe
Current (mA)
Voltage (V)
Vmpp = 0.2549V
Impp = 44mA
Pmax = 11.22mW
Pideal = 32.13mW
FF = 34.91%
Eff. = 1.21%

Appendix H: Solar Power Controller Circuit



Appendix I: LTC3105 Voltage Booster Datasheet

LTC3105

400mA Step-Up DC/DC Converter with Maximum Power Point Control and 250mV Start-Up

FEATURES

- **Low Start-Up Voltage: 250mV**
- **Maximum Power Point Control**
- **Wide V_{IN} Range: 225mV to 5V**
- **Auxiliary 6mA LDO Regulator**
- **Burst Mode® Operation: I_Q = 24µA**
- Output Disconnect and Inrush Current Limiting
- $V_{IN} > V_{OUT}$ Operation
- Antiringing Control
- Soft Start
- Automatic Power Adjust
- Power Good Indicator
- 10-Lead 3mm × 3mm × 0.75mm DFN and 12-Lead MSOP Packages

APPLICATIONS

- Solar Powered Battery/Supercapacitor Chargers
- Energy Harvesting
- Remote Industrial Sensors
- Low Power Wireless Transmitters
- Cell Phone, MP3, PMP and GPS Accessory Chargers

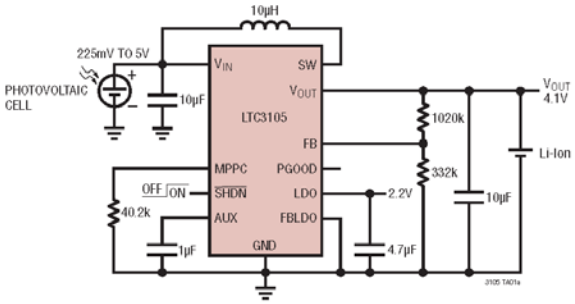
DESCRIPTION

The LTC®3105 is a high efficiency step-up DC/DC converter that can operate from input voltages as low as 225mV. A 250mV start-up capability and integrated maximum power point controller (MPPC) enable operation directly from low voltage, high impedance alternative power sources such as photovoltaic cells, TEGs (thermoelectric generators) and fuel cells. A user programmable MPPC set point maximizes the energy that can be extracted from any power source. Burst Mode operation, with a proprietary self adjusting peak current, optimizes converter efficiency and output voltage ripple over all operating conditions.

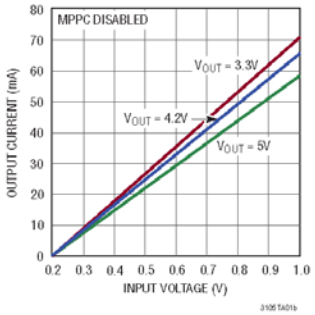
The AUX powered 6mA LDO provides a regulated rail for external microcontrollers and sensors while the main output is charging. In shutdown, I_Q is reduced to 10µA and integrated thermal shutdown offers protection from overtemperature faults. The LTC3105 is offered in 10-lead 3mm × 3mm × 0.75mm DFN and 12-lead MSOP packages.

TYPICAL APPLICATION

Single Photovoltaic Cell Li-Ion Trickle Charger



Output Current vs Input Voltage

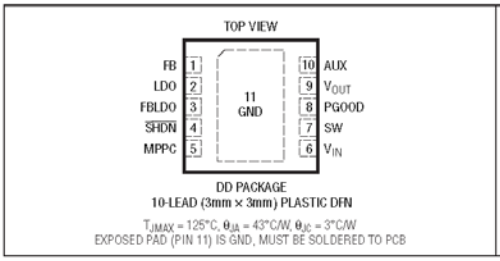


ABSOLUTE MAXIMUM RATINGS (Note 1)

SW Voltage
- DC ..... –0.3V to 6V
- Pulsed (<100ns) ..... –1V to 7V

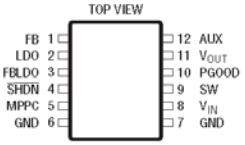
Voltage, All Other Pins ..... –0.3V to 6V
Operating Junction Temperature Range (Note 2) ..... –40°C to 85°C
Maximum Junction Temperature (Note 4) ..... 125°C
Storage Temperature ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec.)
- MS Package ..... 300°C

PIN CONFIGURATION



DD PACKAGE
10-LEAD (3mm × 3mm) PLASTIC DFN

T_{JMAX} = 125°C, θ_{JA} = 43°C/W, θ_{JC} = 3°C/W
EXPOSED PAD (PIN 11) IS GND, MUST BE SOLDERED TO PCB



MS PACKAGE
12-LEAD PLASTIC MSOP

T_{JMAX} = 125°C, θ_{JA} = 130°C/W, θ_{JC} = 21°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3105EDD#PBF	LTC3105EDD#TRPBF	LFQC	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C
LTC3105EMS#PBF	LTC3105EMS#TRPBF	3105	12-Lead Plastic MSOP	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{AUX} = V_{OUT} = 3.3V, V_{LDO} = 2.2V, V_{IN} = 0.6V, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Step-Up Converter						
Input Operating Voltage		●	0.225		5	V
Input Start-Up Voltage	(Note 5) T_J = 0°C to 85°C (Note 5)	●		0.25	0.4 0.36	V V
Output Voltage Adjust Range		●	1.6		5.25	V
Feedback Voltage (FB Pin)		●	0.984	1.004	1.024	V
V_{OUT} I_Q in Operation	V_{FB} = 1.10V			24		µA
V_{OUT} I_Q in Shutdown	$\overline{SHDN}$ = 0V			10		µA
MPPC Pin Output Current	V_{MPPC} = 0.6V		9.72	10	10.28	µA
$\overline{SHDN}$ Input Logic High Voltage		●	1.1			V
$\overline{SHDN}$ Input Logic Low Voltage		●			0.3	V
N-Channel SW Pin Leakage Current	V_{IN} = V_{SW} = 5V, $V_{\overline{SHDN}}$ = 0V			1	10	µA
P-Channel SW Pin Leakage Current	V_{IN} = V_{SW} = 0V, V_{OUT} = V_{AUX} = 5.25V			1	10	µA
N-Channel On-Resistance: SW to GND				0.5		Ω
P-Channel On-Resistance: SW to V_{OUT}				0.5		Ω
Peak Current Limit	V_{FB} = 0.90V, V_{MPPC} = 0.4V (Note 3)		0.4	0.5		A
Valley Current Limit	V_{FB} = 0.90V, V_{MPPC} = 0.4V (Note 3)		0.275	0.35		A
PGOOD Threshold (% of Feedback Voltage)	V_{OUT} Falling		85	90	95	%
LDO Regulator						
LDO Output Adjust Range	External Feedback Network, V_{AUX} > V_{LDO}	●	1.4		5	V
LDO Output Voltage	V_{FBLDO} = 0V	●	2.148	2.2	2.236	V
Feedback Voltage (FBLDO Pin)	External Feedback Network	●	0.984	1.004	1.024	V
Load Regulation	I_{LDO} = 1mA to 6mA			0.40		%
Line Regulation	V_{AUX} = 2.5V to 5V			0.15		%
Dropout Voltage	I_{LDO} = 6mA, V_{OUT} = V_{AUX} = 2.2V			105		mV
LDO Current Limit	V_{LDO} 0.5V Below Regulation Voltage	●	6	12		mA
LDO Reverse-Blocking Leakage Current	V_{IN} = V_{AUX} = V_{OUT} = 0V, $V_{\overline{SHDN}}$ = 0V			1		µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

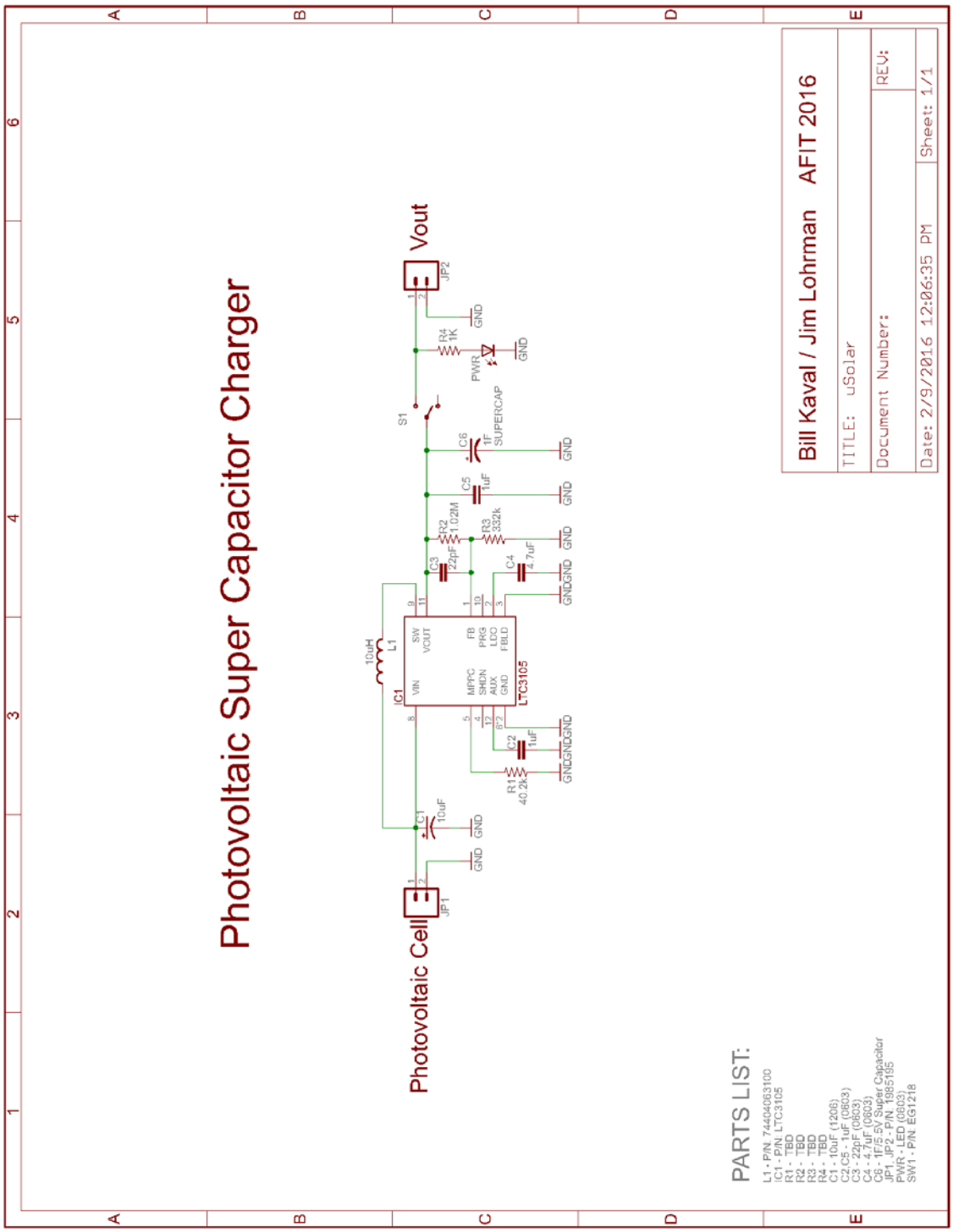
Note 2: The LTC3105 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3105E is guaranteed to meet specifications from 0°C to 85°C junction temperature. Specifications over the –40°C to 85°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors.

Note 3: Current measurements are performed when the LTC3105 is not switching. The current limit values measured in operation will be somewhat higher due to the propagation delay of the comparators.

Note 4: This IC includes over temperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 5: The LTC3105 has been optimized for use with high impedance power sources such as photovoltaic cells and thermoelectric generators. The input start-up voltage is measured using an input voltage source with a series resistance of approximately 200mΩ and MPPC enabled. Use of the LTC3105 with lower resistance voltage sources or with MPPC disabled may result in a higher input start-up voltage.

Appendix J: Photovoltaic Super Capacitor Charger Schematic



Appendix K: N-Ge Wafer Process Follower (Step 1)

Wafer	Purpose	Mask	Process	Print Date
n-Ge	**GeTe pn-junction**	**None**	**Clean & deposition**	**2/1/2016**

Init.	Process Step	Notes	Date Time
	Solvent Clean (by hand) ⊏ 30 sec acetone rinse ⊏ 30 sec methanol rinse ⊏ 30 sec DI water rinse ⊏ Dry with nitrogen on texwipes ⊏ 2 min 110°C hot plate bake	**Start Date** **Start Time**	
	Pre-Metallization Surface Preparation ⊏ DI:BOE (7:1) solution etch for 30 sec ⊏ 30 sec DI water rinse ⊏ Dry with nitrogen		
	Sputter Deposition and Verification ⊏ Place n-Ge wafer (polished-side up) with witness sample on loadlock plate ⊏ Sputter *50nm GeTe (2mins @ 100W RF power)* ⊏ Verify thickness of GeTe on profilometer. Record value		
	GeTe Transition to Create c-GeTe ⊏ Measure GeTe film in several spots with ohmmeter. Record values. ⊏ Bake at 300°C for 2 mins on hotplate ⊏ Measure GeTe film in several spots with ohmmeter. Record values. ⊏ If the average resistance has not decreased to 300-900Ω, increase hotplate temperature by 50°C for 2 mins. Record values and re-evaluate. ⊏ If the average resistance has not decreased to 300-900Ω, use hotplate in Rm 117. Bake at 400°C for 2 mins. Record values and re-evaluate one last time		
	Pre-Metallization Surface Preparation ⊏ DI:BOE (7:1) solution etch for 30 sec ⊏ 30 sec DI water rinse ⊏ Dry with nitrogen		
	Metallization ⊏ Evaporate *100Å of Ti / 5000Å of Au* onto c-GeTe side of n-Ge wafer		
	Photoresist – to protect the bottom GeTe pn-junction side ⊏ Place n-Ge wafer with GeTe pn-junction side up on spinner ⊏ Flood with 1818 photoresist ⊏ 30 sec spin at 4,000 rpm ⊏ 2 min @ 110°C hot plate bake		

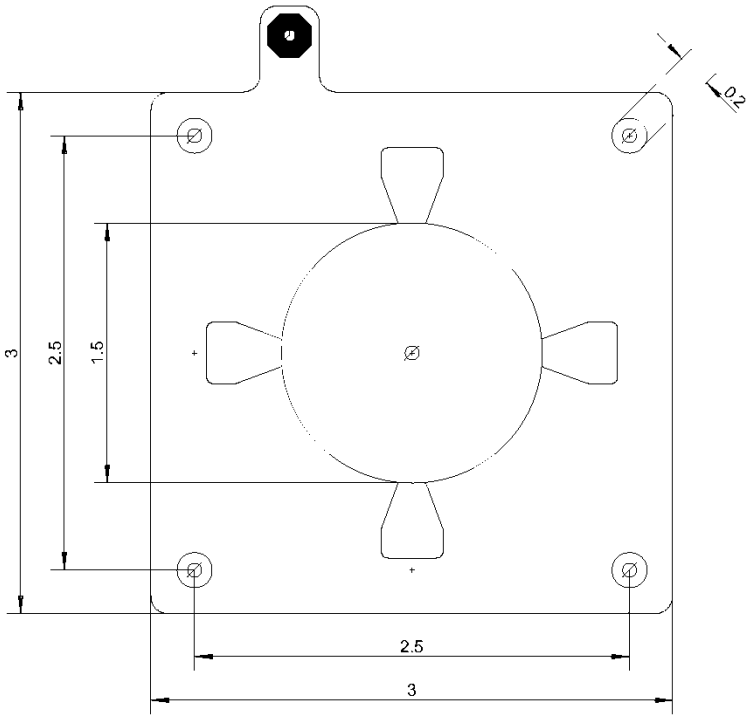
Appendix L: N-Ge Wafer Process Follower (Step 2)

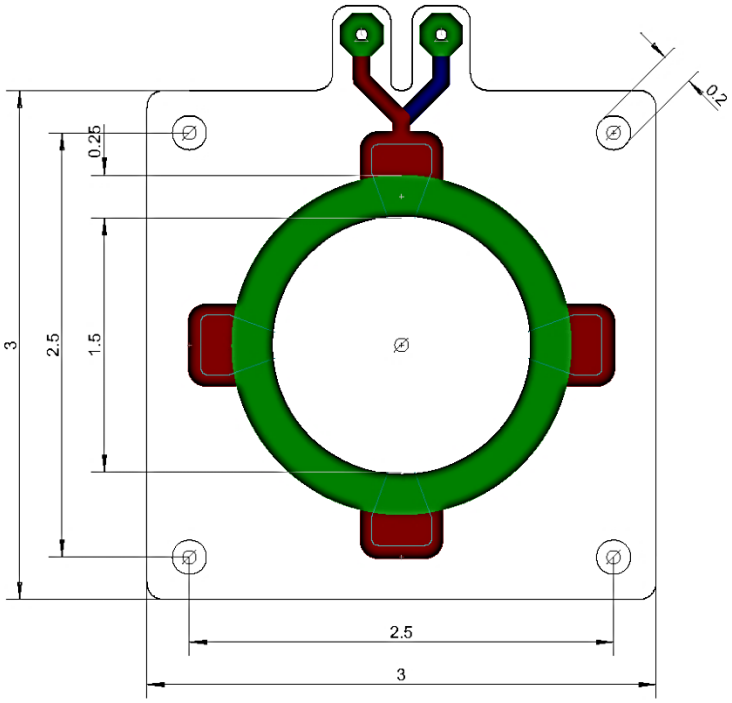
Wafer	Purpose	Mask	Process	Print Date
n-Ge	Top Grating	H-pattern grating	Clean, lithography & deposition	2/1/2016

Init.	Process Step	Notes	Date Time
	Solvent Clean (by spinner @ 500rpms) ⊏ Place n-Ge wafer (*unpolished*-side up) on spinner ⊏ 30 sec acetone rinse ⊏ 30 sec methanol rinse ⊏ 30 sec Di water ⊏ Dry with nitrogen on spinner ⊏ 2 min 110°C hot plate bake	Start Date Start Time	
	Photoresist – for litho of top grating ⊏ Place n-Ge wafer (*unpolished*-side up) on spinner ⊏ Flood with 1818 photoresist ⊔ 30 sec spin at 4,000 rpm ⊏ 2min @ 110°C hot plate bake		
	Clean H-pattern contact mask under solvent hood (by hand) ⊔ 30 sec acetone rinse ⊏ 30 sec methanol rinse ⊔ 30 sec IPA rinse ⊏ Dry with nitrogen ⊔ Position mask in MJB3 Mask Aligner		
	Expose 1818 (H-Pattern Grating Mask) ⊏ Place n-Ge wafer in the MJB3 ⊏ Centered wafer under mask as best as possible ⊏ Expose wafer with UV using MJB3 contact mask aligner for 7 sec		
	1818 Develop ⊏ Place wafer on spinner under Base Hood ⊏ 45 sec develop with DI:351 (5:1) developer at 500 rpm ⊏ 30 sec DI water rinse at 500 rpm ⊔ Dry with nitrogen at 500 rpm ⊏ Dry wafer with nitrogen on clean texwipes ⊔ 2 min 110°C hot plate bake		
	Oxygen Plasma Ash ⊔ Place n-Ge wafer in plasma asher, newly developed patterned-side up ⊏ Ash the wafers for 2 min at 50W making sure the reflected power is 0. ⊔ Remove wafers, turn Asher off, turn off oxygen tank in raceway. **Pre-Metallization Surface Preparation** ⊏ DI:BOE (7:1) solution etch for 30 sec ⊏ 30 sec DI water rinse ⊏ Dry with nitrogen		
	Atomic Layer Deposition ⊏ ALD *30Å of Al_2O_3* onto newly developed patterned-side of n-Ge wafer		
	Metallization ⊏ Evaporate *5000Å of Al* onto patterned-side of n-Ge wafer		
	Solvent Clean (by hand) – remove protective photoresist on GeTe side ⊏ 30 sec acetone rinse ⊏ 30 sec methanol rinse ⊏ 30 sec Di water rinse ⊏ Dry with nitrogen on texwipes ⊏ Repeat rinses with solvents and DI water if photoresist still present on surface ⊏ 2 min 110°C hot plate bake		

Wafer	Purpose	Mask	Process	Print Date
n-Ge	**Top Grating**	**H-pattern grating**	**Clean, lithography & deposition**	**2/1/2016**
	Metal Liftoff (wet) ⊏ Pour DI water into empty ultrasonic bath and place glass petri dish on water ⊏ Place n-Ge metal newly developed patterned-side up wafer in glass petri dish ⊏ Add acetone to petri dish until about 1/8 inch above the wafer surface *(note: do not allow wafer to become dry; add more acetone as necessary during liftoff process)* ⊏ Turn on ultrasonic bath and press the sonic button ⊏ Once metal has lifted, turn off ultrasonic bath ⊏ Take petri dish to Solvent Hood to rinse off metal flakes			
	Rapid Thermal Anneal ⊏ RTA 20secs @ 640°C			

Appendix M: PCB Layer Technical Drawings for Solar Cell Fixture





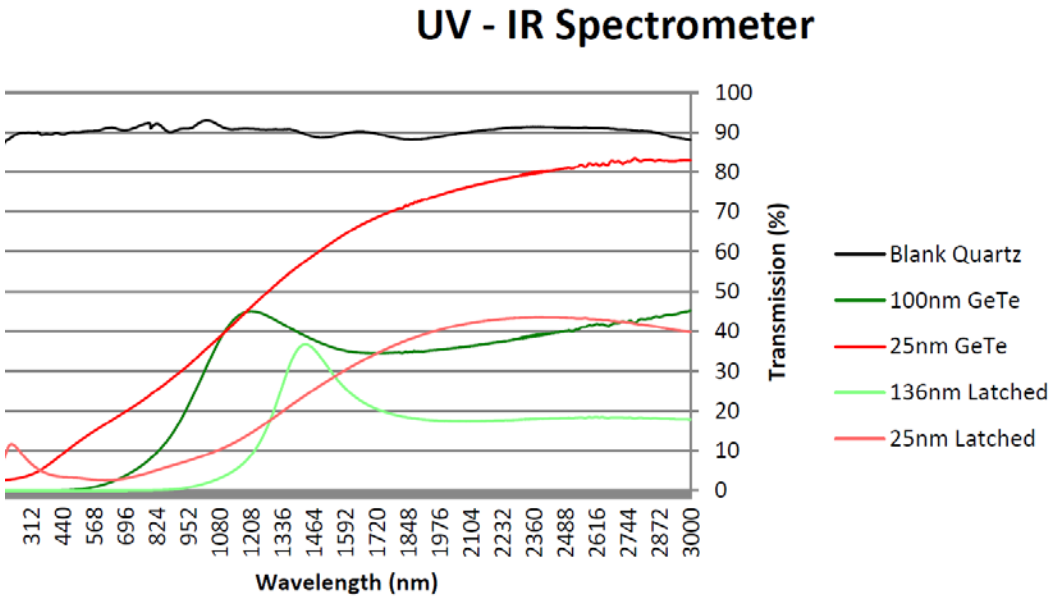
Appendix N: GeTe PN-Junction Testing Data

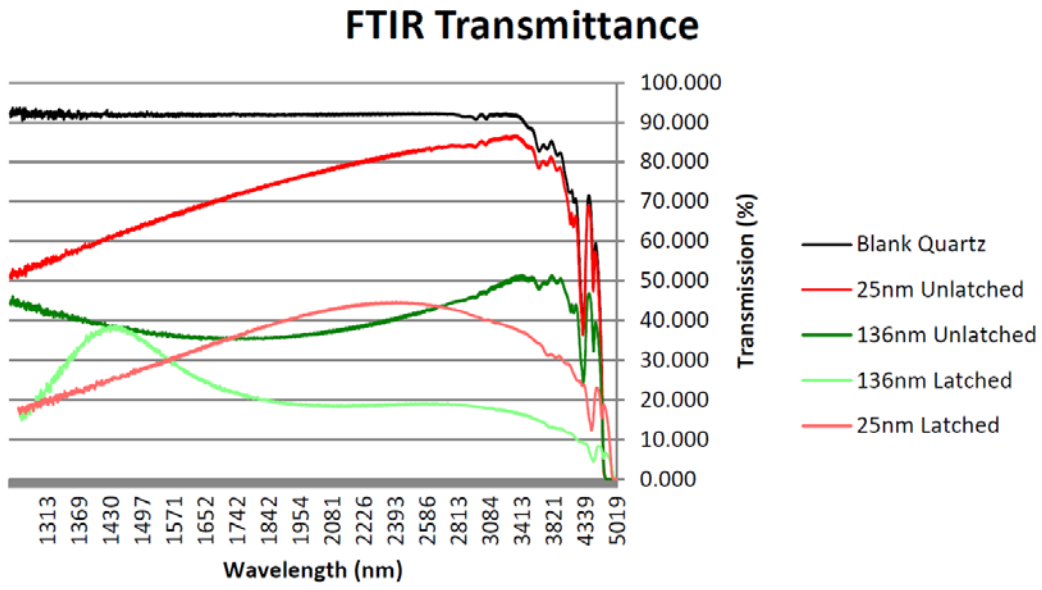
= measurements too jumpy; not confident of data

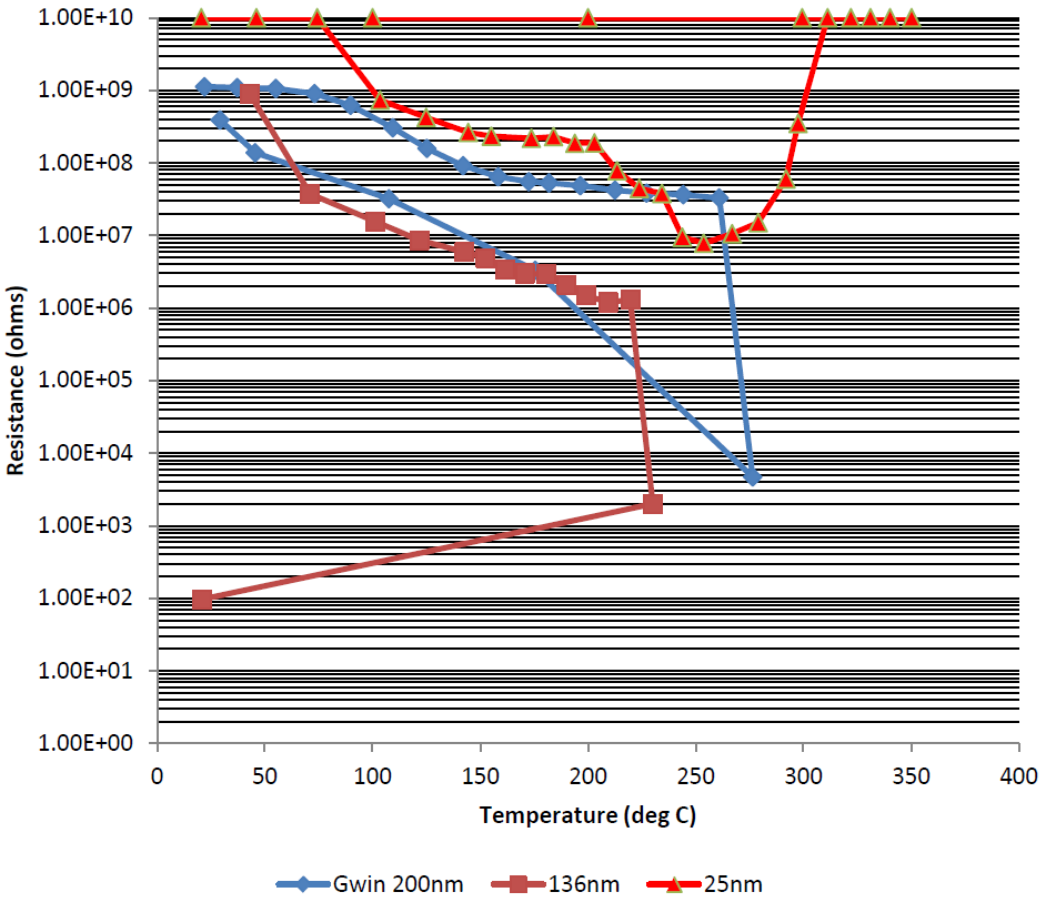
Substrate		N	N	N	N	N	N	N	N	P	P	N	N	P	P
		A	B	C	D	E	F	G	H	I	J	K	L	M	N
Pre-RTA	Voc (uV)	12	4	20	50	8	27	45	230	560	1500	64	326	580	600
	Isc (uA)							1.1	1	0.1	0.2	2.1	1.1	0.1	0.1
	P (pW)							49.5	230	56	300	134.4	358.6	58	60
Thevin R								40.9	230	5600	7500	30.48	296.36	5800	6000
Post-RTA (1x)	Voc (uV)	58	18	34	60	61	bad	29	305	225	150	58	170	250	200
	Isc (uA)	1.5	1.2	2.2	3.3	2.2	bad	1.3	1.2	35.5	13.5	5.3	0.7	44	10
	P (pW)	87	21.6	74.8	198	134.2	bad	37.7	366	7988	2025	307.4	119	11000	2000
Thevin R								22.3	254.2	6.3	11.1	10.9	242.9	5.7	20.0

Item Details	Junction	Description	
A	PN	n-Ge/p-GeTe (600nm)	**600nm** emitter
B	PN	n-Ge/p-GeTe (600nm)	
C	PN	n-Ge/p-GeTe (600nm); evap Au first, then transition	
D	PN	n-Ge/p-GeTe (250nm)	**250nm** emitter
E	PN	n-Ge/p-GeTe (250nm)	
F	PN	n-Ge/p-GeTe (250nm); evap Au first, then transition; accidental rear PN	
G	PIN	n-Ge/i-Ge (10nm)/p-GeTe (250nm)	
H	PN	n-Ge/p-GeTe (250nm); **rear** PN	
I	PIN	p-Ge/i-Ge (10nm)/n-Ge (250nm)	
J	PN	p-Ge/n-Ge (250nm); **rear** PN	
K	PIN	n-Ge/i-Ge (10nm)/p-GeTe (50nm)	**50nm** emitter
L	PN	n-Ge/p-GeTe (50nm); **rear** PN	
M	PIN	p-Ge/i-Ge (10nm)/n-Ge (50nm)	
N	PN	p-Ge/n-Ge (50nm); **rear** PN	

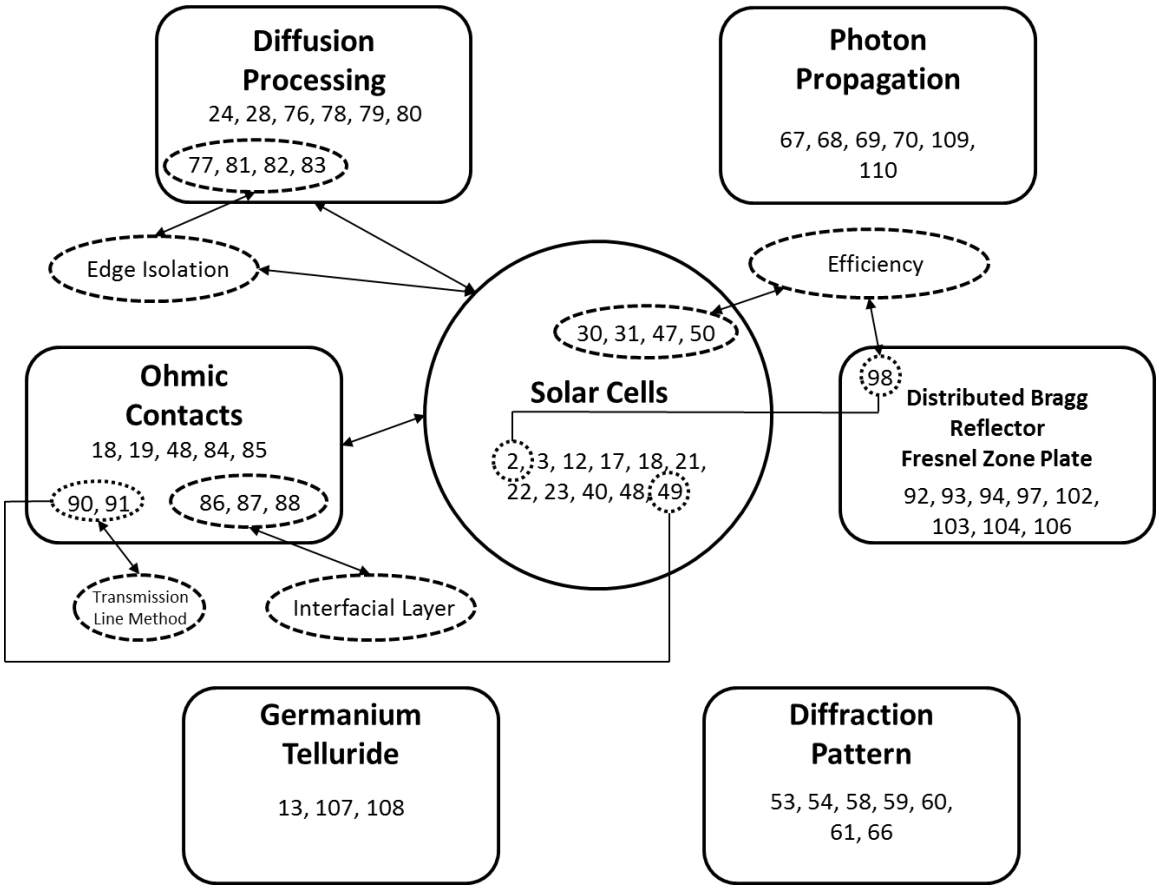
Appendix O: GeTe Transmittance & Transition Data






1.00E+10
1.00E+09
1.00E+08
1.00E+07
1.00E+06
1.00E+05
1.00E+04
1.00E+03
1.00E+02
1.00E+01
1.00E+00
Resistance (ohms)
0
50
100
150
200
250
300
350
400
Temperature (deg C)
Gwin 200nm
136nm
25nm

Appendix P: Visual Bibliography



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14. ABSTRACT

Based on the previous development of the hybrid multi-junction silicon (HMJ-Si) solar cell, this work characterized the preceding design for the development of the hybrid multi-junction silicon germanium (HMJ-SiGe) solar cell architecture. Seven focus areas were investigated: diffraction pattern generation, photon propagation, silicon diffusion processing, ohmic contacts, the distributed Bragg reflector (DBR), the Fresnel zone plate (FZP), and the germanium/germanium telluride (Ge/GeTe) pn-junction. Generated diffraction patterns were theoretically examined, and contact grating design characterization for reflectance and transmittance properties was modeled using rigorous coupled wave analysis. An improved silicon diffusion process follower was developed, and theoretical study and experimental assessment was accomplished for appropriate ohmic contacts, the DBR, the FZP, and the Ge/GeTe pn-junction for incorporation into the new HMJ-SiGe solar cell architecture. Results showed that minima locations are nonexistent, the ratio between the metal width and electrical contact spacing is vital, an interfacial layer is required for de-pinning of the Fermi level, the DBR can reject detrimental wavelengths, the FZP excessively prevents transmittance, and p-type GeTe can form a pn-juncton on n-type germanium. With an average efficiency of 1.27%, the HMJ-SiGe solar cell demonstrated a capstone requirement of charging a capacitor to 2.5 VDC in 11 minutes to illuminate a light emitting diode.

15. SUBJECT TERMS
multi-junction, silicon, germanium, solar cell, germanium telluride, rigorous coupled wave analysis

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