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NANOELECTRONICS DEVELOPMENT AND FABRICATION

SUNY POLYTECHNIC INSTITUTE

JUNE 2018

FINAL TECHNICAL REPORT

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14. ABSTRACT The objective of this effort was to leverage research and development (R&D) investments by New York State and over 300 leading nanoelectronics companies and research institutions at SUNY Polytechnic Institute to developed a process flow for fabricating resistive memory devices (aka: memristors) utilizing a range of different so-called "switching oxides" as the active layer in these devices. After developing and optimizing the process flow, a series of 100 mm wafers containing these devices were fabricated and delivered to AFRL for testing.					
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1. Summary

Leveraged research and development (R&D) investments by New York State and over 300 leading nanoelectronics companies and research institutions at SUNY Polytechnic Institute, located in Albany New York. Combined, these global corporations and the State of New York have invested billions of non-federal dollars to establish SUNY Polytechnic Institute with over 3,000 scientists, faculty and staff as the leading nanotechnology R&D complex. For the research effort described herein, Prof. Nathaniel Cady's research team (at SUNY Polytechnic Institute) developed a process flow for fabricating resistive memory devices (aka: memristors) utilizing a range of different so-called "switching oxides" as the active layer in these devices. After developing and optimizing the process flow, a series of 100mm wafers containing these devices were fabricated and delivered to AFRL for testing.

2. Introduction

The memristor is a two-terminal resistive switching memory (RRAM) nanoscale device, which is recognized as the fourth fundamental electrical element in addition to resistors, capacitors, and inductors. By utilizing different resistance values to store information, memristors can function as low-power, highly-scalable device elements – critically essential properties for memory and field programmable gate array applications. More importantly, memristors have exhibited unique self-learning properties and can execute complex logic functions, which enables innovative logic, data processing, and implementation of neuromorphic systems. And, in contrast with other emerging nanoelectronic devices, memristors can utilize CMOS-compatible oxide and electrode materials, which is dramatically simplifies CMOS-memristor integration. These factors underscore the promise and feasibility of large-scale CMOS-memristor hybrid nanoelectronics and point to their significant impact on future IC applications.

This project resulted in the development of a unique process flow for fabricating memristors consisting of a variety of different switching oxides (including hafnium oxide, tantalum oxide, and zirconium oxide). After optimizing the process flow and memristor device performance, the Cady laboratory delivered a series of 100mm wafers containing memristor devices for subsequent electrical testing experiments by AFRL.

3. Methods, Assumptions and Procedures

3.1 Fabrication

In this effort, memristor devices were built in SUNY Polytechnic Institute's 200mm cleanroom facilities, using a variety of thin film deposition techniques, photolithography, and reactive ion etching. A detailed description of the fabrication process is provided in the results section, below.

3.1 Metrology

To monitor fabrication efforts and troubleshoot problems during device development efforts, a range of different metrology tools were used. These included scanning electron microscopy (SEM), x-ray photoelectron spectroscopy (XPS), transmission electron microscopy (TEM), and secondary ion mass spectroscopy (SIMS). These techniques were all performed in-house at the SUNY Polytechnic Institute metrology facility.

3.3 Device Testing

Professor Cady's lab maintains and operates a B1500A semiconductor analyzer connected to a manual probe station capable of handling wafers or pieces of wafers. The mainframe is equipped with 4 high-resolution SMU units, a capacitive measurement unit (MFCMU) and waveform generating and fast-measurement unit (WGFMU). Memristor device characteristics were extracted by using DC-sweep as well as pulsing techniques. In both cases a 1 transistor 1 ReRAM (1T1R) setup was used to limit the current through the ReRAM during the set and forming operation to the saturation current of the transistor which was set by the transistor gate voltage. Mainly two kinds of transistors were used: **1.** an external JFET (Junction gate field effect transistor) which was connected to the system via a discrete Keithley transistor box and **2.** an integrated on-chip transistor which was implemented right underneath our integrated ReRAM. A manual probe station was used to generate preliminary results and longtime endurance measurements. DC-sweeps were preferably used to form the devices while a self-developed pulsing software in conjunction with the WGFMU enables endurance measurement up to 10^{12} cycles while recording every single cycle. Access to a semi-automatic temperature controlled 300mm probe station equipped with the same semiconductor analyzer already operated in the Cady-lab was possible at an university-owned laboratory on the SUNY Poly campus. This probe station was used to generate statistical data in a short amount of time as well as perform measurements at temperatures ranging from room temperature to 300 C.

4. Results and Discussion

4.1 Key Accomplishments

The key accomplishments for this effort were:

1. *Development of a process flow for fabricating memristor "crossbar" using various metal oxides as the switching layer.*
2. *Fabrication of memristor crossbar devices on 100mm wafers and delivery to AFRL for testing.*

4.2 The specific tasks of the project included:

Optimize a fabrication process for memristor crossbar devices.

- Using a 100mm wafer platform, develop a process flow that yields functional memristive devices in a crossbar array format, that can be subsequently tested via electronic probe station and subjected to thermal fluctuation and radiation bombardment for reliability studies.

Fabricate memristor crossbar arrays and deliver to AFRL for testing.

- Using methods developed in the first task to fabricate memristor crossbar arrays, then deliver to AFRL for testing (temperature and radiation bombardment).

4.3 Fabrication Protocol for Memristors

As a result of this effort, the following fabrication protocol was developed. This protocol represents >1 year of process development in the SUNY Polytechnic Institute 200mm nanofabrication facility. The process consists of photolithography and reactive ion etching steps to define bottom metal electrodes (in a crossbar layout), followed by blanket deposition of the switching oxide (hafnium oxide, tantalum oxide, or zirconium oxide), followed by photolithography and lift-off patterning of a top electrode layer. In summary, this procedure results in arrays of memristive crossbar devices. A detailed summary of the procedure is provided in the sections below, and a visual overview of the process is shown.

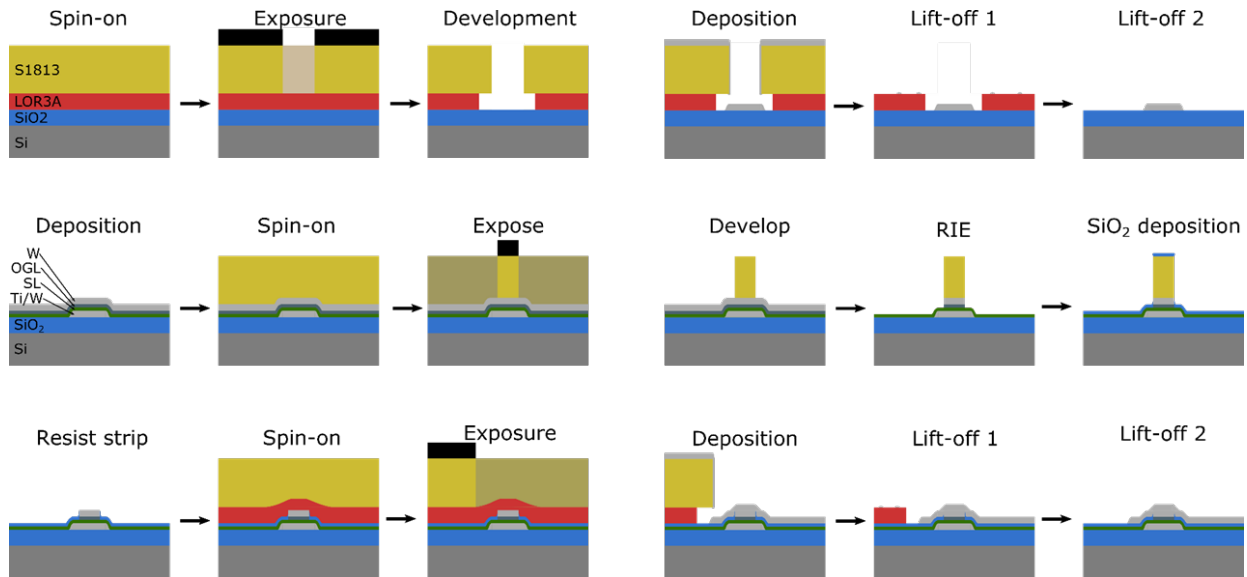


Figure 1. Overview of the fabrication approach for memristor crossbar arrays.

4.3.1 Mask design and usage

The mask is designed as a split mask, meaning we have two layer on one physical mask. This reduces the amount of masks needed and by this reduces the cost of the process. An additional mask was required in later stages of the development resulting in 3 masks for only 4 layers. To access the second layer on a mask one has to rotate the mask from its normal position on the holder of 180°.

The three different masks used in this process are:

- RRAM Main
 - Bottom electrode (not rotated)
 - Top interconnect (180° rotated)
- RRAM Via
 - RRAM device stack etch (not rotated)
- BE contact
 - Bottom contact pad opening (not rotated)

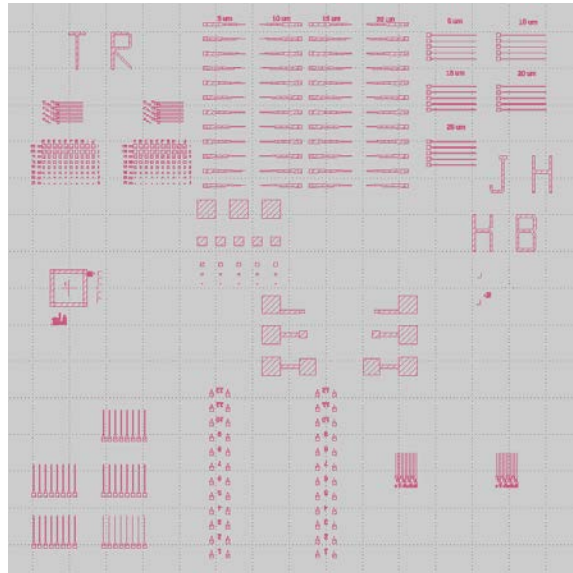


Figure 2: Layout of the mask 'RRAM Main' for the bottom electrode and the top interconnect.

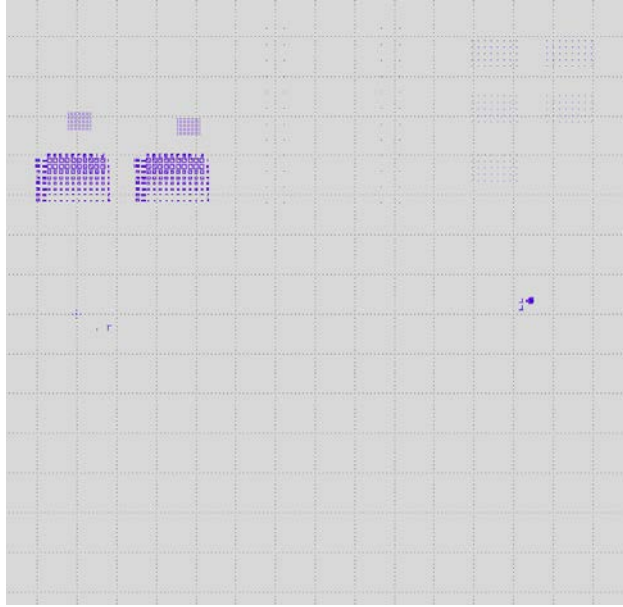


Figure 3: Layout of the mask 'RRAM Via' for the bottom electrode and the top interconnect.

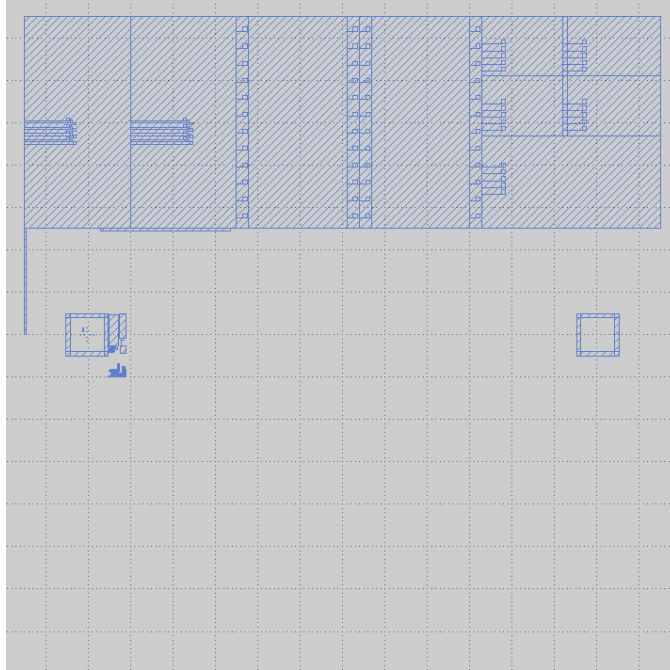


Figure 4: Layout of the mask 'BE contact' for the opening of the bottom contact.

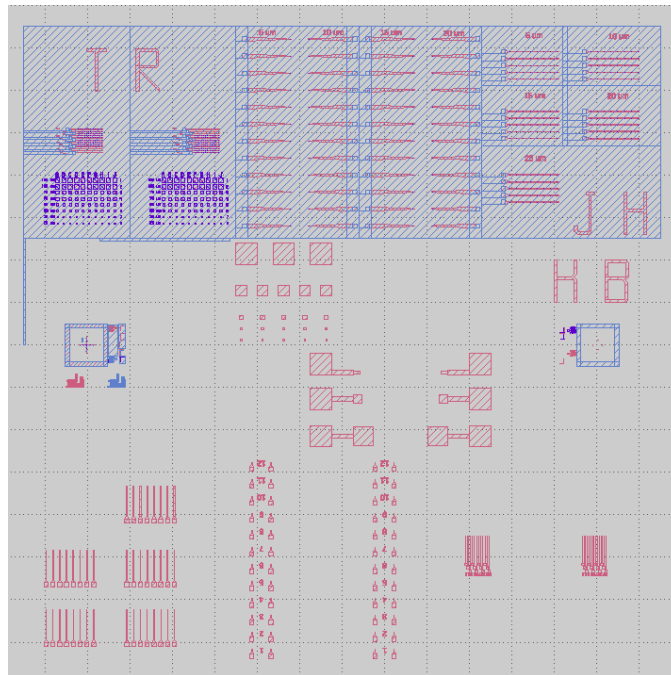


Figure 5: Combined Layout of the masks 'RRAM Main', 'RRAM Via' and 'BE contact'.

Bottom electrode and interconnect

Our design utilizes tungsten as the bottom interconnect which is typically inert enough to serve as the bottom electrode (BE) of the RRAM (memristor) device. To create the BE pattern a lift-

off process was chosen for simplicity purposes. Three different steps are necessary and discussed here: lithography, deposition and the resist lift-off.

4.3.2 Lithography

For the lift-off process a double structure consisting of LOR-3A and S1813 photoresist was used. The S1813 is photosensitive and creates the pattern via exposure while the LOR-3A is not photosensitive but soluble in MIF300. This creates the undercut necessary to avoid metal wings on the edges of the BE (Figure 6). The creation of metal wings is a serious concern because it would cause the BE to shorten with the later created top electrode (TE). Figure 7 shows two AFM images identifying the problem of creating metal wings due to a lack of undercut of the LOR3A under the photoresist. The undercut needs to extend around 500nm to prevent sputtering of the LOR3A wall due to non-directional movement of sputtered atoms. If the undercut extends too far a collapse of the photoresist (here S1813) might occur causing the same problematic with side wings. A far extension might be caused by an adhesion problem of the LOR3A to the SiO₂ surface and a halo will be visible around the pattern.

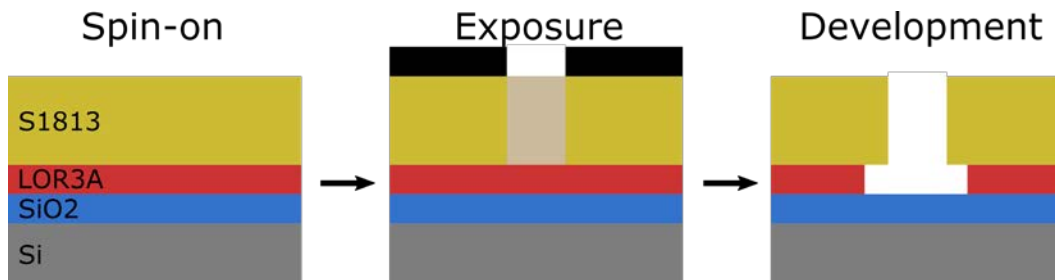


Figure 6: Illustration showing the spin-on of the Lift-off double structure consisting of LOR3A and S1813 photoresist and the subsequent exposure and development of BE pattern.

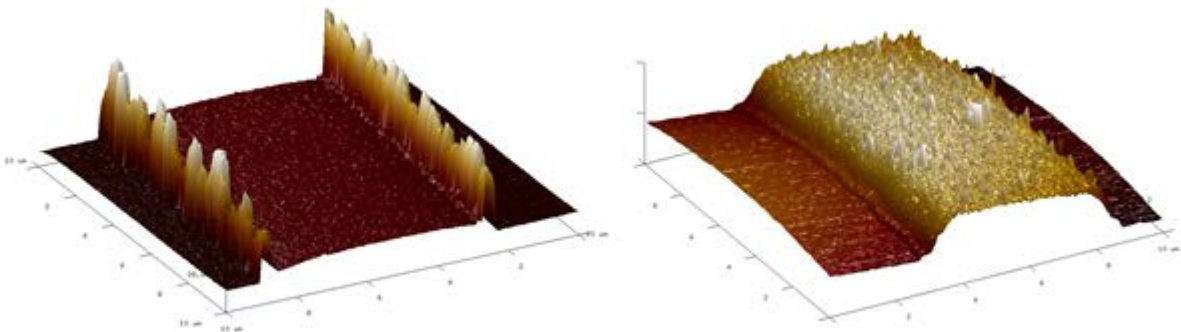


Figure 7: AFM images showing the unintentional formation of metal side wings (left) and a successful fabricated BE (right).

Following steps and parameter should be followed precisely to avoid the above discussed problems:

Use the mask “RRAM Main” without rotation

Dehydration bake on hotplate
150C for 5min

1. P-20 (HMDS)
Distribute on wafer
Wait 10s
Spin at 3000rpm (KBLOR3A recipe)
2. LOR3A (500nm)
Distribute on wafer
Spin at 3000rpm for 30s (KBLOR3A recipe)
Bake for 3min at 150C
3. S1813 (1.2um)
Distribute on wafer
Spin at 4000rpm for 60s (KBS1813 recipe)
Bake for 90s at 110C
4. Expose
minimum dose: 65mJ/cm²
2.2s recommended on OAI aligner
5. Developing and creation of the undercut
Use MIF300 for 30s
move the MIF300 by carefully moving the glassware
Bake for 60s at 110C
Use MIF300 for 60s

4.3.3 Deposition

Deposition of the BE occurs in two steps, first a wetting layer needs to be deposited on the SiO₂ surface of the silicon wafer. This enables a good adhesion of the inert metal which serves as the BE of our RRAM devices. In most cases titanium will be used as the wetting layer due to its oxygen active behavior forming strong bonds with the SiO₂ surface.

The following metals might also be used:

- Chromium
- Nickel
- Aluminum
- Hafnium
- Tantalum

The BE material should be inert to gain a stoichiometric switching layer (SL) at the BE interface. The following sample of inert metals are suited to fulfill this functionality:

- Tungsten
- Platinum
- Ruthenium
- Iridium

- Titanium nitride
- Tantalum nitride
- Osmium
- Rhodium
- Palladium
- Cobalt

The choice of the exact material depends strongly on the deposition capabilities, the desired roughness and in particular the mechanical and electronic interaction of the BE metal with the SL oxide. For HfO₂ a tungsten BE has been shown to be suitable and it will be used as an example material.

Following parameters are used for the deposition of Ti and W in the PVD75 tool from Kurt Lesker at CNSE:

- Titanium wetting layer
 - Titanium target in Source 1
 - Process time: 220s
 - Power: 100W DC
 - Pressure: 3mTorr
 - Gas flow: 100% Ar flow
 - Cleaning time: 300s
- Tungsten electrode
 - Tungsten target in Source 2
 - Process time: 750s
 - Power: 100W DC
 - Pressure: 3mTorr
 - Gas flow: 100% Ar flow
 - Cleaning time: 180s

4.3.4 Resist lift -off

A complete removal of all organic lithography components is necessary for further processing. In addition, the lift-off process should limit the re-deposition of the lifted of metal stack to prevent potential shortening and malfunction of the individual RRAM devices (Figure 8).

The proposed process removes the dual layer of S1813 and LOR3A in two steps.

1. Acetone bath of the wafer in a sonicating bath until the metal has been lifted of by dissolving S1813.
2. Flushing the wafer with 1165 resist remove out of bottle to progressively flushing redeposited metal particles.
3. Leave the wafer in a bath of 1165 for at least 3h
4. Clean the wafer with IPA

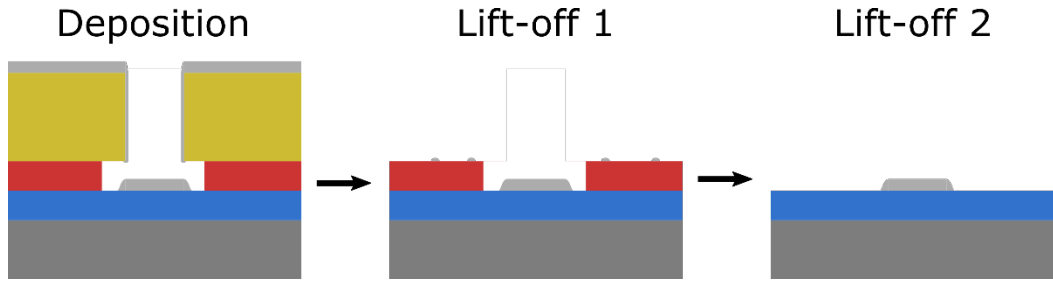


Figure 8: Illustration showing the deposition of the BE on top of a lift-off resist pattern and the subsequent removal via a dual lift-off process.

4.3.5 RRAM device stack and top electrode

Deposition

The deposition of the RRAM device stack on top of the BE requires three separate depositions. The first deposition is the switching layer (SL) typically being a transition metal oxide followed by an oxygen getter layer (OGL) and the top electrode. This process is developed to be only compatible only with a tungsten top electrode due to the necessity for a RIE step. The aimed thickness for the tungsten top electrode is 50 nm fabricated in the PVD75 sputter tool from Kurt Lesker at CNSE. But different deposition techniques could change this and might require an adjustment of the deposition and/or etch time to adjust for different material characteristics. In addition, the OGL layer should be capable of being etched by a combination of SF₆ and O₂. Typical SL compatible with this process are:

- HfO₂
- Ta₂O₅
- TiO₂
- ZrO₂
- La₂O₃

Typical OGL compatible with this process are:

- Ti
- Zr
- Ta
- La

Following parameters are used as an example deposition of HfO₂+Ti+W device in the PVD75 tool from Kurt Lesker at CNSE:

1. HfO₂ switching layer
 - Hafnium target in Source 3
 - Process time: 591s
 - Power: 125W RF
 - Pressure: 3mTorr
 - Gas flow: 70% Ar flow + 30% O₂ flow

- Cleaning time: 300s
- 2. Titanium oxygen getter layer
 - Titanium target in Source 1
 - Process time: 591s
 - Power: 100W DC
 - Pressure: 3mTorr
 - Gas flow: 100% Ar flow
 - Cleaning time: 300s
- 3. Tungsten electrode
 - Tungsten target in Source 2
 - Process time: 750s
 - Power: 100W DC
 - Pressure: 3mTorr
 - Gas flow: 100% Ar flow
 - Cleaning time: 180s

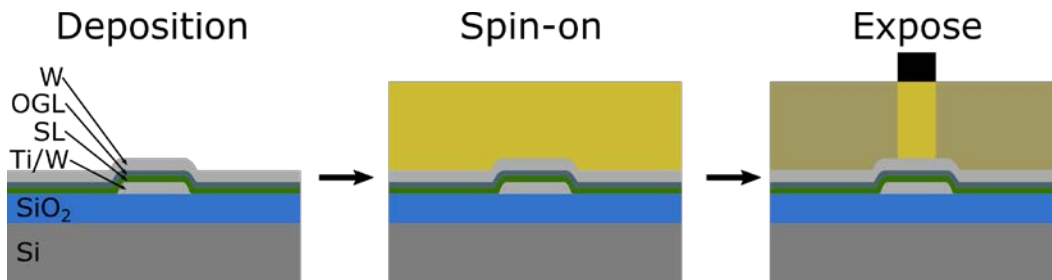


Figure 9: Illustration showing the uniform deposition of the switching layer (SL), oxygen getter layer (OGL) and inert top electrode on top of the patterned BE. S1813 photoresist is subsequently spun-on and exposed to device the RRAM stack.

Lithography

Particular attention has to be given to the RRAM device stack lithography process. To gain a vertical cut-off of the to-be etched tungsten TE the resist tapering angle needs to be as close to 0° as possible. A too large tapering angle would cause a re-deposition of the TE and OGL. This subsequently results in the malfunction of the RRAM devices.

Furthermore, the alignment of the mask has to be accurate within about 750 nm, otherwise the RRAM device stack moves too far to the edges of the BE where a good uniformity is not guaranteed. This would most certainly result in a change in the device performance. Typically characterized by a reduced forming voltage and most likely a reduced yield.

The following steps should be followed as closely as possible:

1. Use the mask “RRAM Via” without rotation
2. Dehydration bake on hotplate
150C for 5min

3. P-20 (HMDS)
Distribute on wafer
Wait 10s
Spin at 4000rpm for 40s (KBS1813 recipe)
4. S1813 (1.2um)
Distribute on wafer
Spin at 4000rpm for 60s (KBS1813 recipe)
Bake for 90s at 110C
5. Rehydrate the photoresist
put a wet towel on the 110C hotplate
put a small glass container on the wet towel
place the wafer for 120s on the glass container
6. Expose
minimum dose: 65mJ/cm²
1.9s recommended on OAI aligner
7. Developing
Use MIF300 for 12s
constantly move the MIF300 by carefully moving the glassware
check for successful development under the microscope

Reactive-ion etch

The RRAM device stack size will be defined by a reactive-ion etch (RIE) as shown in Figure 10. The major challenge of this step is to avoid a change in RRAM device performance due to the RIE. This change might arise as a result from a change in the surface morphology of the sidewalls or due to a re-deposition of tungsten and/or the OGL on a damaged SL. The recipe name in the Versalock PlasmaTherm tool at CNSE is: PM3_Cady_RRAM_W+Ti.

In detail the etch process follows following procedure:

1. Initialization (PM3_Cady_Init)
 - Process time: 30s
 - Pressure: 1mTorr
 - No gas flow
 - No Power
2. Gas stabilization (PM3_Cady_Sta_SF6+O2)
 - Process time: 30s
 - Pressure: 15mTorr
- Gas flow: 40sccm SF6 + 10sccm O2
 - No Power
3. Plasma ignition (PM3_Cady_Ign_SF6+O2)
 - Process time: 5s
 - Pressure: 15mTorr

- Gas flow: 40sccm SF6 + 10sccm O2
 - ICP Power: 500W
 - RIE Power: 50W
4. Etch (PM3_Cady_Etch_SF6+O2)
 - Process time: 50s
 - Pressure: 15mTorr
 - Gas flow: 40sccm SF6 + 10sccm O2
 - ICP Power: 500W
 - RIE Power: 100W
 5. Initialization (PM3_Cady_Init)
 - Process time: 30s
 - Pressure: 1mTorr
 - No gas flow
 - No Power
 6. Gas stabilization (PM3_Cady_Sta_Ar+SF6+O2)
 - Process time: 30s
 - Pressure: 5mTorr
 - Gas flow: 5sccm SF6 + 40sccm Ar + 5sccm O2
 - No Power
 7. Plasma ignition (PM3_Cady_Ign_Ar+SF6+O2)
 - Process time: 5s
 - Pressure: 5mTorr
 - Gas flow: 5sccm SF6 + 40sccm Ar + 5sccm O2
 - ICP Power: 500W
 - RIE Power: 50W
 8. Etch (PM3_Cady_Etch_Ar+SF6+O2)
 - Process time: 20s
 - Pressure: 5mTorr
 - Gas flow: 5sccm SF6 + 40sccm Ar + 5sccm O2
 - ICP Power: 500W
 - RIE Power: 100W
 9. Initialization (PM3_Cady_Init)
 - Process time: 30s
 - Pressure: 1mTorr
 - No gas flow
 - No Power

The etch recipe has following main parameter:

- TemperatureTemperatureSetpt: 30C
- TemperatureTemperatureSetpt: 20C
- HeliumCoolerPressureSetpoint: 3000mTorr

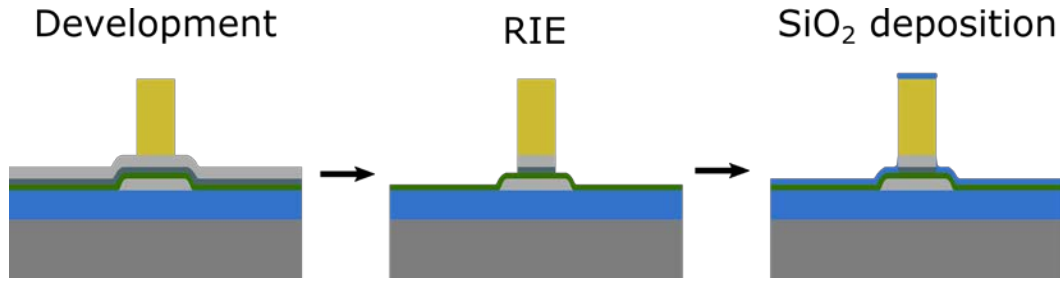


Figure 10: Illustration showing the development of the exposed photoresist layer and the following reactive-ion etch (RIE) and SiO₂ deposition.

An important aspect of this procedure is the vertical etch of the tungsten followed by switching over to a highly anisotropic ion mill process consisting mainly of an argon composing plasma cleans out the OGL and at least parts of the metallic acting sub-stoichiometric SL. This last ion mil step requires a more aggressive clean of the chamber after removing the sample to avoid cross contamination and a degradation of the plasma chamber performance. The carrier wafer needs to be back loaded to have a sufficient cooling of the chamber via the build in helium cooler.

The cleaning recipe name in the Versalock PlasmaTherm tool at CNSE is: PM3_Cady_Chamber_Clean. It comprises of following steps:

1. Pump down (PM3_Chamber_Clean_Pmpdwn_Ca)
 - Process time: 30s
 - Pressure: 1mTorr
 - No gas flow
 - No Power
2. Stabilization (PM3_Chamber_Clean_Sta_Sput)
 - Process time: 30s
 - Pressure: 50mTorr
 - Gas flow: 50sccm SF6 + 10sccm Ar + 20sccm O2
 - No Power
3. Plasma ignition (PM3_Chamber_Clean_Ign_Sput)
 - Process time: 5s
 - Pressure: 50mTorr
 - Gas flow: 50sccm SF6 + 10sccm Ar + 20sccm O2
 - ICP power: 1000W
 - RIE power: 50W
4. Sputter Clean (PM3_Chamber_Clean_sput)
 - Process time: 2400s
 - Pressure: 50mTorr
 - Gas flow: 50sccm SF6 + 10sccm Ar + 20sccm O2
 - ICP power: 1000W
 - RIE power: 0W

5. Stabilization (PM3_Chamber_Clean_Sta_O2)
 - Process time: 30s
 - Pressure: 50mTorr
 - Gas flow: 100sccm O2
 - No Power
6. Plasma ignition (PM3_Chamber_Clean_Ign_O2)
 - Process time: 5s
 - Pressure: 50mTorr
 - Gas flow: 100sccm O2
 - ICP power: 1000W
 - RIE power: 50W
7. Clean (PM3_Chamber_Clean_O2)
 - Process time: 3600s
 - Pressure: 50mTorr
 - Gas flow: 100sccm O2
 - ICP power: 1000W
 - RIE power: 0W
8. Pump down (PM3_Chamber_Clean_Pmpdwn_Ca)
 - Process time: 30s
 - Pressure: 1mTorr
 - No gas flow
 - No Power

The cleaning recipe has following constant parameter:

- TemperatureTemperatureSetpt: 30C
- TemperatureTemperatureSetpt: 20C
- HeliumCoolerPressureSetpoint: 3000mTorr

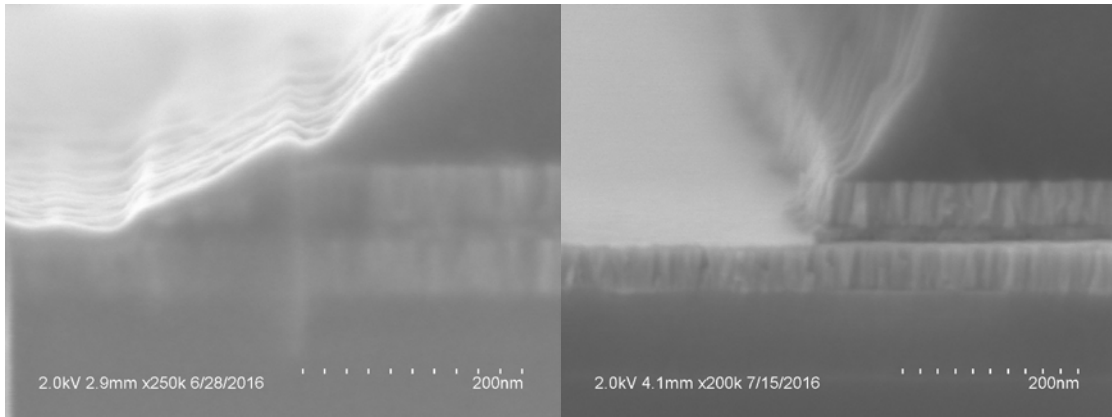


Figure 11: SEM images showing two different RIE approaches. The left image shows the use of a plasma based on CF_4+O_2 creating a large tapering angle of tungsten and re-depositing parts of it on the SL. The right image shows an almost vertical etch with a plasma based on SF_6+O_2 . In this approach the SF_6 based plasma etches tungsten faster than the photoresist not creating the contact area for sputtered re-deposition. A second plasma etch based on $\text{Ar}+\text{SF}_6+\text{O}_2$ removes the $\text{Ti}+\text{HfO}_2$ in an ion milling approach.

Insulator deposition

It is necessary to deposit an insulator in the field and in particular around the RRAM device stack to avoid shorting of the BE and TE. Figure 10 illustrates that the previous RRAM device stack resist from the RIE is used as a lift-off photoresist layer. Experimentally it was concluded that a 15nm co-sputtered SiO_2 layer is sufficient to get a leakage current below the detection limit of our system (around 10pA).

Following parameters are used for the deposition of SiO_2 in the PVD75 tool from Kurt Lesker at CNSE:

- Silicon target in Source 1
- Process time: 1400s
- Power: 150W RF
- Pressure: 3mTorr
- Gas flow: 55% Ar flow - 45% O_2 flow

Resist lift-off/strip

The lift-off of the SiO_2 insulator and strip of the remaining photoresist requires more effort as seen for the BE and TE photoresist stack. The photoresist got exposed a high implantation dose of S-F-O compounds as well as Ar during the RIE process. This implantation changes the structure of the resist, results in additional crosslinking and the creation of an extremely hard resist surface. In addition, the SiO_2 creates a thin layer around the resist further protecting it against a stripper.

The following three steps ensure the complete removal of all photoresist residuals from the wafer in a 1165 remover bath:

1. 1h sonicating with a medium to high sonicating power (4-7)
2. 2h bath at 70C on the hot-plate
3. Overnight bath at room temperature

Top interconnect

Lithography

A very similar Lift-off process is used for the top interconnect (TI) to pattern the second contact to the RRAM device (Figure 12). This step is less prone to a malfunction because it is the last structure and metal wings don't impact the functionality of the device. As for the BE a double structure consisting of LOR-3A and S1813 photoresist is used. For further information, please follow the description in section

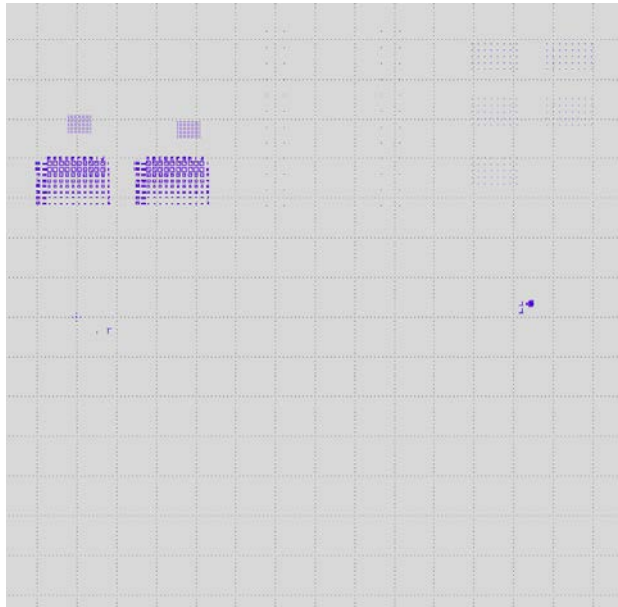


Figure 12: Layout of the mask 'RRAM Via' for the bottom electrode and the top interconnect.

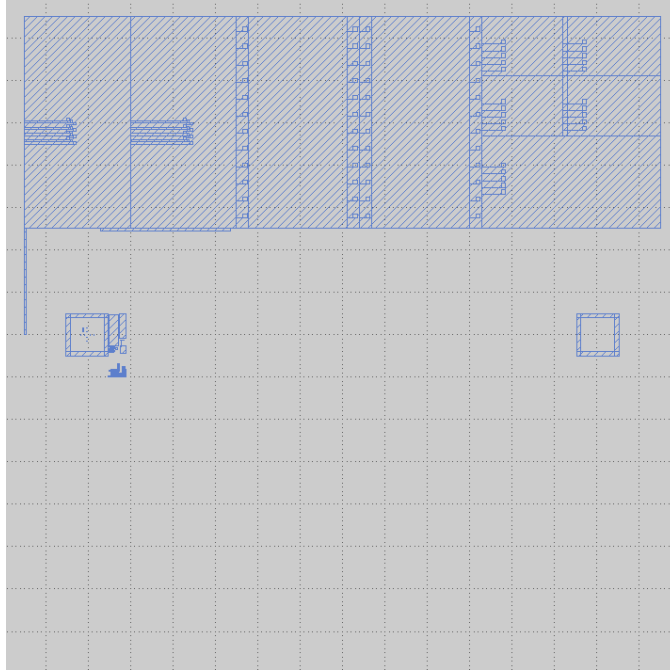


Figure 13: Layout of the mask 'BE contact' for the opening of the bottom contact.

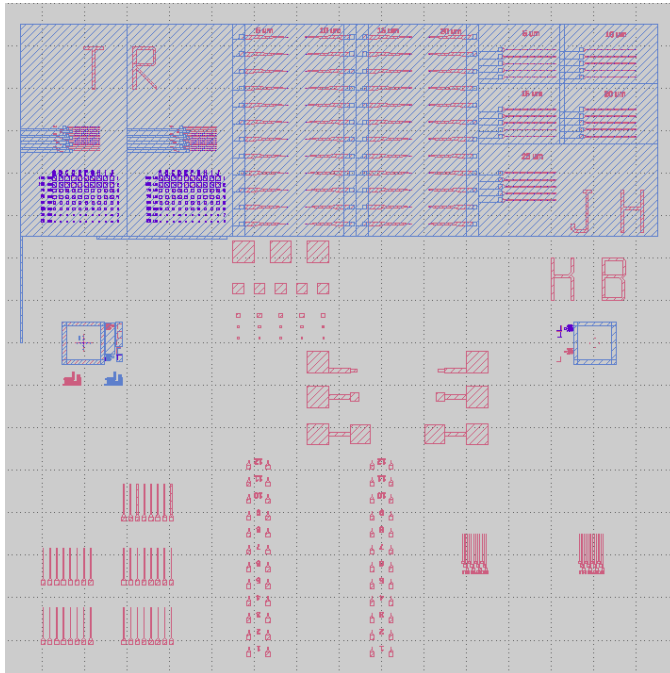


Figure 14: Combined Layout of the masks 'RRAM Main', 'RRAM Via' and 'BE contact'.

Bottom electrode and interconnect -
4.3.2 Lithography”.

The following steps and parameter should be followed:

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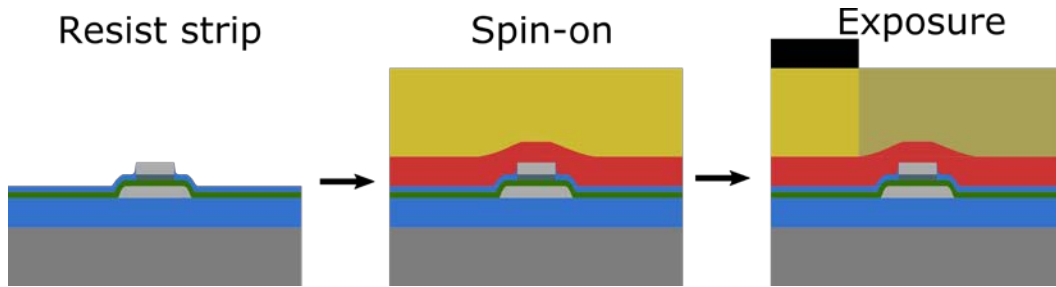


Figure 15: Illustration showing the photoresist removal after RIE and the SiO₂ deposition, the spin on of the double layer consisting of MIF300 and S1813 photoresist and the subsequent exposure to define the top interconnect pattern.

1. Use mask "RRAM Main" without a 180° rotation
2. Dehydration bake on hotplate
150C for 5min
3. P-20 (HMDS)
Distribute on wafer
Wait 10s
Spin at 3000rpm for 30s (KBLOR3A recipe)
4. LOR3A (500nm)
Distribute on wafer
Spin at 3000rpm for 30s (KBLOR3A recipe)
Bake for 3min at 150C
5. S1813 (1.2um)
Distribute on wafer
Spin at 4000rpm for 60s (KBS1813 recipe)
Bake for 90s at 110C
6. Expose
minimum dose: 65mJ/cm²
2.2s recommended on OAI aligner
7. Developing and creation of the undercut
Use MIF300 for 40s
Move the MIF300 by carefully moving the glassware

Deposition

Deposition of the TI occurs in two steps; first a wetting layer needs to be deposited on the SiO_2 surface of the silicon wafer as illustrated in Figure 13. This enables a good adhesion of the inert metal which serves as the BE of our RRAM devices. In most cases titanium will be used as the wetting layer due to its oxygen active behavior forming strong bonds with the SiO_2 surface. The preferred metal for the wetting layer and TI is Ti and W, respectively, but other metals might be used as described in the section

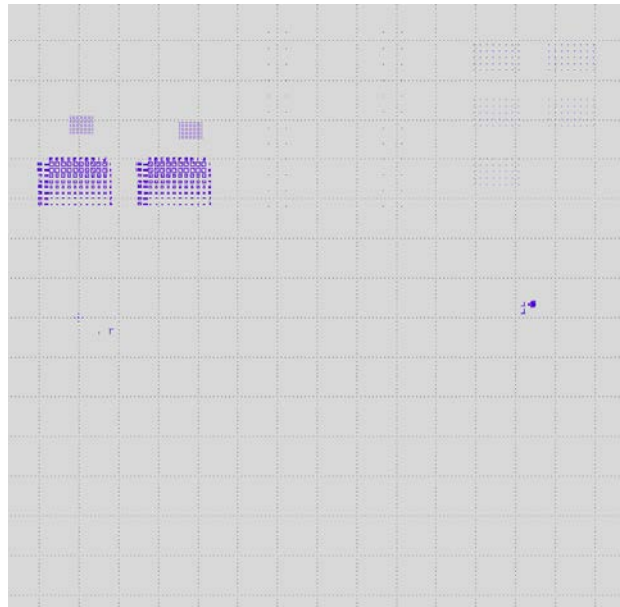


Figure 16: Layout of the mask 'RRAM Via' for the bottom electrode and the top interconnect.

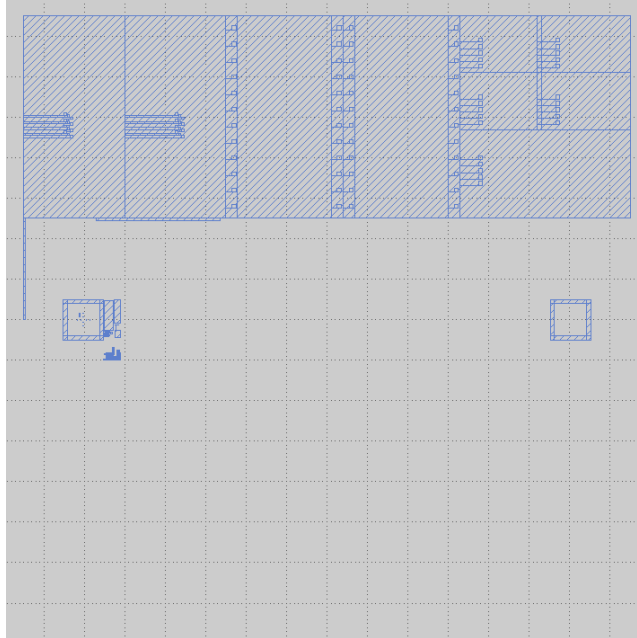


Figure 17: Layout of the mask 'BE contact' for the opening of the bottom contact.

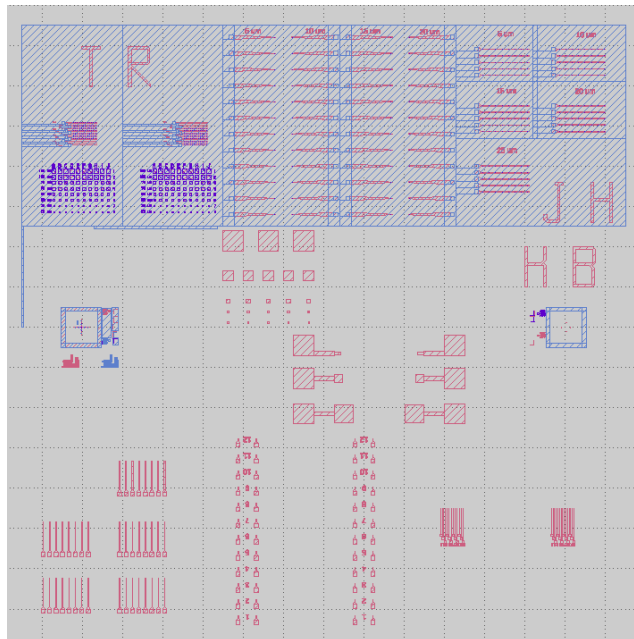


Figure 18: Combined Layout of the masks 'RRAM Main', 'RRAM Via' and 'BE contact'.

Bottom electrode and interconnect- 4.3.3 Deposition (page 8).

The TI should be stable in atmosphere and resistant against oxidation to allow a good contact with W probe tips.

Following parameters are used for the deposition of Ti and W in the PVD75 tool from Kurt Lesker at CNSE:

- Titanium wetting layer
 - Titanium target in Source 1
 - Process time: 220s
 - Power: 100W DC
 - Pressure: 3mTorr
 - Gas flow: 100% Ar flow
 - Cleaning time: 300s
- Tungsten interconnect
 - Tungsten target in Source 2
 - Process time: 750s
 - Power: 100W DC
 - Pressure: 3mTorr
 - Gas flow: 100% Ar flow
 - Cleaning time: 180s

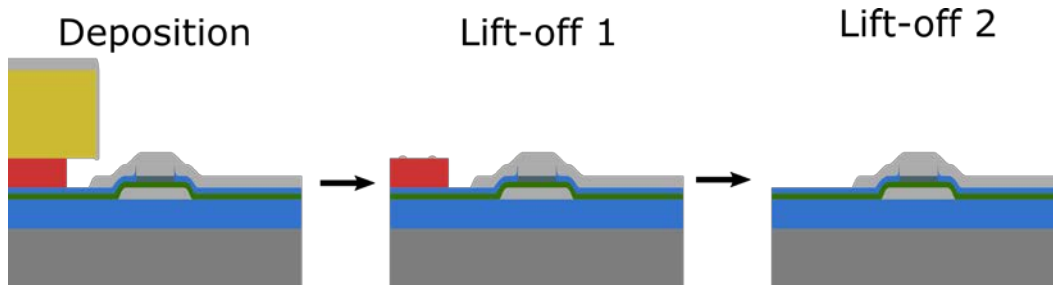


Figure 19: Illustration showing the deposition of the top contact onto the patterned photoresist structure. A dual lift-off of the S1813 photoresist and the LOR3A finishes the top electrode.

Resist lift-off

A complete removal of all organic lithography components is necessary for further processing. In addition, the lift-off process should limit the re-deposition of the lifted of metal stack to prevent potential shortening and malfunction of the individual RRAM devices (Figure 13).

The proposed process removes the dual layer of S1813 and LOR3A in two steps.

1. Acetone bath of the wafer in a sonicating bath until the metal has been lifted of by dissolving S1813.
2. Flushing the wafer with 1165 resist remove out of bottle to progressively flushing redeposited metal particles.
3. Leave the wafer in a bath of 1165 for at least 3h
4. Clean the wafer with IPA

4.3.6 Bottom electrode contact pad opening

Lithography

The final step opens the BE which is buried in a layer of HfO₂ and SiO₂. For this effort a simple photoresist process can be used. Due to the size of the pads (100x100μm²) the alignment is not as crucial as for the past three lithography steps and a time saving rough alignment is sufficient. Because of the use of a wet etch process the adhesion of the photoresist to the substrate plays an important role and attention should be paid to the second and third step.

1. Use the mask "BE contact" without rotation
2. Dehydration bake on hotplate
150C for 5min
3. P-20 (HMDS)
Distribute on wafer
Wait 10s
Spin at 4000rpm for 40s (KBS1813 recipe)
4. S1813 (1.2um)
Distribute on wafer
Spin at 4000rpm for 60s (KBS1813 recipe)
Bake for 90s at 110C
5. Expose
minimum dose: 65mJ/cm²
1.9s recommended on OAI aligner
6. Developing
Use MIF300 for 30s
Move the MIF300 by carefully moving the glassware
check for successful development under the microscope

Wet Etch

The wet etch utilizes a prepared etch solution from Transgene based on HF to remove the 15nm of SiO₂ and the residual HfO₂ layer. The etch solution is 'Improved Buffered HF' which is a mixture of H₂O, HF and NH₄F and designed to give etch 70nm/min of thermal oxide. In practice the rate will far exceed that value for co-sputtered SiO₂ but the value for HfO₂ is currently unknown. An etch time of 30s has been found to remove all oxide material and create a good contact to the bottom electrode.

Resist strip

To remove all residual resist in a timely fashion an approach based on the developer MIF300 is recommended.

Following steps should be followed to completely remove all photoresist from the wafer and in particular from the W TI.

- 10s flood exposure of both sides of the wafer
- 3min bath in in MIF300
- Clean with DI water

4.4 Device Characterization

For each wafer full of devices that was fabricated, initial electrical testing was performed at SUNY Poly, followed by shipping of wafers to AFRL for further testing. Current-voltage (I-V) sweep measurements were made to determine the forming voltage, set and reset voltages. An example of such data, obtained from hafnium oxide memristors are shown in Figure 14.

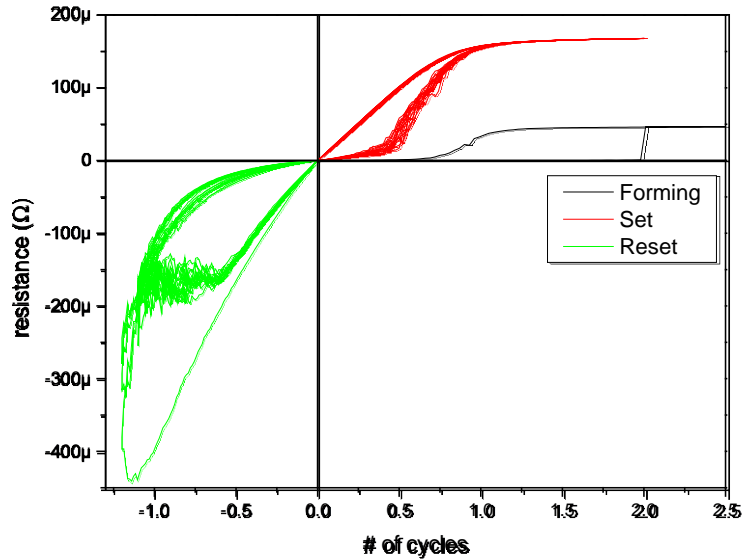


Figure 20. Current voltage plot for hafnium oxide electroforming (black line), and multiple set and reset cycles (red and green plots, respectively).

Devices were cycled for ~10-50 times to ensure reliability, as well as to characterize the average on and off state resistance values. Examples of these data are shown in Figure 15.

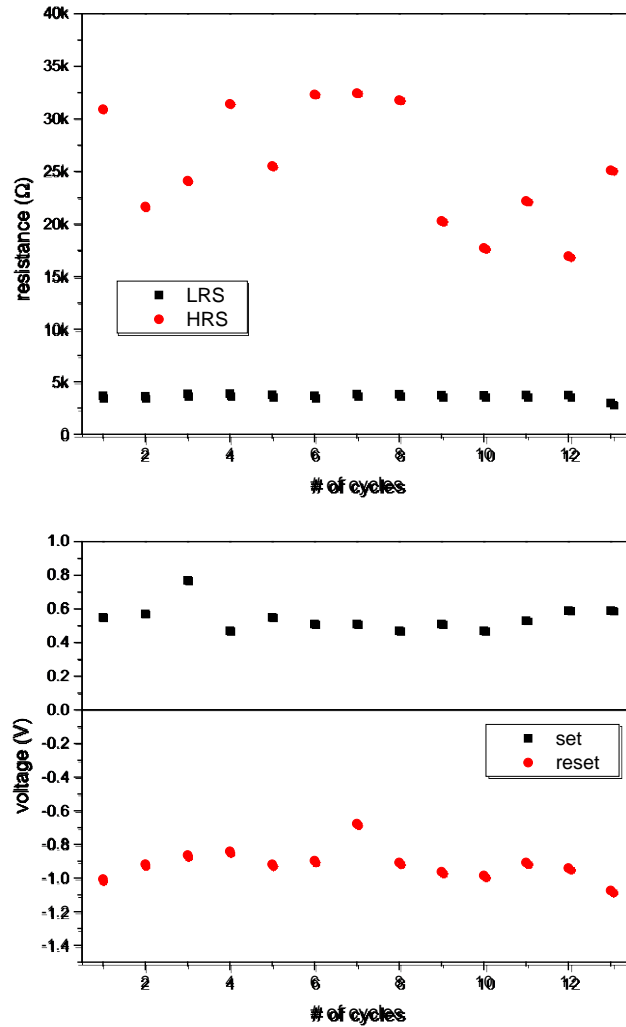


Figure 21. Resistance values for “on” (LRS) and “off” (HRS) states of a hafnium oxide devices (top graph) and corresponding set and reset voltages for the switching cycles (bottom graph).

4.5 Final Results

As a result of this work, multiple 100mm wafers containing memristor crossbar arrays were fabricated and delivered to AFRL for further testing. These included multiple wafers containing hafnium oxide devices, one wafer containing zirconium oxide devices, and multiple “die” (sub-sections of wafers) containing tantalum oxide devices. The SUNY Poly team was not responsible for subsequent testing at AFRL and thus has limited access to results from these follow-on experiments.

4.7 Presentations, Publications and Patent Applications Resulting from this Project

Peer-Reviewed Journal Articles

1. M. Uddin, M.B. Majumder, K. Beckmann*, H. Manem*, Z. Alamgir*, **N.C. Cady**, G.S. Rose. Exploring Best Region of Operation of a Memristive Crossbar Physical Unclonable Function. *Journal on Emerging Technologies in Computing Systems*. (2017) *Accepted – in press*.
2. Z. Alamgir*, K. Beckmann*, J. Holt*, **N.C. Cady**. Pulse width and height modulation for multi-level resistance in bi-layer TaOx based RRAM. *Applied Physics Letters*. (2017) 111: 063111 DOI: <http://dx.doi.org/10.1063/1.4993058>
3. J.S. Holt*, K. Beckmann*, Z. Alamgir*, J. Yang-Scharlotta, **N.C. Cady**. Effect of displacement damage on tantalum oxide resistive memory. (2017) *MRS Advances*. 1-7. DOI:10.1557/adv.2017.422
4. K. Beckmann*, H. Manem*, **N.C. Cady**. Performance enhancement of a time-delay PUF design by utilizing integrated nanoscale ReRAM devices. (2016) *IEEE Transactions on Emerging Topics in Computing – Special issue “Security of Beyond CMOS Devices: Issues and Opportunities*. DOI: 10.1109/TETC.2016.2575448
5. K. Beckmann*, J. Holt*, W. Olin-Ammentorp*, J. Van Nostrand, **N.C. Cady**. Impact of etch process on hafnium dioxide based nanoscale RRAM devices. (2016) *ECS Transactions*. 75(13): 93-99.
6. K. Beckmann*, J. Holt*, H. Manem*, J. Van Nostrand, **N.C. Cady**. Nanoscale hafnium oxide RRAM devices exhibit pulse dependent behavior and multi-level resistance capability. (2016) *MRS Advances*. 1(49): 3355-3360. DOI: <http://dx.doi.org/10.1557/adv.2016.377>

Peer-Reviewed Conference Proceedings Papers

1. S. Amer, S. Sayyaparaju, K. Beckmann*, **N.C. Cady**, G.S. Rose. A Practical Hafnium-Oxide Memristor Model Suitable for Circuit Design and Simulation. ISCAS: International Symposium on Circuits and Systems. May 2017, Baltimore, MD.
2. S. Amer, G.S. Rose, K. Beckmann*, **N.C. Cady**. Design Techniques for in-Field Memristor Forming Circuits. 60th IEEE International Midwest Symposium on Circuits and Systems. August 2017, Boston, MA.
3. M. Uddin, M.B. Majumder, G.S. Rose, K. Beckmann*, H. Manem*, Z. Alamgir*, **N.C. Cady**. Techniques for Improved Reliability in Memristive Crossbar PUF Circuits. 2016 IEEE Computer Society Annual Symposium on VLSI (ISVLSI), Pittsburgh, PA, pp. 212-217. doi: 10.1109/ISVLSI.2016.33

5. Conclusions

In conclusion, the SUNY Polytechnic team, led by Prof. Cady, developed a stable process flow for fabricating memristive crossbar arrays utilizing various switching oxides (hafnium oxide, tantalum oxide, and zirconium oxide). This process flow can be leveraged for fabrication of other types of memristors, and could pave the way for future device development efforts. In addition, the results of this project have been helpful for SUNY Poly's efforts to fabricate nanoscale memristive devices using their 300mm wafer fabrication line (for devices in the 100 x 100nm size regime).

6. List of Acronyms

RRAM:	Resistive random access memory (aka: memristor)
ReRAM:	Resistive random access memory (aka: memristor)
RMD:	Resistive memory device (aka: memristor)
TE:	Top electrode
BE:	Bottom electrode
HRS:	High resistance state
LRS:	Low resistance state
XPS:	X-ray photoelectron spectroscopy
XRD:	X-ray diffraction
TEM:	Transmission electron microscopy
SEM:	Scanning electron microscopy
AFM:	Atomic force microscopy