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DESIGNING AND CONFIGURING PROOF-OF-CONCEPT LPI RADAR RF FRONT END

by

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Various transceiver RF requirement analyses are performed including frequency selection, intermodulation products, minimum discernable signal, dynamic range, filter needs, noise figure, required signal-to-noise power ratio, transmitter and receiver gain analyses, and transmit power. Power, gain, and filter measurements through the receive chain were obtained to validate the RF receiver and transmitter front end designs. Results indicate that various RF requirements are met. Eventual miniaturization and integration of the whole RF transceiver into a single package are discussed.

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DESIGNING AND CONFIGURING PROOF-OF-CONCEPT LPI RADAR RF FRONT END

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LIST OF ACRONYMS AND ABBREVIATIONS

ADC	analog-to-digital converter
AWG	arbitrary waveform generator
BPF	band-pass filter
COTS	commercial off-the-shelf
CW	continuous wave
DC	direct current
DRFM	digital radio frequency memory
DSP	digital signal processor
EW	electronic warfare
IF	intermediate frequency
I/O	input and output
LNA	low noise amplifier
LO	local oscillator
LPF	low pass filter
LPI	low probability of intercept
MATLAB	matrix laboratory software
MDS	minimum detectable signal
NF	noise figure
P1dB	1-dB compression point
PCI	Peripheral Component Interconnect
V_{pp}	peak-to-peak voltage
PXIe	PCI eXtension for Instrumentation express
RBW	resolution bandwidth
RCS	radar cross section
RF	radio frequency
RSNS	robust symmetrical number system
SMA	subminiature version A
SNR	signal-to-noise ratio
VRT	VITA Radio Transport

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I. INTRODUCTION

A. BACKGROUND

As technology matures, single-function systems such as simple radar detection or analog voice-only communications systems give way to systems that support multiple functions such as enabling voice and video communications simultaneously or performing complex target detection, tracking, and identification. Such advances are not limited to the US military. Rapid development cycles in the global technology marketplace have allowed adversarial forces to obtain high-technology equipment for much less cost [1]. In order to win conflicts in such an environment, developing a multi-function system that can perform radar detection, conduct electronic warfare (EW) operations, and enable communications between troops and/or platforms is highly desirable [2].

In the naval context, a multi-function system can reduce ship building time and allows for more effective use of deck space because all the functions can be realized in a single structure. It potentially reduces maintenance and lifecycle cost since only one system is required to be installed or replaced [3].

In [4], the author mentions that multi-function maritime surface sensor systems are used to surveil targets on the surface of the sea. Such systems are able to pinpoint and track targets-of-interest on the surface autonomously; however, the adversaries can potentially know that their platforms are under surveillance if they are able to detect the sensors' transmission. An adversary can then take actions to mitigate such surveillance activities by maneuvering, performing electronic attacks on the friendly force surface sensors, or even launching weapons to destroy the sensors; therefore, the key requirement for such sensor systems are to transmit low probability of intercept (LPI) signals to make it difficult for the adversary to intercept the transmission [4].

It has been shown in [5] that military forces that are networked together to share information are more adaptive and are able to respond readily to the fast changing environment across different types of military operations. The report noted that although individual platforms are still important to achieve success in combat operations,

networking the diverse platforms and organizations together has improved the overall combat survivability and unit effectiveness in recent combat theatres of Afghanistan and Iraq. The report also highlighted that the key to networking is information sharing and communications [5]; therefore, incorporating communications capabilities in such sensor systems to share data is essential for modern warfighting.

In addition to being able to detect adversaries and communicate their locations to other friendly units, the authors in [2] believed that such systems should also possess EW capability to attack adversary sensors and communications systems autonomously. The insertion of complex algorithms into reprogrammable digital radio frequency memory (DRFM) to detect, classify intercepted signals, and generate countermeasures against such signals in real time is a requirement for the EW capability [2].

Integrating the three diverse functions of LPI radar, communications, and EW capability poses a major challenge. The integration of such multi-function system within a common mast presents even more challenges. Designing efficient antennas to provide the required gain and spatial coverage as well as ensure that there is sufficient radio frequency (RF) isolation between antennas in a confined space are competing requirements [2].

Based on thesis work in [6], a multi-function design incorporating the three diverse functions mentioned in the previous paragraph was proposed. The design is modular in nature and consists of an adaptive, power-managed robust symmetrical number system (RSNS) polyphase P4 continuous wave (CW) LPI radar, a short-range LPI communications system with the capability to transmit/receive off-board frequency assignments using the VITA Radio Transport (VRT) standard messaging protocol between ships and shore units, and a reconfigurable EW capability using a DRFM module [6]. In Figure 1, the conceptual positions of the transmit, receive, and auxiliary antennas used for the LPI radar and spiral antennas used for communications and EW is shown.

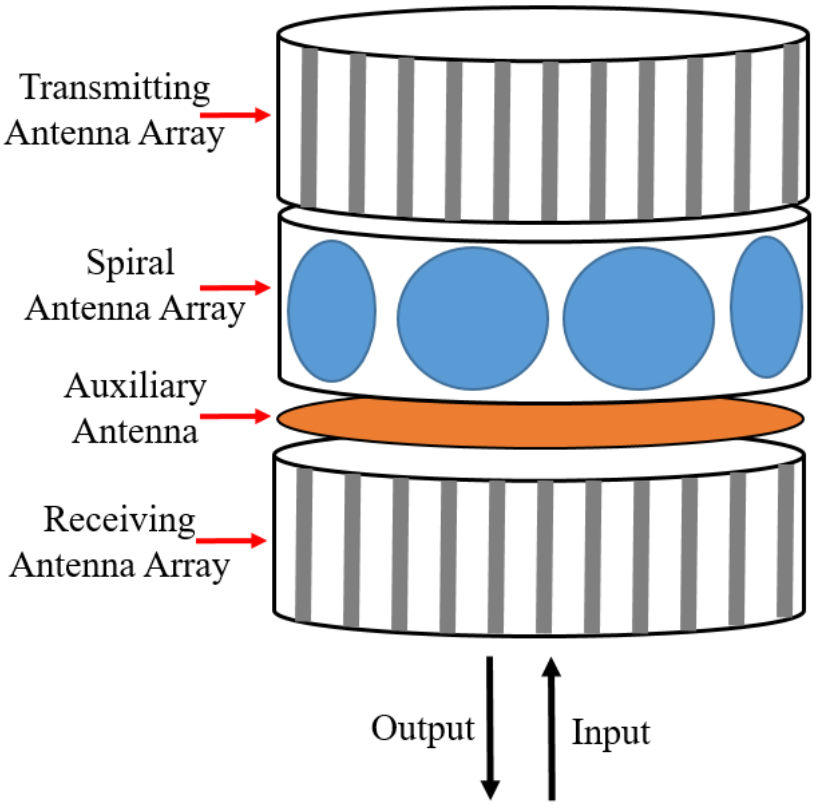

Figure 1. Multi-function Antenna Suite. Adapted from [2].

As described in [2], the LPI radar design utilizes a low-power, non-scanning, omnidirectional transmitting antenna that provides 360 degrees of continuous azimuth coverage. The receiver consists of a digital antenna providing 140 simultaneous overlapping beams over the same coverage area. In order to achieve enough isolation between the transmitting and receiving antennas, an auxiliary antenna is incorporated to provide a cancellation signal. The RSNS polyphase P4 CW enables unambiguous detection beyond a single-code period while minimizing the compression complexity. Other modulation formats such as noise modulation can also be used. Adaptive frequency selection and power management are used to improve the probability of detection. Special processing features such as unique moving target indicator phase detector, detection of targets just beyond the horizon using coherent mismatched RSNS-P4 correlation processor, Doppler filtering, and coherent post-detection integration are included. A greatest-of constant false alarm rate processor is used to improve detection performance in sea clutter [2].

As described in [2], the EW module contains a DRFM that can generate multiple false targets against high range-resolution profiling radars such as synthetic aperture radars and inverse synthetic aperture radars. The authors believe this capability can be used for suppression of enemy air defense or any operation involving high-range resolution imaging sensors since it does not require knowledge of the adversary sensors. The intercepted waveforms are sampled using a phase-sampling digitizer, and the phase values are stored in a parallel array of complex range bins. The phase values are rotated for constructing the Doppler frequency profile using a pipeline design. A set of multiplexers translates the binary in-phase components and quadrature components back and forth in order to implement the desired radar-cross section (RCS) profile. The authors pointed out that detection and classification of intercepted waveforms for autonomous electronic attacks on both the waveforms and frequencies can also be performed by the EW module [2].

Also described in [2] is the VITA 49 standard messaging protocol communications module. The communications module allows the system configuration to be broadcast to other users and allows for the external frequency assignments to be received. External frequency assignments can originate from J-6 (Joint Frequency Management Office) satellite entity that gathers the state-of-the-spectrum from a number of distributed, decentralized spectrum sensors and delivers frequency assignments to all tactical platforms [2].

The three capabilities are managed by a resource manager that operates in a priority interrupt manner to assign available resources to adapt to the different missions as highlighted in [2]. The resource manager also efficiently manages the usage of the EM spectrum based on information from the external frequency assignments and the on-board radar and communications frequency selection [2]. A block diagram of the envisaged design is shown in Figure 2.

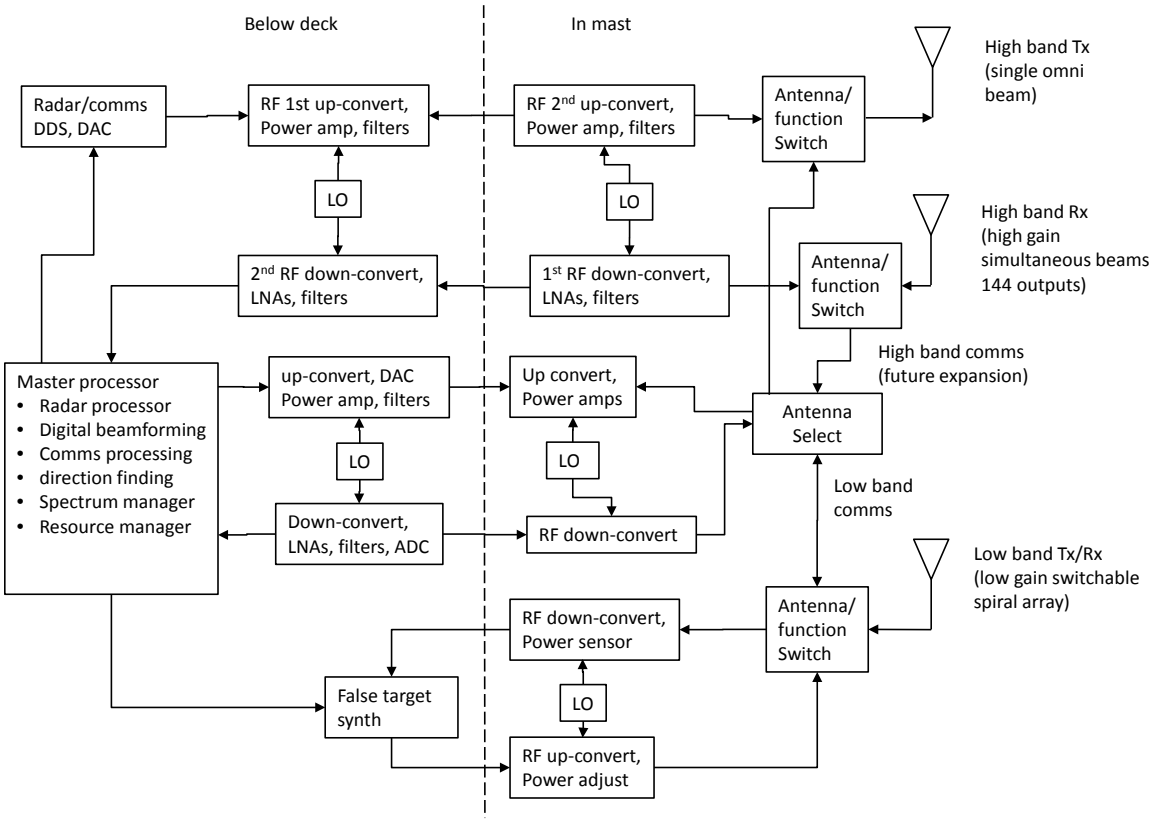

Figure 2. Block Diagram of RF Up-Conversion and Down-Conversion Subsystems. Source: [2].

The multi-function design simultaneously provides persistent LPI surveillance capability, allows real-time EM spectrum control using VITA communications module, provides the ability to detect, classifies intercepted waveforms, and performs electronic attacks on any adversary waveforms without prior knowledge using the EW capability [2].

B. OBJECTIVE

The objective of this thesis is to design and build a proof-of-concept RF-to-digital receiver chain using commercial off-the-shelf (COTS) modules and analyze the system performance and suggest improvements for subsequent custom hardware receiver implementation. Additionally, a transmitter chain design from digital to RF is also implemented.

C. THESIS OUTLINE

In Chapter II, a discussion of the RF front end design is presented. The purpose of this chapter is to provide a background of different types of RF front ends, their associated architecture, design considerations, and constraints. This background is essential for appreciating the design approach, tradeoffs, and constraints that follow. In Chapter III, the receiver architecture and the performance analysis for the LPI radar receiver are discussed. In Chapter IV, the design and performance analysis of the LPI radar's transmitter architecture are discussed. In Chapter V, the COTS prototype setup and measurements from the prototype validating the RF design from Chapters III and IV are presented. In Chapter VI, the conclusion of the thesis and recommendations for future work are presented.

II. RF FRONT END DESIGN REVIEW

A. INTRODUCTION TO RF FRONT END DESIGN

The RF front end is a crucial part for any wireless system such as radar, communications, or EW. According to [7], the RF front end includes the components that are between the antenna and the digital baseband portion. The RF front end consists of two parts: the receiver front end, whose primary job is to convert analog microwave signals to digital baseband signals for processing, and the transmitter front end, whose primary job is to convert digital baseband signals to analog microwave signals for transmission. The RF front end significantly determines the eventual system performance, physical size, and power usage [7].

B. RECEIVER REQUIREMENTS AND ARCHITECTURE

As discussed in [8] and [9], the receiver front end is responsible for extracting the desired signal from a wide spectrum of radio frequency sources and noise. A well-designed receiver must have enough gain, sensitivity, and dynamic range to detect and process the desired signals, yet have the right amount of selectivity and isolation to reject undesirable signals.

The typical signal power from a receive antenna is usually between –100 dBm to –120 dBm, but a typical analog-to-digital converter (ADC) accepts signals with a power level of around 0 dBm. In typical cases, this means that the receiver has to amplify the signal in excess of 100 dB. In order to prevent instabilities and oscillation that may occur as a result of so much gain, amplification of the signal is typically distributed to two or more frequency stages, with a limit of around 50 dB for any particular frequency stage. Amplifiers are generally costly at higher frequencies, so amplification is usually implemented at lower frequencies in order to keep cost to a manageable level [8].

The ability to detect very weak to very strong signals is an important requirement for a RF receiver [9]. The receiver must be able to maintain detection requirements when signal is weak, which can be several magnitudes lower than when the signal is strong. The range of amplitude or power in which the receiver can process the received signal without

degradation to the hardware or detection requirements is called the dynamic range of the receiver [9].

As explained in [8] and [9], selectivity is the ability to accept the desired signal with minimal loss while rejecting the undesired signals such as signals in adjacent frequency channels, image frequencies, unintentional, and intentional interference signals. While using a band-pass filter (BPF) at the RF stage of the receiver can provide selectivity, the narrow bandwidth and steep cutoff requirements of such filters are difficult to realize at RF [8]. It is easier to design a narrow bandwidth filter with steep cutoff requirements at an intermediate frequency (IF); thus, the down conversion from RF to IF is usually performed before the narrowband filtering stage in the receiver section [8], [9].

In the monostatic case, the RF transmitter and receiver are either on the same system or are very close to each other, with the antenna being typically shared between the transmitter and receiver. A RF transmitter is usually of very high power (> 0 dBm) for the transmission to be viable at medium to far ranges. The receiver, on the other hand, has to be sensitive to very low powered signals (< –80 dBm) due to the corresponding range loss. This means that there must be sufficient isolation between the transmitter and receiver in order for the transmitter to not overwhelm and saturate the receiver. For a full duplex communications system, it is common to use separate frequency bands for transmit and receive such that there is no overlap [8]. In a multi-function RF system where the radar, communications, and EW functions have overlapping frequency bands, physically separating the transmit and receive antennas is considered for isolation. The use of auxiliary antennas for coherent signal cancellation to ensure sufficient isolation between the transmitter and receiver is also considered [2]. For half-duplex communications system, the transmitter and receiver do not operate at the same time, thus preventing one from affecting the other. For RF systems which share the same antenna for transmit and receive, a duplexing filter or RF circulator provides isolation between the transmitter and receiver [8].

RF systems typically operate with carrier frequencies in the high megahertz to gigahertz ranges. There is a need to meet the Nyquist criterion, which states that the minimum sampling frequency must be at least twice the highest frequency of the signal to

properly reconstruct the received signal; therefore, in order to sample the received signal at the antenna itself, the minimum sampling frequency for a 10 GHz signal is at least 20 giga-samples per second. The resulting amount of sampled data is too large to be handled by present day's digital signal processor (DSP) in practical or size-constrained systems. In addition, an ADC must sample at such speed, with enough dynamic range, number of bits, and linearity. Such ADC is unfortunately not available with today's technology; therefore, received RF signals need to be down converted to lower frequencies in order to be digitized for signal processing [10].

Several down-conversion methods exist to convert signals from one frequency to another. These are discussed in the next four sections.

1. Homodyne Receiver

As discussed in [7], [8] and [10], a homodyne receiver, also known as zero-IF receiver, or direct conversion receiver, uses a single frequency conversion stage to down convert directly from RF to baseband signal before input to the ADC. A block diagram of a homodyne receiver is shown in Figure 3. The local oscillator (LO) circuit is tuned to the same frequency as the RF carrier. After mixing, the output signal frequency components are $\left(f_{RF} - f_0\right) = 0$ and $\left(f_{RF} + f_0\right) = 2f_{RF}$ since $f_0 = f_{RF}$. A low pass filter (LPF) is responsible for removing the $2f_{RF}$ frequency component. The RF amplifier is used to amplify the low power received signal to ensure that the desired signal is large enough to be processed by the mixer since the loss in the mixer can be relatively large. The baseband amplifier is used to ensure that the baseband signal is large enough to be sampled by the ADC [7], [8], [10].

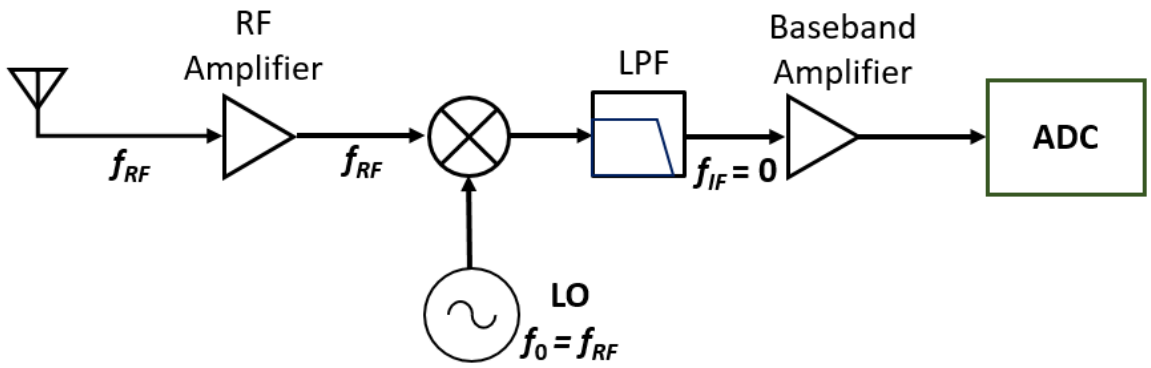

Figure 3. Block Diagram of Homodyne Receiver. Adapted from [8].

The frequency spectrum of an arbitrary desired signal before and after down-conversion is shown in Figure 4. The desired signal is imposed on the RF carrier f_0. After mixing with the LO at the same frequency, only the desired baseband signal is present [10].

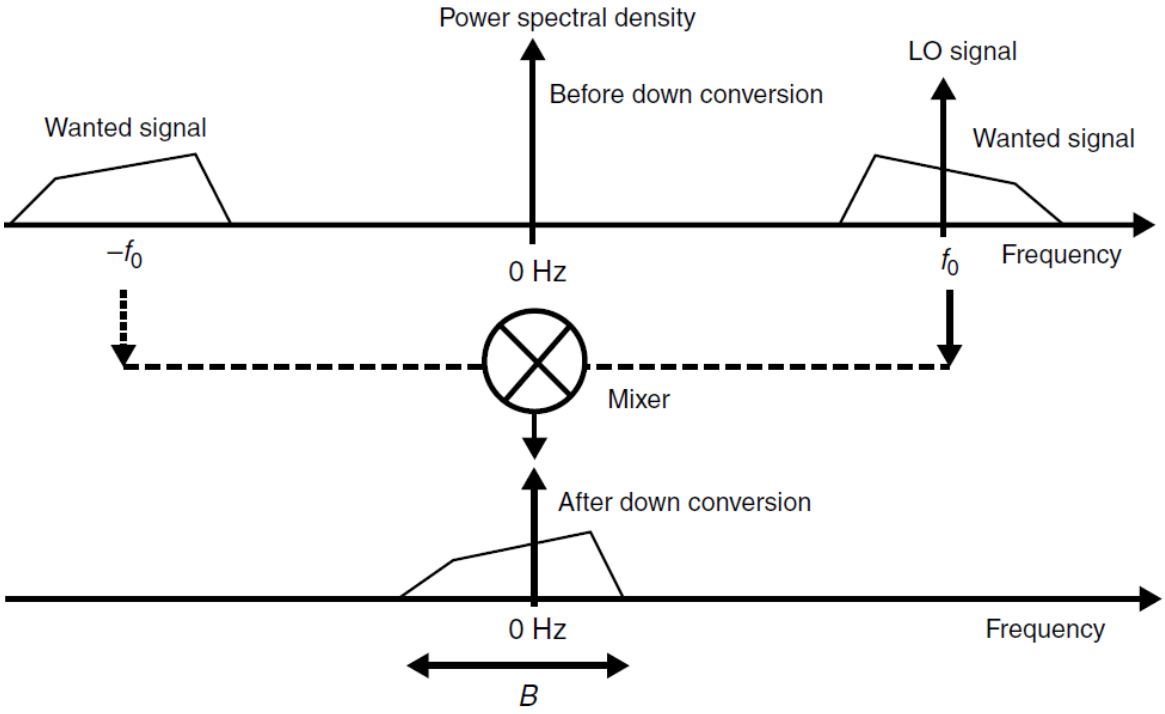

Figure 4. Direct Down-Conversion Technique. Source: [10].

a. Advantages of Homodyne Receiver

The advantages of homodyne receiver architecture are the absence of image frequency problems, a reduction in component count, and the ease of designing receivers with multi-mode capability [8], [10].

Since the LO frequency is the same as the RF carrier, the difference between the LO frequency and RF carrier is zero. The resulting higher frequency term $2f_{RF}$ is easily removed by the LPF, and there is no need for image frequency filtering. Single stage mixing also reduces component count since there are no intermediate mixing stages; therefore, overall power consumption, physical size, and cost are reduced. As the mixing removes the carrier frequency, the LPF operates at baseband and can be integrated onto a digital chip instead of as an analog device. This allows different filtering bandwidths to be incorporated onto a digital chip instead of requiring discrete filter components, which allows multi-mode receivers to be designed easily [8], [10].

b. Disadvantages of Homodyne Receiver

The disadvantages of homodyne receiver architecture are the high LO leakage, self-reception, direct current (DC) offset problems, and flicker noise interference [8], [10].

LO leakage occurs because the LO frequency is exactly the same as the desired input carrier frequency, which falls within the passband of the receiver. A mixer will never have enough isolation to prevent the LO signal from making its way back towards the RF amplifier and be radiated from the antenna. This creates interference to other devices operating in the same frequency band. This leakage also causes self-reception where the radiated signal is received by the antenna. The resultant signal is down-converted into a DC signal and can overwhelm the ADC. If the receiver is moving, the Doppler effect modulates the received signal and results in a DC offset which causes saturation in the active components of the receiver and reduces the dynamic range of the ADC. Flicker noise is also an issue because the down-converted signal is located around zero frequency. Digital devices have high noise levels around zero frequency, and this results in decreased sensitivity in the receiver [8], [10].

2. Heterodyne and Super-Heterodyne Receiver

As explained in [7], [8] and [10], a heterodyne receiver can consist of a single stage or multiple stages of down-conversion from desired RF to one or more intermediate frequencies before input to the ADC. A super-heterodyne receiver simply refers to the receiver utilizing only the lower sideband of the difference between the two frequencies. A block diagram of a single conversion super-heterodyne receiver is shown in Figure 5. The super-heterodyne receiver architecture is the most popular type of architecture in use today [7], [8], [10].

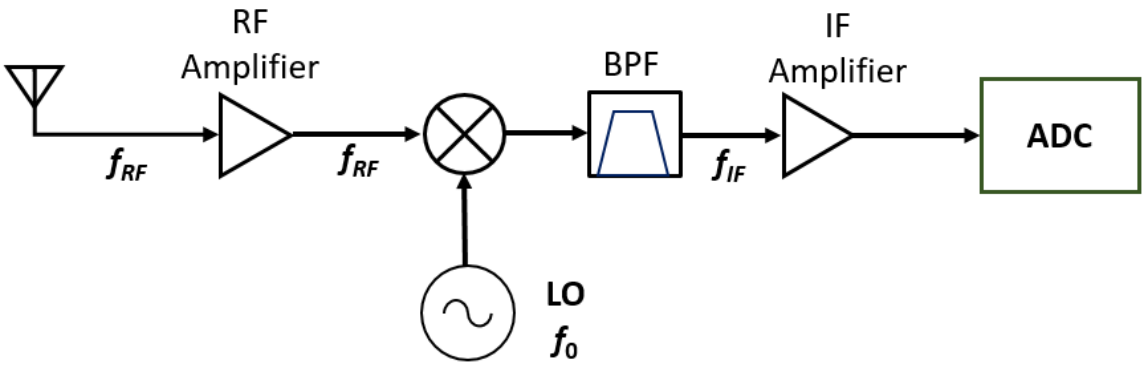

Figure 5. Block Diagram of Single-Conversion Super-Heterodyne Receiver. Adapted from [8].

a. Advantages of Heterodyne Receiver

The advantages of heterodyne receiver architecture are high selectivity and sensitivity [8], [10].

The receiver is able to achieve high selectivity and sensitivity because it performs most of its amplification at the intermediate frequency. It is easier to design high quality factor filters and higher gain amplifiers at the intermediate frequencies as compared to at RF [8], [10].

b. Disadvantages of Heterodyne Receiver

The disadvantages of a heterodyne receiver architecture are image frequency problems and high component count.

The IF frequency can be obtained by mixing the RF frequency with the LO frequency during the down-conversion process. During down-conversion, two frequencies or frequency bands that are of concern are the signal frequency and the so-called image frequency. If an unwanted signal is on the image frequency, it is mixed down in the receiver and causes interference with the desired signal, causing corruption and possibly swamping out the desired signal. This can be mitigated by the inclusion of image rejection filters and additional mixing stages to remove the image frequency components [8], [10].

The need to reject the image frequency as a by-product of mixing results in additional filters and mixing stages. This adds to the component count, which may result in an increase in cost and physical size of the receiver [8], [10].

3. Low-IF Receiver

The low-IF receiver combines the super-heterodyne architecture performance with the simplicity and cost effectiveness of the homodyne architecture. Instead of down-converting the RF signal directly to baseband (homodyne receiver architecture), the low-IF receiver architecture down-converts the desired RF signal to a frequency that is several hundreds of kilohertz or megahertz above the baseband. The signal is then filtered and amplified before being sampled by the ADC [10].

a. Advantages of Low-IF Receiver

Since the filtering and amplification of the RF signal in the low-IF architecture is performed at a lower frequency as compared to the super-heterodyne architecture, this reduces the cost, component count, and power consumption. Also, it is easier to integrate the low frequency components such as filters and amplifiers on a single chip. Issues related to DC offset in the homodyne architecture are no longer present since the signal is carried by a low frequency carrier and not at the DC level. There is also no image frequency problem and less flicker noise as compared with a homodyne architecture [10].

b. Disadvantages of Low-IF Receiver

Low-IF receiver architecture requires better ADC performance compared to homodyne architecture because the signal is not at baseband. A polyphase BPF is required to remove mirror frequency and to prevent aliasing, which results in higher processing power requirements and higher component count compared to the homodyne architecture using a LPF [10].

4. Wideband-IF Receiver

The wideband-IF receiver architecture takes all desired RF frequencies and performs the first stage down-conversion from RF into IF using a mixer with a fixed frequency LO. A LPF is then used to remove intermodulation frequency components before the IF signals are passed to the second stage mixers. The second stage mixer requires a tunable LO to down-convert the previous IF into baseband. Unlike a conventional two-stage super-heterodyne receiver, the first LO frequency down-converts all the desired RF frequencies using a fixed LO frequency, which results in a wide bandwidth at IF. The selection of the desired signal is performed using the second LO, which is lower in frequency. As the selection of the desired signal is implemented at low IF instead of at RF, the requirements for the second stage tunable LO and filters are less stringent and better performance can be achieved [10].

a. Advantages of Wideband-IF Receiver

Since the tuning of the desired frequency channel is performed at the second mixer or IF stage, the first stage down-conversion LO is at fixed frequency and is cheaper to implement. Operating at a lower frequency also results in lower power consumption, less phase noise, and simplified circuitry. There is also less of an issue of having in-band interference caused by LO leakage as compared to homodyne architecture where the LO is the same as the desired RF signal carrier [10].

b. Disadvantages of Wideband-IF Receiver

The requirement for additional mixing stages results in increased complexity of the circuitry, more components, and higher power consumption. There is also a need for better ADC dynamic range due to limited filtering as compared to the heterodyne receiver [10].

C. FREQUENCY CONVERSION AND FILTERING

1. Selection of IF

As described in [8], the selection of the IF is an important part of the design of a super-heterodyne receiver. The relationship between RF, IF, and LO frequencies is described by

$$f_{IF} = \left| f_{RF} - f_0 \right| \tag{1}$$

where f_{IF} is the IF, f_{RF} is the RF center frequency of the transmitter, and f_0 is the LO frequency [8].

The mixing product consists of an upper sideband and a lower sideband signal. For receivers designed to use lower sideband signal, the LO frequency is computed as

$$f_0 = f_{RF} - f_{IF} \ . \tag{2}$$

Frequencies are assumed to be always positive assuming a real signal model at RF. In other words, the symmetrical property of the magnitude spectrum allows for just the use of positive frequencies in terms of frequency selection analysis. For receivers using lower sideband signal, the mixer responds to a RF image frequency described as

$$f_{IM} = f_{RF} - 2 f_{IF} \tag{3}$$

where f_{IM} is the image frequency [8].

The image frequency signal can be easily removed by filtering if the IF selected is high enough for the image to be separated sufficiently so that the cutoff requirement of the filter is not that stringent; however, the IF should not be so high as to approach the ADC's maximum allowed sampling rate. A rule of thumb is for the IF to be no higher than 200 MHz for current generation ADCs [8].

2. Intermodulation Product

The mixer is a non-linear device, and its function is to produce intermediate frequencies from the sum and difference of the input signal and the LO. Due to non-linearity, it also produces harmonics of the input frequencies that are multiples of the input frequencies and the LO. The intermodulation product frequency can be calculated using

$$f_{mn} = \left| mf_{RF} - nf_0 \right| \tag{4}$$

where f_{mn} is the intermodulation product frequency, and *m* and *n* are positive integers [7], [8].

It is important for the LO frequency to be selected with care to ensure that the intermodulation products and harmonics from the mixing stage are as far away as possible from the passband of the desired signal so they can be successfully filtered out in order to prevent interference [7].

3. Filter Selection

Many frequency components are generated after the mixing stage. Only one of the frequency components contains the desired signal. The others are unwanted byproducts of the mixing and are sometimes referred to as “spurious signals”. These spurious signals must be removed to prevent them from corrupting the desired signal. This can be achieved by using a BPF with the required roll-off and attenuation in the stop bands to remove the unwanted signals. The BPF must also have a pass band which has minimal insertion loss and enough bandwidth for the desired signal to pass through [7].

D. DYNAMIC RANGE

1. Minimum Detectable Signal

The minimum detectable signal (MDS) of a receiver is defined as the minimum signal that is required to be present at the receive antenna in order to achieve a desired signal-to-noise ratio (SNR) [7].

2. Noise Figure

The noise figure (NF) of a receiver is defined as

$$F = \frac{\left(\frac{S_i}{N_i}\right)}{\left(\frac{S_o}{N_o}\right)} \tag{5}$$

where S_i is the signal power at the input of the receiver, N_i is the noise power at the input of the receiver, S_o is the signal power at the output of the receiver, and N_o is the noise power at the output of the receiver using the standard temperature of $T_0 = 290$ K [11].

The noise figure of the receiver refers to the degradation of SNR as the signal passes through the receiver chain. The noise figure of a multi-stage system can be calculated if the individual noise figure and gain of each component are known. The overall noise figure of the system can be calculated using

$$F_{system} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \ldots + \frac{F_n - 1}{G_1 G_2 \ldots G_{n-1}} \tag{6}$$

where F_{system} is the overall noise figure of the system, F_1 is the first component noise figure, G_1 is the first component gain, F_2 is the second component noise figure, G_2 is the second component gain, F_n is the *n*-th component noise figure, and G_n is the *n*-th component gain [11].

We see from Eq. (6) that the noise figure of a multi-stage system is highly dependent on the first stage gain and noise figure. If the gain of the first stage is large and its noise figure is low, subsequent stage contribution to the overall noise figure of the system may not be significant. The addition of a pre-amplifier or low noise amplifier (LNA) as close to the antenna as possible improves the overall noise figure significantly [11].

3. P1dB Compression and P3 Intercept Point

The 1-dB compression point (P1dB) is one of the quantifying metrics for active devices such as amplifiers and mixers. It is defined as the point where the output power is decreased by 1 dB from its ideal characteristic curve. This means that the active device no longer operates in its linear region and starts to saturate. An active device that operates in saturation results in clipped off signals and generates harmonic distortion. Amplifiers indicate the P1dB point as its output power, while mixers indicate the P1dB point as its input power [8].

The P3 intercept point, or third-order intercept point, is the intersection point of the first-order product and third-order product power when they are equal. The P1dB compression point and the P3 intercept point are illustrated in Figure 6 [8].

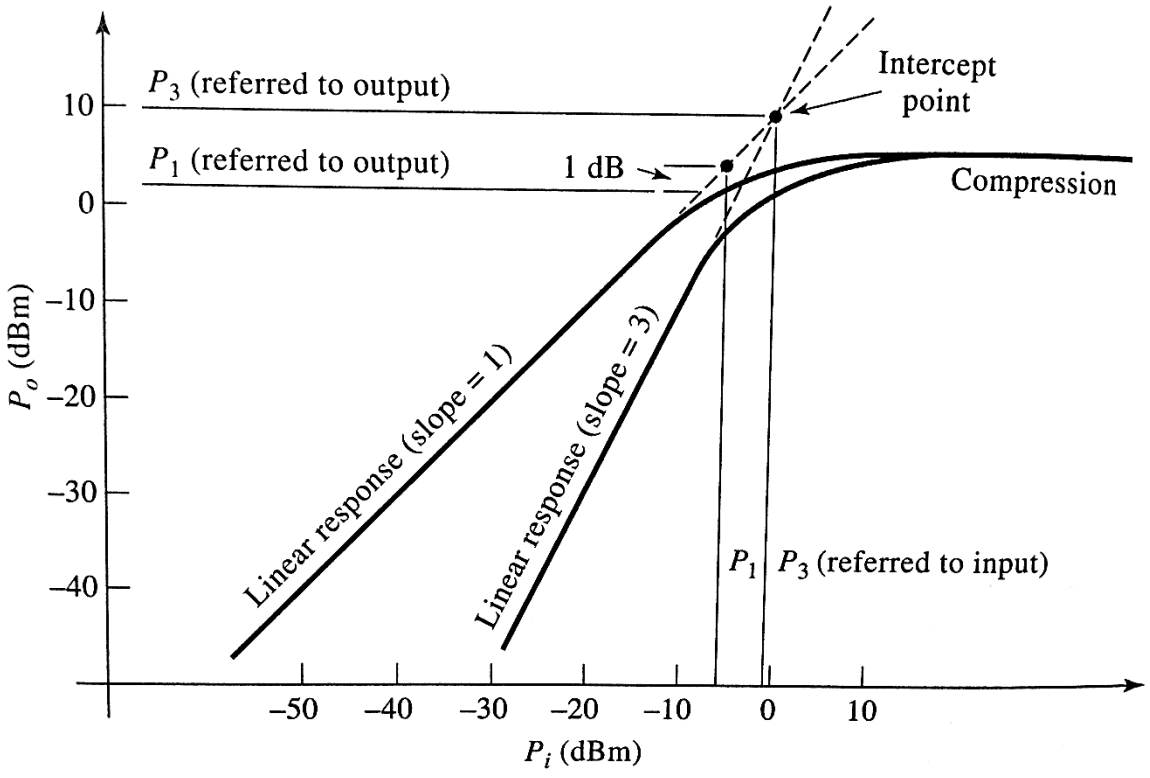

Figure 6. P1dB Compression and P3 Intercept Point. Source: [8].

Power levels exceeding the P3 intercept point of the component result in intermodulation distortions occurring at the output; therefore, it is important to ensure that the P1dB compression points and P3 intercept points at every stage in the receiver are not exceeded [8].

4. ADC Dynamic Range and Sampling Frequency

The ADC is responsible for converting the desired analog signal from the RF front end to digital format. This is achieved through sampling. The range of signal amplitude the ADC is able to sample without distortion is called the ADC's dynamic range. If the signal is too large, the ADC input gets saturated and damage might occur. If the signal is too small, the signal falls below the quantization noise of the ADC which results in reduction of SNR. The receiver must be designed to condition the input signal so that it falls within the dynamic range of the ADC [7].

Another requirement for the ADC is to ensure that enough information from the desired input analog signal is captured. This is dictated by the chosen IF or effective bandwidth of the signal relative to the chosen sampling frequency. Obviously, the sampling frequency is chosen to be higher than the IF Nyquist frequency, which is clearly twice that of the IF [7]. In our design, we intend to use the largest possible sampling frequency dictated by the chosen ADC.

E. TRANSMITTER ARCHITECTURE

The transmitter front end is responsible for converting the digital baseband signal to RF signals for transmission over the air. It has to produce stable carrier frequencies for signal modulation, provide sufficient output power for the transmission to achieve the desired distance, and suppress spurious signals such as harmonics and intermodulation products that might come from the frequency up-conversion process [9].

F. CHAPTER SUMMARY

In this chapter, a review of the RF front end design was presented. A brief background of different types of RF receiver architecture, their advantages, and disadvantages were presented. Frequency conversion, filtering, and receiver dynamic range

were also discussed. Transmitter architecture design considerations and constraints were also reviewed.

III. RECEIVER ARCHITECTURE AND ANALYSIS

A. OVERVIEW OF RECEIVER ARCHITECTURE

The proposed architecture for the multi-function, multi-mission LPI compact mast sensor is shown in Figure 7. The sensor performs three functions: LPI radar, communications, and EW. The RF front end consists of the receiver chain and the transmitter chain. The focus of this thesis is to implement the RF front end design which is illustrated in the dotted red box in Figure 7. In order to ensure the design is technically feasible, a proof-of-concept implementation is constructed and its performance analyzed using COTS modules such as those shown in Figure 8. Once proven that the COTS design can perform the desired functions required for the RF front end, a custom hardware design for performance and miniaturization is proposed for implementation.

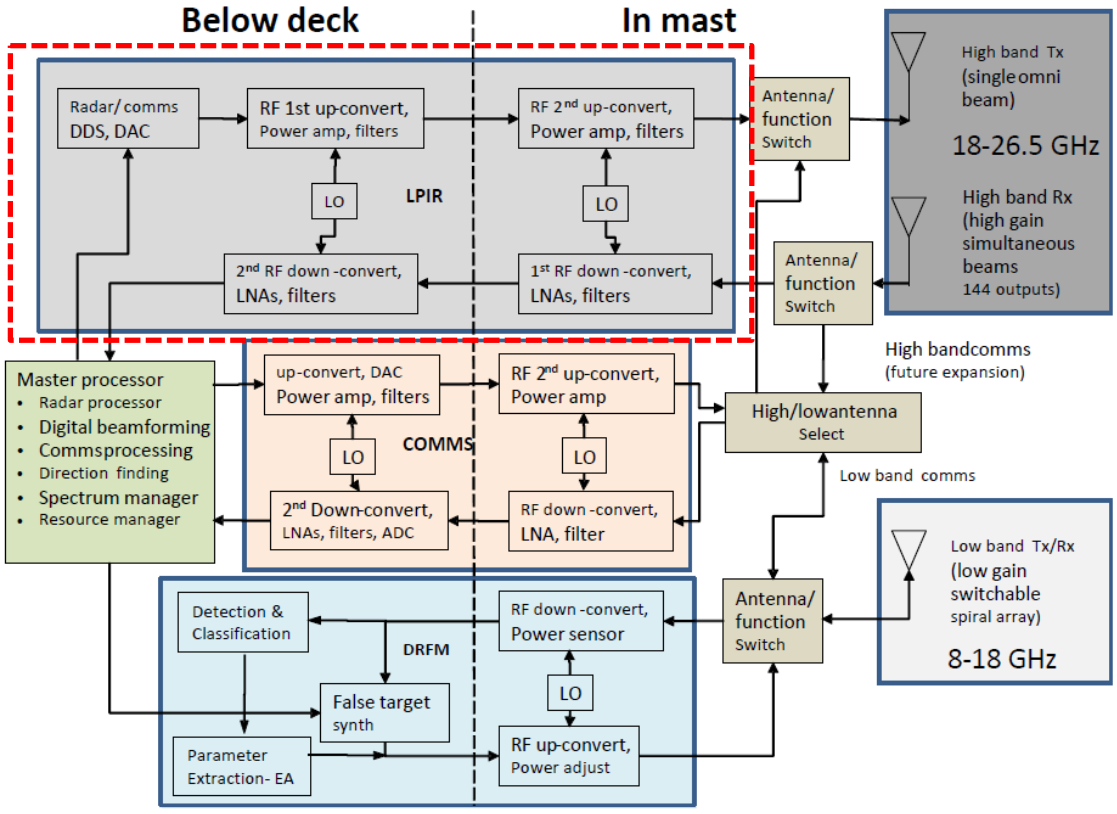

Figure 7. Proposed Architecture for Multi-function LPI Sensor Prototype. Adapted from [2].

Figure 8. COTS Modules for use in Proof-of-Concept Hardware Realization. Adapted from [12]–[18].

B. RECEIVER ARCHITECTURE DESIGN USING COTS MODULES

Three requirements need to be analyzed prior to RF implementation of the receiver. They are ADC dynamic range, MDS, and IF selection. A diagram illustrating information required for detailed receiver design is shown in Figure 9.

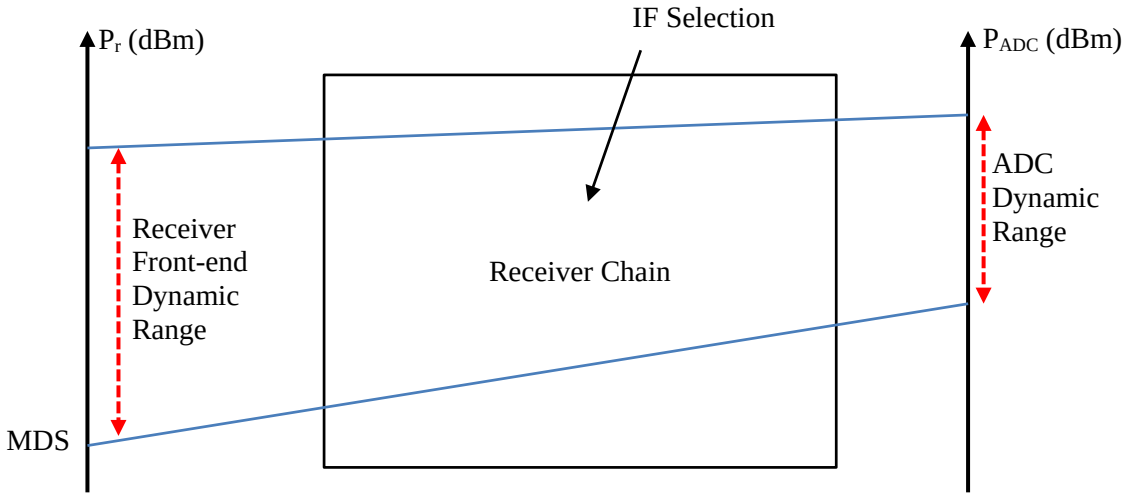

Figure 9. Information Required for Detailed Receiver Design

1. M3302A Digitizer Dynamic Range

One of the most important parts of the receiver design is to condition the received signal so that it falls within the dynamic range of the ADC or digitizer. If the signal power falls below the dynamic range of the ADC, SNR degradation occurs. If the signal power lies above the range, it may cause damage to the ADC. The Keysight M3302A digitizer module is selected for the proof-of-concept design. The input and output (I/O) specifications are shown in Table 1.

Table 1. M3302A Digitizer Parameters. Adapted from [12].

M3302A digitizer parameters	Value
Input frequency	0 to 200 MHz
Sampling rate	500 MSa/s
Input voltage range (50Ω)	125 mV_{pp} to 8 V_{pp}

One of our design goals is to fully utilize the dynamic range of the ADC. We desire the input signal to be as large as possible; however, it should not be larger than the maximum peak-to-peak input voltage (V_{pp}) of 8.0 V_{pp}, otherwise saturation occurs. A useful engineering rule-of-thumb is 3.0 dB below the maximum input voltage.

It is typical to calculate RF signal parameters in terms of power. The maximum allowable signal power level to the ADC is defined by

$$P = \frac{V_p^2}{R} \tag{7}$$

where P is the power level, V_p refers to the peak voltage, and R refers to the resistance across the load; thus, the maximum allowable signal power level to the M3302A Digitizer is

$$P = \frac{V_p^2}{R} = \frac{4^2}{50} = 0.32 \text{ W}. \tag{8}$$

Converting Eq. (8) into dBm (dB relative to a milliwatt), we obtain

$$P_{dBm} = 10\log\left(\frac{0.32}{0.001}\right) = 25.05 \text{ dBm}. \quad (9)$$

The value of 25.05 dBm is assumed for DC or a square wave. A square wave has exactly twice as much power as a sine wave if they both have the same peak-to-peak voltage. The harmonics of a square wave add together to produce exactly as much power as the fundamental frequency; thus, for a sine wave, the power is 3 dB less, or 22.05 dBm.

The minimum input signal power of the ADC is also important since any signal below this threshold falls into the quantization noise of the ADC and causes the desired SNR to decrease; thus, the receiver design must ensure that the MDS is amplified to be larger than the minimum input signal power of the ADC. The minimum input signal power can be calculated using Eq. (7) by substituting the minimum peak-to-peak voltage into the V_p term as

$$P_{\min} = \frac{V_p^2}{R} = \frac{0.0625^2}{50} = 0.0781 \text{ mW}. \quad (10)$$

Converting Eq. (10) into dBm, we obtain

$$P_{\min(dBm)} = 10\log(0.0781) = -11.07 \text{ dBm}. \quad (11)$$

The dynamic range for the input signal power for the ADC is from –11.07 dBm to 25.05 dBm; however, in order to prevent saturating the ADC input, the maximum power must be restricted to 22.05 dBm.

2. MDS at Receiver Front-End

The MDS refers to the minimum signal power required to obtain a particular SNR. The thermal noise power can be computed using

$$N = kTB \quad (12)$$

where k is Boltzmann's constant (1.38×10^{-23} m^2 kg s^{-2} K^{-1}), T is room temperature, and B is the effective bandwidth of the receiver.

The specifications for the LPI radar receiver are shown in Table 2.

Table 2. LPI Radar Receiver Specifications

LPI radar receiver parameters	Value
Operating frequency f	19.2 to 19.46 GHz
Number of frequency channels	13
Radar instantaneous bandwidth B	20 MHz
Minimum SNR at ADC input, SNR_{min}	13.5 dB
Desired Receiver Noise Figure F	< 10 dB
System temperature T	290 K

The thermal noise power of the LPI radar receiver is

$$N = \left(1.38\times10^{-23}\right)\left(290\right)\left(20\times10^{6}\right) = 8.004\times10^{-14}\ \text{W}. \tag{13}$$

Converting Eq. (13) into dBm, we obtain

$$N_{dBm} = 10\log\left(\frac{8.004\times10^{-14}}{1\times10^{-3}}\right) = -101\ \text{dBm}. \tag{14}$$

The result of Eq. (14) refers to the power of the thermal noise floor at the receiver front-end when the instantaneous bandwidth is 20 MHz. For a signal to be successfully detected, it must have a certain power above the noise power. For a detection probability of 0.9 and a false alarm detection probability of 10^{-6} with a single radar pulse, the SNR requirement is 13.5 dB [19]. A targeted noise figure for the entire receiver chain is less than 10 dB; therefore, the input signal power at the receiver front-end (MDS) assuming a worst case noise figure of 10 dB is

$$P_s = -101+13.5+10 = -77.5\ \text{dBm}. \tag{15}$$

This means that if a signal with a power of –77.5 dBm enters the receiver front-end, the receiver is required to boost the signal to the minimum required input power of –11.1 dBm at the input to the ADC in order for the signal to retain its SNR; thus, the entire receiver chain requires a gain of at least 66.4 dB.

3. IF and BPF Selection

As stated in Chapter II, each stage of the receiver should be designed such that it does not have a gain of more than 50 dB. Otherwise, it may become unstable due to the feedback within the active elements, which results in uncontrolled oscillations. The gain of at least 66.4 dB computed in Chapter III, Section B2, requires a minimum of two frequency stages.

The choice of IF is closely related to the availability of filters that have the required cutoff characteristics to remove the intermodulation products that are produced by frequency mixing when converting from one frequency band to another. This may also be dictated by the sampling frequency of the ADC. In order to sample the signal without aliasing, the selected IF must satisfy Nyquist criterion. In practice, the sampling frequency is usually at least four times the Nyquist frequency in order to ensure the aliased signal components are as far away from the information carrying components as possible. A higher sampling frequency also enables better filtering to be performed because there are more samples available for processing.

The ADC sampling frequency is given as 500 MSa/s as shown in Table 1. A choice of 100 MHz as the IF fulfills the criteria. The selected IF is no higher than 200 MHz, but sufficiently high enough for the image frequency to be easily filtered out. The sampling frequency of the ADC is also more than four times the IF.

Given the LPI radar parameters shown in Table 2 and the desired IF of 100 MHz, the center frequency for each channel and the LO frequency required to obtain the IF are tabulated as shown in Table 3.

Table 3. RF Center Frequencies and LO Frequencies of 13 LPI Radar Channels

LPI radar channel	RF center frequency (MHz)	LO frequency (MHz)
1	19210	19110
2	19230	19130
3	19250	19150
4	19270	19170
5	19290	19190
6	19310	19210
7	19330	19230
8	19350	19250
9	19370	19270
10	19390	19290
11	19410	19310
12	19430	19330
13	19450	19350

With the selected IF, a computation of the intermodulation products is required in order to ensure that the higher order intermodulation products do not fall within the IF pass-band of the BPF. The computation of the intermodulation products is given by Eq. (4).

Matrix laboratory software (MATLAB) is used to compute the intermodulation products up to 9^{th} order. This means that the sum of any positive integer values of m and n in Eq. (4) has a maximum value of 9. All possible permutations of $m + n$ from 1 to 9 as long as the sum equals at most 9 are computed. The RF frequency (f1), LO frequency (f2), and their associated intermodulation products of the first frequency channel are shown in Figure 10. Other frequency channels down-convert to exactly the same IF and produce the same IF intermodulation product frequencies. The only differences are their RF and LO frequencies. The amplitude values in the plot are simply placeholders and do not reflect the actual amplitude of the signal. The computation of the amplitude requires knowledge of the mixer design and construction.

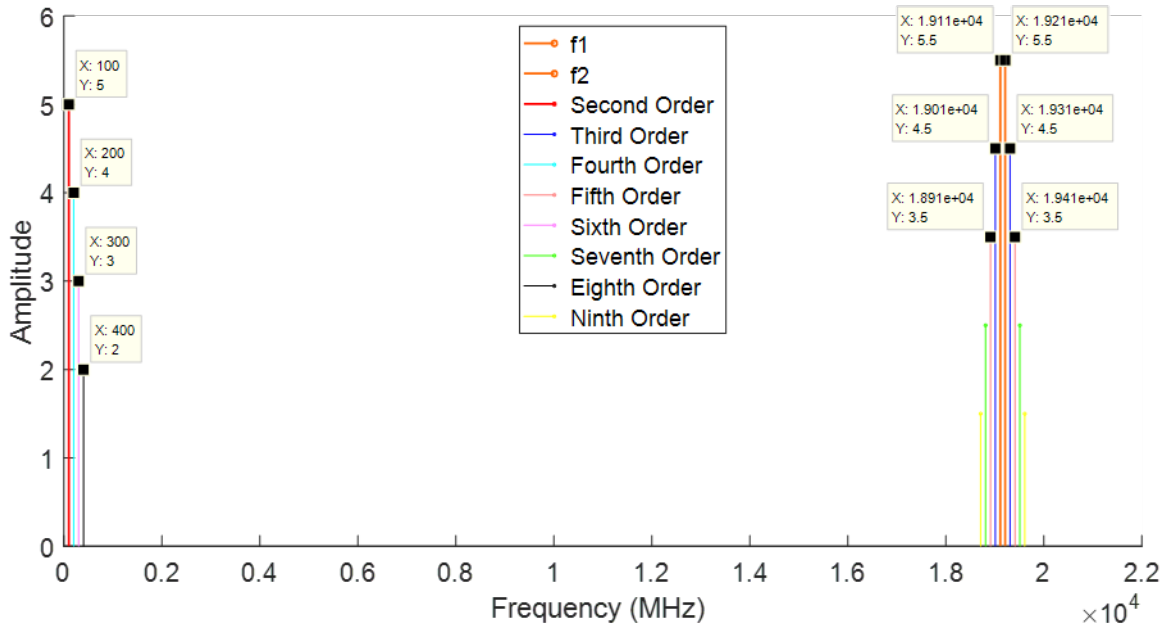

Figure 10. Intermodulation Products Up to 9th Order for 1st Frequency Channel in Table 3

The nearest IF intermodulation product is at 200 MHz, which is 100 MHz away from the desired IF of 100 MHz as shown in Figure 11.

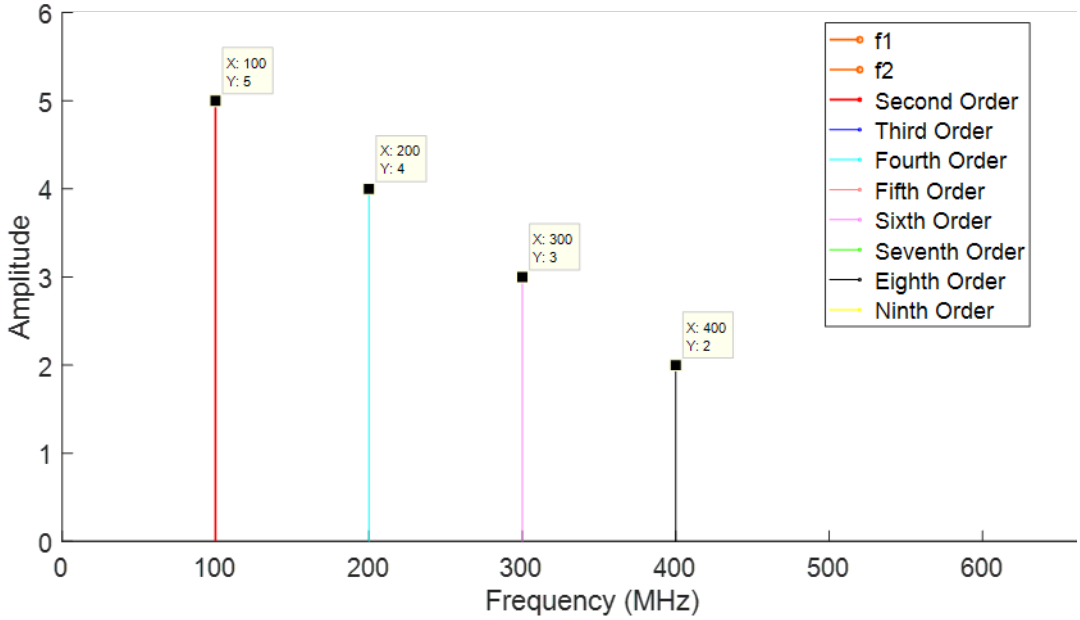

Figure 11. IF Intermodulation Products for 1st Frequency Channel

As mentioned earlier, the true power, or amplitude, of the intermodulation product is dependent on the design and construction of the mixer. Marki Microwave is a microwave company that designs, manufactures, and sells RF components. The company provides a spur calculator on their website (http://www.markimicrowave.com/spur-calculator.aspx) that computes the intermodulation products generated by their mixer design. The input frequency and LO input frequency from the first frequency channel are used for the computation shown in Figure 12. The other frequency channels produce the same results. The nearest intermodulation product is 59 dB below the desired IF. While we do not use Marki Microwave mixers in our design, their spur calculator provides good power estimates for a variety of mixers. As such, we use the results from their spur calculator.

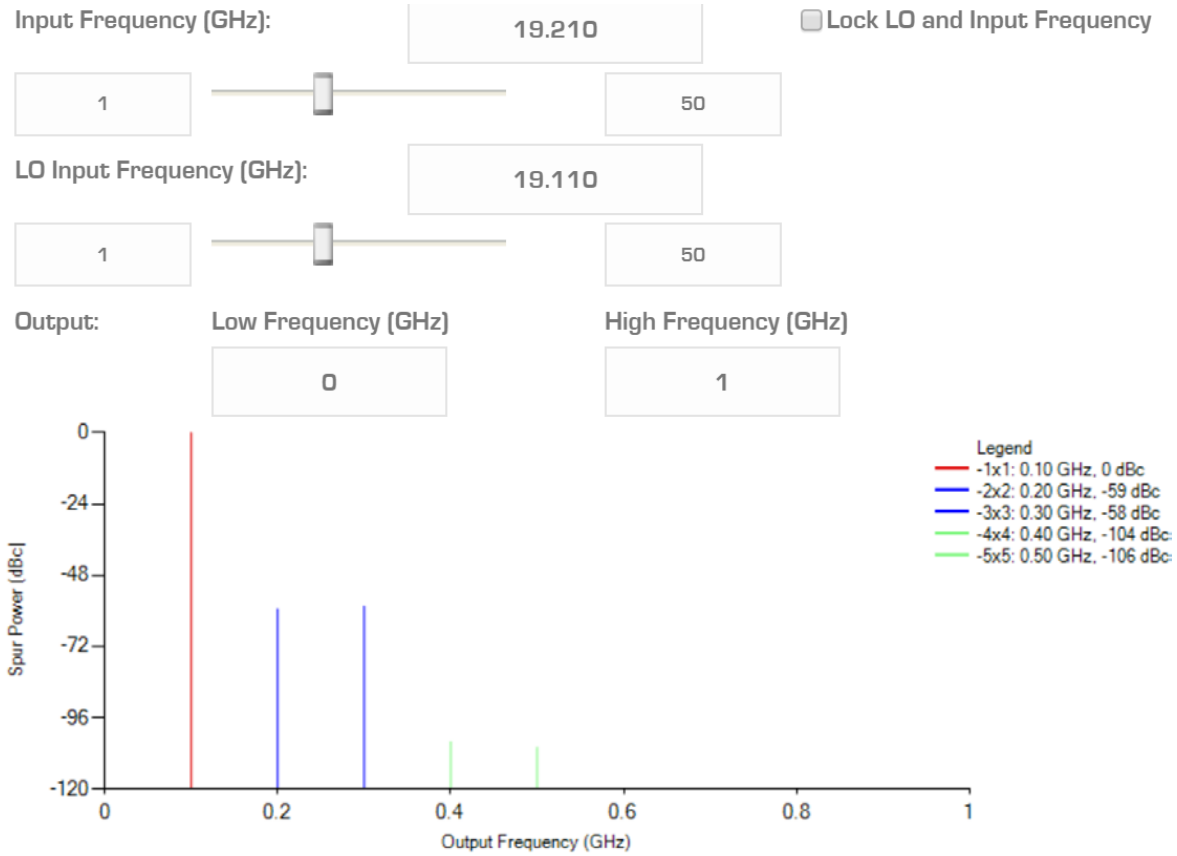

Figure 12. Intermodulation Product Computation with Signal Power Relative to 0 dBm

A BPF with the required roll-off and attenuation is required to suppress the intermodulation products down to the noise floor so that it does not interfere with the desired signal. The required specifications for the BPF are tabulated in Table 4.

Table 4. IF BPF Required Specifications

IF BPF parameters	Value
Center frequency	100 MHz
Instantaneous 3-dB bandwidth	20 MHz
Passband attenuation	< 2 dB
Stopband attenuation	–65 dBc at 100 MHz away

K&L Microwave is a leading designer and manufacturer of discrete RF and microwave filters. If the receiver design is to be compatible with all three functions of the system, we need to ensure that the BPF is able to suppress the intermodulation products down into the noise floor 100 MHz away from the desired IF. Among the three functions of LPI radar, communications module, and EW module, the communications module has the smallest bandwidth of 250 kHz. The true thermal noise floor of the communications module is computed using Eq. (12) and converted to dBm as given by

$$N_{dBm} = 10\log\left[\frac{\left(1.38\times10^{-23}\right)\left(290\right)\left(250\times10^{3}\right)}{1\times10^{-3}}\right] = -120 \text{ dBm}. \tag{16}$$

In order to suppress the intermodulation products into the true thermal noise floor, –59 – (–120) = 61 dB attenuation is required. This is based on the assumption that the input signal power is 0 dBm. The B-series tubular BPF is able to meet the requirements and comes in a suitable package for ease of use in proof-of-concept laboratory assembly as shown in Figure 13.

◆ **Features:**

- Economical Design Yields High Performance Results
- 100 MHz to 6000 MHz Frequency Range*
- 3 dB BW; 4-40%
- Design Available in 2-8 Sections
- 0.05 dB Chebychev Design Response
- Ruggedized Package Designs

◆ **Specifications:**

Model	Diameter (Inches/mm)	Frequency (MHz)	3 dB % BW	VSWR	Average Power (Watts)	Impedance (Ohms)	No. of Sections	Shock	Vibration	Temp.	Relative Humidity
B250	.25/6.35	1000-6000	4-40	1.5:1	2	50	2-8	20 G's, 1/2 Sine, 11 Ms	10 G's, 10 Hz-2000 Hz	-55 to +85 °C	0-95%
B120**	.50/12.7	100-2500	4-40	1.5:1	18						
B340	.75/19.05	100-1000	4-40	1.5:1	40						
B110	1.25/31.7	70-600*	4-40	1.5:1	200						

** Model B120 fits most applications and is the most cost effective choice.

Figure 13. B-series Tubular BPF from K&L Microwave. Source: [20].

The datasheet for the B-Series BPF comes with a set of graphs and equations to determine the customization for the BPF model. The first step is to compute the percentage 3-dB bandwidth as given by

$$\%\ \text{bandwidth} = \left(\frac{\text{3-dB bandwidth}}{\text{Center frequency}} \right) \times 100 . \tag{17}$$

Substituting the 3-dB bandwidth and the center frequency values into Eq. (17) results in

$$\%\ \text{bandwidth} = \left(\frac{20 \times 10^6}{100 \times 10^6} \right) \times 100 = 20\% \ . \tag{18}$$

Next, the number of % bandwidths from the center frequency is

$$\text{No. \% bandwidth} = \frac{\text{reject frequency} - \text{center frequency}}{\text{3-dB bandwidth}} . \tag{19}$$

Substituting the reject frequency, center frequency, and 3-dB bandwidth into Eq. (19) results in

$$\text{No. \% bandwidth} = \frac{200\times10^6 - 100\times10^6}{20\times10^6} = 5. \tag{20}$$

Using the result from Eq. (18), we use the plot shown in Figure 14.

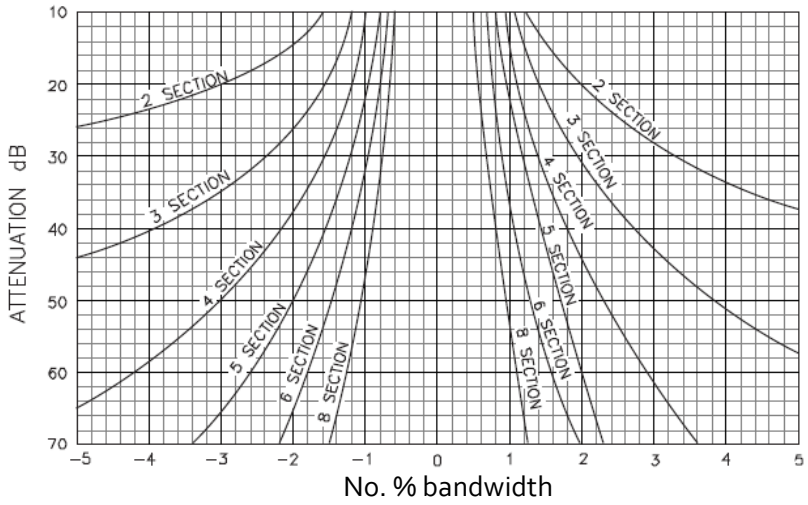

Figure 14. Minimum Stopband Attenuation as Multiples of 3-dB Bandwidth for Bandwidths 15% to 30%. Source: [20].

In order to achieve more than 61 dB attenuation five bandwidths away, a four-section BPF is required as shown in Figure 14. The order code for the customized BPF from K&L microwave is 4B120-100/T20-O/O, which means a four-section BPF model 120 with a center frequency of 100 MHz, 3-dB bandwidth of 20 MHz, and subminiature version A (SMA) with female connectors for both input and output.

4. Proposed Receiver Architecture Design Using COTS Modules

A high level block diagram of a proposed receiver architecture using COTS modules is shown in Figure 15. The proposed design is based on a single stage RF down-conversion super-heterodyne receiver architecture. The actual RF receiver requires 144 receive channels for the LPI radar antenna array, but the proof-of-concept design contains only four receive channels. In order to obtain 144 receive channels, the four-channel design has to be duplicated 36 times.

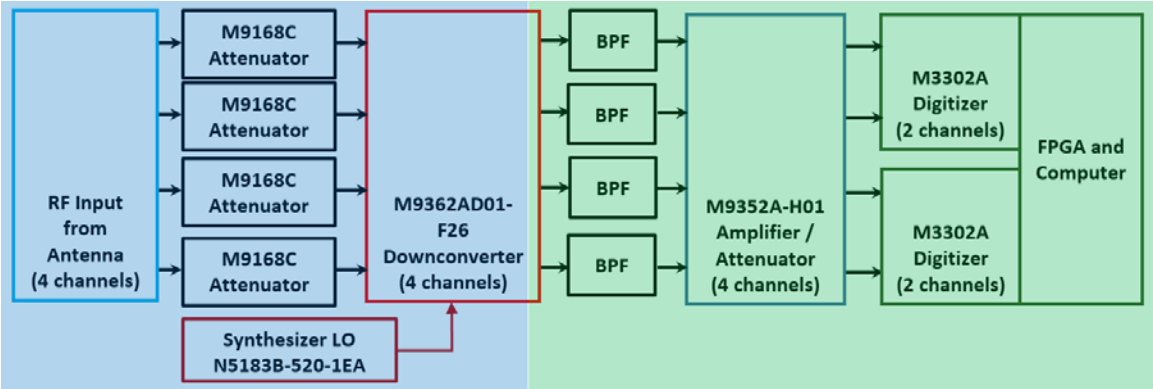

Figure 15. Block Diagram of Proposed Receiver Architecture

The different stages are color coded. The components in the blue section are in the RF stage, and the components in the green section are in the IF stage. The mixer is located within the downconverter module and is responsible for separating the different stages. Within each stage, there are amplifiers and attenuators to condition the signal.

C. COTS RECEIVER ARCHITECTURE PERFORMANCE ANALYSIS

The goal of the receiver is to provide enough amplification to the desired low-power signal without becoming unstable while suppressing the undesirable signals. The three critical parameters that affect the receiver performance are noise figure of the entire receiver chain, gain of each stage, and the total gain. Other parameters such as P1dB and maximum allowable input power into each component also have to be considered for a successful design. A detailed design of the proposed receiver architecture is shown in Figure 16.

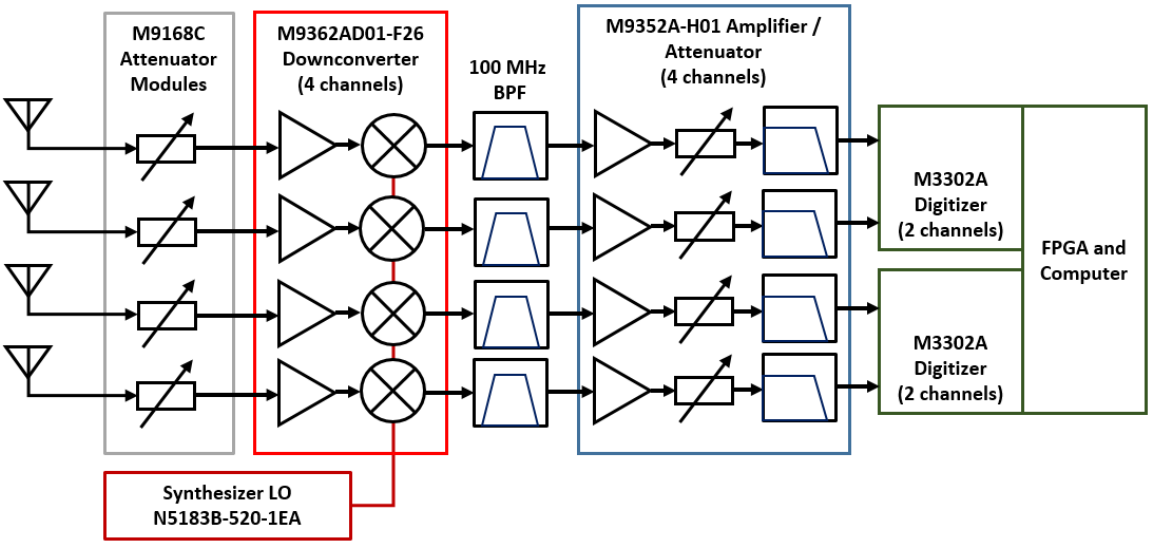

Figure 16. Detailed Block Diagram of Proposed Receiver Architecture

The gain or loss, noise figure, and P1dB parameters for each of the modules are obtained from the datasheets of the respective modules and tabulated in Table 5.

Table 5. Parameters for Each COTS Module. Adapted from [13]–[15], [20].

Module	Gain (dB)	Noise Figure (dB)	P1dB (dBm)
Antenna	11.5	0	30
M9168C Attenuator	–2.5	2.5	30
M9362AD01-F26 Downconverter	1	24	–7
BPF (100 MHz)	–2	2	30
M9352A-H01 Amplifier / Attenuator	31.5	3	17

Ideally, the noise figure of the entire receiver chain should be as low as possible. Converting the parameters in Table 5 from dB to ratios and substituting them into Eq. (6), we find the overall noise figure of the system (without the addition of the LNA) as

$$F_{system} = 1.78 + \frac{251.19-1}{\left(\frac{1}{1.78}\right)} + \frac{1.59-1}{\left(\frac{1}{1.78}\right)(1.26)} + \frac{2-1}{\left(\frac{1}{1.78}\right)(1.26)\left(\frac{1}{1.59}\right)} = 449.68 \quad (21)$$

$$F_{system(dB)} = 10\log(449.68) = 26.53 \text{ dB}.$$

A noise figure of 26.53 dB is considered very poor for a receiver. This means that the receiver output adds approximately 450 times the amount of noise that is at the input. This noise figure also does not meet the LPI radar receiver specifications set out in Table 2. As shown in Chapter II, the noise figure is highly dependent on the first stage gain and noise figure. In Chapter II, it was also proposed that the solution to reduce the noise figure of the entire receiver chain is to include a LNA at the front of the receiver chain directly after the antenna. The selected LNA is from Mini-Circuits with the model number ZVA-213+. The parameters of the LNA obtained from the datasheet are tabulated in Table 6.

Table 6. Mini-circuits LNA ZVA-213+ Parameters. Adapted from [21].

Operating Frequency (GHz)	Gain (dB)	Noise Figure (dB)	P1dB (dBm)
19	24.47	4.11	20.85
20	24.06	4.06	19.74
21	22.91	4.35	18.57

Using the parameters from the operating frequency of 19 GHz, we recompute the noise figure as

$$F_{system} = 2.58 + \frac{1.78-1}{279.9} + \frac{251.19-1}{(279.9)\left(\frac{1}{1.78}\right)} + \frac{1.59-1}{(279.9)\left(\frac{1}{1.78}\right)(1.59)} + \ldots$$
$$+ \frac{2-1}{(279.9)\left(\frac{1}{1.78}\right)(1.59)\left(\frac{1}{1.59}\right)} = 4.18 \quad (22)$$

$$F_{system(dB)} = 10\log(4.18) = 6.21 \text{ dB}.$$

The noise figure with the addition of the LNA is greatly improved from the former 26.53 dB to the current 6.21 dB. This meets the required specification for the LPI radar receiver.

A re-computation of the MDS is required since the overall noise figure of the receiver is reduced from 10 dB to 6.21 dB. Modifying Eq. (15), we obtain

$$P_s = -101 + 13.5 + 6.21 = -81.29 \text{ dBm}. \tag{23}$$

The MDS of the receiver is now –81.29 dBm. The receiver architecture block diagram with the inclusion of the LNA is shown in Figure 17.

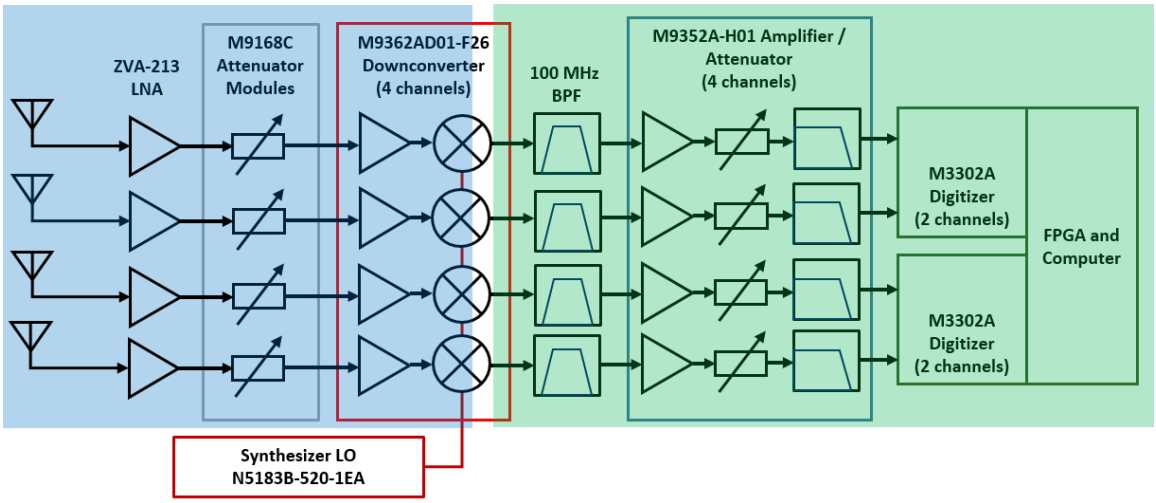

Figure 17. Block Diagram of Receiver Architecture with LNA Included

In Figure 18, the cumulative gain of the receiver at each component is plotted in blue and the noise figure is plotted in red. The total gain of the entire receiver chain is 63.97 dB. The noise figure is 6.21 dB, which is the same value computed by Eq. (22).

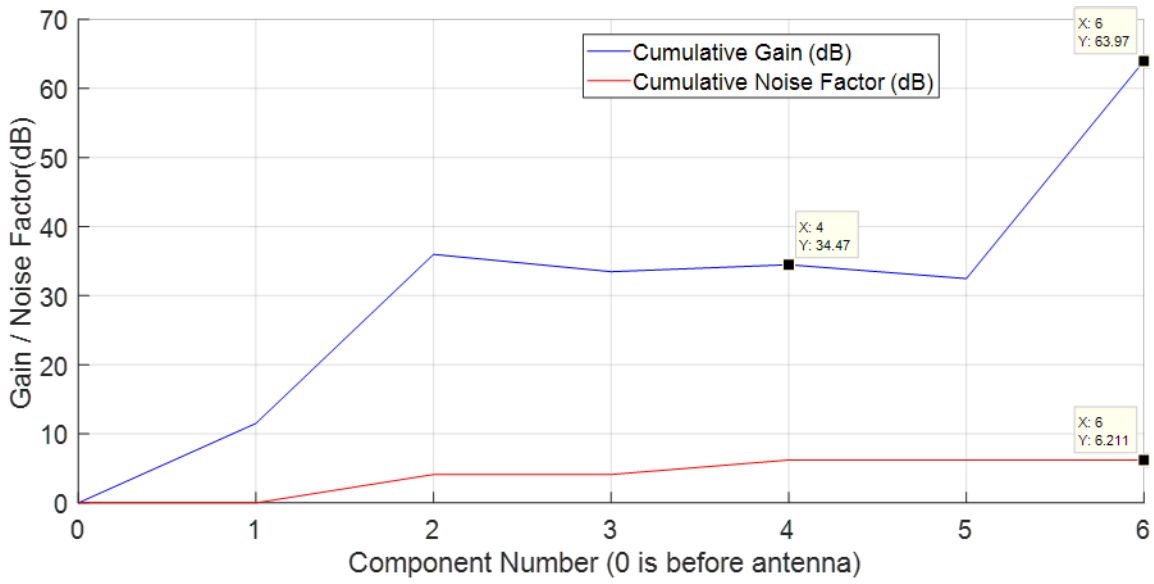

Figure 18. Cumulative Gain (dB) and Noise Factor (dB) at the Input of each Receiver Component

The maximum and minimum input signal power levels for the ADC are 22 dBm and –11 dBm as computed in Chapter III, Section B1. By subtracting the gain of each stage from the maximum and minimum input signal power levels at the ADC, the maximum input power before the antenna is approximately –42 dBm, denoted by the blue plot, and the minimum input power is approximately –75 dBm, denoted by the red plot in Figure 19. A signal within this range is successfully sampled by the ADC. Signals greater than –42 dBm is also easily detectable by the receiver; however, in that case, an automatic gain control (AGC) mechanism is needed to prevent the signal from saturating the receiver chain components and the ADC. The green line shows the P1dB or saturation power level of each of the components in the chain. A successful design must ensure that the highest input signal must be below the P1dB level for every component to ensure signal linearity. The red dotted line shows the noise floor at each stage of the receiver. The noise floor must be below the lowest signal level by 13.5 dB throughout the entire receiver chain. The closest point is at the input to the ADC where the SNR is –11 – (–37.79) = 26.79 dB, which is better than the 13.5 dB minimum SNR requirement.

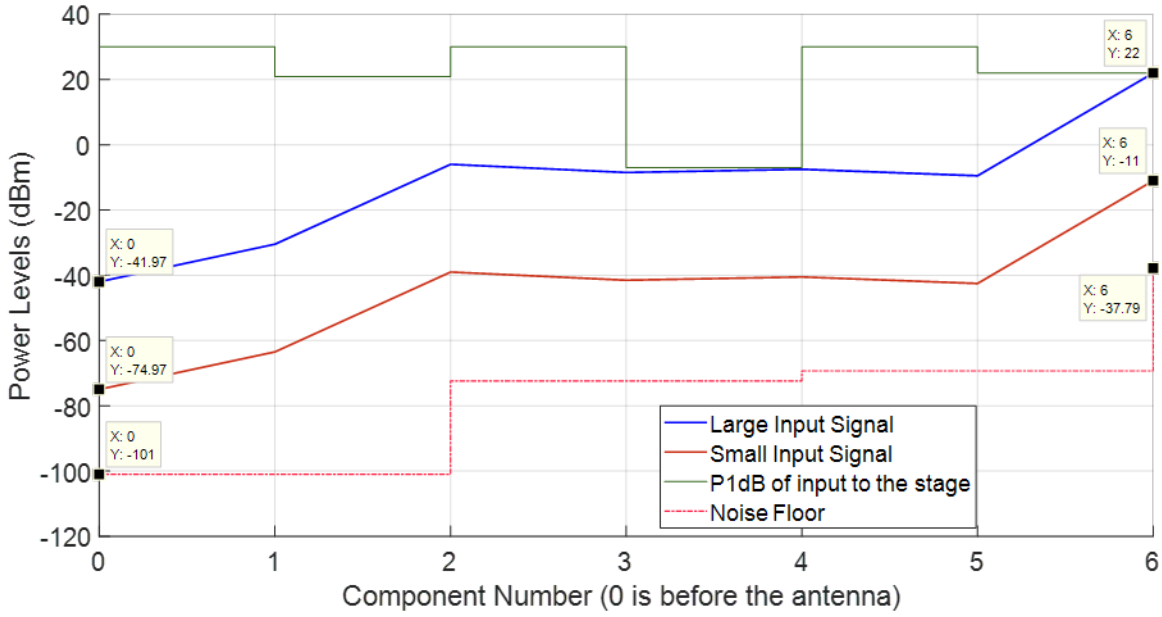

Figure 19. Maximum and Minimum Input Signal Power Level Requirement for Correct ADC Operation

The active gain of the RF stage excluding the antenna gain (i.e., gain of components 1, 2, and 3) is 34.47 – 11.5 = 22.97 dB, and the gain of the IF stage is 29.5 dB as shown in Figure 18. For stability purposes, the maximum gain of each stage must be less than 50 dB. Recall that the MDS is computed to be –81.3 dBm, and the lowest signal power level that can be accommodated by the receiver with respect to the ADC is –75 dBm. As a result, a gain of about 6.3 dB is required for the receiver to reach the MDS requirement. This gain can easily be added to the RF stage of the final design in the form of an amplifier since it has a lower total active gain of 22.97 dB.

D. CHAPTER SUMMARY

An overview of the receiver architecture was presented in this chapter. The design of the receiver using COTS modules was presented. ADC dynamic range, MDS at receiver front-end, IF selection, and BPF selection were identified to be the critical steps in the design of the receiver. Performance analysis of the receiver design was presented, and a LNA was incorporated at the front of the receiver chain after the antenna to reduce the

noise figure of the entire receiver chain. Additional gain was proposed to meet the MDS performance through the addition of an amplifier in the RF section.

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IV. TRANSMITTER ARCHITECTURE AND ANALYSIS

A. OVERVIEW OF TRANSMITTER ARCHITECTURE

As discussed in Chapter III, the focus of the thesis is to realize the RF front end in the red dotted box illustrated in Figure 7. The transmitter chain is part of the RF front end to convert the digital signals generated by the master processor into RF signals suitable for wireless transmission using the antenna array. Similar to the receiver chain in the RF front end, a proof-of-concept implementation is constructed using COTS modules, and its performance is analyzed to determine its feasibility.

B. TRANSMITTER ARCHITECTURE DESIGN USING COTS MODULES

Three RF parameters are required before a detailed transmitter design process can commence. They are transmitter output power, input frequency, and output frequency. The input frequency, output frequency, and gain requirement dictate the type of RF components and the number of RF stages that are utilized to up-convert the input signal to the output for transmission. The transmitter output power determines the type of amplifier and the size of the transmitter.

The requirements for the LPI radar transmitter are shown in Table 7.

Table 7. LPI Radar Transmitter Parameters

LPI radar transmitter parameters	Value
Output frequency f_{out}	19.2 to 19.46 GHz
Input frequency f_{in}	100 MHz
Transmitter Output Power P_{out}	1 W
Transmitter Input Power P_{in}	22.4 mW maximum

A high level block diagram of a proposed transmitter architecture using COTS modules is shown in Figure 20.

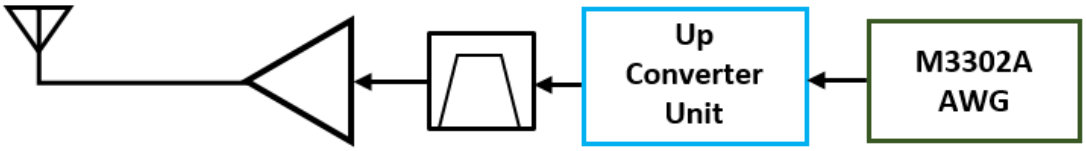


Figure 20. Block Diagram of a Proposed Transmitter Architecture

The proposed design is based on a single-stage RF up-conversion transmitter architecture. The transmit antenna consists of a single omni-directional antenna. The Keysight M3302A digitizer contains an arbitrary waveform generator (AWG) which is able to generate baseband signals up to 200 MHz frequency. It is the source of the signal for the transmitter. The specifications for the AWG are tabulated in Table 8.

Table 8. M3302A AWG Specifications

AWG M3302A specifications	Value
Output frequency f_{out}	DC to 200 MHz
Instantaneous bandwidth	200 MHz
Output voltage V_{out}	–1.5V to 1.5V
Source Impedance R	50 Ω

The output voltage indicates the maximum voltage swing of the AWG output. Converting that to power in dBm, we obtain

$$P_{\max(dBm)} = 10\log\left(\frac{V_P^2}{R}\right) = 10\log\left(\frac{1.5^2}{50}\right) = 10\log(45\text{ mW}) = 16.5\text{ dBm}. \quad (24)$$

Syntonic Microwave is a company that specializes in wideband microwave synthesizers and tuner products. The up-converter unit selected for this design is their RFT-4470 model as shown in Figure 21.

KEY SPECIFICATIONS	
TUNABLE OUTPUT RANGE	0.5–18, 0.5–26.5, 0.5–40 GHz
INPUTS	Wideband and Narrowband (with option)
PHASE NOISE	<0.5 deg RMS

Figure 21. Syntonic Microwave RFT-4470 Up-Converter Unit. Source: [22].

The up-converter unit is responsible for converting the signal generated by the AWG with a center frequency at around 100 MHz up to the desired output frequency between 19.2 to 19.46 GHz. The relevant specifications are tabulated in Table 9.

Table 9. Syntonic Microwave RFT-4470 Specifications. Source: [22].

RFT-4470 specifications	**Value**
Input frequency f_{in}	70, 140, 160, 1000 MHz selectable
Output frequency f_{out}	0.5 to 26.5 GHz
Input Power P_{in}	Up to –10 dBm
Instantaneous bandwidth	50, 100, 500 MHz
Output Power P_{out}	+10 dBm
Gain G	0 to 20 dB in 1 dB step
Spurious	> –50 dBm
Harmonics	–25 dBc at 0 dBm output

The up-converter unit input cannot exceed –10 dBm. This means that the output from the AWG must be attenuated from 16.5 dBm to less than –10 dBm to avoid damaging the input to the up-converter. The AWG has the capability to output signals below –10 dBm. Converting that to voltage, we obtain

$$V = \sqrt{(50)\left(1\times10^{-3}\right)\left(10^{\frac{-10}{10}}\right)} = 70.7 \text{ mV} . \tag{25}$$

It is important to program the AWG to restrict its output signal amplitude to no larger than 70.7 mV to prevent damage to the up-converter input.

The up-conversion process generates spurs and harmonics which are unwanted signals. Although the up-converter unit has specifications to attenuate the spurs and harmonics to less than –50 dBm and –25 dBc, respectively, these undesirable signals can still cause interference if they are amplified and transmitted through the antenna. As such, a BPF is included after the up-converter to remove these unwanted signals. The required specifications for the BPF are tabulated in Table 10.

Table 10. RF BPF Required Specifications

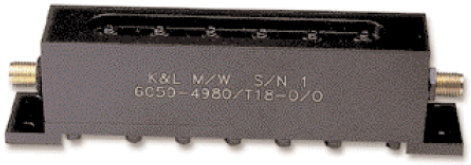
RF BPF parameters	Value
Center frequency	19.2 GHz
Instantaneous 3-dB bandwidth	200 MHz
Passband attenuation	< 2 dB
Stopband attenuation	–40 dBc at 100 MHz away

In order to suppress the spurs and harmonics 100 MHz away from the desired RF, a 40 dB attenuation is required. The C-series cavity BPF from K&L microwave is able to meet the requirements and comes in a suitable package for ease of use in proof-of-concept laboratory assembly as shown in Figure 22.

Cavity Filters Narrow Bandwidth — C Series

◆ **Features:**

- High "Q" Design Allows Narrow Bandwidth While Offering Low Loss
- "Q" Values of up to 10,000
- 3 dB BW Available from 0.1% to 3.5% (f_0)
- Covers the 60 MHz to 30 GHz Frequency Range
- Low Ripple Chebyshev Response
- Ruggedized Package to Withstand Severe Environmental Stress



◆ **Specifications:**

Model	Frequency (MHz)	3 dB % BW	VSWR	Passband Return	Avg. Power (Watts)	Impedance (Ohms)	No. of Sections	Shock	Vibration	Temperature	Relative Humidity
C20	30-140	.2-3.5	1.5:1	> =3.5 X f_0	5	50	2-6	Contact Factory			
C30	141-450	.2-3.5	1.5:1	> =3.5 X f_0	5	50	2-6				
C40	451-2000	.2-3.5	1.5:1	> =3.5 X f_0	5	50	2-6				
C42	800-2500	.2-3.5	1.5:1	> =1.5 X f_0	5	50	2-7	20 G's, 1/2 Sine, 11 Ms	10 G's, 10 Hz-2000 Hz	-20 to +50 °C	0-95%
C45	1000-3000	.2-3.5	1.5:1	> =1.5 X f_0	5	50	2-7				
C50	2000-10000	.2-3.0	1.5:1	> =2.1 X f_0	5	50	2-9				
C52	8000-12000	.2-3.0	1.5:1	> =2.1 X f_0	5	50	2-9				
C60	6000-30000	.1-1.8	1.5:1	> =1.6 X f_0	5	50	2-9				

Figure 22. C-series Cavity BPF from K&L Microwave. Source: [23].

The datasheet for the C-Series BPF comes with a set of graphs and equations similar to the B-Series BPF described in Chapter III, Section B3. The approximate stopband attenuation can be obtained by determining the number of % bandwidths from the center frequency. Substituting the reject frequency, center frequency, and 3-dB bandwidth into Eq. (19) results in

$$\text{No. \% bandwidth} = \frac{19\times10^9 - 19.2\times10^9}{200\times10^6} = -1. \tag{26}$$

Using the result from Eq. (26), we obtain the number of sections required for the BPF from the plot as shown in Figure 23.

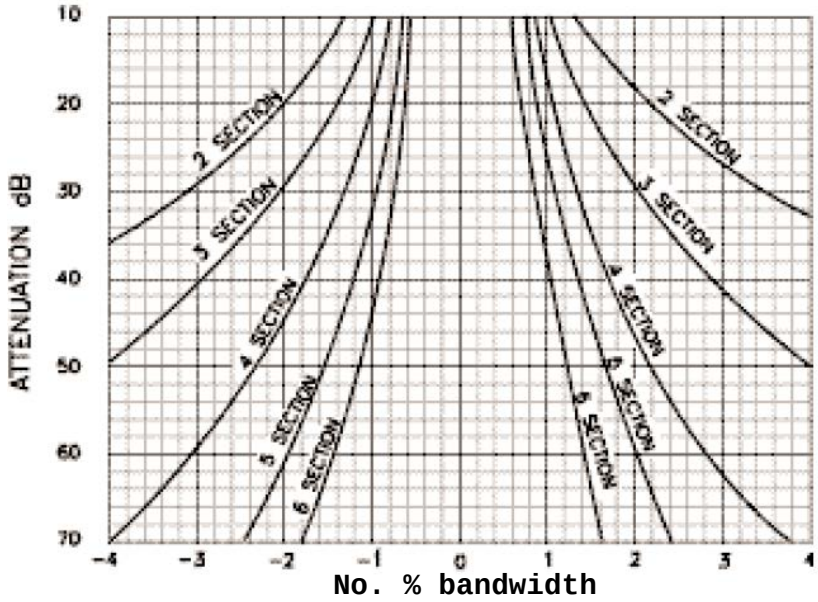


Figure 23. Minimum Stopband Attenuation as Multiples of 3-dB Bandwidth. Source: [23].

In order to achieve more than 40 dB attenuation one bandwidth away, a six-section BPF is required. The order code for the customized BPF from K&L microwave is 6C60-19200/T200-O/O, which means a six-section BPF model C60 with a center frequency of 19200 MHz, 3-dB bandwidth of 200 MHz, and SMA female connectors for both input and output.

The up-converter can only generate a maximum output power of 10 dBm. Converting that to power in watts, we obtain

$$P = \left(1\times10^{-3}\right)\left(10^{\frac{10}{10}}\right) = 0.01\ \text{W}. \tag{27}$$

The transmitter output power requirement is 1.0 W; therefore, an amplifier is required to boost the signal from 0.01 W to 1.0 W. Pasternack is a company that carries a huge selection of off-the-shelf RF components. The PE15A4021 amplifier is able to meet the requirement and comes in a package that is suitable for proof-of-concept laboratory assembly as shown in Figure 24.

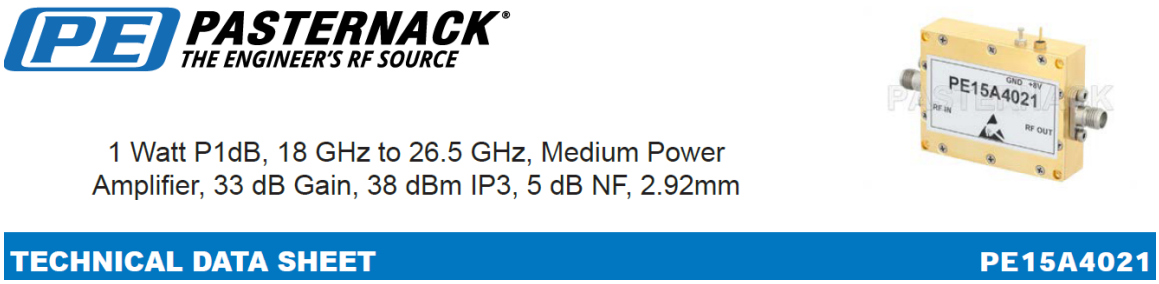


Figure 24. Pasternack RF Amplifier. Source: [24].

C. COTS TRANSMITTER ARCHITECTURE PERFORMANCE ANALYSIS

The goal of the transmitter is to up-convert a baseband signal into a RF signal of desired frequency for transmission through the air. The two critical parameters that affect the transmitter performance are overall gain and the P1dB of each RF component. Other parameters such as input frequencies, output frequencies, and maximum allowable input power into each component also must be addressed for a successful design. A detailed design of the proposed transmitter architecture is shown in Figure 25.

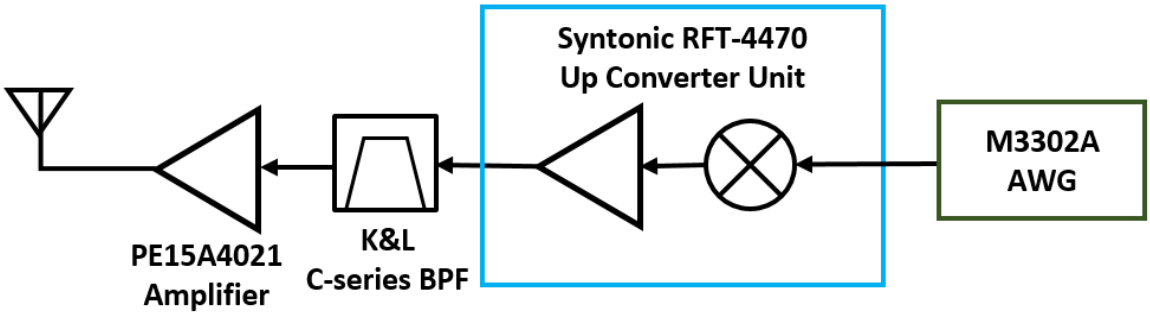


Figure 25. Detailed Block Diagram of Proposed Transmitter Architecture

Similar to the receiver design gain criterion, the gain of each stage of the transmitter should not exceed 50 dB. The gain or loss, P1dB, and maximum allowable input power for each of the modules are tabulated in Table 11.

Table 11. Parameters for the COTS Modules. Adapted from [12], [22]–[24].

Module	Gain (dB)	P1dB (dBm)	Max Input Power (dBm)
M3302A AWG	Adjustable	16.5 dBm	-
RFT-4470 Up-converter	Adjustable from 0 to 20 dB	10 dBm	–10 dBm
C-Series BPF	–1.4 dB	30 dBm	30 dBm
PE15A4021 Amplifier	33 dB	31 dBm	0 dBm

The cumulative gain of the transmitter at each component is plotted as shown in Figure 26. From the plot, we see that the total gain of the entire transmitter required to achieve the desired output power of 1.0 W is 44.6 dB. This can be achieved by a single stage up-conversion. The IF stage has an overall gain of 13.0 dB, and the RF stage has an overall gain of 31.6 dB.

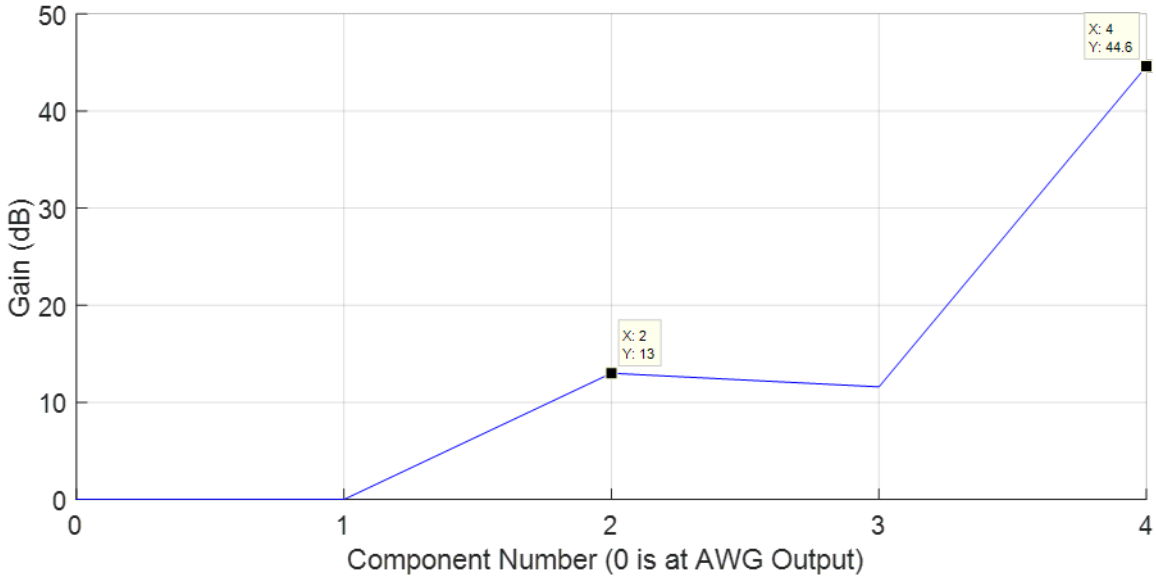


Figure 26. Cumulative Gain (dB) at the Input of Each Transmitter Component

The expected signal power and the P1dB of each transmitter component are plotted in Figure 27. We see that the expected signal power is below the P1dB of all the components, ensuring that the signal remains in the linear region of the components to prevent component saturation from generating unwanted harmonics. We note that the final stage amplification results in the signal exceeding the P1dB of the last stage amplifier. This is usually not an issue since the final stage amplifier is often operated in the saturation region so that maximum power output is achieved. If there is a need to maintain linearity at the output, the input power can be reduced by 2.0 dB to ensure that the output power is within the linear region of the amplifier.

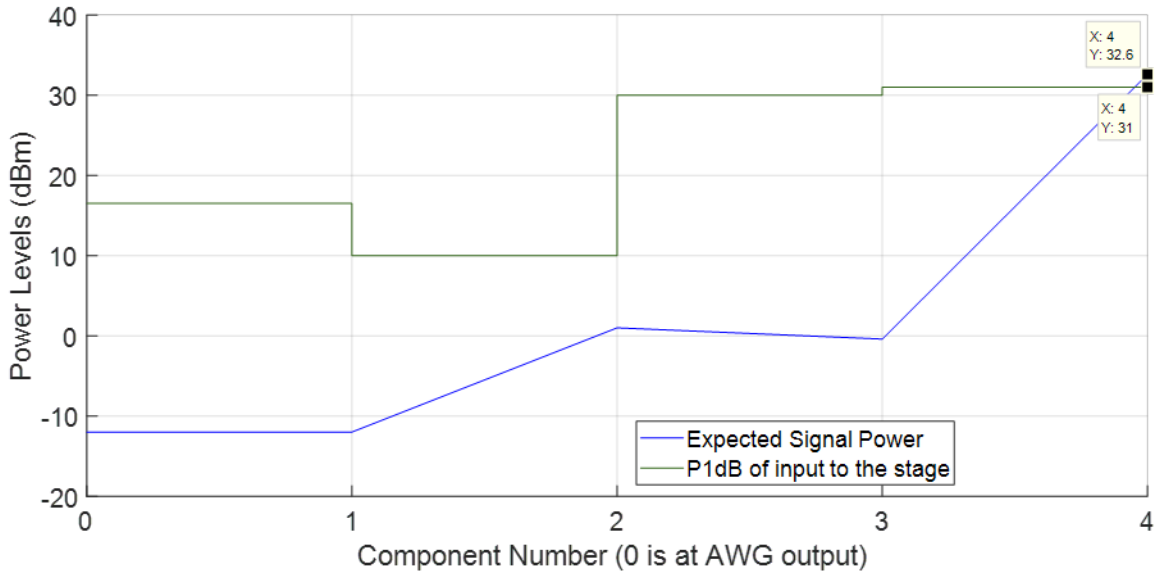


Figure 27. Expected Signal Power and P1dB at the Input of Each Transmitter Component

D. CHAPTER SUMMARY

An overview of the transmitter architecture was presented in this chapter. The design of the transmitter using COTS modules was presented. Transmitter output power, input frequency, and output frequency were identified to be the critical parameters in the design of the transmitter. Performance analysis of the transmitter design was presented. The AWG must be programmed to restrict its output signal amplitude to no larger than

70.7 mV, or –10.0 dBm, output power to prevent damage to the up-converter input. The final stage amplifier may be saturated if the AWG output is at its maximum of –10.0 dBm. If there is a requirement for the output signal to maintain linearity, the AWG output must be reduced by 2.0 dB.

V. PROTOTYPE SETUP, MEASUREMENT RESULTS AND PROPOSED CUSTOMIZED DESIGN

A. OVERVIEW OF COTS PROTOTYPE SETUP

The COTS prototype architecture is shown in Figure 17. The COTS hardware receiver setup is shown in Figure 28.

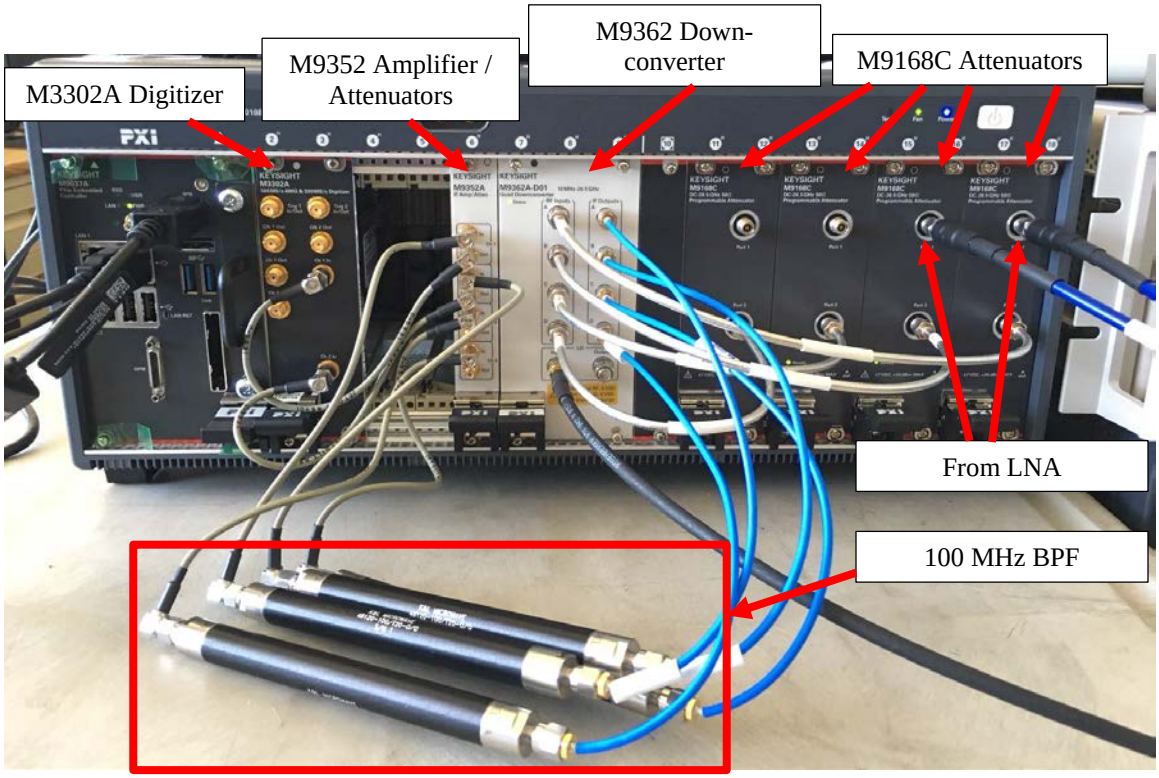


Figure 28. COTS Receiver Setup

The receiver setup with an external signal generator, spectrum analyzer for frequency and power measurement, LNA module, and its associated power supply are shown in Figure 29.

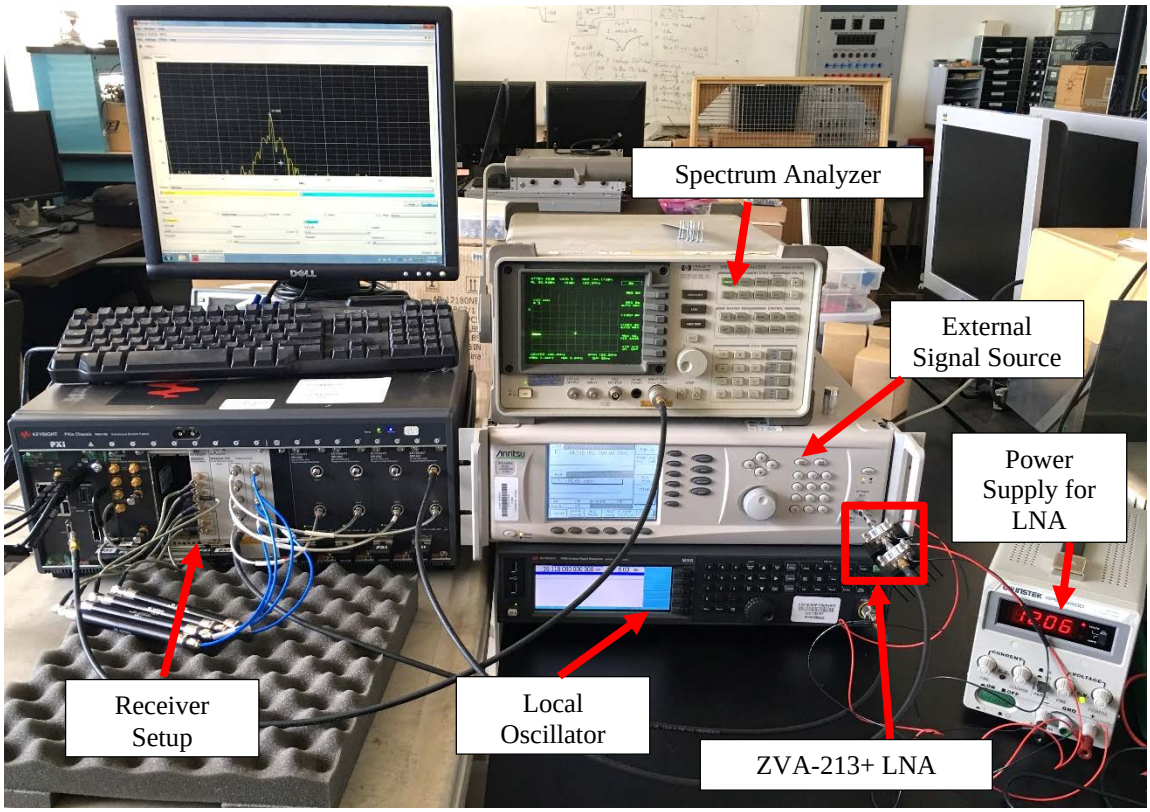


Figure 29. COTS Receiver Setup with Test Equipment

B. BPF FREQUENCY RESPONSE CHARACTERISTICS

1. Receiver BPF Frequency Response

Each receiver channel contains an IF BPF. The BPF is a critical component in the receiver chain to ensure the removal of the unwanted signals before sampling by the ADC. Any unwanted signal that is not removed by the BPF corrupts the receive signal. The required specifications for the BPF are tabulated in Table 4. There are four BPFs in the COTS receiver design. A network analyzer is used to measure the BPF passband frequency response characteristics to determine if the actual hardware meets the required specifications. The filter (S/N 1) forward gain or S_{21} parameter is plotted against the range of frequencies from 10 MHz to 200 MHz. The center frequency, 3-dB instantaneous bandwidth, passband attenuation, and stopband attenuation characteristics are plotted as shown in Figure 30.

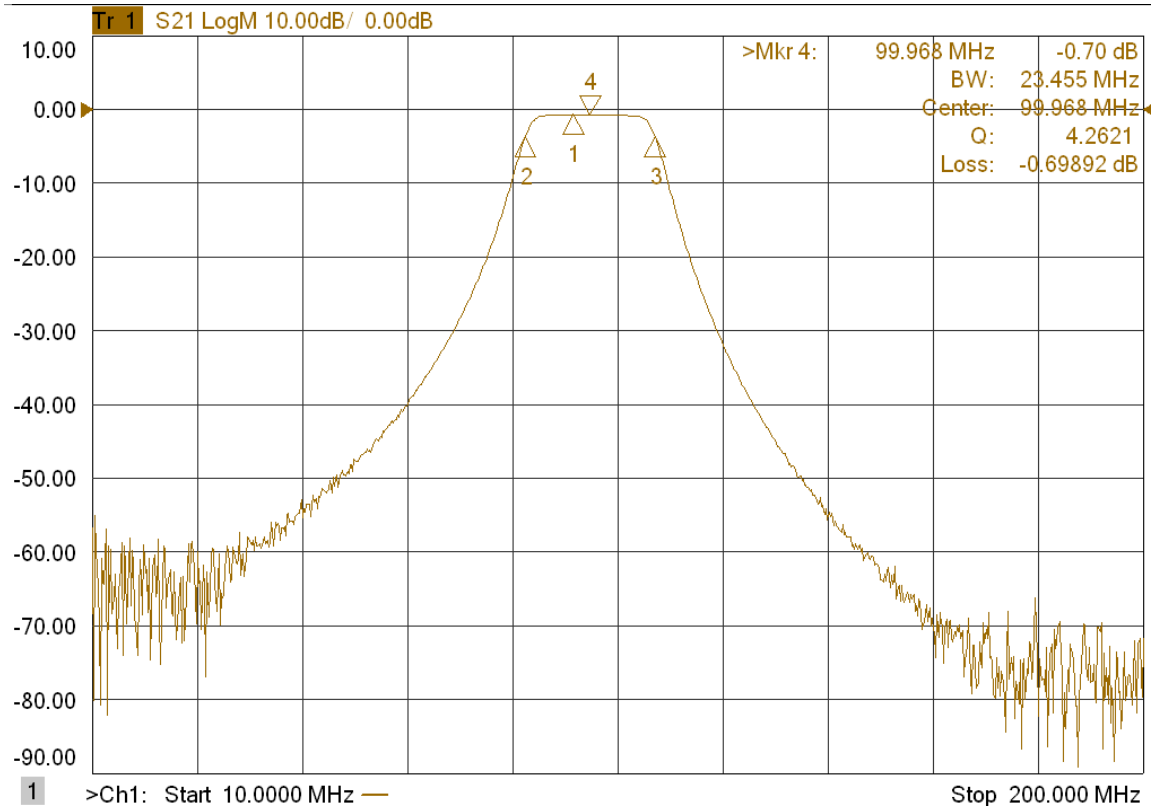


Figure 30. Frequency Response Characteristics of IF BPF S/N 1

The measured parameters of all four BPFs are tabulated in Table 12. The measured parameters of all four BPFs meet the required specifications. Plots for the remaining characteristics are attached in the Appendix.

Table 12. IF BPF Parameter Measurements

IF BPF parameters	S/N 1	S/N 2	S/N 3	S/N 4
Center frequency	99.968 MHz	100.19 MHz	100.05 MHz	101.08 MHz
Instantaneous 3-dB bandwidth	23.455 MHz	24.074 MHz	23.49 MHz	25.993 MHz
Passband attenuation	0.69 dB	0.601 dB	0.605 dB	0.634 dB
Stopband attenuation	–75 dBc at 70 MHz away	–75 dBc at 70 MHz away	–75 dBc at 70 MHz away	–75 dBc at 70 MHz away

2. Transmitter BPF Frequency Response

The transmitter channel contains one RF BPF. The RF BPF is important to ensure the removal of the harmonics and spurious signals that are generated at the up-conversion stage. The required specifications for the RF BPF are tabulated in Table 10. A network analyzer was used to measure the BPF passband frequency response characteristics to determine if the actual hardware met the required specifications. The filter (S/N 1) forward gain or S_{21} parameter is plotted against the range of frequencies from 18.5 GHz to 20.5 GHz to measure the center frequency, 3-dB instantaneous bandwidth, passband attenuation, and stopband attenuation characteristics as shown in Figure 31.

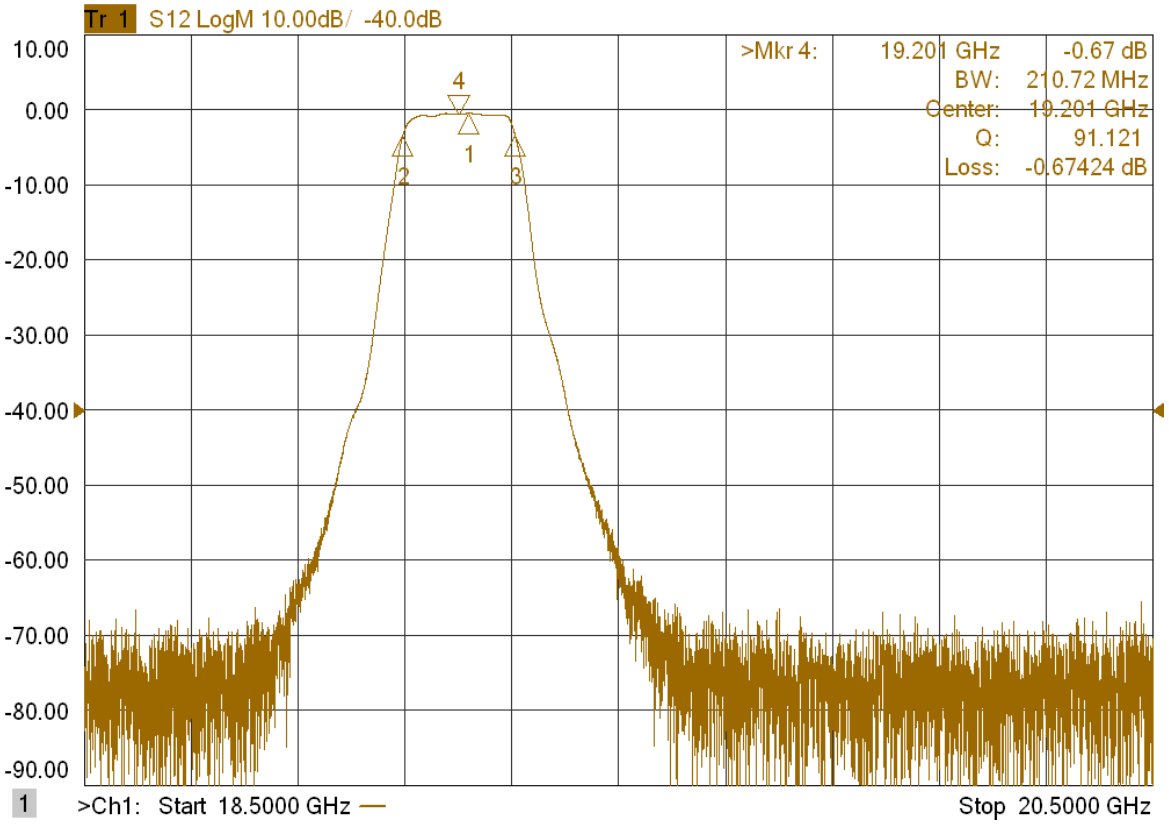


Figure 31. Frequency Response Characteristics of RF BPF S/N 1

The center frequency is 19.201 GHz, passband attenuation is 0.674 dB, 3-dB instantaneous bandwidth is 210.72 MHz, and the stopband attenuation is approximately –40 dB at 100 MHz away. The measured parameters of the RF BPF meet the required specifications.

C. INPUT / OUTPUT MEASUREMENT OF RF DOWN-CONVERSION CHAIN USING INJECTED SIGNAL

The purpose of the input and output measurements of the RF down-conversion chain using injected sinusoidal signal is to ensure that environment factors, i.e., external interference, do not come into play when testing the down-conversion chain. The injection of a single frequency CW signal with a known power level simplifies the gain and loss measurements of each individual component and the measurements for the down-conversion chain as a whole.

The single frequency continuous wave signal is generated by a RF synthesizer, which is shown in Figure 32.

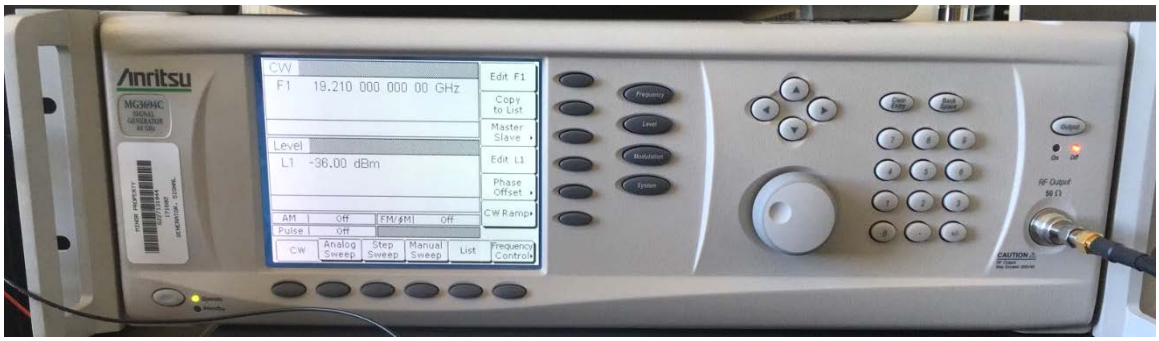


Figure 32. Anritsu RF Synthesizer

The signal is fed using an RF cable of known loss at some test frequency into the front end of the receiver chain immediately after the antenna. The architecture of the receiver using injection mode measurement is shown in Figure 33.

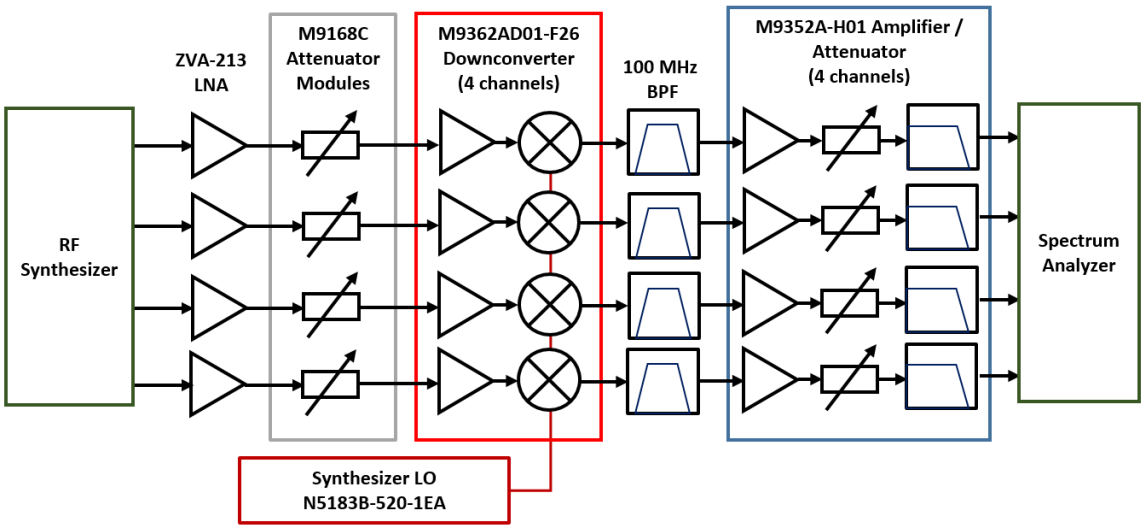


Figure 33. Injection Mode Measurement Receiver Architecture

The spectrum analyzer can be used at an output port of any RF component to measure the power level at that location. The spectrum analyzer is placed at the output of the M9352A amplifier / attenuator for convenience in Figure 33. For example, the RF cable from the RF synthesizer leading to the input of the ZVA-213 LNA can be fed into the spectrum analyzer to obtain the RF cable loss. This process is repeated for each component until the entire RF down-conversion chain is fully characterized. The individual component gains are measured and tabulated in Table 13.

Table 13. RF Component Gain (dB)

Component No.	RF components	Gain (dB)
1	RF Synthesizer	0
2	RF cable (Synthesizer to LNA)	–5.00
3	ZVA-213 LNA	24.00
4	M9168C Attenuator	–2.50
5	M9362AD01-F26 Downconverter	2.30
6	100MHz BPF	–0.70
7	M9352A-H01 Amp / Attenuator	6.83 to 37.33
8	RF cable (Component to Spectrum Analyzer)	–0.50

The cumulative gain of the receiver architecture in injection mode using a single tone at a frequency of 19.21 GHz and input power of 0 dBm with maximum IF amplification is shown in Figure 34.

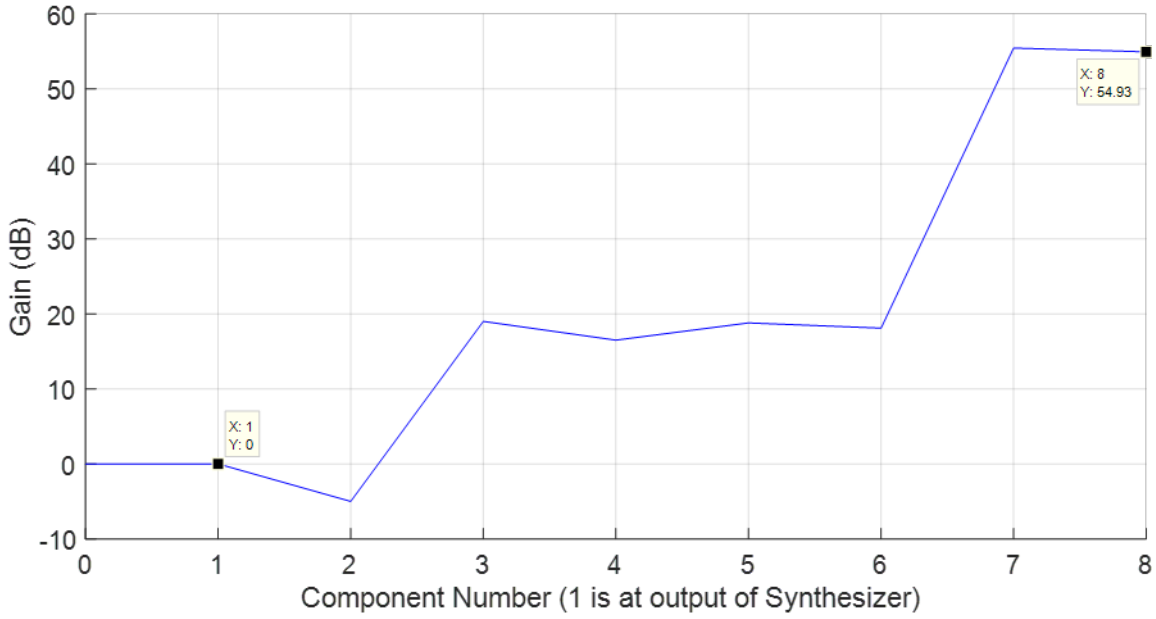


Figure 34. Cumulative Gain of Receiver Chain

The cumulative gain excludes the antenna gain of 11.5 dB because it is measured without the antenna. If we include the antenna gain of 11.5 dB, the total gain is

$$G_r = 11.5 + 54.93 = 66.43 \text{ dB}. \tag{28}$$

The total gain is 2.46 dB higher than the calculated gain using the parameters from the datasheet in Chapter III, Section C. The manufacturers usually provide the worst case tolerance values on the datasheet, and it is likely that the components used have better performance than nominal, which results in a slightly higher gain.

The maximum and minimum input signal power levels for the ADC are 22 dBm and –11 dBm as computed in Chapter III, Section B1. By subtracting the gain of each stage from the maximum and minimum input signal power levels at the ADC, we get the maximum input power at the synthesizer as approximately –33 dBm, which is denoted by

the blue plot, and the minimum input power is approximately –66 dBm, which is denoted by the red plot in Figure 35.

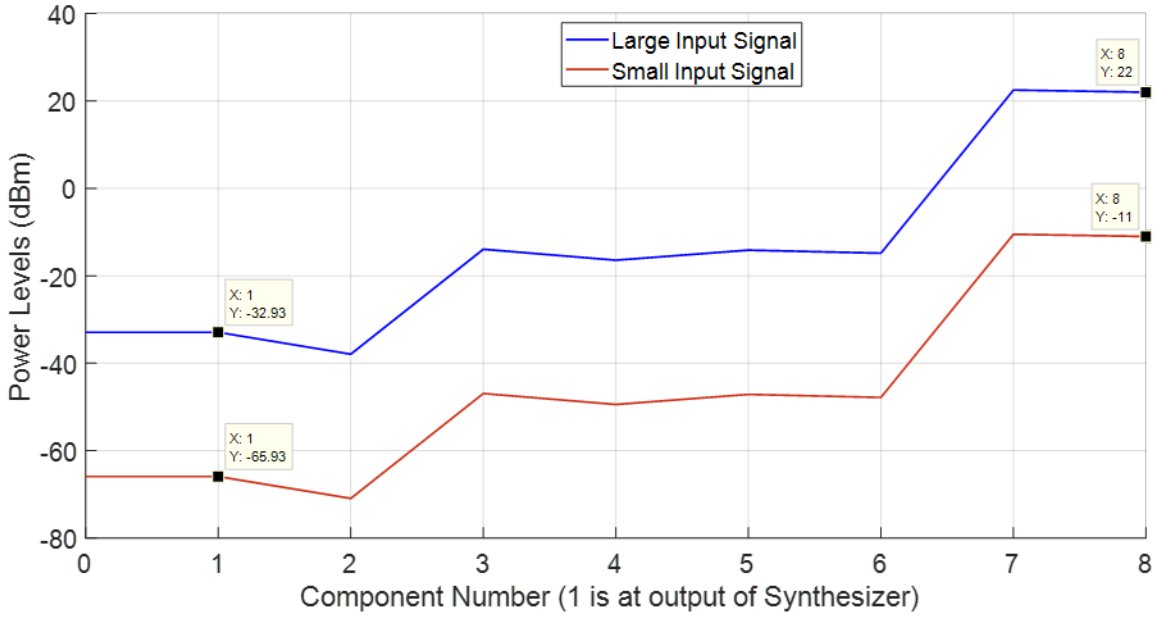


Figure 35. Maximum and Minimum Input Signal for Injection Mode

The minimum and maximum gain values from the plot do not include the antenna gain of 11.5 dB. If we include the antenna gain, the maximum input power is –33 – 11.5 = –44.5 dBm, and the minimum input power is –66 – 11.5 = –77.5 dBm. These values are close to the values computed in Chapter III, Section C, which listed the maximum input power as –43 dBm and minimum input power as –75 dBm.

When the synthesizer output power is set to –66 dBm, the amplitude of the input signal to the ADC after passing through the entire receiver chain is measured as –9.83 dBm as shown in Figure 36. This falls within the ADC dynamic range of between 22 dBm and –11 dBm.

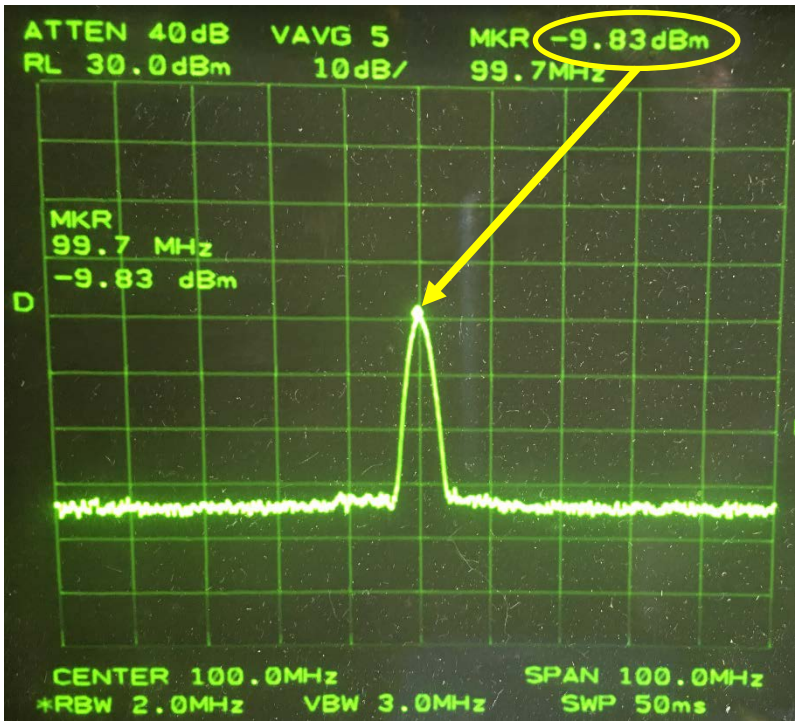


Figure 36. Power Measurement at ADC Input with Synthesizer Output Power Set to –66 dBm

Another critical measurement is the SNR of the input signal. The SNR must meet the requirement of no less than 13.5 dB at the input to the ADC. Although there is other equipment for measuring the noise floor and SNR of the signal, we use the spectrum analyzer to measure the signal power and the average noise floor for SNR computation. The resolution bandwidth (RBW) of the spectrum analyzer relates to the effective bandwidths use by the filters inside the spectrum analyzer in calculating both power of the signal or noise floor. Due to the limitation of the spectrum analyzer, the highest RBW is only 2.0 MHz. The desired RBW is 20.0 MHz as denoted by the radar instantaneous bandwidth in Table 2. The difference between a RBW of 2.0 MHz and 20.0 MHz is ten times, or 10.0 dB; therefore, the measured noise floor power using the spectrum analyzer with a RBW of 2.0 MHz can be converted to a RBW of 20.0 MHz by adding 10.0 dB to the measured value. The SNR of the measurement is 32.83 – 10 = 22.83 dB as shown in Figure 37. This is larger than the 13.5 dB minimum SNR requirement at the ADC input.

The SNR being greater than the required SNR of 13.5 dB is expected since the signal power (–66 dBm) into the receiver is larger than the MDS.

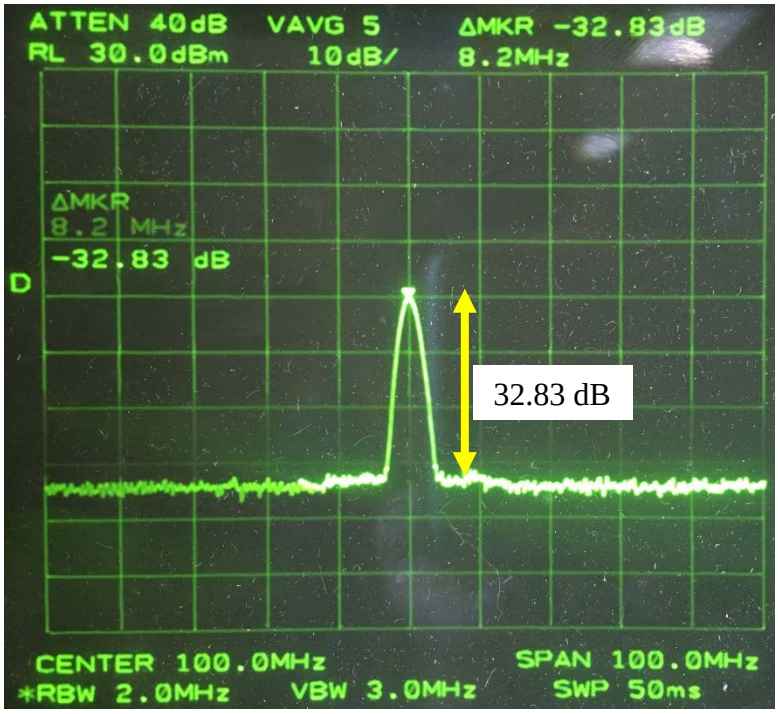


Figure 37. SNR Measurement at ADC Input with Synthesizer Output Power Set to –66 dBm

D. ADDING ADDITIONAL LNA TO MEET MDS REQUIREMENT

In order to meet the requirements of the MDS (–81.3 dBm), there is a need to have an additional gain of approximately –77.5 – 81.3 = 3.8 dB. An additional LNA of the same model is added in the RF stage to design an experiment with input at MDS. The LNA has a gain of 24 dB and is more than enough to amplify the signal.

With the additional gain provided by the LNA, we were able to reduce the input signal from the synthesizer to –82 dBm. This is the MDS computed earlier. Reduction of input signal power relative to the noise floor has the equivalent effect of lowering the SNR. Stated another way, the noise floor is amplified relative to signal power, which is shown in Figure 38. The measured SNR is 24.5 – 10 = 14.5 dB as shown in Figure 39. This is still

better than the 13.5 dB SNR requirement at the input to the ADC. Recall that the factor 10.0 dB is used to account for the RBW adjustment.

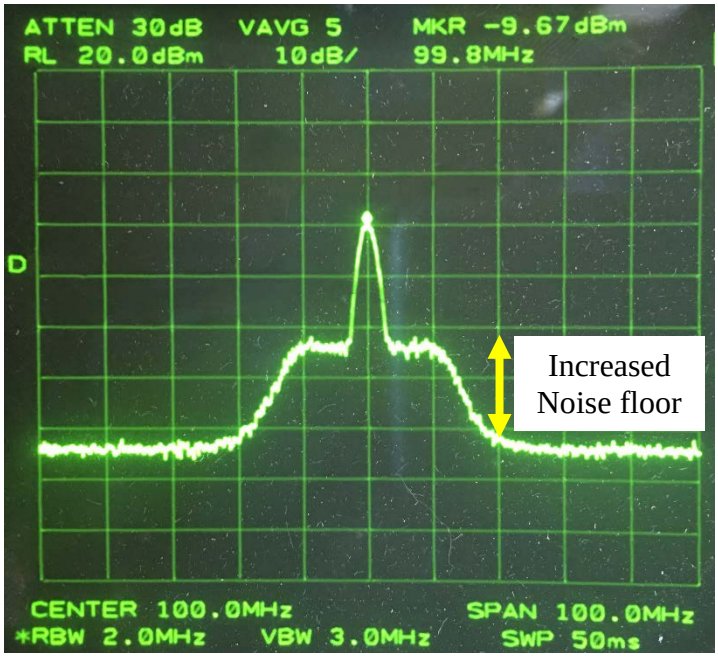


Figure 38. Increased Noise Floor Due to Additional LNA

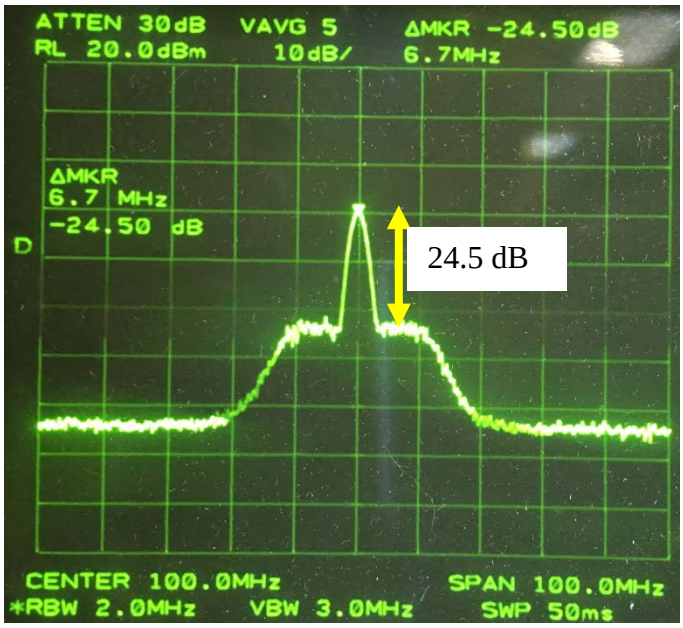


Figure 39. SNR Measurement at ADC Input with Minimum Input Signal Power

E. DIGITIZED SIGNAL OUTPUT

The ADC output is shown in Figure 40. The display shows the frequency domain plot and is similar to the output display of a spectrum analyzer. The x-axis denotes frequency, and the y-axis denotes amplitude in dBV. The ADC output matches the spectrum analyzer output in amplitude.

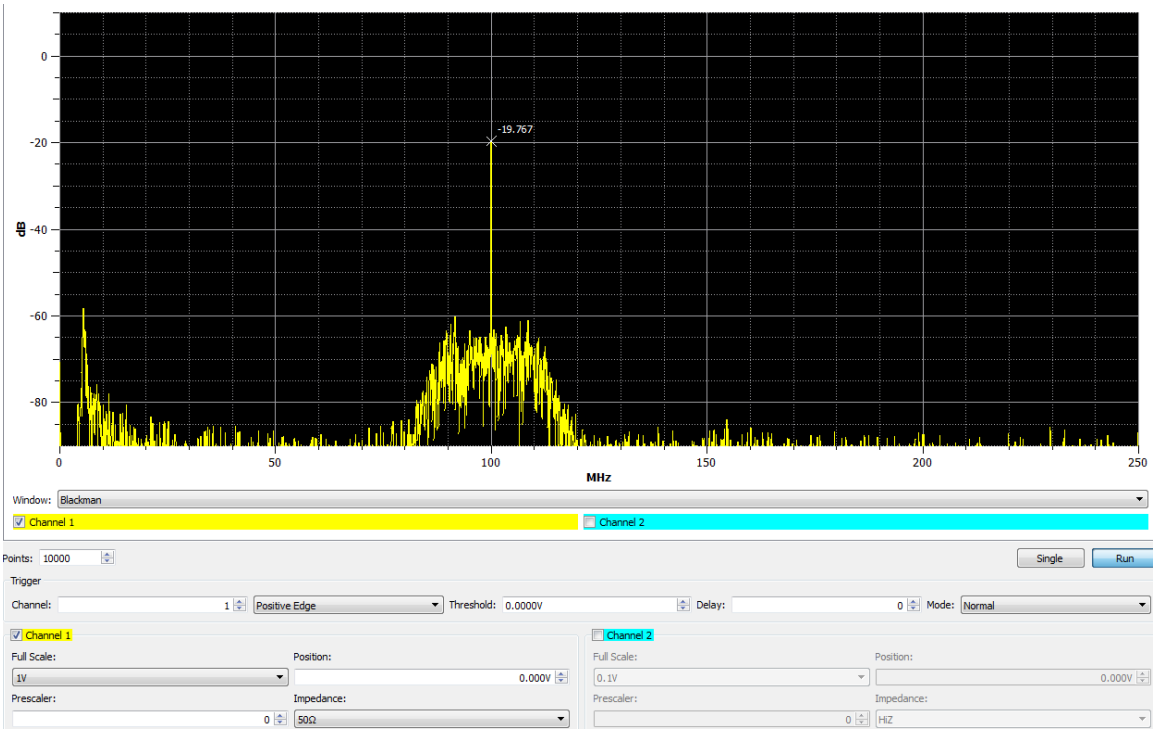


Figure 40. ADC Output Shown on the Keysight Software

F. PROPOSED CUSTOMIZED RECEIVER DESIGN

The proof-of-concept RF receiver front end was shown to meet the system requirements. A two-stage RF down-conversion design was proven to work. The customized design is shown in Figure 41. The diagram only shows a single receiver channel. This design must be duplicated 144 times to accommodate the 144 receive elements in the actual antenna array.

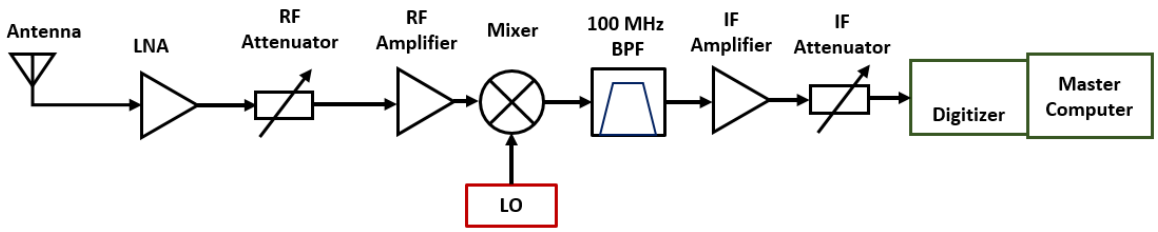


Figure 41. Customized RF Receiver Front End

The specifications of the system can be translated into component design requirements as tabulated in Tables 14 to 21.

Table 14. LNA Requirements

LNA parameters	Value
Operating frequency range	19 to 26.5 GHz
Noise figure	< 4 dB
Gain	20 dB
P1dB	20 dBm

Table 15. RF Attenuator Requirements

RF attenuator parameters	Value
Operating frequency range	19 to 26.5 GHz
Attenuation step	0.5 dB
Attenuation range	0 dB to 80 dB
P1dB	20 dBm

Table 16. RF Amplifier Requirements

RF amplifier parameters	Value
Operating frequency range	19 to 26.5 GHz
Noise figure	< 10 dB
Gain	20 dB
P1dB	20 dBm

Table 17. Mixer Parameters

Mixer parameters	Value
RF / LO frequency range	19 to 26.5 GHz
IF frequency range	0 to 1 GHz
Conversion loss	< 10 dB

Table 18. 100 MHz BPF Parameters

IF BPF parameters	Value
Center frequency	100 MHz
Instantaneous 3-dB bandwidth	20 MHz
Passband attenuation	< 2 dB
Stopband attenuation	–65 dBc at 100 MHz away

Table 19. IF Amplifier Parameters

IF amplifier parameters	Value
Operating frequency range	DC to 1 GHz
Noise figure	< 10 dB
Gain	40 dB
P1dB	20 dBm

Table 20. IF Attenuator Parameters

IF attenuator parameters	Value
Operating frequency range	DC to 1 GHz
Attenuation step	0.5 dB
Attenuation range	0 dB to 80 dB
P1dB	20 dBm

Table 21. Digitizer Parameters

Digitizer parameters	Value
Input frequency	0 to 250 MHz
Sampling rate	500 MSa/s
Input voltage range (50Ω)	125 mV_{pp} to 8 V_{pp}

G. CHAPTER SUMMARY

An overview of the COTS hardware was presented in this chapter. The actual receiver hardware implementation was described and a test methodology was presented. Both RF and IF BPF frequency responses were characterized, and the test results were within the required specifications. In order to eliminate external interference and signals from affecting test results, injection mode testing was used to test the receiver chain. The cumulative gain, noise floor, and SNR of the receiver were measured and met the required specifications of the system. An additional LNA was added to the test setup to show that the MDS requirement could be met. Due to the non-availability of the COTS parts for the transmitter, we were not able to assemble and verify the performance parameters for the transmitter section.

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VI. CONCLUSION AND RECOMMENDATION

A. SUMMARY AND CONCLUSION

The objective of this thesis was to design and build a proof-of-concept RF front end using COTS modules, analyze the system performance, and suggest improvements for subsequent custom hardware implementation to enable integration of multiple functions into a common mast. In the thesis, we presented different types of RF front ends, their associated architecture, design considerations, and constraints. Parameters for the LPI radar were obtained and used to design the transmitter and receiver RF front end. Performance analysis was conducted using MATLAB calculations, and actual COTS hardware modules were selected. Results indicated that the COTS ADC dynamic range was between 22 dBm and –11 dBm. The MDS was computed to be –81.3 dBm with a designed receiver noise figure of 6.21 dB and a requirement to have a SNR of 13.5 dB at the ADC. A gain of approximately 70 dB was required for the RF receiver front end. That was achieved using a two-stage super-heterodyne design. Injection mode testing was performed, and the measurement results closely mirrored the MATLAB computation in the performance analysis section.

Unfortunately, only the receiver components arrived in time for assembly and testing. The transmitter was designed but not tested. A customized receiver design was proposed with the parameters tabulated for subsequent follow up design.

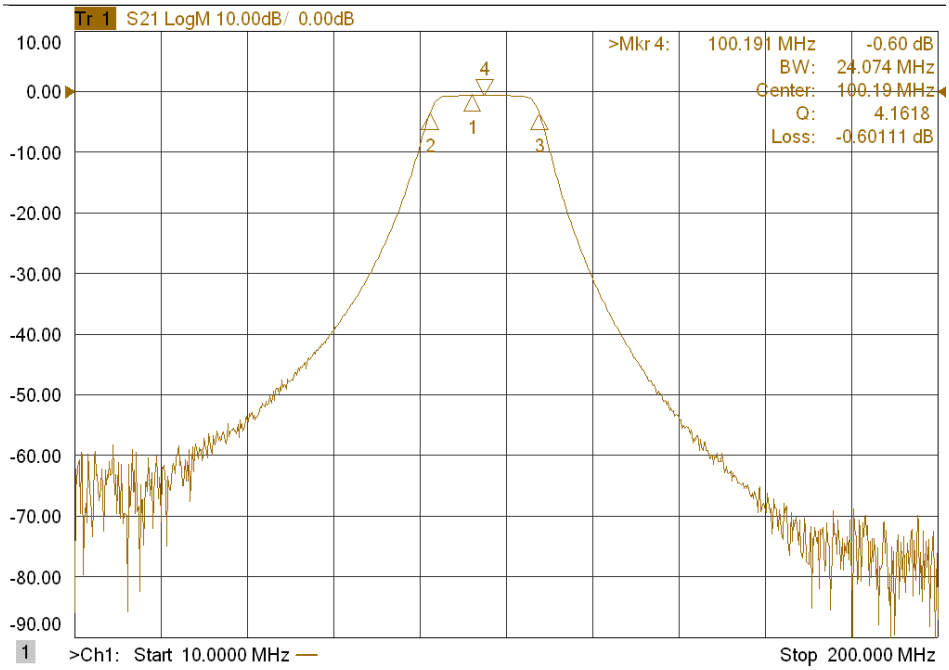
B. FUTURE WORK

It is necessary to assemble, test, and verify the actual COTS hardware for the transmitter design to ensure that the design is workable when the parts arrive. In addition, we need to perform phase measurements between two receive channels to characterize the phase error for LPI phase array beam forming. This can be performed in two parts: the first part uses injection mode testing to prevent environmental factors from affecting the measurement; the second part uses actual antennas for over the air transmission in an anechoic chamber for more realistic measurements. We also need to integrate the RF front end to the master computer for digital signal processing. We can also extend the RF front

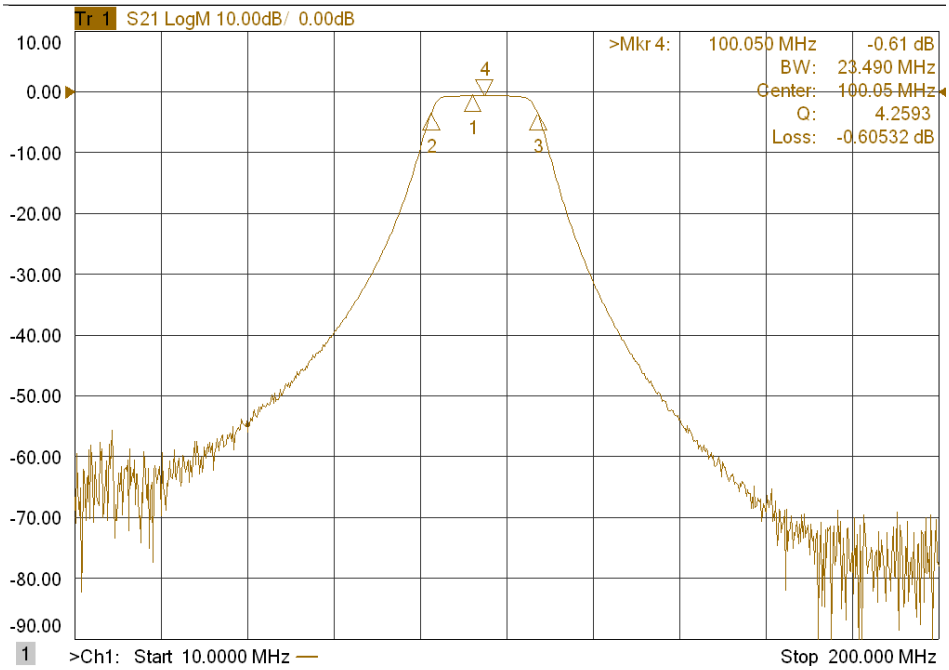
end design to incorporate the communications and EW capability function to verify that the same design can be used. The next phase is to actually build a hardware prototype for implementation.

APPENDIX. IF BPF FILTER RESPONSE PLOTS

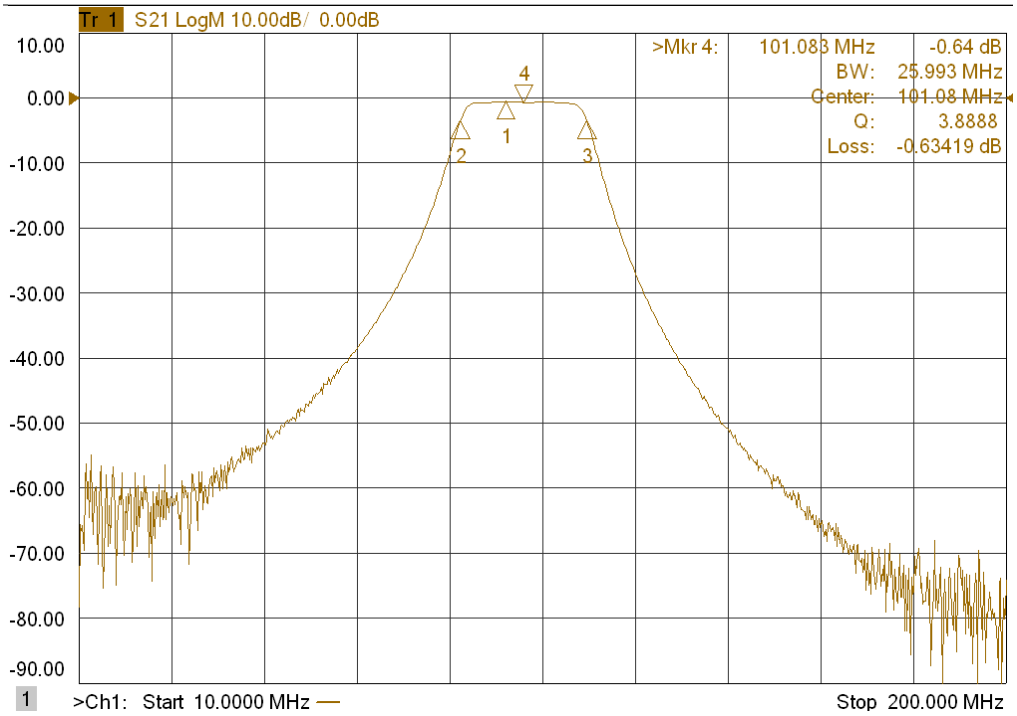
A. IF BPF (S/N 2)



B. IF BPF (S/N 3)



C. IF BPF (S/N 4)


Tr 1 S21 LogM 10.00dB/ 0.00dB
>Mkr 4: 101.083 MHz -0.64 dB
BW: 25.993 MHz
Center: 101.08 MHz
Q: 3.8888
Loss: -0.63419 dB
10.00
0.00
-10.00
-20.00
-30.00
-40.00
-50.00
-60.00
-70.00
-80.00
-90.00
1
>Ch1: Start 10.0000 MHz
Stop 200.000 MHz

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