REPORT DOCUMENTATION PAGE

Form Approved OMB NO. 0704-0188

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1. REPORT DATE (DD-MM-YYYY)	2. REPORT TYPE	3. DATES COVERED (From - To)
01-06-2018	Final Report	1-Aug-2017 - 31-Jul-2018

4. TITLE AND SUBTITLE

Final Report: High-Speed Cryogenic Optical Connector for Focal Plane Array Read-out

5a. CONTRACT NUMBER

5b. GRANT NUMBER
W911NF-17-P-0048

5c. PROGRAM ELEMENT NUMBER
665502

6. AUTHORS

5d. PROJECT NUMBER

5e. TASK NUMBER

5f. WORK UNIT NUMBER

7. PERFORMING ORGANIZATION NAMES AND ADDRESSES

SDPHOTONICS LLC
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8. PERFORMING ORGANIZATION REPORT NUMBER

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS (ES)

U.S. Army Research Office
P.O. Box 12211
Research Triangle Park, NC 27709-2211

10. SPONSOR/MONITOR'S ACRONYM(S)
ARO

11. SPONSOR/MONITOR'S REPORT NUMBER(S)
71371-EL-SB1.1

12. DISTRIBUTION AVAILIBILITY STATEMENT

Approved for public release; distribution is unlimited.

13. SUPPLEMENTARY NOTES

The views, opinions and/or findings contained in this report are those of the author(s) and should not contrued as an official Department of the Army position, policy or decision, unless so designated by other documentation.

14. ABSTRACT

15. SUBJECT TERMS

16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT	15. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON
a. REPORT	b. ABSTRACT	c. THIS PAGE			Dennis Deppe
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RPPR Final Report
as of 11-Jun-2018

Agency Code:

Proposal Number: 71371ELSB1 **Agreement Number: W911NF-17-P-0048**
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Report Date: 31-Aug-2018 Date Received: 01-Jun-2018
Final Report for Period Beginning 01-Aug-2017 and Ending 31-Jul-2018
Title: High-Speed Cryogenic Optical Connector for Focal Plane Array Read-out
Begin Performance Period: 01-Aug-2017 **End Performance Period:** 31-Jul-2018
Report Term: 0-Other

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Distribution Statement: 1-Approved for public release; distribution is unlimited.

STEM Degrees: **STEM Participants:**

Major Goals: The goals of this SBIR project are to develop a cryogenic optical data link to be used with focal plane array readouts of military cameras. The optical data link uses a new type of oxide-free, lithographic VCSEL that can reach the needed reliability and bit energy to increase the camera efficiency and establish the capability of very high speed data extraction for existing and future cameras. These improved cameras are expected to have greater pixel counts and faster frame rates than now possible.

Our Phase I goals have been to demonstrate the cryogenic operation of the lithographic VCSEL and study its temperature characteristics, and establish the optical data connection from the cryostat to the detector outside the cryostat. Both free space and fiber optic connectors have been studied, both of which provide viable routes to the cryogenic optical data link.

Accomplishments: The accomplished are given in the uploaded pdf file provided in the final report format. The accomplishments include the design, epitaxial growth, fabrication and testing of the successful demonstration of the lithographic VCSEL designed for 77 K operation. A wide operating temperature range has been demonstrated from room temperature to 77 K with low threshold obtained over the full regime.

Along with our collaborator Ultra Communications, Inc., we designed the mask for the VCSEL pad layout to flip chip the laser onto Ultra Comm's μTX platform. This platform enables options for use of either an optical fiber or a free space connection through an optical window. Ultra Comm has identified cryogenic optical fiber feed throughs for a robust connection based on multimode fiber coupling. To fully eliminate the need for fiber, the Ultra Comm μTx and μRX platforms enable free space coupling through the optical window to eliminate thermal contact between the cryostat and data connection.

In addition, we have analyzed the electrical readout requirements for the focal plane array hybridized onto a silicon platform. This will be included in a Phase II proposal to be submitted on this project.

Training Opportunities: Training was performed on the Phase I of two sdPhotonics engineers in cryogenic VCSEL design and testing.

Results Dissemination: In addition to monthly reports, several briefings were made of the progress on the project. Analysis has been performed of the cryogenic VCSEL speed potential and a conference submission to the SPIE Photonics West 2019 conference.

RPPR Final Report
as of 11-Jun-2018

Honors and Awards: Nothing to Report

Protocol Activity Status:

Technology Transfer: We are working with Ultra Communications to develop commercial high speed VCSELs based on the lithographic technology for insertion into various military platforms. The advantages of the lithographic VCSEL include very high reliability to meet military specifications and very low bit energy, due to size scaling of the laser. We plan to work with at least one DoD laboratory on the project, and have been contacted by a second laboratory at the AFRL Kirtland Air Force base who is also interested in the technology.

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Person Months Worked: 1.00 **Funding Support:**
Project Contribution:
International Collaboration:
International Travel:
National Academy Member: N
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Project Contribution:
International Collaboration:
International Travel:
National Academy Member: N
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Final Report

(1) Foreword

Cryogenic optical data links can play a valuable role in reducing the power consumption and increasing bandwidth of cryogenic systems for cameras and computing systems. The vertical-cavity surface-emitting laser (VCSEL) provides an important route to a high speed, low cost, compact and efficient solution for such applications. Because of their small size, VCSELs can meet or beat the electrical power draw required by silicon photonics solutions such as microdisk modulators. However the VCSEL solution can produce very high optical coupling efficiency of ≤ 0.5 dB loss into optical fiber. In contrast, small silicon photonics modulators average ~20 dB optical loss making them all but impractical to reach an overall efficiency close to VCSELs.

VCSELs also have the advantages that they enable low loss optical coupling when used as a free space interconnect or an optical fiber interconnect. A free space link can produce fully thermal isolation of the data connection from the cryogenic environment of a camera to the external electrical connections to image processing and displays. The VCSEL requires only a high-speed detector external to the camera as described in this report. Silicon photonics modulators in contrast require a tunable laser external to the cryostat to inject the optical signal into cryogenic modulator. The tunable laser is needed to match the resonance condition of the modulator. In addition, another fiber or fiber splitter is needed to extract the modulated optical signal. Therefore the VCSEL can provide an unbeatable advantage in cost, size, weight and power (CSWAP), the motivating factor in the development of much of the military technology.

This Phase I project has studied a new type of lithographic and oxide-free VCSEL designed for cryogenic operation along with its insertion into cryogenic cameras. The lithographic VCSEL eliminates oxide reliability problems and can be scaled to very small size to achieve very low bit energy. The study shows the important trend in threshold reduction from room temperature to 77 K, and analysis and electrical data show very high modulation speed and ultra low bit energy can be expected for further development. The project reports measured results on the cryogenic lithographic VCSELs fabricated in this Phase I along with an analysis of threshold and differential gain, and the scheme for insertion of the technology into the camera in a collaborative effort with the sdPhotonics subcontract Ultra Comm. Some experimental data is also provided on room temperature modulation characteristics verifying that 10 Gb/s and much greater data speed should be easily achieved for this cryogenic VCSEL link.

(2) List of Illustrations and Tables

Figure

Table

(3) Statement of the Problem Studied

There is a growing need for development of a high-speed optical data link to enable transfer of optical data from cryogenically cooled focal plane arrays (FPAs). The optical link can eliminate or reduce cooling loss due to the thermal connection that results from the wiring needed for electrical data feed-through. In this SBIR sdPhotonics LLC has performed a Phase I effort to study provide development of a low power, high-speed oxide-free VCSEL source with high reliability optimized for cryogenic operation. Although oxide VCSELs are now predominantly used in high speed optical data interconnects, these lasers have reliability problems due to cooling to the cryogenic temperature needed for the cryogenic optical data link. This Phase I effort has instead relied on a new type of lithographic VCSEL that is oxide-free. Instead the VCSEL uses an epitaxial aperture that achieves comparable or greater optical mode confinement and electrical confinement to exceed the oxide VCSEL performance for small aperture sizes. Preliminary data has shown that this new lithographic VCSEL can dramatically improve the laser reliability while also improving performance. Data rates demonstrated to date exceed 10 Gb/s at 95 C even in non-optimized devices. The cryogenic VCSEL source can be integrated with free space optics, high-speed detectors, and high-speed laser drivers and transimpedance amplifier (TIA) to provide a complete optical connector for the transfer of optical data from the cryogenic dewar systems. The optical connector can be designed to interface with focal plane readout circuitry and complete the data link. Ultra Comm has participated in the Phase I and has advanced microoptic components and package integration needed for the cryogenic optical connector. Ultra Comm also has cryogenic test capabilities to enable high speed testing in a Phase II of the cryogenic data link based on the new VCSEL technology.

The SBIR project targets development of both a free space link for cryogenic readout, and a multimode optical fiber cryogenic data link. The free space is illustrated in Fig. 1. The approach centers on using micro-transmitter (μTX) and micro-receiver (μRX) components [1-4]. The μTX utilizes a VCSEL as shown in Fig. 1 in the cryostat interior. The μRX will be aligned through a cryostat window. Figure 1 shows a possible fixture of the μTX and μRX components that can be optically enclosed to avoid dust or other contamination. Additional configurations of the μTX and μRX components are also possible and will be studied in the SBIR. The μTX and μRX have numerous advantages and include the VCSEL, microlens, application specific integrated circuit (ASIC), and electrical interconnections and contact pads. The μRX replaces the VCSEL with a high speed detector. UltraComm has novel technology for the μTX and μRX components for this project.

In the Phase I effort sdPhotonics designed and tested a cryogenic lithographic VCSEL and developed a high-speed design to be developed in a Phase II. The cryogenic design requires the cavity and gain region of the VCSEL to be spectrally matched at the desired cryogenic temperature for the data link, or ~ 77 K. The high-speed design developed in the Phase I targets minimizing internal electrical parasitics and uses a special type of implant to reduce capacitance and resistance in key places in the VCSEL.

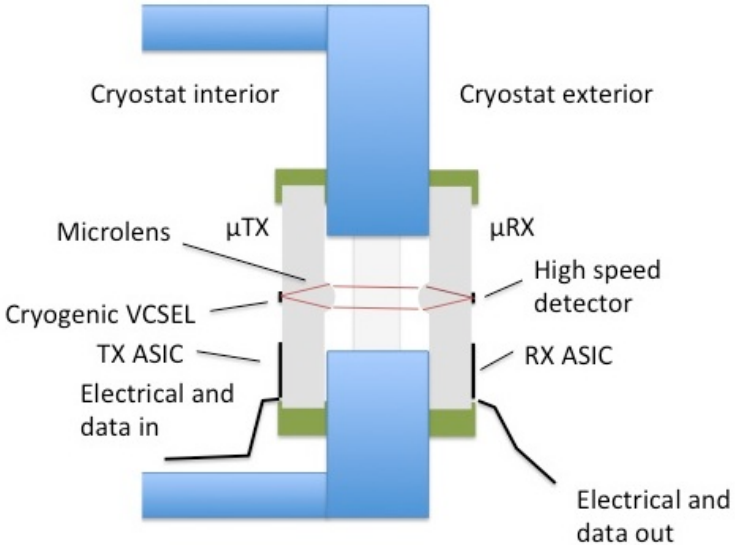

Fig. 1 Configuration for a free space high speed optical interconnect transmitting through a cryostat window. The optical link uses a µTX component inside the camera cryostat and a µRX link outside to extract the optical data.

Ultra Comm's µTX and µRX optoelectronic components have been tested utilizing oxide VCSELs for temperatures down to ~ 150 K. To reach cryogenic temperatures the commercial off the shelf (COTS) oxide VCSEL now used in the µTX must be replaced with a custom cryogenic VCSEL design. Part of the problem with COTS oxide VCSELs is that their design for room temperature and higher requires a cavity design poorly tuned for cryogenic operation. However another problem with the COTS oxide VCSEL is its poor reliability at the cryogenic temperatures because of increased thermal stress in the semiconductor cavity caused by the oxide aperture.

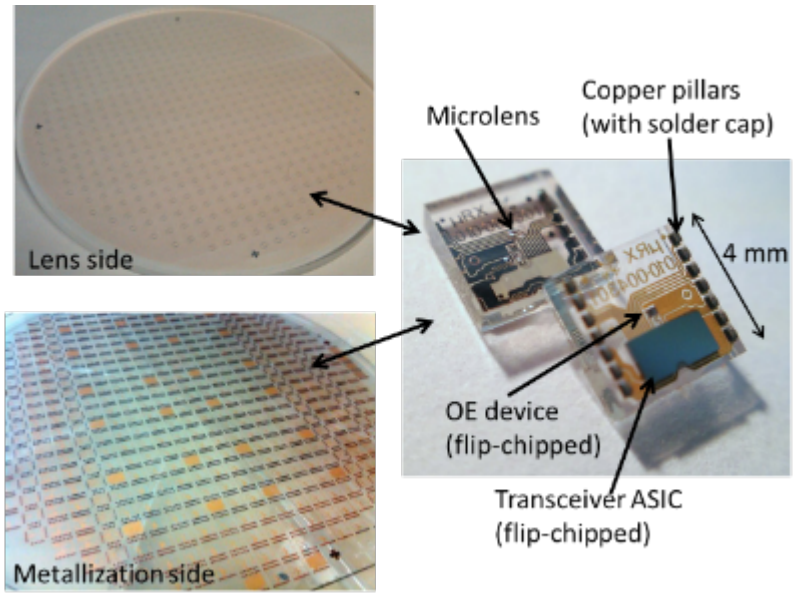

Fig. 2 UltraComm's µTX component for its free space optical interconnect. The transmitter including ASIC and coupling lens measures 4 x 4 mm^2.

(4) Summary of the most important results

The Phase I technical objectives for the base project are given below.

Table 1. Tasks and Technical Objectives	
Tasks	**Technical Objectives**
1. (Base) Design and growth of VCSELs for cryogenic operation. (SP)	Develop and produce VCSEL design for 77 K operation.
2. (Base) Package and lens design of μTX for cryogenic operation and distance. (UC)	Develop μTX and μRX lens and package for integration with lithographic VCSEL.
3. (Base) Cryogenic testing of VCSEL. (SP)	Optimized performance at ~ 77 K.
4. (Option) VCSEL mask and pad layout for high speed and flip-chip integration into μTX. (SP, UC)	Supply of cryogenic VCSELs for integration into a cryogenic μTX in an Phase II effort.
5. (Option) ASIC design for integration with focal plane array read out circuitry. (UC)	Develop electrical interconnection and data transfer from focal plane array readout to μTX.
6. Final report. (SP)	Provide a summary of the Phase I results.
Responsibilities: SP = sdPhotonics, UltraComm = UC	

The first three tasks in Table I were completed in the Phase I. The approach for task 2 was discussed above and a more complete discussion can be found in the reports and briefings presented to the Army. Here we present the measured results of the cryogenic VCSELs at room temperature and low temperature to verify the impact of cavity tuning. For cryogenic operation, the lithographic VCSELs have been designed with a spectral offset of the cavity resonance that is shown in Fig. 3. This design accounts for the difference in the temperature dependent spectral shift for the cavity resonance relative to the quantum well gain region. This temperature dependent spectral shift is ~0.7 nm/K for the cavity resonance but ~3 nm/K for quantum well gain peak. Therefore the cryogenic VCSEL should be designed with a cavity resonance and quantum well to obtain spectral alignment at the desired temperature of the 77 K as shown in Fig. 3. The Phase I effort included this key feature of the design, and epitaxial growth, VCSEL fabrication and testing were completed in the Phase I to verify and study the cryogenic operation over temperature.

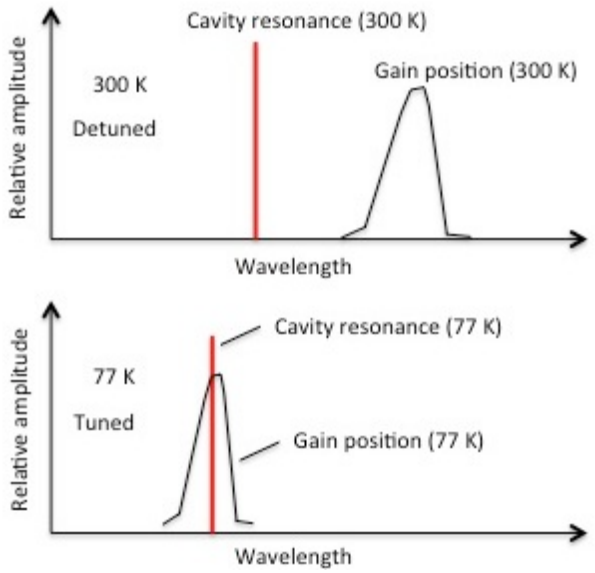

Fig. 3 Plots illustrating cryogenic VCSEL design to obtain high performance at 77 K. The spectral detuning at room temperature must account for thermal shift between the cavity mode and gain position to bring these into resonance at 77 K.

Threshold and differential gain benefit dramatically from cooling for a properly tuned VCSEL. The threshold decreases as k_BT, while the differential gain increase as $1/(k_BT)$. The result is that the bit energy for a properly tuned VCSEL can also be dramatically reduced for the 77 K operation. The actual VCSEL operation can occur over a very wide temperature range and this range may be increased for the lithographic design. Operation from above room temperature down to temperatures as low as 4 K and possibly below.

In our testing lasing was obtained over the full range of testing from room temperature down to 79 K. All lasing occurred with low threshold. The cavity can also be further optimized for low bit energy when the design is matched for the needed speed. A 10 Gb/s VCSEL for example can use a relatively high quality factor laser cavity. The threshold can then be reduced over that of a higher speed design. Since the differential gain also increases at the cryogenic temperature, the VCSEL bias current can be much lower than for room temperature. We also include some results from room temperature operation of very small VCSELs, and these promise extremely low bit energy. Based on room temperature results for high speed VCSELs, we expect that optimized devices can be reduced to ≤ 1 fJ.

A range of sizes was tested and measured results are presented below for a 6 μm diameter device. The VCSELs were mounted on an open TO header for insertion into a liquid nitrogen cooled cryostat as shown in Fig. 4. The wire bond was made to a large Au contact pad shown on the right in Fig. 4. The measurements show several important results. These include:

1. CW room temperature operation of the VCSEL tuned for 79 K, and low threshold operation from 79 K to 300 K. This enables the optical link to be operated at room temperature to verify operation prior to cooling.

2. Low threshold operation of a 6 μm diameter VCSEL of ~ 200 μA at 79 K. This low threshold and the results described below show that a very low bit energy data link is possible.

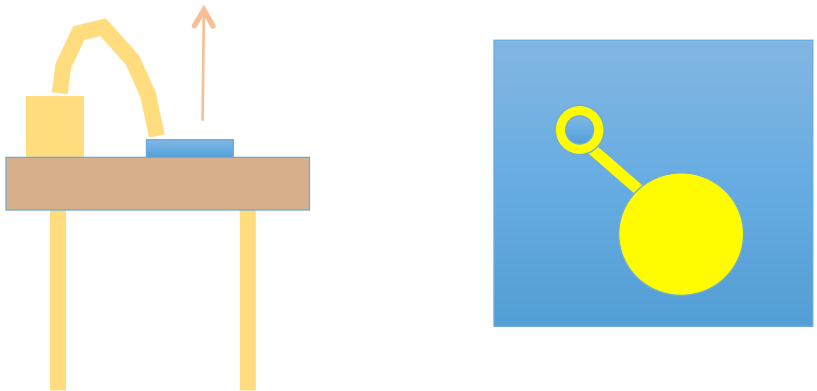

Fig. 4 Left shows a schematic illustration of the VCSEL mounting. On the right is a diagram of a single VCSEL test pad with aperture size ranging from 1-6 um and center to center spacing of 250 um between individual devices.

The measured results are shown in Fig. 5. On the left is shown the light vs. current curves for the VCSEL at 300 K and 79 K. The threshold decrease between room temperature and 79 K can be seen with the cryogenic design. We note that this VCSEL design and epitaxial growth were not yet fully optimized for the cryogenic operation. The results though show the importance of cavity resonance tuning at the 79 K to obtain optimal performance for cryogenic operation. The decrease in lasing threshold tracks K_BT.

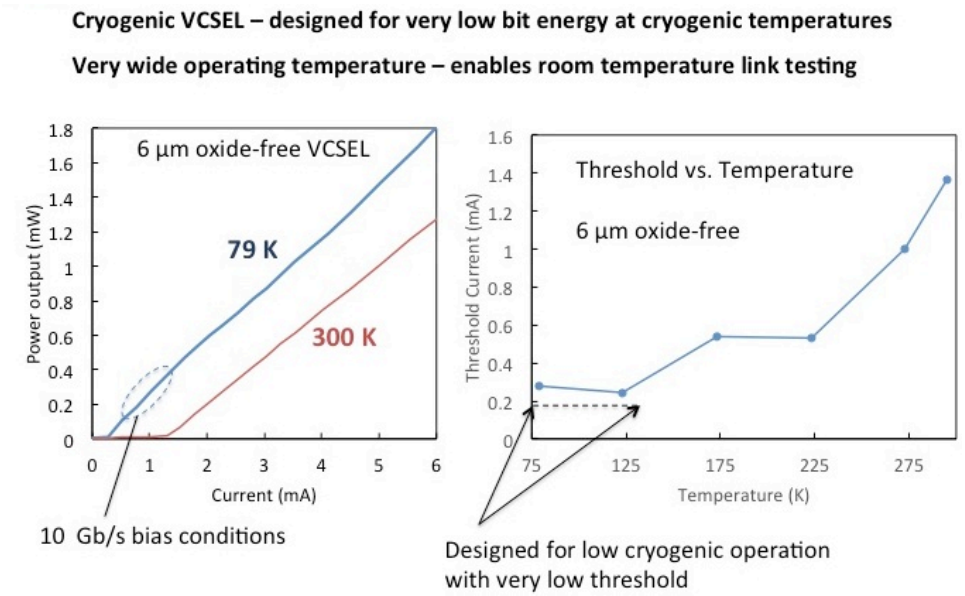

Fig. 5 79 K and 300 K L-I's showing the threshold decrease with temperature. The dashed region shows the bias currents projected to produce > 10 Gb/s.

Past work on the lithographic VCSELs is presented below showing that the lithographic single mode VCSEL can achieve high output power and reliability at room temperature [5]-[10]. These very small VCSELs are of interest to reach minimum bit energy. Some results at room temperature are shown in Fig. 6.

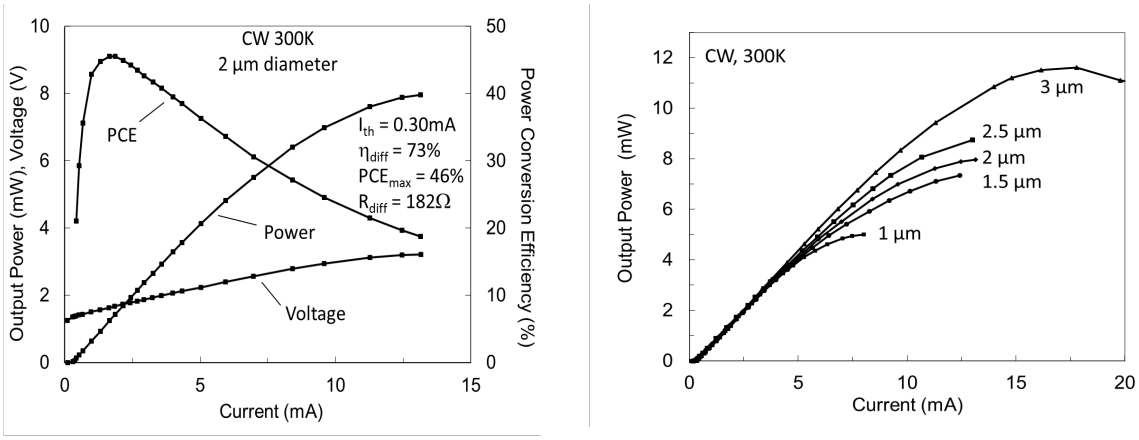

Fig. 6 On the left shows L-I-V measurements and the resulting key device characteristics. The graph on the right shows L-I characteristics for varying device sizes.

The reliability and output power of lithographic VCSELs are superior to that of oxide VCSEL's at room temperature. Under cryogenic conditions the lithographic VCSELs ouput

power will increase and retain high reliability when compared to the oxide VCSEL due to the internal strain caused by the oxide at cryogenic temperatures. The lithographic VCSEL becomes much faster with cooling as the threshold current decreases and differential gain increases. As a result of these qualities the lithographic VCSEL is capable of reaching very low bit energy under cryogenic conditions. Fig. 5 1 shows that the lasing threshold of the 6 μm VCSEL decreases to 220 μA at 79 K. However we know that this 6 μm device is not optimized yet, and the threshold can in fact be much lower.

Table 2 below tabulates the key device characteristics relative to device size.

Size (μm)	I_{th} (mA)	Pmax (mW)	Diff. Slope Eff.	PCE	J_{th} (kA/cm^2)
1.0	0.33	5.0	80 %	37%	42 kA/cm^2
1.5	0.31	7.3	77 %	42 %	17.5
2.0	0.30	8.0	73 %	46 %	9.5
2.5	0.28	8.7	80 %	47 %	5.7
3.0	0.32	11.6	76 %	49 %	4.5

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