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RPPR Final Report
as of 29-Oct-2018

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Major Goals: During this project several different test structures will be studied and compared. It is expected that the different samples will have different defect structures and defect densities. Analysis of these different test structures will be used to elucidate the defect formation mechanisms and study the evolution of defects. The overall trends can then be used to develop possible defect mitigation strategies. During this project, we will chose the best designs along the way in order to minimize the appearance of the types of defects that we already investigated, so that we can isolate and study the various defects (bulk, interface, point, surface, etc.). However, the main focus of this study is on the surface defects' origin. Finding the behavior of surface defects will help us to develop an effective surface passivation for T2SL-based photodetectors.

In this effort, surface defect delineation and mitigation strategies will be investigated in diode-based junctions. The comparison of surface behaviors between different structures (homojunction, heterojunction, barriered junctions), surface cleaning treatments, and passivation techniques (SiO2, polyimide, SANDs) will reveal the origin of defects, and correlate behaviors with the physical chemistry of the process. In parallel, capacitancevoltage and I-V measurements and modeling will be performed to extract the carrier lifetime, doping and mobility; which will be compared to the values found earlier in the bulk material to see how surface defects change the material properties. At the end of this effort, we expect to achieve a comprehensive understanding of defect mechanisms at the surface, construct a theoretical model to describe the processes, and obtain an optimal strategy to suppress the effect of surface defects and leakage in T2SL material.

Accomplishments: See Upload Section.

In conclusion, we established a method for theoretical analysis of surface states by taking a phenomenological approach to the measured dark current density. This method was applied in studying the influence of deposition of SiO2 by PECVD on the performance of LWIR barrier detectors. It was shown that oxide deposition passivates the dangling bonds and increases the trap energy level, however, it increases the trap density. Consequently the dark current is decreased at low (operation) bias voltages, while at larger applied bias the trap-assisted tunneling becomes dominant. Regarding the surface resistance, the SiO2 may either increase or decrease the value, as the experiment suggests both.
We discussed different characterization techniques for T2SL material, single photodetector processing procedures, and photodetector characterization techniques. Different dark current mechanisms and its optimization methods were discussed in detail. We also discuss how the responsivity and quantum efficiency are measured in Center for Quantum Devices, and how the transparency of the substrate and the front-side and back-side illumination can

affect the quantum efficiency. Besides that, the concept of capacitance-voltage and photoluminescence are also described.
By considering MOS capacitor concept, we are going to do the C-V measurement of the surface of the Type-II InAs/GaSb based superlattice. We also discusses how to transfer the gating technique from MWIR to LWIR. In the LWIR T2SL p-pi-M-n photodiode, gating technique also demonstrates its strong capability of eliminating the surface leakage current generated by SiO2 passivation. Minimizing the SiO2 thickness from 600nm to 10nm not only reduces saturated gated bias from -120 volt to -4.5 volt, but also confirms that the origin of surface leakage is from fixed charges at the SiO2/T2SL interface or within the very thin SiO2 passivation layer near the surface, and that a thicker SiO2 passivation layer will not further affect surface leakage current.
At 77K, the gated photodiode shows RA-100mV of 3071 cm^2, and detectivity of 7 x 10^11 Jones. Moreover, gated diode offers a much wider operation range than the photodiode without gating architecture. Most importantly, the gating technique reveals different surface leakage current mechanisms, which provides much deeper understanding of surface leakage current and facilitates further research work on surface leakage suppression.
On another stage of our research, the combination of the MWIR and AlAsSb/GaSb barrier were implemented to permit decreasing of the G-R dark current and at the same time to suppress the surface leakage current in order to have a reliable SiO2 passivation, compare to a degradation of several orders of magnitude with a MWIR barrier. Using this sample, a microjunction structure with 25µm mesa/10µm microjunction diode permits to decrease the dark current from 1.9x10^-5A/cm^2 to 6.3x10^-6A/cm^2, and to reach a 1.2x10^12cm.Hz^1/2/W. We also reported the use of a new photodetector structure, CpDBn, to improve passivation quality and suppress the G-R current. The barrier consists of a large bandgap (>1 eV) AlAsSb/GaSb barrier and an undoped MWIR barrier in order to reduce the G-R current by transferring the depletion region inside this second barrier. The large bandgap barrier is employed to suppress the surface leakage current and the G-R current. We also reported that the use of a microjunction structure further improves the electrical performances by reducing the bulk dark current originating from the junction area, especially the G-R current. A study of the bias dependence of optical performances of 5×5 µm^2, 10×10 µm^2 and 15×15 µm^2 microjunctions photodiodes for a 25×25 µm^2 mesa area combined with electrical measurement, shows an optimum microjunction photodiode structure of 25×25 and 10×10 µm^2 microjunction and mesa areas, respectively, which exhibits a dark current reduction of 3 times compare to the reference at quantum efficiency saturation bias. The structure increases the special detectivity value to 1.2x10^12 cm.Hz^1/2/W.

Training Opportunities: 4 post doctoral scholars, three graduate students, one undergraduate student, and a visiting pre-doctoral scholar (French) were sported by this grant. They received invaluable instruction while working on this grant. In particular an undergraduate student working on this project and obtained credit for his work in the lab. One PhD student also featured this work in his dissertation.

Results Dissemination: 5 peer-reviewed publications were published during this project. These publications have been hosted on the CQD website (http://cqd.eecs.northwestern.edu/) and made available for free (when allowable by copyright law). These results have also been featured at multiple conference presentations. The results have also contributed to one PhD dissertation.

Honors and Awards: 1. 2018 Franklin Instutute Gold Medal in Electrical Engineering
Awarded to Manijeh Razeghi

2. 2016 Best Student Oral Presentation Award-Devices
Awarded to Romain Chevallier

3. 2017 Summer Undergraduate Research Award
Awarded to Thomas Yang

4. Virginia Tech College of Engineering recognizes Manijeh Razeghi for delivering a Bradley Distinguished Lecture
Awarded to Manineh Razeghi

5. 2017 Jan Czochralski Gold Medal
Awarded to Manijeh Razeghi

6. Prix de la Chaire Saint Gobain
Awarded to Xun Victor Suo

7. 2016 IIN Outstanding Researcher Award
Awarded to Abbas Haddadi

8. EECS 2016 Best Dissertation Award
Awarded to Abbas Hadadi

9. Third Place at 2016 EECS Poster Session
Awarded to Thomas Yang

10. 2015 Optics and Photonics Education Scholarship
Awarded to Abbas Haddadi

11. Best Paper Award for the Breakthroughs in Human-Centered Research
Awarded to Andy (Guanxi) Chen

12. Northwestern University Terminal Year Fellowship
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13. Northwestern University Terminal Year Fellowship
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A Comprehensive Study of Surface Defects in Traditional Type-II InAs/GaSb Superlattices and Ga-free Type-II

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Abstract (limit 200 words):

This article serves as the progress report of the first quarter of year 2015 Leakage currents limit the operation of high performance type II InAs/GaSb superlattice-based photodiodes. Surface leakage current becomes a dominant limiting factor, especially for small pixel pitch focal plane arrays (< 25 μm), and must be addressed. Strategies for controlling surface leakage current include reduction of the surface trap state density, unpinning the Fermi level at the surface, and appropriate termination of the semiconductor crystal. This report focuses on influence of SiO_2 passivation of type II InAs\GaSb superlattice-based photodetectors on surface leakage current and, subsequently, total dark current density of the devices. Our analysis indicates that deposition of SiO_2 enhances the surface trap energy state level, which results in an improvement in device electrical performance under small bias voltages ($|V_{bias}|$<200mV). However, the dark current density increased under larger bias voltages as a consequence of increased surface trap density on oxide-semiconductor interface.

Key Words (Limit 5): Surface passivation, heterojunction, Type-II superlattice

1. Background and Motivation

Development of Type-II superalttice

Type-II InAs/GaSb superlattices (T2SLs) were first proposed by Sai-Halasz *et al.* in the 1970's.[1] These superlattices are formed by alternating InAs and GaSb layers over several periods (Figure 1). This creates a one dimensional periodic structure, like that of the periodic atoms in naturally occurring crystals. InAs and GaSb are two members of the 6.1Å family which have a similar lattice constant around 6.1Å. This close lattice matching enables growth of T2SL with very high material quality.

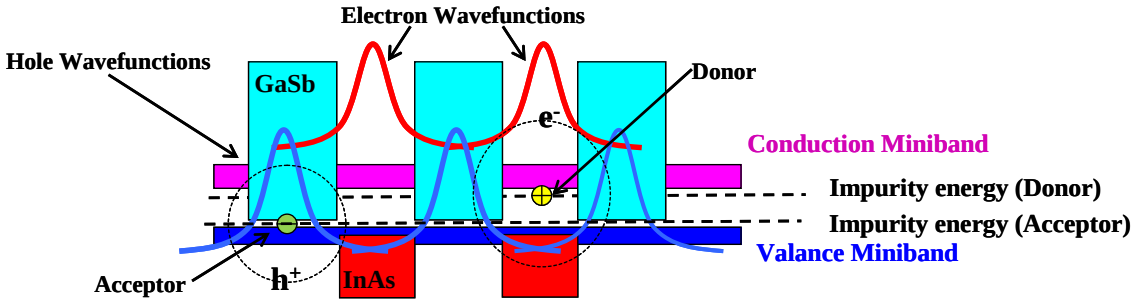

Figure 1 Spatial band alignment in Type-II superlattice (red regions represent InAs forbidden gap and cyan regions represent GaSb forbidden gap)

More importantly, the Type-II band alignment of the material (configuration in such the conduction band of InAs lies below the valence of GaSb (Figure 1) separation of electrons and holes into the InAs and GaSb layers, respectively. This charge transfer gives rise to a high local electric field and strong interlayer tunneling of carriers without the requirement of an external bias or additional doping. The resulting energy gap depends upon the layer thicknesses and interface compositions. In reciprocal space, the system is a direct-bandgap material with a high transition probability and a high optical absorption coefficient. This makes Type-II superlattices an attractive approach for realizing infrared photodetectors.[2]

In recent years, T2SL has experienced a drastic development, attaining a performance level comparable to state of the art MCT detectors.[3] Major advances in detector performance have enabled the demonstration of infrared focal plane arrays (FPAs) with excellent quality.[9, 20-21] However, these achievements to date only take advantage of the band gap tunability of T2SL, whereas this is a quantum mechanical material system and still offers quantum mechanical advantages that haven't yet been fully explored and utilized. For example, Auger recombination, which is a limiting factor for high temperature operation of infrared detectors, can be suppressed by manipulating the superlattice to control the band structure.[22] Compared to MCT and most other small band gap semiconductors that have very small electron and hole effective masses, the effective masses in T2SLs are relatively large, due to its superlattice design which involves the interaction of electrons and holes via tunneling through adjacent barriers. By

adjusting the superlattice design the effective masses can be increased further to reduce the tunneling current, which is a major component of the dark current in MCT detectors. Moreover, the capability of band structure engineering opens the horizon for exploring novel device architectures that are unthinkable using simple binary or ternary compound semiconductor band alignments like MCT. Recent research has proposed a novel variant of T2SL, the M-structure SL,[23] with large effective mass and large tunability of band edge energies.[11]

Despite the apparent and demonstrated advantages of the type-II InAs/GaSb material system, the issue of proper surface passivation is a topic of concern and needs to be properly addressed in order for type-II to surpass MCT as a state-of-the-art infrared detection technology. Unlike silicon, which has a natural, stable passivation of SiO_2, GaSb, InAs, and other III-Vs must be passivated by another means to reduce the surface state density and unpin the Fermi level from mid-gap, at the surface.

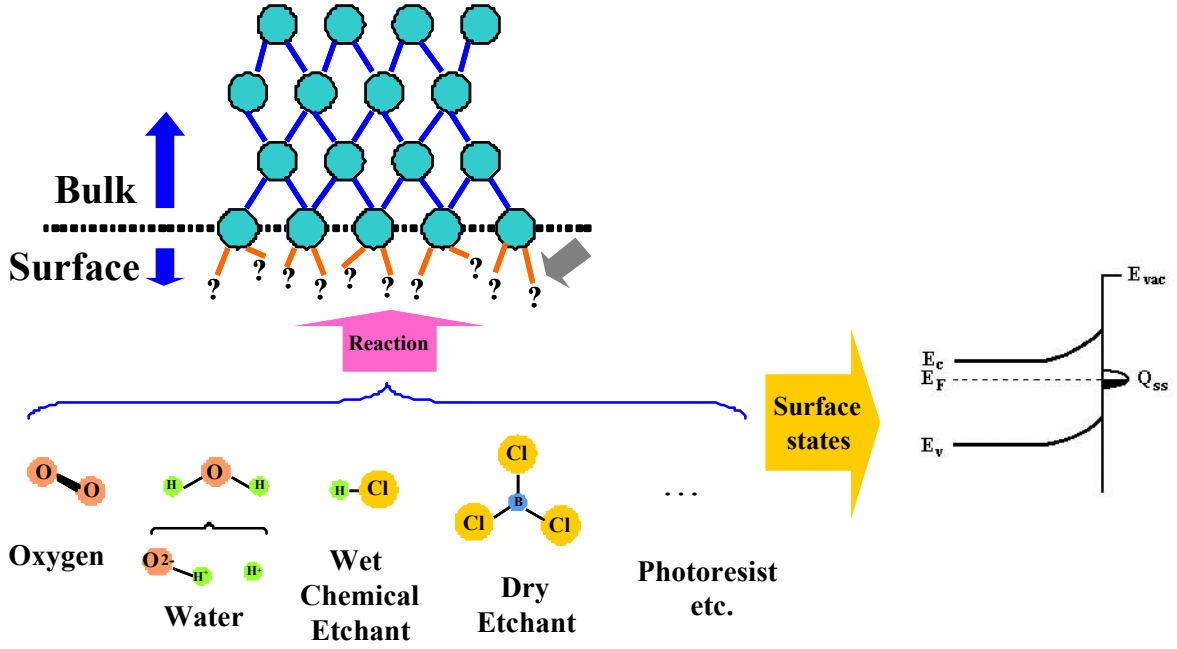

Figure 2 Abrupt termination of the semiconductor crystal causes dangling bonds that are improperly satisfied and introduce band bending at the surface.

The need to passivate photodetector devices stems from the abrupt termination of the semiconductor crystalline lattice at the semiconductor-air interface. When the periodic crystal structure is terminated at a surface, dangling or unsatisfied bonds remain and are highly reactive sites for the formation of native oxides and the bonding of contaminants (photoresist, etch by-products, water, etc.). The introduction of chemical compounds with properties different than that of the semiconductor material causes a band-bending at the surface and has a tendency to pin

the Fermi energy level at mid-gap. This phenomenon is illustrated in **Error! Reference source not found.**.

Due to the location of the Fermi level, increased trap-assisted tunneling and generation-recombination (G-R) current can result. Such an increase in reverse-bias currents is manifested in a reduction of the differential resistance-area product, a critical parameter for achieving high-detectivity photodiodes.

In some photodiode applications, some surface leakage current due to surface states is acceptable as it does not degrade the overall device performance too much. In typical photodiodes, surface effects are not readily observed in the current-voltage (IV) characteristics of large dimension devices; 100s of microns in diameter, for example. But as device sizes are shrunk in order to increase density and resolution such as in focal plane array pixels (< 30 μm × 30 μm), the ratio of the diode perimeter to the bulk's cross-sectional area increases and surface effects become more pronounced.

A simple electrical model of the photodiode, when discussing surface effects, can be considered as two resistors in parallel. One resistor, R_{bulk}, represents the bulk resistance of the device. R_{bulk} is solely dependant upon intrinsic material parameters. The other resistor, $R_{surface}$, represents all surface-related contributions to the overall device. Such a model is illustrated in Figure 3.

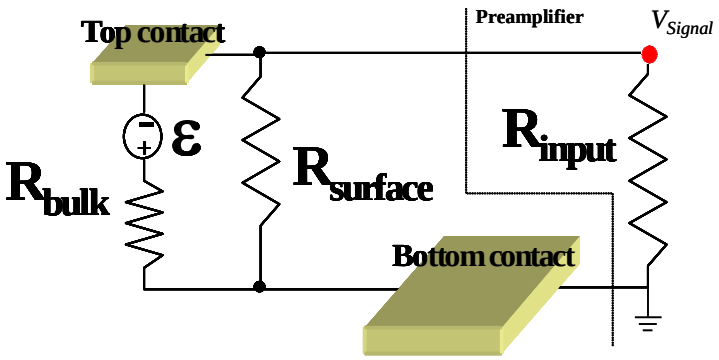

Figure 3 Simple two, parallel resistor electrical model of a photodiode.

The two, parallel resistor electrical model can also be represented by the following expression:

$$\frac{1}{R} = \left[\frac{1}{R_{bulk}} + \frac{1}{R_{surface}} \right], \qquad \text{Equation 1}$$

where R_{bulk} varies linearly with device thickness, d, and sidewall length, a, as

$$R_{bulk} \propto \frac{d}{a}. \qquad \text{Equation 2}$$

$R_{surface}$, on the other hand, varies quadratically with sidewall length, assuming the device height remains constant, as

$$R_{surface} \propto \frac{d}{a^2}. \qquad \text{Equation 3}$$

As discussed previously, depending on the resistivity coefficients in front of the dimension terms for both R_{bulk} and $R_{surface}$, R_{bulk} will dominate at large device dimensions. But as device dimensions scale down, there is a point where, after which, the surface resistance component begins to dominate as the surface area of the device begins to become more considerable than the volume. This concept is shown graphically in Figure 4.

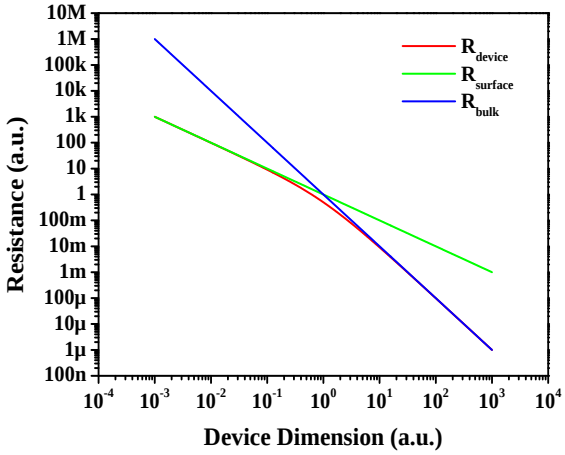

Figure 4 Device resistance as a function of device dimension. At large dimensions, the bulk (blue) resistance dominates the device resistance (red). At small device dimensions, the surface resistance (green) will dominate the overall resistance.

Most development of high-performance type-II infrared detectors is done with the goal of focal plane array (FPA) imaging in mind. FPA pixel sizes tend to be on the order of 20-30 µm and well within the regime where the surface plays a major role in the overall resistance of the device. It is for this reason that surface passivation is so important for the realization of next-

generation, high-performance focal plane array imaging systems using the type-II material system. We will later discuss techniques for measuring the effectiveness of a particular passivation technique at different length scales with variable area diode analysis.

In this work we focus on determining the dark current mechanisms involved in the electronic performance of type-II superlattice-based photodiodes with appropriate modeling and post-measurement curve fitting. The surface resistance value is deduced from the experimentally measured dynamic resistivity of the photodiodes. The devices are then passivated by SiO_2 deposition using plasma-enhanced chemical vapor deposition (PECVD), and re-measured to investigate the influence of passivation method on dark current performance and surface resistance.

Theoretical modeling of dark current

1.2.1. Dark current mechanisms in a type-II superlattice photodetector

Type-II superlattice photodiodes are junction-based devices, with the distinction of a superlattice (SL) structure substituting the bulk materials. Usage of the SL provides a degree of freedom in engineering the band gap to detect certain wavelength of the incident optical signal. The electronic performance of these SL based photodiodes follows the physics of well-understood p-n junctions. The photodiodes operate at a reverse applied bias voltage. In this regime, the contributing dark current mechanisms that are considered are diffusion current from the field-free region of the device, generation-recombination current from the depletion region, coherent band-to-band tunneling current, and trap-assisted tunneling (TAT) current. The TAT current is believed to originate from defect energy levels, such as those introduced by surface states.

The generation-recombination current density is expressed as

$$J_{GR} = \frac{en_i d(V)}{\tau_{GR}} \frac{\sinh(-eV/2k_bT)}{e(V_{bi}-V)/2k_bT} f(b), \qquad \text{Equation 4}$$

$$f(b) = \int_0^\infty \frac{du}{u^2 + 2bu + 1}, \quad \text{and} \quad b = \exp\left(\frac{-eV}{2k_BT}\right) \qquad \text{Equations 5-6}$$

where n_i is the intrinsic carrier concentration, d(V) is the depletion width as a function of bias voltage, e is the electron charge, k_b is the Boltzmann constant, T is temperature, τ_{GR} is the generation-recombination carrier lifetime, and V_{bi} is the built-in potential.

Diffusion current density is expressed as

$$J_{diff} = n_i^2 \sqrt{ek_bT}\left(\frac{1}{N_A}\sqrt{\frac{\mu_e}{\tau_e}} + \frac{1}{N_D}\sqrt{\frac{\mu_h}{\tau_h}}\right)(e^{eV/k_bT} - 1), \qquad \text{Equation 7}$$

where N_A is the acceptor concentration, μ_e and μ_h are the electron and hole mobilities, respectively, and τ_e and τ_h are the electron and hole carrier lifetimes, respectively.

The band-to-band Zener tunneling current density is expressed by the following:

$$J_T = \frac{e^3 F(V) V}{4\pi^2 \hbar^2} \sqrt{\frac{2m_T}{E_g}} \exp\left(-\frac{4\sqrt{2m_T E_g^3}}{3e\hbar F(V)} \right) \qquad \text{Equation 8}$$

where, F is the electric field, ħ is Planck's constant, m_T is the tunneling effective mass, and E_g is the bandgap energy.

The analytical equation for trap-assisted tunneling current density is

$$J_{trap} = \frac{e^2 m_T V M^2 N_t}{8\pi\hbar^3} \exp\left(-\frac{4\sqrt{2m_T (E_g - E_t)^3}}{3e\hbar F(V)} \right) \qquad \text{Equation 9}$$

where N_t is the trap density, M^2 is a matrix element associated with the trap potential, and E_t is the trap energy location.

1.2.2. Determination of surface resistance from the I-V characteritics

Performing a dark current modeling, and also extracting the surface resistance from the experimental I-V data provide notable insight into the effectiveness of any passivation method. If we take the parallel resistor electrical model, describe in Sec. 1.1, and introduce area and perimeter dependent terms, the device R_0A product can be expressed as

$$\frac{1}{R_0 A} = \left[\frac{1}{(R_0 A)_{bulk}} + \frac{1}{r_{0,surface}} \left(\frac{p}{A} \right) \right] \qquad \text{Equation 10}$$

where $(R_0A)_{bulk}$ is the bulk R_0A product, $r_{0,surface}$ is the dynamic surface resistance per unit length, p is the perimeter of the diode, and A is the cross-sectional area of the detector p-n junction. By plotting the inverse of measured R_0A product as a function of the perimeter to area ratio, the slope, if there is one, of the plotted points gives the surface resistance term, and thus information regarding the effectiveness of the passivation.

2. Work completed

Methodology

By applying our vast prior experience on the development of type-II superlattice based photodetectors, the best material structure is designed and grown that is optically functioning at long wavelength infrared regime. Reference single pixel devices with various sizes and shapes are then processed and electrically characterized. The dark performance is analyzed by applying the described theory to the experimental results. Upon verification of the established processing method, the exact same structure is passivated by deposition of SiO_2 by PECVD. The dark performance is again measured and the same theoretical analysis is applied to investigate the influence of passivation method. In order to verify the reliability of the analysis a second set of reference and passivated samples are designed, processed, passivated and analyzed.

Device design and material growth

In order to probe the influence of surface leakage current, it is essential to select the most appropriate device structure. For this purpose a material structure has to be selected that is more prone to the effects of the surface states:

a. In long-wavelength infrared (LWIR) photodetectors the surface current has a more dominant role, mainly due to the smaller band gap of the material.
b. Among various possible designs for the device, a heterjunction-based detector with the so-called 'M' barrier for blocking the generation-recombination current is selected as the primary choice. A p-π-M-n photodiode structure is the best candidate to study for surface leakage and passivation, because such structures can be designed to be diffusion-limited and surface current will be a major contributor to the overall dark current.

For the mentioned reasons, for the initial steps in this project the main focus is on passivation of LWIR p-π-M-n devices with InAs/GaSb superlattice. More complicated structures, i.e. nBn and pMp are going to be studied for the next phases of the project.

By applying these selection criteria, the structures were grown on GaSb (001) n-doped wafers by Intevac Modular Gen II molecular beam epitaxy system equipped with As/Sb valved cracker cells and Ga/In SUMO® cells. They all have the same device structures, consisting of a 0.5 μm thick GaSb:Si n^+ buffer, a 0.5μm InAs/GaSb:Si n^+ region, a 0.5μm InAs/GaSb M barrier, 2μm nid InAs/GaSb active region, a 0.5μm InAs:Be/GaSb p^+ region, and a 10 nm InAs:Be p^+ doped top contact layer. Material characterization with high resolution x-ray diffraction shows consistent SL periods with the theoretical values.

Device processing and passivation

Samples A and B were processed, as a reference, by using standard processing technique[4]. They were not passivated but were kept in vacuum chamber to minimize the exposure to ambient atmospheric conditions. The details of processing are as the following:

I. Substrate cleaning by Acetone-Methanol-Isopropanol

II. Optical lithography for mesa-isolation

III. Dry etching of the mesa by using an inductively-coupled plasma etching

IV. Post-etch cleaning by AZ400T stripper, acetone, methanol and isopropanol

V. Lithography for contact definition

VI. Deposition of contacts by e-beam evaporator

VII. Lift-off and subsequent cleaning similar to step IV

VIII. Placement of processed devices in vacuum to prevent exposure to atmosphere and enhance contaminant desorption from the surface and sidewalls. This may decrease the effect of surface on the dark current performance of the device.

To control the quality of process, the etch depth for the mesa were confirmed by using an optical profiler. Additionally the quality of the sidewalls was visually verified by acquiring high-resolution images using a scanning electron microscope. As indicated in Figure 5, the sidewalls are smooth, and free of visible defects. Furthermore, the corners of the square-shaped pixels are round to minimize the high-potential spots and the associated undesired current mechanisms.

The SEM images indicated a smooth sidewall and a round corner for the mesa.

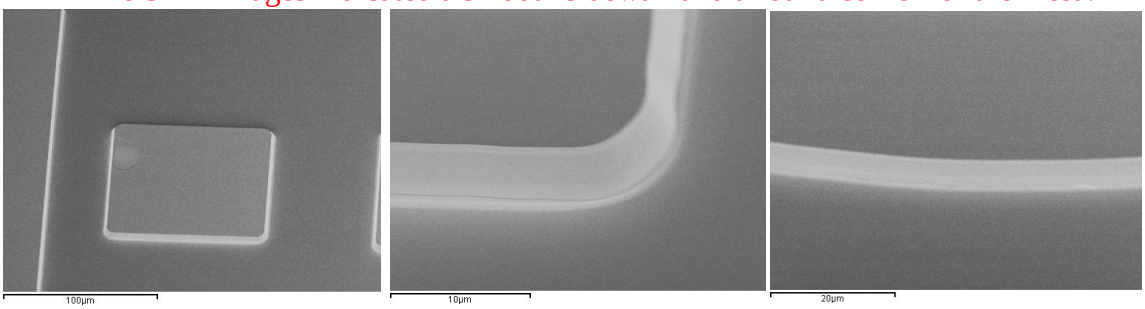

Figure 5 Verification of the quality of sidewalls after mesa isolation and cleaning

The optical characteristics of reference samples A and B were first measured in a Janis Liquid Helium cryostat at 77K. The quantum efficiency (QE) versus wavelength of each sample are shown in Figures 6a and 6b, for samples A and B, respectively. These results match with the calculated band gap based on the empirical tight binding model (ETMB)[24]. Specifically sample A has a cut-off wavelength of 11.5μm with QE=48%, and sample B has a cut-off wavelength and QE of 12μm and 54% respectively.

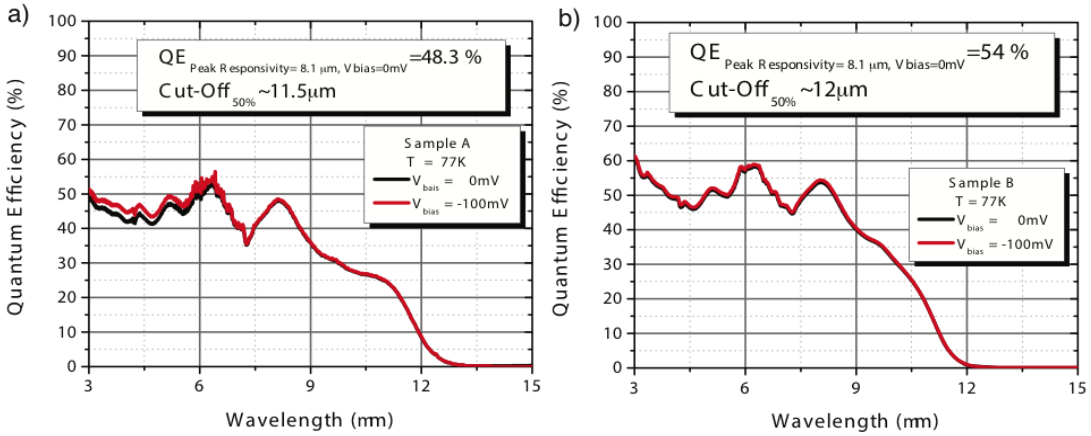

Figure 6 Quantum efficiencies measured at different applied bias voltages for a) Sample A, and b) Sample B. Both curves indicate no bias-dependency.

Measurement and analysis of dark current

2.4.1. Dark current measurement

All samples were measured in the Janis Liquid Helium cryostat at 77K by exactly the same way. The optical characteristics of all samples were first measured in a Janis Liquid Helium cryostat at 77K. The analysis of each sample was performed on sets of diodes with sizes from

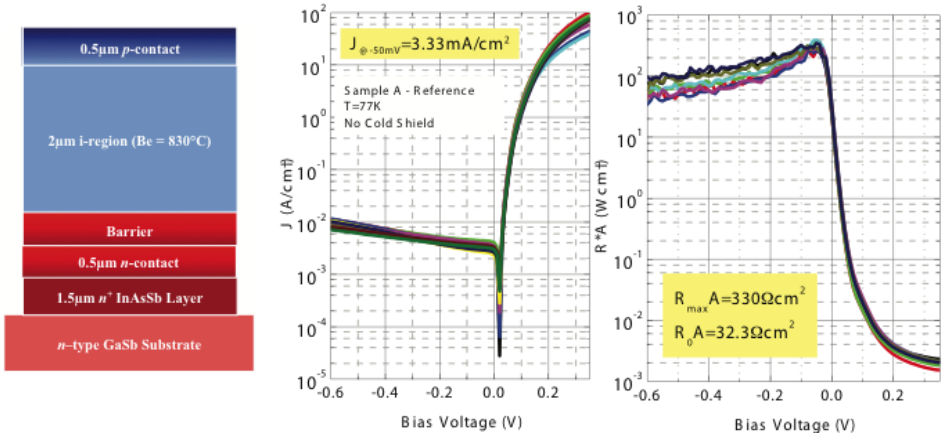

Figure 7 Layer structure (left), dark I-V (middle), and R.A vs voltage characteristics (right) for sample A. Various curves at each plot corresponds to different diode sizes on the sample.

100 x 100 μm to 400 x 400 μm.

Figure 7 indicates the layer structure of sample A, the measured dark current vs voltage, and the associated R.A curve. This sample has a dark current value of 3.33mA/cm^{-2} at -50mV of bias and a R_0A=32.3Ω.cm^2.

2.4.2. Extraction of dark current components

Four current components, and their constituent parameters, (Equations 4-9) are modeled using MATLAB scripting language. Carrier lifetimes, both G-R and diffusion, carrier concentrations, trap density, and trap energy are among the fitting parameters for current modeling.

Figure 8 indicates the I-V modeling of the reference sample A by fitting Equations 4-9 to the experimental data. The modeling indicates that the device is mainly limited by the diffusion current at the region of operation, V<200mV. An inspection of the diffusion current equations indicates that this current depends on constants and material properties such as intrinsic carrier and doping concentration. Hence for any sample that is diffusion limited, it can be concluded that the processing has had minimal effect on the dark-current performance of the device. This way we could verify that the established processing technique is indeed functional.

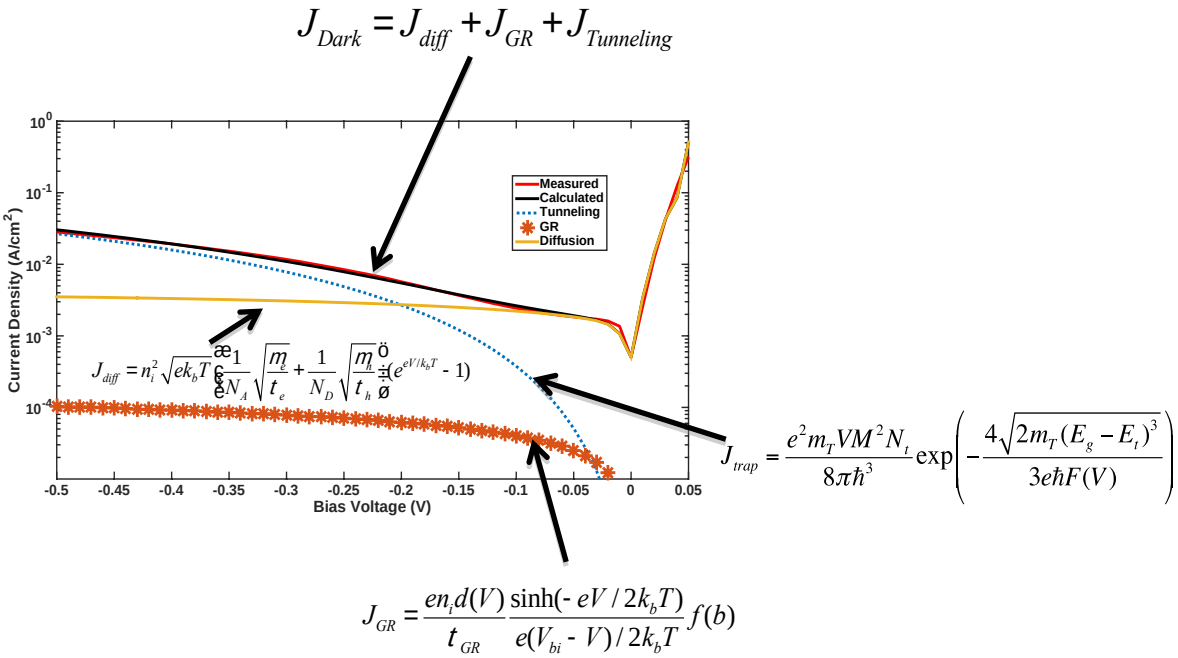

Figure 8 Measured and modeling of reference sample A, with inclusion of different contributing current mechanisms.

2.4.3. Influence of passivation on dark current

Upon verification of processing, the sample A was processed for addition of the passivation steps. Specifically, the following steps were taken to for this purpose:

I. Baking of the sample in vacuum for ~1.5 hours at 260°C. This step may assist on curating the damages on the sidewalls, caused by ICP dry etching, and would help on desorption of chemical contaminants.

II. SiO_2 was deposited on the processed sample by plasma enhanced chemical vapor deposition. The gases that were used during this step were SiH_4 and N_2O_3. The deposition temperature was 260°C, and the deposition thickness was 600nm.

III. Window opening: In order to have access to the metal contacts, a lithography and subsequent etching was performed to remove the SiO_2 right on top of the metal contacts. The etching was performed by an Oxford Plasma Lab 100 reactive ion etching system.

IV. Thorough cleaning of the photoresist was performed similar to previous cleaning steps.

Figure 7 indicates the layer structure of passivated sample A (Sample A-Pass), and the measured dark I-V and R.A. This sample exhibits a dark current density 2.6mA/cm^2 at the region of operation, which is less than the reference sample. The R_0A value is 31.5Ω.cm^2, which remains similar to the reference.

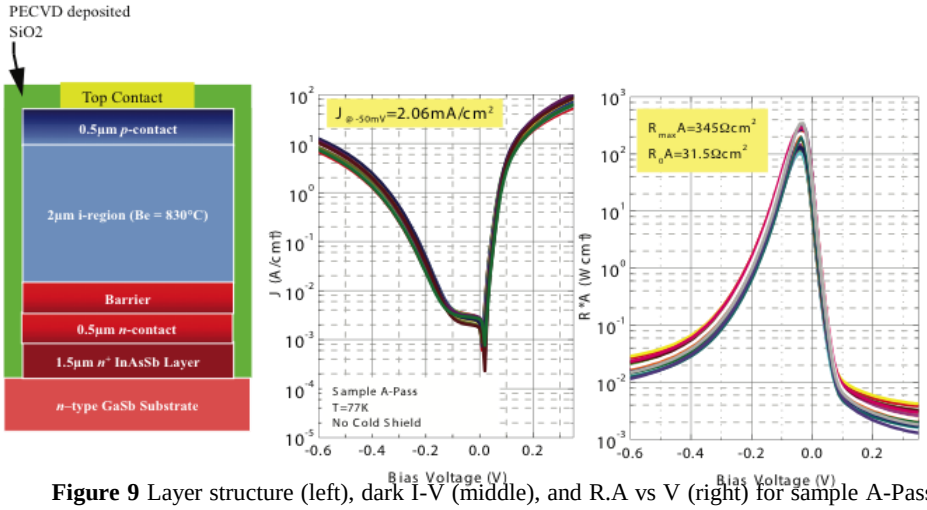

Figure 9 Layer structure (left), dark I-V (middle), and R.A vs V (right) for sample A-Pass. Various curves at each plot corresponds to different diode sizes on the sample.

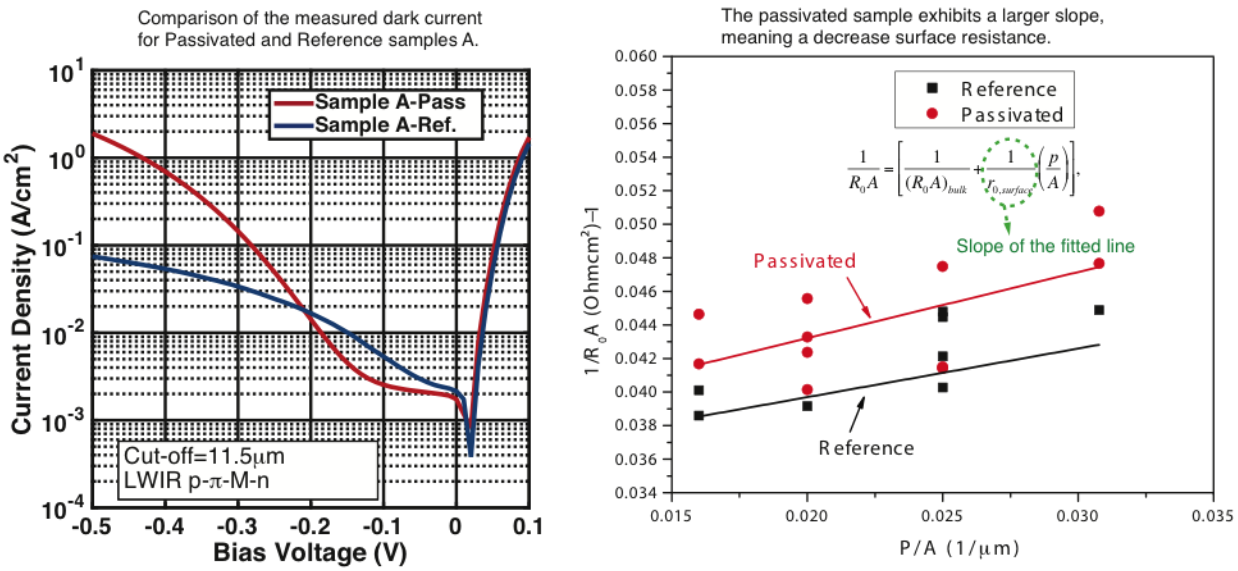

Figure 10 left) Comparison of the measured dark current density vs voltage characteristics for Samples A-Ref and A-Pass, and right) Line fitting for extraction of surface resistance for reference and passivated sample A.

Figure 10 compares the performance of the reference and the passivated samples. As it can be seen from the figure, the dark current for the passivated sample is less than that of the reference and in the region of operation: V_{bias}>-200mV. This, however, changes when the applied bias is increase, and the dark current for the oxide passivated device surpasses that of the other one. Examination of the plot of inverse of resistance vs P/A for both samples, indicate that the passivated sample has a larger slope, which by inspecting Equation 10, shows a smaller $r_{0,surface.}$This means the passivation of sample A was not effective in order to decrease the surface resistance. I-V modeling of the passivated sample presents further information on the changes in device behavior as a result of passivation.

Inspection of the I-V curves in of figure 10 signifies that for the sample A-Pass the contribution of the trap-assisted tunneling has significantly increased. A non-trivial fact, however, is the reduction of dark current at the region of operation despite the increased contribution of the trap-assisted tunneling current. This may be explained by inspecting the fitting parameters for the tunneling current. Table 1 indicates the fitting parameters for I-V modeling that were used in calculation of the TAT currents in the reference and passivated samples. It indicates that the trap density for passivated sample has drastically increased. At the same time, the difference between band gap and trap energy level in the passivated sample is enhance. These two changes are the determining factors in rate and level of increase in trap assisted tunneling current with an applied bias voltage.

Table 1 Fitting parameters for sample A, reference and passivated, used for I-V modeling

Fitting Parameter for I-V Model	Reference A	Passivated A
Trap Density N_t ($1/cm^3$)	$6.2x10^{12}$	$2x10^{17}$
Trap Level E_g-E_t (eV)	0.0114	0.0285

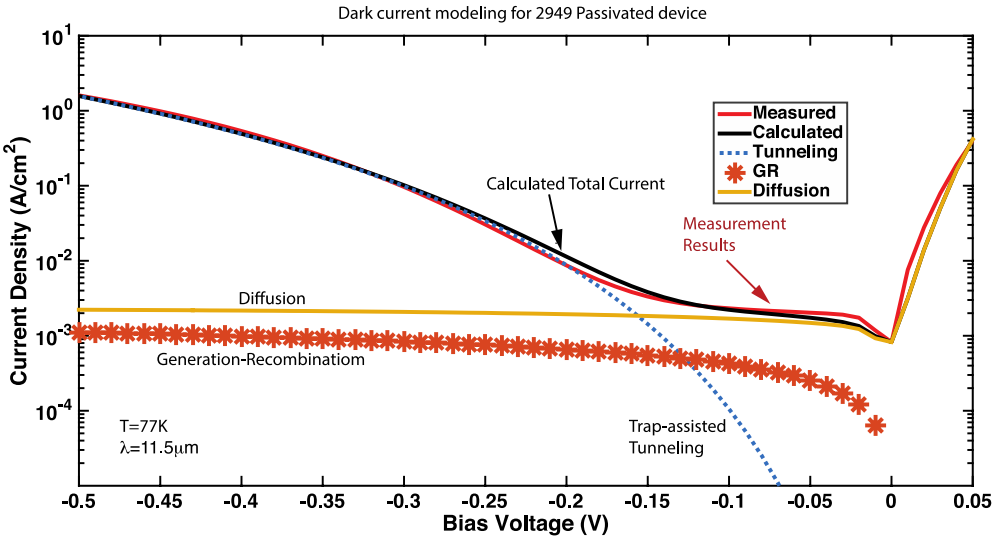

Figure 11 Fitting the dark current density mechanisms into the experimental results for sample A-Pass.

Equation 6 indicates that the trap assisted tunneling is **proportional to N_t**, which is the trap density, while it **exponentially decays with E_g-E_t**. Looking into the fitting parameters that are used for I-V modeling of samples A and A-Pass (Table-I), it is seen that for the passivated sample N_t has increased, while the trap energy levels are also enhanced. It is then concluded that the deposition of the SiO_2 passivates the surface by removing the dangling bonds and increasing the energy level of traps at the band gap, which decreases the probability of tunneling by enhancing the barrier level, hence decreasing the dark current at low bias voltages. At the same time, however, it also increases the trap density that destructively contributes to the dark current and becomes dominant only at larger bias voltages.

2.4.4. Verification of the hypothesis

In order to verify the results of the previous section and validity of the analysis, samples B, and B-Pass were processed, and passivated in identical steps as samples A, and A-Pass, respectively. Figure 12 shows the dark current performance and R.A for samples B and B-Pass. The dark current for the reference sample at -50mV of bias voltage is 1.92mA/cm^2 while at the same bias voltage, the passivated one incurs a dark current density of 1.36mA/cm^2, which indicates a reduction in dark current. Furthermore, the R_0.A value decreases from 18.0Ωcm^2 for the reference to 5.9Ωcm^2 for the passivated sample.

This batch of samples exhibits similar behavior as batch A. In the region of operation the dark current for the reference B and passivated B-Pass samples are 1.92 and 1.36mA/cm^2,

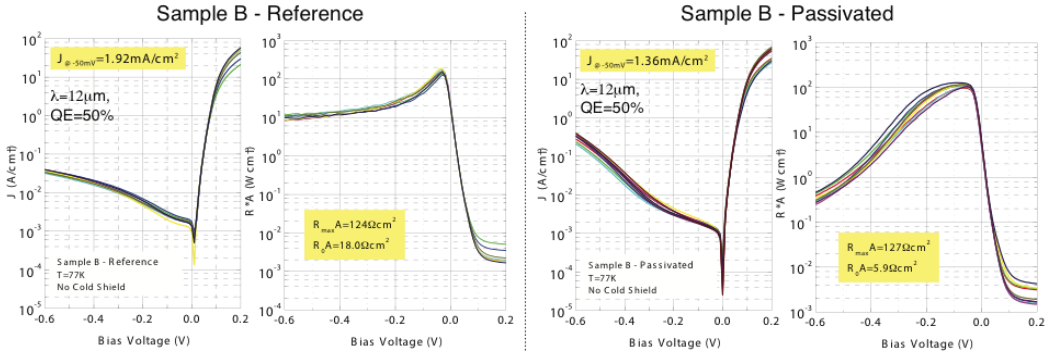

Figure 12 I-V and R.A-V for sample B reference (left) and B-Pass (right). Various curves at each plot corresponds to different diode sizes on the sample.

respectively, as can be seen in left side of Figure 13. Passivation, again, decreased the dark current value, at large bias voltages for the sample B-Pass the trap-assisted tunneling dominates Surface resistance may be extracted by fitting a linear curve to the $(R_0A)^{-1}$ vs P/A curve by following the discussions of Equation 10. In the case of sample B, the passivated sample has a smaller slope compared to the reference, which is an indication of increase of surface resistance. However, it can be seen from right side of Figure 13 that the intercepts of the fitted lines with the vertical access are different.

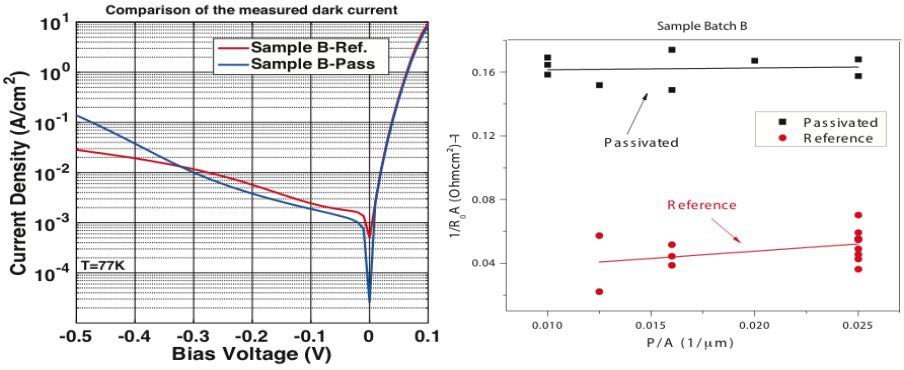

Figure 13 left) Comparison of the measured dark I-V for the reference and passivated sample B. Right) Extraction of the surface resistance from the $(R_0A)^{-1}$ vs P/A curve.

As a result the two samples exhibit different bulk resistances. Consequently, a thorough look into the dark-current fitting, as indicated in Figure 14.

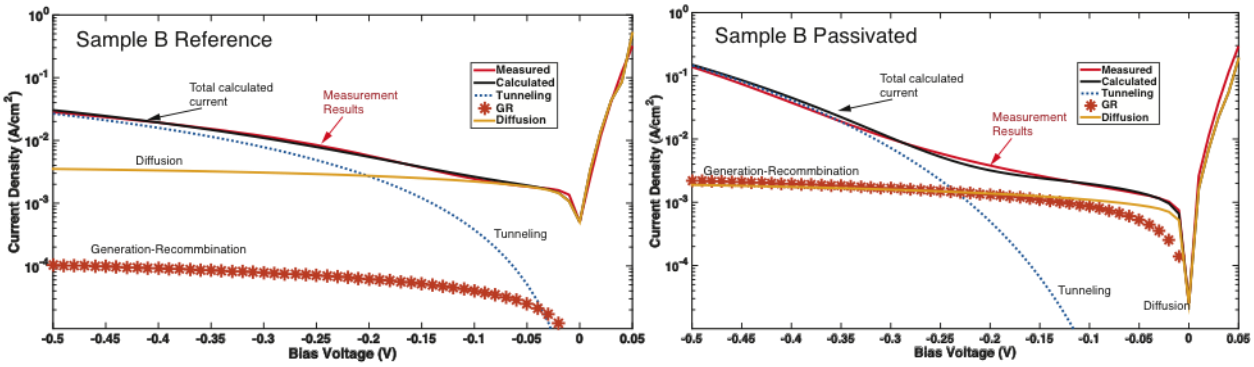

Figure 14 Fitting of the dark current mechansims into the experimental data for left) Sample B reference, and right) Sample B Passivated.

For the passivated sample, (Fig. 14 right) the trap-assisted tunneling becomes significant at large bias voltages, and is about an order of magnitude larger than that of the reference. At small bias voltages, howver, the TAT current is much less than that of the reference. The fitting values used for the reference and the passivated samples are indicated in Table 2. Similar to the case of sample A, here the trap density has increased, however, the trap energy level is also enhanced. This means that deposition of oxide has passivated the dangling bonds, however it has added new traps that have higher activation energy compared to the reference. Importantly, the generation-recombination current for the passivated sample is an order of magnitude larger than that of the reference. The underlying reason for this behavior requires further research, however, this can account for the differences on the extracted bulk-resistance for the reference and passivated sample, as can be seen in the right side of Figure 13.

Table 2 Fitting parameters for I-V modeling of batch B

Fitting Parameter for I-V Model	Reference B	Passivated B
Trap Density N_t ($1/cm^3$)	$2.3x10^{12}$	$3x10^{17}$
Trap Level E_g-E_t (eV)	0.01	0.0238

3. C-V measurement on the sidewall surface

3.1.1. MOS structure

As explained earlier surface defects are due to the damages at the device surface and sidewalls created during mesa etching. High densities of carriers at the sidewall surfaces and trap states within the forbidden gap fundamentally change the carrier recombination and transport mechanism, resulting in additional unknown measurement parameters.

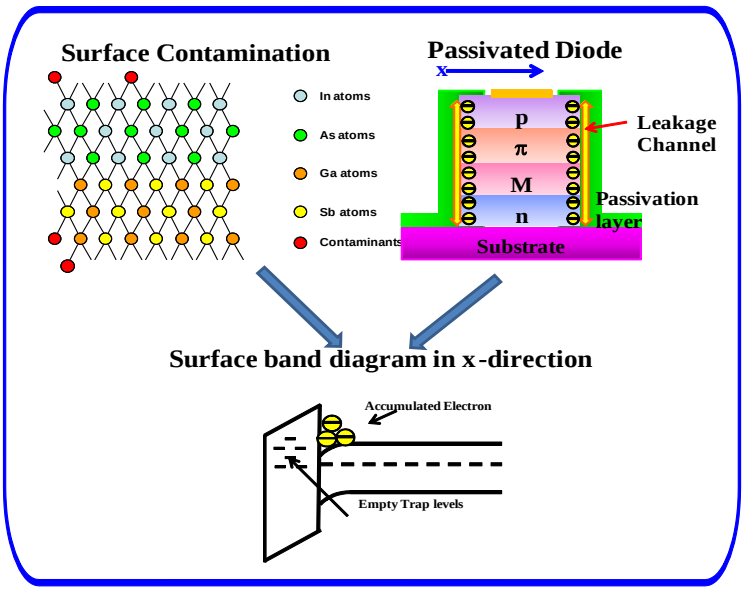

Figure 15: Surface bonds and band bending origin

By considering MOS capacitor concept, we performed C-V measurement of the surface of the Type-II InAs/GaSb based superlattice.

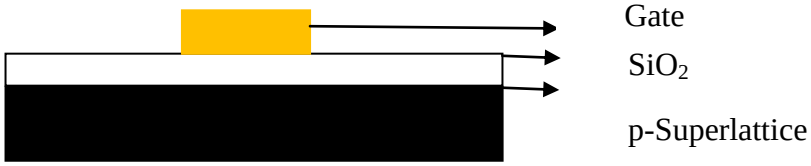

Figure 16: Basic MOS capacitor structure

Consider, p-type semiconductor, if N_a is the doping concentration, n_i is the intrinsic carrier concentration, then,

$$\phi_B = \frac{kT}{q} \ln \frac{N_a}{n_i} \qquad \text{Equation 11}$$

If ψ_s is the surface potential, the band diagram is given below at different gate voltage for the MOS structure:

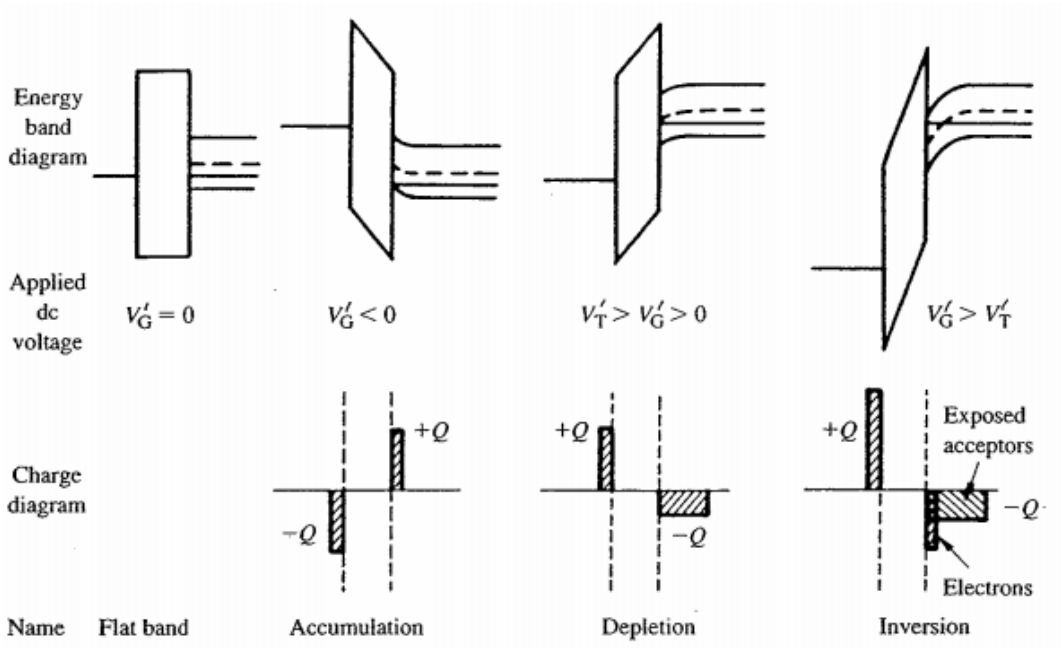

Figure 17: Band bending of MOS capacitor at different gate voltage

When negative voltage applied at the gate, majority carriers (here holes) are attracted to the surface of the semiconductor from the bulk. The excess carriers produce a positively charged layer at the surface. This condition is called accumulation since it results in an accumulation of majority carriers at the metal-semiconductor interface. When positive voltage applied (not too large) the majority carriers are repelled away from the surface of the semiconductor producing a depletion region. The depletion region contains a negative charge corresponding to the ionized acceptors known as depletion. When positive and sufficiently large voltage applied at the gate, the bands in the semiconductor bend enough that the conduction band comes close to the Fermi level. This means that, the surface of the semiconductor layer has effectively become n-type

known as inversion. The carriers in the inversion layer which contribute to conduction in a MOS based transistor.

The threshold voltage is defined as the gate voltage required to just producing inversion at the surface. It is given by,

$$V_T = 2\phi_B + \frac{\sqrt{4\varepsilon_S q N_a \phi_B}}{C_{ox}}. \qquad \text{Equation 12}$$

3.1.2. Analysis of the C-V measurements

Reference CV curve for MOS capacitor for low and high frequency is given below:

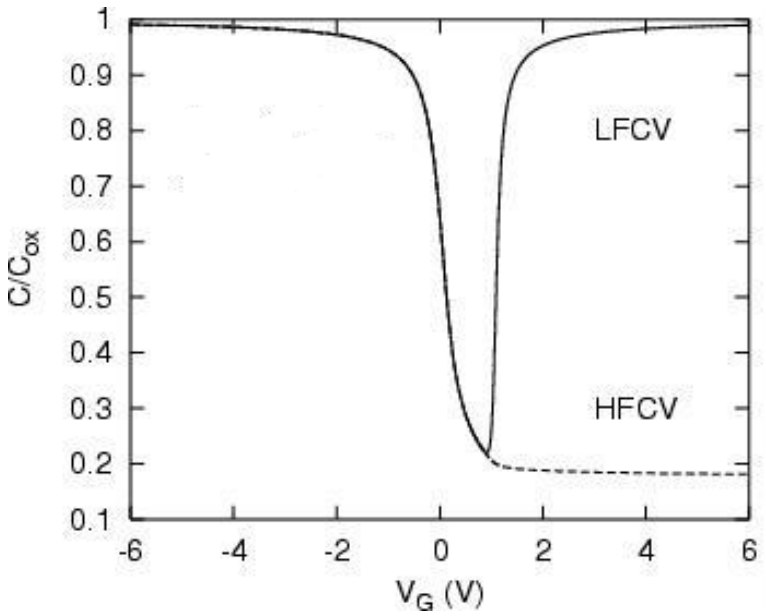

Figure 18: CV curve for MOS capacitor for low and high frequency

At low frequency both majority and minority carrier responded with gate voltage, but at high frequency, minority carrier not able to respond with gate voltage therefore, at inversion region it does not follow the low frequency CV curve. From C-V curve, we can calculate different parameters,

Flat band capacitance:

$$C_{S,FB} = \frac{\varepsilon_s}{L_B} \qquad \text{Equation 13}$$

Mid-gap Capacitance:

$$C_{S,MG} \approx \frac{\varepsilon_s}{\sqrt{2}L_B} \frac{1}{\left(\frac{q\phi_B}{kT} - 1\right)^{1/2}} \qquad \text{Equation 14}$$

Non-ideal MOS capacitor:

In ideal case, we have considered gate metal and semiconductor have same work function but actually they are different. At equilibrium, the band diagram is given below,

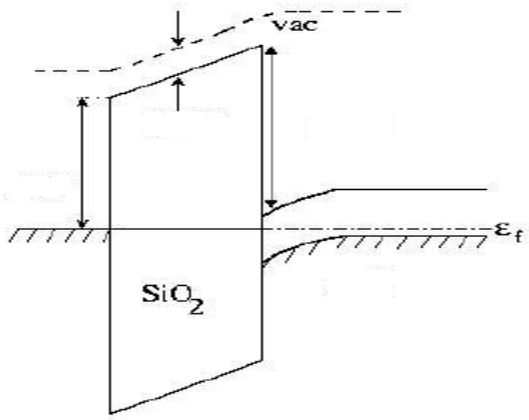

Figure 19: Band diagram at equilibrium of MOS structure

The work function of the semiconductor is given by,

$$\phi_s = \chi + \frac{\varepsilon_g}{2q} + \phi_B \qquad \text{Equation 15}$$

The modified threshold voltage then can be calculated as,

$$V_T = V_{FB} + 2\phi_B + \frac{\sqrt{4\varepsilon_s q N_a \phi_B}}{C_{ox}}$$ Equation 16

Effect of oxide charge:

For the ideal case, we have neglected the oxide charge at metal-semiconductor interface, as interface states, or interface traps, which are spread throughout the forbidden energy region between E_c and E_v of semiconductor. The energy density of interface states, D_{it}, which is the number of interface states per energy interval per unit area.

The interface states N_{it} can be calculated by,

$$N_{it} = \int_{\varepsilon_c}^{\varepsilon_v} D_{it}\, d\varepsilon$$ Equation 17

The schematic band diagram contains oxide charges given below:

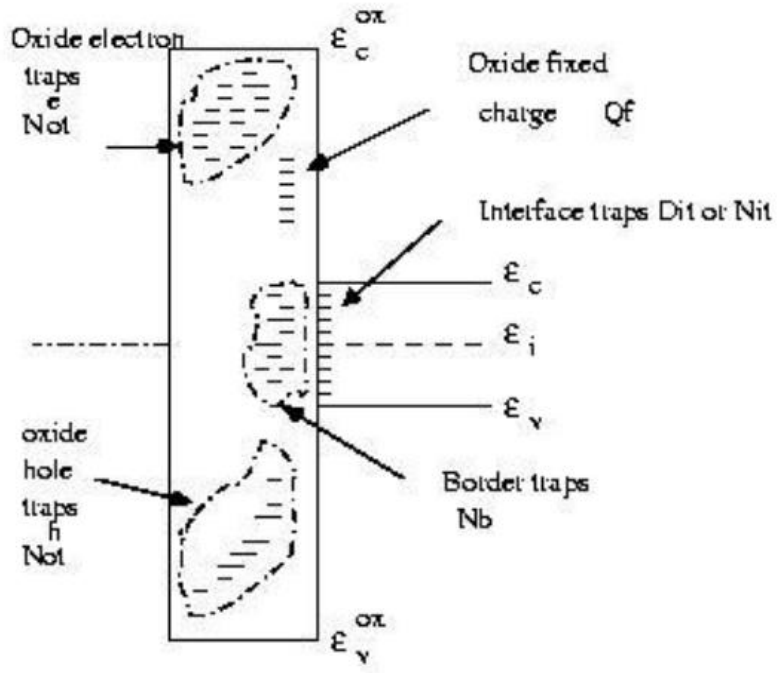

Figure 20: Band diagram of non-ideal MOS with oxide charge

If Q_{ox} is the oxide charge,

$$V_{FB} = \frac{-Q_{ox}}{C_{ox}} \qquad \text{Equation 18}$$

In general, if we have, instead of a sheet of charge Q_{ox} , an arbitrarily distributed volume charge density $\varrho_{ox}(x)$ (per cm^3), the flat-band voltage will be

$$V_{FB} = -\frac{1}{\varepsilon_{ox}} \int_{o}^{t_{ox}} x\, \rho_{ox}(x)\, dx \qquad \text{Equation 19}$$

Effect of interface state:

Consider a charge Q_{it} at the interface, the band diagram given below, in the presence of interface states accepter like above mid gap and donor like below mid gap.

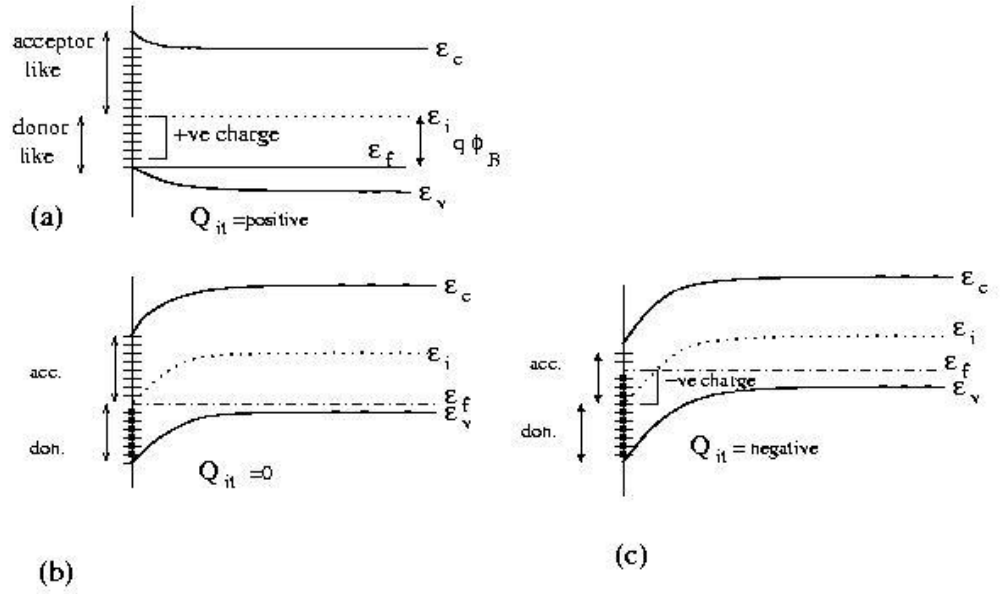

Figure 21: Band diagram in silicon in the presence of interface states which are acceptor-like above midgap and donor-like below. (a) In accumulation (b) At mid-gap (c) In inversion

The effect of CV curve due to interface states is given below:

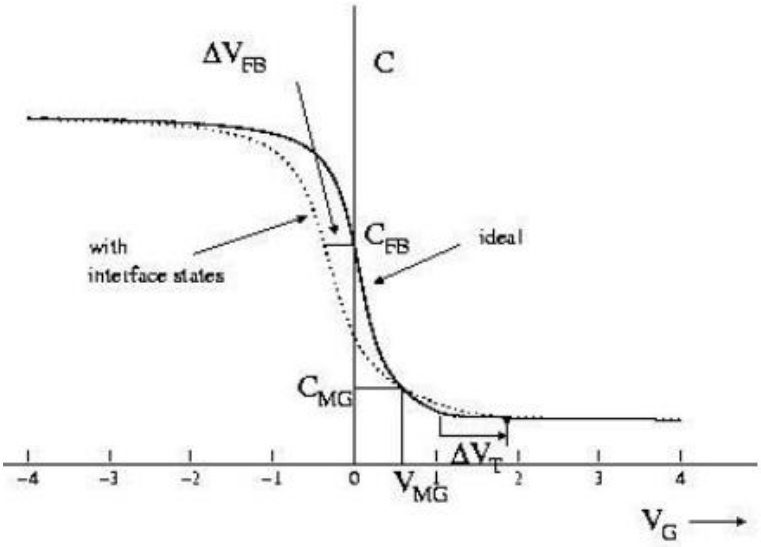

Figure 22: Effect of interface states on CV curve

Let's assume that D_{it} is uniform across the band-gap. In that case, at flat-band, Q_{it} is

$$Q_{it}^{FB} = +q\,D_{it}\,\phi_B \qquad \text{Equation 20}$$

At the onset of inversion,

$$Q_{it}^{T} = -qD_{it}\phi_B \,. \qquad \text{Equation 21}$$

Therefore, the shifts of flat-band voltage and threshold voltage with respect to the ideal are as following:

$$\Delta V_{FB} = -\frac{qD_{it}\phi_B}{C_{ox}}, \qquad \text{Equation 22}$$

$$\Delta V_T = +\frac{qD_{it}\phi_B}{C_{ox}} \qquad \text{Equation 23}$$

3.1.3. Principle and Advantage of Gating Technique

The origin of surface leakage is generally believed to be due to abrupt termination of the periodic crystal structure, which creates a band bending on the sidewall of the mesa. This band bending can cause electron accumulation or even type inversion at the sidewall surfaces, thus allowing for a conduction channel along the sidewalls. A dielectric passivation layer, aimed to physically protect the material from exposure to atmosphere, can alter the band bending by its native fixed charges. Sometimes this leads to an improvement of device performance, but sometimes results in performance deterioration. Although different surface treatments have been discussed in before to suppress the surface leakage current and understand the surface, however, none of them can give very clear understanding of the surface. In this chapter, gating technique will be introduced, which can actively control the mesa sidewall band bending by applying a voltage along the sidewall of the devices, and which is expected to eliminate the surface leakage current problem and bring in-depth understanding of the surface. This concept is similar as the metal-insulator-semiconductor (MIS) technology in field transistors, but it is applied on the vertical surface of the device sidewall. Figure 23a shows the schematic diagram of the device while Figure 23b represents the effect of gate bias on the band bending at the insulator/superlattice interface. Without applying any gate bias (V_G = 0 V), band bending occurs and electrons are accumulated on the insulator/T2SL interface, which generates a conducting channel and causes surface leakage. Once negative gate bias is applied, negative charges are stored at the metal-insulator interface and repel the accumulated electrons away from the insulator/T2SL interface.

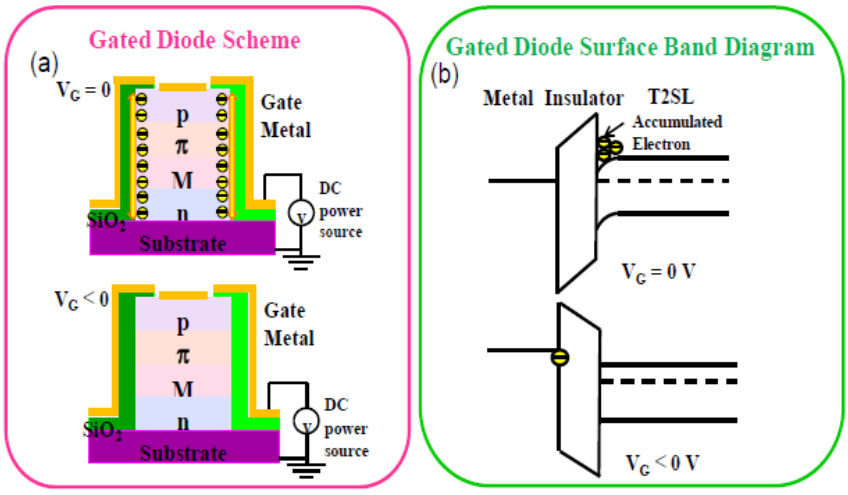

Figure 23: The schematic diagram of gated diode at zero bias and negative bias, (b) and their associated surface band diagram.

Therefore, flat band conditions can be established and surface leakage can be suppressed. More importantly, gating technique has the following benefits:

1. It has the ability to completely eliminate surface leakage.
2. It can accommodate with different dielectric passivation materials.
3. It can help to investigate the property of surface, such as type of charge, trapping level, band bending, and etc.
4. It can help to restore the quantum efficiency by suppressing the surface recombination.

3.1.4. Processing of Gating Photodetector

The sample will be first processed into single element photodetector by the same steps as explained earlier. First, single element photodetector will be delineated by electron cyclotron resonance-reactive ion etching (ECR-RIE) and citric-acid based wet etching, followed by top and bottom metal contacts deposition by electron beam metal evaporation. After that, the photodetector will be passivated by dielectric material using plasma-enhanced chemical vapor deposition (PECVD) or ion-beam sputtering deposition (IBD). Half of the sample will have a Ti/Au gate metal contact deposited on their mesa sidewalls so that it contains both gated photodetector and ungated diode (UGD). The regions of dielectric layer covering the top and bottom contacts were etched away by using ECR-RIE system so that gold wire can be directly wire bonded on to the top, bottom, and gating contact of the photodiode.

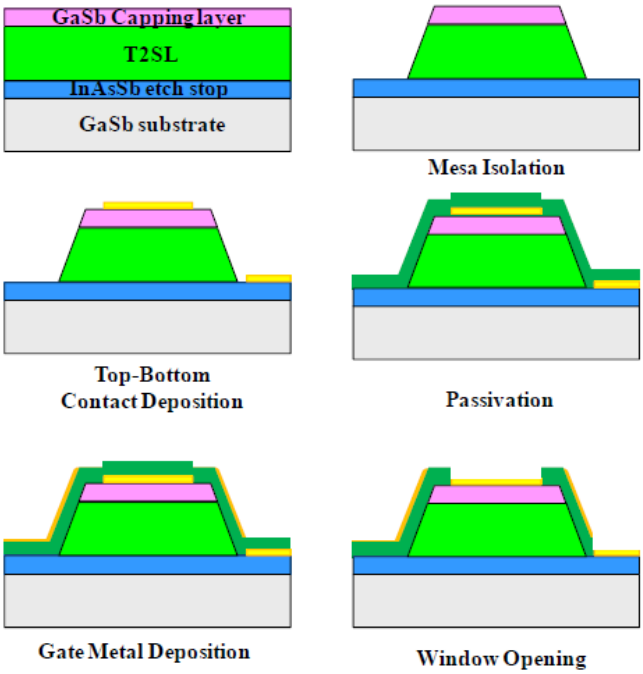

Figure 24: Processing procedures of the fabrication of type-II superlattice single element photodetector: mesa isolation, top-bottom metal contact deposition, passivation, and window opening

3.1.5. Challenges of Gating Technique in LWIR

The gating technique has been demonstrated to have the ability to eliminate surface leakage in mid-wavelength infrared (MWIR) p+-π-M-n+ T2SL photodetectors. However, this technique requires very high gate biases to be applied, and has not been transferred to LWIR because for small band gap active region, the surface leakage in LWIR p+-π-M-n+ T2SL heterostructure photodetector is more severe and the leakage phenomenon might be more complicated. The change of the surface potential is related to the band gap, doping level and the effective mass of the semiconductor. The n+- and p+-contact are large band gap heavily doped semiconductors, and the M-structure is a large band gap semiconductor with a much larger effective mass than the π- and p+-regions. Therefore, for simplicity, the discussion is focused on the π-region while the influence of gate bias on the M-structure, p+-, and n+-contact is assumed to be less pronounced than the π-region.

3.1.6. Method of Reducing Gate Bias

In order to reduce the high saturated gate bias, two possible options are applying: a high-k dielectric material or reducing the dielectric layer thickness. The gate bias can be expressed by the parallel capacitance formula:

$$\sigma = \varepsilon\varepsilon_0 V/d \qquad \text{Equation 24}$$

where V is the saturated gate bias, ε_0 is the permittivity in vacuum, ε is the SiO_2 dielectric constant, assumed to be 3.9, σ is the SiO_2 surface charge density, and d is the dielectric thickness. Here, we report high performance LWIR gated diodes with low gate bias achieved by reducing the SiO_2 passivation layer thickness.

The LWIR T2SL p_+-π-M-n_+ heterojunction was grown on a GaSb substrate. After a 1.5 μm n-doped InAsSb buffer layer, the device structure consisted of a 0.5 μm thick n_+-contact (n_+~10^{18} cm^{-3}), 0.5 μm thick lightly n-doped M-barrier, 3 μm thick π-region (p_- ~6 x 10^{16} cm^{-3}), 0.5 μm thick p_+-contact (p_+~10^{18} cm^{-3}) and capped with a p_+-type InAs capping layer. The superlattice period in the π-region and p_+-contact region consisted of 13/7monolayers (MLs) of InAs/GaSb and 7/11 MLs of InAs/GaSb respectively. Both regions were doped with beryllium. The M-barrier and n_+-contact superlattice periods consisted of 18/3/5/3 MLs of InAs/GaSb/AlSb/GaSb in one period and both were doped with silicon. The material was processed into six dies of single element diodes with diameters ranging from 100 to 400 μm with the same processing procedures as discussed before. One die (sample A) was left unpassivated for reference and the unpassivated diodes (UPD) were used for electrical and optical characterization. The other dies (sample B, C, D, E, and F) were passivated with 10 nm, 20nm, 60nm, 300nm, and 600nm thick SiO_2 dielectric layer respectively using plasma-enhanced chemical vapor deposition (PECVD). An additional metal gate was deposited on the mesa sidewalls of half the diodes in those samples so that they contained both gated diodes (GD) and ungated diode (UGD). In the final step, the

top contacts were opened using electron cyclotron resonance etching. All samples were wire-bonded onto 68 pin leadless ceramic chip carriers, loaded into a cryostat, and cooled down to 77K for characterization. Average I-V characteristics of five different sizes UPDs and UGDs are compared at Figure 25-a. All UGDs exhibit much leakier I-V characteristics than the UPDs because SiO_2 passivation layers cause severe surface leakage for diodes in the LWIR. UGDs with different SiO_2 passivation layer thickness have the same I-V characteristics, which indicate that, above some threshold thickness, fixed charges in the SiO_2 do not have any effect on surface leakage.

Therefore, the fixed charges that cause band bending and surface leakage are mainly situated in the SiO_2-T2SL interface or the very thin SiO_2 layer near the mesa sidewall. Additional surface treatment to reduce the amount of fixed charges is required before or after SiO_2 passivation.

As shown in Figure 25-b, the average dark current densities of GDs at $V_G = V_{sat}$ are orders of magnitude lower than that of UPDs. The best RA_{-100mV} value the GD achieved is 3071 Ωcm^2, which is ~10 times higher than that of UPDs, and ~500 times higher than that of UGDs. After eliminating the surface leakage, the bulk dark current characteristic should be achieved and all GDs saturate at the same level, which is confirmed in Figure 25-b. The best saturated gate bias achieved is -4.5 volt with 10nm SiO_2 passivation layer. The linear correlation between the saturated gate bias and the thickness of SiO_2 (Figure 25c) follows the calculated SiO_2 fixed charged density is estimated to be about 4×10^{12} cm^{-2}.

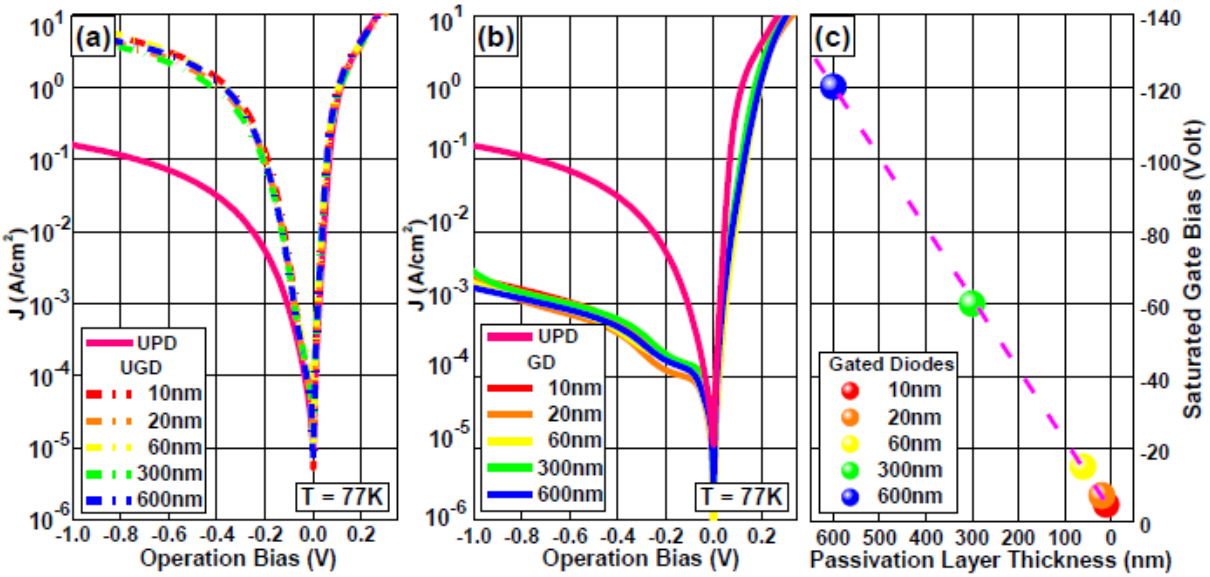

Figure 25: (a) Electrical performance comparison between unpassivated diodes (UPD) and ungated diodes (UGD) with different SiO2 passivation layer thickness. (b) Electrical performance comparison between UPD and gated diodes (GD) at saturated gate bias. (c) Correlation between gate bias and SiO2 passivation layer thickness

3.1.7. Surface Leakage Mechanisms

Since we already know that applying negative gate bias can realize flat band condition and eliminate surface leakage, positive fixed charges must exist at the T2SL-SiO_2 interface or within the SiO_2 passivation layer. When the gate bias is less than or equal to saturated negative gate bias ($V_G < V_{sat}$) and not enough to generate a distinct field-induced depletion region at the M-structure surface, holes are accumulated at the surface of the π-region, and the space charge region (SCR) is still mainly at the metallurgical junction (Figure 26a). Since there is no significant change on the SCR region or type inversion occurring on the surface, the surface leakage current is eliminated. Therefore, when $V_G < V_{sat}$, the dark current density remains unchanged with respect to the gate bias and is identical to the bulk dark current. When the gate bias is larger than V_{sat} but smaller than the threshold voltage of inversion ($V_{sat} < V_G < V_T$), fixed charges at the SiO_2-T2SL interface or within the SiO_2 attract electrons, leaving behind an SCR of uncompensated ionized acceptor ions near the π-region surface (Figure 26b).

The surface generation-recombination (G-R) current associated with the surface depletion region is related to the surface field-induced depletion width, x_{sd}. When the mesa surface is depleted, the surface field-induced depletion width and hence surface G-R current increases with increasing gate bias, resulting in rising reverse dark current. Therefore, dark current density depends on the gate bias. As gate bias increases above V_T, the field-induced depletion width reaches its maximum value ($x_{sd\ max}$) and type inversion occurs on the surface (Figure 24c). Therefore, there is no further increase in the surface G-R current and the dark current density remains unchanged with respect to gate bias.

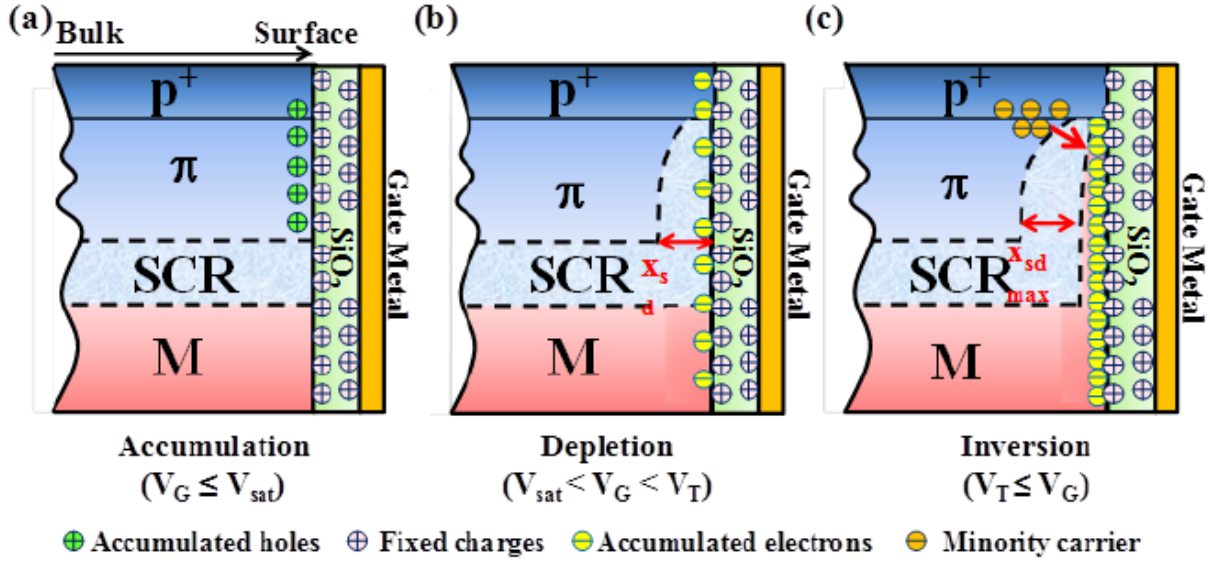

Figure 26: The schematic diagram of gated diode π-region surface condition at (a) accumulation, (b) depletion, and (c) inversion situation

4. Work completed

Methodology

By applying our vast prior experience on the development of type-II superlattice based photodetectors, various LWIR structures were designed and grown. Reference single pixel devices with various sizes and shapes are then processed and electrically characterized. The dark performance is analyzed by the shape of the curve which is very typical of each type of dark current. Upon verification of the established processing method, the exact same structure is passivated by deposition of SiO_2 by PECVD. The dark performance is again measured and the same analysis is applied to investigate the influence of passivation method.

InAs/InAsSb type-II superlattice

In order to probe the influence of surface leakage current, it is essential to select the most appropriate device structure. For this purpose a material structure has to be selected that is more prone to the effects of the surface states:

c. In long-wavelength infrared (LWIR) photodetectors, the surface current has a more dominant role, mainly due to the smaller band gap of the material.
d. It has shown that the carrier lifetime for LWIR InAs/InAsSb T2SL is longer than for InAs/GaSb because of Ga-related native defects inducing SRH recombination centers and therefore can theoretically have lower G-R dark current.
e. InAs/InAsSb type-II superlattice photodetectors have been demonstrated first with low performances, mainly with low quantum efficiency. However, in CQD, high quantum efficiency has been demonstrated combined with good electrical performances, in the range of dark current of $10^{-4}A/cm^2$.[27]
f. However, passivation with SiO_2 had so far been unreliable with generally strong degradation of the dark current with a very strong surface leakage current.

Because of the promising performances of this new superlattice structure, the passivation is very important to be devised and efficient in order to be able to go toward small size pixels. Moreover, in this study, we are interested with the effect of the structure on the surface leakage, and in how to minimize the effect of the surface of the diodes.

Design of the structure

We were first using a similar nBn structure as Haddadi et al [27]. However, passivation of the nBn structure (n-contact, undoped MWIR barrier, n-type active region) in a single element device with diodes between 100µm to 400µm was resulting in a large degradation of the dark current density, with SiO_2 passivation. In addition, smaller dimensions ($d<100\mu m$) shall result in a higher surface leakage current and have even more degradation compare to the reference. Therefore, to address the issue, an additional barrier with larger band gap (~1eV) is introduced in

the structure to suppress the surface leakage current as much as possible. The top n-contact is replaced with a p-type GaSb capping layer. We call this structure p-Contact Double Barrier n-type absorption region (C_pDBn).

At first, the idea was to replace the mid-wavelength infrared (MWIR) barrier (~250eV) from the structure and use a larger band gap barrier instead, an AlAsSb barrier, as it is used in MWIR InAsSb/AlAsSb nBn photodetectors. However, since LWIR absorption region have smaller band gap and a different valence band energy, the two barriers are not aligned, which creates a large bias dependence and low performances, and is the reason why this type of barrier is usually not used for LWIR detectors. This band alignment issue was solved by making a type-I superlattice by introducing two monolayers of GaSb every five monolayers of AlAsSb, pushing up the valence band of the barrier at the level of the absorption region valence band. In addition, the Fermi levels must also be aligned to avoid large bias dependence and in a similar way as for MWIR PπMN structure for Pour et al [28], the barrier must be this time highly p-doped to align the Fermi levels. This makes the depletion region shift from the barrier to the LWIR absorption region, which induces a higher G-R current. The solution is to reintroduce the undoped MWIR barrier in between the AlAsSb/GaSb barrier and the absorption region, which makes the depletion region shift back to the MWIR region to reduce the G-R current and which permits to keep the large band gap barrier for suppression of the surface leakage current. The structure is shown in Figure 27.

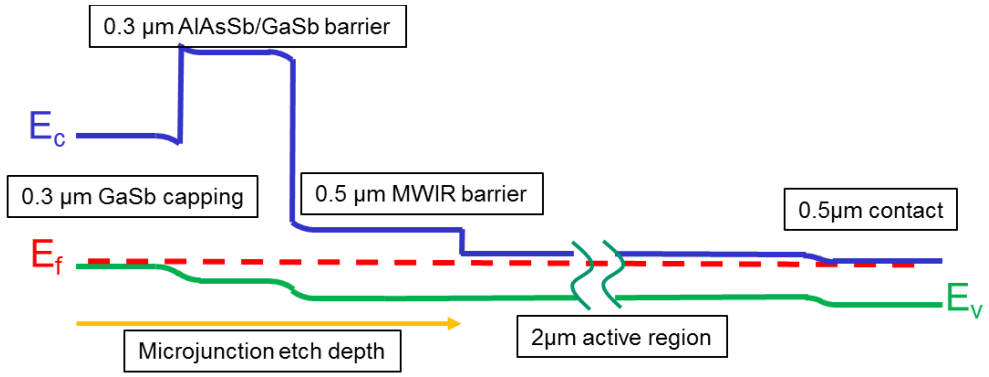

Figure 27: band diagram of C_pDBn structure

Device processing and passivation

Three wafers were grown: the C_pDBn structure, the same structure with only the MWIR barrier and another one with only the AlAsSb/GaSb barrier. A single element sample was processed for each wafer, as a reference, by using standard processing technique described below. The reference samples were not passivated. The details of processing are as the following:

IX. Substrate cleaning by Acetone-Methanol-Isopropanol

X. Optical lithography for mesa-isolation

XI. Dry etching of the mesa by using an inductively-coupled plasma etching followed by a citric acid based wet etching

XII. Post-etch cleaning by AZ400T stripper, acetone, methanol and isopropanol

XIII. Lithography for contact definition

XIV. Deposition of contacts by e-beam evaporator

XV. Lift-off and subsequent cleaning similar to step IV

To control the quality of process, the etch depth for the mesa were confirmed by using an optical profiler. Additionally, the quality of the sidewalls was visually verified by acquiring high-resolution images using a scanning electron microscope. As indicated in Figure 15, the sidewalls are smooth, and free of visible defects. Furthermore, the corners of the square-shaped pixels are round to minimize the high-potential spots and the associated undesired current mechanisms.

Passivation is done with the sample process except for the wet etching that is not done, that the combination of wet etch and SiO_2 was not compatible.

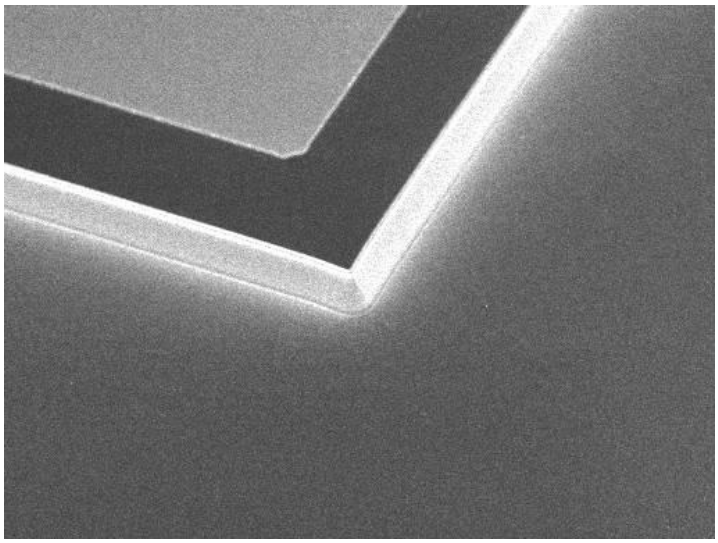

Figure 28: SEM picture of single element reference sample

Measurement and analysis of dark current

All samples were measured in the Janis Liquid Helium cryostat at 77K by exactly the same way. The optical characteristics of all samples were first measured in a Janis Liquid Helium cryostat at 77K. The samples have a 9µm cut-off wavelength for 2µm absorption region and about 34% quantum efficiency.

The electrical performances are measured in the same cryostat but with cold shield, which permits not to have a 300K background of the sample but only a 77K background, which decreases significantly the photocurrent which becomes completely negligible. The analysis of each sample was performed on sets of diodes with sizes from 100 x 100 µm to 400 x 400 µm for the reference sample. The passivated samples also have the same range for the diode sizes except for the CpDBn structure, given it had much better performances was processed with diodes ranging from 5µm to 400µm.

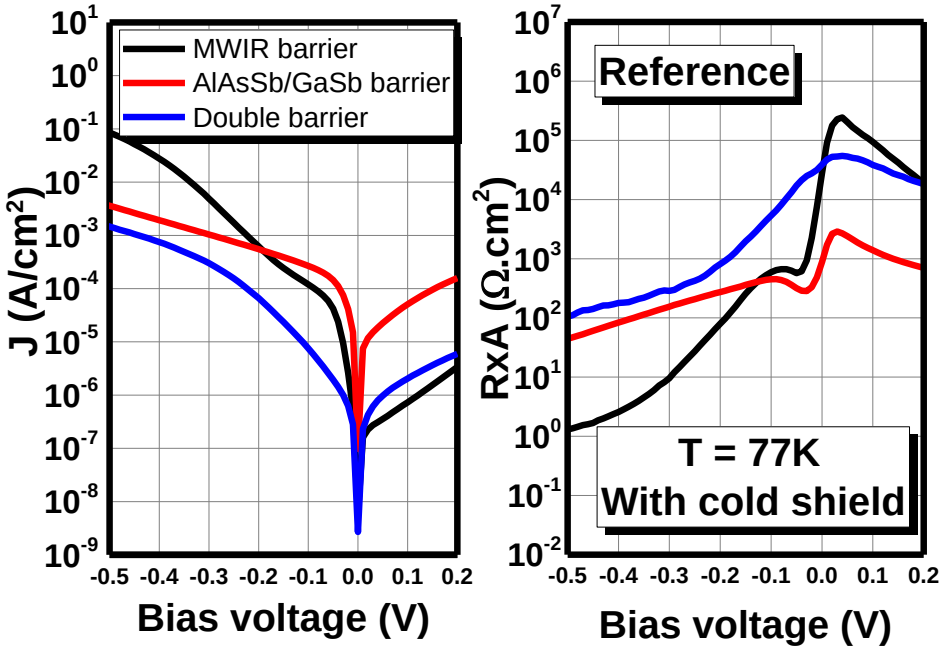

Figure 29: Electrical performances of reference samples

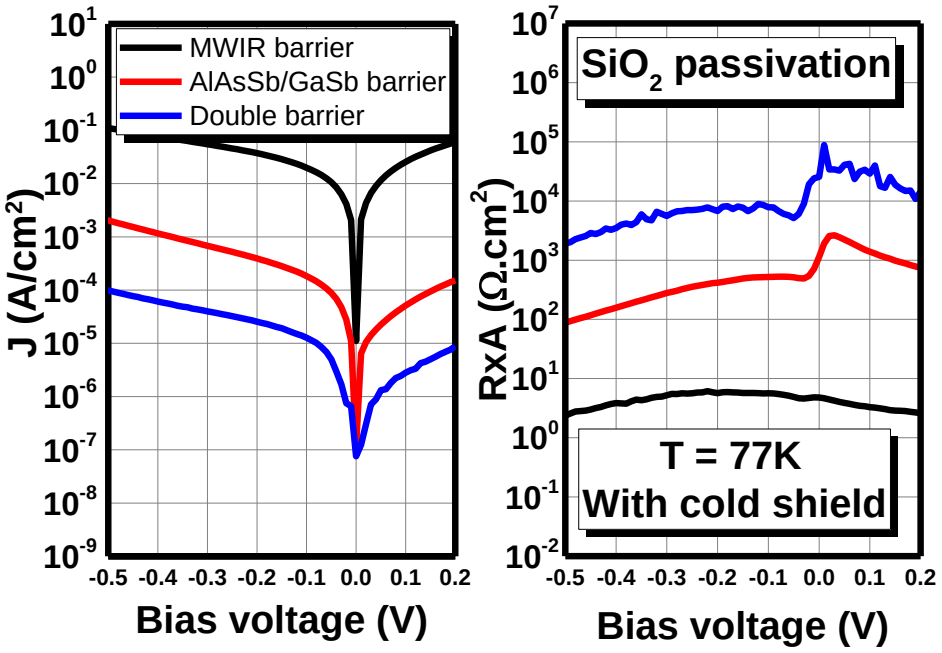

Figure 30: Electrical performances of passivated samples

As can be seen in Figures 29, the MWIR sample has good performances as low bias, and is G-R limited, however, at higher biases, the sample has a high dark current, which looks to be surface leakage via trap assisted tunneling current. Passivation of this sample (Figures 30) creates a strong degradation of the performances. It seems the band bending in the barrier is strong enough to cancel the effect of the barrier and we can see the barrier is almost "short-circuited" given the resistance area product curve is almost flat.

For the sample with AlAsSb/GaSb barrier, the main limiting dark current mechanism is the G-R current. As expected, the high doping density in the barrier close to the absorption region creates a shift of the depletion region toward the LWIR absorption region. However, passivation on this sample doesn't change the dark current at all. The barrier blocks the surface leakage completely.

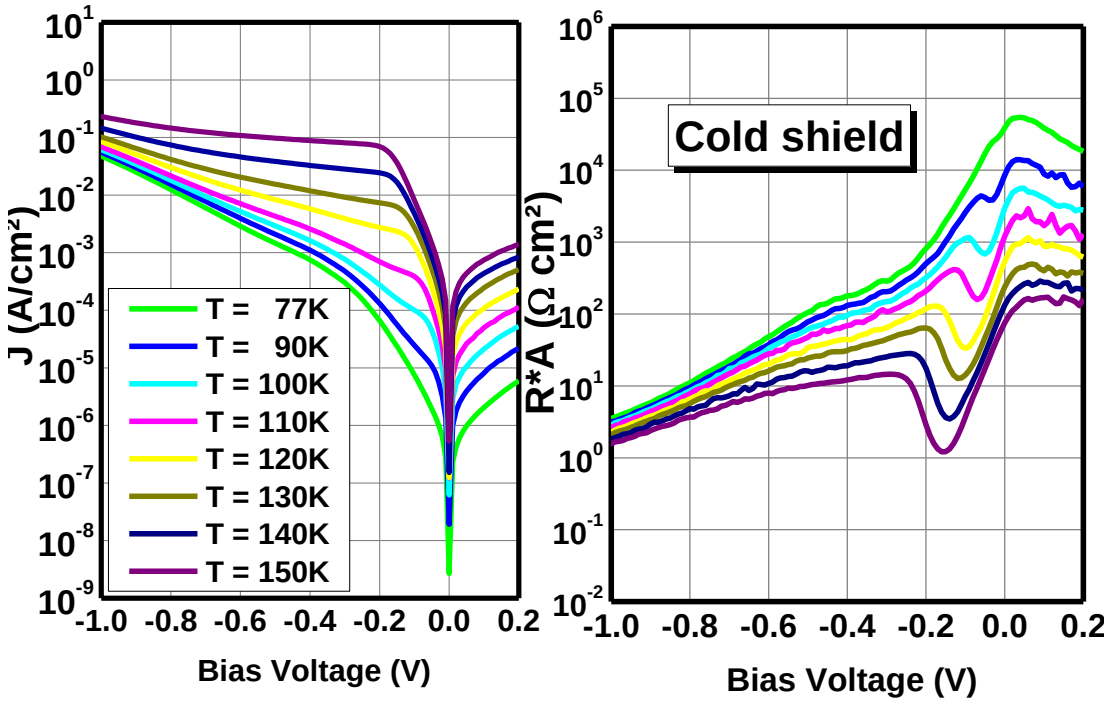

Figure 31: Electrical performances of C_pDBn structure with temperature

For the double barrier, the sample combines the advantages from both samples: while the reference sample looks to suffer a little from trap assisted tunneling current, the dark current after passivation is G-R limited and is kept at the same level as the reference sample, because of the wet etch for the reference sample which is typical of the reference sample, compare to the passivation samples which are processed with dry etching only as Huang et al has proved to have less surface leakage. The P/A curve is shown in Figure 32 and a surface resistivity of $3.1 \times 10^7 \Omega.cm$ is extracted from the curve.

There is still some surface leakage remaining as we can see on the P/A curve. It is possible it is due to the damages created by the ICP dry etching and mainly with the Ar, which is used for a physical etching with BCl_3 for chemical etching, and that could create more G-R current from the surface.

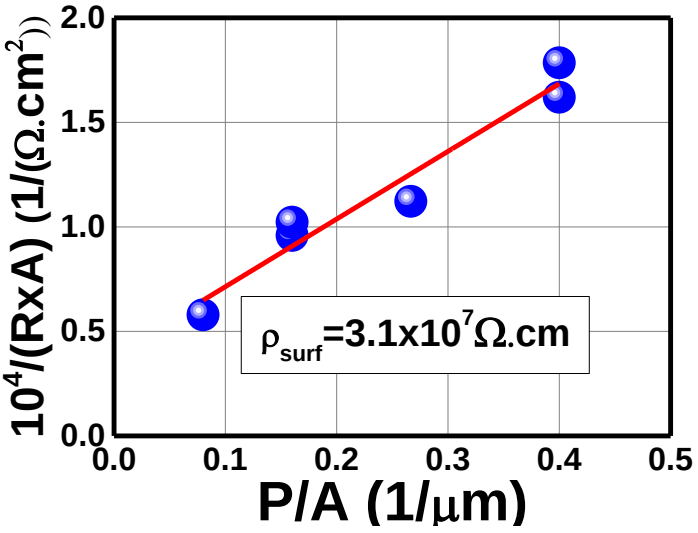

Figure 32: P/A curve for diodes ranging from 400µm to 5µm

As the dark current is low and the surface leakage not too important, a microjunction process is feasible. Separating the optical and electrical area permits to reduce the junction size compare to the mesa size, which reduces the dark current originating from the junction area, mainly the G-R current. The photo-carries are collected laterally and therefore the optical performances are the same.

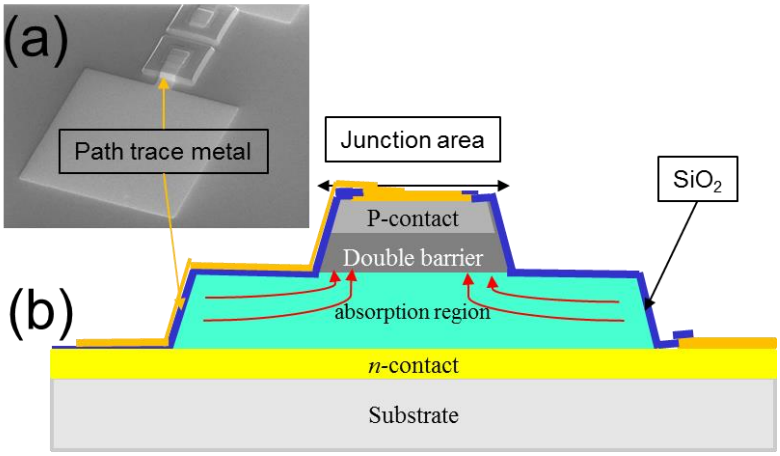

Figure 33: Microjunction structure

A sample was processed in the exact same way as the passivated samples with various sizes of microjunction on the C_pDBn structure wafer. Two parameters in the design of the microjunction have to be taken into account, the ratio of the mesa area over the microjunction area ($R_{M/MJ}$) and the distance between the microjunction and the outside collection area. One would think having the larger ratio $R_{M/MJ}$ would permit to the best dark current since the bulk

dark current originating from the junction are divided by this ratio, however, it also increases the bias dependence of the optical performances because extra applied bias is required to extract the carrier beyond the diffusion length and the dark current is increasing with the applied bias. Moreover, the smaller the microjunction, the higher the surface leakage current which could be diminishing the gain from the microjunction.

With 25µm mesa as a base, 5µm, 10µm and 15µm microjunction diodes were processed to study which diodes have the best overall performances. Since microjunction diodes are passivated since they need to be connected with a path trace metal, the optical performances were measured and compared to the passivated samples. They all reached full quantum efficiency however the bias dependence shifted with the microjunction sizes as is shown in figure 22. Electrical performances were measured with cold shield and the 25µm mesa/10µm microjunction diodes ended up having the best overall performances with $6.3x10^{-6}A/cm^2$ dark current at V_b=-180mV, quantum efficiency saturation bias, therefore having a 3 times decrease of the dark current density. The special detectivity is $1.2x10^{12}cm.Hz^{1/2}/W$ compare to $1.69x10^{11}cm.Hz^{1/2}/W$ for the reference. 25µm mesa/15µm microjunction diodes showed almost as good performances with $6.5x10^{-6}A/cm^2$ at V_b=-160mV however, 25µm mesa/5µm microjunction diodes have $1.3x10^{-5}A/cm^2$ at V_b=-250mV.

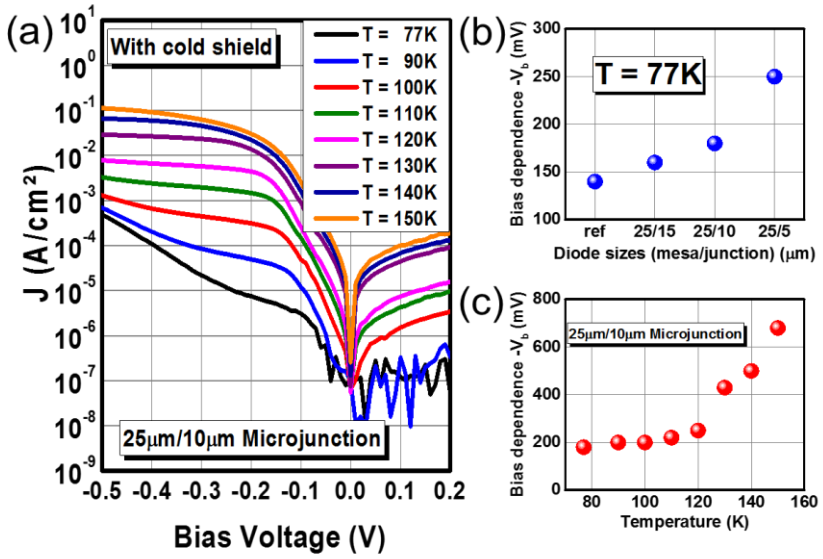

Figure 34: Electrical and optical performances of microjunction sample

As microjunction photodiodes are passivated with SiO_2, their optical performances are compared with the passivated single element test chip performances (B) to study their bias

dependence (Figure 36) and relative blackbody integrated response. All sizes of microjunction diodes reach full quantum efficiency, however, the bias dependency shifts with the microjunction size (Figure 36(a)): the photodetector needs a higher bias voltage in order to have lateral collection of all the photocarriers.

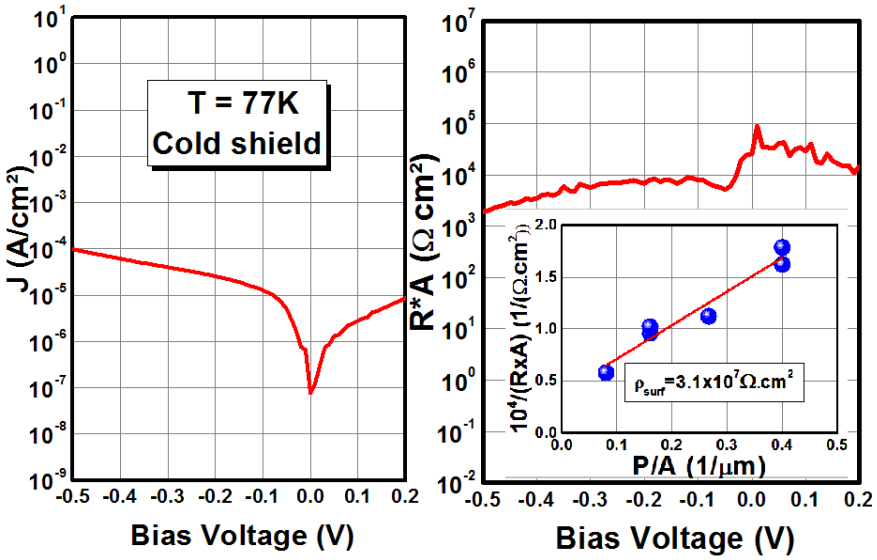

Figure 35: Electrical performances of passivated single element test chip (B) and resistivity area product dependence on diode size

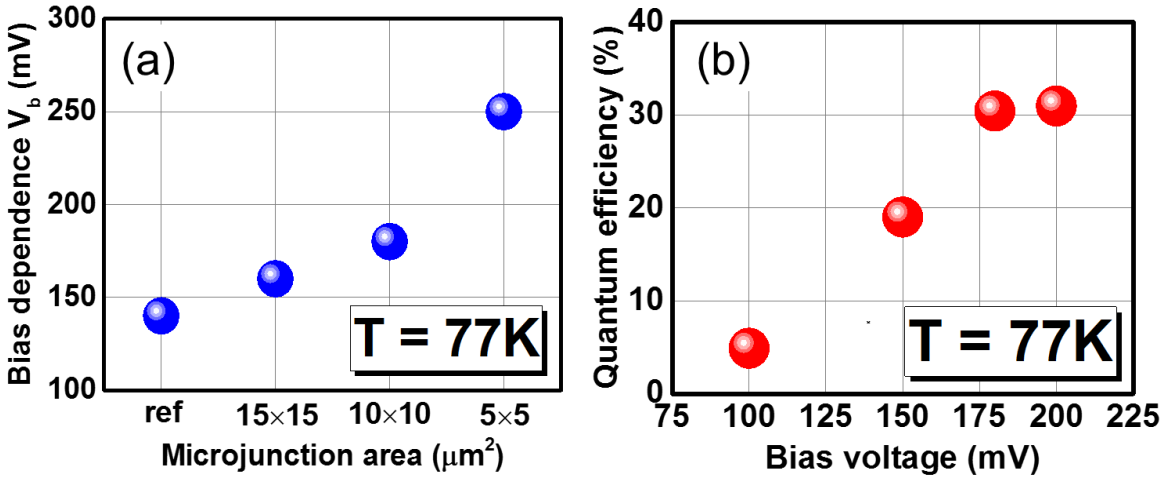

Figure 36: SEM picture of single element reference sample--(a) Bias dependency of 25×25 μm² mesa photodiodes with 5×5 μm², 10×10 μm² and 15×15 μm² microjunction and of an unpassivated photodiode. (b) Quantum efficiency at 77K of a 25×25 μm² mesa/10×10 μm² microjunction photodetector with applied bias voltage.

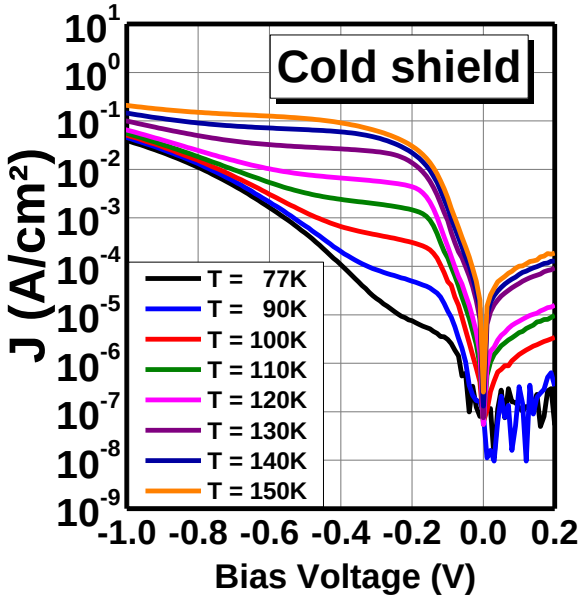

Figure 37: Electrical performances of 25×25 µm² mesa/10×10 µm² microjunction photodetectors

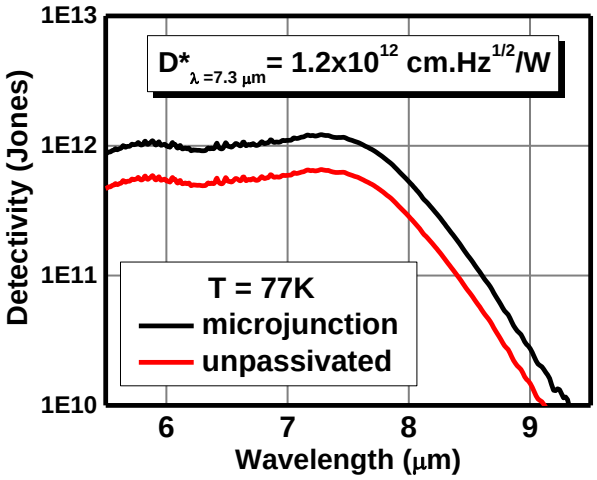

Figure 38: Comparison of specific detectivity of unpassivated and microjunction test chips

Electrical performances were measured with a cold shield and the 25×25 µm^2 mesa/10×10 µm^2 microjunction diodes have the best overall performances with a dark current density of 6.3x10^{-6} A/cm^2 at V_b=-180 mV (Figure 37) quantum efficiency saturation bias (Figure 36). Thus, these diodes' dark current density was decreased by 3 times compared to the reference sample electrical performances. The special

detectivity is $1.2x10^{12}$ cm.Hz$^{1/2}$/W for the microjunction sample (Figure 38). The 25×25 µm^2 mesa/15×15 µm^2 microjunction diodes showed almost as good performances with $6.5x10^{-6}$ A/cm^2 at V_b=-160 mV, however, the 25×25 µm^2 mesa /5×5 µm^2 microjunction diodes have $1.3x10^{-5}$ A/cm^2 at V_b=-250 mV because the lateral collection requires a significantly larger applied bias voltage.

5. **Conclusion**

In conclusion, we established a method for theoretical analysis of surface states by taking a phenomenological approach to the measured dark current density. This method was applied in studying the influence of deposition of SiO_2 by PECVD on the performance of LWIR barrier detectors. It was shown that oxide deposition passivates the dangling bonds and increases the trap energy level, however, it increases the trap density. Consequently the dark current is decreased at low (operation) bias voltages, while at larger applied bias the trap-assisted tunneling becomes dominant. Regarding the surface resistance, the SiO_2 may either increase or decrease the value, as the experiment suggests both.

We also discusses how to transfer the gating technique from MWIR to LWIR. In the LWIR T2SL p-π-M-n photodiode, gating technique also demonstrates its strong capability of eliminating the surface leakage current generated by SiO_2 passivation. Minimizing the SiO_2 thickness from 600nm to 10nm not only reduces saturated gated bias from -120 volt to -4.5 volt, but also confirms that the origin of surface leakage is from fixed charges at the SiO_2/T2SL interface or within the very thin SiO_2 passivation layer near the surface, and that a thicker SiO_2 passivation layer will not further affect surface leakage current. At 77K, the gated photodiode shows RA_{-100mV} of 3071 Ωcm^2, and detectivity of 7×10^{11} Jones. Moreover, gated diode offers a much wider operation range than the photodiode without gating architecture. Most importantly, the gating technique reveals different surface leakage current mechanisms, which provides much deeper understanding of surface leakage current and facilitates further research work on surface leakage suppression.
On onother stage of our research, the combination of the MWIR and AlAsSb/GaSb barrier were implemented to permit decreasing of the G-R dark current and at the same time to suppress the surface leakage current in order to have a reliable SiO_2 passivation, compare to a degradation of several orders of magnitude with a MWIR barrier.

Using this sample, a microjunction structure with 25µm mesa/10µm microjunction diode permits to decrease the dark current from $1.9x10^{-5}$A/cm^2 to $6.3x10^{-6}$A/cm^2, and to reach a $1.2x10^{12}$cm.Hz$^{1/2}$/W. We also reported the use of a new photodetector structure, C_pDBn, to improve passivation quality and suppress the G-R current. The barrier consists of a large bandgap (>1 eV) AlAsSb/GaSb barrier and an undoped MWIR barrier in order to reduce the G-R current by transferring the depletion region inside this second barrier. The large bandgap barrier is employed to suppress the surface leakage current and the G-R current. We also reported that the use of a microjunction structure further improves the electrical performances by reducing the

bulk dark current originating from the junction area, especially the G-R current. A study of the bias dependence of optical performances of 5×5 μm^2, 10×10 μm^2 and 15×15 μm^2 microjunctions photodiodes for a 25×25 μm^2 mesa area combined with electrical measurement, shows an optimum microjunction photodiode structure of 25×25 and 10×10 μm^2 microjunction and mesa areas, respectively, which exhibits a dark current reduction of 3 times compare to the reference at quantum efficiency saturation bias. The structure increases the special detectivity value to $1.2x10^{12}$ $cm.Hz^{1/2}/W$.

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