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RECONFIGURABLE PHASED-ARRAY ANTENNA HARDWARE USING INTEGRATED CIRCUIT TECHNOLOGY

MICHIGAN STATE UNIVERSITY

APRIL 2019

FINAL TECHNICAL REPORT

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14. ABSTRACT
A tunable matching network design was designed for a K/V dual-band RF frontend. The tuning capability was separately demonstrated. Techniques for impedance tuning were investigated and achieved in hardware. The study determined the required range of impedance adaptation, and the most suitable method was identified to cover the desired impedance plane. A hardware prototype was developed consisting of the matching network, which was later integrated into a power amplifier. The benefit of the developed tunable network was experimentally demonstrated by comparing power amplifiers at K-band with and without tunable matching networks under varying load conditions using active load-pull system. K-band was specifically chosen for demonstration purposes due to the maximum frequency of the load-pull system. There were two integrated circuit fabrication runs to implement the successful demonstration.

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1.0 SUMMARY

This project aimed at the development of an integrated, highly functional frontend technology that will facilitate the interoperability feature of aerial data links. This involved the development of dual-band frontend electronics, including reconfigurable components that can adapt to potentially significant impedance variations in each band. To this end, Silicon-Germanium (SiGe) based millimeter-wave integrated circuit prototypes were developed, demonstrating the dual-band capability. In addition to this, tunable matching networks were investigated and prototyped, and the potential of such networks was be demonstrated using MSU's state of the art measurement facilities.

A tunable matching network design was designed for a K/V dual-band RF frontend. The tuning capability was separately demonstrated. Techniques for impedance tuning were investigated and achieved in hardware. The study determined the required range of impedance adaptation, and the most suitable method was identified to cover the desired impedance plane. A hardware prototype was developed consisting of the matching network, which was later integrated into a power amplifier. The benefit of the developed tunable network was experimentally demonstrated by comparing power amplifiers at K-band with and without tunable matching networks under varying load conditions using active load-pull system. K-band was specifically chosen for demonstration purposes due to the maximum frequency of the load-pull system. There were two integrated circuit fabrication runs to implement the successful demonstration.

Stacked power amplifiers (PAs) have gained a lot of attention recently because of increased output power through equal distribution of output voltage swing among the stacked transistors. However, commonly employed PA design techniques, such as waveform engineering or harmonic tuning, often suffer in stacked configuration and the enhancement in power-added efficiency (PAE) remains poor. This work analyzes the feasibility of harmonic tuning techniques applied to stacked amplifiers. An analysis is presented to show how harmonic tuning at the output affects harmonic optimization of stacked transistors and how this depends on the base termination impedance. Three different device configurations (cascode, tri-stacked, and quad-stacked) have been characterized at X-band. Measured results show harmonic PAE enhancement degrades as the number of stacked transistors increases, which is in agreement with the analysis included.

A 0.13-µm SiGe BiCMOS dual-band power amplifier (PA) was developed which can be operated at 28 GHz or 60 GHz. The PA employs an LC tank at the input to perform dual-band impedance matching, while the output is switched from one band to the other using a tunable stub. The stub is made tunable by using an HBT switch, which reduces the stub's length when turned ON shifting the PA between 28 and 60 GHz modes. The switch has 0.7 dB ON- and 0.3 dB OFF-state loss. The measured results exhibit 16.2/11.8 dB small signal gain, 18.4/17.2 dBm saturated output power and 33/21 % peak PAE at 28/60 GHz respectively. The dual-band compact PA has a chip size of 0.55 × 0.52 mm^2 and consumes a DC current of 11 mA at 3.5 V supply voltage. This is the first known demonstration of a 28/60 GHz dual-band PA with performance comparable to dedicated PAs in each band.

A tunable matching network integrated with the PA has been developed to recover the performance degradation caused by the scan impedance variation in phased array antennas. The matching network is designed to match loads within half-gamma around 50Ω. The tunability is provided by changing the length of transmission line stubs using the reverse saturated SiGe switches. S-parameters and load-pull measurements have been obtained and show that the PA is able to match to different load impedances, therefore providing constant peak PAE and output power at these impedances.

In addition, we have developed a 28-60 GHz multi-band low-noise amplifier (LNA) suitable for K-, Q- and V-band applications, which was realized in 0.13-µm SiGe BiCMOS technology. The proposed LNA achieves its multi-band performance by employing a T-type matching topology as inter-stage matching network (IMN). The LNA has a measured gain of 14.5 dB and 14.1 dB, and simulated noise figure (NF) of 2.4 dB and 3.4 dB at 28 and 60 GHz with a mean NF of 2.9 dB. The input return loss is less than -10 dB from 22-67 GHz. The chip occupies an area of 0.15 mm^2 and consumes 27 mW from a 2.5 V power supply. To the authors' knowledge the realized LNA is superior to any state-of-the-art LNAs in similar silicon technologies.

Our approach required a compact and linear V-band up-converting double-balanced Gilbert cell mixer implemented in a 0.13-µm SiGe BiCMOS technology. Detailed design procedures for the on-chip transformer baluns are provided that enables the compact implementation. The mixer occupies an area of 365-µm × 400-µm with pads and 175-µm × 300-µm without pads, consuming 52 mW from a 2.5 V power supply. The mixer achieves an OP1dB of -1.4 dBm at 60 GHz RF frequency, IF-bandwidth of 0.5-8.5 GHz on both sidebands, a maximum conversion gain of 13.4 dB and a 3-dB bandwidth of 50 to above 67 GHz. The performance of the mixer outperforms the other state-of-the-art V-band mixers in terms of chip area, IF bandwidth and linearity.

Finally, this work also demonstrates a 24-32 GHz upconverting mixer implemented in SiGe process technology. The mixer uses double-balanced Gilbert cell architecture with on-chip transformer-based baluns for the LO input and RF output ports. With LO power of 6 dBm, the mixer achieves a maximum conversion gain of 13.7 dB at 26.5 GHz, a 24-32 GHz 3-dB bandwidth, IF-bandwidth of 0.25-1.25 GHz on both side-bands with 27 GHz LO frequency and OP1dB of -1.5 dBm at 28 GHz. It occupies an area of 468-µm × 465-µm consuming 90 mW from a 2.5 V power supply. The performance is comparable to any state-of-the-art mixers in similar silicon technologies.

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2.0 INTRODUCTION

As the new generations of airborne systems are being deployed with improved sensor technology and environmental awareness, effective airborne communication systems that preserve existing aperture installations are becoming key assets that are simultaneously desired. However, many links make use of separate frequency bands (e.g., K-band and V-band), requiring different hardware, and limiting the interoperability between generations of fighters.

Interoperability between the airborne platform generations has been demonstrated in several specific cases with unique hardware solutions. It is possible to further pursue this trend, and develop a universal hardware solution that can be reconfigured by integrated circuit (IC) technology for improved interoperability supporting multiple frequency bands. There are several approaches that could enable the realization of such a hardware solution. This is summarized in Figure 1.

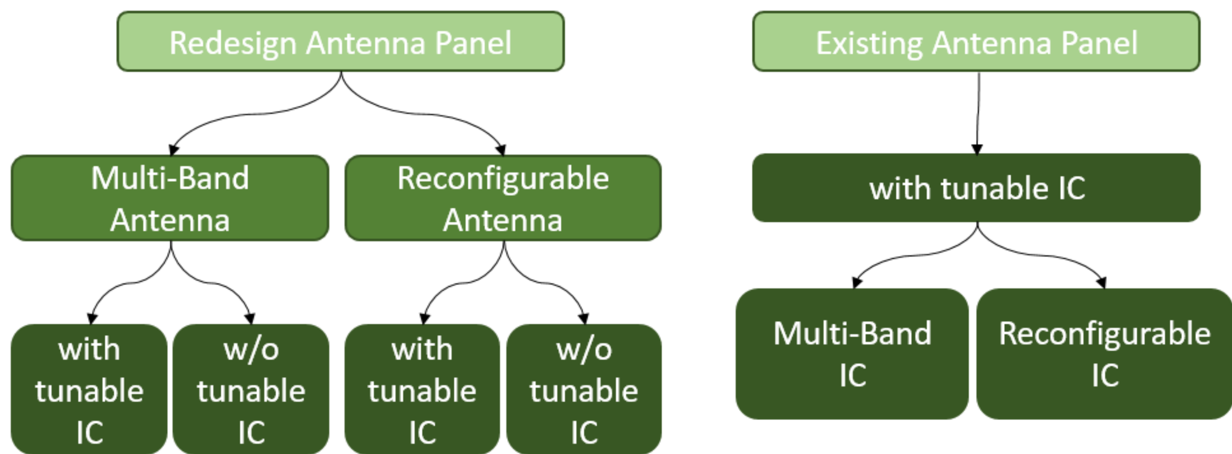

Figure 1: Solution paths for the reconfigurable phased-array.

The first solution path will allow access to the antenna panel, where the array antennas can be optimized for multiple bands of operation. This can be done in two ways: Multi-band antennas and reconfigurable antennas.

One possibility is to design and optimize multi-band antennas that resonate at the desired frequency bands. Examples exist in the literature, for instance, an X-/K-band reflect array [1.1], a dual-band linear array at K-band [2.1], and a 12 GHz/24 GHz linear antenna array [3.1] have been demonstrated. The disadvantage of such an approach is that the hardware will be strictly constrained by the limited number of potential optimized antenna geometries that can operate at the desired frequency bands. A potential way to extend this approach is to include a reconfigurable IC frontend following the antenna array, providing an additional degree of freedom.

A similar approach is to design and optimize a reconfigurable antenna that can adjust its geometry electronically by inclusion of control circuitry on the antenna panel, in order to accommodate the target frequency bands. The approach here is similar to examples from other open architecture

efforts, while here a much higher frequency of operation will be aimed that may constrain the available switch technologies to be employed within the reconfigurable array. In Figure 2, a potential reconfigurable antenna solution is proposed that uses silicon-germanium (SiGe) ICs as control units that can adjust the length of radiating dipole antenna elements. Such SiGe control units can operate at the desired high frequencies and can include additional functionalities such as phase and amplitude control in addition to switching. The drawback of this approach is the increased complexity of the array panel, especially concerning routing of supply and control signals required for the control units. Similar to the Multi-Band Antenna approach, the reconfigurable antenna concept can be combined with a reconfigurable IC frontend following the array.

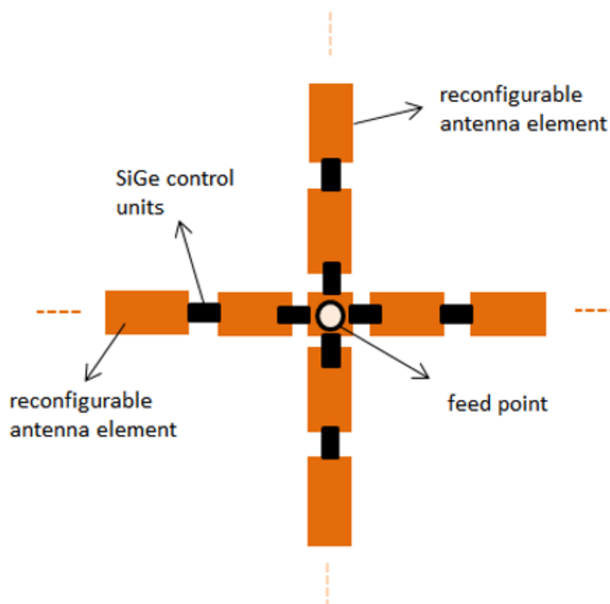

Figure 2: Reconfigurable antenna employing SiGe ICs.

In certain cases, it may not be desired to redesign the antenna panel and it may be preferred to make use of existing hardware and enable interoperability only by making use of the following electronics. This can be possible by making use of advanced IC technology including tunable elements into the frontend that interfaces the antenna panel. Considering the large difference between the target frequency bands, there a number of development paths.

One solution is to integrate two frontends operating at the desired bands into one single die, and switch between the two making use of a wideband switch. This is depicted in Figure 3. Here, a wideband switch covering both bands will select the corresponding frontend that is optimized to operate in one of the desired operation bands. In Figure 3, a K-band antenna aperture is chosen as an example, in this case, the V-band frontend will be optimized to match the impedance that the K-band antennas present at V-band.

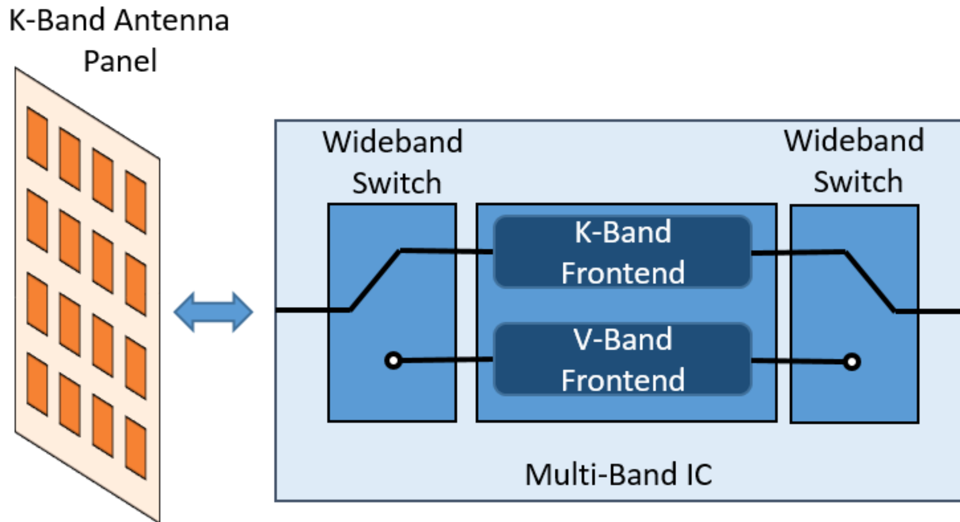

Figure 3: Multi-Band IC concept interfacing K-band antenna panel.

Another potential path is to integrate tunable matching networks (TMN) so that the frontend electronics can be adapted to operate in the desired frequency bands. This is shown in Figure 4. Here, tunable matching networks (potentially making use of shunt active switches and length adjustable transmission lines, e.g. [4.1]) adjust the impedance of the frontend electronics to enable operation in the desired frequency bands. The main challenge here would be the impedance presented to the IC, for instance, from a K-band aperture at V-band. Potentially, this will require a very large range of impedances that would need to be covered by the tunable network, resulting in increased implementation loss.

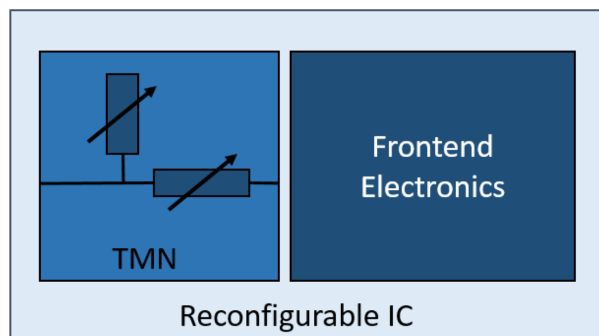

Figure 4: Reconfigurable IC concept incorporating a tunable matching network.

A third solution that combines the previous two approaches would potentially result in highest flexibility and performance. This is shown in Figure 5.

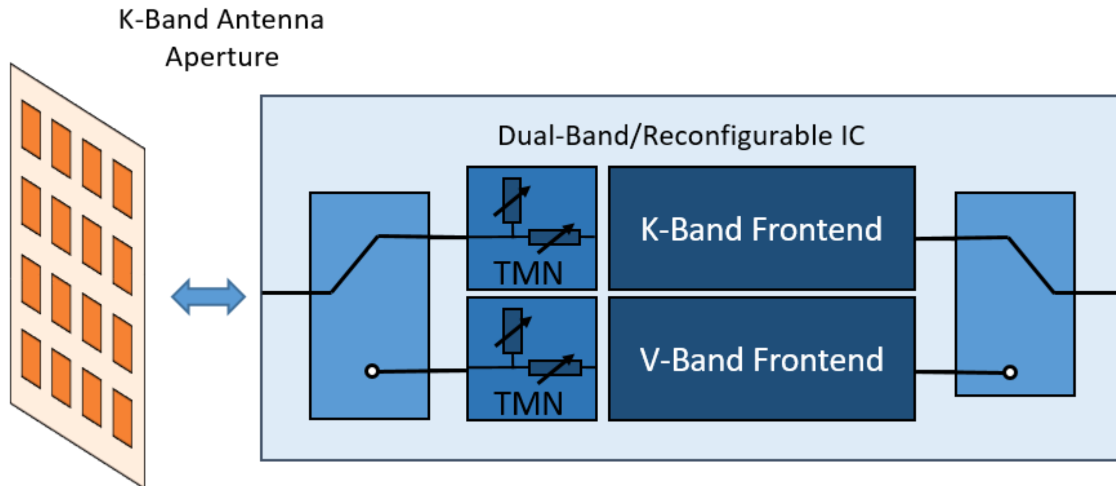

Figure 5: Multi-band & reconfigurable IC concept.

This approach will alleviate the potentially high loss that may arise due to the required range of impedances, as now each frontend can be optimized to be close to the impedance that the antennas present at each band. In addition to this, the additional capability of impedance tuning will have added benefits of adapting to impedance changes during beam-steering resulting in improved electronic beam-forming and beam-steering capabilities. This clearly requires high flexibility from the electronics following the K-/V-band antenna panel. It is possible to achieve such high degree of functionality within a small form factor by making use of advance silicon-based IC technologies.

The detailed concept is illustrated in Figure 6, where a dual-band IC interfaces the K-band aperture, as extension of Figure 5. The IC will include frontend electronics at K- and V-bands, separately optimized for the impedance presented from the antenna array at each band. Depending on how the antenna elements are realized in the fixed aperture, a wideband switch can be utilized to select the desired frontend with a single output, or two separate outputs can be provided without the switch. In addition to these, tunable matching networks (TMNs) will be included that can be realized by on-chip transmission lines with shunt-connected active switches. The impedance tuning capability will have added benefits of adapting to impedance changes during beam-steering resulting in improved electronic beam-forming and beam-steering capabilities.

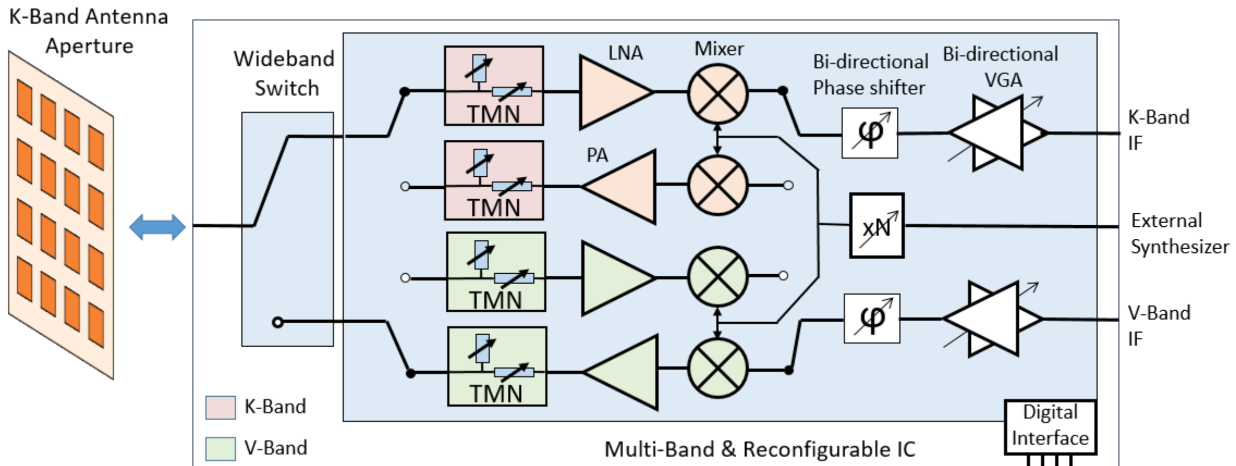

Figure 6: Multi-band & reconfigurable IC concept.

The frontends will include receive and transmit capability, as well as phase-shifting and gain adjustment for the electronic beamforming and beam-steering operation. The common electronics will consist of up-/down-conversion, intermediate frequency (IF) amplification and filtering. In addition to these, a reconfigurable frequency synthesizer with an external reference source and a programmable multiplication ratio will be included for the K- and V-band up- and down-conversion mixers. A digital interface (e.g. Serial/Parallel Interface) will be included for the programming of the phase shifters, variable gain amplifiers, frequency synthesizer and switches.

Inclusion of simple (single transistor) active switches along a transmission line segment can enable tuning over a wide range of impedances. This concept is illustrated in Figure 7. A similar tuning concept was demonstrated by the offerors making use of shunt Micro-Electro Mechanical (MEM) switches in a 24 to 79 GHz tunable LNA [4.1]; while, shunt active Heterojunction Bipolar Transistor (HBT) switches have been recently demonstrated by the offerors with excellent performance up to D-band frequencies [5.1]. Here, we propose to combine both approaches towards a highly miniaturized, high-performance TMN making use of high-yield SiGe HBT devices as switches.

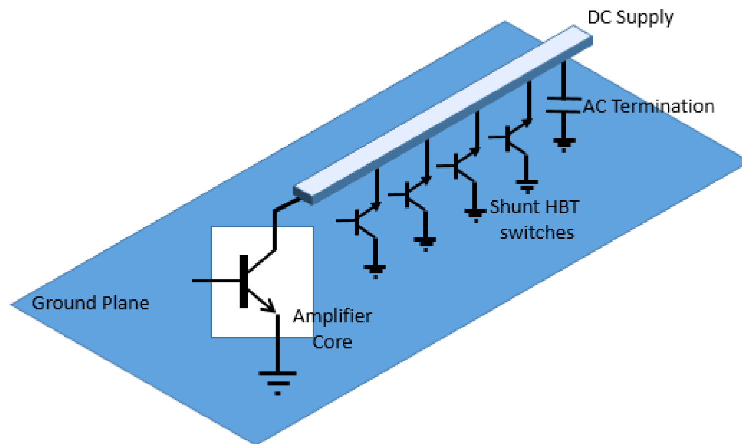

Figure 7: Tunable transmission line concept making use of shunt HBT switches.

For the application in question, silicon-germanium (SiGe) BiCMOS technology is considered to be an excellent candidate. This technology platform has quickly matured in the last two decades, and 4th generation HBTs today achieve maximum frequency of oscillation (f_{max}) values reaching 500 GHz. In addition to excellent high-speed characteristics, the SiGe HBTs also provide good low-noise performance (e.g., 4 dB noise figure at W-band demonstrated by the offerors [6.1]), and include CMOS transistors suitable to be used for digital control electronics. In terms of output power, 18 dBm at W-band has been also demonstrated by the offerors with reasonable power-added efficiency of 30% [7.1].

In addition to these considerations, significant advances have been made in the area of heterogeneous integration, and a possible approach would be to divide the proposed frontend into two ICs, making use of a higher performance III-V technology (e.g. GaN) to realize the PAs and the LNAs.

The overall goal of this program was to utilize the capability of state of the art integrated circuit technologies, specifically SiGe, for the implementation of a fully integrated dual-band frontend for aerial data link interoperability. Towards this purpose, a K/V dual-band frontend was developed in a state-of-the art SiGe BiCMOS technology platform. Furthermore, tunable matching network implementations were investigated, following the basic concept outline in Figure 7, and a prototype was implemented demonstrating the impedance tuning capability. The tunable matching network was integrated into a power amplifier, and the benefits were experimentally demonstrated using MSU’s active load-pull system.

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3.0 METHODS, ASSUMPTIONS, AND PROCEDURES

3.1 Stacked SiGe Power Amplifier Design

The continuous scaling in modern semiconductor technologies for higher transit frequency (f_τ) leads to a monotonic decrease in the breakdown voltages of the devices, especially for silicon-based device technologies. Therefore, the achievable output power using conventional power amplifier (PA) architectures, where a single device provides the output voltage swing, also decreases more and more. To overcome the low breakdown voltage limitation, it is possible to stack several devices in series. Series stacking of transistors makes it theoretically possible to obtain a higher output voltage swing by dividing the voltage equally among the stacked transistors. For an unchanged output current swing, the output power and the optimal load impedance are higher, allowing a high output power, as well as low impedance transformation ratio for matching networks [1.2]. On the other hand, power added efficiency (PAE) is often degraded due to parasitic capacitances of intermediate nodes and non-constructive addition of voltage swings because of phase variations [2.2]. In order to boost PAE, waveform engineering is commonly applied to PAs by harmonic tuning. The harmonic terminations at the output are typically optimized using load pull measurements, resulting in lower power dissipation and PAE enhancement.

In this work, we studied the applicability of harmonic tuning techniques to stacked amplifiers. We conducted basic circuit analysis to show that the impact of harmonic tuning done at the topmost transistor significantly depends on the number of stacked transistors and the base termination impedance. Therefore, enhancement in efficiency turns out to be quite low as lower transistors continue dissipating more power. As a proof of concept, different X-band PA cores (cascode, tri-stacked and quad-stacked) have been designed, and characterized using an active load-pull system with harmonic tuning capability. PAE contours are acquired for each case, and the measurements confirm the dependence of efficiency enhancement by harmonic tuning on the number of stacked transistors.

3.2 K/V Dual Band Amplifiers

This work deals with the design of a K/V dual-band power amplifier, which is proposed as one of the sub-blocks in a dual-band transceiver architecture. A dual-band transceiver operating at K/V band is of special interest for both radar and wireless communication purposes. The vast unlicensed bandwidth (7 GHz) at V-band can provide multi-Gbps data rates for communications or very high resolution for radar at V-band, whereas the low atmospheric and free-space propagation loss at K-band can provide long distance communication or higher range for radar. Furthermore, due to the varying propagation characteristics and capacities among different potential 5G bands, a reconfigurable or multi-band RF transceiver unit is proposed, which can use the appropriate frequency band as required by the environment, country or application.

Multi-band frontend electronics has been a topic of interest towards single-chip integration in order to decrease the power consumption and IC area. For example, [1.3] uses variable inductors or varactors to adjust operational frequency, [2.3] uses LC tanks in matching network for dual-band operation, [3.3] uses MEMS switches to change matching network configuration, and [4.3] uses CMOS switches at both input and output matching networks to shift between frequencies. However, tunable inductors or capacitors give narrow tuning range and MEMS switches add cost and complexity to the fabrication process, while [4.3] operates at less than 10 GHz.

This paper presents, for the first time, the design of a 28/60 GHz band-switchable power amplifier in 0.13um BiCMOS process. The PA uses cascode as the core amplifier biased in class AB mode. Dual-band operation has been achieved by employing an LC tank in the input matching network and a switchable output matching network. The PA achieve 18.4/17.2 dBm output power and 33/21 % PAE, which is comparable to the state-of-art single-band 28 or 60 GHz PAs. To the authors' knowledge, this PA is the first demonstration of dual-band operation at K- and V-band with comparable or better performance to dedicated PAs in each frequency band.

3.3 K-band Reconfigurable Impedance Matching Network for Phased Arrays

Phased array antennas have received huge attention in recent years because of several advantages. These include rapid scanning, high gain and creating a pattern with a very low side lobe level. On the other hand, they suffer from active scan impedance variation. Mutual coupling between adjacent antenna elements leads to deviation from nominal 50 ohms impedance. Therefore, each antenna element in the array undergoes impedance variation as the scan angle of the beam is varied [1.4-2.4]. If not taken care of, active impedance variation can result in reduced antenna efficiency, mismatch between power amplifier (PA) and antenna, breakdown of PA in case of large reflections, increase in noise figure of receiver and distortion in radiation pattern of antenna.

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Numerous techniques have been developed to alleviate the mutual coupling in an array. Some of the prominent techniques being: high impedance electromagnetic surfaces for mutual coupling reduction [3.4], wide angle impedance matching using dielectric sheets [4.4], split ring resonators and meta-surfaces [5.4], and defected ground planes [6.4]. These techniques present difficulty in developing meta-materials, placement of materials on top of the array, limited performance enhancement and relatively high cost. Contrary to these approaches, a possible solution can be realized in circuit design domain: a tunable matching network (TMN) can be inserted between PA and each antenna element. Ideally, this TMN would transform different antenna impedances to the desired load impedance for the power amplifier, thus eliminating the effects of scan impedance variation.

Although there are a lot of publications on the tunable matching networks, only a few shows them integrated with the PA. The reconfigurable PAs in [9.4]-[10.4] use MEMS based high-Q inductors and capacitors to construct tunable matching network and have scattered impedance coverage, the tunable PAs in [11.4]-[12.4] use on-chip lumped inductors and capacitors for multi-band operation and therefore have non-uniform impedance coverage, and some PAs [13.4] use tunable matching networks for output harmonic tuning with limited impedance coverage on Smith charts. To the best of authors' knowledge, there is no direct demonstration of a PA integrated with tunable output matching network with uniform impedance coverage, built for minimizing scan impedance variation in phased array system. In this paper, the authors present a K-band PA integrated with a reconfigurable TMN. The TMN is designed using double shunt stub topology and can match load impedance within half-gamma magnitude circle around center point (50 Ω). Therefore, the load impedance mismatch during beam steering (in phased arrays) can be overcome in real time.

3.4 K-band HBT LNA

The millimeter-wave frequency range has gained a lot of attention from the researchers to cope up with the increasing demand for high data rate communication systems. The unlicensed spectrum around 60 GHz for indoor wireless systems, 28 and 39 GHz for upcoming 5G and internet-of-things (IoT), 26-46 GHz satellite systems for high-resolution radars, 35-50 GHz for radio-astronomy are some examples. Similar to GSM standards, a multi-band system that can adapt to various communication standards at mm-waves according to the functionality would reduce cost and enable wide-spread application. Also, realizing fully integrated transceivers on low-cost platforms like silicon are suitable for large-volume production.

In this paper, we present a 28-60 GHz multi-band low-noise amplifier (LNA) suited for applications in K-, Q- and V-band. We chose LNA as a building block to demonstrate wide functionality because LNAs, being the first block along the receiver chain of a transceiver, determine the overall noise figure (NF) of the receiver, and therefore it should have the lowest NF with enough gain sufficient to suppress the noise of the subsequent blocks.

The LNA is implemented in 0.13-μm IHP Microeletronics SG13G2 BiCMOS process with 300 GHz-f_T/500 GHz-f_{MAX}. The measured gain of the LNA is greater than 10 dB from 22.5-66.6 GHz

and greater than 14 dB from 27.5 GHz- 60.1 GHz. The simulated mean noise figure (NF) is 2.87 dB for 28-60 GHz with the minimum being 2.271 dB at 32.1 GHz. The measured S11 is less than -10 dB from 22-67 GHz. The realized LNA shows better performance than any other state-of-the-art circuits in similar technologies when compared in terms of bandwidth and NF.

3.5 V-band Upconversion Mixer

Within the last decade, the V-band has drawn much attention from researchers especially for high data rate communication systems. Recently, it is also considered as one of the mm-Wave frequency bands approved by FCC for the "fifth-generation" (5G) mobile communication technology that aims to provide a reliable and dependable network with high data rate and low latency. Transceiver components on silicon platforms can deliver high-capacity performance at a low-cost to support the proposed 5G infrastructure. The upconverting mixer is one of the most important blocks of the transmitters, particularly in millimeter-wave domain for converting low intermediate frequency (IF) to high radio-frequency (RF) transmit signal at the input of the PA. Therefore, the power-handling capability and the linearity of the upconverting mixer is crucial as it needs to provide the required input power to the PA.

A V-band upconverting mixer for millimeter-wave transmitter is presented using a 0.13-μm SiGe BiCMOS process. The size of the chip is 0.146 mm^2 with pads and 0.052 mm^2 excluding pads. The extremely compact design is achieved by using transformer-based baluns at the LO and RF ports. Although, similar topologies using transformer baluns have been reported, various design trade-offs that need to be considered have not been discussed. In this report, these factors are discussed with a detailed overview providing design guidelines. The realized mixer demonstrates state-of-the-art performance in terms of linearity, size and bandwidth.

3.6 K-band Upconversion Mixer

The increasing demand for high data rate wireless communication systems has driven researchers to introduce the fifth-generation (5G) mobile communication technology [1.5]. K-band is one of the primary frequency bands that have drawn interest for 5G transceivers. The upconverting mixer is one of the most important blocks for transmit-section of the transceivers, particularly in millimeter-wave regime for converting low intermediate frequency (IF) to high radio-frequency (RF) transmit signal at the input of the power amplifier (PA) followed by the transmitting antenna. The power-handling capability and the linearity of the upconverting mixer is therefore important as it needs to provide the required input power to the PA. Although III-V technologies are commonly the preferred choice for PAs, the other transmitter components are typically built in silicon technologies which provide high integration density and a low-cost platform for large-scale market production.

In this report a 24-32 GHz upconverting mixer for millimeter-wave transmitters in a 0.13-μm SiGe BiCMOS process is detailed. It shows an excellent linearity with OP1dB of -1.5 dBm at 28 GHz, consuming 90 mW of DC power, with a maximum conversion gain of 13.7 dB at 26.5 GHz, 3-dB bandwidth of 24-32 GHz and has an area of 0.218 mm^2. It uses transformer-based baluns at the LO and RF ports to achieve the very compact design. Such performance is comparable to any state-of-the-art K-band mixers in III-V technologies while it outperforms most of those that are demonstrated in CMOS and BiCMOS processes.

4.0 RESULTS AND DISCUSSION

4.1 Harmonic Tuning of Stacked SiGe Power Amplifiers Using Active Load Pull

In a stacked PA, where the output transistor is terminated with a certain load impedance (at fundamental or harmonics), each transistor in the stack will see this impedance differently, mainly depending upon the base terminations. To clarify how the base termination affects the impedance seen by lower transistors, we analyze a generalized case as shown in Fig. 8. Consider a transistor whose base is terminated with an admittance, Y_B, and the collector is terminated with a load admittance, Y_L. Using the small signal π-model as shown in Fig. 8, a Y-matrix can be derived. The input admittance of the two port network can be written as:

$$Y_{in} = y_{11} - \frac{y_{12} y_{21}}{Y_L + y_{22}} \quad (1)$$

To clarify the impact of base termination, we will consider two limit cases:

When the base is shorted:

Using $Y_B=\infty$, corresponding to a common-base topology, we get:

$$Y_{in} = g_m + Y_{10} - \frac{Y_{20}(g_m + Y_{20})}{Y_L + Y_{20} + Y_{12}} \quad (2)$$

Since a transistor's small signal r_o is high and collector to emitter capacitance is small, Y_{20} becomes very small and we can neglect it. Therefore,

$$Y_{in} \approx g_m + Y_{10} \quad (3)$$

This shows that for the shorted base, Y_{in} becomes almost independent of load termination at output.

When base is open:

This can be further divided into two cases for simplification:

a) When the load is shorted, that is $Y_L=\infty$, (1) gives:

$$Y_{in,SL} = \frac{Y_{12}}{Y_{12} + Y_{10}}[g_m + Y_{10}] \tag{4}$$

b) When the load is open, that is Y_L=0, (1) gives:

$$Y_{in,OL} = Y_{in,SL} - \frac{y_{12}y_{21}}{y_{22}} \tag{5}$$

This shows that $Y_{in,OL}$ is smaller than $Y_{in,SL}$ by $\frac{y_{12}y_{21}}{y_{22}}$. This means that Y_{in} has not only become dependent upon Y_L, but also follows the same trend as Y_L; that is, when load is short, Z_{in} becomes low and when load is open, Z_{in} becomes high.

The above analysis draws an important conclusion that if the base of a transistor is terminated with high impedance, its input impedance (seen from the emitter) follows the load impedance (at collector); and if base is shorted (common base), the input impedance becomes independent of load impedance.

Since in stacked PAs, each lower transistor sees the load impedance through the emitter of the transistor above, this means that if the base termination of upper transistor is high, lower transistors can also see load harmonic impedances to a certain extent. However, as the number of stacked transistors increases, the load impedance seen by the lower transistors also reduces, eventually reaching a point where the impedance seen by lower transistors become independent of load impedance. This can be better understood with the help of examining a quad-stacked device as shown in Fig. 9(c). Assume T4, the topmost transistor, is harmonically tuned for class F operation where the second harmonic is shorted and the third harmonic is presented with open circuit. This results in rectangular voltage waveform across T4. Transistor T3 sees the harmonic terminations through the emitter of T4. Considering that in a stacked design, the base termination impedance is high, the short and open are translated to some low and high impedances, as determined by (4) and (5), so voltage waveform across T3 also gets partially optimized for class F operation. However, T2 does not benefit as it sees the open load through T3, which translates the open load impedance to a value which is not sufficiently high. Similarly, conditions for T1 tends to be even worse.

A simulation is also performed for the quad-stacked case to see how the impedance seen by each stacked transistor varies as a function of load impedance at the output node. Fig. 10 shows a Smith chart plot of Z_{in1}, Z_{in2} and Z_{in3} while Z_L is varied from short to open. It can be observed that Z_{in3} follows the trend of Z_L; that is, when Z_L is short, Z_{in3} is also small and when Z_L is open, Z_{in3} is also high. Z_{in2} also follows the trend of Z_L but with smaller variation, whereas for Z_{in1} the variation is very small. This variation in Z_{in} keeps getting smaller as we increase the number of stacked transistors, and eventually converges to (4). Fig. 10 also includes the case when the base of T4 is grounded and Z_{in3} becomes constant and independent of Z_L variation as expected from (3). These simulations confirm the theoretical analysis presented.

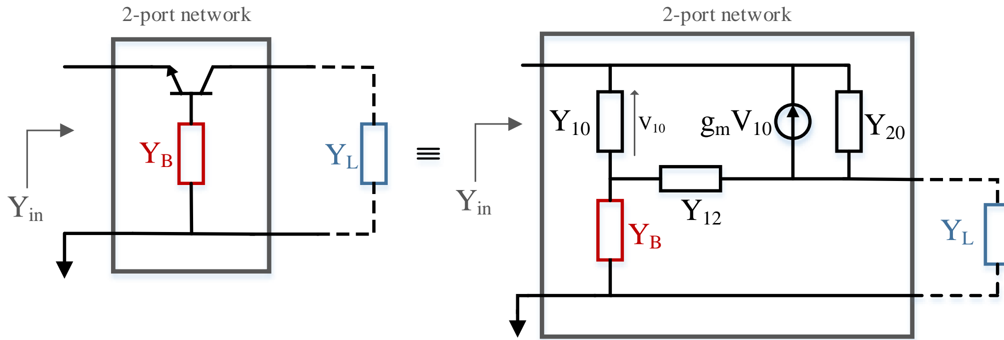

Figure 8: Y-parameter analysis of transistor with base and collector termination

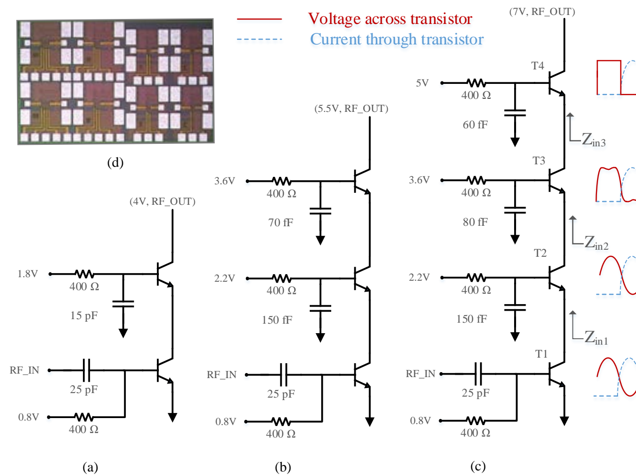

Figure 9: Y-parameter analysis of transistor with base and collector termination. Designed X-Band power amplifiers: a) Cascode, b) Tri-stacked, c) Quad-stacked, d) Fabricated chip.

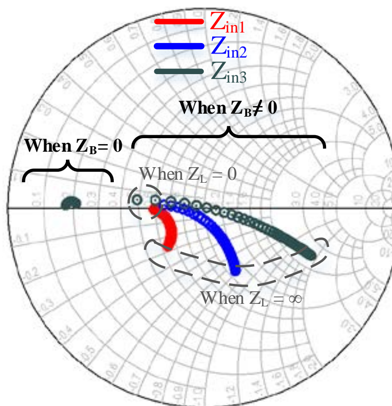

Figure 10: Variation of Z_{in1}, Z_{in2}, and Z_{in3} when Z_L is varied from short to open

Cascode, tri-stacked, and quad-stacked PA cores have been designed at X-band using IHP SG25H4 0.25 µm SiGe HBTs with a specified f_T/f_{max} of 180/220 GHz.

Fig. 9(a) shows the designed cascode topology where the upper base is terminated with ample capacitance to have AC ground at X-band frequencies. Figs. 9(b) and (c) show tri-stacked and quad-stacked topologies where the upper bases are not AC grounded; instead, they are terminated with specific capacitances, based on the guidelines provided here and in [3.2]. The values of base capacitors and bias voltages have been optimized through simulations to allow equal voltage swings across each transistor. The 400 Ω resistors are included in bias paths, and serve the purpose of RF blocking.

The MT2000 (Maury Microwave) mixed-signal active load pull system is used to perform fundamental and harmonic load pull measurements. All the PAs have been measured with continuous wave (CW) operating conditions at 10 GHz. Source pull is performed for fundamental only, whereas load pull is performed up to three harmonics. On-wafer small signal calibration is done using SOLT standards, and an absolute large signal power calibration is performed using manufacturer supplied SOL standards.

All designed device topologies are biased in class B operation. First, input power and fundamental impedances are swept to find the optimum load and source impedance for maximum PAE, while 2nd and 3rd harmonics are terminated by 50 Ω. Having the fundamental impedance terminated at the desired point, the 2nd harmonic impedance is swept (keeping the 3rd harmonic terminated at 50 Ω), and PAE contours have been measured. After terminating fundamental and 2nd harmonic load impedances at the highest PAE point, 3rd harmonic impedances are swept and PAE contours have been measured. Fig. 11 shows measured PAE contours, and Fig. 12 shows measured fundamental output power contours at 2 dB gain compression point.

Table 1 lists the PAE and output power (Pout) enhancement by harmonic tuning, where enhancement means the difference between PAE or Pout when a harmonic is terminated at the best possible and the worst possible location. The cascode device (Fig. 12(a)) shows the highest PAE improvement of 18% for the 2nd harmonic and 5% for 3rd harmonic tuning. The tri-stacked device (Fig. 12(b)) shows a PAE improvement of 10% for 2nd harmonic, and 2% for 3rd harmonic tuning. The quad-stacked device (Fig. 12(c)) shows 7% improvement for 2nd harmonic tuning and 1% for the 3rd harmonic. These results are in parallel with the expectations and the analysis provided here.

While recent work suggests individual tuning of harmonic impedance for each stacked transistor [4.2], the effectiveness of this technique will potentially be limited, because the suggested additional harmonic termination appears in parallel to the emitter impedance of the next transistor. Our analysis shows that this impedance approaches the value derived in Eq. (4) as the number of the stacked transistors increases, which as a result dominates the impedance at these intermediate nodes.

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Table 1: Comparison of PAE and Pout Enhancement by Harmonic Tuning

Topology	Enhancement by 2nd Harmonic Tuning		Enhancement by 3rd Harmonic Tuning	
	PAE (%)	Pout (dBm)	PAE (%)	Pout (dBm)
Cascode	18	2.1	5	0.44
Tri-stacked	10	1.4	2.3	0.26
Quad-stacked	7	0.9	1.6	0.18

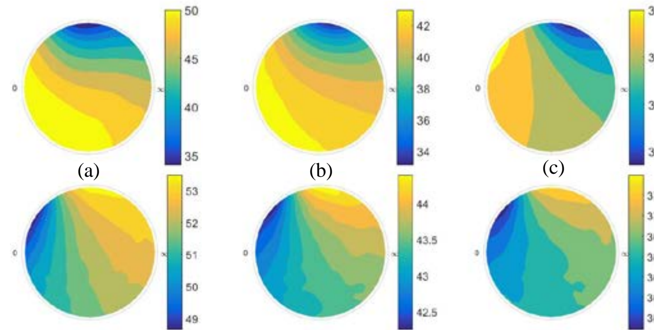

Figure 11: Variation of Z_{in1}, Z_{in2}, and Z_{in3} when Z_L is varied from short to open

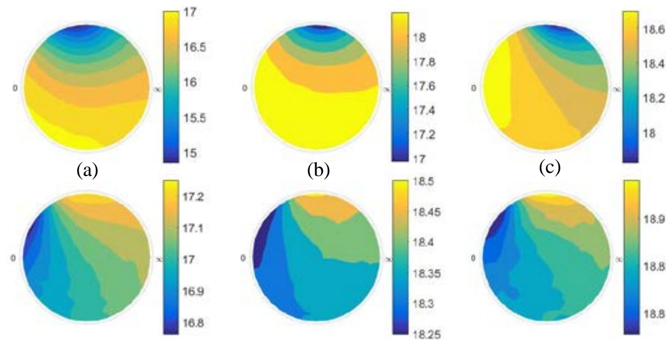

Figure 12: Measured fundamental output power (dBm) contours for 2nd harmonic (top) and 3rd harmonic (bottom) impedance sweep: a) Cascode, b) Tri-stacked, c) Quad-stacked

4.2 28/60 GHz Dual-band Power Amplifier

The PA is designed in IHP SG13G2 BiCMOS process. The technology features high performance 130 nm HBTs with a specified f_T/f_{max} of 300/450 GHz. The collector-emitter breakdown voltage, BV_{CEO}, equals 1.7 V and collector-base breakdown voltage, BV_{CBO}, equals 4.8 V.

Amplifier Design

Fig. 13 shows the circuit diagram of the designed PA. T_1 (g_m transistor) and T_2 (cascode transistor) have been biased in class AB mode. T_2 operates in weak avalanche region with its base terminated with a very low impedance (AC ground). SiGe HBT cascode PAs designed in this fashion with low upper base resistance allow large-signal collector voltage excursions beyond BV_{CEO} without occurrence of catastrophic damage and without impact to long-term hot-carrier reliability [5.3]. Device sizes and bias current are optimized through load pull simulations to achieve output power around 17 to 18 dBm. The base node of cascode transistor (T_2), which is AC grounded, is very prone to oscillation at mm-wave frequencies. Therefore, large AC ground capacitors have been laid out as close to the base as possible, and EM simulations have been performed to ensure stability. Also, the low-frequency oscillations arising due to RF chokes in the bias paths have been suppressed by shunting the bias paths with proper low-Q capacitors. Fig. 14 shows chip photo and EM simulation model.

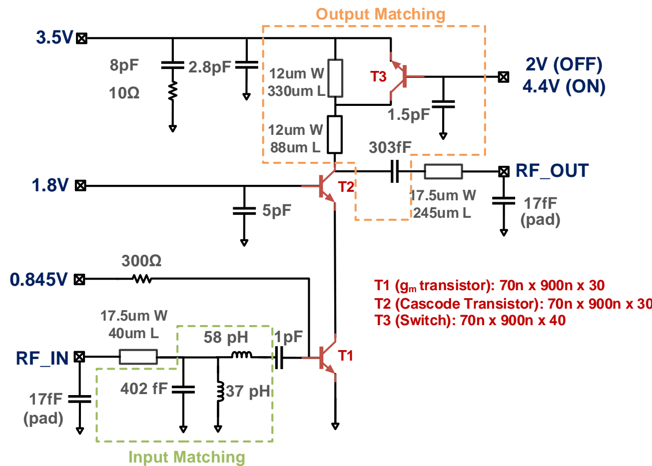

Figure 13: Schematic of the designed 28/60 GHz PA

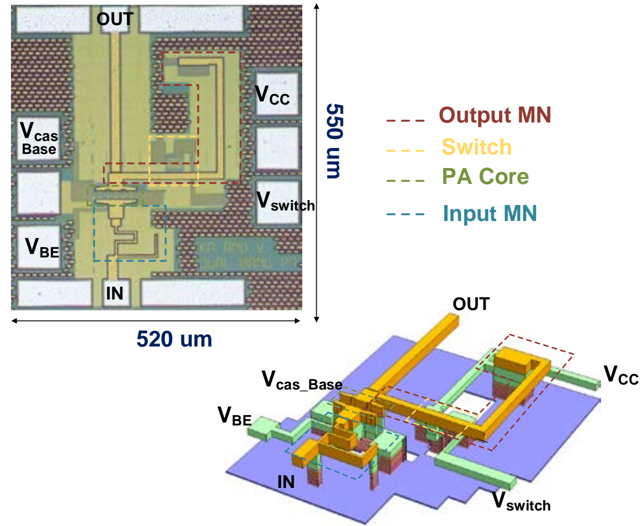

Figure 14: Chip photo and EM model in Sonnet software

Matching Network Design

The input of the PA has been dual-band matched at 28/60 GHz by employing a parallel LC tank and a series inductor. This tank resonates around 36 GHz, thereby providing positive reactance below 36 GHz and a negative reactance above 36 GHz. Therefore, the LC tank behaves as an inductor at 28 GHz and as a capacitor at 60 GHz. In essence, it's an L-type matching network with a L_{shunt}-L_{series} topology at 28 GHz and a C_{shunt}-L_{series} topology at 60 GHz, as shown in Fig. 15 (a).

The output of the PA has been dual-band matched at 28/60 GHz by using a shunt stub and series capacitor. The shunt stub is a thin film microstrip line (TFML) with an HBT switch used to tune its length. When the switch is turned OFF, the RF signal sees a longer stub length and PA switches to the 28 GHz mode. When the switch is turned ON, it shorts a part of the stub to the ground, effectively reducing the length of the TFML, as shown in Fig. 15 (b). Therefore, RF signal sees a shorter stub length and the PA switches to the 60 GHz mode.

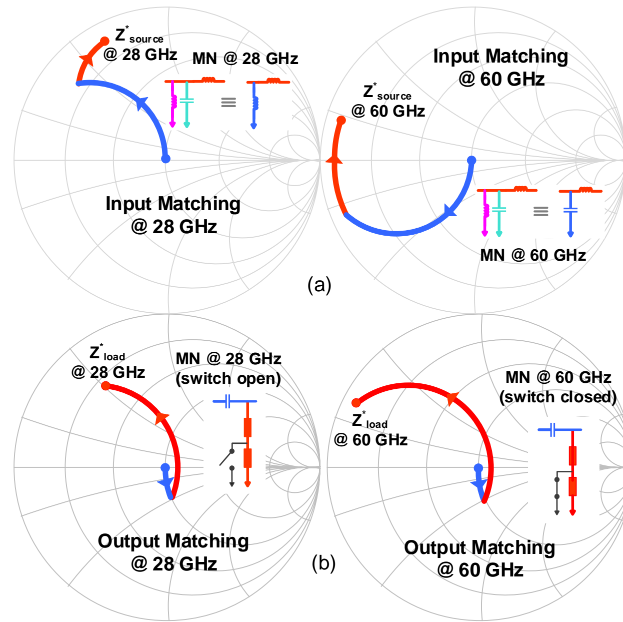

Figure 15: Dual-band matching networks (MNs). (a) Input matching network with parallel LC resonator for 28/60 GHz match, (b) Output matching network with tunable shunt stub.

Switch Design

The loss incurred by the switch in the TFML can be minimized by reducing the product I^2R_{sw}, where I is the current through the shunt stub and R_{sw} is the switch ON resistance. The current, I, depends upon multiple factors including electrical length of the stub, characteristic impedance of the stub and the location of the stub. In general, if a stub is connected to a high impedance node in the matching network, the loss would go down with a higher electrical length and higher characteristic impedance. Since the length and the placement of the stub are dictated by the matching network, they cannot be controlled. However, the characteristic impedance of the stub can be optimized. Fig. 16 (a) shows dependence of the switch loss on the characteristic impedance of the stub. As we move to low characteristic impedances, input impedance of the shunt stub decreases, which increases the switch loss; whereas for high characteristic impedances metallic loss through conductor dominates (as physical width of the conductor decreases). Therefore, there exists an optimum where the loss is minimum. Fig. 16 (b) shows this is Z_0=60 Ω in our case. Therefore, while designing the shunt stub a 60 Ω characteristic impedance is chosen, and the length is then determined according to the matching network requirement.

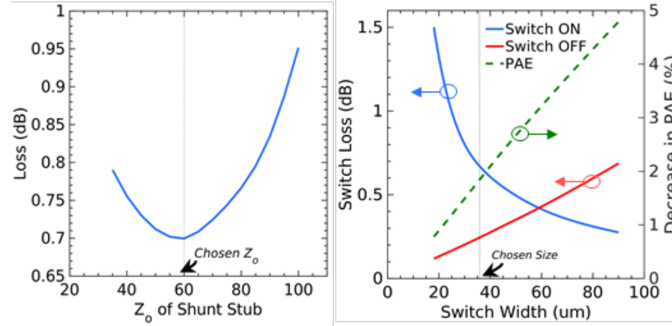

Figure 16: Tradeoffs between switch loss, switch width and characteristic stub impedance.

(a) Dependence of loss on characteristic impedance of the stub, (b) 36um wide transistor switch achieves as low as 0.7dB ON loss, 0.3dB OFF loss and 2% additional decrease in PAE due to switch bias current.

As for the switch ON resistance, R_{sw}, it can be minimized by increasing the switch size. However, there is a trade-off between the ON resistance, OFF resistance and OFF capacitance. Since the transmission line itself is a distributed element, the capacitance of the switch in the OFF state can be absorbed into the transmission line, allowing for much larger transistors to be used with lower ON resistance. After a certain size, the reduction in insertion loss in ON state (due to decrease in ON resistance) becomes insignificant whereas the increase in insertion loss in OFF state (due to proportional decrease in OFF resistance) becomes significant. Also, at large switch size, there is additional drop to PAE due to the switch bias current. Fig. 16 (b) captures these tradeoffs. Based on these tradeoffs, switch size of 0.09 x 36 mm^2 is chosen which results in 0.7dB loss in ON state, 0.3dB loss in OFF state and 2% additional decrease in PAE due to switch bias current.

An additional concern is the linearity of the switch. This is critical in the OFF state, as the AC voltage present at the TFML (the collector of T_3 in Fig. 13), leaks to the base of the switch and develops a base-emitter differential, which may self-actuate the switch. This can be alleviated by applying a reverse bias on the switch. Fig. 17 plots 1-dB compression point of the switch against reverse bias applied to it. The reverse emitter-base breakdown limit for HBT in this process is -1.6V, therefore we use a V_{BE} of -1.5V, which gives 23 dBm compression point which is far higher than the PA 1dB output compression point of 15.5 dBm. Therefore, the linearity of the PA is not affected, and switch is not operated beyond its breakdown limit. It should be noted that a negative bias of -1.5 V is achieved by applying an OFF-state voltage of 2 V, because the emitter is connected to a supply of 3.5 V, therefore no actual negative potential is required.

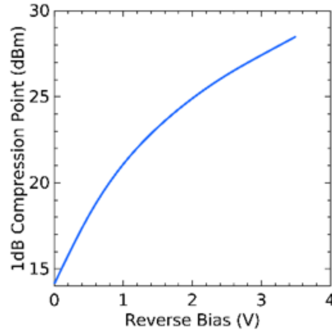

Figure 17: 1-dB compression point of switch against reverse bias during OFF state

Small signal measurements have been performed using Keysight N5227A PNA network analyzer which is calibrated using SOLT standards from 0.1MHz to 67 GHz range. Fig. 18 (a) and (b) shows measured and simulated s-parameters at 28 GHz and 60 GHz respectively. Measured gain at 28/60 GHz is 16.2/11.8 dB and measured input return loss is -8/-19 dB. To measure the output power, input of the PA is excited using a Keysight E8257D analog signal generator and the output is measured using Keysight N9010B EXA signal analyzer. Fig. 18 (c) shows measured and simulated PAE at 28/60 GHz and Fig. 18 (d) shows measured and simulated output power at 28/60 GHz. Due to the measurement setup, there is measurement uncertainty of ± 0.2 dB in the output power which also adds uncertainty of ± 1.5 % to the peak PAE. The PA shows simulated P_{sat} of 18/16.5 dBm and simulated peak PAE of 32/22 % at 28/60 GHz whereas the measured Psat is 18.4/17.2 dBm and measured peak PAE is 33/21 % at 28/60 GHz.

Table 2 compares this PA with the most recent single-band and wideband PAs around 28/60 GHz frequencies. The designed PA shows state of the art performance in terms of PAE and output power. The very promising dual-band performance is achieved by minimizing switch loss, while maintaining high linearity as described in this paper. To the authors' knowledge, this is the first demonstration of dual-band PA at 28 GHz and 60 GHz.

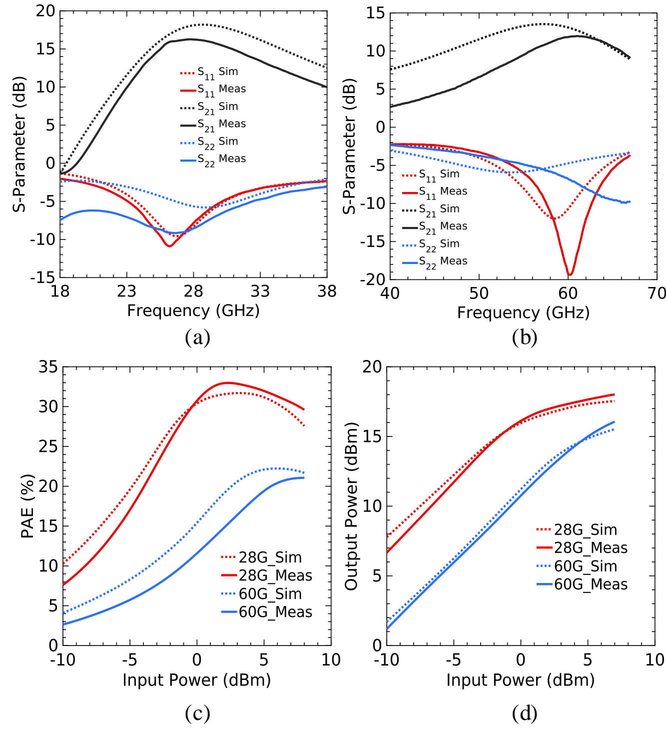

Figure 18: Simulated and measured PA results.

(a) 16 dB gain and -8dB input return loss at 28 GHz, (b) 11.8 dB gain and -19 dB input return loss at 60 GHz, (c) 33/21 % peak PAE at 28/60 GHz, (d) 18.4/17.2 dBm saturated output power (extrapolated from plots) at 28/60 GHz.

Table 2: Comparison with Recent 28GHz and 60GHz PAs

Reference		Technology	Topology	Frequency (GHz)	P_{sat} (dBm)	Peak PAE (%)	Gain (dB)	Core Area (mm^2)
Dual-band PA	This Work	130 nm SiGe	Class AB Cascode	28	18.4	33	16.2	0.1
				60	17.2	21	11.8	
Dedicated Single Band PAs	2017 ISSCC [6.3]	45 nm SOI	Cascode w/ Output Combiner	60	16.7	28.3	24	0.067
	2018 MWCL [7.3]	45 nm SOI	Cascode w/ Output Combiner	60	18.5	25.5	15	0.12
	2016 ISSCC [8.3]	130 nm SiGe	Cascode w/ Output Combiner	60	23.6	27.7	24	0.55*
	2015 ISSCC [9.3]	28 nm CMOS	Doherty	60	18.2	21	15.2	0.16
	2017 TMTT [10.3]	130 nm SiGe	Class AB Harmonically Tuned	28	18.8	35.3	15.5	0.27
	2018 MWCL [11.3]	45 nm SOI	Doherty	28	22.4	40	10	0.25*
	2018 RFIC [12.3]	45 nm SOI	Hybrid Class F/F^{-1}	28	18.6	45.7	11.4	0.14
	2018 RFIC [13.3]	90 nm CMOS	Cascode w/ Output Combiner	28	26	34	16.3	0.4
	2016 JSSCC [14.3]	28 nm CMOS	CS w/ Source Degen.	28	14	35.5	15.7	0.155
Wideband PAs	2011 TMTT [15.3]	130 nm SiGe	Distributed	DC-77	17.5	13	10	$2.2^{\#}$
	2018 PAWR [16.3]	130 nm SiGe	Distributed	12-40	21.5	20.1	14	$1.2^{\#}$
	2016 JSSC [17.3]	90 nm SiGe	Distributed	14-105	$15^{\&}$	9.7	12	$1.51^{\#}$
	2017 MWCL [18.3]	180 nm CMOS	Distributed	2-22	$14.5^{\&}$	10	11.9	$1.7^{\#}$

*estimated from figures in paper $^{\&}$OP1 dB $^{\#}$Total chip Area

4.3 K-Band Power Amplifier with Half-Gamma Reconfigurable Impedance Matching Network for Phased Array Antenna

Typical phased array antennas achieve 120° field of view [14.4], which means the beam steering range is limited to around ±60° for most of the applications. An analysis on infinite patch array by Pozar [15.4] suggests that the magnitude of reflection coefficient varies from 0 to 0.5 for scan angles up to 60° in E, H or D-plane. Therefore, the design goal is set to match any load within half-gamma around center of Smith chart. To realize a more practical circuit, only 7 impedance points (3 inductive, 3 capacitive and one nominal 50 Ω) are chosen which would be able to provide better than 0.2 magnitude mismatch (i.e., $|\Gamma|<0.2$) for all the loads in half-gamma circle. This concept is illustrated in Fig. 19.

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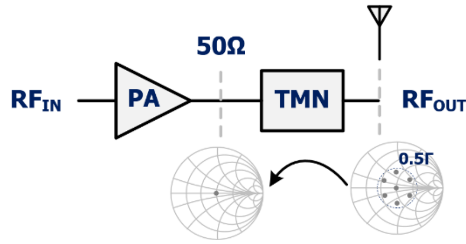

Figure 19: Simulated and measured PA results.

The power amplifier has been designed using IHP SG13G2 0.13 µm SiGe HBTs with specified f_T/f_{max} of 300/500 GHz. The amplifier uses cascode topology and operates common base transistor beyond BV_{ceo} region. Input has been matched to 50 Ω for small signal conditions whereas output has been matched to 50 Ω for maximum PAE condition determined through loadpull analysis. Input series capacitor and output shunt capacitors are de-qued to make PA unconditionally stable. Fig. 20 shows the schematic of the PA.

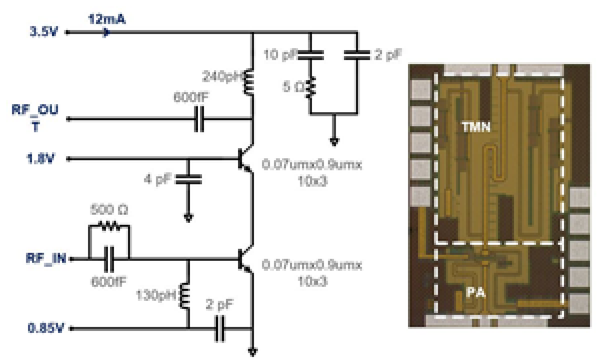

Figure 20: Power amplifier schematic and fabricated chip

To design a tunable matching network, transmission line based stubs have been preferred over varactors as the varactors provided very limited tuning range with very low Q. Double shunt stub topology (Fig. 21) has been chosen as it provides greater flexibility to move around in half-gamma circle and low loss compared to a L-sections where the series tunable element would appear in main signal path and incur more loss.

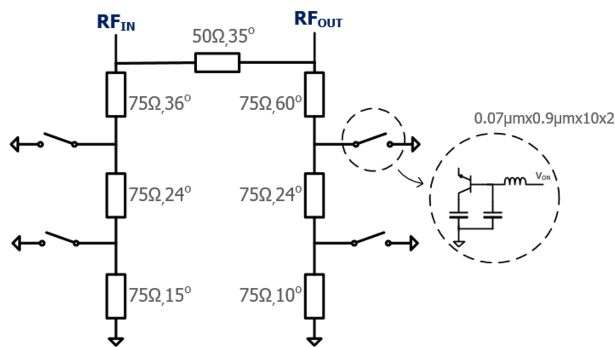

Figure 21: Tunable Matching Network

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To tune the stubs, transistor switches are used to short out the stub at various points, thus, controlling the effective length of the stub [16.4]. The transistor switches are operated in reverse saturated mode where the collector is grounded, and the emitter is connected to RF signal path. This improves the insertion loss of the switch as the emitter is physically well isolated from the conductive silicon, therefore providing better isolation [17.4]. One concern of using transistors as switches at mm-wave frequencies is the tradeoff between the on resistance and off capacitance. However, since the transmission line itself is a distributed reactive element, it can be modeled as a series of inductors and capacitors, the capacitance of transistors in their off state can be absorbed into the transmission line model, allowing for much larger transistors to be used, which reduces the on resistance. On the other hand, too big transistor would have a big off state capacitance which, in turn, would reduce the required length of transmission line to such a point that the physical separation between two switches may not be enough. Also, after a certain size, the decrease in insertion loss (due to decrease in on resistance) is not significant. Therefore, an optimum size is chosen by running simulations with different sizes. The collector of the transistor is DC blocked to avoid any static current while the switch is ON. Shunt stubs are chosen to be of high characteristic impedance to reduce the signal current going through them. This helps reducing I^2R loss of switch resistance. On the other hand, too high characteristic impedance results in smaller physical width, if the stub is realized using microstrip topology, which increases metallic losses. Therefore, 75 Ω characteristic impedance is chosen as a tradeoff between physical width and switch loss. Series stubs appear in main signal path. Therefore, standard 50 ohms is chosen as it provides reasonable physical width. The total electrical length of stubs and number of switches have been determined through simulations to cover the at least 7 impedance points as shown in Fig. 19. The switches are not operated beyond their breakdown limits.

Two sets of measurements have been performed. First, tunable matching network has been characterized by measuring small signal parameters using Agilent N5227A PNA. Fig. 22 shows the simulated and measured smith chart coverage at 26.5 GHz, which essentially means the impedances that this TMN can perfectly match to 50 Ω. The measured impedances are a bit off from the simulated impedances because of the imperfections in layout. Second, large signal measurements of PA integrated with TMN have been performed at 26.8 GHz using MT2000 (Maury Microwave) active load pull system. The 3dB compression power and peak PAE contours have been measured for each impedance point, giving total 8 datasets for PAE and 8 datasets for power, and then the maximum of power and PAE have been picked up among these datasets. The resultant contours are plotted in Fig. 23 with 5% PAE steps and 1dBm Pout steps. The max PAE contour (20%) is very wide which means the PA is able to match to different impedances within that contour and provide constant efficiency. Next, 15% PAE contour covers more than half of the Smith chart, and similarly power contours are very wide, indicating the ability of the PA+TMN to match different load impedances and provide constant performance throughout the half-gamma region. However, a drawback here is that the absolute value of max PAE and Pout is lower due to the losses in TMN.

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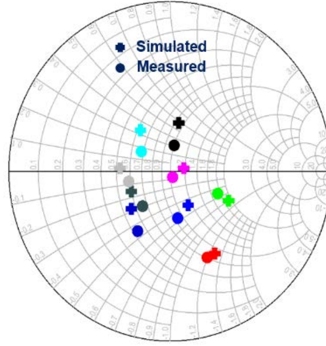

Figure 22: Measured and simulated impedance points

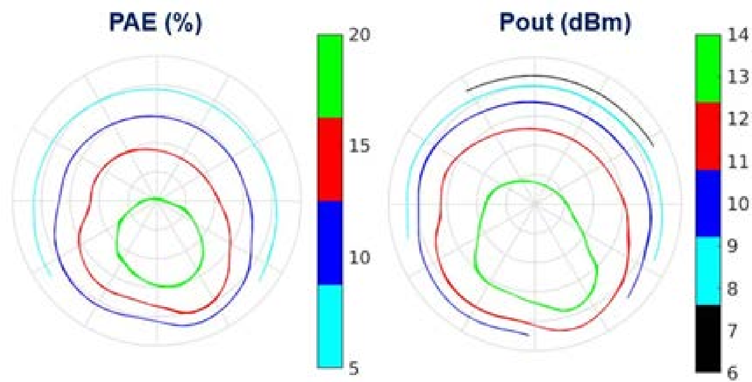

Figure 23: Measured PAE and 3dB compression Pout contours

4.4 28-60 GHz SiGe HBT LNA

The LNA was designed using two-stage cascode topology as depicted in Fig. 24. The two-stage configuration was chosen for the design because it allows for more design freedom. The first stage was optimized to reduce the NF while the second stage was utilized to boost the gain. Even though the cascode topology has a slightly higher noise than common-emitter configuration, it was chosen as it offers higher gain per stage and improves bandwidth by isolating input and output better than a common-emitter design.

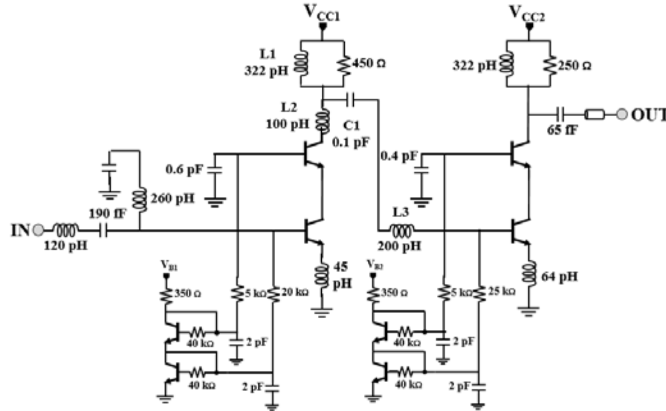

Figure 24: Circuit diagram Using the Two-stage Cascode Topology.

The input impedance of the LNA is crucial because it needs to be optimized for low noise and power match simultaneously. The transistor sizes were selected such that the optimum noise source resistance is around 50 Ω. The noise correlation susceptance is then cancelled using the inductors at the base and emitter. Since the emitter degeneration inductor, when lossless, provides a real input impedance of 50 Ω without changing the optimum noise source impedance, it was optimized to achieve a reasonable input power match [1.6].

A T-type matching topology was used for the inter-stage matching [2.6]. Since, the noise of the second stage of the 2-stage cascode is not very significant, the inter-stage matching was optimized for gain across the band. The load of the first stage includes the inter-stage matching and the input impedance of the second stage. For the inter-stage matching network (IMN), initially a series capacitor and a shunt inductor is connected at the input of the second stage to form a parallel resonance circuit with the input capacitance of the second stage that results in narrow matching as shown in Fig 25 (Step 1). In the next step, a series inductor L2 is introduced before the L1-C1 circuit that increase both the imaginary and real part of the impedance at the input of the second stage. The overall gain increases (Fig 25-Step 2) but the variation in gain response across the frequency range remains the same. Finally, another inductor (L3) is placed after L1-L2-C1 so that C2 and the input impedance in series with parallel resonance circuit that already existed, thereby generating a flat gain response (Fig 25-Step 3). The output matching was narrow band because a broader matching will cause a rapid gain roll-off at higher frequencies.

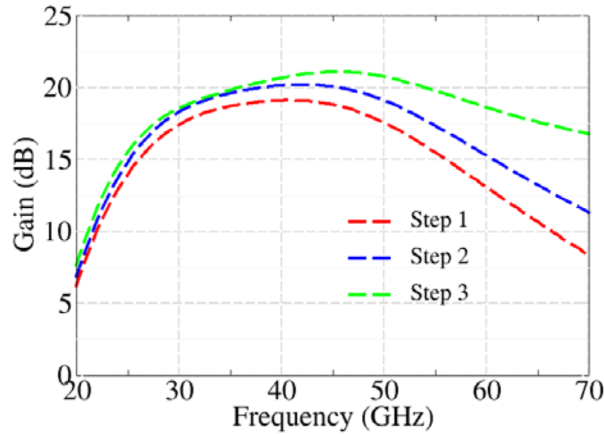

Figure 25: Simulated gain showing the step by step inter-stage matching

All the passives including the inductors and capacitors used for the input matching network (IMN), IMN and output MN were optimized by electromagnetic (EM) simulation using ADS Momentum.

The multi-band LNA chip photograph is shown in Fig. 26. The overall dimension of the chip is 610 μm × 450 μm and 510 μm × 290 μm excluding the pads. The lower transistors sizes were chosen to be 11 × 0.07 μm × 0.9 μm and 14 × 0.07 μm × 0.9 μm for the first and second stage and the upper transistors were 12 × 0.07 μm × 0.9 μm and 11 × 0.07 μm × 0.9 μm respectively. It consumes 26.8 mW from 2.5 V power supply.

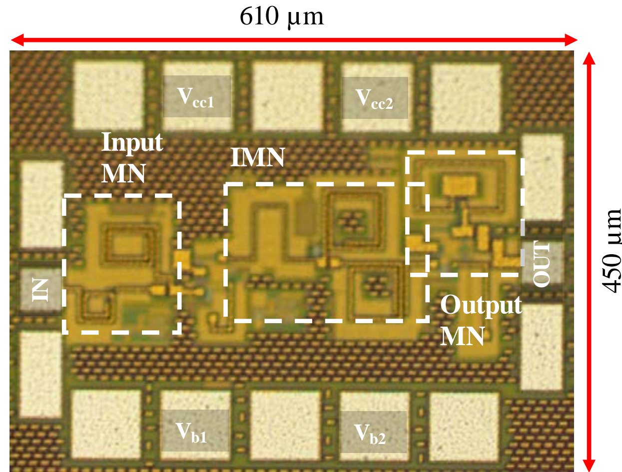

Figure 26: Chip photograph of the multiband LNA.

The measured and simulated S-parameters of the multi-band LNA is shown in Fig. 27 and 28. S-parameters were measured using the Agilent N5227A PNA Network Analyzer (for 0.1-67 GHz) and 100 μm probe pitch GSG MPI Titan probes. The measured gain of the LNA is greater than 10 dB from 22.2-65.5 GHz with maximum gain of 19.25 at 45 GHz. Gain is greater than 14 dB from 28 GHz-60 GHz with 14.5 dB and 14.1 dB at 28 GHz and 60 GHz respectively. The measured input return loss is less than -10 dB from 22-67 GHz. Fig. 29 shows that the simulated Sopt and measured conjugate of S11 are close. Fig. 30 depicts the NF and NFmin. The Mean noise figure

from 28-60 GHz is 2.87 dB with 2.361 dB at 28 GHz and 3.38 at 60 GHz. Due to equipment limitations, the linearity for the LNA were measured around K- and V-band and plotted in Fig. 31. The input-referred P1dB was found to be -27.3 dB and -18.6 dB for 28 GHz and 60 GHz.

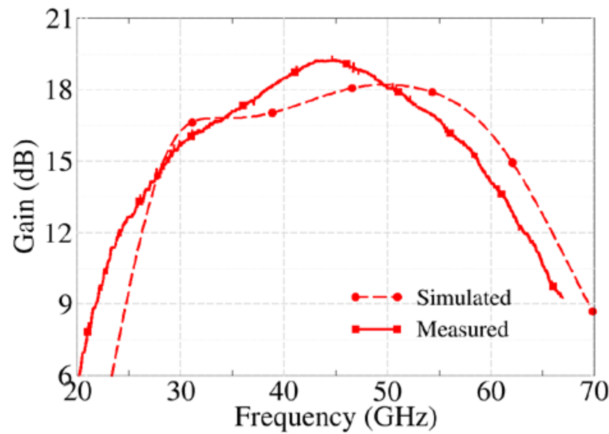

Figure 27: Measured and simulated gain of the multi-band LNA.

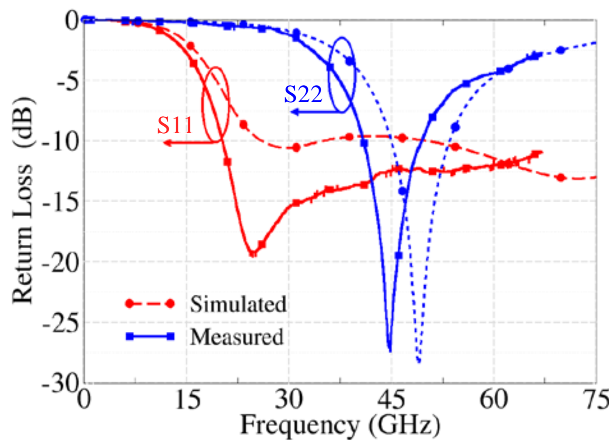

Figure 28: Measured and simulated return losses of the multi-band LNA.

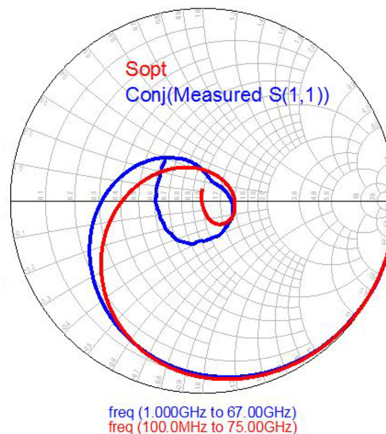

Figure 29: Simulated Sopt and conjugate of measured S11 of the LNA.

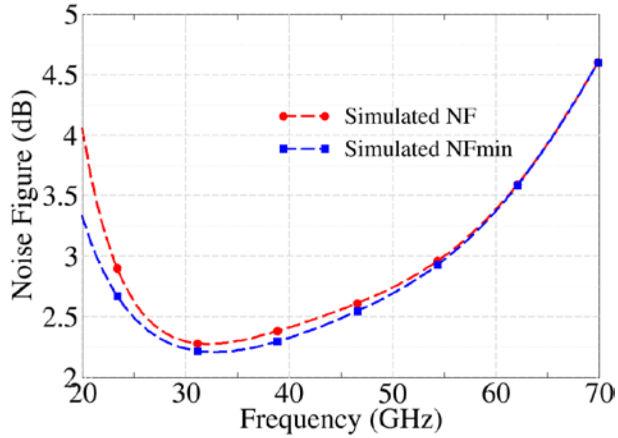

Figure 30: Simulated noise figure and minimum noise figure of the LNA.

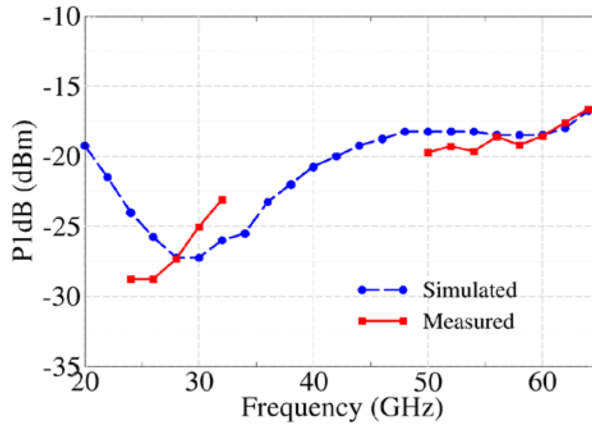

Figure 31: Simulated and measured P1dB for different frequencies.

A comparison of the realized LNA with published state-of-the-art K-band, Q-band and V-band LNA is shown in Table 3. Based on the figure-of-merit calculated, the realized LNA's performance is comparable to other designs at narrow-bands. However, the multi-band feature of this LNA is absent in all of the other published LNAs in similar silicon and SiGe technologies.

Table 3: LNA Performance Comparison

	Ref.	Technology	Frequ-ency (GHz)	Gain (dB)	Noise Figure (dB)	IP1dB (dBm)	Area (mm^2)	F.O.M.	Power (mW)
	This work	**130 nm SiGe BiCMOS**	**28-60**	**14.5 @28GHz 19.2 @45GHz 14.1 @60GHz**	**2.87* (mean) 2.36@ 28GHz 3.38@ 60GHz**	**-27.3* @ 28GHz -19@ 44GHz -18.5@ 60GHz**	**0.142**	**4.28 (K-) 8.09 (Q-) 1.94 (V-band)**	**26.8**
K-band	MTT'14 [1.6]	180 nm SiGe BiCMOS	16-24	19	2.2	-16	0.485[a]	5.63	22.5
K-band	BCTM'17 [2.6]	250 nm SiGe BiCMOS	19.25-21.5	32.8	3.5	-34.3	0.117	4.22	7
K-band	CSICS'13 [3.6]	45 nm CMOS SOI	16-24	19.5	2.2	-18.5	0.15	7.03	18.5
K-band	RFIT'15 [4.6]	90 nm CMOS	22.7-24.7	20	3.6	-	0.349	0.93	16.5
Q-band	MTT'12 [5.6]	90 CMOS (LP)	29-44	13.8 @37 GHz	3.8** @ 37 GHz	-11.1	0.4826	4.11	18
V-band	IMS'17 [6.6]	130 nm SiGe BiCMOS	55-66	15	3.3-3.6	-13.5	0.11	3.44	19.6
V-band	MWCL'16 [7.6]	180 nm SiGe BiCMOS	43-67	32.5	6[b]	-38	0.39	13.33	11.7
V-band	IJSSC'13 [8.6]	250 nm BiCMOS	47-77	22.5	6.8[b]	-17.5	0.5	2.24	52
V-band	MTT'15 [9.6]	28 nm SOI CMOS	54.5-72.5	13.8	4	-12.5	0.38	3.45	24
V-band	EuMC'13 [10.6]	90 nm CMOS	55-61	22	3.7	-23	0.6	3.62	13.5

4.5 Compact V-band Upconversion Mixer

The schematic of the upconverter mixer is shown in Fig. 32. It consists of a double-balanced Gilbert cell core with two on-chip transformer baluns at the LO and RF ports. The input IF port is differential for monolithic integration. The transformer baluns were preferred for efficient usage of chip area, as they allow DC feeding via the center tap, and at the same time act as resonant loads at the desired frequency. However, the symmetry of the balun becomes crucial for the mixer performance. Fig. 33(a) depicts the equivalent circuit for the balun transformer including the parasitic component C_F generated due to capacitive coupling between the coils. This configuration leads to a strong asymmetry, because C_F results in different low-pass response for each half of the circuit. The upper half in Fig. 33(a), having the C_F in the feedback path, exhibits a lower corner frequency than the lower half, where C_F shunts L_{S2}, creating a low pass response with higher cut-off frequency [1.7]. The difference in cut-off frequency in each half results in amplitude and phase imbalance when operated as a balun.

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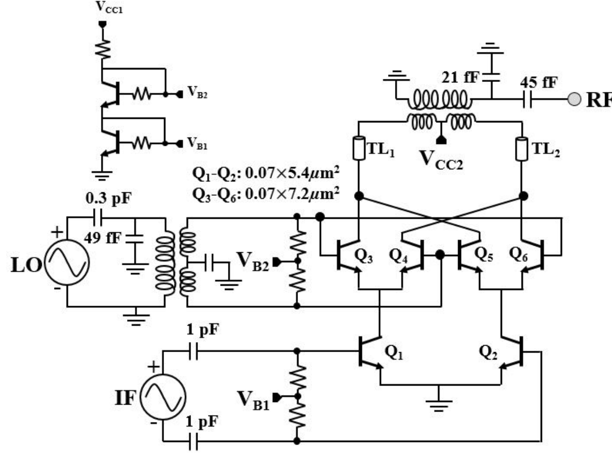

Figure 32: Circuit diagram of the V-band Upconverting Mixer.

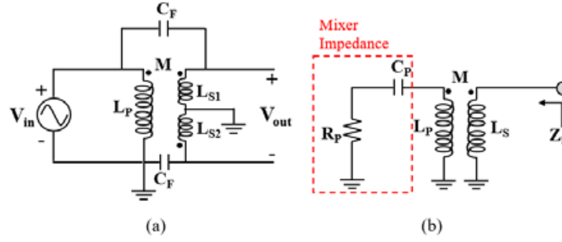

Figure 33: Transformer (a) as a balun including capacitive coupling between the windings, (b) resonant load connected to mixer output.

The simplest approach to reduce the impact of C_F is to minimize the transformer dimensions. This, however, will reduce the coupling factor of the transformer, significantly limiting the bandwidth of the circuit. The impact of low coupling factor is analyzed through the circuit shown in Fig. 33(b). Here, we assume the transformer is connected to an arbitrary complex load modeled by a resistor and capacitor; for instance, this could be seen as the output impedance of the mixer. When we analyze the resulting impedance Z_S, we acquire the following expression:

Here, M is the mutual inductance with $M = k\sqrt{L_P L_S}$ and k is the coupling coefficient. From this

$$Z_S = \frac{C_P M^2 \omega^2 + C_P M^2 \omega^2 L_P R_P}{(1 + R_P C_P L_P)^2 + (\omega C_P L_P)^2} + j\omega \left[L_S - \frac{{C_P}^2 M^2 \omega^2 L_P}{(1 + R_P C_P L_P)^2 + (\omega C_P L_P)^2} \right] \quad (6)$$

expression, we see that the real part of Z_S is proportional to the square of M, while the imaginary part is inversely proportional to the square of M. The outcome of this analysis is that a too small coupling factor will result in a mostly imaginary impedance, requiring a high-Q, possibly higher order matching network. On the other hand, a too large transformer will perform poorly as a balun, due to the capacitive coupling between the windings. In order to demonstrate this effect, simulations of various transformer baluns are provided in Table 4. In Fig. 34(a) details of the designed transformer are presented.

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Table 4: Different Transformer-based Balun Dimensions

Metal Layers	Wo	Lo	Coup-ling factor	Imbalance	
				Amp. (dB)	Phase (°)
TM2-TM1	37	37	0.39	0.5	1
TM2-TM1	56.5	78	0.504	3.47	3.67
TM2-TM1	85	85	0.62	5.127	9
TM1-M5+M4	52.5	68	0.62	0.85	4.5
TM1-M5+M4	56.5	78	0.695	4.51	8.66

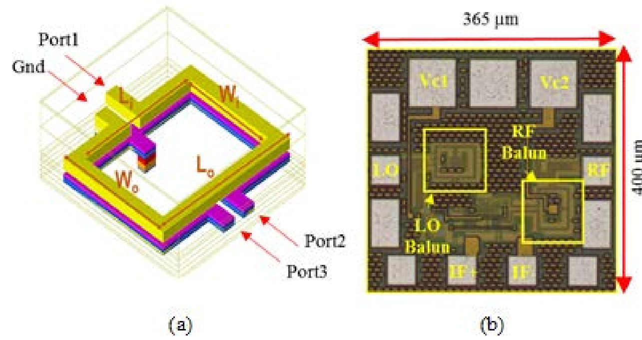

Figure 34: (a) Transformer balun used for LO and RF ports, (b) Chip micrograph of the upconverting mixer.

The baluns are designed in two basic configurations either using the two top-most metals (TM2-TM1) or using a top-metal layer with two lower layers tied together (TM1-M5+M4). A broad-side coupled design is preferred, as sufficient coupling can be achieved while enabling a very compact implementation. The width of the coils was chosen to be 3 µm to achieve desired coupling factor, without contributing too much to the capacitive coupling between the stacked coils. The simulation results confirm the predictions; a larger transformer yields a higher coupling factor but a stronger imbalance. As the transformer size is reduced, balun performance improves, but low coupling factor converts the mixer impedance to a high-Q point. For instance, for a k=0.4, the mixer output impedance is converted from $11 - j * 109\ \Omega$ to $3 + j * 28\ \Omega$, whereas for k=0.6, the output impedance is converted to $18 + j * 50\ \Omega$. Based on these studies, we choose the TM1-M5+M4 transformer with a coupling factor of 0.6, trading off circuit size, balun performance and bandwidth. By providing sufficient coupling factor, the rest of the matching network design, as shown in Fig. 32, is significantly simplified, and a simple network consisting of a shunt capacitor and series transmission line that performs the connections to the measurement pads is sufficient. The same balun was used for the RF and LO ports but rotated 90º to better fit the floor plan. The baluns are highlighted on the chip micrograph shown in Fig. 34(b).

The emitters of the transconductance stage are grounded forming a pseudo-differential pair that saves voltage headroom and offers larger dynamic range. Moreover, the output RF balun does not introduce any distortion to the RF signal and hence preserves linearity [2.7], [3.7].

The V-band upconverter mixer chip was realized in 0.13-μm IHP Microelectronics SG13G2 BiCMOS process with 300 GHz-f_T / 500 GHz-f_{MAX} occupying a total area of 0.146 mm^2 (0.052 mm^2 without pads). The mixer operates from a 2.5 V supply and consumes a total of 52 mW DC

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power. The conversion gain is obtained by sweeping the LO frequency from 49-66 GHz with 3 dBm LO power while keeping the IF frequency constant at 1 GHz. Fig. 35 displays the measured conversion gain vs. the RF frequency. The mixer provides a maximum gain of 13.4 dB at 57 GHz and a 3-dB bandwidth from 50 to above 67 GHz. The output power is measured at 60 GHz and is shown in Fig. 36. The mixer achieves an OP1dB of -1.4 dBm and at 3-dB compression it can deliver 0.61 dBm output power with -8.2 dBm IF input power. Fig. 36 also shows the measured OP1dB for different bias currents. The realized mixer has the smallest chip area when compared to other state-of-the art circuits, as can be seen in Table 5. It also exhibits the best linearity except [4.7] but they require much larger chip area and more power than this mixer. The measured IF frequency bandwidth is shown in Fig. 37(a). It can be seen that the IF bandwidth depends on the RF bandwidth and has a 3-dB bandwidth of 0.5-8.5 GHz on both sidebands with 59 GHz LO that corresponds to 50-67 GHz RF. Fig. 37(b) displays the measured return loss for the RF and LO ports. The LO port and RF port return loss are less than -10 dB and -5 dB from 50-67 GHz.

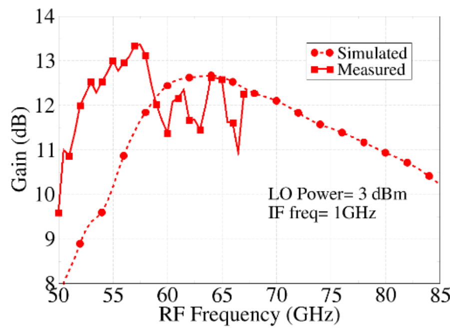

Figure 35: Conversion gain vs. RF frequency with constant IF.

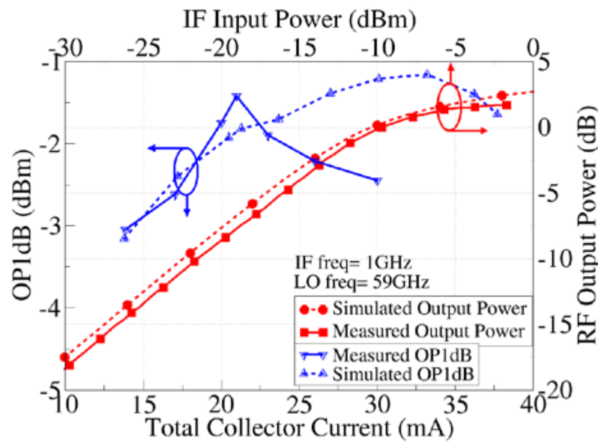

Figure 36: OP1dB for different bias current at 60 GHz RF frequency (left and bottom axis) and RF output power as a function of IF input power (right and upper axis).

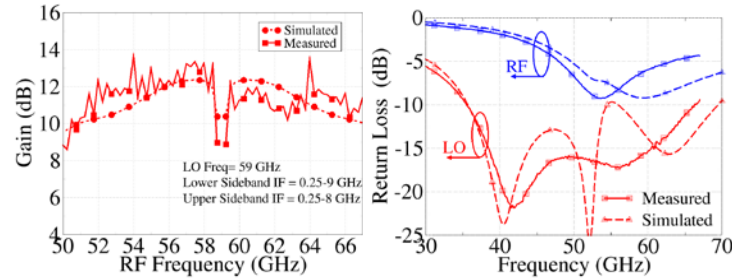

Figure 37: Measured and Simulated (a) Gain as a function of RF frequency with constant LO frequency and (b) Returns loss of LO and RF ports.

Table 5: V-band Performance Comparison

	Freq. (GHz)	Frac. BW (%)	Technology	CG (dB)	OP1dB (dBm)	Power (mW)	Chip size (mm²)	LO input (dBm)	Topology
This work	50-67 (meas.) 54-85 (sim.)	29 (meas.) 45 (sim.)	130 nm SiGe	13.4 * @57 GHz 11.38 @60 GHz	-1.4	52 66 $	0.146 (with pads) (0.365x0.4) 0.052 (0.175x0.3)	3 @ 59GHz	Gilbert Cell with on-chip transformer baluns
IMS'14 [4]	71-86	19	130 nm SiGe	1.5	1	80	1.8	3	Multi-tanh
MWCL'17 [5]	57-66	14	130 nm SiGe	-2.5	-2.1+	27	0.22	0	Mixing stage only
RFIC'06 [6]	35-65	60	180 nm SiGe	-7 ± 1.5	-25 @40GHz	14	0.27	5	Gilbert Cell Mixer
RFIT'07 [7]	60	-	250 nm SiGe	-6.5	-6	82.5	1.21	0	Micromixer
RFIC'08 [8]	58-62	7	65 nm CMOS	-7.5	-6.5	29	0.98	5	Gilbert cell with current steering
MOTL'16 [9]	53-65	20	90 nm CMOS	0.78	-11	27.8	0.75	NR	Gilbert-Cell
E. Lett.'08 [10]	59-65	10	130 nm CMOS	2 ± 2	-5.6	24	0.15	0	Gilbert Cell
IMS'10 [11]	15-50	107	180nm CMOS	-14.5 ± 1.5	-11.5- -7.5 (-10)	0	0.2	10	Resistive Ring Mixer
MTT'12 [12]	40-108	92	90nm LP CMOS	0 ± 2	-12 @60GHz	9.6	0.23	0	Weak inversion ring mixer with IF buffer
MOTL'12 [13]	30-65	74	150 nm pHEMT	2.22 ± 1.5	-2.4 @40GHz	105	1.68	2	Gilbert Cell

*maximum $including bias circuit +calculated from OIP3=OP1dB+9.6 dBm

4.6 Compact 24-32 GHz Linear Upconverting Mixer

The circuit schematic of the upconverter mixer is displayed in Fig. 38. It employs a double-balanced Gilbert cell topology that inherently suppresses the even-order harmonics and provides better IF to RF and LO to RF isolation. The input of the mixer is chosen to be differential for common mode cancellation and power supply rejection. Transistors Q1-Q4 for the switching core are chosen to be small to enable faster switching [2.5] and Q5-Q6 are chosen to provide high gain and linearity. On-chip transformer baluns were used to convert single-ended LO input to differential LO signal and differential RF signal to single ended output. The transformers were realized by stacking the primary and secondary coils on top of each other using adjacent metal layers rather than placing side-by-side in the same layer. The advantage of using the stacked configured transformer in comparison with other transmission-line based passive baluns are smaller size and better output balance without sacrificing the coupling factor [3.5]. Another challenge was to lay out the chip to allow LO, RF, IF and DC probing so that it can be characterized on-chip. Accordingly, the lengths and widths of the LO and RF baluns had to be tailored to maximally use the pad limited chip area while maintaining the balanced performance of the balun.

Also, the inductance of the RF transformer balun was designed to act as the load for the mixer core. Finally, the capacitors C1, C2 and C3 are used at the LO and RF ports to improve matching at design frequency.

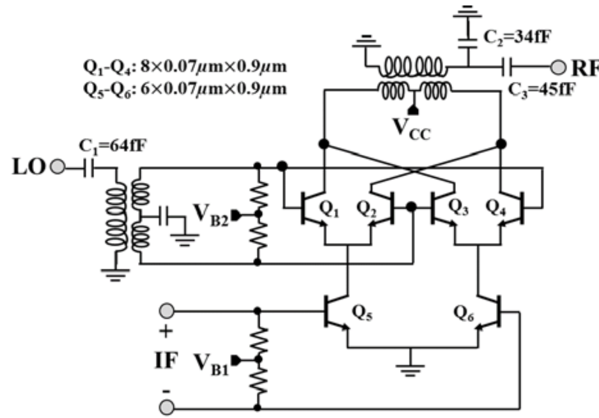

Figure 38: Circuit diagram of the 24-32 GHz Upconverting Mixer.

The upconverter mixer chip was fabricated using the 0.13-μm IHP Microelectronics SG13G2 BiCMOS process with 300 GHz-f_T / 500 GHz-f_{MAX}. The thick top two layers were stacked as the primary and secondary coils of the transformers. All the passives (including the LO and RF baluns and MIM capacitors) were EM simulated using the 2.5-D ADS Momentum simulator and optimized to enhance the performance of the mixer. Fig. 39(a) and Table 6 shows the dimensions of the LO and RF baluns. The simulated coupling factor of the LO and RF baluns are 0.6 and 0.59. They are highlighted on the chip photograph given in Fig. 39(b). The values of C1, C2, C3 and the device sizes are shown in Fig. 38 and were chosen to give a total collector current of 29.2 mA.

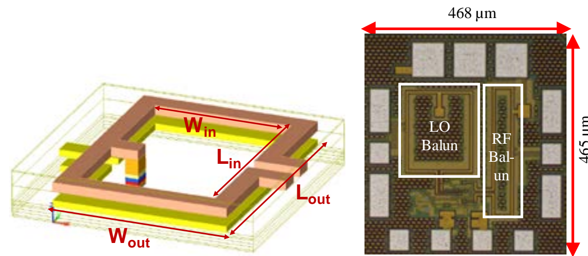

Figure 39: (a) Transformer balun used at LO and RF ports and (b) Chip photograph of the fabricated upconverting mixer.

Table 6: Balun Dimensions

	Win (μm)	Wout (μm)	Lin (μm)	Lout (μm)	Coupling factor
LO	149	161	171	183	0.6
RF	39	51	281	293	0.59

The realized chip of the upconverting mixer is shown in Fig. 39(b) and has a total area of 0.218 mm^2. The mixer operates with a 2.5 V supply and consumes a total of 90mW DC power. The measurement setup consists of a Keysight E8257D signal generator with an off-chip balun from

Marki Microwave as the IF input, Agilent N5227A PNA Network Analyzer in CW-mode as LO input and a Keysight EXA Signal Analyzer for measuring the RF output. 100-µm probe pitch GSG probes from GGB Picoprobes were used for chip probing. The performance of the upconverter mixer are displayed in Figs. 40, 41, and 42.

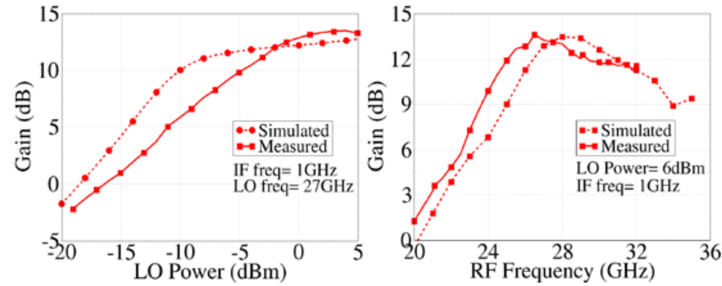

Figure 40: Measured and Simulated gain (a) as a function of LO power and (b) as function of RF frequency as IF frequency is kept constant.

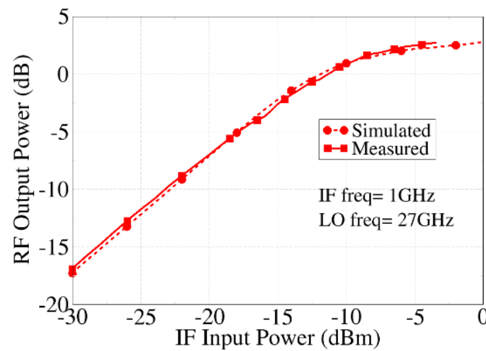

Figure 41: Measured and Simulated RF output power as a function of IF input power.

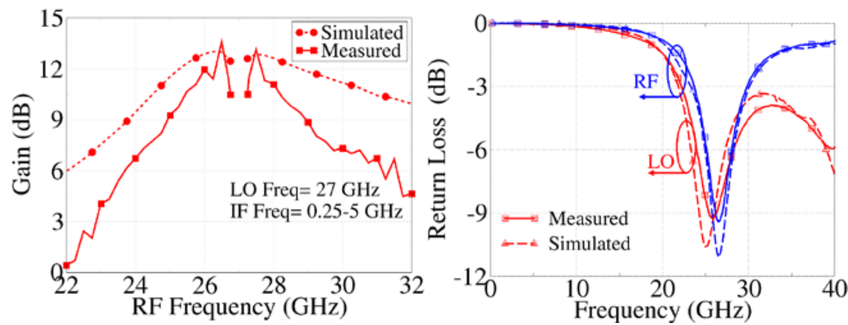

Figure 42: Measured and Simulated (a) Gain as a function of RF frequency as LO frequency is kept constant and (b) Returns loss of LO and RF ports.

To find an optimum value, the LO power of the mixer is swept at 27 GHz LO frequency and at 1 GHz IF frequency and the gain is plotted as shown in Fig. 40(a). It is found that the gain remains constant beyond 2 dBm LO power. The conversion gain as a function of RF frequency is plotted in Fig. 40(b) with constant 1 GHz IF frequency and swept LO frequency of 6 dBm power. Maximum gain of 13.7 dB at 26.5 GHz, 13 dB gain at 28 GHz and a 3-dB bandwidth from 24-32 GHz RF frequency were measured. The RF output power is displayed in Fig. 41. The mixer has

an OP1dB of -1.5 dBm at 28 GHz and can deliver 0 dBm power at -11 dBm IF input power. In terms of OP1dB, the designed circuit outperforms most of the other mixers in similar processes except [4.5], [5.5] and [6.5]. However, since all these use various methods to boost linearity, their chip areas are at least 3.5 times larger than this designed mixer. Only [7.5] has smaller chip area than the one in this work but the linearity is very poor. A comparison of the realized mixer with the state-of-the art circuits are listed in Table 7. Fig. 42(a) shows the measured IF frequency bandwidth of 0.25-1.25 GHz on both sidebands with 27 GHz LO frequency. The return loss for the RF and LO ports is shown in Fig. 42(b) and is lower than -9 dB around 28 GHz.

Table 7: K-band Performance Comparison

	Freq. (GHz)	**Technology**	**CG (dB)**	**OP1dB (dBm)**	**Power (mW)**	**Chip size (mm^2)**	**LO input (dBm)**	**Topology**
This work	24-32	130 nm SiGe BiCMOS	13.7* @ 26.5GHz 13 @ 28GHz	-1.46 @ 28GHz	90	0.21762 (0.468x0 .465)	5.96 @ 27GHz	Gilbert Cell with on-chip transformer baluns
[8]	10-40	130 nm SiGe BiCMOS	3 @ 40GHz	-9 (calc.)	93	0.544	-7	Gilbert Cell
[4]	21-25	180 nm SiGe BiCMOS	27.5± 2.5	1.36	72	1.08	-2	Gilbert Cell
[9]	30-35	180 nm SiGe BiCMOS	24.5± 2.5	-2.4 @35GHz	72	NR	0.6	Gilbert Cell
[10]	19-31	180 nm SiGe BiCMOS	-0.8	-8.6	38	1	-4	Modified Gilbert Cell with series-conn. triplet at IF port
[5]	27.5-43.5	65 nm CMOS	-5	0.42	14	0.686	5	Modified Gilbert Cell
[6]	23.4-29.2	130 nm CMOS	-1.9	0.3	22.8$ (core)	0.86	0	Gilbert Cell with a low distortion Gm-stage
[11]	25-27.5	130 nm CMOS	1.3	-21.7	3.9	NR	NR	Current-mode Mixer
[12]	18-28	130nm CMOS	-2- 0.7	-7- -5.2	8	0.47	3	Dual gate
[7]	15-50	180nm CMOS	-14.5± 1.5	-11.5- -7.5	0	0.2	10	Resistive Ring Mixer
[13]	30-65	150 nm GaAs pHEMT	2.22± 1.5	-2.4 @40GHz	105	1.68	2	Gilbert Cell

*maximum $39.3 mW for core+LO buffer

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5.0 CONCLUSIONS

Stacked transistor PAs where only the output transistor is loaded with a harmonic termination network does not result in significant overall PAE enhancement. This letter shows that the more the number of stacked transistors, the lesser the improvement in PAE. This, in part, has to do with the fact that voltage swing is shared between each transistor in a stacked power amplifier; but also due to the reduction of impedance presented by the emitters moving downward in the stack. Our analysis furthermore shows importance of correct base termination that can lead to a higher impedance at the emitter.

A dual-band PA operating in 28 GHz and 60 GHz mode was reported. The PA employs cascode topology, LC tank at input matching network and tunable stub at the output matching network to shift the frequency of operation between 28 GHz and 60 GHz. Performances in each band are comparable to single band state of the art PAs. The designed PA is suitable for 5G transceivers or dual-band phased array radars.

This work demonstrates a tunable matching network integrated with the PA at K-band for the purpose of eliminating mismatch between PA and antenna due to scan impedance variation in a phased array system. The matching network uses double shunt stub topology to reduce losses and covers half-gamma area in Smith chart. The measured results confirm feasibility of this approach by showing wide and expanded PAE and Pout contours. The proposed integrated impedance matching networks can also be used to tune the center frequency of the PA or compensate for variations in the active device parameters due to temperature drift or fabrication tolerances or on-chip load pull purposes.

A multi-band LNA for K-, Q- and V-band has been designed and characterized. The LNA exhibits more than 14 dB gain from 28-60 GHz and the input return loss of less -10 dB from 22-67 GHz. The mean NF for the LNA is 2.87 dB for 28-60 GHz. In terms of bandwidth, multi-band functionality and NF, the realized LNA shows better performance than other state-of-the-art LNAs in similar technologies.

A compact V-band upconverting mixer with on-chip transformer-based LO and RF balun is presented. The mixer was realized using the 0.13-µm IHP SiGe process and occupies only 0.052 mm^2 excluding the pads. It has a maximum conversion gain of 13.4 dB at 57 GHz, OP1dB of -1.4 dBm at 60 GHz, and can deliver 0.61 dBm output power with -8.2 dBm IF input power. The realized mixer outperforms the state-of-the-art mixers in similar technologies in terms of chip area, bandwidth and linearity.

A 24-32 GHz upconverting mixer using 0.13-µm SiGe process has been designed and characterized. The topology is based on double-balanced gilbert cell and transformer type RF and LO baluns. It has a maximum conversion gain of 13.7 dB at 26.5 GHz, OP1dB of -1.5 dBm at 28 GHz and occupies only 0.218 mm^2 area. The realized mixer outperforms most of the state-of-the-art mixers in similar technologies as shown in Table 7.

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LIST OF ACRONYMS

5G	Fifth Generation Wireless Communication
AB	Amplifier in class AB mode
AC	Alternating Current
BICMOS	Bipolar/Complementary Metal Oxide Semiconductor combinations
BV	Breakdown Voltage
CMOS	Complementary Metal Oxide Semiconductor
CW	Continuous Wave
DC	Direct Current
EM	Electromagnetic
FCC	Federal Communications Commission
GSG	Ground-Signal-Ground
GSM	Global System for Mobile Communications
HBT	Heterostructure Bipolar Transistor
IC	Integrated Circuit
IF	Intermediate Frequency
III-V	Group III and Group V Compound Semiconductors
IMN	Inter-stage Matching Network
IMN	Input Matching Network
LC	Inductor-Capacitor
LNA	Low-Noise Amplifier
LO	Local Oscillator
MEMS	Micro-Electro-Mechanical Switch
MIM	Metal-Insulator-Metal Capacitor
NF	Noise Figure
PA	Power Amplifier
PAE	Power-Added Efficiency
PNA	Performance Network Analyzer
Pout	RF Output Power
RF	Radio Frequency
SiGe	Silicon-Germanium
SOI	Silicon-on-Insulator
SOLT	Short, Open, Load, Through Calibration
TFML	Thin-Film Microstrip Line
TMN	Tunable Matching Network
Vbe	Base-Emitter Voltage
Y	Admittance
Z	Impedance

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