AFRL-RI-RS-TR-2019-089

MULTIFUNCTIONAL NANOTECHNOLOGY RESEARCH

APRIL 2019

FINAL TECHNICAL REPORT

APPROVED FOR PUBLIC RELEASE; DISTRIBUTION UNLIMITED

STINFO COPY

AIR FORCE RESEARCH LABORATORY
INFORMATION DIRECTORATE

■ **AIR FORCE MATERIEL COMMAND** ■ **UNITED STATES AIR FORCE** ■ **ROME, NY 13441**

NOTICE AND SIGNATURE PAGE

Using Government drawings, specifications, or other data included in this document for any purpose other than Government procurement does not in any way obligate the U.S. Government. The fact that the Government formulated or supplied the drawings, specifications, or other data does not license the holder or any other person or corporation; or convey any rights or permission to manufacture, use, or sell any patented invention that may relate to them.

This report was cleared for public release by the 88th ABW, Wright-Patterson AFB Public Affairs Office and is available to the general public, including foreign nationals. Copies may be obtained from the Defense Technical Information Center (DTIC) (http://www.dtic.mil).

AFRL-RI-RS-TR-2019-089 HAS BEEN REVIEWED AND IS APPROVED FOR PUBLICATION IN ACCORDANCE WITH ASSIGNED DISTRIBUTION STATEMENT.

FOR THE CHIEF ENGINEER:

/ S /
JOSEPH A. CAROLI
Chief, High Performance Systems Branch
Computing & Communications Division

/ S /
QING WU
Technical Advisor, Computing
& Communications Division
Information Directorate

This report is published in the interest of scientific and technical information exchange, and its publication does not constitute the Government's approval or disapproval of its ideas or findings.

REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

The public reporting burden for this collection of information is estimated to average 1 hour per response, including the time for reviewing instructions, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the collection of information. Send comments regarding this burden estimate or any other aspect of this collection of information, including suggestions for reducing this burden, to Department of Defense, Washington Headquarters Services, Directorate for Information Operations and Reports (0704-0188), 1215 Jefferson Davis Highway, Suite 1204, Arlington, VA 22202-4302. Respondents should be aware that notwithstanding any other provision of law, no person shall be subject to any penalty for failing to comply with a collection of information if it does not display a currently valid OMB control number.
PLEASE DO NOT RETURN YOUR FORM TO THE ABOVE ADDRESS.

1. REPORT DATE *(DD-MM-YYYY)*	2. REPORT TYPE	3. DATES COVERED *(From - To)*
APRIL 2019	FINAL TECHNICAL REPORT	OCT 2013 – SEP 2018

4. TITLE AND SUBTITLE

MULTIFUNCTIONAL NANOTECHNOLOGY RESEARCH

5a. CONTRACT NUMBER IN-HOUSE: R18K

5b. GRANT NUMBER N/A

5c. PROGRAM ELEMENT NUMBER 61102F

6. AUTHOR(S)

Joseph E. Van Nostrand

5d. PROJECT NUMBER T2NR

5e. TASK NUMBER IH

5f. WORK UNIT NUMBER N2

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)

Air Force Research Laboratory/Information Directorate
Rome Research Site/RITB
525 Brooks Road
Rome NY 13441-4505

8. PERFORMING ORGANIZATION REPORT NUMBER

N/A

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)

Air Force Research Laboratory/Information Directorate
Rome Research Site/RITB
525 Brooks Road
Rome NY 13441-4505

10. SPONSOR/MONITOR'S ACRONYM(S)

AFRL/RI

11. SPONSORING/MONITORING AGENCY REPORT NUMBER

AFRL-RI-RS-TR-2019-089

12. DISTRIBUTION AVAILABILITY STATEMENT

Approved for Public Release; Distribution Unlimited. PA# 88ABW-2019-1732
Date Cleared: 15 APR 2019

13. SUPPLEMENTARY NOTES

14. ABSTRACT

The objective of this effort was to utilize emerging nanoelectronics with advanced computing and neuromorphic architectures as a vehicle to explore research and development, and deployment of nanotechnology based information analysis systems utilizing the emerging disciplines of nanoscience and nanoengineering.

15. SUBJECT TERMS

nanoelectronics, CMOS, memristor, crossbar

16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT	18. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON
					JOSEPH E. VAN NOSTRAND
a. REPORT	b. ABSTRACT	c. THIS PAGE			19b. TELEPHONE NUMBER (*Include area code*)
U	U	U	UU	32	N/A

Table of Contents

1. SUMMARY **1**

2. INTRODUCTION **2**

3. METHODS, ASSUMPTIONS AND PROCEDURES **4**

3.1 FABRICATION **4**
3.1 METROLOGY **4**
3.3 DEVICE TESTING **4**

4. RESULTS AND DISCUSSION **5**

4.1 KEY ACCOMPLISHMENTS **5**
4.2 THE SPECIFIC TASKS OF THE PROJECT INCLUDED: **5**
4.3 FABRICATION PROTOCOL FOR MEMRISTORS **5**
4.3.1 Mask design and usage *6*
4.3.2 Lithography *9*
4.3.3 Deposition *10*
4.3.4 Resist lift -off *12*
4.3.5 RRAM device stack and top electrode *12*
Top interconnect *19*
4.3.6 Bottom electrode contact pad opening *21*
4.4 DEVICE CHARACTERIZATION **22**
4.5 FINAL RESULTS **24**
4.7 PRESENTATIONS, PUBLICATIONS AND PATENT APPLICATIONS RESULTING FROM THIS PROJECT **25**

5. CONCLUSIONS **26**

6. LIST OF ACRONYMS **27**

List of Figures

FIGURE 1. IMAGE AND SCHEMATIC OF AFRL/RI HYBRID CMOS/RESISTIVE MEMORY NANODEVICES BEING DEVELOPED FOR LOW POWER LOGIC/MEMORY AND AUTONOMOUS SYSTEMS. 3
FIGURE 2: OVERVIEW OF THE FABRICATION APPROACH FOR MEMRISTOR CROSSBAR ARRAYS. 6
FIGURE 3: LAYOUT OF THE MASK 'RRAM MAIN' FOR THE BOTTOM ELECTRODE AND THE TOP INTERCONNECT. 7
FIGURE 4: LAYOUT OF THE MASK 'RRAM VIA' FOR THE BOTTOM ELECTRODE AND THE TOP INTERCONNECT. 7
FIGURE 5: LAYOUT OF THE MASK 'BE CONTACT' FOR THE OPENING OF THE BOTTOM CONTACT... 8
FIGURE 6: COMBINED LAYOUT OF THE MASKS 'RRAM MAIN', 'RRAM VIA' AND 'BE CONTACT'. 8
FIGURE 7: ILLUSTRATION SHOWING THE SPIN-ON OF THE LIFT-OFF DOUBLE STRUCTURE CONSISTING OF LOR3A AND S1813 PHOTORESIST AND THE SUBSEQUENT EXPOSURE AND DEVELOPMENT OF BE PATTERN. 9
FIGURE 8: AFM IMAGES SHOWING THE UNINTENTIONAL FORMATION OF METAL SIDE WINGS (LEFT) AND A SUCCESSFUL FABRICATED BE (RIGHT). 9
FIGURE 9: ILLUSTRATION SHOWING THE DEPOSITION OF THE BE ON TOP OF A LIFT-OFF RESIST PATTERN AND THE SUBSEQUENT REMOVAL VIA A DUAL LIFT-OFF PROCESS. 12
FIGURE 10: ILLUSTRATION SHOWING THE UNIFORM DEPOSITION OF THE SWITCHING LAYER (SL), OXYGEN GETTER LAYER (OGL) AND INERT TOP ELECTRODE ON TOP OF THE PATTERNED BE. S1813 PHOTORESIST IS SUBSEQUENTLY SPUN-ON AND EXPOSED TO DEVICE THE RRAM STACK. 13
FIGURE 11: ILLUSTRATION SHOWING THE DEVELOPMENT OF THE EXPOSED PHOTORESIST LAYER AND THE FOLLOWING REACTIVE-ION ETCH (RIE) AND SiO_2 DEPOSITION. 16
FIGURE 12: SEM IMAGES SHOWING TWO DIFFERENT RIE APPROACHES. THE LEFT IMAGE SHOWS THE USE OF A PLASMA BASED ON CF4+O2 CREATING A LARGE TAPERING ANGLE OF TUNGSTEN AND RE-DEPOSITING PARTS OF IT ON THE SL. THE RIGHT IMAGE SHOWS AN ALMOST VERTICAL ETCH WITH A PLASMA BASED ON SF6+O2. IN THIS APPROACH THE SF6 BASED PLASMA ETCHES TUNGSTEN FASTER THAN THE PHOTORESIST NOT CREATING THE CONTACT AREA FOR SPUTTERED RE-DEPOSITION. A SECOND PLASMA ETCH BASED ON AR+SF6+O2 REMOVES THE TI+HFO2 IN AN ION MILLING APPROACH. 18
FIGURE 13: ILLUSTRATION SHOWING THE PHOTORESIST REMOVAL AFTER RIE AND THE SIO2 DEPOSITION, THE SPIN ON OF THE DOUBLE LAYER CONSISTING OF MIF300 AND S1813 PHOTORESIST AND THE SUBSEQUENT EXPOSURE TO DEFINE THE TOP INTERCONNECT PATTERN. 20
FIGURE 14: ILLUSTRATION SHOWING THE DEPOSITION OF THE TOP CONTACT ONTO THE PATTERNED PHOTORESIST STRUCTURE. A DUAL LIFT-OFF OF THE S1813 PHOTORESIST AND THE LOR3A FINISHES THE TOP ELECTRODE. 21
FIGURE 15. CURRENT VOLTAGE PLOT FOR HAFNIUM OXIDE ELECTROFORMING (BLACK LINE), AND MULTIPLE SET AND RESET CYCLES (RED AND GREEN PLOTS, RESPECTIVELY). 23
FIGURE 16. RESISTANCE VALUES FOR "ON" (LRS) AND "OFF" (HRS) STATES OF A HAFNIUM OXIDE DEVICES (TOP GRAPH) AND CORRESPONDING SET AND RESET VOLTAGES FOR THE SWITCHING CYCLES (BOTTOM GRAPH). 24

1. Summary

Under this in-house effort, he AFRL/RI Nanotechnology Team explored numerous research, development, and deployment opportunities in the emerging disciplines of multifunctional nanoscience and nanoengineering for energy efficient and secure advanced computing architectures for Cyber Information Technology, and Autonomous Guidance and Control Systems. The effort consisted of a five year multidisciplinary effort focusing on research and development of nanocomputers systems utilizing alternative nanotechnology processing approaches that can deliver revolutionary computational capabilities crucial to maintaining technological progress. The research involved both modeling and simulations, as well as measurements of candidate nanoelectronics. Modeling results were compared with experimental data as a validity check, and results were published in refereed journals and conferences. The research and development under this effort explored taking advantage of advances in nanoscience and technology, such as hybrid CMOS/memristive nanoelectronics, which show great promise for smaller, faster, and reduced consumed power computing systems. Research into the electronic properties of both nanomaterials and nanoelectronics, both by modeling and simulation as well as experimental measurements, have provided insights into the possibilities and limitations of various nanocomputing architectures. Rather than providing summaries of all the research and development efforts that occurred under this in-house effort, this final technical report will focus on the detailed technical accomplishments in the CMOS fabrication process research and development that were accomplished in the last half of this in-house effort in collaboration with SUNY Poly College of Nanoscale Science and Engineering (CNSE) that have led to a front-end-of-the-line CMOS compatible “memristor” or “RRAM” process.

2. Introduction

The emerging revolution of multifunctional nanotechnology is expected to stimulate enormous improvements in IT capabilities. Computer architectures are high on the list of technologies that will benefit from nanoscale breakthroughs in the structures, properties, and performance of microelectronics. For example, critical feature sizes of a transistor have been less than 100 nm for years, and yet continued reduction in transistor dimensions is expected to continue as new material capabilities as well as new circuit architectures accentuating nanoscale properties are developed. However, the emerging trend in cyber-focused nanotechnology development is one that tends to look beyond CMOS technologies. The general consensus in this area is that the fundamental road blocks for continued enhancement of traditional approaches to transistor scaling and interconnects are very close to reality. Therefore, finding new computer architecture constructs – inventing and developing novel switching and interconnect technologies for processing information, as well as development of revolutionary new, ultra-low power spike-based neuromorphic computers – is central to the emerging barrier(s) facing the IC industry. Any new nanotechnology-based approach will initially work in conjunction with CMOS computer architecture, but the development of nanotechnology complementary to CMOS architectures will result in a major shift in IC technology and redefine improvement in commercial and military information systems in ways that far surpass CMOS alone. This research will include an on-going survey of progress in this broad but critical area of science and technology, as well as employ locally available resources and expertise that are germane to the research at hand.

The trend of increasing manufacturing costs for enhanced functionality of information processing systems is a result of the end of photolithography as the driver for Moore's Law. Subsequently, opportunities for emerging technologies, mostly nanoscale, are expected to complement and/or replace the current CMOS-based system integration paradigm. As nanotechnology is developing, there is a strong and growing need for DoD nanoscale systems scientists and engineers to exploit the SWAP and cyber security advantages enabled through nanotechnology.

Emerging research and developments at nanometer dimensions promise revolutionary technological changes for a wide range of AF and DoD applications and platforms. Nanotechnologies to be incorporated within the platforms which are directly relevant to the AF include the areas of aerodynamics, mobility, stealth, sensing, power generation and management, smart structures and materials, resilience and robustness, and augmented human performance. In addition, nanotechnologies will impact battlespace systems concerned with information and signal processing, autonomy and intelligence. With regards to information technology, in particular, substantial advantages are expected to be gained from nanotechnologies new enabling capabilities which include threat detection, novel electronic displays and interface systems, as well as a pivotal role for the development of miniaturized unmanned combat vehicles and robotics. Finally, nanotechnology will enable the development of novel materials providing the basis for the design and development of new properties and structures which will result in increased performance (for example through nano-energetics and new types of catalysts), reduced cost of maintenance (for example through wear reduction, self-healing and self-repair), enhanced functionality (for example through adaptive materials), and new types of electronic/opto-electronic/magnetic material properties.

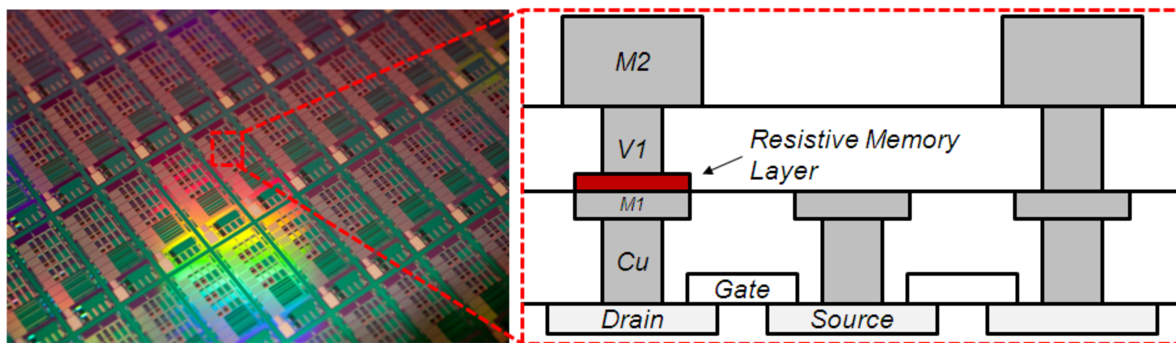

Figure 1: Image and schematic of AFRL/RI hybrid CMOS/Resistive Memory nanodevices being developed for low power logic/memory and autonomous systems.

One emerging nanotechnology that was a focus of this in-house research and development effort was the “memristor” or “RRAM” device. The memristor is a two-terminal resistive switching memory (RRAM) nanoscale device, which is recognized as the fourth fundamental electrical element in addition to resistors, capacitors, and inductors. By utilizing different resistance values to store information, memristors can function as low-power, highly-scalable device elements – critically essential properties for memory and field programmable gate array applications. More importantly, memristors have exhibited unique self-learning properties and can execute complex logic functions, which enables innovative logic, data processing, and implementation of neuromorphic systems. And, in contrast with other emerging nanoelectronic devices, memristors can utilize CMOS-compatible oxide and electrode materials, which is dramatically simplifies CMOS-memristor integration. These factors underscore the promise and feasibility of large-scale CMOS-memristor hybrid nanoelectronics and point to their significant impact on future IC applications. Game changing technologies enabled by memristor and related nanotechnologies include large-scale symbolic inference models and subsequent computing architecture implementations for affordable, agile, autonomous, and trusted systems capable of ingesting and processing big/massive data to support decision makers. Multifunctional nanoelectronics and nanomaterials involving hybrid and 3-D stacking will provide over 100X increase in computing density (Figure 1), and enable human-level computing capacity in embedded systems. On-shoring of nanofabrication capabilities will be critical to competitively enabling this functionality in domestic systems. This in-house research project resulted in the development of a unique process flow for fabricating memristors consisting of a variety of different switching oxides (including hafnium oxide, tantalum oxide, and zirconium oxide). The key elements of this emerging technology are summarized in this report.

3. Methods, Assumptions and Procedures

3.1 Fabrication

In this effort, memristor devices were built in collaboration with SUNY Polytechnic Institute in their commercial cleanroom facilities, using a variety of thin film deposition techniques, photolithography, and reactive ion etching. A detailed description of the fabrication process is provided in the results section, below.

3.1 Metrology

To monitor fabrication efforts and troubleshoot problems during device development efforts, a range of different metrology tools were used. These included scanning electron microscopy (SEM), x-ray photoelectron spectroscopy (XPS), transmission electron microscopy (TEM), and secondary ion mass spectroscopy (SIMS). These techniques were all performed in-house in collaboration with the SUNY Polytechnic Institute metrology facility.

3.3 Device Testing

For device testing, we utilized a B1500A semiconductor analyzer connected to a manual probe station capable of handling wafers or pieces of wafers. The mainframe is equipped with 4 high-resolution SMU units, a capacitive measurement unit (MFCMU) and waveform generating and fast-measurement unit (WGFMU). Memristor device characteristics were extracted by using DC-sweep as well as pulsing techniques. In both cases a 1 transistor 1 RRAM (1T1R) setup was used to limit the current through the RRAM during the set and forming operation to the saturation current of the transistor which was set by the transistor gate voltage. Mainly two kinds of transistors were used: **1.** an external JFET (Junction gate field effect transistor) which was connected to the system via a discrete Keithley transistor box and **2.** an integrated on-chip transistor which was implemented right underneath our integrated RRAM. A manual probe station was used to generate preliminary results and longtime endurance measurements. DC-sweeps were preferably used to form the devices while a self-developed pulsing software in conjunction with the WGFMU enables endurance measurement up to 10^{12} cycles while recording every single cycle. This probe station was used to generate statistical data in a short amount of time as well as perform measurements at temperatures ranging from room temperature to 300 C.

4. Results and Discussion

4.1 Key Accomplishments

The key accomplishments for this in-house research and development effort were:

1. *Development of a process flow for fabricating memristor "crossbar" architectures using various metal oxides as the switching layer.*
2. *Fabrication of memristor crossbar devices on 300mm wafers utilizing commercial CMOS compatible materials and processes, thus shortening the time to warfighter.*

4.2 The specific tasks of the in-house research and development effort included:

Optimize a fabrication process for memristor crossbar devices.

- Using a 300mm wafer platform, develop a process flow that yields functional memristive devices in a crossbar array format, that can be subsequently tested via electronic probe station and subjected to thermal fluctuation and radiation bombardment for reliability studies.

Fabricate memristor crossbar arrays for testing.

- Using methods developed in the first task to fabricate memristor crossbar arrays, then testing the device array performance under different environmental conditions (temperature and radiation bombardment).

4.3 Fabrication Protocol for Memristors

As a result of this effort, the following fabrication protocol was developed. This protocol represents several years of process development in collaboration with the SUNY Polytechnic Institute nanofabrication facility. The process consists of photolithography and reactive ion etching steps to define bottom metal electrodes (in a crossbar layout), followed by blanket deposition of the switching oxide (hafnium oxide, tantalum oxide, or zirconium oxide), followed by photolithography and lift-off patterning of a top electrode layer. In summary, this procedure results in arrays of memristive crossbar devices. A detailed summary of the procedure is provided in the sections below, and a visual overview of the process is shown in Figure 2.

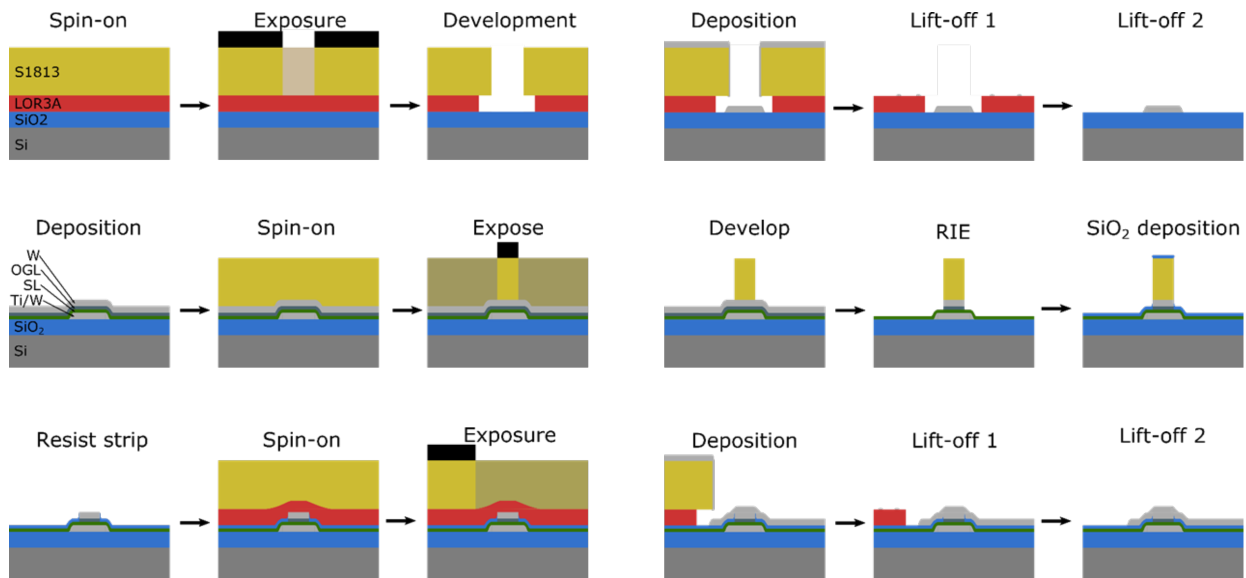

Figure 2: Overview of the fabrication approach for memristor crossbar arrays.

4.3.1 Mask design and usage

The mask is designed as a split mask, meaning we have two layer on one physical mask. This reduces the amount of masks needed and by this reduces the cost of the process. An additional mask was required in later stages of the development resulting in 3 masks for only 4 layers. To access the second layer on a mask one has to rotate the mask from its normal position on the holder of 180°.

The three different masks used in this process are:

- RRAM Main
  - Bottom electrode (not rotated)
  - Top interconnect (180° rotated)
- RRAM Via
  - RRAM device stack etch (not rotated)
- BE contact
  - Bottom contact pad opening (not rotated)

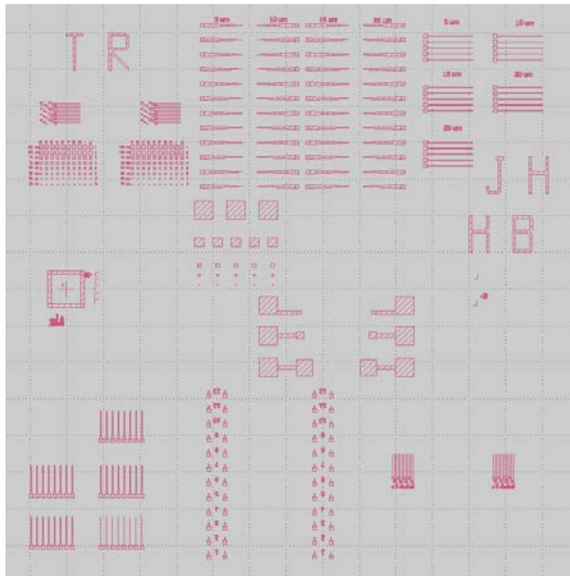

Figure 3: Layout of the mask ‘RRAM Main’ for the bottom electrode and the top interconnect.

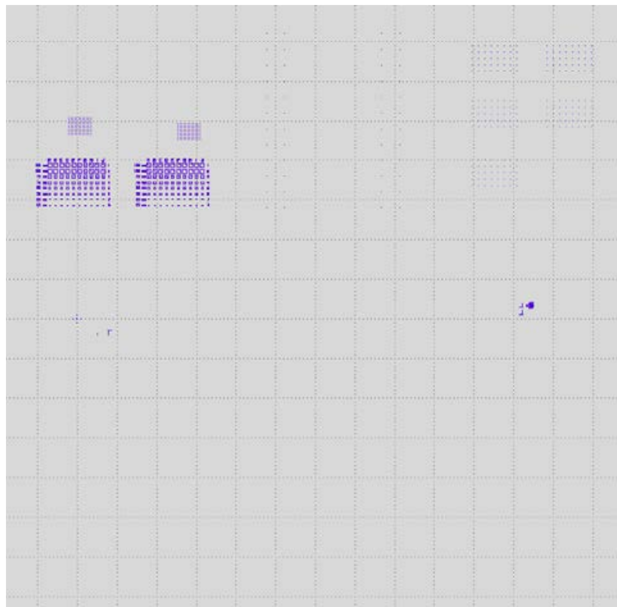

Figure 4: Layout of the mask ‘RRAM Via’ for the bottom electrode and the top interconnect.

Approved for Public Release; Distribution Unlimited.

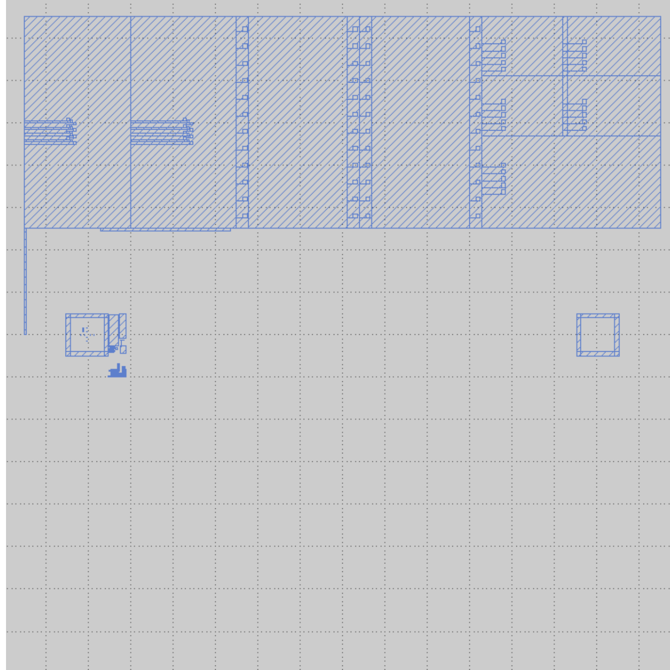

Figure 5: Layout of the mask 'BE contact' for the opening of the bottom contact.

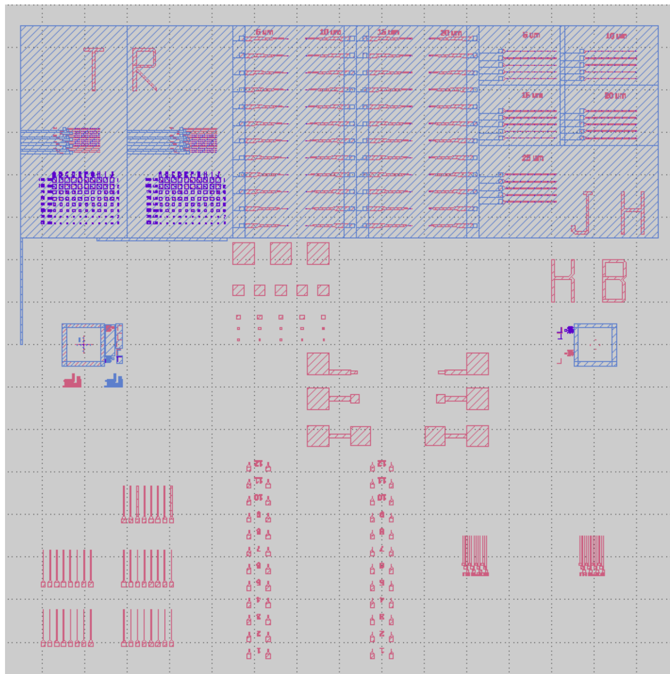

Figure 6: Combined Layout of the masks 'RRAM Main', 'RRAM Via' and 'BE contact'.

Bottom electrode and interconnect
Our design utilizes tungsten as the bottom interconnect which is typically inert enough to serve as the bottom electrode (BE) of the RRAM (memristor) device. To create the BE pattern a lift-off process was chosen for simplicity purposes. Three different steps are necessary and discussed here: lithography, deposition and the resist lift-off.

4.3.2 Lithography

For the lift-off process a double structure consisting of LOR-3A and S1813 photoresist was used. The S1813 is photosensitive and creates the pattern via exposure while the LOR-3A is not photosensitive but soluble in MIF300. This creates the undercut necessary to avoid metal wings on the edges of the BE (Figure 7). The creation of metal wings is a serious concern because it would cause the BE to shorten with the later created top electrode (TE). Figure 8 shows two Atomic Force Microscope (AFM) images identifying the problem of creating metal wings due to a lack of undercut of the LOR3A under the photoresist. The undercut needs to extent around 500nm to prevent sputtering of the LOR3A wall due to non-directional movement of sputtered atoms. If the undercut extends too far a collapse of the photoresist (here S1813) might occur causing the same problematic with side wings. A far extension might be caused by an adhesion problem of the LOR3A to the SiO2 surface and a halo will be visible around the pattern.

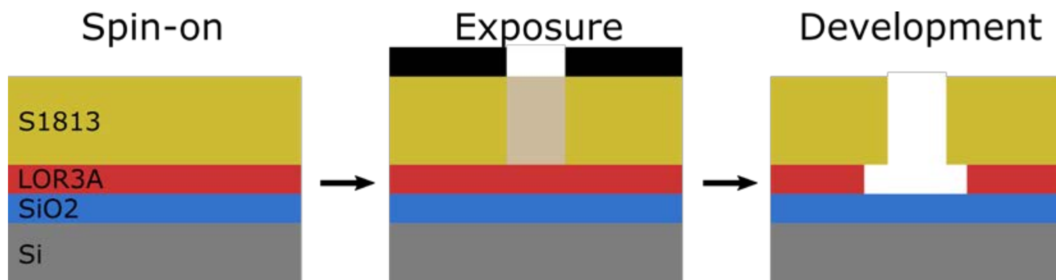

Figure 7: Illustration showing the spin-on of the Lift-off double structure consisting of LOR3A and S1813 photoresist and the subsequent exposure and development of BE

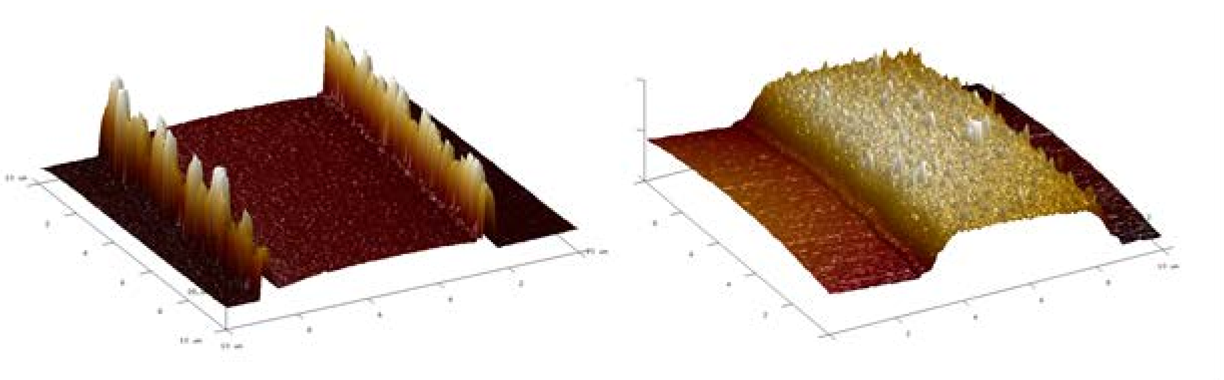

Figure 8: AFM images showing the unintentional formation of metal side wings (left) and a successful fabricated BE (right).

Following steps and parameter should be followed precisely to avoid the above discussed problems:

Use the mask "RRAM Main" without rotation
Dehydration bake on hotplate
150C for 5min

1. P-20 (HMDS)
   Distribute on wafer
   Wait 10s
   Spin at 3000rpm (KBLOR3A recipe)

2. LOR3A (500nm)
   Distribute on wafer
   Spin at 3000rpm for 30s (KBLOR3A recipe)
   Bake for 3min at 150C

3. S1813 (1.2um)
   Distribute on wafer
   Spin at 4000rpm for 60s (KBS1813 recipe)
   Bake for 90s at 110C

4. Expose
   minimum dose: 65mJ/cm2
   2.2s recommended on OAI aligner

5. Developing and creation of the undercut
   Use MIF300 for 30s
   move the MIF300 by carefully moving the glassware
   Bake for 60s at 110C
   Use MIF300 for 60s

4.3.3 Deposition

Deposition of the BE occurs in two steps, first a wetting layer needs to be deposited on the SiO_2 surface of the silicon wafer. This enables a good adhesion of the inert metal which serves as the BE of our RRAM devices. In most cases titanium will be used as the wetting layer due to its oxygen active behavior forming strong bonds with the SiO_2 surface.
The following metals might also be used:

- Chromium
- Nickel
- Aluminum
- Hafnium
- Tantalum

Approved for Public Release; Distribution Unlimited.

The BE material should be inert to gain a stoichiometric switching layer (SL) at the BE interface. The following sample of inert metals are suited to fulfill this functionality:

- Tungsten
- Platinum
- Ruthenium
- Iridium
- Titanium nitride
- Tantalum nitride
- Osmium
- Rhodium
- Palladium
- Cobalt

The choice of the exact material depends strongly on the deposition capabilities, the desired roughness and in particular the mechanical and electronic interaction of the BE metal with the SL oxide. For HfO_2 a tungsten BE has been shown to be suitable and it will be used as an example material.
Following parameters are used for the deposition of Ti and W in the PVD75 tool from Kurt Lesker using the nanofabrication facility at SUNY Polytechnic Institute:

- Titanium wetting layer
    - Titanium target in Source 1
    - Process time: 220s
    - Power: 100W DC
    - Pressure: 3mTorr
    - Gas flow: 100% Ar flow
    - Cleaning time: 300s
- Tungsten electrode
    - Tungsten target in Source 2
    - Process time: 750s
    - Power: 100W DC
    - Pressure: 3mTorr
    - Gas flow: 100% Ar flow
    - Cleaning time: 180s

4.3.4 Resist lift -off

A complete removal of all organic lithography components is necessary for further processing. In addition, the lift-off process should limit the re-deposition of the lifted off metal stack to prevent potential shortening and malfunction of the individual RRAM devices (Figure 9)
The proposed process removes the dual layer of S1813 and LOR3A in two steps.

1. Acetone bath of the wafer in a sonicating bath until the metal has been lifted of by dissolving S1813.
2. Flushing the wafer with 1165 resist remove out of bottle to progressively flushing redeposited metal particles.
3. Leave the wafer in a bath of 1165 for at least 3h
4. Clean the wafer with IPA

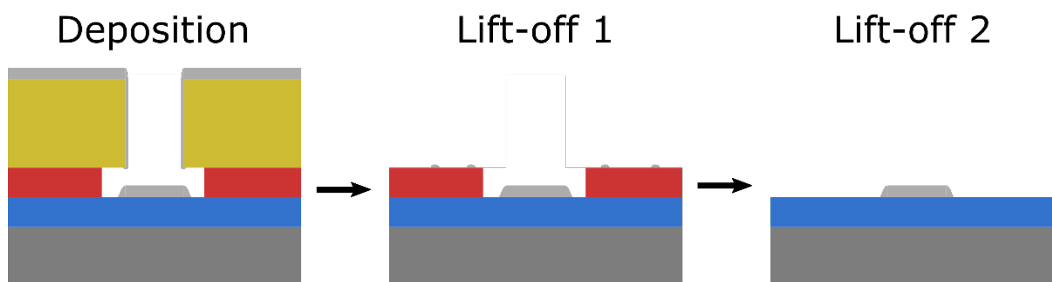

Figure 9: Illustration showing the deposition of the BE on top of a lift-off resist pattern and the subsequent removal via a dual lift-off process.

4.3.5 RRAM device stack and top electrode

Deposition

The deposition of the RRAM device stack on top of the BE requires three separate depositions. The first deposition is the switching layer (SL) typically being a transition metal oxide followed by an oxygen getter layer (OGL) and the top electrode. This process is developed to be only compatible only with a tungsten top electrode due to the necessity for a RIE step. The aimed thickness for the tungsten top electrode is 50 nm fabricated in the PVD75 sputter tool from Kurt Lesker. However, different deposition techniques could change this and might require an adjustment of the deposition and/or etch time to adjust for different material characteristics. In addition, the OGL layer should be capable of being etched by a combination of SF_6 and O_2. Typical SL compatible with this process are:

- HfO_2
- Ta_2O_5
- TiO_2
- ZrO_2
- La_2O_3

Typical OGL compatible with this process are:

- Ti
- Zr
- Ta
- La

Following parameters are used as an example deposition of HfO_2+Ti+W device in the PVD75 tool from Kurt Lesker:

1. HfO_2 switching layer
    - Hafnium target in Source 3
    - Process time: 591s
    - Power: 125W RF
    - Pressure: 3mTorr
    - Gas flow: 70% Ar flow + 30% O2 flow
    - Cleaning time: 300s
2. Titanium oxygen getter layer
    - Titanium target in Source 1
    - Process time: 591s
    - Power: 100W DC
    - Pressure: 3mTorr
    - Gas flow: 100% Ar flow
    - Cleaning time: 300s
3. Tungsten electrode
    - Tungsten target in Source 2
    - Process time: 750s
    - Power: 100W DC
    - Pressure: 3mTorr
    - Gas flow: 100% Ar flow
    - Cleaning time: 180s

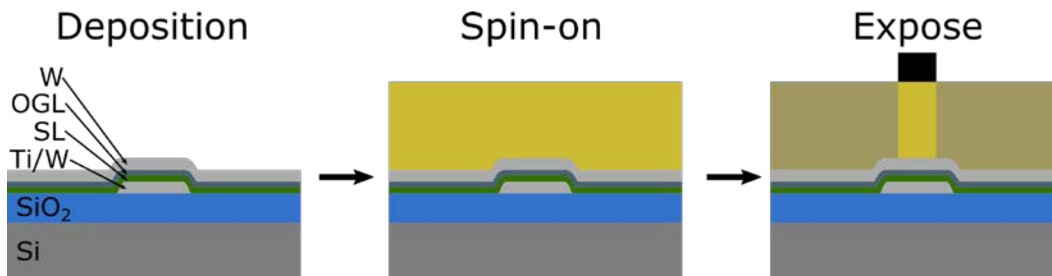

Figure 10: Illustration showing the uniform deposition of the switching layer (SL), oxygen getter layer (OGL) and inert top electrode on top of the patterned BE. S1813 photoresist is subsequently spun-on and exposed to device the RRAM stack.

Lithography
Particular attention has to be given to the RRAM device stack lithography process. To gain a vertical cut-off of the to-be etched tungsten TE the resist tapering angle needs to be as close to 0° as possible. A too large tapering angle would cause a re-deposition of the TE and OGL. This subsequently results in the malfunction of the RRAM devices.
Furthermore, the alignment of the mask has to be accurate within about 750 nm, otherwise the RRAM device stack moves to far to the edges of the BE where a good uniformity is not guaranteed. This would most certainly result in a change in the device performance. Typically characterized by a reduced forming voltage and most likely a reduced yield.

The following steps should be followed as closely as possible:

1. Use the mask "RRAM Via" without rotation
2. Dehydration bake on hotplate
   150C for 5min
3. P-20 (HMDS)
   Distribute on wafer
   Wait 10s
   Spin at 4000rpm for 40s (KBS1813 recipe)
4. S1813 (1.2um)
   Distribute on wafer
   Spin at 4000rpm for 60s (KBS1813 recipe)
   Bake for 90s at 110C
5. Rehydrate the photoresist
   put a wet towel on the 110C hotplate
   put a small glass container on the wet towel
   place the wafer for 120s on the glass container
6. Expose
   minimum dose: 65mJ/cm2
   1.9s recommended on OAI aligner
7. Developing
   Use MIF300 for 12s
   constantly move the MIF300 by carefully moving the glassware
   check for successful development under the microscope

Reactive-ion etch
The RRAM device stack size will be defined by a reactive-ion etch (RIE) as shown in Figure 11. The major challenge of this step is to avoid a change in RRAM device performance due to the RIE. This change might arise as a result from a change in the surface morphology of the sidewalls or due to a re-deposition of tungsten and/or the OGL on a damaged SL.
The recipe name in the Versalock PlasmaTherm tool at SUNY Polytechnic Institute is: PM3_Cady_RRAM_W+Ti.

In detail the etch process follows following procedure:

1. Initialization (PM3_Init)
    - Process time: 30s
    - Pressure: 1mTorr
    - No gas flow
    - No Power
2. Gas stabilization (PM3_Sta_SF6+O2)
    - Process time: 30s
    - Pressure: 15mTorr

- Gas flow: 40sccm SF6 + 10sccm O2
    - No Power
3. Plasma ignition (PM3_Ign_SF6+O2)
    - Process time: 5s
    - Pressure: 15mTorr
    - Gas flow: 40sccm SF6 + 10sccm O2
    - ICP Power: 500W
    - RIE Power: 50W
4. Etch (PM3_Etch_SF6+O2)
    - Process time: 50s
    - Pressure: 15mTorr
    - Gas flow: 40sccm SF6 + 10sccm O2
    - ICP Power: 500W
    - RIE Power: 100W
5. Initialization (PM3_Init)
    - Process time: 30s
    - Pressure: 1mTorr
    - No gas flow
    - No Power
6. Gas stabilization (PM3_Sta_Ar+SF6+O2)
    - Process time: 30s
    - Pressure: 5mTorr
    - Gas flow: 5sccm SF6 + 40sccm Ar + 5sccm O2
    - No Power
7. Plasma ignition (PM3_Ign_ Ar+SF6+O2)
    - Process time: 5s
    - Pressure: 5mTorr
    - Gas flow: 5sccm SF6 + 40sccm Ar + 5sccm O2
    - ICP Power: 500W
    - RIE Power: 50W
8. Etch (PM3_Etch_ Ar+SF6+O2)
    - Process time: 20s

- Pressure: 5mTorr
- Gas flow: 5sccm SF6 + 40sccm Ar + 5sccm O2
- ICP Power: 500W
- RIE Power: 100W

9. Initialization (PM3_Init)
    - Process time: 30s
    - Pressure: 1mTorr
    - No gas flow
    - No Power

The etch recipe has following main parameter:

- Temperature1TemperatureSetpt: 30C
- Temperature1TemperatureSetpt: 20C
- HeliumCoolerPressureSetpoint: 3000mTorr

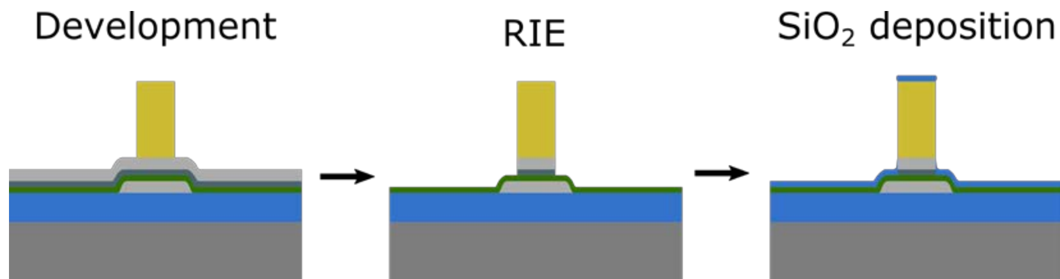

Figure 11: Illustration showing the development of the exposed photoresist layer and the following reactive-ion etch (RIE) and SiO_2 deposition.

An important aspect of this procedure is the vertical etch of the tungsten followed by switching over to a highly anisotropic ion mill process consisting mainly of an argon composing plasma cleans out the OGL and at least parts of the metallic acting sub-stoichiometric SL.
This last ion mil step requires a more aggressive clean of the chamber after removing the sample to avoid cross contamination and a degradation of the plasma chamber performance. The carrier wafer needs to be back loaded to have a sufficient cooling of the chamber via the build in helium cooler.

The cleaning recipe name in the Versalock PlasmaTherm tool at SUNY Polytechnic Institute is: PM3_Chamber_Clean. It comprises of following steps:

1. Pump down (PM3_Chamber_Clean_Pmpdwn_Ca)
    - Process time: 30s
    - Pressure: 1mTorr
    - No gas flow
    - No Power
2. Stabilization (PM3_Chamber_Clean_Sta_Sput)
    - Process time: 30s

- Pressure: 50mTorr
- Gas flow: 50sccm SF6 + 10sccm Ar + 20sccm O2
- No Power

3. Plasma ignition (PM3_Chamber_Clean_Ign_Sput)
    - Process time: 5s
    - Pressure: 50mTorr
    - Gas flow: 50sccm SF6 + 10sccm Ar + 20sccm O2
    - ICP power: 1000W
    - RIE power: 50W
4. Sputter Clean (PM3_Chamber_Clean_sput)
    - Process time: 2400s
    - Pressure: 50mTorr
    - Gas flow: 50sccm SF6 + 10sccm Ar + 20sccm O2
    - ICP power: 1000W
    - RIE power: 0W
5. Stabilization (PM3_Chamber_Clean_Sta_O2)
    - Process time: 30s
    - Pressure: 50mTorr
    - Gas flow: 100sccm O2
    - No Power
6. Plasma ignition (PM3_Chamber_Clean_Ign_O2)
    - Process time: 5s
    - Pressure: 50mTorr
    - Gas flow: 100sccm O2
    - ICP power: 1000W
    - RIE power: 50W
7. Clean (PM3_Chamber_Clean_O2)
    - Process time: 3600s
    - Pressure: 50mTorr
    - Gas flow: 100sccm O2
    - ICP power: 1000W
    - RIE power: 0W
8. Pump down (PM3_Chamber_Clean_Pmpdwn_Ca)
    - Process time: 30s
    - Pressure: 1mTorr
    - No gas flow
    - No Power

The cleaning recipe has following constant parameter:

- Temperature1TemperatureSetpt: 30C
- Temperature1TemperatureSetpt: 20C
- HeliumCoolerPressureSetpoint: 3000mTorr

Approved for Public Release; Distribution Unlimited.

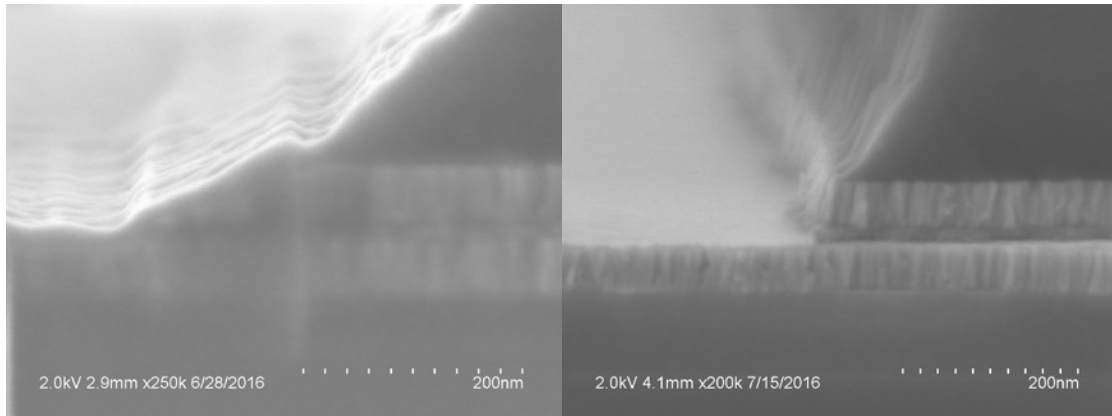

Figure 12: SEM images showing two different RIE approaches. The left image shows the use of a plasma based on CF4+O2 creating a large tapering angle of tungsten and re-depositing parts of it on the SL. The right image shows an almost vertical etch with a plasma based on SF6+O2. In this approach the SF6 based plasma etches tungsten faster than the photoresist not creating the contact area for sputtered re-deposition. A second plasma etch based on Ar+SF6+O2 removes the Ti+HfO2 in an ion milling approach.

Insulator deposition

It is necessary to deposit an insulator in the field and in particular around the RRAM device stack to avoid shorting of the BE and TE. Figure 11 illustrates that the previous RRAM device stack resist from the RIE is used as a lift-off photoresist layer. Experimentally it was concluded that a 15nm co-sputtered SiO_2 layer is sufficient to get a leakage current below the detection limit of our system (around 10pA).

Following parameters are used for the deposition of SiO_2 in the PVD75 tool from Kurt Lesker:

- Silicon target in Source 1
- Process time: 1400s
- Power: 150W RF
- Pressure: 3mTorr
- Gas flow: 55% Ar flow - 45% O2 flow

Resist lift-off/strip

The lift-off of the SiO_2 insulator and strip of the remaining photoresist requires more effort as seen for the BE and TE photoresist stack. The photoresist got exposed a high implantation dose of of S-F-O compounds as well as Ar during the RIE process. This implantation changes the structure of the resist, results in additional crosslinking and the creation of an extremely hard resist surface. In addition, the SiO_2 creates a thin layer around the resist further protecting it against a stripper.

The following three steps ensure the complete removal of all photoresist residuals from the wafer in a 1165 remover bath:

1. 1h sonicating with a medium to high sonicating power (4-7)
2. 2h bath at 70C on the hot-plate
3. Overnight bath at room temperature

Top interconnect

Lithography

A very similar Lift-off process is used for the top interconnect (TI) to pattern the second contact to the RRAM device (Figure 13). This step is less prone to a malfunction because it is the last structure and metal wings don't impact the functionality of the device. As for the BE a double structure consisting of LOR-3A and S1813 photoresist is used. For further information, please follow the description in section "Bottom electrode and interconnect – Lithography".
The following steps and parameter should be followed:

1. Use mask "RRAM Main" without a 180° rotation

2. Dehydration bake on hotplate
   150C for 5min

3. P-20 (HMDS)
   Distribute on wafer
   Wait 10s
   Spin at 3000rpm for 30s (KBLOR3A recipe)

4. LOR3A (500nm)
   Distribute on wafer
   Spin at 3000rpm for 30s (KBLOR3A recipe)
   Bake for 3min at 150C

5. S1813 (1.2um)
   Distribute on wafer
   Spin at 4000rpm for 60s (KBS1813 recipe)
   Bake for 90s at 110C

6. Expose
   minimum dose: 65mJ/cm2
   2.2s recommended on OAI aligner

7. Developing and creation of the undercut
   Use MIF300 for 40s
   Move the MIF300 by carefully moving the glassware

Approved for Public Release; Distribution Unlimited.

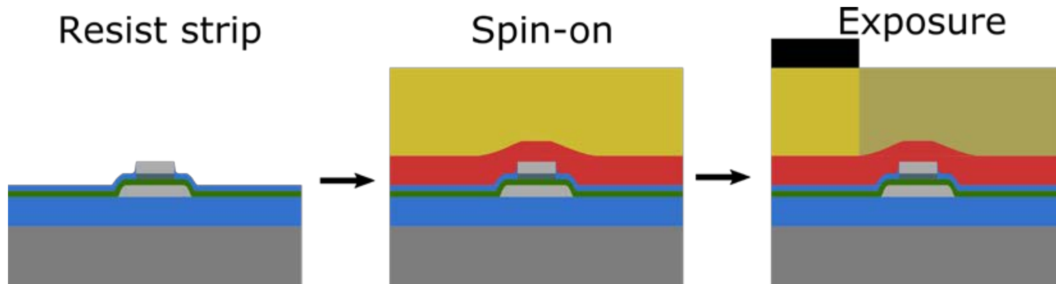

Figure 13: Illustration showing the photoresist removal after RIE and the SiO2 deposition, the spin on of the double layer consisting of MIF300 and S1813 photoresist and the subsequent exposure to define the top interconnect pattern.

Deposition

Deposition of the TI occurs in two steps; first a wetting layer needs to be deposited on the SiO_2 surface of the silicon wafer as illustrated in Figure 14. This enables a good adhesion of the inert metal which serves as the BE of our RRAM devices. In most cases titanium will be used as the wetting layer due to its oxygen active behavior forming strong bonds with the SiO_2 surface. The preferred metal for the wetting layer and TI is Ti and W, respectively, but other metals might be used as described in the section "Bottom electrode and interconnect – Deposition (page 5). The TI should be stable in atmosphere and resistant against oxidation to allow a good contact with W probe tips.

The following parameters are used for the deposition of Ti and W in the PVD75 tool from Kurt Lesker:

- Titanium wetting layer
  - Titanium target in Source 1
  - Process time: 220s
  - Power: 100W DC
  - Pressure: 3mTorr
  - Gas flow: 100% Ar flow
  - Cleaning time: 300s
- Tungsten interconnect
  - Tungsten target in Source 2
  - Process time: 750s
  - Power: 100W DC
  - Pressure: 3mTorr
  - Gas flow: 100% Ar flow
  - Cleaning time: 180s

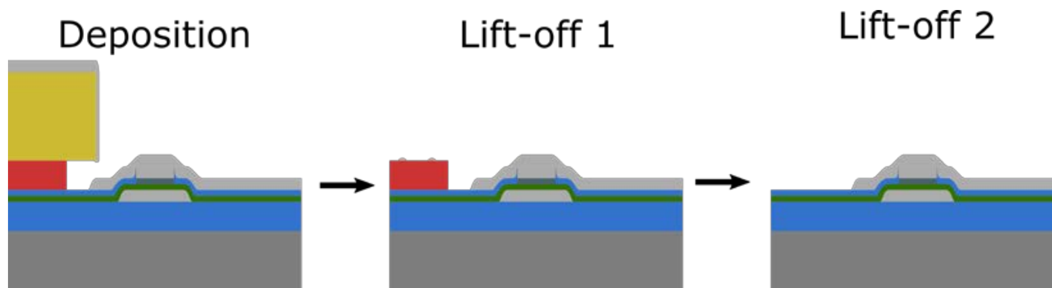

Figure 14: Illustration showing the deposition of the top contact onto the patterned photoresist structure. A dual lift-off of the S1813 photoresist and the LOR3A finishes the top electrode.

Resist lift-off
A complete removal of all organic lithography components is necessary for further processing. In addition, the lift-off process should limit the re-deposition of the lifted of metal stack to prevent potential shortening and malfunction of the individual RRAM devices (Figure 14).
The proposed process removes the dual layer of S1813 and LOR3A in two steps.

1. Acetone bath of the wafer in a sonicating bath until the metal has been lifted of by dissolving S1813.
2. Flushing the wafer with 1165 resist remove out of bottle to progressively flushing redeposited metal particles.
3. Leave the wafer in a bath of 1165 for at least 3h
4. Clean the wafer with IPA

4.3.6 Bottom electrode contact pad opening

Lithography
The final step opens the BE which is buried in a layer of HfO_2 and SiO_2. For this effort a simple photoresist process can be used. Due to the size of the pads ($100x100\mu m^2$) the alignment is not as crucial as for the past three lithography steps and a time saving rough alignment is sufficient. Because of the use of a wet etch process the adhesion of the photoresist to the substrate plays an important role and attention should be paid to the second and third step.

1. Use the mask “BE contact” without rotation

2. Dehydration bake on hotplate
   150C for 5min

3. P-20 (HMDS)
   Distribute on wafer
   Wait 10s
   Spin at 4000rpm for 40s (KBS1813 recipe)

4. S1813 (1.2um)
   Distribute on wafer
   Spin at 4000rpm for 60s (KBS1813 recipe)
   Bake for 90s at 110C

5. Expose
   minimum dose: 65mJ/cm2
   1.9s recommended on OAI aligner

6. Developing
   Use MIF300 for 30s
   Move the MIF300 by carefully moving the glassware
   check for successful development under the microscope

Wet Etch

The wet etch utilizes a prepared etch solution from Transgene based on HF to remove the 15nm of SiO_2 and the residual HfO_2 layer. The etch solution is 'Improved Buffered HF' which is a mixture of H_2O, HF and NH_4F and designed to give etch 70nm/min of thermal oxide. In practice the rate will far exceed that value for co-sputtered SiO_2 but the value for HfO_2 is currently unknown. An etch time of 30s has been found to remove all oxide material and create a good contact to the bottom electrode.

Resist strip

To remove all residual resist in a timely fashion an approach based on the developer MIF300 is recommended.
Following steps should be followed to completely remove all photoresist from the wafer and in particular from the W TI.

- 10s flood exposure of both sides of the wafer
- 3min bath in in MIF300
- Clean with DI water

4.4 Device Characterization

For each wafer full of devices that was fabricated, initial electrical testing was performed at both SUNY Polytechnic Institute and AFRL/RI. Current-voltage (I-V) sweep measurements were made to determine the forming voltage, set and reset voltages. An example of such data, obtained from hafnium oxide memristors are shown in Figure 15.

Approved for Public Release; Distribution Unlimited.

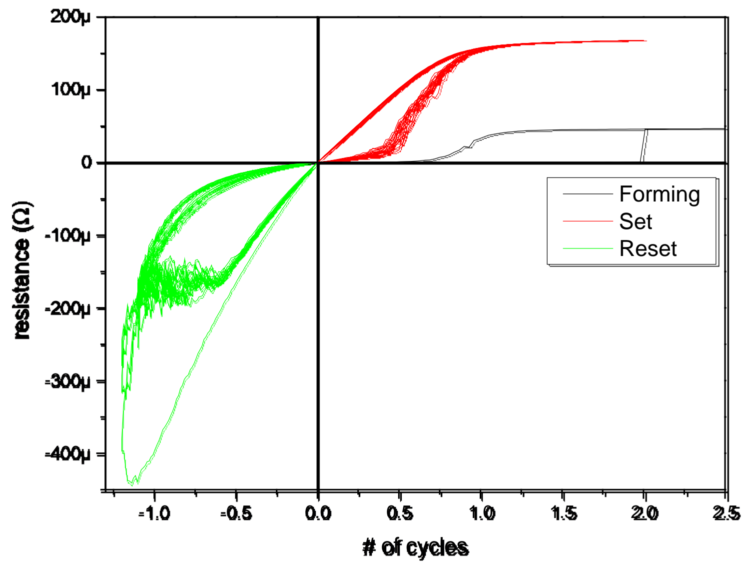

Figure 15: Current voltage plot for hafnium oxide electroforming (black line), and multiple set and reset cycles (red and green plots, respectively).

Devices were cycled for ~10-50 times to ensure reliability, as well as to characterize the average on and off state resistance values. Examples of these data are shown in Figure 16.

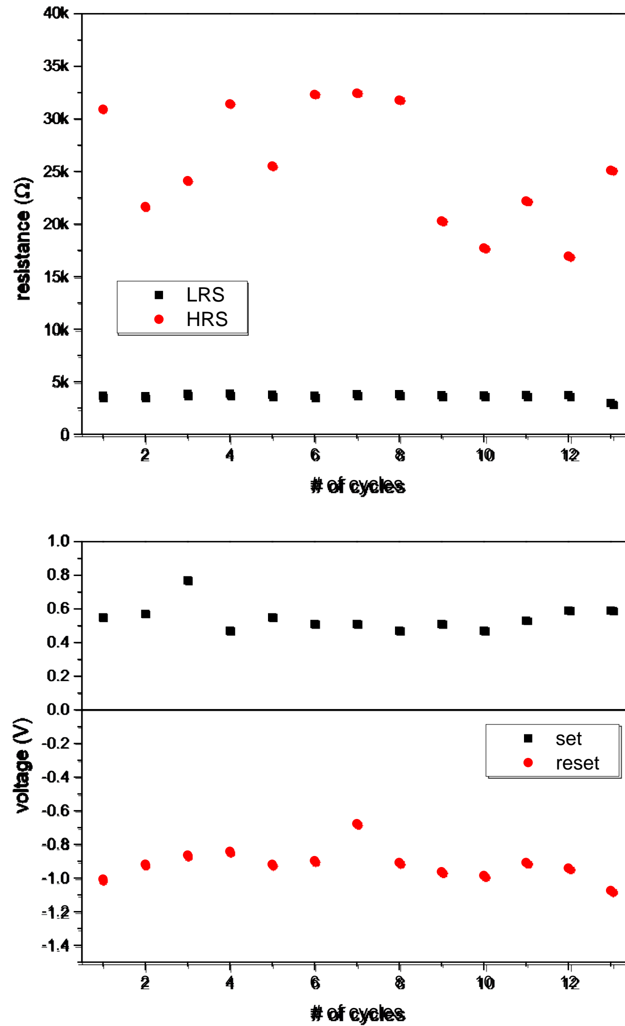

Figure 16: Resistance values for "on" (LRS) and "off" (HRS) states of a hafnium oxide devices (top graph) and corresponding set and reset voltages for the switching cycles (bottom graph).

4.5 Final Results

As a result of this work, multiple 300mm wafers containing memristor crossbar arrays were fabricated and tested by AFRL/RI and their collaborators. These included multiple wafers containing hafnium oxide devices, one wafer containing zirconium oxide devices, and multiple "die" (sub-sections of wafers) containing tantalum oxide devices. The results were used to inform future memristor based architectures for neuromorphic processors as well as novel cyber security designs

4.7 Presentations, Publications and Patent Applications Resulting from this Project

Peer-Reviewed Journal Articles

1. K. Beckmann*, J. Holt*, W. Olin-Ammentorp*, J. Van Nostrand, N.C. Cady. Impact of etch process on hafnium dioxide based nanoscale RRAM devices. (2016) *ECS Transactions.* 75(13): 93-99.
2. K. Beckmann*, J. Holt*, H. Manem*, J. Van Nostrand, N.C. Cady. Nanoscale hafnium oxide RRAM devices exhibit pulse dependent behavior and multi-level resistance capability. (2016) *MRS Advances.* 1(49): 3355-3360. *DOI:* http://dx.doi.org/10.1557/adv.2016.377

5. Conclusions

In conclusion, this in-house research and development effort developed a stable process flow for fabricating memristive crossbar arrays utilizing various switching oxides (hafnium oxide, tantalum oxide, and zirconium oxide). This process flow can be leveraged for fabrication of other types of memristors, and could pave the way for future device as well as architecture development efforts.

6. List of Acronyms

RRAM: Resistive random access memory (aka: memristor)
ReRAM: Resistive random access memory (aka: memristor)
RMD: Resistive memory device (aka: memristor)
TE: Top electrode
BE: Bottom electrode
HRS: High resistance state
LRS: Low resistance state
XPS: X-ray photoelectron spectroscopy
XRD: X-ray diffraction
TEM: Transmission electron microscopy
SEM: Scanning electron microscopy
AFM: Atomic force microscopy

Approved for Public Release; Distribution Unlimited.