REPORT DOCUMENTATION PAGE			Form Approved OMB NO. 0704-0188

The public reporting burden for this collection of information is estimated to average 1 hour per response, including the time for reviewing instructions, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the collection of information. Send comments regarding this burden estimate or any other aspect of this collection of information, including suggesstions for reducing this burden, to Washington Headquarters Services, Directorate for Information Operations and Reports, 1215 Jefferson Davis Highway, Suite 1204, Arlington VA, 22202-4302. Respondents should be aware that notwithstanding any other provision of law, no person shall be subject to any oenalty for failing to comply with a collection of information if it does not display a currently valid OMB control number.
PLEASE DO NOT RETURN YOUR FORM TO THE ABOVE ADDRESS.

1. REPORT DATE (DD-MM-YYYY)	2. REPORT TYPE	3. DATES COVERED (From - To)
07-09-2015	MS Thesis	-

4. TITLE AND SUBTITLE
Fabrication of graphene-on-GaN vertical transistors

5a. CONTRACT NUMBER
W911NF-14-2-0071

5b. GRANT NUMBER

5c. PROGRAM ELEMENT NUMBER
611102

6. AUTHORS
Ahmad Zubair

5d. PROJECT NUMBER

5e. TASK NUMBER

5f. WORK UNIT NUMBER

7. PERFORMING ORGANIZATION NAMES AND ADDRESSES
Massachusetts Institute of Technology (MIT
77 Massachusetts Ave.
NE18-901
Cambridge, MA 02139 -4307

8. PERFORMING ORGANIZATION REPORT NUMBER

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS (ES)
U.S. Army Research Office
P.O. Box 12211
Research Triangle Park, NC 27709-2211

10. SPONSOR/MONITOR'S ACRONYM(S)
ARO

11. SPONSOR/MONITOR'S REPORT NUMBER(S)
65437-EL.1

12. DISTRIBUTION AVAILIBILITY STATEMENT
Approved for public release; distribution is unlimited.

13. SUPPLEMENTARY NOTES
The views, opinions and/or findings contained in this report are those of the author(s) and should not contrued as an official Department of the Army position, policy or decision, unless so designated by other documentation.

14. ABSTRACT
The recently discovered two-dimensional materials opened up a new era of physics and applications in the field of electronics. Various exciting and promising applications of this materials have been demonstrated already in the conventional electronic structures which is based on the principle of in plane transport. The goal of this thesis to explore the physics and application of the out of plane transport of two dimensional materials specifically graphene to study the underlying physics and future technological applications.

15. SUBJECT TERMS
Graphene, hot electron transistor, GaN

16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT	15. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON
a. REPORT	b. ABSTRACT	c. THIS PAGE			Tomas Palacios
UU	UU	UU	UU		19b. TELEPHONE NUMBER 617-324-2395

Standard Form 298 (Rev 8/98)
Prescribed by ANSI Std. Z39.18

Report Title

Fabrication of graphene-on-GaN vertical transistors

ABSTRACT

The recently discovered two-dimensional materials opened up a new era of physics and applications in the field of electronics. Various exciting and promising applications of this materials have been demonstrated already in the conventional electronic structures which is based on the principle of in plane transport. The goal of this thesis to explore the physics and application of the out of plane transport of two dimensional materials specifically graphene to study the underlying physics and future technological applications.

Fabrication of Graphene-on-GaN Vertical Transistors

by

Ahmad Zubair

B.Sc., Bangladesh University of Engineering and Technology (2011)

Submitted to the Department of Electrical Engineering and Computer Science

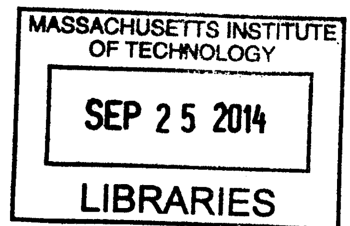
in partial fulfillment of the requirements for the degree of

Master of Science

at the

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

September 2014



© Massachusetts Institute of Technology 2014. All rights reserved.

Signature redacted

Author ....

Department of Electrical Engineering and Computer Science

August 29, 2014

Signature redacted

Certified by ....

Tomás Palacios

Associate Professor, Electrical Engineering and Computer Science

Thesis Supervisor

Certified by .... Signature redacted

Mildred S. Dresselhaus

Institute Professor,Emerita; Professor of Physics and Electrical Engineering and Computer Science

Thesis Supervisor

Accepted by .... Signature redacted ......

Leslie A. Kolodziejski

Chairman, Department Committee on Graduate Students

Fabrication of Graphene-on-GaN Vertical Transistors

by

Ahmad Zubair

Submitted to the Department of Electrical Engineering and Computer Science
on August 29, 2014, in partial fulfillment of the
requirements for the degree of
Master of Science

Abstract

The excellent transport properties of graphene make it an excellent option for very high frequency electronics. However, the poor output resistance and difficult lithography of lateral transistors significantly limit its performance. In this thesis, we propose a new kind of vertical graphene base transistor to take advantage of both wide bandgap GaN semicodnductors and zero bandgap graphene for high frequency transistors. This majority-carrier device has a metal collector, a graphene base and an AlGaN/GaN emitter. The first device prototype exhibits very promising current density($\sim$mA/cm^2) and current gain ($\alpha \sim 50$ %). Simulations further support that with proper optimization of the materials and device structure, the proposed transistor can be a promising candidate for future high frequency applications.

Thesis Supervisor: Tomás Palacios
Title: Associate Professor, Electrical Engineering and Computer Science

Thesis Supervisor: Mildred S. Dresselhaus
Title: Institute Professor,Emerita; Professor of Physics and Electrical Engineering and Computer Science

Acknowledgments

First of all, I would like to thank my supervisors Professor **Tomás Palacios** and Professor **Mildred Dresselhaus** for all the guidance and help over the course of this thesis. I'm grateful for their patience,support and enthusiasm over the last two years.Without their inspiration and support it would not have been possible. I'm thankful to all the members of Palacios and Dresselhaus group for their help. I learned every single things related to fabrication and experiment from them. I found them always there with help and support. Especially **Omair Saadat** who helped from starting from mask design, fabrication, sputtering,measurement and problem solving. I'm grateful to **Yi Song** for providing me with the CVD graphene required for this thesis and also to teach me the transfer process. I would like to express my earnest gratitude to Professor **Gianluca Fiori** and Professor **Giuseppe Iannaccone** , Universitá di Pisa, Italy for helping with device simulations and hosting me in their lab to learn the simulation. Most importantly, my deepest thankfulness to my parents and siblings for all their love and support. Finally, I would like to thank **Saima** who is always there with love, support and inspiration.

Contents

1 Introduction **15**

1.1 Hot Electron Transistors 18

1.2 III-Nitride Hot-Electron Transistor 19

1.3 Vertical Graphene Transistors 21

1.3.1 Graphene Barristor 22

1.3.2 Graphene Base Transistor (GBT) 24

1.3.3 Graphene-base Hot Electron Transistor 24

2 Device design **27**

2.0.4 Operating principle of Graphene-Base Transistor 27

2.0.5 Material selection 29

2.0.6 Physical Structure design 33

3 Fabrication **37**

3.1 Ohmic Contact 37

3.2 Mesa Etching 38

3.3 Graphene Growth and Transfer 38

3.4 Base Contact and device isolation 38

3.5 BCI and Collector formation 39

4 Device Characterisitics **41**

4.1 Heterojunction current-voltage measurement 41

4.1.1 Emitter-Base heterojunction 42

4.1.2 Base-collector heterojunction 47
4.2 Common-emitter Characteristics 49
4.3 NanoTCAD Vides simulation 53

5 Conclusion and Future Works **57**
5.1 Design with a thinner AlGaN layer 58
5.2 Design with InAlN layer 58
5.3 Design with hBN 59
5.4 GaN Collector 59

A Tables **65**

List of Figures

1-1 a) Schematic diagram of the atomic structure of monolayer honeycomb graphene . The archair and zig-zag indicates the nature of edge-states of planar semi-infinite sheet of Carbon atoms. [1] b) Three inplane $\sigma(s, p_x, p_y)$ and out of plane $\pi(p_z)$ orbitals of sp^2bonded hexagonal network of Carbon atoms. 16

1-2 (a) Scanning Electron Microscope (SEM) image of a state-of the art Heterojunction bipolar transistor (HBT) [2],(b)small signal hybrid pi equivalent circuit of a HBT 16

1-3 Energy band diagrams of different versions of Metal base transistors. Left: (a) MOMOM; (b) MOMS; (c) SMS. Each metal (M) and semiconductor (S) can be biased independently. [3] 19

1-4 (a)Emitter-collector transfer ratio for different base width and (b) the energy band diagram of first monolithic metal base transistor[4] . . . 20

1-5 The device structure of proposed III-Nitride Induced base transistor[5] 20

1-6 (a) Device Structure and (b) band diagram of fabricated III-Nitride HET [6] 21

1-7 Graphene barristor. (A) A schematic diagram to show the concept of a GB. (B) Current versus bias voltage characteristic of a GB at a fixed gate voltage Vgate = 0 V, showing a Schottky diode characteristic. The inset shows a TEM image of graphene/Si [7] 22

1-8 a) Switching and b) Output characteristics of graphene barristor , c) Inverter operation based on graphene barristor [7] 23

1-9 Schematic cross sections of (a) GFET and (b) GBT and the schematic band diagrams of (c) an unbiased and (d) biased GBT. [8] 23
1-10 a) Output characteristics of simulated GBT b) Cut-off frequency of the simulated GBT. [8] 24
1-11 (a) and (c)Structure and (b) and (d)output characteristics of graphene-base HETs as demonstrated in[9, 10] 25

2-1 The operation principle of GBT. a) Flatband condition b) Off-state c) On state 28
2-2 a) Wurtzite b) Zinc blend crystal structure 30
2-3 Structure of GaN wafer used in the current study 31
2-4 Simulated energy band diagram of GBT in a) Flatband condition b) Off-state c) On state 34
2-5 Band line-up of the device used in this work. 35
2-6 A schematic representation of designed graphene-on-GaN GBT. . . . 35

3-1 SEM image of the top view of a fabricated device 40
3-2 Optical image of the fabricated devices. 40

4-1 (a) Measurement configuration for base-emitter heterojunction characterization . Carrier flow for the given biasing condition is shown by white arrows. (b) Top view of device layout. 42
4-2 Energy band diagram of the Base-Emitter heterojunction 44
4-3 Current-voltage characteristics of base-emitter heterojunction 45
4-4 Current-voltage characteristics of Base-emitter heterojunction at three different temperatures 48
4-5 (a) Measurement connection for the characterization of Base-Collector heterojucntion 48
4-6 Current-Voltage characteristics of Base-Collector heterojunction . . . 49
4-7 Device configuration for common-emitter characteristics measurement 50

4-8 Common-Emitter characteristics for different base-emitter voltage of the device 51
4-9 a) Transfer ratio and b) Transconductance of the GBT 52
4-10 Common-emitter characteristics of fabricated device for different base-emitter voltage at three different temperatures (250 K, 150 K and 4 K). The solid lines represent characteristics at 250 K, circles represent 150 K and dashed line represent 4K characteristics. 53
4-11 a) Simulated output characteristics for different V_{BE}. b) Simulated output characteristics computed for V_{BE} =2.5 and 2.75 V for different oxide thicknesses. Oscillations shown are due to quantum interference at the two interfaces of the Al_2O_3 layer, as previously observed in MOS structures, and might experimentally be smeared out by surface roughness of the Al_2O_3 layer and by electron-phonon interaction at room temperature, which broadens the energy distribution of the electrons impinging onto the Al_2O_3 layer[39] and this effect is not taken into account in our simulations. 54
4-12 Simulated Cut-off frequency for different bias points for the device with the 8 nm Al_2O_3 barrier for different V_{BE} biases at a step of 0.25 V. The bottom curve represents the curve for V_{BE}=2.0 V. 55

5-1 (a) Comparison of lattice constant and energy gap between $In_{0.17}Al0.83N$ and other nitride alloys. (b) Comparison of simulated 2-DEG sheet charge density between InAlN/GaN and AlGaN/GaN heterostructure[40] 59
5-2 Simulated common-emitter characteristics of GBT with GaN collector 60

List of Tables

4.1 Calculated diode parameters obtained from two terminal measurements 46

A.1 Detailed process flow for Graphene/GaN vertical Transistor 65

Chapter 1

Introduction

The first isolation of graphene, the isolated monolayer of well-known and widely used Carbon allotrope graphite, by micromechanical exfoliation [11] opened up a new era for the electronics. Thanks to its unique electronic structure, transport properties and morphology, as well as exciting physics and chemistry, graphene has opened up new opportunities for novel device engineering and circuit design. The excellent mobility of graphene, combined with its high saturation velocity, thermal conductivity and micrometer-scale ballistic transport, makes this material an outstanding candidate for the next generation high frequency transistors .

Graphene transistors exhibit high current density[12] and excellent electrostatic confinement[13] which increase the conversion efficiency, reduce their noise level, and improve the operating frequencies of future amplifiers. Despite of rapid progress in the field of GFETs in terms high frequency performances and its future application in circuits and systems, many challenges are needed to overcome.However, for the high frequency and analog/mixed technologies both CMOS and bipolar technologies provide solutions for specific applications in the specific frequency range. The CMOS circuits are used for mobile transceivers in radio frequency (RF) range (0.4-30 GHz), various commercial applications in millimeter-wave (30-300 GHz) frequency range and optical communications using CMOS photonics.Bipolar circuits are used in low frequency ($<$ 5GHz) cellular power amplifiers, for wireless (60 GHz) and wireline communications (40 Gb/s, 100 Gb/s, 400 Gb/s Ethernet and beyond), automotive

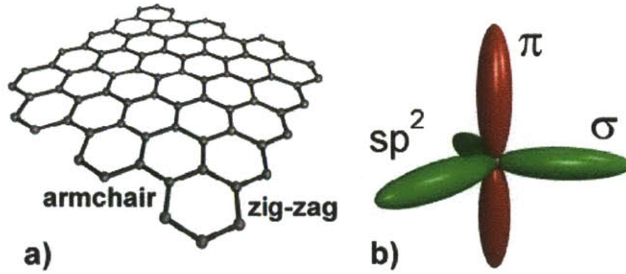
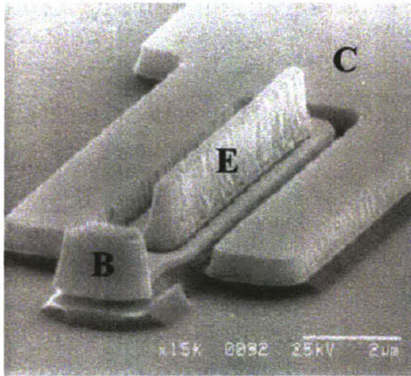
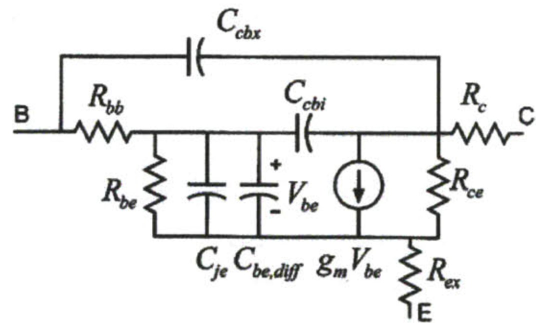


Figure 1-1: a) Schematic diagram of the atomic structure of monolayer honeycomb graphene . The archair and zig-zag indicates the nature of edge-states of planar semi-infinite sheet of Carbon atoms. [1] b) Three inplane $\sigma(s, p_x, p_y)$ and out of plane $\pi(p_z)$ orbitals of sp^2bonded hexagonal network of Carbon atoms.

radar (77 GHz) and emerging applications up to 170 GHz for industrial, medical, security, space, radio-astronomy, and other technologies[4]. The primary goal of this thesis to focus to develop a vertical unipolar transistor for potential replacement of future bipolar circuit applications.



(a) (a)



(b) (b)

Figure 1-2: (a) Scanning Electron Microscope (SEM) image of a state-of the art Heterojunction bipolar transistor (HBT) [2],(b)small signal hybrid pi equivalent circuit of a HBT

The need for vertical graphene transistors in high frequency electronics can be understood using the small signal equivalent circuit of HBT as in Fig. 1-2b. The

current gain frequency of a HBT is given by

$$\frac{1}{2\pi f_T} = \tau_b + \tau_c + \frac{kT}{qI_C}(C_{je} + C_{cb}) + C_{cb}(R_{ex} + R_c) \tag{1.1}$$

$$\tau_b = T_b/v_{inj} \tag{1.2}$$

$$C_{cb} = \frac{\epsilon A_c}{T_c} \tag{1.3}$$

$$C_{je} = \frac{\epsilon A_e}{T_e b} \tag{1.4}$$

Here in equation 1.1 τ_b is the base transit time for the injected carrier from emitter and given by equation 1.2 which depends on base thickness , T_b and carrier injection velocity v_{inj}; τ_c is the collector transistor time which depends on the collector thickness; C_{je} and C_{cb} is the emitter and collector junction capacitance respectively and depends on emitter area, A_e and collector area, A_c respectively.
One of the most important figures of merit of a high frequency transistor is the current gain cut-off frequency (f_T) which needs to maximized to ensure wide bandwidth operation of high frequency circuits and systems. It is clearly evident that to maximize the cut-off frequency the base transit time is needed to be minimized and collector current density needed to be maximized. Also, another limitation in HBTs is minority carrier diffusion capacitance. If the device can get rid of minority carrier induced delay and reduce the base thickness, the device can simultaneously achieve high cut-off frequency and high power driving capability. Hot electron transistors which is based on unipolar transport and vertical transport can overcome this limitation of HBTs in terms of maximizing high frequency performances.
Another figure of merit in high frequency transistor is the common-base current gain or current transfer ratio or injection ratio which is defined by

$$\alpha = \frac{I_C}{I_E} \tag{1.5}$$

Here I_C is the collector current and I_E is emitter current of the device. This ratio ef-

fectively determines the conversion efficiency of the device by determining percentage of injected carriers from the base is collected in the collector and contributing active device current. The ideal value of α is 1 for any device. The gain and bandwidth of bipolar jucntion transistor based amplifier are strong functions of common-base current gain. So,to maximize device performance both f_T and α need to be maximized.

1.1 Hot Electron Transistors

Hot-electron transport plays an important role in semiconductor device operations, mostly considered as responsible for degradation of gate dielectric in MOSFET which eventually may lead to device failure. However, potential of high speed operation courtesy to high energy injection which leads to ultra fast carrier velocity leads to devices utilizing the hot electron phenomena . Most popular hot electron device is Gunn diode[14] and non-volatile memory devices(FAMOS)[15]. The first proposal of a three terminal hot electron transistor was made by Mead [16] as shown in Fig. ??His proposed device, the MOMOM (metal-oxide-metal-oxide-metal), was based on electron tunneling through a thin oxide into a high energy state in the metal base.

These high-energy electrons were then able to surmount the second oxide barrier and get collected in the metal electrode on the right of Fig. ??). The MOMOM was a potentially fast device for two main reasons; it employed a thin base region which resulted in low transit times for the injected electrons and exhibited low RC charging delays due to the metal base layer. Since the mean free path of hot electrons in metals are very short, and pinhole-free thin metal layers were difficult to fabricate, the current gain of the transistor was low. The low injection and collection efficiencies, due to traps and thickness of the second oxide layer, resulted in these devices being subsequently modified into Metal Base Transistors (MBT)[17, 18], which employed a metal base layer between two semiconductors and the injection of hot electrons was primarily by thermionic emission over the metal-semiconductor Schottky barrier.
The semiconductor-metal-semiconductor here denotes a metal base transistor which operates based on the principle of thermionic emission of carriers from an emitter

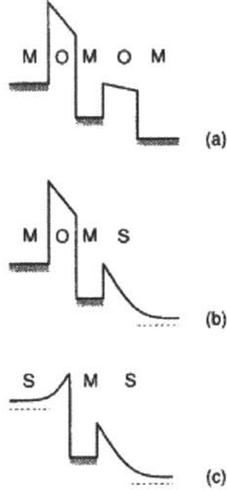
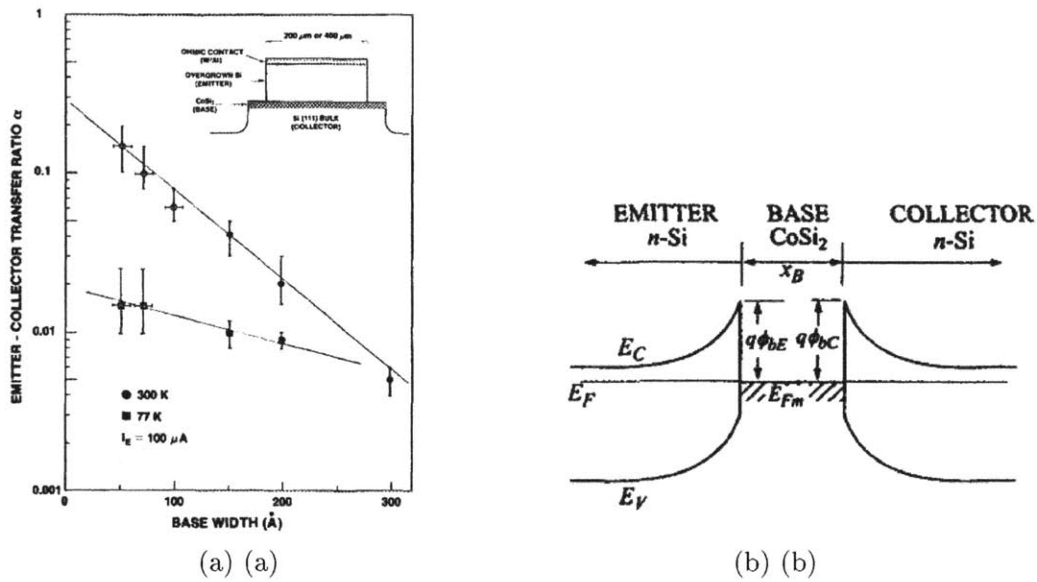


Figure 1-3: Energy band diagrams of different versions of Metal base transistors. Left: (a) MOMOM; (b) MOMS; (c) SMS. Each metal (M) and semiconductor (S) can be biased independently. [3]

rather than the quantum mechanical tunneling of hot carriers into the base.[17, 18]. These devices were point contact based and their performance was limited by quantum mechanical reflection and other fabrication-related issues and later after the discovery of epitaxial growth first monolithic device was demonstrated on the $Si/CoSi_2/Si$[4]system which had a base thickness of 5-30 nm. This device suffered from low common a low transfer ratio, α, even when extrapolated to zero base thickness as demostrated in Fig. 1-4a.

1.2 III-Nitride Hot-Electron Transistor

III-Nitrides (mainly GaN) High Electron Mobility Transistors (HEMT) are widely popular in high frequency and high power applications. Cut-off frequencies of GaN HEMTs have been demonstrated as high as 375 GHz [13]. However, the bipolar technology in III-Nitrides has not reached the same level success as in HEMTs. This limitation arises from the low hole concentrations ($<10^{18}\ cm^{-3}$)[14] in bipolar devices due to the high activation energy of acceptor impurities activation and hence affecting their base resistance . To achieve high gain and current-gain cut-off frequencies the



(a) (a)

(b) (b)

Figure 1-4: (a)Emitter-collector transfer ratio for different base width and (b) the energy band diagram of first monolithic metal base transistor[4]

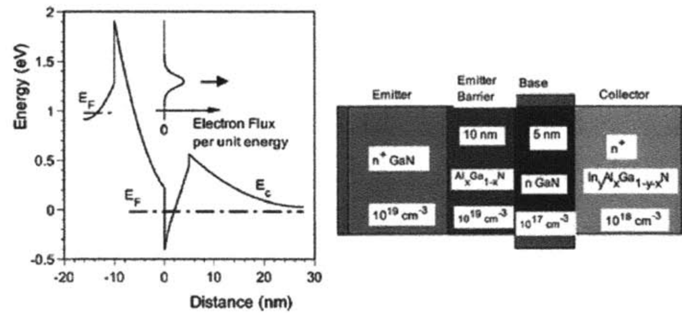


Figure 1-5: The device structure of proposed III-Nitride Induced base transistor[5]

base resistance need to be minimized. These challenges can be overcome through the fabrication of unipolar GaN HETs[19] or induced base transistors as shown in Fig. 1-5 instead of HBT's with a heavily n-doped base . High electron concentration due to n-doping, the presence of a polarization induced 2-DEG (n_s $10^{13}cm^{-2}$) and a high mobility (1300 cm^2/Vs) in these devices has the potential of a low base resistance and hence better high frequency performance. Simulation results[5] demonstrated the possibility of 0.6 THz cut-off frequency operation of these transistors.

Dasgupta et al.[6] demonstrated HET based on III-Nitrides using an AlGaN (24%) emitter,10-nm GaN base, and an AlGaN (8%) collector structure as shown in Fig. 1-6

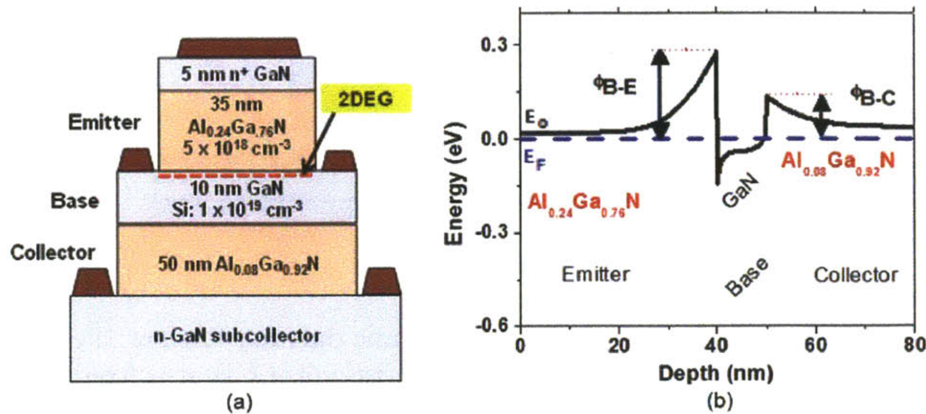


Figure 1-6: (a) Device Structure and (b) band diagram of fabricated III-Nitride HET [6]

The use of AlGaN in the emitter and collector provides flexibility in the device design by varying mole fraction of Al. For the demonstration the B-E and B-C barrier was 0.27eV and 0.13 eV respectively. Temperature dependent measurement of the device characteristics confirms the transport mechanism as thermionic emission. So, in strict terms the device is not hot electron transistor but rather a metal base transistor. But the thermionic nature of transport facilitates the high drive current capability in this device and For V_{CB} greater than>0.5 V, a common base transfer ratio, $=$ IC/IE,ofâĹij0.97âĂŞ0.98 was obtained. The current gain or β which was calculated from the $= /(1)$ found to be around 30-45[6]. The device serves a inspiration for a perfect HET to be realized. Despite of demonstrating high current and transfer ratio the device cant fulfill the promise HETs because the limitation of scalability of base thickness. This is an inherent limitation of the conventional semiconductor growth process, which increases the interface roughness and degrades the transport properties in very thin ($<$ 5 nm) base layers.

1.3 Vertical Graphene Transistors

Two-dimensional materials have the natural advantage of being ultra-thin stable materials. This makes them ideal candidates to overcome the issue of scalability in the

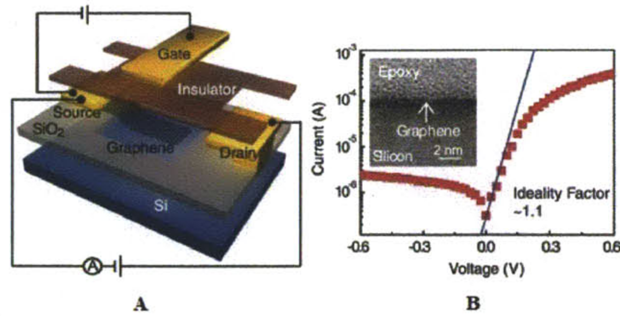


Figure 1-7: Graphene barristor. (A) A schematic diagram to show the concept of a GB. (B) Current versus bias voltage characteristic of a GB at a fixed gate voltage Vgate = 0 V, showing a Schottky diode characteristic. The inset shows a TEM image of graphene/Si [7]

base of HETs and during the last few years several groups have proposed different versions of vertical graphene transistors[20, 7, 9, 10]. In the following section several vertical graphene transistors demonstrated on a large scale are discussed.

1.3.1 Graphene Barristor

Graphene is the most celebrated two-dimensional material because of its large array of unique properties, including ultra-high mobility, high thermal conductivity and high saturation velocity. But the absence of a band gap and the resulting high off-state leakage currents severely limits the use of graphene as the channel material in field effect transistors (FETs) for logic applications. At the same time, the use of graphene RF transistors in analog applications, where the off-state leakage current is not that important, is limited by the poor current saturation and subsequent low voltage gain of these devices. To overcome some of these limitations, Yang et al.[7] demonstrated a three terminal device which was based on vertical transport across graphene(Fig. 1-7). The device operational principle is based on an electrostatically gated graphene/silicon interface where a tunable Schottky barrier controls charge transport across a vertically stacked structure. The device was named as graphene barristor (GB), after its variable barrier operation, and it is a solid state counterpart of vacuum triodes. In this device large modulation on the device current (on/off ratio of10^5) is achieved by adjusting the gate voltage to control the graphene-silicon

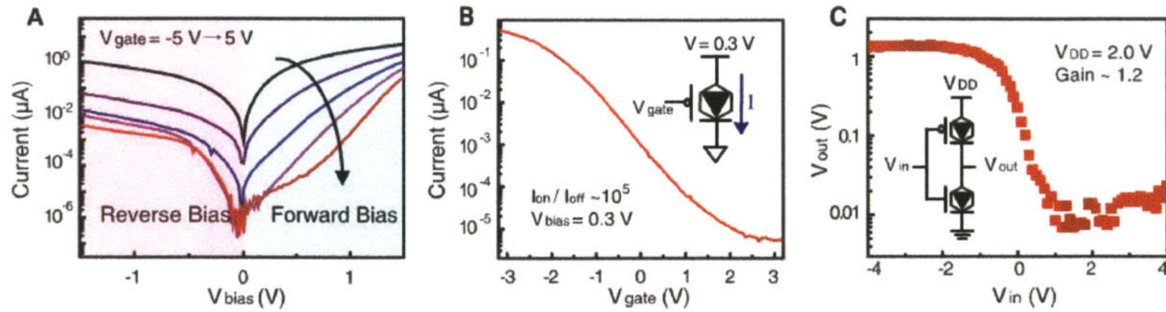


Figure 1-8: a) Switching and b) Output characteristics of graphene barristor , c) Inverter operation based on graphene barristor [7]

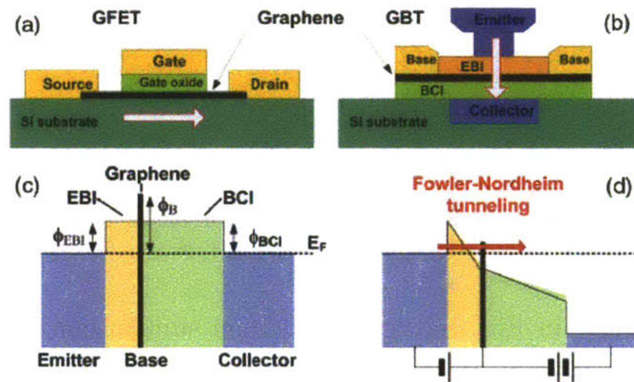


Figure 1-9: Schematic cross sections of (a) GFET and (b) GBT and the schematic band diagrams of (c) an unbiased and (d) biased GBT. [8]

Schottky barrier. The lack of Fermi-level pinning at the interface of Schottky junction allows the barriers height to be tuned 0.2 electron volt by adjusting graphenes work function, which results in large shifts of the diode threshold voltages.

Wafer scale fabrication of Graphene Barristors on respective 150-mm wafers also demonstrated in this work. Figure 1-8 demonstrates that these devices can also be configured as both p and n type .combining complementary p- and n-type GBs, inverter and half-adder logic circuits has been demonstrated. But the frequency performance and drive current capability of this kind of devices are yet to be reported.

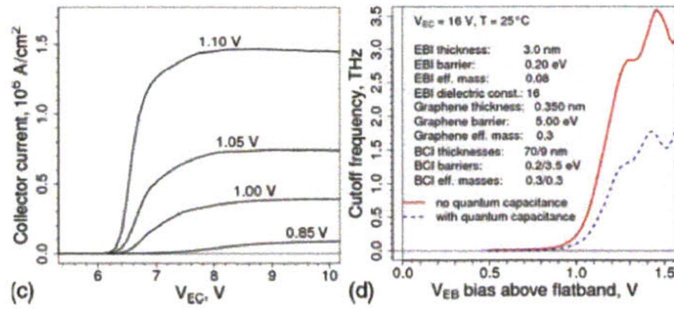


Figure 1-10: a) Output characteristics of simulated GBT b) Cut-off frequency of the simulated GBT. [8]

1.3.2 Graphene Base Transistor (GBT)

The Graphene Base Transistor (GBT) is a new class of vertical device as shown in Fig. 1-9(b) that tries to achieve record high frequency operation [8, 21]. GBTs combine a graphene base with some of the key the concepts of early HETs [16, 17] to demonstrate low-off current , full drain current saturation and power amplification, all of them absent in GFETs.

The device performance in Fig. 1-10 expected from simulations was very promising as it exhibits collector current switching over several orders of magnitude (10^4), collector current saturation, intrinsic voltage gain higher than unity[22, 23] and cut-off frequency greater than THz. Although these simulations were just a first order estimation without considering any secondary effects, they provide the basic framework for fabrication and design of GBTs. Reference [23] shows that when base-emitter and base-collector barriers are chosen appropriately GBTs can be made with combination of conventional semiconductor systems like SiC, InGaAs, GaN, InP or Poly-Si.

1.3.3 Graphene-base Hot Electron Transistor

Vaziri et al.[9] and Zeng et al.[10] demonstrated the first graphene-base vertical hot electron transistors. Both groups used a similar to each other structure as shown in Fig. 1-11 (a) and (c) respectively, consisting of a heavily doped Si emitter, SiO_2 E-B barrier, Al_2O_3/HfO_2 B-C barrier and a metal (Ti/Pt) collector. The operation

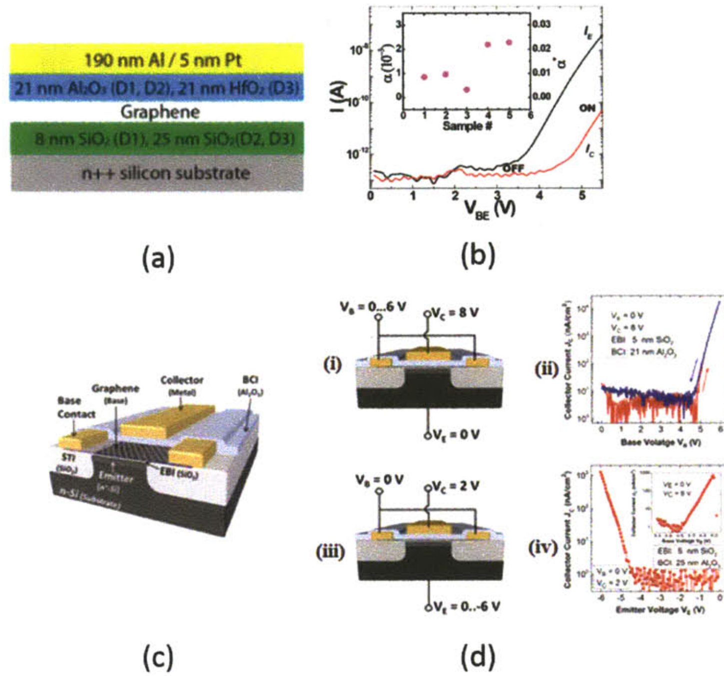


Figure 1-11: (a) and (c)Structure and (b) and (d)output characteristics of graphene-base HETs as demonstrated in[9, 10]

of these devices is based on the tunneling injection of electrons from n+ Si emitter to graphene and exhibit high on-off ratio (10^4). But the devices suffer low current density ($nA - \mu A/cm^2$) (Fig. 1-11(d)) and very low (4.8%[9], 6.5%[10]) unnormalized common-base current gain (α) (Fig. 1-11(b)) . The low current density is mainly due to low tunneling through the amorphous oxide and it limits the application of these devices at high frequencies, where the cut-off frequency strongly depends on the collector current density. Although these devices are the first successful demonstration of HETs in two-dimensional materials, they still need very significant work to improve their performance to the point where they can be useful.

The focus of the work summarized in this thesis is to design, fabricate and analyze the performance of a new kind of vertical graphene base transistor with high current drive capability and transfer ratio, in order to evaluate its potential in high frequency electronics.

Chapter 2

Device design

This chapter describes a new kind of vertical graphene-base transistor that overcomes the limitations of existing structures in terms of both technological and performance point of view.

2.0.4 Operating principle of Graphene-Base Transistor

HETs or GBTs are the unipolar analogue of HBT and likewise it has three terminals

1. Emitter: To source the carrier
2. Graphene Base: To control the device operation by means of controlling the different energy barriers
3. Collector: To collect the injected and successfully transported carrier

Apart from these three terminals GBTs require two additional layers in their physical structures. To achieve efficient device operation both emitter and collector are highly conductive but unlike the base of HBT which is made of a semiconductor, graphene is a highly conductive semi-metal. So to ensure electrical isolation the graphene base is sandwiched between a base-emitter and collector-emitter barrier.

The device operation of a GBT can be explained using the cartoons in Fig. 2-1.

- Flatband condition: In the flatband condition there is no bias applied in any terminal of the device. In ideal case in the flatband condition there is no bending

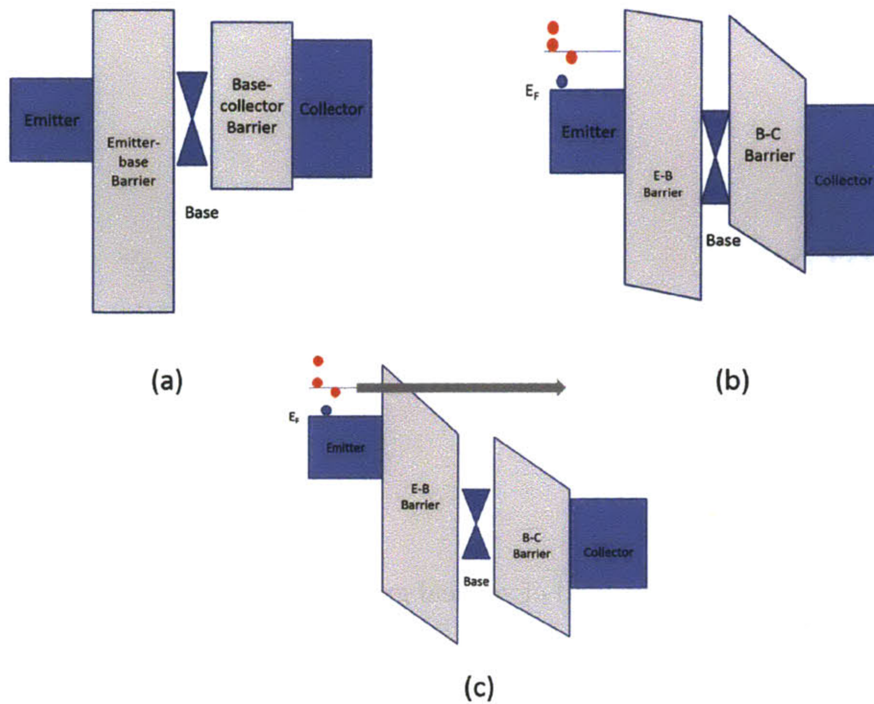


Figure 2-1: The operation principle of GBT. a) Flatband condition b) Off-state c) On state

in the energy band diagram and no resulting electric field across the device and hence no current flow in the device. In practice, there is always a finite amount of electric field in the device which causes a carrier flow.

- Off-state: When there is no carrier flow from emitter to collector, the device is considered to be off as in Fig. 2-1(b). The carriers in the emitter experience a large energy barrier which prevent them from reaching the base. In practice there is always some finite amount of current flow in the off-state, the off-state leakage current.

- On-state: In this bias as shown in Fig. 2-1(c) condition the bias between base and emitter is such that energy barrier is lowered enough to allow carrier flow from emitter to base.

Carrier Injection

This flow of carrier can be supported by two different mechanism

1 Quantum mechanical tunneling

2 Thermionic emission

When carriers experience a thin barrier due to an applied electric field, carriers can tunnel through the barrier according to quantum mechanics. This tunneling can be either Fowler-Nordheim or Pool-Frankel tunneling. Tunneling is a very fast process and high frequency operation can be expected in tunneling-dominated devices. Even when the physical barrier is not thin enough to support the tunneling process, some carriers can still be injected across the barrier if they have more energy than the barrier. This mechanism is known as thermionic emission of carriers.

Base Transport

In the base, carriers are either ballistically transported to the collector or lost through scattering or quantum mechanical reflection at the base-collector interface. The lost carriers constitute the base leakage current of the GBTs. Depending on the bias between base and collector injected carriers can be collected or blocked by the B-C barrier.

2.0.5 Material selection

To maximize the electrical performance of GBTs, the material for each layer should be designed carefully. As mentioned in the sections above, previously demonstrated GBTs have very limited current driving capability because of poor carrier injection. Therefore, our initial focus is to maximize the drive current and achieve a reasonable common-base transfer ratio. Once that these goals are satisfied, the device structure will be optimized to achieve desired high frequency operation.

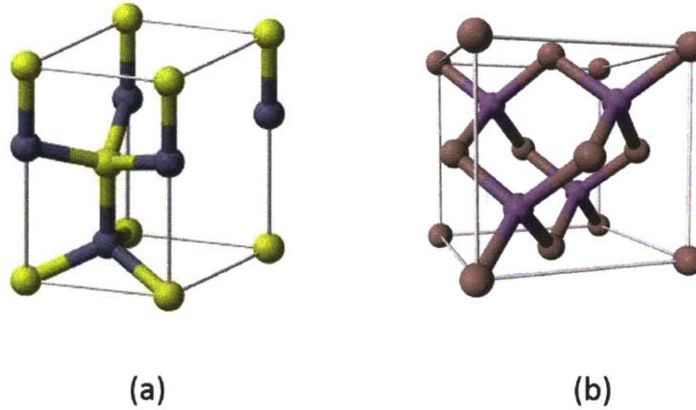


Figure 2-2: a) Wurtzite b) Zinc blend crystal structure

Emitter and Emitter-base barrier

In the current study, a $GaN/Al_{0.3}Ga_{0.7}N$ heterostructure is chosen as the emitter and emitter-base barrier. The III-Nitride semiconductors are popular in the field of semiconductor devices for their unique properties (i.e. wide bandgap, polarization etc.) Among them, GaN is arguably the most popular material thanks to its well understood growth and many uses in optoelectronic devices. The crystal structure of GaN is Wurtzite, with Gallium (Ga) and Nitrogen (N) atoms ionically bonded, which in combination with the non-centrosymmetry of the Wurtzite crystal structure and high electronegativity of the nitrogen atom induces a large net polarization field in these materials. This polarization field is referred to as a spontaneous polarization (Psp) because it originates from the intrinsic material properties like crystal structure and material composition. Alongside of this spontaneous polarization, an additional polarization field is also present in the III-Nitride heterostructures. When two different III-Nitride materials (i.e. GaN and AlGaN) are grown on top of each other, the lattice constants of the both materials are not always perfectly matched. This mismatch in lattice constants induces strain or defects into the thin layer depending on its thickness relative to a critical thickness. If the thickness is less than critical thickness then an additional polarization field, the piezoelectric polarization, is induced due to the lattice mismatch strain. In the AlGaN/GaN heterostructure, free electrons

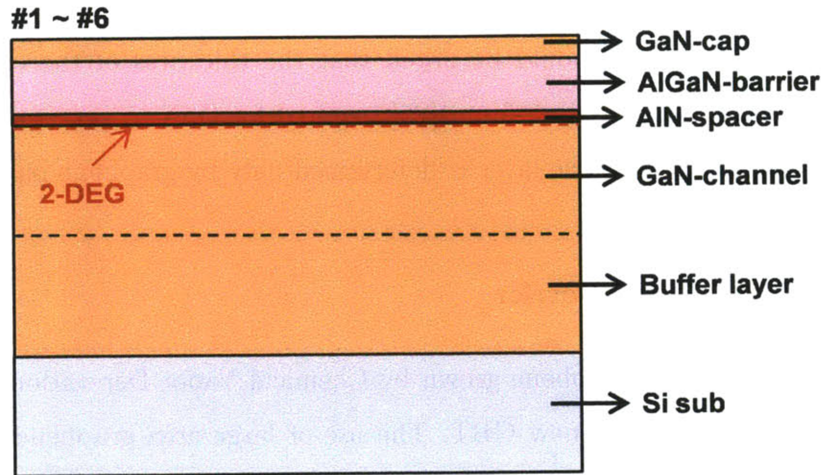


Figure 2-3: Structure of GaN wafer used in the current study

accumulate at the interface between the GaN and AlGaN material, helped by the high electric field induced in the AlGaN barrier due to the difference in polarization between AlGaN and GaN, and form a two-dimensional electron gas $(2 - DEG)$[24] The wide bandgap AlGaN barrier provides the separation of 2-DEG from the positive charges and hence reduces the possibility of scattering which eventually leads to a high mobility in the order of 1000-2000 $cm^2/V - s$ in the 2-DEG. Also due to the large difference in polarization fields between AlGaN and GaN a high carrier density ($10^{13}cm^{-2}$) can be achieved in these heterostructure. that the AlGaN/GaN structure has traditionally being used in lateral HEMT structures, however we use is as an emitter because of the high conductivity and excellent quality of the AlGaN barrier.

Fig. 2-3 shows the detailed structure of the wafer used for the device fabrication in this study.The GaN film is grown using Metal Organic Vapor Phase epitaxial (MOCVD) technique on a Si substrate. The use of Si substrate makes it suitable for integration with Si electronic technology in the future. The buffer layer accommodates the large lattice mismatch between the GaN and the Si substrate and thus minimize the lattice-mismatch induced strain. The aluminum mole fraction in the AlGaN barrier of the samples used in the current study is 30%. An AlN spacer between GaN and AlGaN was present in some of the samples to increase the energy barrier between the GaN channel and the AlGaN barrier, and hence to reduce the

Coulomb scattering. The epitaxial structure is cap by a 3 nm GaN layer to improve the surface morphology. It should be noted that the thickness of the cap-layer is below the minimum thickness (~5-6 nm)[25] required for GaN to generate a 2-DEG so that the transport in the base layer is determined only by graphene base.

Base and Base-Collector Barrier

A monolayer of large area graphene grown by Chemical Vapor Deposition (CVD) is used as the base layer in our new GBT. The use of large area graphene facilitates the possibility of wafer scale fabrication of GBTs. Also CVD graphene is low cost compared when compared with epitaxial graphene and has higher yield than when using micromechanical exfoliated graphene. For the base-collector barrier, a thin oxide layer can be used, such as Al_2O_3 or HfO_2. For the initial study Al_2O_3 was chosen as the B-C barrier. Ti/Au stack was chosen as collector material.

The working principle of the device demonstrated in this paper is shown in Fig 2-4 by a series of band diagrams drawn from the energy band data available from the literature[26, 27]. Under zero bias condition (both base-emitter and base-collector voltages are zero), the band alignment is such that electrons are not energetically favorable for carrier injection and hence there is no current flow in the device (Fig. 2-4a(a)). When a base-emitter voltage VBE, is applied, the carrier concentration and potential in graphene changes. The shift of the graphene Fermi level is related to the change in the carrier concentration by the relation,

$$E_F = \frac{h}{2\pi} vF\sqrt{\pi \Delta n} \tag{2.1}$$

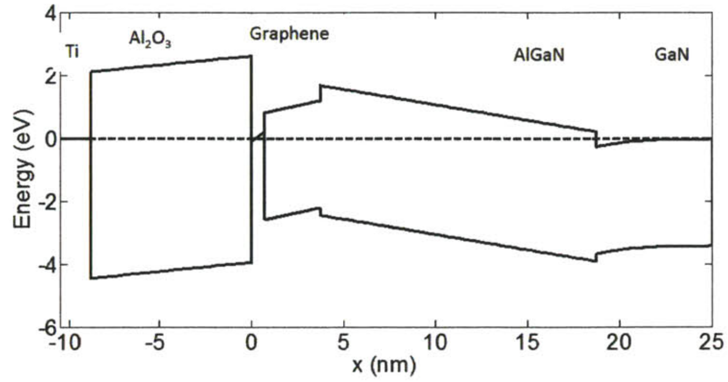
This downward shift of Fermi level and change of barrier shape due to the applied electric field increases the carrier injection probability significantly. However the band alignment and bias condition still do not favor electron tunneling or over the barrier thermionic transport through the base-collector junction and hence the device is in the off-state (Fig. 2-4a(a)). If a positive collector-base voltage, VCB, is now applied, the device is in reverse bias and the electrons can tunnel through the GaN/AlGaN

barrier or over the barrier and the graphene, to be finally collected at the collector. The device is then in ON state as shown in Fig. 2-4c. The corresponding band-lineup for the material selected is given in Fig. 2-5.

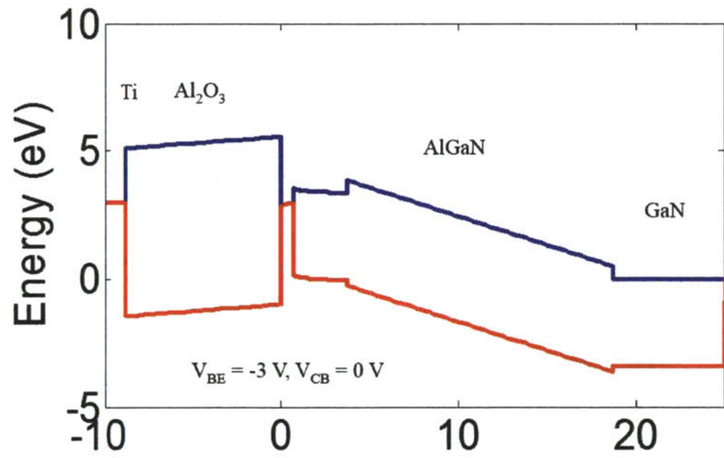
2.0.6 Physical Structure design

After selection of materials for different layers the physical layout of device was carefully designed. The final structure

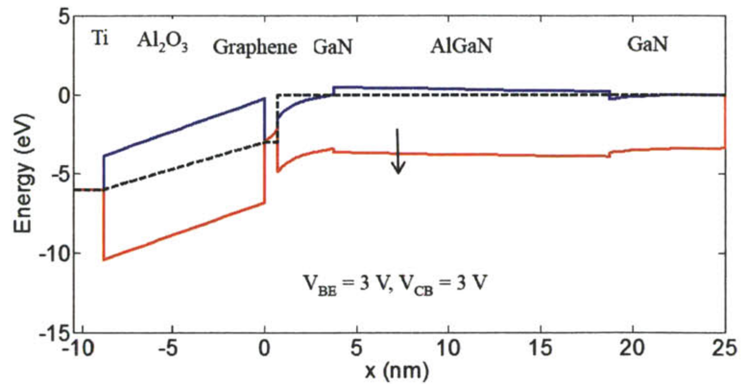
The top view of a designed physical layout of RF transistor is shown in Fig. 2-6. The measurement pads are designed such a way that the structure is compatible with GSG probe configuration. Also the mask contains structures like TLM for both base and emitter contact, capacitors; Hall bars; open and short RF transistors to facilitate the de-embedding of parasitics during RF measurement



(a) (a)



(b) (b)



(c) (c)

Figure 2-4: Simulated energy band diagram of GBT in a) Flatband condition b) Off-state c) On state

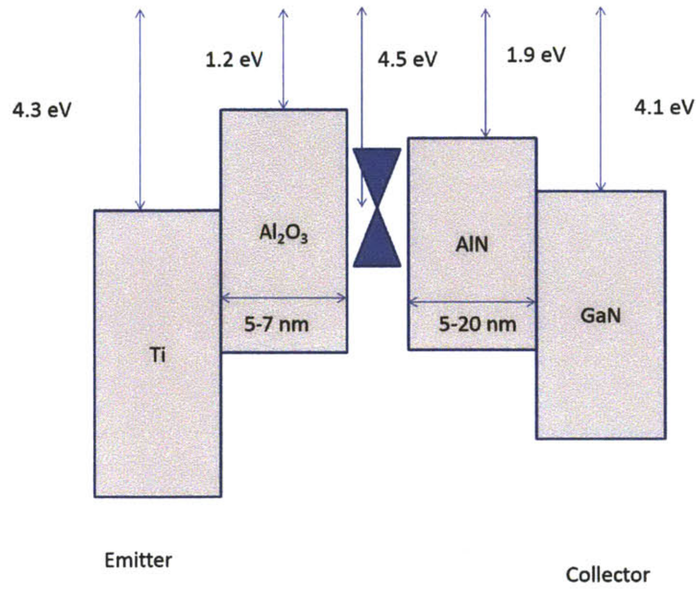


Figure 2-5: Band line-up of the device used in this work.

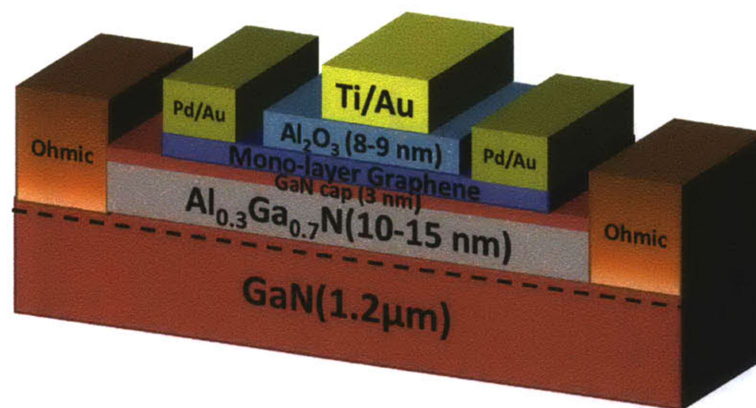


Figure 2-6: A schematic representation of designed graphene-on-GaN GBT.

Chapter 3

Fabrication

The details of fabrication of graphene-on-GaN vertical transistors is given below:

3.1 Ohmic Contact

The fabrication starts with the formation of ohmic contact to the 2-DEG formed in the interface of the GaN/AlGaN heterojunction. For ohmic contact there are several widely used recipe. Most popular one is the metal stack use of the combination of Ti/Al (i.e. Ti/Al/Ni/Au, Ti/Al/Mo/Au, Ti/Al/Ti/Au). Ti has a workfunction of 4.3eV and Al also has similar workfunction. Ti forms TiN with creating Nitrogen vacancies in AlGaN and thus creates a low resistance tunneling path from the metal to the 2-DEG. The Ti/Al has the tendency of oxidizing in the ambient condition and increase the contact resistivity. So Au is used on top of the Ti/Al stack as a protection layer. The overall metal stack is Schottky in nature and ohmic contact formation requires a step of rapid thermal annealing (RTA) at a very high temperature (800-900 °C). At this temperature Au tends to diffuse through the Al and thus causing degradation of contact resistance. However, to avoid this diffusion an layer of Ni is inserted between Ti/Al and Au. In this work, formation of ohmic contacts consist of photolithography using AZ5214 photoresist and subsequent ebeam evaporation of Ti(20 nm)/Al(100 nm)/Ni(25 nm)/Au (50 nm) .

3.2 Mesa Etching

After ohmic contact formation mesa etching is performed using a low power Reactive Ion Etching(RIE) etch in BCl_3/Cl_2 chemistry to perform device isolation. The depth of etching is around 150 nm to confirm that it is much deeper than 2-DEG channel ensuring complete isolation.

3.3 Graphene Growth and Transfer

A monolayer graphene film was then transferred onto the GaN/AlGaN substrate using a poly(methyl methacrylate) (PMMA) transfer method[28]. The graphene used here was grown in a low pressure chemical vapor deposition (LPCVD) system on copper foil which ensures uniform large area monolayer graphene. The graphene synthesis is done at 1000 °C while flowing H_2 and CH_4 gas. To transfer graphene from the copper foil to the target substrate PMMA (950k 4.5% dissolved in Anisole) is spin-coated on the graphene film grown on copper. The stack is then placed PMMA-side-up in CE-100 copper etchant (mixture of HCl and $FeCl_3$) for 10 min (depending on the thickness of copper foil), allowing the copper to completely dissolve. The PMMA/graphene film remains floating and is transferred into 10% HCl using a glass slide for 20 min to remove $FeCl_3$ residues. Finally, the film is rinsed with DI water for some amount of time and transferred onto the patterned GaN/AlGaN wafer. To ensure this, we first place the substrate/graphene/PMMA stack in an oven set to 800 °C for 5min to evaporate most of the trapped water and then bake the sample for 20 min at 1300 °C to remove any remaining residues. To remove the residual PMMA the sample is kept in acetone overnight and then annealed in forming gas (200 sccm H_2/200 sccm Ar) at 350 °C for 3 hours.

3.4 Base Contact and device isolation

The contact on graphene is a fabricated by photolithography using AZ-5214 resist and subsequent ebeam deposition of 1.5-nm Ti/45-nm Pd/15-nm Au. Contact resistance

of these metal stack is 200âĂŞ500 $\omega\mu m$ [29]. After lift-off graphene device isolation is performed through photolithography and subsequent RIE. This step is required because graphene is an excellent conductor and all the devices in the sample are electrically shorted through graphene. A bilayer resist (MMA/OCG834) is used in this step. OCG 834 is a positive photoresist which is used to pattern graphene and remove unwanted graphene. To assist remove OCG834 and keep the graphene surface relatively clean, an MMA layer is spin-coated as a buffer layer. This buffer layer of MMA can easily be removed in acetone after isolation. After exposure and subsequent development in OCG934 developer, the sample is transferred to Reactive Ion etcher (RIE) and exposed to O_2 plasma for 4 minutes. This step removed all the unwanted graphene.

3.5 BCI and Collector formation

Next step in the fabrication involves formation of base-collector barrier. In the current study this layer is a oxide (Al_2O_3 or HfO_2). In both cases the deposition is done in a two-step process. At first step a thin layer of Al (1.5 nm) is deposited on the sample at a very slow deposition rate (0.1 nm/s) in ebeam evaporator. Then the sample is taken out from the chamber and let it oxidized in ambient condition. The oxidation can be assisted by heating the sample in a oven or hotplate. This thin layer of oxide acts as the seed layer of subsequent Atomic Layer Deposition (ALD). The sample is then transferred to the ALD chamber. The Al_2O_3 is then deposited by flowing the pre-cursors TMA and water at a temperature of 250 °C. Final step of the device fabrication involves the deposition of collector contact. If the base-collector barrier is Al_2O_3 then during photolithography and additional step is required. This because common photolithography developers are TMAH based which etches the Al_2O_3. Depending on the deposition temperature of ALD this etch rate can be 2.5-5 nm/min. We have to alternatives here for the lithography of collector contact. We can use Electron Beam Lithogrpahy or we can use sputtered Tungsten as the mask to protect the oxide from etching. 100 nm Tungsten is deposited by sputtering. Finally

Figure 3-1: SEM image of the top view of a fabricated device

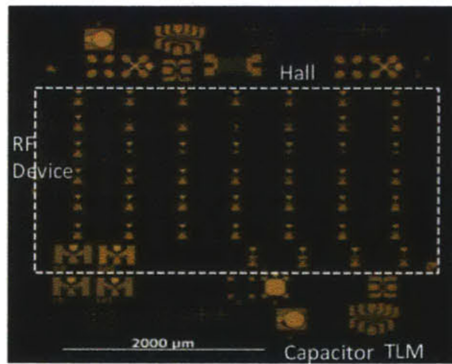


Figure 3-2: Optical image of the fabricated devices.

a Ti/Au (20nm/100nm) collector contact was patterned and deposited by electron beam evaporation. After the deposition of collector metal stack the Tungsten can be etched through RIE using SF6. Fig. 3-1 and 3-2 respectively shows a top-view Scanning Electron Microscopy (SEM) and optical image of the fabricated device.

Chapter 4

Device Characterisitics

In this chapter the characterization of the fabricated transistor is discussed in detail. The fabricated device is a three terminal device which can be considered as the combination of two two-terminal devices cascaded together. To understand the device operation properly first we characterized the individual two terminal devices separately and then study the three terminal metal base transistor. All the measurements presented in this device were done using a Cascade MicroTech Summit 11000AP cryogenic Probe Station under high vacuum ($10^{-4} - 10^{-5}$ Torr). Before measurements the devices were kept in high vacuum overnight to minimize the absorption of water by graphene which tends to dope it and shift the Fermi level and hence affect the device operation. To accurately measure the low leakage currents of this device, a tri-axial cable configuration was used, where the leakage current between the core and the inner-shield can be minimized.

4.1 Heterojunction current-voltage measurement

The device fabricated in this thesis is made of two back-to-back two-terminal devices or junctions:

- Emitter-Base heterojunction diode
- Base-collector diode

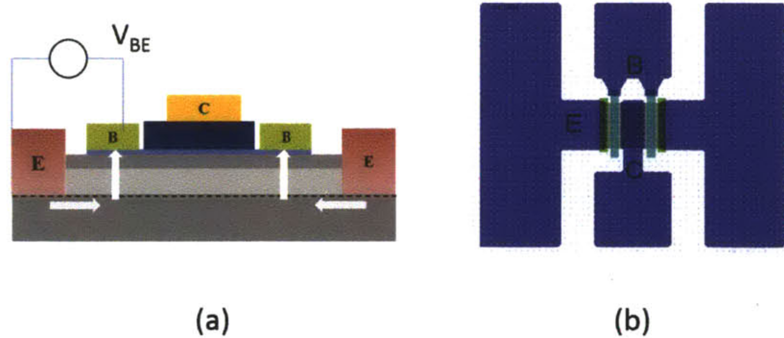


Figure 4-1: (a) Measurement configuration for base-emitter heterojunction characterization . Carrier flow for the given biasing condition is shown by white arrows. (b) Top view of device layout.

4.1.1 Emitter-Base heterojunction

The emitter-base heterojunction consists of the GaN/AlGaN/graphene structure. Fig 4-1(a) shows the measurement connection during the measurement of E-B heterojunction and Fig. 4-1 (b) shows the top view of the device layout.

The active area of the device is 37μm $\times$ 60 μm. To ensure uniform potential in the base region , the base electrodes are designed as shown in Fig 4-1(b). The current conduction in this heterojunction consists in general of two different components: thermionic emission and quantum mechanical tunneling. However the probability of tunneling through a barrier depends both on the height and thickness of the barrier. Here, the thickness of AlGaN is 10 nm and the barrier height from $GaN/Al_{0.3}Ga_{(}0.7)N$ is 0.34eV, so from the WKB approximation we find the tunneling probability is very low. So the transport in our devices is expected to be mainly due to thermionic emission of the carriers.

Both graphene and GaN/AlGaN systems have unique physics and applications. But combination of these two unique systems has not been studied in details for application in electronics. The use of graphene to improve GaN/AlGaN HEMT by inserting graphene between metal and GaN/AlGaN, graphene as a contact to GaN/AlGaN system[30],transparent conductive electrode in GaN optoelectronic devices[31] and graphene as a heat spreader for the thermal management[32] of high power GaN/AlGaN system has been reported in literature. But there has been no report present according

to our knowledge in the literature where the maximum potential of both graphene and GaN/AlGaN system is utilized in the electronic applications. Recently study of transport in the graphene/AlGaN/GaN heterostructure has been present in the literature by means of conductive atomic force microscopy (CAFM) and scanning capacitance microscopy (SCM)[33] . This study mainly focused in the nature of transport between graphene and 2-DEG through AlGaN but not on application of this transport in electronics. Also but there are several differences between the structure in and the current structure under study.

- The mole fraction of Al and thickness of AlGaN in the current structure is 30% and 15 nm where in[33] it is 25% and 24 nm. At such a high thickness the nature of transport is expected to be dominated by different mechanism.
- The presence of a thin (3nm) GaN cap-layer between AlGaN and graphene in the structure under study which may affect the effective barrier height and transport in the heterojunction.
- The contact to graphene in our work is evaporated and over a uniform area. Also the contact metal stack is chosen such way which minimize the contact resistance where in [33] Au coated AFM tip is used as contact. In spite of these differences, we can analyze our heterostructure using a methodology similar to the one described in [33].

In the thermionic transport model we can express the current of a junction by

$$J_{BE} = J_{BEs} exp(\frac{qV_{BE}}{n_{BE}kT})) \tag{4.1}$$

$$J_{BEs} = RWL exp(\frac{q\phi_{BE}}{kT})) \tag{4.2}$$

Where J_{BE} is the current density through the base-emitter heterojunction, J_{BEs} is the saturation current density, V_{BE} is the applied bias across the base-emitter junction and n_{BE} is the ideality factor of the junction. The the overall junction can be

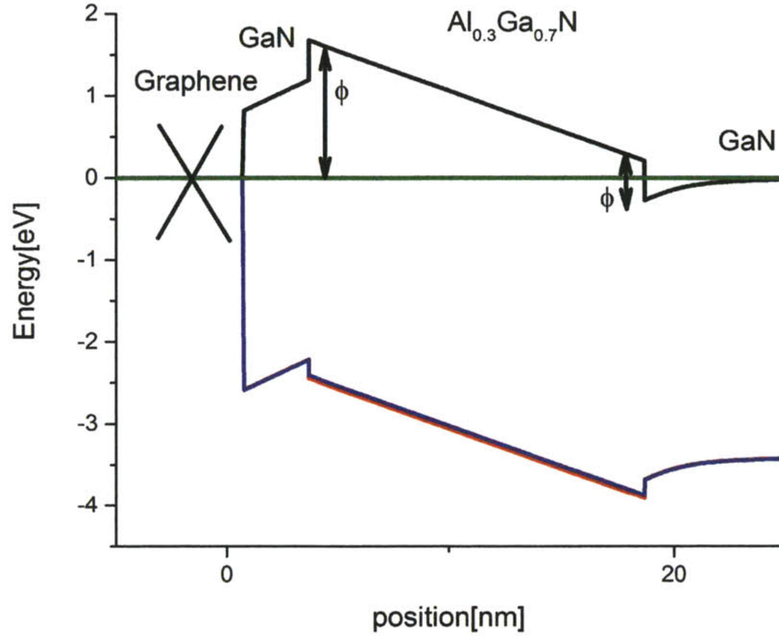


Figure 4-2: Energy band diagram of the Base-Emitter heterojunction

considered a combination of three separate heterojunction diodes (D1, D2, D3) as seen from Fig. 4-2. D1 represents the heterojunction between graphene and GaN cap-layer, D2 represents the heterojunction between GaN cap-layer -AlGaN and D3 represents AlGaN- GaN channel. But from the band diagram D1 and D2 can be considered a single diode. We can calculate the barrier height and reverse saturation current from the I-V characteristics given in Fig. 4-3

$$J_{D1eff} = J_{D1effs} exp(\frac{qV_{D1eff}}{n_{D1eff}kT}) \tag{4.3}$$

Where J_{D1effs} can be expressed as

$$J_{D1effs} = RWLexp(\frac{q\phi_{D1eff}}{kT})) \tag{4.4}$$

Here R is the effective Richardson constant, ϕ_{D1eff} is the effective barrier height of D_{1eff}, W and L are the width and length of the heterojunction area. Similarly for

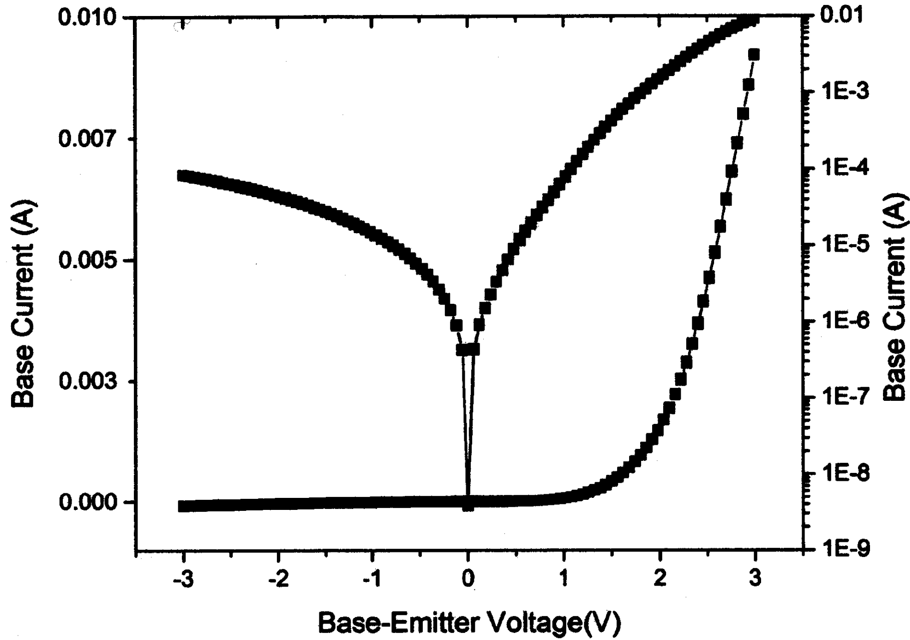


Figure 4-3: Current-voltage characteristics of base-emitter heterojunction

D3 it can be written that

$$J_{D3} = J_{D3}exp(\frac{qV_{D3}}{n_{D3}kT})) \tag{4.5}$$

Where J_{D3s} can be expressed as

$$J_{D3} = RWLexp(\frac{q\phi_{D3}}{kT})) \tag{4.6}$$

Here R is the effective Richardson constant, ϕ_{D3} is the effective barrier height of D_{1eff}, W and L are the width and length of the heterojunction area. To extract the ideality factor and reverse saturation current we can use the semi-logarithmic plot from Fig. 4-3. From the energy band diagram of Fig. 4-2, it is evident that operation of this heterojunction in the low bias regime is dominated by the D3 and in the moderate high bias regime by D_{1eff}. . By piecewise linear fitting of ln(I) vs V_{BE} ideality factor and reverse saturation current of each diode can be extracted

Table 4.1: Calculated diode parameters obtained from two terminal measurements

Diode	D_{1eff}	D_3
Slope	3.78586	8.239
Intercept	−13.42651	−14.98
Ideality factor	8.24	5.6339
Reverse saturation current	1.475510^{-6} A	3.1210^{-7} A

separately.

From the fitted line of the low bias regime in Fig 4-3 the intercept and slope can be calculated . From this value we can using equation 4.7 ,

$$slope = (\frac{e}{kT})(\frac{1}{n_{D3}}) \tag{4.7}$$

$$intercept = ln(I_{D3s}) \tag{4.8}$$

All the values obtained for both of the diodes are summarized in 4.1 Barrier height of each diode is related to the reverse saturation current by [25].

$$\phi_B = (\frac{kT}{q})ln(\frac{WLRT^2}{I_s}) \tag{4.9}$$

To find ϕ_B from the I_s the exact value of Richardson constant, R is required. For GaN a wide number of Richardson constant in available in literature (0.006-6 A/cm^2K^2). Using a representative value of 0.006 A/cm^2K^2 [26] ϕ_{D3} is found to be 0.17eV which is comparable to the reported value in[33] for $Al_{0.25}Ga_{0.75}N$ while if 6 A/cm^2K^2 is used then ϕ_{D3is} found to be 0.06eV. The correct extraction of barrier height can be done using temperature dependent measurements of the diodes. However to calculate ϕ_{D1eff} usingthis approach is not possible because of the unavailability of experimental data of Richardson constant in literature for the structure under study. Fortunately, the barrier height can also be calculated as discussed in[33] by using the energy band diagram in Fig. 4-2. The built-in potential across the

heterostructure can then be expressed by

$$\phi_{Bbi} = \phi_{D1eff} - \phi_{D3} = \frac{kT}{q}[ln(I_{D3s}) - ln(I_{D1effs})] \tag{4.10}$$

But the built-in potential across the junction can also be expressed by,

$$\phi_{Bbi} = \frac{q(\sigma - n_{2DEG})d}{\epsilon_{rAlGaN}} \tag{4.11}$$

The average σ and n_{2DEG} are found to be $7\times10^{12}cm^{-2}$ and $1.5\times10^{12}cm^{-2}$, as measured by C-V and Hall measurement respectively. For the current structure AlGaN thickness is 10 nm and ϵ_{rAlGaN} is $10.373\epsilon_0$, which gives ϕ_{Bbi}=0.947 eV. From equation 4.10 we get ϕ_{D1eff}= 1.11eV.

To analyze the transport property of the junction in more detail, the temperature dependent transport properties are measured over a wide temperature range (250K-4K) for the same devices. For any heterojunction diode dominated by thermionic emission transport can be analyzed through Richardson plot which can be derived from equations 4.1 and 4.2.

$$J_{D1eff} = J_{D1effs}exp(\frac{qV_{D1eff}}{n_{D1eff}kT}) \tag{4.12}$$

Figure 4-4 exhibits the I−V of the base-emitter heterojunction for three different temperature (250K, 150K, 4K) and the nature of transport characteristics does not change significantly over this wide temperature range.

4.1.2 Base-collector heterojunction

The base-collector heterojunction of the device is less complicated than the emitter-base heterojunction and consists of graphene-Al_2O_3(9nm)- Ti/Au. The device connection and top view of B-C heterojunction is shown in Fig. 4-5.

The heterojunction is essentially a metal-insulator-metal (MIM) diode which active area is $30\mu m \times 60\mu m$.

Although isolated graphene-Al_2O_3-Ti/Au should act like a perfect tunneling de-

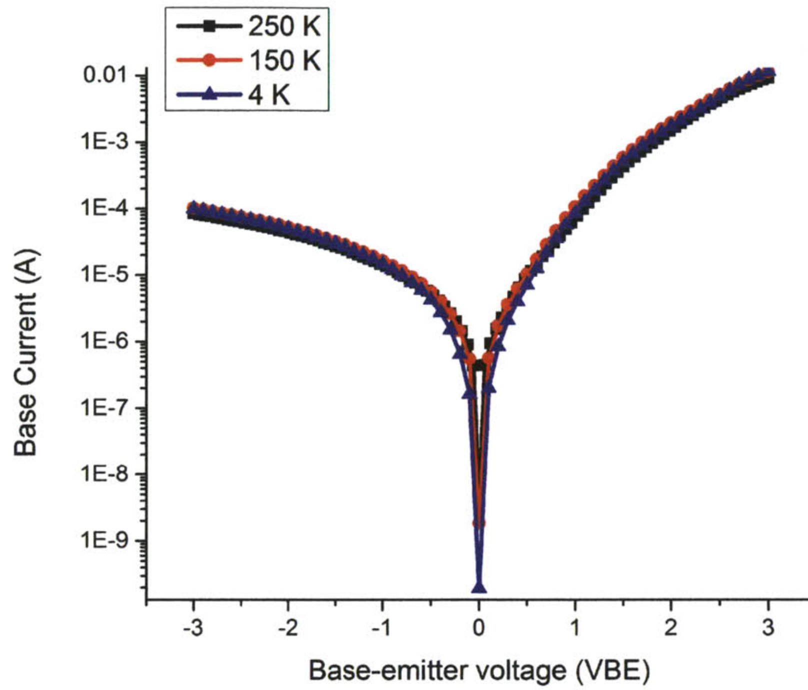


Figure 4-4: Current-voltage characteristics of Base-emitter heterojunction at three different temperatures

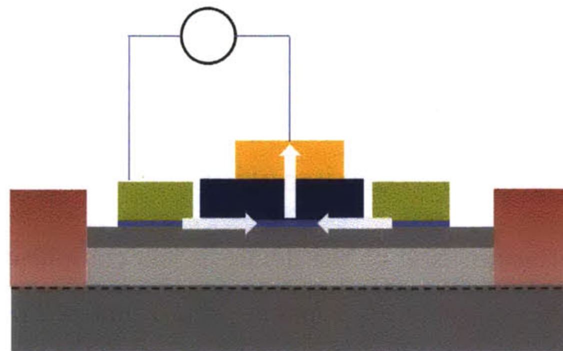


Figure 4-5: (a) Measurement connection for the characterization of Base-Collector heterojucntion

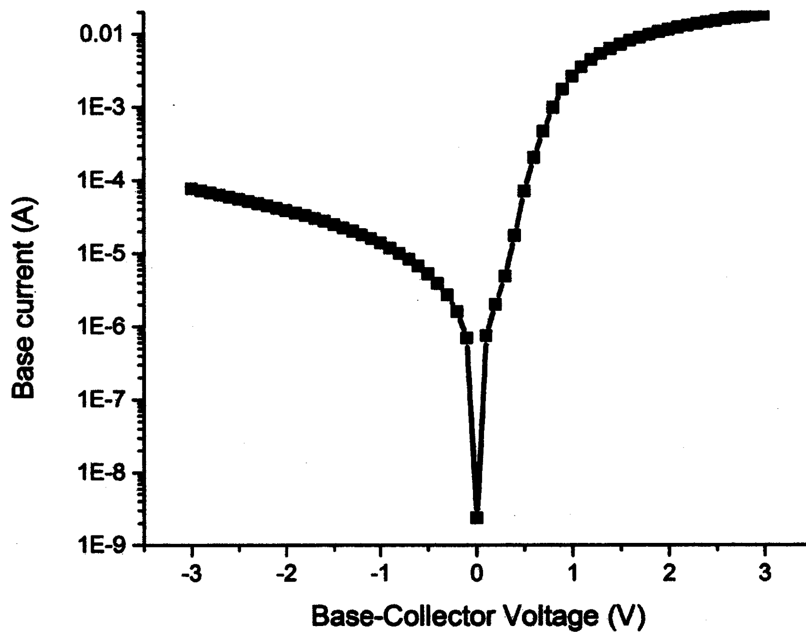


Figure 4-6: Current-Voltage characteristics of Base-Collector heterojunction

vice but in this case the oxide is too thick to assist tunneling of carrier by Fowler-Nordheim mechanism, but there might be some Pool-Franknel tunneling due to trap states in the oxides. As the thin layer Al is used as the seed for the ALD, it should accumulate a bulk charge that affects the transport through the junction. The C – B heterojunction characteristics is exhibited in Fig. 4-6.As a thin layer Al is used as the seed for the ALD, this low quality layer could accumulate bulk charge that affects the transport through the junction.

4.2 Common-emitter Characteristics

The main goal of fabricating this device is to use as amplifier in high frequency operations. With the understanding of two individual junctions, the extent of the current study can be extended to the three terminal device measurement where the performance as an amplifier can be studied. For the different applications different

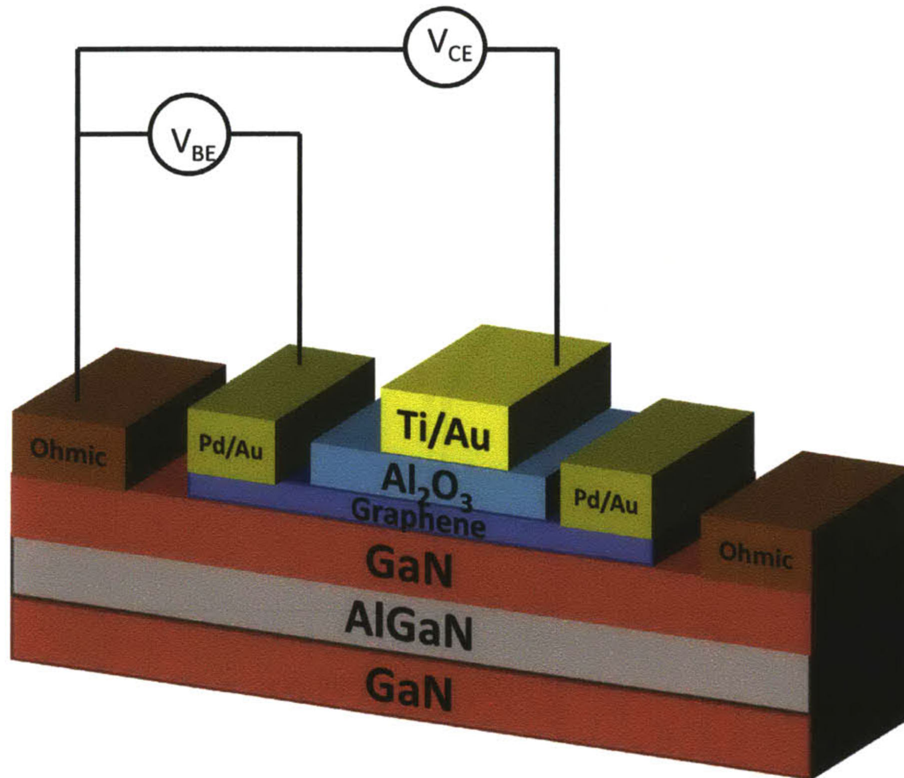


Figure 4-7: Device configuration for common-emitter characteristics measurement

biasing condition of bipolar transistor based amplifiers are used but for high gain application common-emitter configuration is most appropriate because of its inherent high gain[2]. In this configuration emitter terminal is grounded or considered as reference, and bias is applied in both base and collector terminals.

In the common-emitter configuration the emitter is grounded as shown Fig. 4-7. Collector current, I_C, is measured as a function of collector-emitter voltage, V_{CE}, for different base-emitter voltages. In the off-state condition (when V_{BE} is less than 1.5 V), there is no current through the device as the energy barrier does not favor carriers to be injected from the emitter towards the base and finally to the collector. When a large enough negative V_{BE} is applied the effective barrier height for the electrons in the 2-DEG of GaN increases and eventually there is no significant current flow. If the base-emitter voltage is gradually increased the injection from emitter towards base is increased significantly. On this way V_{BE} allows us to modulate the carrier

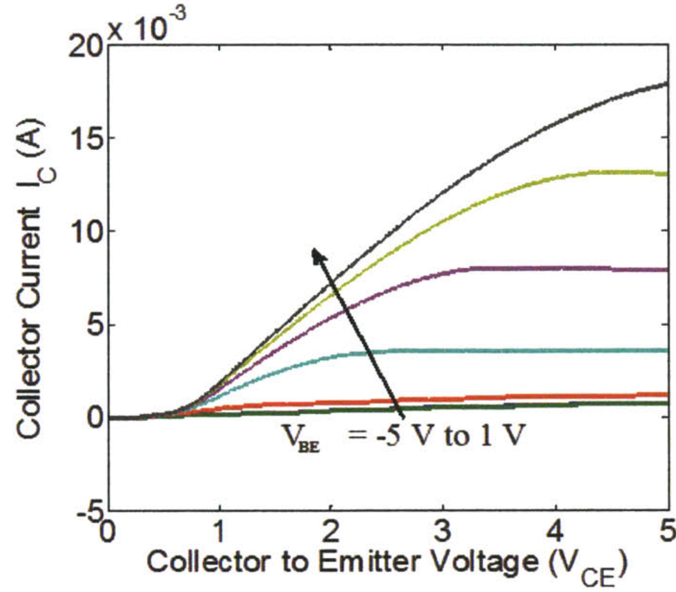


Figure 4-8: Common-Emitter characteristics for different base-emitter voltage of the device

flow between the emitter and the base. When the collector-emitter voltage, V_{CE}, is increased, it lowers the barrier between the collector and emitter. At a particular V_{BE}, increasing V_{CE} effectively results in the lowering of the barrier height and increasing the current. At low V_{CE} electrons may reach the base depending on the specific V_{BE} voltage, but if V_{CE} is not high enough, most of the electrons are backscattered and contribute to the base current, which for this unipolar device can be considered as a leakage current. However, when V_{CE} is very high then the Fermi level of the base is significantly higher than the collector and, beyond that bias,increasing V_{CE} does not increase the current rather the current begins to drop slightly. The true nature of this behavior is not fully understood from the band diagram point of view and requires further study in the future. Due to the presence of a high quality crystalline heterojunction between GaN and AlGaN, the current level of this device is much higher when compared with graphene-based HETs with an oxide tunneling barrier. The I_{ON}/I_{OFF} ratio of the proposed device is on the order of 10^2 and it depends on the quality of the filtering barrier of Al_2O_3. Improving the quality of filtering barrier can lead to higher on-off ratios as well as a better current driving capability. The current gain (α) is an important figure of merit for the device performance. This represents

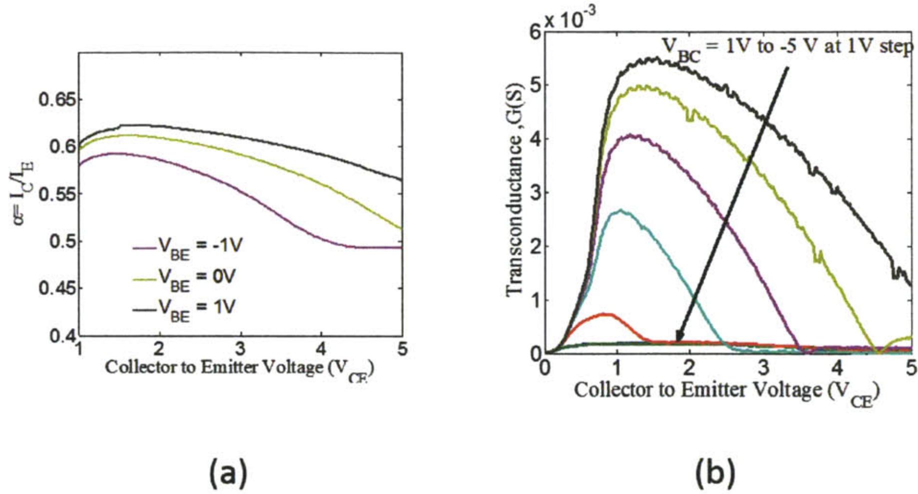


Figure 4-9: a) Transfer ratio and b) Transconductance of the GBT

the fraction of electrons injected from the emitter and successfully collected at the collector. Ideally this ratio should be close to 1 if there were no scattering and energy relaxation in the graphene base.

Fig. 4-9 shows (a) the current gain and (b) the transconductance, $G_m = \delta I_C/\delta V_{CE}$ as a function of V_{CE}. The current gain is (Fig. 4-9(b)) in the range of 0.5-0.6 in the ON state. With the increase of V_{CE} the current gain begins to drop because of current saturation. The relatively low value of α occurs because of a two-step process consisting of scattering and reflection at the filtering barrier, followed by energy relaxation in the graphene base. However, the current gain, α of our proposed device is an order of magnitude higher than the current gain reported in other graphene-based HETs[9, 10] ($10^{-2} - 10^{-4}$). To explore the underlying transport mechanism in the proposed graphene/GaN metal base transistor, the current-voltage characteristics were measured over a wide temperature range.

Fig. 4-10 exhibits the common-emitter characteristics of the device in three different temperatures in vacuum (250 K, 150 K and 4 K). From these measurements, it is clearly shown that the conduction in this device is strongly temperature dependent. As the temperature goes below room temperature the electron injection from the emitter is reduced and eventually the overall device current level is lowered, although the shape of the common-emitter characteristic remains identical. This indicates

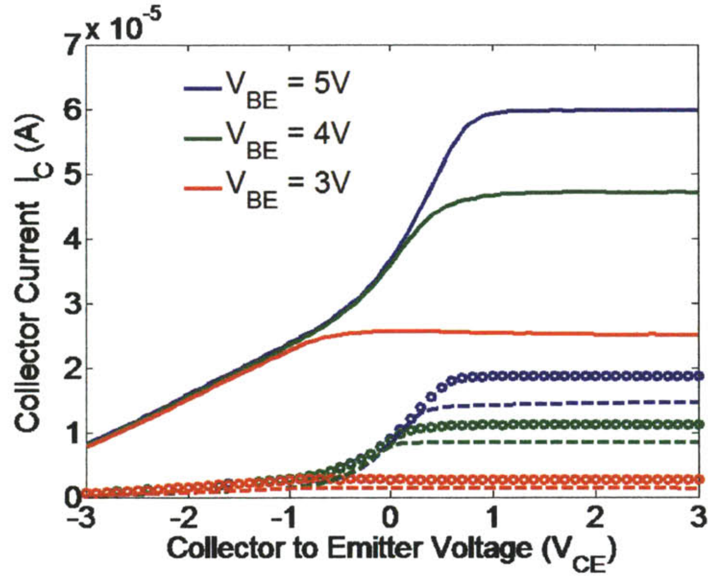


Figure 4-10: Common-emitter characteristics of fabricated device for different base-emitter voltage at three different temperatures (250 K, 150 K and 4 K). The solid lines represent characteristics at 250 K, circles represent 150 K and dashed line represent 4K characteristics.

that the conduction mechanism in this device is dominated by thermionic emission of carriers rather than by tunneling.

4.3 NanoTCAD Vides simulation

To understand the underlying physics of device operation the fabricated transistor was simulated by means of the open-source code NanoTCAD ViDES[34] , by self-consistently solving the 1D Poisson and Schrödinger equations within the Non-Equilibrium Green's Function(NEGF) formalism[?]. Fully ballistic transport and uniform energy dispersion relation was assumed in the transversal direction, so that the simulation results have to be considered as an upper bound for the actual device performance. The coupling between graphene and the GaN and between graphene and the dielectric layer were assumed to be sufficiently strong as to consider the graphene barrier completely transparent for electrons.

In Fig. 4-11(a), we show the simulated output characteristics for different V_{BE}

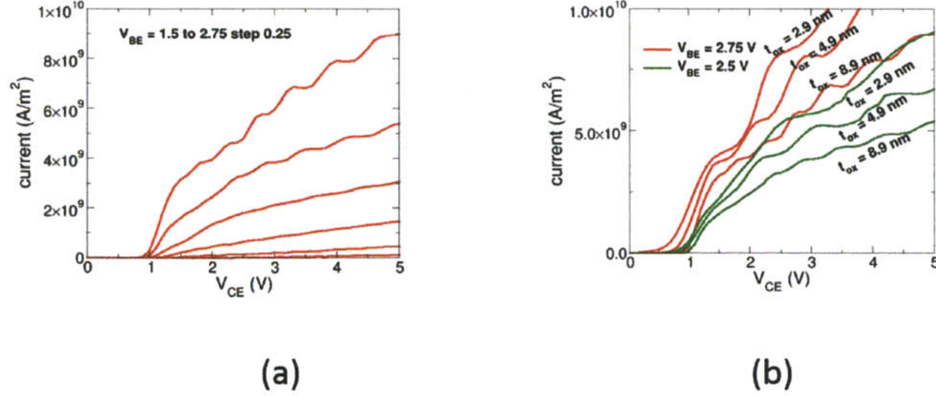


Figure 4-11: a) Simulated output characteristics for different V$_{BE}$. b) Simulated output characteristics computed for V_{BE} =2.5 and 2.75 V for different oxide thicknesses. Oscillations shown are due to quantum interference at the two interfaces of the Al_2O_3 layer, as previously observed in MOS structures, and might experimentally be smeared out by surface roughness of the Al_2O_3 layer and by electron-phonon interaction at room temperature, which broadens the energy distribution of the electrons impinging onto the Al_2O_3 layer[39] and this effect is not taken into account in our simulations.

values. As in the experimental results, I_C is negligible for V_{CE}<1 V, regardless of the applied V_{BE}. This behavior is due to the effect of the Al_2O_3 barrier, which prevents carrier flowing from the emitter to the collector for small V_{CE}. This is confirmed by simulations shown in Fig. 4-11(b), where the output characteristics for V_{BE} =2.5 and 2.75 V are shown, for different oxide thicknesses t_{ox} from 2.9 to 8.9 nm. As can be seen, the thinner the Al_2O_3 layer, the smaller the V_{CE} at which the device starts to conduct. Oscillations shown in Fig. 4-11(b) are due to quantum interference at the two interfaces of the Al_2O_3 layer, as previously observed in MOS structures, and might experimentally be smeared out by surface roughness of the Al_2O_3 layer and by electron-phonon interaction at room temperature, which broadens the energy distribution of the electrons impinging onto the Al_2O_3 layer[30] and this effect is not taken into account in our simulations.

To understand the potential of high frequency operation of the fabricated device simulated cut-off frequency is shown for different bias points for the device with 8

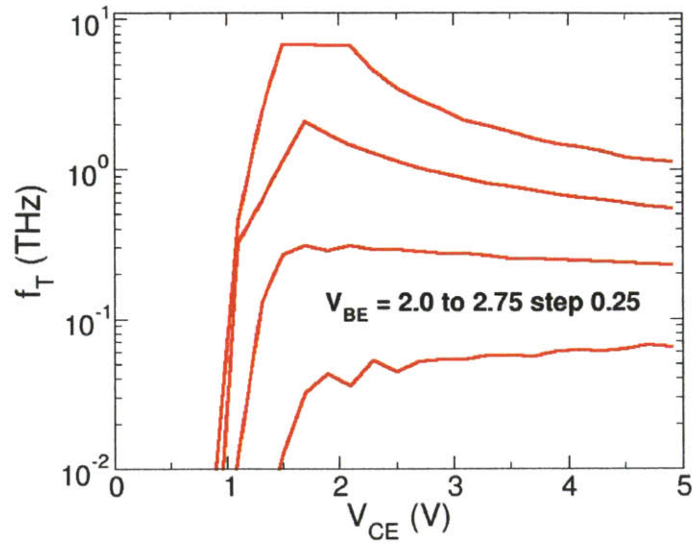


Figure 4-12: Simulated Cut-off frequency for different bias points for the device with the 8 nm Al_2O_3 barrier for different V_{BE} biases at a step of 0.25 V. The bottom curve represents the curve for V_{BE}=2.0 V.

nm Al_2O_3 barrier in Fig. 4-12. As shown by simulations, the proposed device is in principle able to operate in the THz frequency range, provided that stray capacitances and other sources of non-idealities are kept under control.

Chapter 5

Conclusion and Future Works

In summary, the work in the thesis demonstrates a graphene-based metal base transistor with a promising future in high frequency electronics. In chapter 2, a novel device structure for the graphene base transistor (GBT) was proposed towards the goal of exploiting the potentials of wide bandgap GaN and zero bandgap graphene for future THz electronics. In chapter 3, the fabrication process and challenges are presented to fabricate the novel GBT. The detail of the fabrication process flow is provided in Appendix. The DC electrical measurements and related analysis was presented in chapter 4. The base-emitter and base-collector characteristics were presented and corresponding diode parameters were extracted to understand the intrinsic device physics. With the understanding of individual diodes, common-emitter amplifier configuration for the device was studied in both room temperature and low temperature. The device is able to achieve a significantly better performance than other graphene-based hot-electron transistors demonstrated in the literature by simultaneously taking advantage of the high quality of the GaN/AlGaN heterojunction and an ultra-thin graphene base. The on-state current (mA/cm^2) of the device is greatly improved compared to similar devices on Si/SiO_2 (nA/cm^2)[24]. Also an order improvement of the injection ratio, α, is achieved in this structure. From the NanoT-CAD Vides simulation using 1st order one dimensional model ,this device shows the potential of integrating graphene layers with more conventional semiconductor materials, such as GaN, for developing new high-speed devices. This work demonstrates

first ever graphene-on-GaN GBTs which opened up the opportunity of integration of 2D materials with III-Nitrides for the application in high frequency and high power electronics. The device structure presented and studied in this thesis can be further optimized towards the goal of large scale technological implementation.

5.1 Design with a thinner AlGaN layer

In this work in the AlGaN emitter barrier layer was 10-15 nm thick. At this physical thickness carrier injection is mainly due to thermionic emission from the emitter to the base. If AlGaN thickness can be reduced it will also allow quantum mechanical tunneling and transport mechanism can be hot electron transport in which case device should operate faster than device based on thermionic emission. Also NanoTCAD Vides simulation shows that reducing the barrier thickness increases the current density of the voltage at same V_{BE}. Also at reduced AlGaN thickness shifts the threshold voltage of the device towards the negative voltages which means device will require lower turn-on voltage and similar current level can be achieved at smaller bias level.

5.2 Design with InAlN layer

As shown previously, reduction of emitter barrier thickness improves the device performance but AlGaN has an inherent limitation in terms of thinness. Thinning down the AlGaN thickness reduces the 2-DEG charge density as shown in Fig. 5-1 (b). For example, a reduction of AlGaN thickness from 15 nm to 10 nm reduces the 2-DEG density to half. Also if the AlGaN thickness is less than 5-6 nm, there is no significant 2-DEG formed in case of AlGaN. To solve this problem AlGaN can be replaced with another high bandgap III-Nitride which has higher polarization field. InAlN with Al composition of 17% is lattice matched with GaN as seen from Fig. 5-1 (a). Also, for the same thickness, InAlN has higher 2-DEG concentration compared with AlGaN and most importantly the critical thickness of InAlN to have significant 2-DEG density is lower than AlGaN as can be seen in Fig. 5-1(b). An InAlN with 17% Al has a

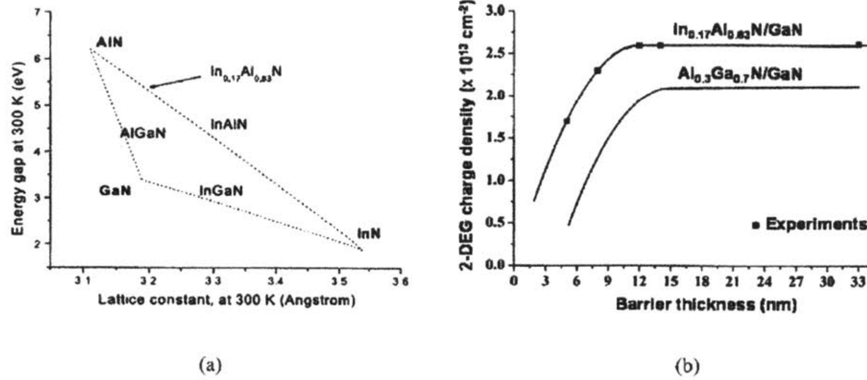


Figure 5-1: (a) Comparison of lattice constant and energy gap between $In_{0.17}Al0.83N$ and other nitride alloys. (b) Comparison of simulated 2-DEG sheet charge density between InAlN/GaN and AlGaN/GaN heterostructure[40]

2-DEG density of $10^{13}cm-2$ [40] for a thickness of 3 nm. Therefore, it is expected InAlN can improve the device performance in graphene-on-GaN GBTs.

5.3 Design with hBN

The performance of the device demonstrated in this work is limited by the transfer ratio 0.5-0.6. This low transfer ratio arises mainly due to the base-collector barrier which is made of a low quality oxide. It is expected that the use of a 2 dimensional material at the base-collector interface will significantly improve the device performance. As an alternative to the Al_2O_3 oxide used so far, we would like to propose the use of hexagonal Boron Nitride (hBN), which is an excellent 2D material [41][43]. However, the lack of large area high quality CVD grown hBN limits possibility of wafer scale fabrication of graphene-on-GaN GBTs at this time. The use of large area CVD-grown MoS_2, another 2D dielectric, can be another option as it has been used in other device applications[44][46].

5.4 GaN Collector

From the quantum mechanical point of view the transfer ratio is mostly affected by the quantum mechanical reflection at the base-collector interface. To overcome this limi-

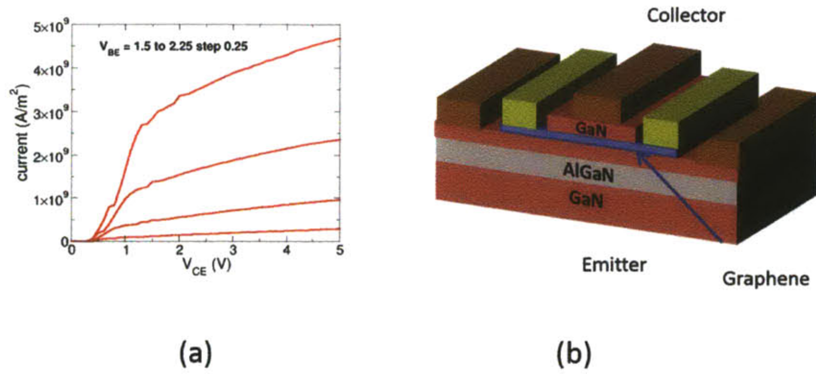


Figure 5-2: Simulated common-emitter characteristics of GBT with GaN collector

tation an alternative structure as shown Fig. 5-2 can be used where top Al_2O_3/Ti/Au stack is replaced by a GaN layer. The performance of the device is simulated using NanoTCAD Vides as shown in Fig.5-2. The device with GaN collector can provide higher on-current and lower threshold voltage compared to the current structure. But technological implementation of such structure still remains challenging.

Bibliography

[1] Max C. Lemme. Current Status of Graphene Transistors. *Solid State Phenomena*, 156-158:11, November 2009.

[2] Umesh Kumar Mishra and Jasprit Singh. *Semiconductor device physics and design*, volume 189. Springer, 2008.

[3] N Balkan. Hot electrons in semiconductors. *Physics and Devices*, page 528, 1998.

[4] E Rosencher, PA Badoz, JC Pfister, F Arnaud dâĂŹAvitaya, G Vincent, and S Delage. Study of ballistic transport in si-cosi2-si metal base transistors. *Applied physics letters*, 49(5):271–273, 1986.

[5] M. S. Shur, A. D. Bykhovski, R. Gaska, M. Asif Khan, and J. W. Yang. âĂIJalgan–GaN–AlInGaN induced base transistor. *âĂİ Appl. Phys*, 76:3298âĂŞ3300, 2000.

[6] S. Dasgupta and A. Raman. âĂIJexperimental demonstration of III-nitride hot-electron transistor with GaN base, âĂİ IEEE electron device lett. 32(9):1212âĂŞ1214, 2011.

[7] H. Yang, J. Heo, S. Park, H. J. Song, D. H. Seo, K.-E. Byun, P. Kim, I. Yoo, H.-J. Chung, and K. Kim. Graphene Barristor, a Triode Device with a Gate-Controlled Schottky Barrier, 2012.

[8] Wolfgang Mehr, Jarek Dabrowski, J. Christoph Scheytt, Gunther Lippert, Ya-Hong Xie, Max C. Lemme, Mikael Ostling, and Grzegorz Lupina. Vertical Graphene Base Transistor, 2012.

[9] Sam Vaziri, Grzegorz Lupina, Christoph Henkel, and AD Smith. A graphene-based hot electron transistor. *Nano letters*, 13(4):1435–9, March 2013.

[10] Caifu Zeng, Emil B. Song, Minsheng Wang, Sejoon Lee, Carlos M. Torres, Jianshi Tang, Bruce H. Weiller, and Kang L. Wang. Vertical graphene-base hot-electron transistor. *Nano Letters*, 13:2370–2375, 2013.

[11] K S Novoselov, A K Geim, S V Morozov, D Jiang, Y Zhang, S V Dubonos, I V Grigorieva, and A A Firsov. Electric field effect in atomically thin carbon films. *Science (New York, N.Y.)*, 306(5696):666–9, October 2004.

[12] Joel Moser, Amelia Barreiro, and Adrian Bachtold. Current-induced cleaning of graphene. *Applied Physics Letters*, 91(16):163513, 2007.

[13] Lei Liao, Yung-Chen Lin, Mingqiang Bao, Rui Cheng, Jingwei Bai, Yuan Liu, Yongquan Qu, Kang L Wang, Yu Huang, and Xiangfeng Duan. High-speed graphene transistors with a self-aligned nanowire gate. *Nature*, 467(7313):305–8, September 2010.

[14] J.B. Gunn. Microwave oscillations of current in III-V semiconductors, 1993.

[15] Chenming Hu, Simon C Tam, Fu-Chieh Hsu, P-K Ko, T-Y Chan, and Kyle W Terrill. Hot-electron-induced mosfet degradationâĂŤmodel, monitor, and improvement. *Electron Devices, IEEE Transactions on*, 32(2):375–385, 1985.

[16] C. a. Mead. Operation of Tunnel-Emission Devices. *Journal of Applied Physics*, 32:646, 1961.

[17] DV Geppert. The metal-base transistor. *Electron Devices, IRE Transactions on*, 9(6):507–507, 1962.

[18] MM Atalla and RW Soshea. Hot-carrier triodes with thin-film metal base. *Solid-State Electronics*, 6(3):245–250, 1963.

[19] P. Kozodoy, S. Keller, and S.. Denbaars, and u. *Mishra, âĂIJMOVPE growth and characterization of Mg-doped GaN, âĂİ Journal of Crystal Growth*, 195:265âĂŞ269, 1998.

[20] Thanasis Georgiou, Rashid Jalil, Branson D Belle, Liam Britnell, Roman V Gorbachev, Sergey V Morozov, Yong-Jin Kim, Ali Gholinia, Sarah J Haigh, Oleg Makarovsky, et al. Vertical field-effect transistor based on graphene-ws2 heterostructures for flexible and transparent electronics. *Nature nanotechnology*, 8(2):100–103, 2013.

[21] F. Driussi, P. Palestri, and L. Selmi. Modeling, simulation and design of the vertical Graphene Base Transistor. *Microelectronic Engineering*, 109:338–341, 2013.

[22] VD Di Lecce, Roberto Grassi, Antonio Gnudi, and Elena Gnani. Graphene-Base Heterojunction Transistor: An Attractive Device for Terahertz Operation. *IEEE TRANSACTIONS ON ELECTRON DEVICES*, 60:4263–4268, 2013.

[23] Valerio Di Lecce, Roberto Grassi, Antonio Gnudi, and Elena Gnani. Graphene Base Transistors: A Simulation Study of DC and Small-Signal Operation. pages 1–8, 2013.

[24] Masakazu Kanechika, Masahiro Sugimoto, Narumasa Soejima, Hiroyuki Ueda, Osamu Ishiguro, Masahito Kodama, Eiko Hayashi, Kenji Itoh, Tsutomu Uesugi, and Tetsu Kachi. A Vertical Insulated Gate AlGaN/GaN Heterojunction Field-Effect Transistor . 46:L503–L505, 2007.

[25] J Kuzm k. InAlN/(In)GaN high electron mobility transistors: some aspects of the quantum well heterostructure proposal. *Semiconductor Science and Technology*, 17(6):540–544, June 2002.

[26] Sam Vaziri, Grzegorz Lupina, Christoph Henkel, AD Smith, Mikael Ostling, Jarek Dabrowski, Gunther Lippert, Wolfgang Mehr, and M.C. Lemme. A Graphene-Based Hot Electron Transistor. *Nano letters*, 13(4):1435–1439, 2013.

[27] Sansaptak Dasgupta and Ajay Raman. Experimental Demonstration of III-Nitride Hot-Electron Transistor With GaN Base. *IEEE Electron Device Letters*, 32(9):1212–1214, 2011.

[28] Allen Hsu, Han Wang, Ki Kang Kim, Jing Kong, and Tomas Palacios. Impact of Graphene Interface Quality on Contact Resistance and RF Device Performance. *IEEE Electron Device Letters*, 32:1008–1010, 2011.

[29] FJ Kub. Transistor having graphene base. *US Patent App. 13/238,728*, 1(19), 2011.

[30] Pil Sung Park, Kongara M Reddy, Digbijoy N Nath, Zhichao Yang, Nitin P Padture, and Siddharth Rajan. Ohmic contact formation between metal and algan/gan heterostructure via graphene insertion. *Applied Physics Letters*, 102(15):153501, 2013.

[31] S Tongay, M Lemaitre, X Miao, B Gila, BR Appleton, and AF Hebard. Rectification at graphene-semiconductor interfaces: zero-gap semiconductor-based diodes. *Physical Review X*, 2(1):011002, 2012.

[32] Zhong Yan, Guanxiong Liu, Javed M Khan, and Alexander A Balandin. Graphene quilts for thermal management of high-power gan transistors. *Nature communications*, 3:827, 2012.

[33] Gabriele Fisichella, Giuseppe Greco, Fabrizio Roccaforte, and Filippo Giannazzo. Current transport in graphene/AlGaN/GaN vertical heterostructures probed at nanoscale. *Nanoscale*, 6(15):8671–80, July 2014.

[34] Gianluca Fiori and Giuseppe Iannaccone. Multiscale modeling for graphene-based nanoscale transistors. *Proceedings of the IEEE*, 101(7):1653–1669, 2013.

[38] S. Datta, "Nanoscale device modeling: the Green's function method," *Superlattices Microstruct.*, vol. 28, pp. 253–278, 2000.

[39] G. Lewicki and J. Maserjian, "Oscillations in MOS tunneling," *J. Appl. Phys.*, vol. 46, no. 7, p. 3032, 1975.

[40] D. S. Lee, "Deeply-scaled GaN high electron mobility transistors for RF applications." Massachusetts Institute of Technology, 2014.

[41] H. Wang, T. Taychatanapat, A. Hsu, K. Watanabe, T. Taniguchi, P. Jarillo-Herrero, and T. Palacios, "BN/Graphene/BN Transistors for RF Applications," *IEEE Electron Device Lett.*, vol. 32, no. 9, pp. 1209–1211, Sep. 2011.

[42] M. P. Levendorf, C.-J. Kim, L. Brown, P. Y. Huang, R. W. Havener, D. A. Muller, and J. Park, "Graphene and boron nitride lateral heterostructures for atomically thin circuitry.," *Nature*, vol. 488, no. 7413, pp. 627–32, Aug. 2012.

[43] L. Britnell, R. V Gorbachev, R. Jalil, B. D. Belle, F. Schedin, M. I. Katsnelson, L. Eaves, S. V Morozov, A. S. Mayorov, N. M. R. Peres, A. H. C. Neto, J. Leist, A. K. Geim, L. A. Ponomarenko, and K. S. Novoselov, "Electron tunneling through ultrathin boron nitride crystalline barriers.," *Nano Lett.*, vol. 12, no. 3, pp. 1707–10, Mar. 2012.

[44] H. Wang, L. Yu, Y.-H. Lee, Y. Shi, A. Hsu, M. L. Chin, L.-J. Li, M. Dubey, J. Kong, and T. Palacios, "Integrated circuits based on bilayer MoS_2 transistors.," *Nano Lett.*, vol. 12, no. 9, pp. 4674–80, Sep. 2012.

[45] S. Bertolazzi, D. Krasnozhon, and A. Kis, "Nonvolatile memory cells based on MoS2/graphene heterostructures," *ACS Nano*, vol. 7, pp. 3246–3252, 2013.

[46] G. H. Lee, Y. J. Yu, X. Cui, N. Petrone, C. H. Lee, M. S. Choi, D. Y. Lee, C. Lee, W. J. Yoo, K. Watanabe, T. Taniguchi, C. Nuckolls, P. Kim, and J. Hone, "Flexible and transparent MoS2 field-effect transistors on hexagonal boron nitride-graphene heterostructures," *ACS Nano*, vol. 7, pp. 7931–7936, 2013.

Appendix

Detailed PROCESS FLOW for Graphene/GaN vertical Transistor

Process and process number	Process steps	Tool
1) Wafer cleaning	Wash with Acetone from squirt bottle	Photo-wet-r
	Wash with Isopropanol from squirt bottle	Photo-wet-r
	Wash with DI water	Photo-wet-r
	Bake hotplate 5 min at 130C in order to dehydrate sample	Hot plate
	3 min cool down	
2) Ohmic contacts lithography	HMDS #5 (Note: HMDS is not necessary if you are not going to dip in BOE)	HMDS
	Resist coat (AZ 5214). Dispense AZ 5214 in Al tray. Use pipet to put resist on stationary resist. Then Spread at 750 rpm for 2 s Spin at 3000 rpm for 30s	Coater
	Bake at Hotplate 2 or Hotplate 300 at 80C for 5 min. This step cures the resist by evaporating the solvent away.	Hot plate
	Exposure for 8 sec. The exposure mode is low vacuum contact. The vacuum pressure should be -11psi. See Error! Reference source not found. **for more information**	**MA-6**
	Post Exposure Bake. **Hotplate 2 at 105C, Hotplate 300 at 110 C for 1 min**. Note: Hotplate 2 is 5 C hotter than Hotplate 300, which is why the temperatures are different	Hot plate

	Flood exposure for 80 s. No clear mask required	**MA-6**
	Develop in AZ 422 for 2 min. Make sure to agitate sample.	Photo-wet-r
	DI-H2O rinse 1 min	Photo-wet-r
	Dry off with N2 gun	Photo-wet-r
	Inspect in fluoroscope. In the fluoroscope, all organic materials appear as red. Therefore, the pattern should look black (all the resist is gone). **Note: If you are having a hard time with the contrast, the lamp might need to be replaced. Contact Dave Terry**	Fluoroscope
	Once the fluoroscope inspection looks good, inspect under an optical microscope. Basically, if you can see colored fringes where the resist was supposed to be gone, then you still have resist. There have been cases where the sample looked OK in the fluoroscope but there was this residue in the sample	**Optical Microscope**
	Descum for 5 min at **1000 W**. The descum will create a thin layer of Ga2O3, which will be stripped away in the oxide strip.	AsherTRL
3) Oxide strip	DI-H2O dip 1 min	Acid-hood
	HCl: H2O (1:3) 1 min. When transferring the sample from the water to the acid, make sure that the sample still have water on top. This will allow for the acid to wet the surface.	Acid-hood
	DI-H2O dip 1 min	Acid-hood
4) Evaporation	The sample should be placed in vacuum as soon as possible after the oxide strip so please time yourself accordingly Ti (200A)/ Al (1000A) / Ni (250A) /Au (500A) For the EbeamFP, set the rotation speed to 0 rpm in order to ensure an easier liftoff. Monitor deposition power levels as described	EbeamAu or EbeamFP

	in **Error! Reference source not found.**. Don't forget to set rotation speed to 15 after use.	
5) Lift off	**Place in Acetone. You can leave it overnight but you can also use a pipet to squirt away the metal film while the sample is in acetone within 5 min of putting it in acetone. Be sure to label your beaker if you will leave it overnight**	Photo-wet-Au
	After the liftoff wait, use a pipet in order to squirt away as much of the metal as possible. Then, place the sample in a **new** beaker with acetone and agitate for 1-2 min at power level 3 in the ultrasonic bath	Photo-wet-Au
	Agitate in isopropanol for 2 min at power level 3 in ultrasonic bath	Photo-wet-Au
	Rinse in DI water and dry off with N2 gun	Photo-wet-Au
6) RTA	The RTA recipe is called GaN870. First, run the recipe w/o your sample in order to make sure that the tool is working correctly. Then, open the chamber and place sample. Wait for 5 min in order to ensure a pure N2 atmosphere. Then, execute GaN870: Ramp in 40 s to 800C Hold 7s Ramp 870C Hold 30s (870C) Cool down 3m40s Wait until the temperature is below 100C before opening. This is to ensure that the sample does not react with oxygen present in the room	Rta35 RTA-pieces
7) Wafer cleaning	Wash with Acetone from squirt bottle	Photo-wet-r
	Wash with Isopropanol from squirt bottle	Photo-wet-r
	Wash with DI water	Photo-wet-r

	Bake hotplate 5 min at 130C in order to dehydrate sample	Hot plate
	3 min cool down	
8) Lithography for Mesa isolation	Spin on OCG 825 with the following settings. Static dispense with pipet Spread for 2 sec at 750 rpm Spin for 30 sec at 3000 rpm	Coater
	Bake at Hotplate 2 or Hotplate 300 at 80C for 5 min. This step cures the resist by evaporating the solvent away.	Hot plate2 or Hotplate 300
	Exposure for 9 sec. Use low vac mode but hard contact also works	Ksaligner2
	Develop in OCG 934 (1:1). The resist develops away in 30s – 1 min	Photo-wet-r
	DI-H2O rinse 1 min	Photo-wet-r
9) Mesa etch	**Run ETCHCLN.RCP for 10 min w/o sample in order to clean the chamber. Your ECR reflected power should not exceed 5W** **Then run GANETCH.RCP w/o sample in order to prepare the chamber. The reflected power should not exceed 1 W**	PlasmaQuest SAMCO
	Run GANETCH.RCP with the sample. Here is the recipe for GANETCH.RCP. Chuck temperature is 15 C (change on chiller). step 1: BCL3 10sccm / 10mtorr / 30s Step 2: BCL3 10sccm / 10mtorr / ECR = 50W/ RF = 15 W/ 5 s step 3: BCL3 10sccm / 10mtorr / ECR=100W / RF=15W / 60s step 4: BCL3 20sccm / CL2 5sccm / 10mtorr / 30s step 5: BCL3 20sccm / CL2 5sccm / 10mtorr / ECR=50W / RF=15W / 5s **step 6: BCL3 20sccm / CL2 5sccm / 10mtorr / ECR=100W / RF=15W / 400s for around 150 nm etch.** **We changed from 600s to 400s because the 600s etch was hardening the photoresist and making it very difficult to remove.**	PlasmaQuest SAMCO

	As described in Error! Reference source not found.**, it is important to track the DC bias.**	
10) Wafer cleaning after mesa	Acetone with ultrasonic 5 min at power level 3-5. Glass beakers are more effective It is important to make sure that the sample is agitated (i.e. does not just sit in a corner) in order to get rid of the resist	Photo-wet-Au
	Isopropanol with ultrasonic 2 min at power level 3	Photo-wet-Au
	Running DI-H2O 3 min	Photo-wet-r
	Optional: 5-10 min descum in the asher at a 1000W. This ensures that all the photo-resist is gone. This is very important if your sample is going to go through a second anneal step of some sort.	**Asher**
11) Graphene Growth	LPCVD on Metal Catalyst @ 1000C Hydrogen/Methane	Jing Kong Furnace
12)	Spin PMMA 4% Anisole - 2500 rpm – 60 s 8% Anisole – 2500 rpm – 60 s Bake 130 C – Hotplate – 5 min	Jing Kong 's lab PMMA Coater
13) Catalyst Etch	Cu Etchant – 30 min HCl:DiH2O (1:4) – 30 min DiH2O – 30 min	Jing Kong 's lab Acid Hood
14) Substrate Transfer	Place PMMA graphene film on GaN Wafer	Jing Kong 's lab
15) PMMA Removal	Acetone Vapor @ 90 C for 20 minutes Anneal at 350C in forming gas for 3-6hs to remove the residues	Jing Kong 's lab Solvent Hood
16) Ohmic Contact lithography	Using same process as described in step 2.	

17) ALD dielectric layer	Clean wafer as described in the first cleaning step	ICL-Cambridge nanotech ALD
	Put an empty wafer in the chuck as the substrate for real sample. Atomic Layer Deposition(ALD) at 170C for 250 cycles. Take out the sample. ALD of 15nm Al2O3 in the empty chamber using standard recipe	
18) Lithography for Gate contact	Clean wafer as described in the first cleaning step	HMDS
	Resist coat (AZ 5214). Dispense AZ 5214 in Al tray. Use pipet to put resist on stationary resist. Then Spread at 750 rpm for 2 s Spin at **4000** rpm for 30s. (Note: Omair has also got gate lithography to work with 3000 rpm)	Coater
	Bake at Hotplate 2 or Hotplate 300 at 80C for 5 min. This step cures the resist by evaporating the solvent away.	Hot plate
	Exposure for 8 sec. The exposure mode is low vacuum contact. The vacuum pressure should be -11psi. and the WEC should be 0.05 bar. See Error! Reference source not found. **for more information about alignment**	MA-6
	Post Exposure Bake. Hotplate 2 at 105C, Hotplate 300 at 110 C for 2 min. Note: Hotplate 2 is 5 C hotter than Hotplate 300, which is why the temperatures are different. This bake time is VERY critical to get reproducible results so try to use the same hotplate consistently.	Hot plate

	Flood exposure for 80s. No clear mask necessary.	**MA-6**
	Develop in AZ 422 for 2 min. Make sure to agitate sample. Agitation is also VERY important to get good gate lithography	Photo-wet-r
	DI-H2O rinse 1 min	Photo-wet-r
	Inspect in fluoroscope. In the fluoroscope, all organic materials appear as red. Therefore, the pattern should look black (all the resist is gone)	Fluoroscope
	Once the fluoroscope inspection looks good, inspect under an optical microscope. Basically, if you can see colored fringes where the resist was supposed to be gone, then you still have resist. There have been cases where the sample looked OK in the fluoroscope but there was this residue in the sample	**Optical Microscope**
	Descum for 5 min at 1000 W. The descum will create a thin layer of Ga2O3, which helps reduce the gate leakage.	AsherTRL
19) Evaporation of gate metals	The sample should be placed in vacuum as soon as possible after the asher in order to prevent contamination in the gate contact Ni (300A)/Au(2000A)/Ni(500A) For the EbeamFP, set the rotation speed to 0 rpm in order to ensure an easier liftoff. **See** Error! Reference source not found. **for more information about deposition power**	EbeamAu or EbeamFP
20) Lift off of gate metal	**Place in Acetone. You can leave it overnight but you can also use a pipet to squirt away the metal film while the sample is in acetone within 5 min of putting it in acetone. Be sure to label your beaker if you will leave it overnight**	Photo-wet-Au
	After the liftoff wait, use a pipet in order to squirt away as much of the metal as possible. Then, place the sample in a **new** beaker with	Photo-wet-Au

	acetone and agitate for 1-2 min at power level 3 in the ultrasonic bath	
	Agitate in isopropanol for 2 min at power level 3 in ultrasonic bath	Photo-wet-Au
	Rinse in DI water and dry off with N2 gun	Photo-wet-Au