

FlexTrate

A Biocompatible Flexible Electronics Platform for High Performance Applications using Fan-Out Wafer-level Packaging

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Abstract—A novel mechanically flexible platform based on fan-out wafer-level packaging (FOWLP) is demonstrated. FlexTrate enables heterogeneous integration of high performance dies in a flexible and biocompatible elastomeric package. We demonstrate two applications: 1) a foldable seven segment display that is bendable to 1 mm radius for more than 1000 cycles, and 2) a near field wireless implantable optogenetic system that is bendable to 5mm bending radius.

I. INTRODUCTION

Commercially available wearable applications typically rely on integration of packaged chips mounted on rigid-flex printed circuit board (PCB) that are partially bendable[1]. The other approach for achieving higher flexibility needed for wearable electronics is the Flexible Hybrid Electronics (FHE) approach, which relies on integration of ultra-thin Si dies ($\leq 50 \mu\text{m}$ thicknesses) on a flexible organic substrate using printed interconnects to achieve higher flexibility compared to flex-rigid PCBs, as shown schematically in Fig. 1 (a)[2]. However, this approach has three major limitations. Firstly, it is dependent on achieving high yield after: i) wafer thinning and die singulation from bulk inorganic substrates and ii) die handling of potentially warped ultra-thin dies during flip chip bonding [3]. Secondly, conventional FHE does not support high number of I/Os needed for high performance logic and memory dies due to coarse interconnect pitch of printed nanoparticle based conductors [4]. Thirdly, as thinned dies are bent to smaller bending radii, the mechanical bending induced strain can lead in performance degradation of high performance CMOS dies [5]. This is why our approach of integrating FHE relies on embedding mechanically rigid dies in a soft elastomeric molding compound and interconnecting them using Fan-Out Wafer-Level Packaging (FOWLP), which is illustrated schematically in Fig. 1(b). We call this FOWLP based platform: FlexTrate. The bendability of FlexTrate package is similar to the way a bicycle chain bends, which consists of both hard and soft segments that allow for bending. We use soft Polydimethylsiloxanes (PDMS) as the molding compound, which has sufficient flexibility to allow for use of rigid small sized (1-5 mm²) “dielets” without compromising the flexibility of the overall system or inducing stress in the integrated Si dielets even when bent to small bending radii [6].

FlexTrate approach also allows for scaled fine pitch interconnects ($\leq 40 \mu\text{m}$) using a wafer-level electroplating

process, which can allow for on-chip like communication between neighboring dielets as the interconnect pitch approaches that of the back end of the line (BEOL) fat wire level. To sum up, in the flexibility of overall package can be optimized as a function of dielet size, inter-dielet spacing. An important implication of this approach is that FlexTrate allows for heterogeneous integration of high-performance dies, using a high performance electroplated Cu interconnect system similar to that used in rigid FOWLP used extensively in smart portable devices and allows us to pack significant processing power in truly flexible, low form factor, biocompatible, and implantable packages.

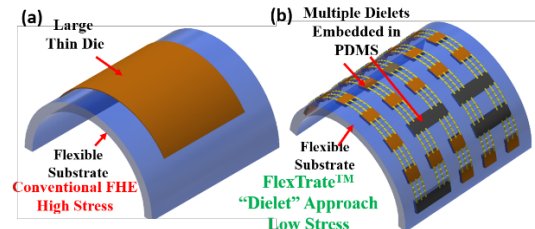


Fig. 1. (a) Schematic of a single large thin die bonded on flexible substrate in conventional FHE approach, where the die undergoes high stress upon bending to small bending radius (2 mm). (b) schematic of “dielet” approach in FlexTrate, showing multiple Si dielets connected at fine interconnect pitch.

II. PROCESS FLOW

Fig. 2 shows the schematic of the FlexTrate process integration scheme. FlexTrate follows the die-first Fan-out Wafer-level Packaging scheme practiced for rigid electronics with a few important differences:

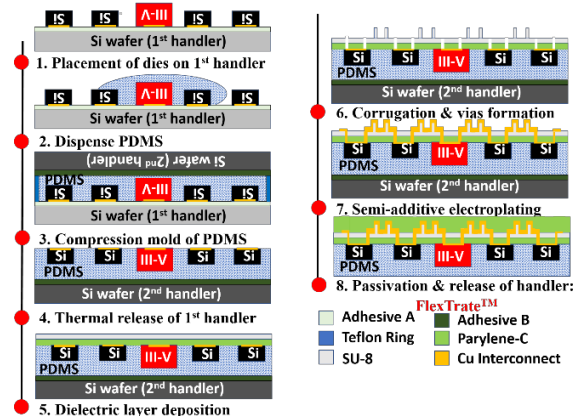


Fig. 2. Schematic of the FlexTrate Process

(1) the molding compound used here is a low glass transition temperature elastomeric flexible molding compound (Silastic MDX4-4210 (Dow)) rather than a rigid one. (2) the maximum temperature used in the process is below 200C, and (3) the wiring that connects the heterogenous dies is corrugated to avoid any strain induced buckling and allow for extreme bendability and stretching [6]. We have shown up to two levels of wiring at less than 40 μm pitch. This includes the vias that connect to the dielets. This pitch is limited by so-called die shift that occurs during the processing of the assembly as the PDMS cures. By precision placement of the dies on the first adhesive, lowering the thickness of the adhesives used, and limiting the curing temperatures, we have been able to reduce the die-shift to below 6 μm [6]. This allows the inter-die connection pitch to be reduced to below 18 μm and when combined with adaptive lithography that is being developed, can be reduced even further to below 10 μm . The integrated structure is passivated with Parylene C and has been able to withstand both saline immersion tests and repeated bending cycling at <5mm bending radius for over 3000 bending cycles.

III. APPLICATIONS

Using the process integration scheme described we have demonstrated several prototypical applications that showcase the capability of the FlexTrate integration scheme:

(a) Fig. 3 shows the integration of a 10 \times 20 array of 1mm \times 1mm dies on FlexTrate that are interconnected at 40 μm pitch. We were able achieve complete die transfer and 100% yield over an area of 37mm \times 17mm and maintain connectivity after 6000 bending cycles.

(b) We integrated 42 commercially available 335 μm thick, 1 mm², InGaN blue/green LEDs on FlexTrate to demonstrate a 7-segment foldable display, as shown in Fig. 4. Full functionality under repeated extreme bending was demonstrated with no degradation of LED characteristics.

(c) We have also successfully integrated an optogenetic implant assembly powered by wireless power transfer, which is based on eight heterogeneous dies connected at 40 μm interconnect pitch along with the optimized implant coil, as shown in Fig. 5. The system functions successfully at different bending radii. The optogenetic μLED has excellent luminescence even at 5mm bending radius.

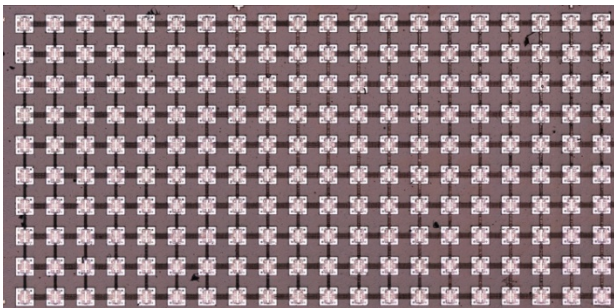


Fig. 3. Integration of 200 interconnected dies on FlexTrate

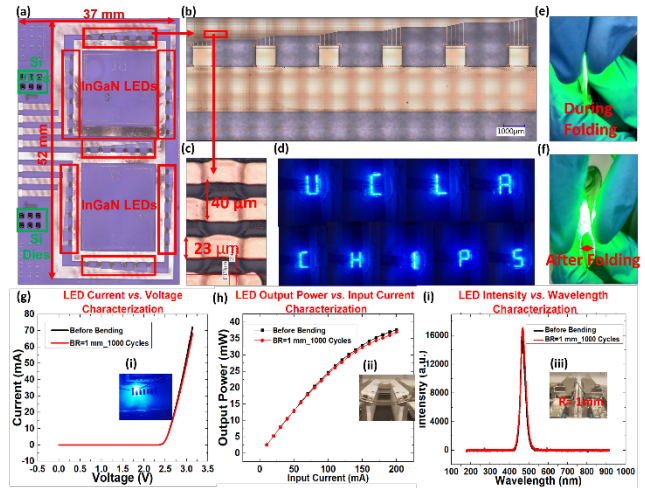


Fig. 4. (a) Foldable display with 42 LEDs on FlexTrate in the form of 7-segment display along with embedded Si dielets for accurate alignment purpose demonstrating a truly heterogeneous integration, (b) zoomed in image of a segment of the 7-segment display consisting of six LEDs, (c) 40 μm pitch “corrugated” interconnects, and (d) programming of 7-segment display to display “UCLA CHIPS”, as an example, on the foldable display. Image if foldable display (e) during folding and (f) after folding, where the green LEDs remain illuminated throughout the folding process. Plot of characterization of the blue LEDs on the fabricated foldable display before and after bending to 1 mm bending radius for 1000 bending cycles, for (g) current (mA) vs. voltage (V), (f) output power (mW) vs. input current (mA), and (i) intensity (a.u.) vs. wavelength (nm) at 100 mA.

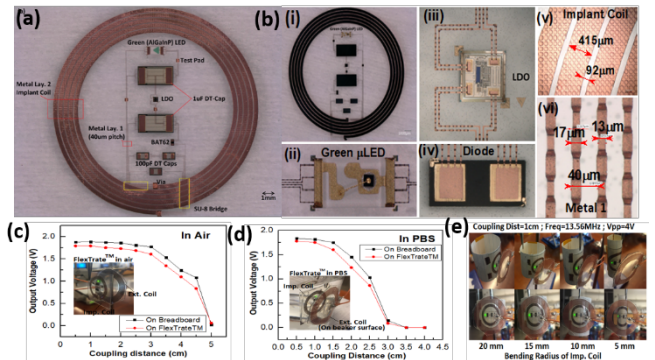


Fig. 5. (a) Optical image (Top-side) of the fabricated WPT system. (b) Optical image (i) shows the bottom-side of the same sample looking through the PDMS; zoomed in images of Green μLED (bottom-side), LDO & Schottky Diode (Top-side) are given in (ii), (iii) & (iv) respectively. Optical images of corrugated metal layer 2 & 1 are shown in (b), (v) & (vi) respectively. Comparison of output voltage (V_o of LDO, in Volts) vs. coupling distance for the breadboard test system and actual integrated system on FlexTrate in (c) air and (d) PBS. (e) shows a series of images for the FlexTrate system operating at different bending conditions in air for a coupling distance of 1cm (center-center). Insets in (c) & (d) are images of the integrated system operating in air & PBS respectively at 1cm coupling

IV. CONCLUSION

In summary, we have described a flexible (FOWLP) platform for heterogeneous integration of high performance dies in a flexible and biocompatible elastomeric package used to assemble >600 dies with die-shift (<6 μm) and a corrugated-interconnect ($\rho=2.3\mu\Omega\text{-cm}$) respectively with >1000

(R=1mm) bending cycles showing less than 7% change in average resistance. Through FlexTrate, we can target wearable and implantable applications that require high-performance foldable systems, and implantable neural implants.

ACKNOWLEDGMENT

This work was supported in part by AFRL, NBMC, DARPA, SRC JUMP and the UCLA CHIPS consortium.

REFERENCES

- [1] K. Jain, M. Klosner, M. Zemel, and S. Raghunandan, "Flexible electronics and displays: high-resolution, roll-to-roll, projection lithography and photoablation processing technologies for high-throughput production," *Proceedings of the IEEE*, vol. 93, pp. 1500-1510, 2005.
- [2] J. S. Chang, A. F. Facchetti, and R. Reuss, "A circuits and systems perspective of organic/printed electronics: Review, challenges, and contemporary and emerging design approaches," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, vol. 7, pp. 7-26, 2017.
- [3] M. Madsen, K. Takei, R. Kapadia, H. Fang, H. Ko, T. Takahashi, *et al.*, "Nanoscale semiconductor "X" on substrate "Y"—processes, devices, and applications," *Advanced Materials*, vol. 23, pp. 3115-3127, 2011.
- [4] J. Perelaer, P. J. Smith, D. Mager, D. Soltman, S. K. Volkman, V. Subramanian, *et al.*, "Printed electronics: the challenges involved in printing devices, interconnects, and contacts based on inorganic materials," *Journal of Materials Chemistry*, vol. 20, pp. 8446-8453, 2010.
- [5] K. Lee, S. Tanikawa, M. Murugesan, H. Naganuma, H. Shimamoto, T. Fukushima, *et al.*, "Degradation of memory retention characteristics in DRAM chip by Si thinning for 3-D integration," *IEEE Electron Device Letters*, vol. 34, pp. 1038-1040, 2013.
- [6] A. Hanna, A. Alam, T. Fukushima, S. Moran, W. Whitehead, S. C. Jangam, *et al.*, "Extremely Flexible (1mm Bending Radius) Biocompatible Heterogeneous Fan-Out Wafer-Level Platform with the Lowest Reported Die-Shift ($\leq 6 \mu\text{m}$) and Reliable Flexible Cu-Based Interconnects," in *2018 IEEE 68th Electronic Components and Technology Conference (ECTC)*, 2018, pp. 1505-1511.