Direct Measurement Structure of SRAM SNM

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***Abstract*—Static noise margin (SNM) is a major parameter of a Static Random Access Memory (SRAM) cell. Current approaches measure SNM indirectly or through probe points. This paper provides an approach to have flexible and direct access to the internal nodes of SRAM cells. It is possible to measure the SNM of a large number of SRAM cells quickly with a simple test setup, due to the controllability and visibility of the SRAM internal nodes. Therefore this approach can be used to characterize SRAM SNM in reliability stresses and radiation tests. Simulation proves that the error introduced in this approach is less than 5%.**

Keywords— Static noise margin; static random access memory; reliability; radiation environment

I. INTRODUCTION

Static noise margin (SNM) is a major parameter in the design of a Static Random Access Memory (SRAM) cell. It helps a designer determine the ratio of pull-up (PU), pull-down (PD) and passgate (PG) transistors, as shown in Fig. 1. To focus on the key point of SNM, this paper discusses a standard 6-transistor SRAM cell without write or read assist, but the test structure is applicable for other cell designs (such as an 8T cell) and for SRAMs that use write or read assist.

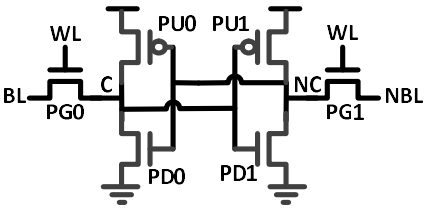


Fig. 1. 6-cell SRAM schematic, with pull up (PU), pull down (PD) and passgate (PG) transistors.

The SNM of an SRAM cell was first defined in [1] as the maximum value of the static voltage noise that can be tolerated by an SRAM cell without flipping state. The static noise is caused by offsets and mismatches that come from variations in processing and operation conditions. Fig. 2 is a graphic representation of read SNM, obtained from voltage transfer characteristic (VTC) of half of a SRAM cell. The VTC curves are usually referred as butterfly curves.

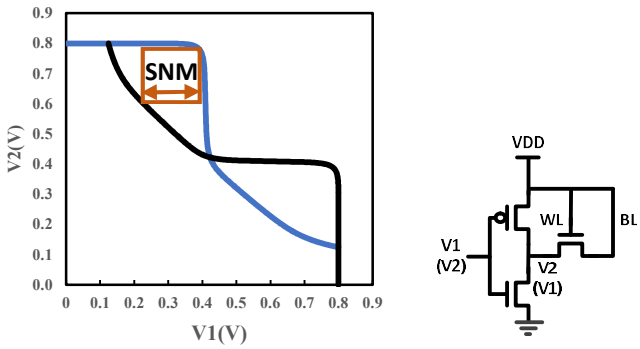


Fig. 2. Graphical representation of read SNM and the circuit to simulate it.

While most SRAM users care about speed, power, layout area, and reliability, a designer has to design the SRAM cell to have sufficient SNM. The balance between read, hold and write stability must be carefully considered while designing an SRAM cell. The greater read or hold stability of an SRAM cell, the more difficult it is to write to it, and vice versa. SNM provides insight into most problems associated with SRAM operation, reliability, and behavior in special environments such as a space radiation environment. SNM simulation is essential in SRAM cell design.

However, silicon measurement of SNM is not very common. With limited access to silicon fabrication resources and tight project schedules, most designers rely on foundry-provided transistor models, and only perform simulations. This approach works for most cases, since foundries model SRAM cells very carefully. Further, at advanced process nodes, designers often use foundry-provided SRAM cells. In this case, SNM simulations are performed only as a sanity check.

When SRAM cells must be operated in extreme environments not covered by foundry models, it is necessary to measure SNM in silicon tests. SNM measurement has been done in three ways. The first approach is to add probe points to have access to SRAM cell internal nodes [2]. The second approach is to fabricate isolated individual SRAM cells, then connect internal nodes to bumps for measurement [3]. Both approaches can measure only a small number of SRAM cells, because of cost in time and the complicated setup. The third approach is to measure SNM indirectly [4][5]. This works for write SNM. The write SNM is measured by raising the bit line (BL or NBL) from ground or lowering power from the normal operation voltage until the SRAM cell flips, while the word line is held at the power supply. The difference between the

power supply and bit line is the write-ability margin. Alternatively, the bit lines (BL and NBL) are set at the power supply and at ground while the word line (WL) is ramped up until the SRAM cell flips. The difference between the power supply and WL is the write-ability margin. The write-ability margin obtained in these two approaches gives indirect indication of the write SNM. It is not easy to measure read and hold SNM indirectly. In [5], the shift of read SNM with radiation was analyzed from the change of the cell trip point.

SRAM SNM measurement in total ionizing dose tests is valuable to evaluate the long term SRAM performance in a radiation environment. TID effects can reduce the SRAM SNM [6]. Some of the latest studies on transistor-level TID effects have been performed on planar 22-nm partially-depleted silicon-on-insulator and 14-nm bulk FinFET technologies [7]. In [6], there are simulations and measurements of the SNM of discrete 14 nm SRAM cells as a function of total dose.

This paper provides a test structure that allows flexible and direct access to the internal nodes of SRAM cells. It can be used to characterize SRAM SNM in reliability stresses and radiation tests, especially TID tests.

II. DIRECT MEASUREMENT STRUCTURE

A. Scheme

The controllability and observability of SRAM internal nodes are critical to measure SRAM SNM. In addition, it is preferred to be able to test a large number of SRAM cells in a short time with a simple test setup. The following paragraphs describe an approach to measure SNM using transmission gates (TG) to provide flexible and direct access to SRAM internal nodes. It can measure the SNM of a large number of SRAM bits in a short time. In addition, the test setup is simple. This approach is implemented with a commercial 14 nm technology as an example.

The design starts with a foundry provided 14 nm high density SRAM cell. Transmission gates are added to connect to internal node C and NC. The transistors of the transmission gate are the same transistors as in the SRAM cell to make the layout pass design rules check (DRC). To avoid the disturbance from the right side inverter, the connection from the right side inverter output to the left side inverter input is removed, as the "cut off" shown in Fig. 3. Limited by available space, only node B and C are connected outside of the SRAM cell. Node NC is not connected to the outside. Because the SRAM cell is symmetrical, the left and right side transistors should have identical characteristics, over than differences due to process variation. This assumption can be verified with one column of SRAM cells to measure left side of cell, and the next column to measure right side of cells. The VTCs from the left side transistors are enough to calculate SNM. Therefore, it is not necessary to control and observe node NC. The internal nodes of each bit are connected together through multiple levels of transmission gates to chip IOs for testing as shown in Fig. 4. Access to the SRAM cell internal nodes is allowed by enabling the transmission gates for a specific row and column. Row and column decoding circuitry are used to quickly and easily select the SRAM cell being tested, enabling rapid testing of many cells. The WL, BL and NBL are independently driven by control logic, to allow various setups for read, hold and write SNM measurement.

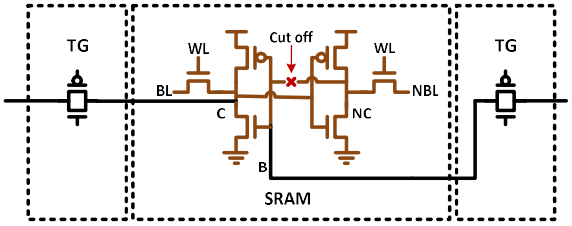


Fig. 3. The test structure of SRAM SNM with transmission gate.

The voltage drop along the path from chip IO to a SRAM internal nodes is the major source of SNM measurement error. The components for the voltage drop along the path are: 1. Voltage across the drain and source of transmission gates; 2. IR drops because of the metal resistance along the path; 3. Voltage drop in IO. This can be controlled by the transmission gate design and the number of transmission gates in the control path.

The transmission gates adjacent to the SRAM cells use the same type and size of transistors as those in the SRAM cells. Only the space between transistors and the metal connections are adjusted as little as possible to allow signal routing. Therefore the layout of the SRAM SNM test structure array is as close to an actual SRAM array as possible. This ensures that the SRAM SNM measurements are close to real applications, and it enables the test structure to pass the strict layout DRC for SRAM cells.

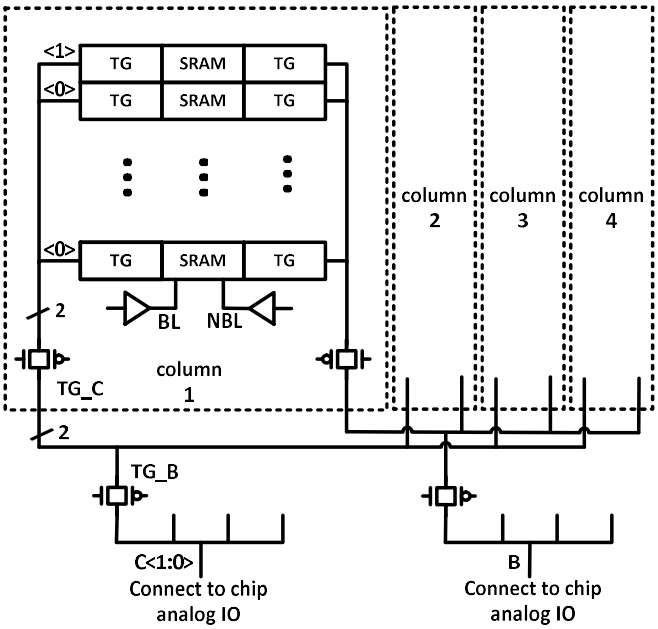


Fig. 4. Test structure block diagram.

The transmission gates for column selection and bank selection (TG_C and TG_B in Fig. 4) can be sized large enough to achieve an acceptable voltage drop across the

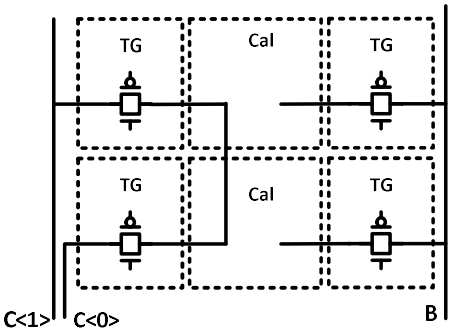
transmission gate, since they are handing active current from the select cell and leakage current from other cells. In the example implemented in a 14 nm technology, the voltage across all levels of transmission gate is limited to be less than 1% of power supply voltage, e.g. less than 8 mV as the VDD=0.8V.

The IR drop can be reduced by two ways. One way is to reduce the resistance along the path, such as using wide and short multiple layers of metal connection and redundant vias. The other way is to reduce the current along the path. Since we are measuring the active current of the selected SRAM cells, only the leakage current from unselected cells can be reduced by using fewer rows of cells in each column.

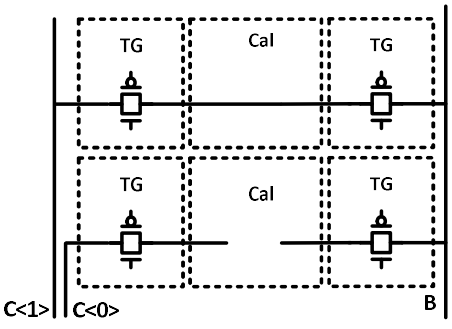
The IO structure should be carefully selected to ensure minimum voltage drop while satisfying the ESD protection.

B. Compensation of the voltage drop along path to the internal nodes

In the scheme described in the above section, voltage drop along the paths to the SRAM nodes are the major reason for measurement errors. Although the voltage drop is minimized by using large size transmission gate, careful consideration in layout, and the best IO structure, it still could be large enough to cause concern. For example, in reliability tests, and radiation tests, the voltage drop of transmission gates and the metal resistance may increase dramatically. It is necessary to monitor the voltage change and compensate for it in the measurements.



(a) The cells for output path C<1> and C<0>.



(b) The cells for input path B.

Fig. 5. Two cells to measure the voltage drop

Fig. 5 shows two kinds of cells that will be put inside the SRAM array to measure the voltage drop. These cells are similar to the cell shown in Fig. 3, with the SRAM cell replaced by a Cal cell. The Cal cells have direct connections between two nodes, while the other two nodes are opens. The Cal cells are created from a SRAM cell, and only metal connections are changed. The cell shown in Fig. 5 (a) can be used to measure the voltage drop from output C<1> and C<0> to the SRAM internal nodes. By configuring the transmission gates, node C<0> can be connected a voltage source while the voltage at node C<1> is measured. The voltage difference between the voltage source and measured voltage is the voltage drop along the path from C<0> to C<1>. Half of this value is the voltage drop along one path, i.e. from one output to the SRAM cell, since this path is identical for a Cal cell and a SRAM cell. The cell shown in Fig. 5 (b) can be used to measure the voltage drop along the path from node B to node C<1>, which allows the calculation of the voltage drop from node B to the SRAM cell.

C. Simulation results

A complete design structure is implemented with a commercial 14 nm technology. It has been used to simulate the read, write and hold SNM of foundry provided SRAM. The netlist with parasitics extracted for the test structure and IO structure are used in the simulation. The results show VTC curves simulated from test structure are very close to those simulated directly from the SRAM cell. The differences are too small to be shown in a plot. The simulations cover typical (TT), slow (SS) and fast (FF) process corners. The voltage range is from 0.7V to 0.9V, with typical operation voltage of 0.8V. The operation temperature is -55° C to 125° C. The worst error between the simulated SNM from test structure and SRAM cell is 4.0%. This is much less than the variation of the SNM over process corners, which is about 10%.

TABLE I. COMPARISON BETWEEN THE SNMS FROM THE TEST STRUCTURE AND SRAM CELL

	-55°C 0.9V FF		
	SNM test structure	SRAM cell	Error
Write SNM (V)	0.291	0.287	1.4%
Read SNM (V)	0.138	0.144	-3.9%
Hold SNM (V)	0.357	0.359	-0.45%

	27°C 0.8V TT		
	SNM test structure	SRAM cell	Error
Write SNM (V)	0.267	0.265	0.87%
Read SNM (V)	0.149	0.152	-1.5%
Hold SNM (V)	0.340	0.340	-0.1%

	125°C 0.7V SS		
	SNM test structure	SRAM cell	Error
Write SNM (V)	0.238	0.229	4.0%
Read SNM (V)	0.140	0.142	-0.8%
Hold SNM (V)	0.298	0.299	-0.3%

D. SRAM SNM measurement in TID tests

SRAM SNM measurement in TID tests requires a more complicated test setup than a regular SRAM SNM test. Limited by the TID irradiation space, available connection channels, short time window for measurements, and long test time, it is challenging to measure the SNM of large amount of SRAM cells needed to get meaningful statistics. With the test structure described in this paper, it is easy and fast to switch SRAM cells for SNM measurement. Therefore, it is allowable to measure SNM of many SRAM cells in TID tests.

III. FUTURE WORK

The proposed test structure is planned to be included on a test chip and the tape-out will be in the summer of 2019. Silicon will be available to test by the end of 2019. This test structure can be used to characterize the SRAM SNM over normal operation conditions, in a reliability or radiation test. The change in SNM can be used to explain and predict the SRAM performance across operating conditions and lifetime.

IV. SUMMARY

This paper presents an approach to measure read, write and hold SNM of SRAM cells by direct control and observation of SRAM internal nodes. This approach can be used to measure SNM quickly with a simple setup. Therefore, it can be used to characterize SNM of a large number of SRAM bits in a short time. This approach is suitable to characterize SRAM SNM in reliability stresses and radiation tests. Simulation shows this approach has a maximum error of 4%. A test chip is in design, and it is expected to be available to test in late 2019.

REFERENCES

[1] E. Seevinck, F. List, and J. Lohstroh, “Static-noise margin analysis of 748–754 MOS SRAM cells,” *IEEE J. Solid-State Circuits*, vol. SC-22, no. 5, pp., Oct. 1987.

[2] R. E. Stallcup, II and Z. Cross, “Measuring static noise margin of 65 nm node SRAMs using a 7-point SEM nanoprobing technique,” in Proc. ISTFA, 2007, pp. 223–225.

[3] Q. Zheng *et al*., "Read Static Noise Margin Decrease of 65-nm 6-T SRAM Cell Induced by Total Ionizing Dose," in *IEEE Transactions on Nuclear Science*, vol. 65, no. 2, pp. 691-697, Feb. 2018.

[4] S. Chellappa *et al*., "In-situ characterization and extraction of SRAM variability," *Design Automation Conference*, Anaheim, CA, 2010, pp. 711-716.

[5] Xiaoyin Yao, N. Hindman, L. T. Clark, K. E. Holbert, D. R. Alexander and W. M. Shedd, "The Impact of Total Ionizing Dose on Unhardened SRAM Cell Margins," in *IEEE Transactions on Nuclear Science*, vol. 55, no. 6, pp. 3280-3287, Dec. 2008.

[6] M. P. King *et al*., "Analysis of TID Process, Geometry, and Bias Condition Dependence in 14-nm FinFETs and Implications for RF and SRAM Performance," in *IEEE Transactions on Nuclear Science*, vol. 64, no. 1, pp. 285-292, Jan. 2017

[7] M. P. King *et al*., "TID-Induced Leakage and Drive Characteristics of Planar 22-nm Partially-Depleted Silicon-on-Insulator and 14-nm Bulk and Quasi-Silicon-on-Insulator FinFET Devices,” presented at NSREC, 2018.