

A Radiation-Tolerant D Flip-Flop Designed for Low-Voltage Applications

Grant D. Poe, Jeffrey S. Kauppila, Dennis R. Ball, Bharat L. Bhuva, Timothy D. Haeffner, and Lloyd W. Massengill
Department of Electrical Engineering and Computer Science
Vanderbilt University
Nashville, TN 37235
Email: grant.d.poe@vanderbilt.edu

Abstract—A radiation-hardened by design (RHBD) D flip-flop (DFF) is presented that demonstrates a tolerance to radiation induced single-event upsets (SEUs), while maintaining desirable electrical performance characteristics over a wide range of supply voltages. The flip-flop is based on the unhardened Static Single-phased Contention Free Flip-Flop (S2CFF) and maintains all three characteristics of being static, single-phased, and contention free for robustness in low voltage operation. The radiation robustness and electrical performance of the new RHBD D flip-flop design is then compared to the unhardened S2CFF, and an RHBD DICE FF design.

Keywords—D flip-flop, DICE, single-event upset, NTC, low-voltage, PVT

I. INTRODUCTION

With highly-scaled CMOS devices, radiation induced SEUs in sequential logic elements are an increasing problem. Smaller device sizes have led to smaller node capacitances and smaller time constants, leaving individual nodes susceptible to Single-Event Transients (SETs) with diminished deposited energy required to cause a bit corruption (upset). Dual Interlocked Storage Cell (DICE) [1] designs provide hardness in latch-type memory cells by utilizing interleaved feedback such that an SET must simultaneously affect at least two separate nodes in order to cause an upset. However, this hardening technique comes with significant penalties in terms of circuit speed and layout efficiency.

Another major concern with increasing device density has become localized power dissipation, resulting in significant on-chip thermal stress. One popular technique to control power scaling is to lower the circuit operating voltage to limit per-cycle energy dissipation. Lowering the voltage, however, comes at an overall performance cost, in particular with respect to speed and sensitivity to Process/Voltage/Temperature (PVT) variations[2]. This work focuses on a DFF design that has robust performance over a wide range of supply voltage, and is more resistant to radiation than existing commercial DFF designs.

Section II of this paper outlines the S2CFF[3], which is a commercial design that this work seeks to harden against radiation. Section III then describes the newly designed radiation hardened DICE S2CFF or DS2CFF which is the primary focus of this paper. Section IV compares the S2CFF, DS2CFF, and a standard RHBD DICE FF[1] in terms of electrical performance and also discusses the relative radiation hardness of each design. Section V discusses the layout

characteristics and extracted simulation results of each design. This is followed by a brief overview of key points in the conclusion.

This work is targeted for application at the 14/16nm bulk FinFET technology generation.

II. STATIC SINGLE-PHASE CONTENTION FREE FLIP-FLOP

The radiation tolerant DFF presented in this work is derived from the Static Single-Phased Contention-Free Flip-Flop (S2CFF) design[3]. The stated purpose of S2CFF is to operate as an effective flip-flop at both nominal voltages and Near-Threshold Computing (NTC) voltages. To accomplish this, the S2CFF has static operation, uses a single-phased clock, and has contention free transitions. Static operation is desirable because at low voltages dynamic nodes are particularly vulnerable to noise and leakage under PVT variations. A single-phase clock allows for the removal of the local clock buffers, and causes less power to be dissipated by switching clock nodes while the flip-flop input remains constant. Contention-free operation is required due to decreased reliability in ratioed logic caused by larger relative variations in device drive strength at low voltage.

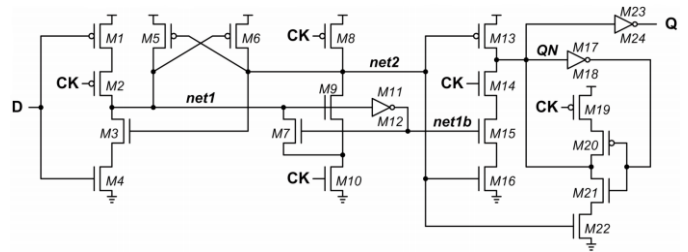


Fig. 1. Schematic of the S2CFF from [3]

Shown in Figure 1 is the schematic of the S2CFF. Figure 2(a) displays the circuit's basic operation. For the S2CFF, the worst-case Hold time and Clock-to-Q (C-Q) delay in large part are dictated by how quickly net2 in the schematic shown can be discharged through M9 and M10. For the worst-case Hold time, this is because net2 controls the gate to M3, and must be pulled low to electrically isolate net1 from the input D. Similarly for the worst-case C-Q delay, net2 must be pulled low to turn on M13 and load a high value to node QN. Therefore, it is of particular importance that M9 and M10 have strong and consistent drive strength. While the focus of this paper is not on optimizing the timing characteristics of the S2CFF, the

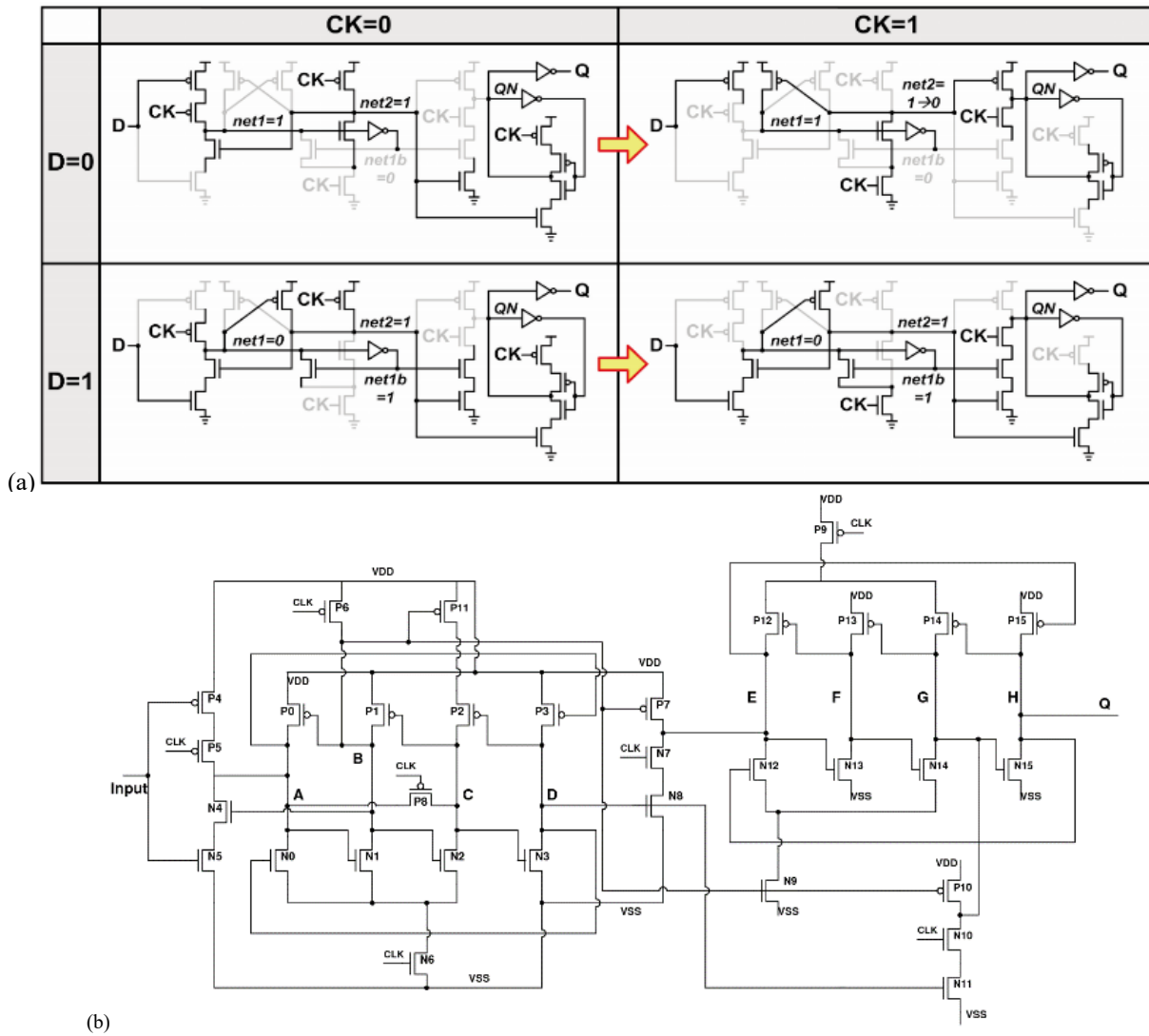


Fig. 2. (a) basic operation of the S2CFF from [3], (b) schematic of the DS2CFF without transistors N6, N9, or P9 split

DS2CFF has an analogous node to $net2$ that is similarly important for the electrical timing characteristics of the circuit.

This work identified that 15 of the 24 transistors in the S2CFF could cause an upset when voltage-perturbed by a single-event transient. Despite most of these vulnerabilities only existing during a specific timing window, with so many nodes soft to radiation, a significant portion of the S2CFF will be vulnerable to single-node strikes at all times. This work applied a targeted hardening approach to mitigate SEUs while incurring as little performance penalty as possible. Therefore, to maintain PVT robustness at low voltage, the new design presented in this work is also static, single-phased, and contention-free.

III. DICE S2CFF

In order to harden the S2CFF against radiation, the internal storage nodes of the flip-flop were converted to a DICE configuration, resulting in the DICE S2CFF or DS2CFF cell. The DICE configuration splits the internal feedback nodes into

four nodes such that if the voltage at one node is perturbed, such as by a radiation transient, at most one other node will be affected, and the remaining unaffected nodes will maintain and restore the previously held value. The DICE hardening technique was selected over other hardening methods, e.g. hardening through capacitance to increase the value of critical charge, because these hardening methods demonstrated a significant penalty in area, speed, and power, while providing a relatively small increase in design robustness to SEUs.

Figure 2(b) shows the schematic of the DS2CFF. The operation of this circuit is similar to the S2CFF, except it utilizes a DICE configuration in both the Master and Slave latch. In this new flip-flop the nodes A and C are effectively analogous to $net1$ in the S2CFF. Similarly, nodes B and D are analogous to $net2$ and $net1b$, respectively. Node B therefore is critical in determining the DS2CFF's worst-case Hold time and C-Q delay, as $net2$ is for the S2CFF. This schematic maintains all three qualities of being static, single-phased, and contention-

DFF (Voltage)	C-Q Delay	Setup Time	Hold Time	Power ($\alpha=.1$)	Power ($\alpha=.5$)
DICE DFF[1] (.8V)	14.26 ps	4.93 ps	-0.17 ps	2.079 uW	2.819 uW
S2CFF[3] (.8V)	9.12 ps	7.27 ps	-2.97 ps	1.069 uW	1.525 uW
DS2CFF (.8V)	10.78 ps	13.88 ps	-2.21 ps	1.645 uW	2.340 uW
DICE DFF[1] (.4V)	159.4 ps	44.6 ps	1.69 ps	175.63 nW	236.67 nW
S2CFF[3] (.4V)	115.1 ps	57.5 ps	-7.55 ps	86.70 nW	122.77 nW
DS2CFF (.4V)	126.2 ps	100.7 ps	-5.47 ps	133.61 nW	186.33 nW

Table 1. Schematic level electrical simulation results

free. Furthermore, with this DS2CFF configuration, most single node strikes do not cause the value stored in the flip-flop to alter.

While the DICE hardening technique has proven to be effective in increasing the robustness to SEUs, DICE designs at highly scaled technology generations have been shown to be vulnerable to an effect known as charge sharing[4] - a phenomenon where a single ion can generate enough charge over a broad enough area to perturb more than one node in a given circuit. DICE latches are vulnerable to upsets resulting from multi node transients, therefore extra care must be taken to separate co-vulnerable nodes in the cell layout at a distance that is not affected by charge sharing. Specifically, as shown in Fig. 1, nodes A, B, E, and F must be separated from nodes C, D, G, and H, respectively, to mitigate the charge sharing vulnerability mechanism. This adds to the overhead of the design, and causes transistors N6, N9, and P9 to be split so that additional long metal lines are not required.

IV. CIRCUIT COMPARISON

The proceeding results were all produced in simulation using the Virtuoso schematic capture tool with the transistor models provided in the commercial PDK along with data-validated bias-dependent single-event models[5] in Cadence. The use of this tool allows for the identification of single node vulnerabilities within a circuit, and was employed in standard schematic simulations to identify vulnerabilities, and then again with full extracted layout parasitics to determine the LET threshold for which upsets can occur. All of these simulations were carried out with 2-fin (minimum sized) devices, with one noted exception.

Despite the DICE configuration of the storage nodes in the DS2CFF, there still exist single node vulnerabilities. All of these vulnerabilities are due to node B in the circuit, which facilitates the use of a single phased clock. A strike that pulls node B from high to low while the clock is low can pull up nodes E and G through transistors P7 and P10, respectively, which would change the value stored at nodes E, F, G, and H to 1, 0, 1, and 0, respectively, regardless of the originally stored values. This can occur when transistors N1 or N6 are struck. However, when N6 is struck, the only way an upset can occur is if N1 is on, and N1 has a stronger drive strength than P6. By increasing the size P6 to 3 fins, P6 will have a stronger drive strength than N1 and therefore N6 will no longer be a vulnerable transistor. Furthermore, using the parasitics

extracted from the layout, the LET upset threshold for N1 was 21.5 MeV-cm²/mg, which would make it resistant to single node strikes in many environments. A strike that pulls B from low to high while the clock is high will turn on N4 and allow A to be pulled down through N4 and N5, causing two co-vulnerable nodes (A and B) to perturb which will cause an upset. The LET threshold for this vulnerability is much lower at 1.84 MeV-cm²/mg. In order for this second case to occur, however, the input must switch from 0 to 1 immediately after the clock edge. This vulnerability will only persist for as long as the clock is still high after this input transition occurs, and thus for many common input patterns, this vulnerability will have a small or possibly zero timing window in which it can occur.

Table 1 above shows a comparison of the simulated schematic level electrical performance of the DS2CFF against the S2CFF, and a DICE DFF, with all minimum sized devices except P6 in the DS2CFF. The DICE DFF design selected for this comparison is static and contention-free, making it a likely competitor for low-voltage applications in radiation environments. It can be seen from the table below that the DS2CFF has electrical performance advantages over the DICE DFF at both nominal and NTC voltages, particularly with respect to power. α in the chart refers to the activity ratio, or the portion of time that the input switches in between positive clock edges.

While the DICE DFF itself does not have any single node vulnerabilities in its internal storage nodes, it is possible to strike one of the internal clock buffers and cause a false clock edge that could prematurely load data into the flip-flop, which would be considered an upset. Because it is single-phased, the DS2CFF has the advantage of having no local clock buffers, such that multiple flip-flops can be driven by a single larger clock buffer. This would cause the clock node in the DS2CFF to have a significantly higher capacitance, and thus a higher value of critical charge to perturb the node, making the node more robust against radiation induced transients.

In reliability simulations, it was found that due to the large capacitance of node B in the DS2CFF, the size of N1 and the split N6 directly underneath N1 needed to be 3 fins instead of 2 for more consistent operation in worst-case conditions. However, for the data presented in the entirety of this paper, N1 and N6 are 2 fin devices. Increasing the size of N1 and N6 causes N6 to be vulnerable again because of the drive strength of N1. Increasing the size of P6 to 4 fins would correct

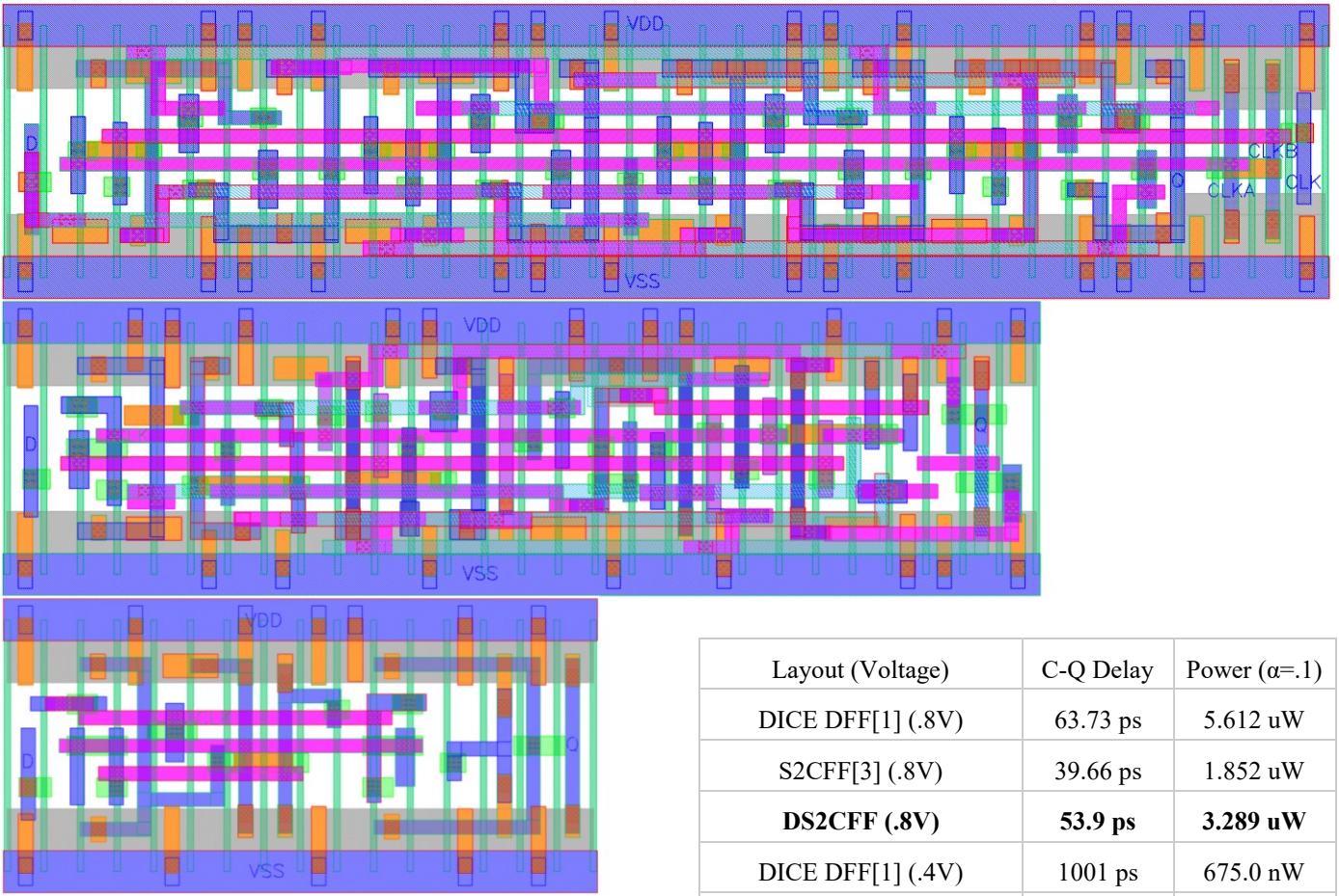


Fig. 3 Layout images of DICE DFF(top), DS2CFF(middle), and S2CFF(bottom)

this, but that would likely be unnecessary for many environments considering that the upset threshold for N6 would likely be as high or higher than N1's upset LET threshold of 21.5 MeV-cm²/mg. Increasing the size of N6 and N1 also has the added benefit of improving both worst-case C-Q delay and hold time in the DS2CFF, as node B being pulled from high to low is part of the critical path of both of these timing characteristics.

The upsets discussed so far in this paper all pertain to memory bit flips occurring while the master or slave latches are storing data. However, upsets can also occur due to transients seen at the input of the flip-flop near the positive clock edge. If the input to the flip-flop has not changed between clock cycles, an upset can only occur if the transient is larger than the sum of the setup time and hold time[6]. For the DICE DFF, the setup-and-hold window is similar in magnitude whether the input is high or low. However, the S2CFF and DS2CFF have asymmetric setup-and-hold windows. From the parasitic extracted layouts, it was found that a minimum LET of ~3 MeV-cm²/mg was required to upset all three flip-flops. The lopsided setup time for the S2CFF and DS2CFF, however, cause the upset threshold to be >10 MeV-cm²/mg when the input is high. This may provide a moderate improvement in radiation hardness, but considering it only applies when the input is high, and when the input hasn't switched between positive clock

Layout (Voltage)	C-Q Delay	Power ($\alpha=.1$)
DICE DFF[1] (.8V)	63.73 ps	5.612 uW
S2CFF[3] (.8V)	39.66 ps	1.852 uW
DS2CFF (.8V)	53.9 ps	3.289 uW
DICE DFF[1] (.4V)	1001 ps	675.0 nW
S2CFF[3] (.4V)	701.1 ps	215.9 nW
DS2CFF (.4V)	1052 ps	376.2 nW

Table 2. Extracted Layout electrical simulation results

edges, this is more of a serendipitous benefit instead of a deliberate design choice.

V. LAYOUT COMPARISON

Shown in Figure 3 are the layouts for the S2CFF, DICE DFF, and DS2CFF. All three of these layouts were created for the purpose of this research at the 14/16nm node. The DS2CFF and DICE DFF are 1.75x and 2.25x larger than the S2CFF, respectively. Meaning the DS2CFF is roughly a 22% area savings when compared to the similarly radiation hardened DICE DFF.

From the images it is clear that there is significantly more metallization over the DICE DFF and the DS2CFF compared to the S2CFF. This is due to the efforts taken to separate co-vulnerable nodes in these designs to reduce the effects of charge sharing. Nodes A, B, E, and F were separated from C, D, G, and H respectively. This is because for these node pairs, the PMOS and NMOS transistors will be off at the same time, and when they are simultaneously struck, an upset can occur. Separating these nodes greatly reduces the probability that a single strike will collect charge at both nodes. For the DS2CFF,

the closest co-vulnerable nodes are separated by 756 nm. The DICE DFF shown similarly has at least 1022 nm of separation. For both layouts, this node separation was achieved by splitting both the master and slave latches and interleaving them such that the layouts are organized as follows: first half of master, first half of slave, second half of master, and second half of slave, from left to right. While the DICE DFF has more node separation, the DS2CFF has significant enough node separation such that the effect of charge sharing will be greatly mitigated in it as well. No such node separation is done for the S2CFF because this circuit contains many single-node vulnerabilities where node separation would serve no purpose in mitigating SEUs. Additionally, this node separation does not protect against strikes that effect the opposite sides of two adjacent nodes (e.g. a strike that pulls node B high and node A low).

Table 2 is similar to Table 1 except it uses the parasitics extracted from the layout to show electrical performance and would therefore be likely more indicative of how the circuit instantiated at the 14/16nm technology node would actually perform. The parasitic resistance, capacitance, and coupled capacitance were extracted using the Calibre Parasitic Extraction tool for this generated data, as well as the data previously discussed relating to upset LET thresholds. The clock buffers for the DICE DFF were increased from 2 fins to 3 fins to mitigate a disproportionate slowdown initially seen in the DICE DFF when switching from the schematic to the layout. The DS2CFF contains all 2 fin devices except for P6 which is 3 fins, and N15 and P15 are increased to 2 fingers of 2 fins for a stronger output stage. Simulations were conducted by creating a layout with an external clock buffer feeding into 2 identical flip-flops. Then the circuits with extracted parasitics were simulated. The power value in the chart is the power consumption of only one of the flip-flops from this set up. From the table it can be seen that the DS2CFF has comparable speed to the DICE DFF but has significantly reduced power consumption and reduced area.

VI. CONCLUSIONS

This work targets a middle ground between absolute radiation hardness and electrical performance for a low-power latch element designed for advanced FinFET technology nodes

– called the DS2CFF. Calibrated simulations based on instantiated layouts at 14/16nm show the DS2CFF achieves this target with a significantly reduced number of vulnerable nodes and limited temporal upset windows for nodes susceptible to SEU compared to commercial DFF designs, while also having electrical performance advantages over an existing DICE DFF. The DS2CFF contains single-node vulnerabilities, however the specific timing conditions required for an upset to occur mitigate their impact on overall error rate. In addition to increased radiation hardness over its antecedent design (the S2CFF), the DS2CFF remains static, single phased, and contention free, which makes it a strong candidate for low-voltage applications where radiation reliability is a concern.

ACKNOWLEDGMENT

This work was supported in part by the Defense Threat Reduction Agency (DTRA) under grant HDTRA1-17-1-0003. The authors would also like to thank the Cadence and Mentor Graphics University Programs for providing access to design, verification, and simulation tools.

REFERENCES

- [1] T. Calin, M. Nicolaidis, and R. Velazco, "Upset hardened memory design for submicron cmos technology," *Nuclear Science, IEEE Transactions on*, vol. 43, no. 6, pp. 2874–2878, Dec. 1996.
- [2] R. Dreslinski et al, "Near-threshold computing: Reclaiming Moore's law through energy efficient integrated circuits," *Proceedings of the IEEE*, vol. 98, no. 2, pp. 253–266, Feb. 2010.
- [3] Y. Kim et al., "A static contention-free single-phase-clocked 24T flip-flop in 45nm for low-power applications," *Proceedings of the IEEE International Solid-State Circuits Conference*, pp. 466–467, February 2014.
- [4] O. A. Amusan, A. F. Witulski, L.W. Massengill, B. L. Bhuvu, P. R. Fleming, M. L. Alles, A. L. Sternberg, J. D. Black, and R. D. Schrimpf, "Charge Collection and Charge Sharing in a 130 nm CMOS Technology", *IEEE Trans. On Nuclear Science*, Vol. 53, No. 6, pp. 3253–3258, December 2006.
- [5] J. S. Kauppila, D. R. Ball, J. A. Maharrey, R. C. Harrington, T. D. Haeffner, A. L. Sternberg, M. L. Alles, and L. W. Massengill, "A Bias-Dependent Single-Event-Enabled Compact Model for Bulk FinFET Technologies," Accepted for Publication in *IEEE Transactions on Nuclear Science*, 2019.
- [6] V. Joshi, R. R. Rao, D. Blaauw, and D. Sylvester. Logic SER reduction through Flip-Flop redesign. In *IEEE Symposium on Quality Electronic Design, ISQED*, pages 611–616. IEEE Society, 2006.