A Rapid Microelectronics Packaging Platform Implementing Self-Shielded Interconnects

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***Abstract*—Miniature Multi-wire Systems (MMS) is an emerging rapid packaging platform for complex microelectronic systems. Packaging time is minimized by creating all interconnects using bond wires and micron-sized coaxial cables (MCCs). Design cycle time is greatly reduced by installing shield bond wires for high frequency interconnects, preventing electromagnetic interference. The MCCs are typically partitioned into two classes, one for signal distribution with characteristic impedances between 30-70 ohms, and one for power distribution with impedances less than 10 ohms. We have developed methods to fabricate, strip and bond MCCs with outer diameters between 25-100 microns. Crosstalk measurements show at least 20 dB greater isolation for MCCs than bare bond wires. Customized hardware and software algorithms compatible with a conventional wire bonder enable automated interconnect design and routing capabilities for modules with hundreds of interconnects. The software incorporates geometric and electrical design targets for the MMS platform and outputs a full interconnect placement order with geometric data for 3-dimensional routing geometries.**

Keywords— Rapid Integration; High Frequency Electronics; Microelectronics Packaging; Heterogeneous Integration

I. Introduction

Today's electronic devices continue to shrink in size while computing functionality becomes more complex. This is driven by the demand for massive amounts of data, both received and transmitted. Data rates may increase up to 3Gbps with the introduction of 5G cellular and for applications including "Internet of Things" (IoT), RF communications, mobile and wearable devices, autonomous vehicles, and others [1,2]. Heterogeneous multi-die System-in-Package (SiP) integration has become the preferred method of mating a diverse set of individual components with specific functionalities (CMOS, MEMS, Power devices, RF modules, passive components, etc.) over foundry-scale homogeneous integration. SiP offers smaller form factor, higher performance, faster time-to-market, lower cost and increased platform flexibility relative to the homogeneous analogs [2].

Fig. 1 compares the amount of time it takes to progress from an electrical schematic to the first testable hardware article for common multi-chip module (MCM) SiP packaging solutions. The x-axis is an estimate of the integration complexity, which is a weighted sum of the types of interconnects normalized by the area over which those connections are made. Connections are partitioned into three types: standard digital interconnects, power, and high frequency. The weighting coefficients qualitatively reflect the difficulty of the electrical design.

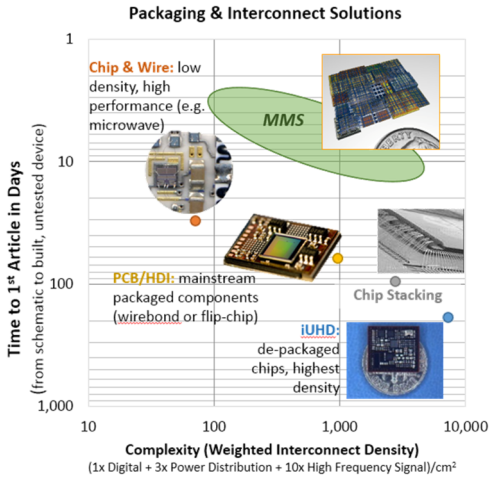

Fig. 1. Packaging time versus device complexity for conventional and MMS packaging platforms.

Layout, simulation and fabrication time cumulatively increase with device complexity when using today's existing packaging strategies. Chip and Wire is a relatively rapid method of integration, but is typically only used for millimeter wave integrated circuits (MMICs), requiring small numbers of interconnects over a large area [3]. Printed circuit boards (PCB) and high density interconnect (HDI) packaging strategies leverage rapid fabrication strategies such as soldering and wire bonding [4]. However, PCB/HDI technologies push the limits of through-substrate via (TSV) pitch capabilities and TSVs are expensive and time consuming to fabricate. Both PCB/HDI and chip-stacking leverage wire bonding, a high speed integration process, but time is often lost in lengthy design, simulation, and re-design cycles to evaluate electrical performance of longer wire bonds, which yield higher inductance and resistance interconnects [4]. Integrated ultra-high density iUHD MCMs offer the highest interconnect density of all packaging methods discussed here. The interconnect density is enabled by lithographic processing of both the metals and dielectrics in the redistribution layers (RDLs)[5]. However, lithographic patterning of RDLs can take up to a week for each layer. Due to the high density of interconnects, both thermal and electrical design time and simulation is quite lengthy with iUHD modules, with some designs taking as much as two years prior to first article fabrication.

The Miniature Multiwire Systems (MMS) packaging paradigm has been conceptualized by Draper to provide a solution in which rapid fabrication of complex microelectronics

is possible [6]. MMS leverages the integration speed of wire bonding processes and minimizes design and simulation cycles by using shielded interconnect wires. These concepts can be utilized to integrate a diverse set of components from chip-scale packages to bare die. The key challenges in achieving rapid integration using the MMS paradigm are fabrication of micron-sized coaxial cables (MCCs), integration tool design for stripping and bonding the MCCs, establishing wire placement order, and grounding the MCCs and module components. In this paper, we will discuss the MMS module layout procedure, MCC interconnect design, and MCC attachment processes.

II. Module Design

We will refer to two different module configurations, interposer and "dead bug." Fig. 2A shows a cartoon of the cross-section for an interposer configuration in which chips are flip-chip mounted on one side of the board and encapsulated. Wires and MCCs are then placed on the opposite side of the board. The interconnect side of the board also has a ground plane to which all of the coax shields are connected. The interposer configuration simplifies interconnect installation and grounding because it standardizes the metallization to which the MCCs are connected, and it brings the ground plane directly adjacent to the signal contacts, which minimizes joint inductance. However, high density through-via interposers are challenging to fabricate, making the interposer configuration most compatible with chip-scale packaging, rather than die-scale integration. While we do expect accelerated design time with the interposer configuration, fabrication time may not be accelerate relative to a PCB/HDI format due to the need for a 2-layer interposer board.

Fig. 2B shows the second MMS configuration, called the "dead-bug" configuration, most compatible with bare die, but could be used to integrate chip-scale packages. In the dead-bug configuration, chips are placed face up on a substrate. Wire bonds and MCCs are then directly connected to the chip pads. Here, time savings is expected both in design and fabrication. Grounding to avoid large inductance loops and power insertion for multiple power domains are the largest challenges in the dead-bug configuration.

Fig. 3 shows a module containing bare-die components for a high complexity MCM containing memory and logic components requiring more than 60 RF and HSD interconnects, with more than 400 power insertion points over 8 power

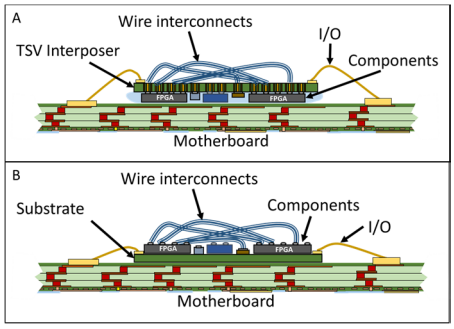

Fig. 2. Cartoon cross sections of MMS module configurations: (A) interposer, and (B) "dead-bug."

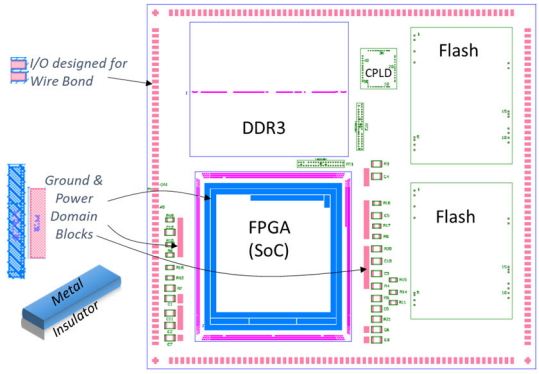

Fig. 3. Sample high complexity module requiring bare-die integration in the dead-bug configuration.

domains. In this design, we have added metallized chips for power domains partitioning and grounding.

In the following sections, we define electrical design criteria for both the interposer and dead-bug MMS module configurations. The electrical considerations for the MCC interconnects are evaluated against the geometric constraints for both chip-scale and die-scale integration. Finally, we discuss further MCC material and geometric design criteria with respect to the methods chosen for stripping and bonding the MCCs. We conclude with a baseline performance summary of both PDN and SDN MCCs and junctions to the substrate.

III. Process Flow and Layout

Fig. 4 shows the MMS module design flow process. After a schematic and bill of materials is decided with the customer, an initial layout is constructed using a standard electronics computer aided design (ECAD) software package, such as Mentor Graphics. The MMS design process begins when the ECAD engineer places all of the virtual components onto a planar substrate. The input/output (I/O) interface for the module is placed at the perimeter of the substrate and is de-signed to interface with the motherboard using wire bonds. Designs for flip-chip integration will be considered in future work. Once the components are placed on the substrate, the "rat's nest" layout is plotted and adjustments are made to the location and orientation of the components and I/O by the ECAD engineer to visually minimize route crossings seen in the rat's nest. A custom software algorithm is used to export geometric data and the net list required to physically route wires. This file is referred to as the "augmented net list."

This augmented net list is then imported into customized automated routing software that establishes an ordered placement of the interconnects to avoid placement conflicts, such as obstructions due to bond pads and intersecting routes. For the most complex modules, such as the one shown in Fig. 4, obstructions cannot be avoided when using straight line routing. For these scenarios, we insert "stopover points" to bend the routes around features where obstructions are not permitted. A thorough discussion about how the code assigns routing priority can be found in [9].

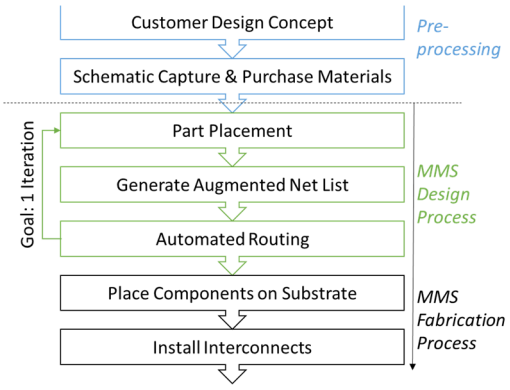

Fig. 4. Layout and fabrication process for MMS modules.

Geometric design rules for individual interconnects are driven by the electrical design targets, which can be built into the automated routing code as well. The geometric design constraints depend on the net class to which the interconnect belongs. There are two major net classes: one for the power distribution network (PDN), and one for the signal distribution network (SDN). The PDN is typically routed using coax with low impedance (e.g. low inductance), whereas the SDN is routed with higher impedance coax, load matched per component specifications. A typical SDN cable is between 30-75Ω.

For complex modules, such as the one in Fig. 3, requiring more than 700 interconnects, it is advantageous to further subdivide the PDN and SDN net classes for two reasons. First, the installation of MCCs is more challenging than installing standard wire bonds. Due to the availability of automated wire bonding tools, it is desirable to use standard wire bonds whenever possible. Second, the most critical data and power transmission lines often have additional constraints on length and these constraints need to be individually addressed in the routing code. SDN sub-net classes include:

- High speed digital (HSD), reqiring length matching to hundreds of microns
- High speed differential (HSDif), requiring MCC pairs to be length matched within hundreds of microns
- RF, requiring MCCs length matching to tens of microns
- Standard digital, which can be routed with standard wire bonds or thinly insulated wires with no length constraints

Ideally, the PDN interconnects are routed using shielded wires to prevent voltage ripple on the power supply due to mutual inductance [8]. However, it may be useful to use standard bond wire in place of coax when possible due to simpler installation when routing modules with hundreds of power connections. Sub-division of the PDN net class would be driven by the length over which the power is transmitted and an evaluation of the current requirements. A cut-off length would be imposed by the routing code and wires that are longer than the cut-off length would require coaxial connections. Additionally, power domain subdivisions may be driven by different current requirements yielding a need for different diameter wires.

Once the routing has been rendered, the layout proceeds to a full design review by the electrical and fabrication engineers. Iterations on the layout are minimized by incorporating the majority of the geometric and electrical design targets into the routing code.

IV. MCC Design and Fabrication

The three functional portions of the MCCs are the core, dielectric and shield. A cross sections for PDN and SDN MCCs are shown Fig. 5. The following sections discuss how each portion is sized relative to the geometric and electrical requirements of the components. The dimensions of each portion of the MCC drive the types of processes used during fabrication. Whenever possible, we try to leverage the resources of commercial wire manufacturers, but some dimensions are too challenging for commercial processes. This lead us to create custom processes for the most challenging portions of the MCCs.

A. Power Distribution

A thorough discussion of how the PDN MCCs are designed and fabricated can be found in [8] and [10]. However, we will briefly review it here. While power distribution networks can be quite complicated to design, we simplified the design rules and added significant margins of error. Equation (2) shows the simplified method for determining the minimum radius of the PDN MCC core, r_c,

$$r_c \geq \sqrt{\frac{2\bar{l}}{\pi N \sigma_c Z_{sys}}} \tag{2}$$

where N is the number of power insertion points, $\bar{l}$ is the mean distance the coax needs to traverse, σ_c is the conductivity of the core, and Z_{sys} is the maximum tolerable system impedance.

The dielectric thickness, t_d, for a PDN MCC should be as thin as possible, $t_d \ll r_c$, such that the inductance of the power transmission line is minimized. Finally, the conductance of the shield is designed to be at least the same conductance as the core to handle any possible magnitude of ground return currents. If the shield has a conductivity, σ_s, the minimum thickness, t_s, is

$$t_s \geq r_c \left(\sqrt{\left(\frac{\sigma_c}{\sigma_s}\right) + 1} - 1 \right). \tag{3}$$

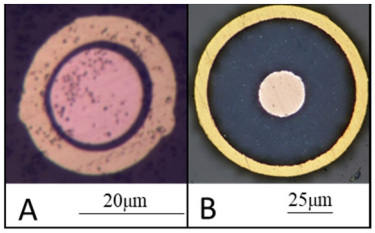

Fig. 5. (A) PDN MCC with 18µm Cu core, 1µm polyimide dielectric and 8µm Au shield. (B) SDN MCC with 25µm Cu core, 30µm PFA dielectric, and 5µm Au shield.

For a power hungry chip-scale packaged component, such as the Kintex 7 FPGA, having 16 power insertion points, $r_c \geq 41\mu m$ for a Cu core, $t_d \leq 3\mu m$ for common manufacturable polymer coatings, and $t_s \geq 28\mu m$ for plated Au [8]. This yields a MCC outer diameter (OD) of 144µm, which should geometrically fit into a pad-to-pad pitch, $p = 400\mu m$. The bare die equivalent of the Kintex 7 FPGA has 685 power insertion points, yielding $r_c \geq 4.4\mu m$ for Cu, $t_d \leq 0.4\mu m$, and $t_s \geq 3.3\mu m$ for plated Au. The total OD of these MCCs would be 16.2µm, much smaller than $p = 170\mu m$.

There are currently no commercial processes available to fabricate any portion of the minimum size PDN MCC described above for the Kintex 7 bare die. Given $p = 170\mu m$, it is not necessary to create processes to fabricate MCCs with these dimensions. Here, we can determine the dimensions based on geometric, rather than electrical constraints. A typical wire bonding processes require that the spacing between pads be greater than or equal to 2.5 times the wire diameter to allow bonding head access to the pads [11], meaning OD ≤ 68µm. Starting with a commercially available insulated wire as the MCC core and dielectric, we can fabricate MCCs for the PDN with dimensions: $r_c = 12.7\mu m$ for Cu, $t_d = 1.3\mu m$ for polymers such as polyimide or polyurethane, and $t_s = 9.2\mu m$ of plated Au, yielding a total OD = 46.4µm. This is done by using thin film deposition methods, such as sputtering or evaporation to deposit an adhesion and seed layer on top of the wire dielectric, then subsequently plating on top of the seed as described in [10]. We do realize that some bare die have a more challenging geometric requirements, $p \sim 60\mu m$ [11]. Given commercially available materials, the smallest coax we are able to fabricate has r_c=5µm, $t_d = 1.3\mu m$, $t_s = 3.5\mu m$, OD = 19.6µm.

B. Signal Distribution

MCC geometry for the SDN is described by the maximum allowable signal attenuation. As a rule of thumb, we require that power attenuation be < 5%. For a 50Ω MCC transmitting a signal over a distance of approximately 10mm, this yields a maximum resistive loss in the core, $R_0 = 1\Omega/mm$. The minimnum r_c is

$$r_c \geq \sqrt{\frac{2}{\pi \sigma_c R_0}}. \tag{4}$$

Equation (5) is used to derive t_d using r_c, the characteristic impedance, Z_0, and the dielectric constant, ε_d.

$$t_d = r_c \left(e^{Z_0 \sqrt{\varepsilon_d}/60} - 1 \right) \tag{5}$$

Like the PDN MCCs, the shield is designed to have at least the same conductance as the core. However, since t_d is no longer negligible, the simplified value of t_s in (3) is no long sufficient to describe the minimum shield thickness for SDN MCCs. Instead, we calculate t_s using (6).

$$t_s \geq \sqrt{r_c^2 \left(\frac{\sigma_c}{\sigma_s}\right) + (r_c + t_d)^2} - (r_c + t_d) \tag{6}$$

For $R_0 = 1\Omega/mm$, this yields the following minimum dimensions for a 50Ω MCC: r_c=3.3µm for a Cu core, $t_d = 9.0\mu m$ for $\varepsilon_d = 2.5$, $t_s = 0.9\mu m$ for plated Au, and a total OD = 26.4µm. It should be noted here that skin depth, δ, decreases proportionally with the square root of frequency and higher resistive loss occurs when the t_s or $r_c < \delta$. For that reason, we ensure that r_c and $t_s \geq \delta$. For example, the SDN may contain high speed digital components, such as a DDR3, may have an I/O bus operating at 800 MHz. At this frequency, $\delta = 2.3\mu m$ in the Cu core, and $\delta = 3.4\mu m$ for a plated Au shield, meaning the minimum core dimension from (4) is sufficient to maintain $R_0 = 1\Omega/mm$, but t_s from (6) is not. Therefore, a minimum of 3.4µm of Au must be plated for the shield, requiring a minimum OD = 31.4µm based on electrical requirements for the DDR3 chip.

SDN MCCs for bare die integration are more difficult to fabricate than PDN MCCs. While the shield deposition strategy is the same, the SDN MCCs require a very thick dielectric coating compared to PDN MCCs. Some wire manufacturers are willing to custom deliver a 25µm Cu core wire with 30µm of a dielectric ($\varepsilon_d = 2.1$), which yields a 50Ω SDN cable with OD = 93µm. This is a sufficient for integrating high frequency signals for chip-scale packages, typically having $p > 300\mu m$. Manufactures are unable to deliver similar coating on a 10µm Cu wire because the core has insufficient tensile strength to survive the extrusion process used for polymer deposition.

To fabricate SDN coax smaller than p for bare-die integration, we coat 10µm Cu wires with Parylene, a polymer deposited using a chemical vapor deposition (CVD) process. Wires coated using CVD processes are exposed to far less tensile strain than enameling or extrusion processes. We are currently investigating how scalable this coating process may be. An SDN MCC with a 10µm core would yield a total OD of 54.5µm. For the smallest bare die, OD < p = 60µm, but this will require clever stripping and bonding processes and hardware development because 2.5OD ≥ p.

V. Integration

The shield and the dielectric must be stripped away from the MCCs prior to bonding both the core and the shield to electrical contacts on the substrate. We envision the addition of specialized hardware to a commercial wire bonder that would be capable of performing automated feed, strip and core bonding. The shield bonding process could be done on the same tool, but is currently performed on a separate solder jetting tool after the coax cores are bonding.

A. Stripping

We employ two separate thermal processes for stripping the core and the shield, illustrated in Fig. 6. For the shield removal, we leverage a process already built into common ball bonding tools that releases a plasma discharge, called electric-flame-off (EFO) [11]. When this EFO discharge is applied to an MCC, there is a high degree of selectivity in melting and peeling back the shield, leaving the underlying layers exposed.

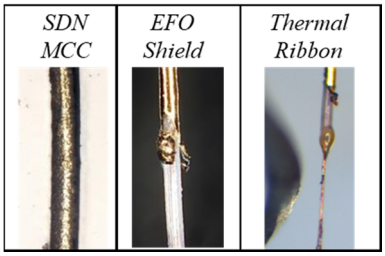

Fig. 6. Stripping process for an SDN MCC with 10µm Cu core, 12µm Parylene dielectric and 2µm Au shield.

The EFO spark is followed by contact with a joule-heated kanthal-based thermal ribbon to melt the dielectric. This process drives the types of materials we can choose for the dielectric. For the PDN MCCs, thermoplastic enamel formulations with operating temperatures of at least 180°C, such as solderable polyester and polyurethane, survive EFO shield stripping processes without charring and seed layer deposition during coax fabrication without melting. For SDN MCCs, PFA and Parylene have shown resilience during stripping and fabrication and have working temperatures ratings > 260°C.

The stripping parameters used during shield and dielectric stripping are significantly different for the PDN and SDN MCCs due to the different cross sectional geometries. In the case of PDN cables, the EFO discharge alone can be sufficient to remove both the shield and the dielectric. EFO spark parameters need to be optimized for each type of MCC. If power settings are too low or the shield metal is thick, full circumferential removal of the shield will not be achieved. If settings are too high or shield metal is thin, the core of the MCC may cleave. For a PDN MCC with a Cu core, r_c = 8.9µm, the Au platine thickness should be 6.4µm < t_s < 10µm. This yields a PDN MCC with 33µm < OD < 40µm.

For SDN MCCs, the shield is reliably removed using the EFO spark. For Parylene N and PFA dielectrics, no decomposition or charring is observed when the spark is applied. For 10µm < r_c < 20µm, full circumferential removal of the shield is observed for plated Au 2µm < t_s < 5µm. This is sufficient to meet most electrical requirements between 400MHz and 2.5GHz without significant skin effect loss. Following the EFO shield stripping step, the dielectric is melted, leaving the core exposed and available for ultrasonic bonding.

B. Bonding

Bonds to the substrate are made using ultrasonic welding. In an automated bonder, the stripped portion of the wire will be fed through a capillary similar to a ball bonding head. The core bond closely resembles the second bond in a ball bonding process. The strength of the bond depends highly on the substrate hardness, core diameter, cleanliness of the wire and cleanliness of the substrate. Bonding parameters are optimized for each substrate and core diameter combination. For Cu cores with r_c > 8.9µm bonded to FR4 or ceramic substrates with electrical contacts made using electroless Ni/ electroless Pd/ immersion Au (ENEPIG) processing, typical bond strength is greater than 3g. While the ultrasonic bond is sufficient to fully attach the core, we often reinforce the bond with a solder ball dispensed from a laser solder jetting tool, which has a mean bond shear strength of 115g.

The shield bonding strategy varies depending on the module configuration. Fig. 7 shows two shield bonding concepts for the interposer configuration, ultrasonic bonding and jetted solder ball attach. The advantage to ultrasonic bonding is that the core and the shield bonding can theoretically be attached using the same tooling, limiting tool sets and fabrication time required for integration. This technique is more likely to work with rigid and/or thin dielectrics as the ultrasonic energy needs to be transmitted through the dielectric to the MCC-substrate junction. Laser solder jetting will guarantee strong bonds, but may require more time in fab because two processing tools are needed. It is also essential that the shield of the MCC be in close proximity to the substrate at the bonding location because the substrate acts as a thermal sink for the jetted solder. Once the concept used for shield bonding is finalized, additional geometric design constraints can be written into the automated routing code.

There are two concepts for shield attachment in dead-bug configuration. First, Au wire bonds can be made directly bridging the MCC shield to a substrate contact. Second, the dam/fill/ground concept requires that core connections are insulated using conventional dam and fill processes prior to grounding. The dams should be deposited prior to the MCC attachment. The custom routing software will need to incorporate geometric design contraints based on the dam geometry. After all of the cores have been attached, the dam is filled to insulate the core contacts. Conductive epoxy or ink is then used to connect the shields to the ground contact points. These materials can either be printed or glob topped.

VI. Performance

We have employed the methods discussed above to install MCCs onto characterization substrates to measure MCC and joint performance across a range of frequency. A complete discussion on RF characterization, modelling, and test methods can be found in [8]. To date, we have measured 24 joints for both PDN and SDN MCCs. The average inductance is 103.73 pH. Joint inductance tolerance will vary based on application, but the characterization fixture requires joint inductances to be less than 300 pH. The characteristic impedances of PDN MCCs measured between 3.30 – 7.30Ω, suffienctly low for most power distribution networks and typical lengths of the cables.

For SDN MCCs, we measured insertion loss and crosstalk because the MMS platform design assumes these

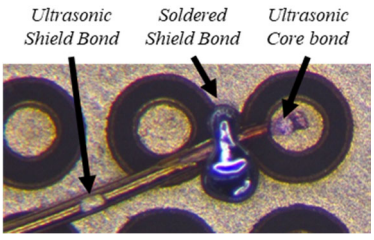

Fig. 7. Two shield attachment methods demonstrated for the interposer configuration

values are negligible compared to standard wire bonds or trace interconnects found in RDLs. Table 1 shows a summary of the data collected for a 50Ω MCC. Measurements were taken up to 36 GHz, with resonant peaks occurring above 10 GHz, likely due to small reflections caused by attenuation in the cables and joints. The max insertion loss at 36 GHz is -0.16 dB. This corresponds to a power loss of 2.5% well below our target of 5.0%.

Crosstalk measurements for a pair of 50Ω SDN MCC compared to a pair of bare Au bond wires can be seen in Fig. 8. The pitch between bare wires and SDN MCCs is 500µm. At 10 GHz, crosstalk between bare Au is -12.6 dB and crosstalk between SDN MCCs is -45 dB. We observe an improvement with MCCs due to the shield which protects the signals from electromagnetic interference. Additionally, we observe fewer resonant peaks from 2.0-4.5GHz in SDN MCCs compared to bare Au wires because the Au wire is not impedance matched. We note that for this test the SDN MCCs were longer than the Au wire, 20 mm and 4 mm, respectively. For future tests, we plan to match lengths for a better comparison.

VII. Conclusions and Future Work

The MMS packaging platform has the potential to greatly accelerate packaging of complex microelectronic devices. The ability to install shielded MCCs to connect disparate components greatly reduces the number of design, simulation and redesign cycles compared to conventional packaging methods. Initial crosstalk measurements confirm that shielded interconnects show two to three orders of magnitude greater signal isolation than bare wires over a wide frequency range. The incorporation of geometric and electrical design constraints into custom wire routing software enables automation of the MMS layout procedure and allows us to directly route the rat's nest structures from ECAD software.

In this work, we have laid the foundation to enable the MMS packaging platform, conceptualizing the configurations and electrical design criteria, fabricating raw MCC materials with a wide impedance range and establishing MCC stripping and installation techniques. Our current work focuses on finalizing MCC material selection and establishing repeatable, reliable, and scalable fabrication strategies. Custom hardware compatible with a commercial wire bonder for MCC feed, strip and bonding is in development. The modified bonding tool will be capable of importing the routing information and relevant for ordered placement of all interconnects from the routing software. This will enable fabrication of the first MMS chip-scale SiP in the interposer configuration with a couple of years.

TABLE I. 50Ω MCC Performance with Frequency

Frequency	Au Wire	50Ω MCC		
	Crosstalk (dB)		*Insertion Loss (dB/mm)*	*Power Loss*
200 MHz	-55	-77	0.003	0.009%
400 MHz	-47.5	-71.7	0.005	0.0025%
800 MHz	-40	-63	0.006	0.0036%
2 GHz	-14.8	-54	0.02	0.04%
10 GHz	-12.6	-45	0.06	0.36%

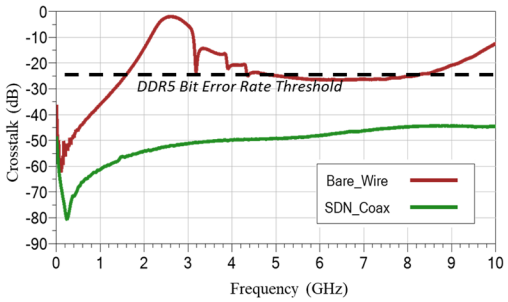

Fig. 8. Crosstalk measurements for a 50Ω MCCs with OD = 83µm compared to 25µm Au wire bonds.

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