Vertical GaN Fin Transistors for Power and RF Applications

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***Abstract*—While lateral HEMTs have traditionally dominated the GaN device market, they are still limited by issues such as current collapse and thermal management. These stem from device structures where current conduction takes place near the surface and is therefore highly dependent on surface conditions. To counteract these limitations, it is necessary to shift from lateral devices to those utilizing vertical current flow. These allow for bulk heat dissipation, area independent breakdown, and reduced dependence on surface states. Here we present our work on creating fin based vertical GaN transistors for 200 V Ka band operation and medium-voltage (600-2000 V) power applications.**

By employing a variable-fin-width based structure, we are able to use device level threshold voltage engineering to study its effects on improving radio frequency (RF) device linearity. We also demonstrate vertical power transistors with extremely high current density by using a bulk GaN substrate, increasing the drift region to accommodate the larger voltages, and increasing the gate length.

***Keywords*—RF Transistors; Power Transistors; Vertical GaN FET**

I. Introduction

Gallium nitride (GaN) based devices have seen great success in recent years. Thanks to its wide bandgap and excellent transport properties, it is ideally suited for higher power applications where it can support high breakdown fields. While the high electron mobility transistor (HEMT) is the most common architecture for GaN transistors as it allows for high frequency operation and large current densities, it is not without its limitations. Due to its tight confinement of electrons close to the device surface and high fields near the gate that cause trapping effects, HEMTs tend to suffer from current collapse [1], [2]. Additionally, the tight current confinement results in significant self-heating that further degrades RF and power performance [3]. While success has been shown with field-plates to reduce trapping and improve breakdown [4], [5] and alternate substrates have been explored such as silicon carbide (SiC) or diamond for improved thermal management [6], these solutions complicate device design and optimization.

As an alternate solution to the limitations surrounding HEMTs, we present a vertical transistor structure that provides several advantages when compared to its lateral counterparts. As seen in Fig. 1, this design uses etched fins to confine the current in the vertical direction with the conductivity of the fin controlled by the gate bias. With this design, there are two options for current collection: a truly vertical device with a backside drain contact, or a quasi-vertical device with all contacts on the same surface. In a quasi-vertical structure, a highly doped drain layer is used beneath the fins to collect electrons and allow for all terminals to remain on the top surface. Due to the vertical conduction path, the breakdown voltage of the vertical devices is primarily dependent on growth thickness, not later dimensions, thus providing reduced device area for a given breakdown voltage. Moreover, vertical devices without a 2-dimensional electron gas (2DEG) have improved thermal management because of the increased bulk heat conduction and more uniform heat generation in a drift region with a larger physical volume [7].

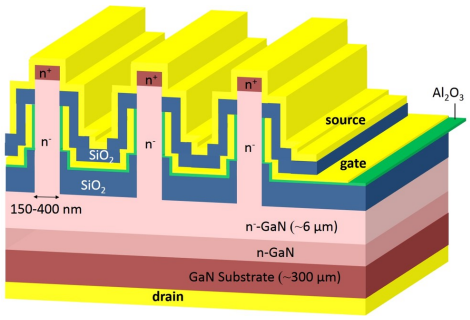

Fig. 1. Schematic for the proposed fully vertical FinFET design. This structure uses a conductive bulk GaN substrate with a backside drain contact. Current is controlled by the gate metal on either side of the fins.

II. Vertical Power Fin Transistor

The transistor presented in Fig. 1 was initially created for medium power (600-2000 V) applications [8], [9]. This fully vertical wafer structure was grown by metal-organic chemical vapor deposition (MOCVD) on 2 in bulk GaN wafer. The layers consist of a 200 nm n+ region doped with silicon (Si) ($5 \times 10^{18}\,\mathrm{cm}^{-3}$) followed by an 8 µm lightly doped ($2 \times 10^{16}\,\mathrm{cm}^{-3}$) n-type drift region, which allows the device to achieve up to 2000 V breakdown. The final layer is 300 nm thick and heavily Si doped ($5 \times 10^{18}\,\mathrm{cm}^{-3}$) to allow for lower contact resistance. This vertical device has been demonstrated to operate at 5 A and breakdown of 1200 V for power switching applications [9].

III. RF Device Fabrication

The design used for the RF devices has been adopted from the vertical power transistor structure. By shrinking the gate length from 1 µm to 100 nm, we can expect significantly

improved high frequency performance. Additionally, with the aim of 200 V breakdown, the drift region can be reduced, thus further reducing on resistance. Finally, a new fabrication process is designed to reduce parasitic capacitances between the source and gate and allow for improved yield when scaling down device dimensions.

The wafers used in the fabrication of vertical RF devices were grown by MOCVD on 2-inch sapphire substrates by MIT Lincoln Laboratory. The structure consists of a 0.5 µm unintentionally doped (UID) GaN buffer followed by a 3 µm heavily Si doped ($5 \times 10^{18}\,\mathrm{cm}^{-3}$) drain layer, a lightly Si doped ($1 \times 10^{17}\,\mathrm{cm}^{-3}$) drift region, and a 100 nm heavily Si doped ($1 \times 10^{19}\,\mathrm{cm}^{-3}$) cap layer. The drain layer and cap layer are heavily doped to improve the ohmic contacts for the drain and source respectively, and the drift region thickness was chosen to allow for 200 V breakdown.

Using the methods described in [10] and [8], 100 nm wide fins are defined by electron beam lithography. Then, using a nickel mask, 500 nm tall fins are etched with a Cl_2 and BCl_3 dry etch. After the dry etch, a wet etch of tetramethylammonium hydroxide (TMAH) at 25 % concentration and 85 °C is used to smooth the sidewalls.

After the fin formation, a 15 nm Al_2O_3 gate dielectric is then deposited through atomic layer deposition (ALD) and annealed at 400 °C. To form the sidewall gate, molybdenum is deposited by sputtering, which provides a more conformal coverage than metal evaporation. After the metal deposition, a SiO_2 sidewall passivation layer is deposited by using a plasma enhanced chemical vapor deposition (PECVD) system with a tetraethoxysilane (TEOS) Si precursor. This results in a zero-stress, conformal oxide layer. With these layers deposited on the GaN surface and fin sidewalls, a highly anisotropic SF_6/O_2 dry etch is used to remove the gate stack from the horizontal surfaces while the oxide coating protects the molybdenum on the sidewalls from any non-vertical etch components. This process can be seen in Fig. 2 where the residual "L" shaped gate metal is observed in the tilted scanning electron microscope (SEM) image. This process of gate formation has the advantage of not being limited by photolithography, and is instead only limited by dry etching control.

To protect the fins during subsequent processing, a sacrificial oxide layer is deposited so that deep GaN etches can be performed for mesa isolation and drain layer access. These etches again use a Cl_2/BCl_3 dry etch chemistry and a nickel (Ni) hard mask. Once the deep etching is complete, the oxide layer is removed.

With the vertical design, it is necessary to have an insulator between the source metal on the tops of the fins and the gate on the sidewalls. This is done using a geometry based planarization and etch-back process. To first planarize the fin surface, another conformal SiO_2 layer is deposited such that the sidewall growth is enough to span the gap between the fins. By growing an oxide thick enough that the two opposing growth fronts from the sides of adjacent fins merge, the degree of planarization is substantially improved. With thicker oxide layers, the oxide surface continues to flatten. This can be seen

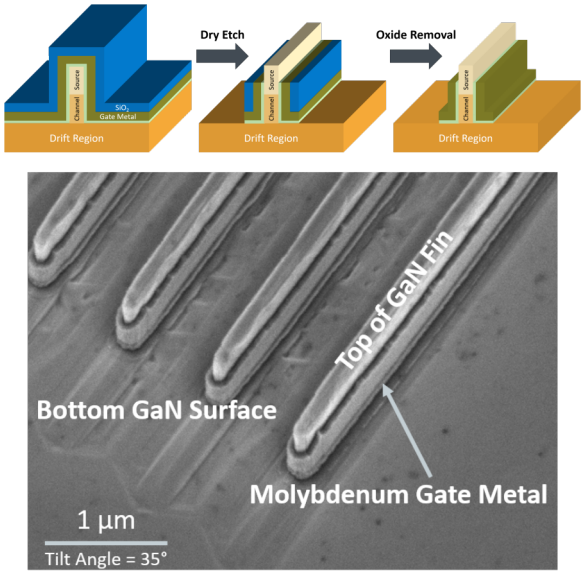

Fig. 2. (Top) Cross-sectional schematic of gate formation. After conformal coatings of the gate oxide (light green), gate metal (dark green), and oxide sidewall passivation layer (blue), a dry etch is used to remove the material deposited on the horizontal surfaces. A wet etch is then used to remove the oxide coating. (Bottom) SEM image of the fins with sidewall gate deposition. The "L" shaped gate remains after removal of the oxide layer.

in Fig. 3 where the densely spaced fin allows the sidewall growth to merge much faster than the sparser spacing in the bottom image, which results in a flatter oxide. Once sufficient planarization is achieved, a CF_4/O_2 based dry etch can be used to etch back the oxide until the tops of the fins are exposed but the gate metal remains buried.

With the fins exposed the wafer is coated in 8 µm of photoresist to cover all devices and provide isolation for the probe pads. Using conventional photolithography, vias are opened to the source, gate, and drain layers and the resist is then hardened using a deep UV cross-linking process to prevent thermal reflow. It is then cured at 225 °C to form a permanent dielectric layer. Ti/Al contacts to the GaN are deposited through sputtering for via filling and defined through wet etching. A completed device schematic and cross section is shown in Fig 4.

IV. Discussion

A major advantage of this fin based approach is the ability to tune the threshold voltage of the device by adjusting the fin width. With a narrower fin, the schottky junction formed by the gate metal is able to fully deplete the fin and cut off current. By biasing the gate, the depletion region shrinks and accumulation regions form on either side of the fin, thus allowing current to flow. With sufficiently narrow fins, this causes the threshold voltage to increase enough that the devices are normally-off, providing a major advantage of the traditionally normally-on HEMTs.

As explored in [11], the large signal linearity of lateral fin transistors can be improved through device level threshold voltage (V_T) engineering. When deriving the output signal for

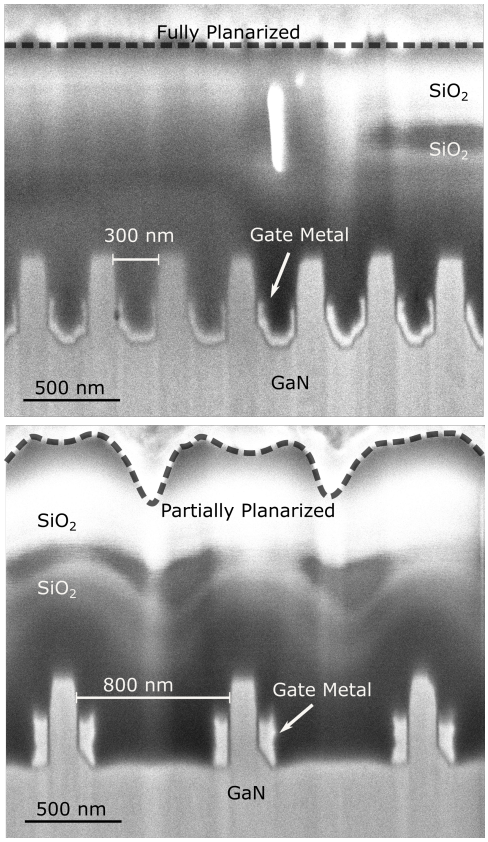

Fig. 3. (Top) Cross-sectional SEM of densely spaced fins with sufficient oxide thickness to fully planarize the oxide surface. (Bottom) Cross-sectional SEM of sparsely spaced fins where the oxide has not fully merged between fins. Further growth is expected to lead to the same degree of planarization as in the upper image. The color variations in the regions labeled SiO_2 are due to charging effects of the insulating oxide.

a transistor amplifier, it can be shown that the harmonics and intermodal distortion depend on the first and second derivatives of the transconductance, g'_m and g''_m respectively. We can therefore create more linear transistors by minimizing these quantities. Since the peaks and valleys of g'_m shift with the threshold voltages, if we utilize the threshold voltage tuning capabilities on a fin-by-fin basis, we can tune each fin such that the peaks destructively interfere with one another. The resulting transistors acts as many optimized devices working in parallel and creates a more linear transistor. Using lateral nano-fin devices, this has shown a 20 dB reduction in harmonics, and a third order intercept point (OIP3) increase of 6dB [11].

With major processing steps completed, further optimization is still necessary. Due to the photoresist dielectric layer's maximum temperature of $250\,^{\circ}\mathrm{C}$, it is not possible to anneal the ohmic contacts, which limits their performance. To counter that, the use of a thicker ($300\,\mathrm{nm}$) very heavily doped ($1 \times 10^{20}\,\mathrm{cm}^{-3}$) molecular beam epitaxy (MBE) grown cap layer is being explored. The increased contact area and reduced tunneling barrier thanks to increased doping should reduce the contact resistance and improve device performance. Alternatively, Cr/Au based nonalloyed contacts to n-GaN have been reported [12] that may be explored.

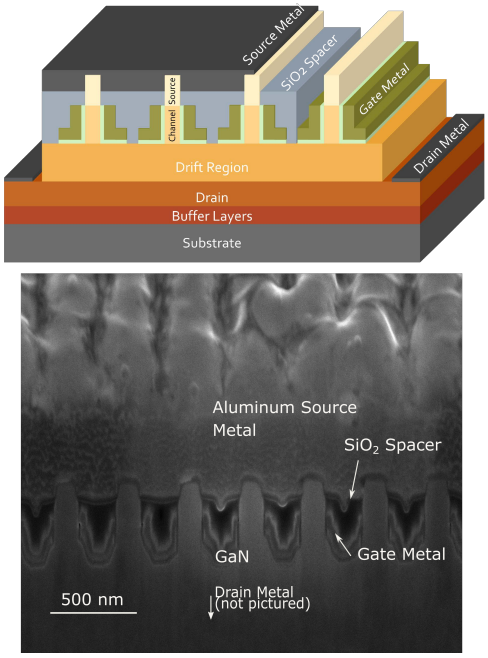

Fig. 4. (Top) Schematic of final device structure. (Bottom) SEM cross-sectional image of final structure. Due to the thickness of the drift region, the drain layer could not be shown.

V. Conclusion

Vertical GaN fin transistors have been adopted from power-switching devices and are being explored for RF applications. The devices have been optimized to reduce parasitic capacitance and scale device dimensions. Thanks to the unique vertical fin design, it is possible to implement device level threshold voltage engineering to improve the linearity of the devices.

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