



ARL-TR-8742 • JULY 2019



# Monolayer Molybdenum Disulfide Common-Source Amplifiers on Rigid and Flexible Substrates

by Alex Mazzoni, Matthew Chin, Robert Burke, Katherine Price, Michael Valentin, and Sina Najmaei

Approved for public release; distribution is unlimited.

## **NOTICES**

### **Disclaimers**

The findings in this report are not to be construed as an official Department of the Army position unless so designated by other authorized documents.

Citation of manufacturer's or trade names does not constitute an official endorsement or approval of the use thereof.

Destroy this report when it is no longer needed. Do not return it to the originator.



# **Monolayer Molybdenum Disulfide Common-Source Amplifiers on Rigid and Flexible Substrates**

**by Alexander L Mazzoni, Katherine M Price, and Michael D Valentin**  
*Oak Ridge Associated Universities (ORAU) Maryland*

**Matthew L Chin and Sina Najmaei**  
*Sensors and Electron Devices Directorate, CCDC Army Research Laboratory*

**Robert A Burke**  
*General Technical Services, LLC*

## REPORT DOCUMENTATION PAGE

*Form Approved*  
*OMB No. 0704-0188*

Public reporting burden for this collection of information is estimated to average 1 hour per response, including the time for reviewing instructions, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the collection information. Send comments regarding this burden estimate or any other aspect of this collection of information, including suggestions for reducing the burden, to Department of Defense, Washington Headquarters Services, Directorate for Information Operations and Reports (0704-0188), 1215 Jefferson Davis Highway, Suite 1204, Arlington, VA 22202-4302. Respondents should be aware that notwithstanding any other provision of law, no person shall be subject to any penalty for failing to comply with a collection of information if it does not display a currently valid OMB control number.

**PLEASE DO NOT RETURN YOUR FORM TO THE ABOVE ADDRESS.**

<b>1. REPORT DATE (DD-MM-YYYY)</b> July 2019		<b>2. REPORT TYPE</b> Technical Report		<b>3. DATES COVERED (From - To)</b> 1 June 2017–31 May 2019	
<b>4. TITLE AND SUBTITLE</b> Monolayer Molybdenum Disulfide Common-Source Amplifiers on Rigid and Flexible Substrates				<b>5a. CONTRACT NUMBER</b>	
				<b>5b. GRANT NUMBER</b>	
				<b>5c. PROGRAM ELEMENT NUMBER</b>	
<b>6. AUTHOR(S)</b> Alex Mazzoni, Matthew Chin, Robert Burke, Katherine Price, Michael Valentin, and Sina Najmaei				<b>5d. PROJECT NUMBER</b>	
				<b>5e. TASK NUMBER</b>	
				<b>5f. WORK UNIT NUMBER</b>	
<b>7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)</b> CCDC Army Research Laboratory* ATTN: FCDD-RLS-RL Adelphi, MD 20783-1138				<b>8. PERFORMING ORGANIZATION REPORT NUMBER</b>  ARL-TR-8742	
<b>9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)</b>				<b>10. SPONSOR/MONITOR'S ACRONYM(S)</b>	
				<b>11. SPONSOR/MONITOR'S REPORT NUMBER(S)</b>	
<b>12. DISTRIBUTION/AVAILABILITY STATEMENT</b> Approved for public release; distribution is unlimited.					
<b>13. SUPPLEMENTARY NOTES</b> ORCID ID(s): Alex Mazzoni, 0000-0002-8184-4373; Robert Burke, 0000-0002-1772-9848; Katherine Price, 0000-0001-6120-0020; Sina Najmaei, 0000-0003-4650-1997 * The work outlined in this report was performed while the US Army Research Laboratory (ARL) was part of the US Army Research, Development, and Engineering Command (RDECOM). As of 31 January 2019, the organization is now part of the US Army Combat Capabilities Development Command (formerly RDECOM) and is now called CCDC Army Research Laboratory.					
<b>14. ABSTRACT</b> Using monolayer molybdenum disulfide as the transistor channel material, common-source n-type metal-oxide-semiconductor amplifier circuits are fabricated and tested. Two different load transistor configurations are investigated: a depletion-mode load transistor (gate and source tied together) and a diode-connected load transistor (drain and gate tied together). After transferring from the growth substrate via a potassium hydroxide wet etch process, devices are fabricated on a thermal oxide substrate and on a spin-on polyimide layer. The depletion-mode load transistor devices show a DC voltage gain up to –10 with a supply voltage of 4 V, with the device gain mainly determined by the doping level after the top-gate dielectric deposition. AC voltage gain for both load types is typically –1 to –2.5 at frequencies of 1 kHz to 10's of kilohertz. The AC performance is mainly limited by parasitic resistances and capacitances of the testing setup. Possible solutions to increase the device performance and considerations for future devices are discussed.					
<b>15. SUBJECT TERMS</b> MoS <sub>2</sub> , molybdenum disulfide, 2-D materials, van der Waals monolayers, amplifier, flexible electronics					
<b>16. SECURITY CLASSIFICATION OF:</b>			<b>17. LIMITATION OF ABSTRACT</b>  UU	<b>18. NUMBER OF PAGES</b>  50	<b>19a. NAME OF RESPONSIBLE PERSON</b> Alex Mazzoni
<b>a. REPORT</b> Unclassified	<b>b. ABSTRACT</b> Unclassified	<b>c. THIS PAGE</b> Unclassified			<b>19b. TELEPHONE NUMBER (Include area code)</b> (301) 394-0494

## Contents

---

<b>List of Figures</b>	<b>v</b>
<b>List of Tables</b>	<b>vii</b>
<b>1. Introduction</b>	<b>1</b>
1.1 Review of Common-Source Amplifiers	1
1.2 Depletion-Mode Transistor Load	3
1.3 Diode-Connected Transistor Load	4
<b>2. Methods</b>	<b>6</b>
2.1 MoS <sub>2</sub> Growth Process	6
2.2 Device Substrate Preparation	7
2.3 MoS <sub>2</sub> Transfer Process	8
2.4 MoS <sub>2</sub> CS Amplifier Fabrication Process	8
2.4.1 Depletion-Mode Load Transistor on SiO <sub>2</sub>	9
2.4.2 Diode-Connected Load Transistor and Polyimide Devices	19
2.5 DC Electrical Characterization	21
2.6 AC Electrical Characterization	22
<b>3. Results</b>	<b>22</b>
3.1 DC Electrical Data	22
3.1.1 Back-Gated Testing	22
3.1.2 Top-Gated Testing	24
3.2 AC Electrical Results	31
3.3 Testing Setup Impact	32
<b>4. Conclusions/Future Work</b>	<b>34</b>
4.1 Increasing Gain	34
4.2 Improving Frequency Response	36
4.3 Other Observations	36

<b>5. References</b>	<b>38</b>
<b>List of Symbols, Abbreviations, and Acronyms</b>	<b>39</b>
<b>Distribution List</b>	<b>41</b>

## List of Figures

---

Fig. 1	Common-source amplifier with generic load impedance. Subscript $D$ corresponds to the lower transistor (device). ....	2
Fig. 2	CS amplifier with depletion-mode load transistor. Subscripts $D$ and $L$ correspond to the lower transistor (device) and upper transistor (load), respectively. ....	4
Fig. 3	Common-source amplifier with diode-connected load transistor .....	5
Fig. 4	Diagram of the MoS <sub>2</sub> PV system. The MoO <sub>3</sub> powder and the substrates were loaded in the same alumina boat. The samples were placed on top of the alumina boat, face up. The MoO <sub>3</sub> powder was spread along the base of the alumina boat. ....	7
Fig. 5	Overview of the MoS <sub>2</sub> transfer process .....	8
Fig. 6	CAD drawing used for the CS amplifier with depletion-mode load transistor. The colors represent different layers, with the green representing boundaries of the MoS <sub>2</sub> mesa etch, pink representing the contact metal, cyan representing the top-gate metal, and yellow showing the via to connect the contact and gate layers. ....	9
Fig. 7	Zoomed-in version of the CAD design in Fig. 6. The colors represent different layers, with the green honeycomb representing the MoS <sub>2</sub> channel, pink representing the contact metal, and cyan representing the top-gate metal.....	10
Fig. 8	Example device after the MESA (channel-defining) EBL step. The light blue triangular shapes/conglomerations are areas of monolayer MoS <sub>2</sub> growth. The small dark square in the center is PMMA, which will protect that region of MoS <sub>2</sub> to serve as the channel material of the transistors, while the rest of the MoS <sub>2</sub> will be etched away. ....	11
Fig. 9	Cross section of device after the mesa (channel-defining) etch step ..	12
Fig. 10	Example device after the metal contact EBL step. The light-blue square in the center is a square of MoS <sub>2</sub> that was protected during the mesa etch step and serves as the channel material.....	12
Fig. 11	Example device after the metal contact layer evaporation and liftoff. The residue seen on the left side and top right is left over from the transfer process. Only clean areas of monolayer MoS <sub>2</sub> were targeted for device fabrication. ....	13
Fig. 12	Cross section of device after the metal contact evaporation and liftoff .....	14
Fig. 13	Cross section of device after the top-gate dielectric deposition .....	14
Fig. 14	Etch rates determined prior to the via etching step.....	15

Fig. 15	Example device after the gate via etch step. The larger square in the center is the via etch that enables the connection of the top-gate node with the output voltage node.....	16
Fig. 16	Cross section of device after the via etch step .....	16
Fig. 17	Example device after the gate metal EBL step .....	17
Fig. 18	Example completed device after the gate metal evaporation step .....	18
Fig. 19	Cross section of CS amplifier with depletion-mode load transistor ...	18
Fig. 20	CAD drawing used for the CS amplifier with an enhancement load transistor. The lower transistor has a width of 18 $\mu\text{m}$ , while the upper transistor's width is 6 $\mu\text{m}$ . The location of the via etch is noted by the yellow box.....	19
Fig. 21	Area chosen for device fabrication on the substrate coated with a polyimide layer. The lighter region highlighted by the dashed line is just the polyimide substrate, whereas the darker area has monolayer $\text{MoS}_2$ . .....	20
Fig. 22	Example of a completed amplifier with a diode-connected load on the substrates coated with a polyimide layer. ....	21
Fig. 23	$I_{\text{DS}}\text{-}V_{\text{GS}}$ curve for the bottom transistor (width of 18 $\mu\text{m}$ ) of a CS amp with a diode-connected load, tested in a back-gated configuration. ...	23
Fig. 24	$I_{\text{DS}}\text{-}V_{\text{GS}}$ curve for the load transistor (width of 6 $\mu\text{m}$ ) of a CS amp with a diode-connected load, tested in a back-gated configuration. Note the current is roughly 3 times lower than that of the transistor in the previous image. ....	23
Fig. 25	Cross section of a top-gated $\text{MoS}_2$ device showing the location of fixed positive charge in the gate oxide and how it changes the threshold voltage by attracting electrons to the channel. ....	24
Fig. 26	Si/SiO <sub>2</sub> substrate – device A13 CS transistor – top gated – $I_{\text{DS}}$ vs. $V_{\text{GS}}$ , $V_{\text{DS}} = 100$ [mV] .....	25
Fig. 27	Si/SiO <sub>2</sub> substrate – device A13 CS transistor – top gated – $I_{\text{DS}}$ vs. $V_{\text{DS}}$ , $V_{\text{GS}} = -10, -5, 0, 5, 10$ [V] .....	26
Fig. 28	Si/SiO <sub>2</sub> substrate – device A13 load (depletion) transistor – top gated – $I_{\text{DS}}$ vs. $V_{\text{DS}}$ , $V_{\text{GS}} = 0$ .....	27
Fig. 29	Si/polyimide substrate – device M5 load (enhancement) transistor – $I_{\text{DS}}$ vs. $V_{\text{DS}}$ , $V_{\text{DS}} = 0\text{-}5$ [V], $V_{\text{GS}} = V_{\text{DS}}$ .....	28
Fig. 30	Example load-line analysis of a CS amp with a depletion-mode load transistor.....	28
Fig. 31	Plotted in blue is the output voltage versus the input voltage. The derivative of this blue curve gives the DC gain, plotted in orange. The maximum gain approaches $-3$ at $V_{\text{in}} = -2$ V with a $V_{\text{DD}}$ of 5 V.....	29
Fig. 32	Example load-line analysis of a CS amp with a depletion-mode load transistor.....	30

Fig. 33	Plotted in blue is the output voltage versus the input voltage. The derivative of this blue curve gives the DC gain, plotted in orange. The maximum gain approaches $-9$ at $V_{in} = -0.5$ V with a $V_{DD}$ of 4 V. ....	30
Fig. 34	Example oscilloscope waveform showing the input voltage (green) and output voltage (yellow) at a frequency of 1 KHz .....	31
Fig. 35	Circuit diagram of the CS amplifier including the parasitic capacitances and resistance coming from the testing setup .....	33

## List of Tables

---

Table 1	Summary of the gain and frequency response measured.....	32
---------	--	----

## 1. Introduction

---

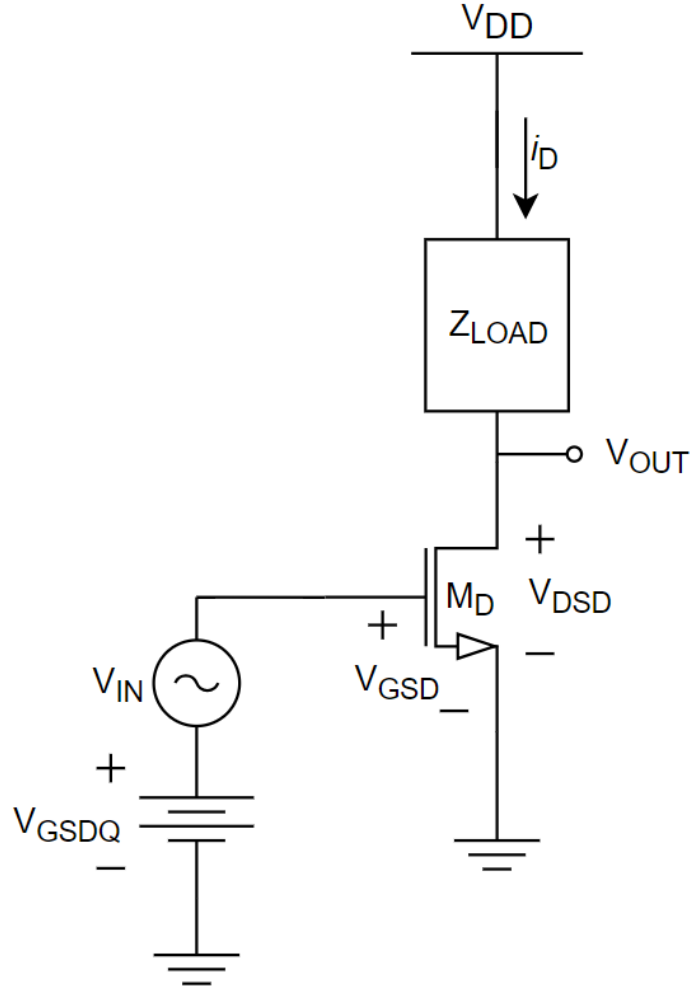
Following the discovery of graphene, researchers looked to other 2-D materials to make up for graphene's main disadvantage for electronic devices—its lack of a bandgap. A heavy focus was placed on molybdenum disulfide ( $\text{MoS}_2$ ), another van der Waals (vdW) material well known in the bulk form for its lubrication and semiconducting properties. At the monolayer limit, it was discovered that  $\text{MoS}_2$  changes from an indirect to a direct bandgap semiconductor at the K-point. The photoluminescence spectrum from monolayer  $\text{MoS}_2$  shows a peak around 1.9 eV; however, this represents the excitonic transition and not the band-to-band transition. Due to the large exciton binding energy in monolayer  $\text{MoS}_2$ , the actual electronic bandgap is around 2.2–2.3 eV, as discussed in detail by Wang et al.<sup>1</sup> The atomic thinness of monolayer materials leads to high mechanical strain limits.<sup>2</sup> This, combined with the respectable mobility ( $\sim 10 \text{ cm}^2/\text{V}\cdot\text{s}$ ) at low dimensionality, provides an avenue for niche applications using  $\text{MoS}_2$ , such as flexible electronics.

Previously, we investigated the impact that growth conditions have on the electrical properties of n-type  $\text{MoS}_2$  metal-oxide-semiconductor (NMOS) field-effect transistors (FETs).<sup>3</sup> Here we take one of the first steps toward making more complicated integrated circuits from monolayer  $\text{MoS}_2$  by creating two-transistor NMOS amplifier circuits. This report details the fabrication and testing of our first-round basic amplifier circuits on both rigid and flexible substrates.

### 1.1 Review of Common-Source Amplifiers

---

The amplifier circuits we chose to make are common-source (CS) amplifiers with two different load transistor configurations: a depletion-mode load transistor with the gate shorted to the source and a diode-connected load transistor (gate tied to the drain). The CS amplifier (Fig. 1) is the most commonly used FET amplifier configuration, analogous to the common-emitter amplifier based on the bipolar junction transistor. The following sections review the analytical expressions for the gain of these transistor amplifier circuits. The book by Gray, Hurst, Lewis, and Meyer<sup>4</sup> was used as a reference for all of the equations relating to transistor and circuit operation.



**Fig. 1 Common-source amplifier with generic load impedance. Subscript <sub>D</sub> corresponds to the lower transistor (device).**

Given a generic load impedance,  $z_L$ , the CS amplifier has the following expression for gain (assuming the transistor is operating in the saturation regime):

$$A_v = \frac{V_{out}}{V_{in}} = -g_{mD} (r_{oD} \parallel z_L). \quad (1)$$

Here  $g_{mD}$  is the transconductance of the MOSFET,  $M_D$ :

$$g_{mD} = \frac{\partial I_{DS}}{\partial V_{GS}} \quad (2)$$

and  $r_{oD}$  is the output resistance of the MOSFET  $M_D$ :

$$r_{oD} = \left( \frac{\partial I_{DS}}{\partial V_{DS}} \right)^{-1}. \quad (3)$$

As Eq. 1 shows, for high gain it is beneficial for  $g_{mD}$  to be large. To see how transistor parameters affect the transconductance, an expression for  $g_{mD}$  can be derived from the MOSFET current equation in the saturation regime:

$$I_{DSAT} = \frac{\mu_n C_{OX} W}{2L} [V_{GS} - V_{th}]^2 [1 + \lambda(V_{DS})] \quad (4)$$

and 
$$g_{mD} = \frac{\partial I_{DSAT}}{\partial V_{GS}} = \frac{\mu_n C_{OX} W}{L} [V_{GS} - V_{th}] [1 + \lambda(V_{DS})]. \quad (5)$$

Here  $\mu_n$  is the channel mobility,  $C_{OX}$  is the capacitance of the gate per unit area,  $W$  is the channel width,  $L$  is the channel length,  $V_{th}$  is the threshold voltage, and  $\lambda$  is the channel length modulation parameter.

Neglecting channel length modulation and using the constant  $K_n$  to account for the transistor parameters, a simplified and useful formula for  $I_{DSAT}$  and  $g_{mD}$  can be derived.

Setting  $K_n = \frac{\mu_n C_{OX} W}{2L}$ , we find

$$I_{DSAT} = K_n [V_{GS} - V_{th}]^2 \quad (6)$$

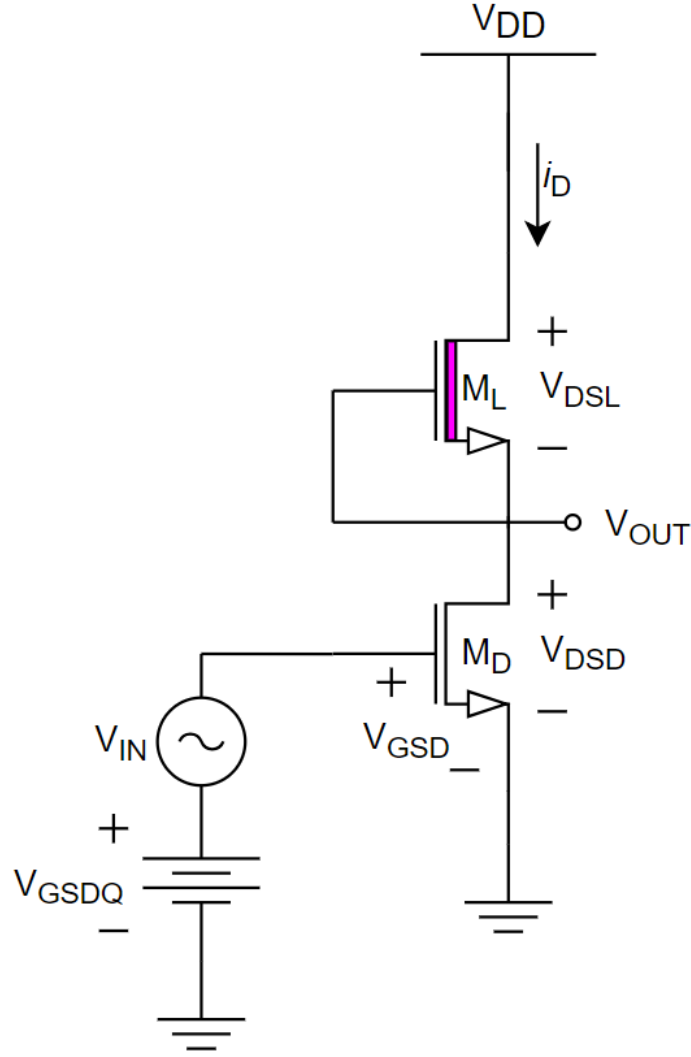
and 
$$g_{mD} = \frac{\partial I_{DSAT}}{\partial V_{GS}} = 2K_n [V_{GS} - V_{th}] = 2\sqrt{K_n} \sqrt{I_{DSAT}}. \quad (7)$$

Again, looking at Eq. 1, for high gain it is also beneficial for  $r_{oD}$  and  $z_L$  to be large. A high  $r_{oD}$  is achieved by operating the transistor in the saturation regime where the  $I_{DS}-V_{DS}$  curve is relatively flat (where the differential resistance is high). It is difficult to implement large load resistors on an integrated circuit to achieve a large  $z_L$ , so transistors are often used as the amplifier load. In the next sections, we look at two possible methods of implementing a transistor as a load in a common-source amplifier configuration.

## 1.2 Depletion-Mode Transistor Load

---

In this configuration (Fig. 2), the gate and source are tied together ( $V_{GS} = 0$ ), meaning modulations in the output node voltage only changes  $V_{DS}$  of the load transistor while  $V_{GS}$  stays constant at 0. For this load transistor to allow substantial DC current to flow, the load transistor needs a threshold voltage that is less than zero, meaning the device is normally on (depletion mode).



**Fig. 2** CS amplifier with depletion-mode load transistor. Subscripts  $D$  and  $L$  correspond to the lower transistor (device) and upper transistor (load), respectively.

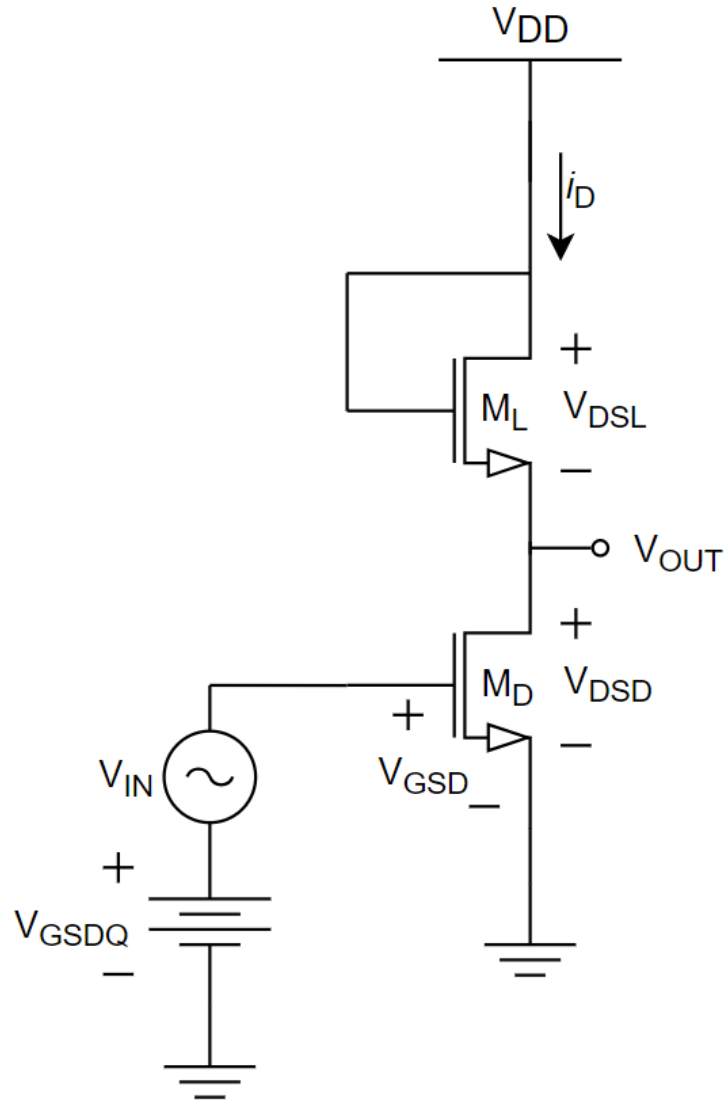
If the threshold voltage is less than zero and  $V_{GS} = 0$ , then the saturation condition for the load transistor ( $V_{DS} > V_{GS} - V_{th}$ ) becomes  $V_{DS} > (-V_{th})$ . When in saturation, its small-signal resistance is  $r_{oL}$  and the expression for the gain of this amplifier becomes

$$A_v = \frac{V_o}{V_i} = -g_{mD} (r_{oD} \parallel r_{oL}). \quad (8)$$

### 1.3 Diode-Connected Transistor Load

In this configuration, the drain and gate of the load transistor are tied together ( $V_{DS} = V_{GS}$ ). The circuit diagram of this configuration is provided in Fig. 3. In this configuration, once the device is on ( $V_{GS} > V_{th}$ ) the saturation condition

$(V_{DS} > V_{GS} - V_{th})$  is always true for  $V_{th} > 0$  and never true for  $V_{th} < 0$ , assuming positive  $V_{DD}$ .



**Fig. 3 Common-source amplifier with diode-connected load transistor**

The simplified formula for gain of a common source amplifier with a diode-connected transistor load is readily achieved by knowing the resistance looking into the source of the load transistor is  $1/g_{mL}$ , which is usually much smaller than  $r_{oD}$ . The formula for the amplifier gain becomes a ratio of the transconductance of the two transistors. Looking back at Eq. 7, the ratio of transconductances becomes a ratio of  $\sqrt{K_n}$  since the same current flows through both transistors. The W/L ratio is the easiest parameter to change and the gain is therefore often presented as proportional to the square root of the W/L ratios.

$$A_v = \frac{V_o}{V_i} = -g_{mD} \left( r_{oD} \parallel \frac{1}{g_{mL}} \right) = -\frac{g_{mD}}{g_{mL}} = -\frac{\sqrt{K_{nD}}}{\sqrt{K_{nL}}} = -\sqrt{\frac{(W/L)_D}{(W/L)_L}}. \quad (9)$$

Comparing these two different load configurations, the main differences are that a depletion-mode load enables a larger output resistance  $r_{oL}$  and gain than the diode-connected load, but requires doping control to achieve the desired threshold voltage less than zero.

## 2. Methods

---

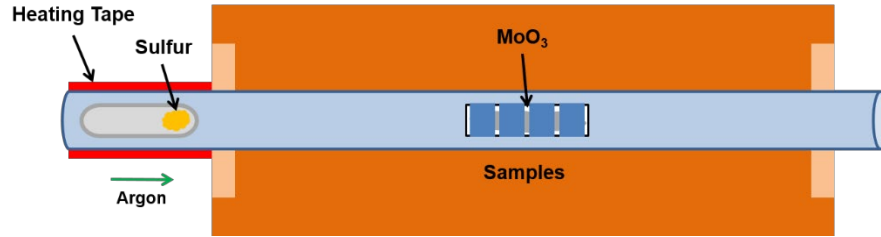
This section outlines our methods used to fabricate and test the CS amplifiers made from monolayer MoS<sub>2</sub>.

### 2.1 MoS<sub>2</sub> Growth Process

---

Prior to growth, highly doped (p<sup>++</sup>) silicon (Si) substrates with a 220-nm thermal oxide were soaked in piranha etch (3:1 ratio of sulfuric acid [H<sub>2</sub>SO<sub>4</sub>]:hydrogen peroxide [H<sub>2</sub>O<sub>2</sub>]) for 15 min, followed by 5-min soaks in deionized (DI) water, acetone, and isopropyl alcohol (IPA). The samples were rinsed with DI water and dried with nitrogen. Afterward, the substrates were treated in an oxygen plasma for 5 min to create a hydrophilic surface.

Four samples (15 mm × 16 mm) were placed face up on top of an alumina crucible (CoorsTek) containing MoO<sub>3</sub> powder (Sigma Aldrich, 99.5%) and loaded into the center of a tube furnace (Fig. 4). 40 μL of Perylene-3,4,9,10-tetracarboxylic acid tetrapotassium salt (PTAS) was spin coated onto the furthest upstream of the four samples at 500 rpm for 5 s, 2,000 rpm for 45 s, and then 4,000 rpm for 15 s to prevent excess PTAS in the corners of the sample. The spun PTAS acts as a seeding layer for growth. The sample we ended up using for these devices was the furthest downstream sample that did not receive any direct PTAS treatment. A second alumina boat with sulfur powder (Sigma Aldrich, 99.98%) was loaded upstream of the MoO<sub>3</sub> powder and substrates. The system was sealed and purged with 200 sccm of argon for 10 min. Afterward, the argon flow rate was reduced to 5 sccm and the tube furnace was heated at a rate of approximately 17 °C/min until it reached its growth temperature. The temperature set point of the heating tape for the sulfur source (250 °C) was set 3 min before the system reached growth temperature (700 °C). Once the growth step was complete (10 min), the heating tape was turned off, the furnace was opened, and the argon flow rate was increased to 200 sccm to quench the growth process. The system was cooled for 25–30 min before unloading the samples from the furnace.



**Fig. 4** Diagram of the MoS<sub>2</sub> PV system. The MoO<sub>3</sub> powder and the substrates were loaded in the same alumina boat. The samples were placed on top of the alumina boat, face up. The MoO<sub>3</sub> powder was spread along the base of the alumina boat.

## 2.2 Device Substrate Preparation

MoS<sub>2</sub> was grown on SiO<sub>2</sub> but was transferred to different substrates for fabrication. Section 2.3 covers the transfer process, while this section covers the device substrate preparation. MoS<sub>2</sub> amplifier circuits were fabricated on two different substrates. The first substrate was a degenerately doped Si wafer with a 300-nm thermal oxide. The second substrate was a Si wafer with a 9- $\mu$ m film of polyimide spun on it. A spin-on polyimide was chosen in order to enable standard fabrication on a rigid carrier wafer, with the ability to peel off the flexible device upon completion.

The specific polymer chosen was HD Microsystems Polyimide PI 2611. This polyimide has an associated optional adhesion promoter VM-651. The polyimide was spun onto a Si wafer at 2,000 rpm for 60 s and then soft-baked on a hot plate at 150 °C for 2 min. To cure the polyimide, the wafer was loaded into a vacuum furnace (IVI) with controlled heat ramping rates. The furnace ramped from room temperature to 250 °C over 1 h, stayed at temperature for 2 h, then took 1 h to cool down to room temperature. According to the data sheet, the polyimide thickness should be approximately 9  $\mu$ m after curing.

A layer of plasma-enhanced atomic layer deposition (PEALD) Al<sub>2</sub>O<sub>3</sub> was deposited on both substrates to serve as the bottom interface of the MoS<sub>2</sub> transistor. First, a 1-nm aluminum (Al) seed layer was deposited via electron beam evaporation (CHA Industries) at a pressure of 1  $\mu$ Torr and then set out in ambient overnight to oxidize. 250 cycles of PEALD (Kurt J. Lesker Company) Al<sub>2</sub>O<sub>3</sub> were then deposited at 200 °C. Both substrates then had a titanium/gold (Ti/Au) marker layer deposited via electron beam evaporation and lift-off to enable location of specific MoS<sub>2</sub> domains for device fabrication.

### 2.3 MoS<sub>2</sub> Transfer Process

---

After MoS<sub>2</sub> growth, the MoS<sub>2</sub> film was transferred from the growth substrate to the substrate used for device fabrication.

While transfer only was necessary for fabrication on the polyimide substrates, we transferred onto new SiO<sub>2</sub> chips to have a more direct comparison between the two substrates. (Material was transferred for both the rigid SiO<sub>2</sub> substrates and the polyimide.)

To protect the monolayer MoS<sub>2</sub> film, a layer of poly(methyl methacrylate) (PMMA) is first spun on the as-grown film. Floating the sample in a solution of 15% potassium hydroxide (KOH) by weight releases the PMMA/MoS<sub>2</sub> film from the Si/SiO<sub>2</sub> chip, leaving the PMMA/MoS<sub>2</sub> film floating in the KOH solution. After release, the PMMA/MoS<sub>2</sub> film is cleaned by moving it through multiple DI water baths using a glass slide (or similar piece of plastic). After cleaning, the PMMA/MoS<sub>2</sub> film is scooped out of the DI water using the desired new substrate. After air-drying, the sample is heated on a hotplate to improve adhesion and then the PMMA is removed with acetone. This transfer process is shown in Fig. 5.

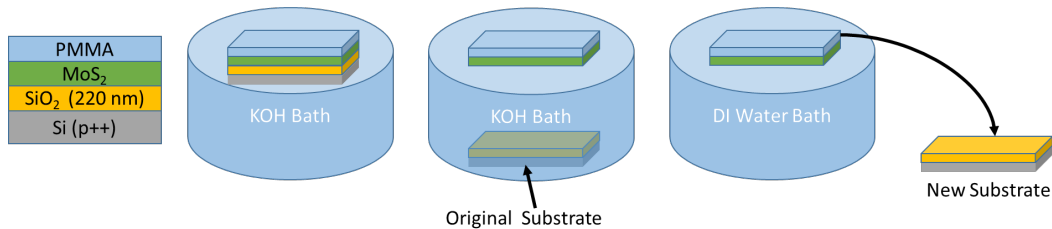


Fig. 5 Overview of the MoS<sub>2</sub> transfer process

### 2.4 MoS<sub>2</sub> CS Amplifier Fabrication Process

---

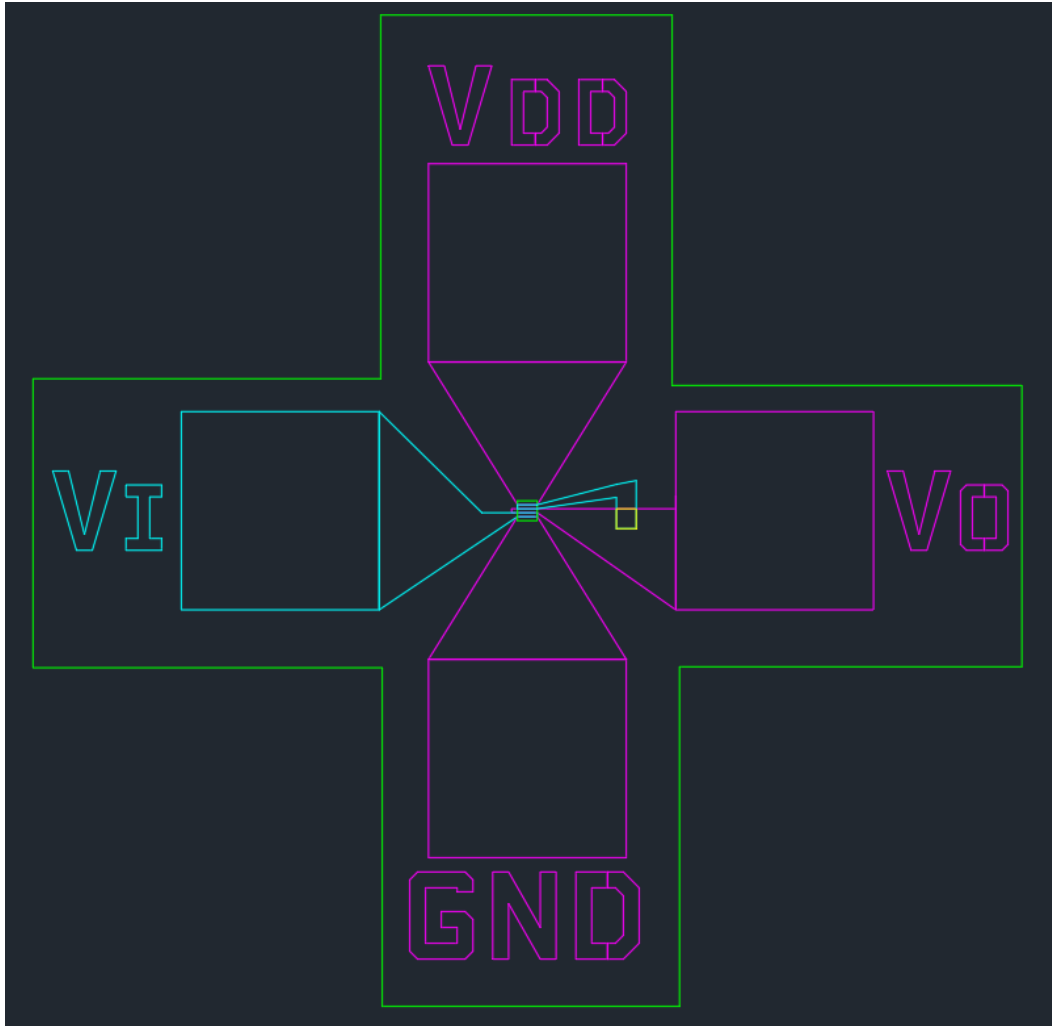
This section outlines the methods used to fabricate the MoS<sub>2</sub> CS amplifiers. As an example, each step of the fabrication of an amplifier with a depletion-mode load transistor is shown.

All patterning for etching and deposition steps was achieved using a PMMA layer defined by a standard electron beam lithography (EBL) process. This process is as follows: PMMA 950 A4 was spun at 2000 rpm, giving a thickness around 300 nm, and baked on a hotplate at 180 °C for 2 min. The base exposure dose used was 850  $\mu\text{C}/\text{cm}^2$  and development was performed in a 10-mL methyl isobutyl ketone (MIBK): 25-mL IPA solution for 75 s, followed by nitrogen drying.

## 2.4.1 Depletion-Mode Load Transistor on SiO<sub>2</sub>

### 2.4.1.1 Computer-Aided Design (CAD)

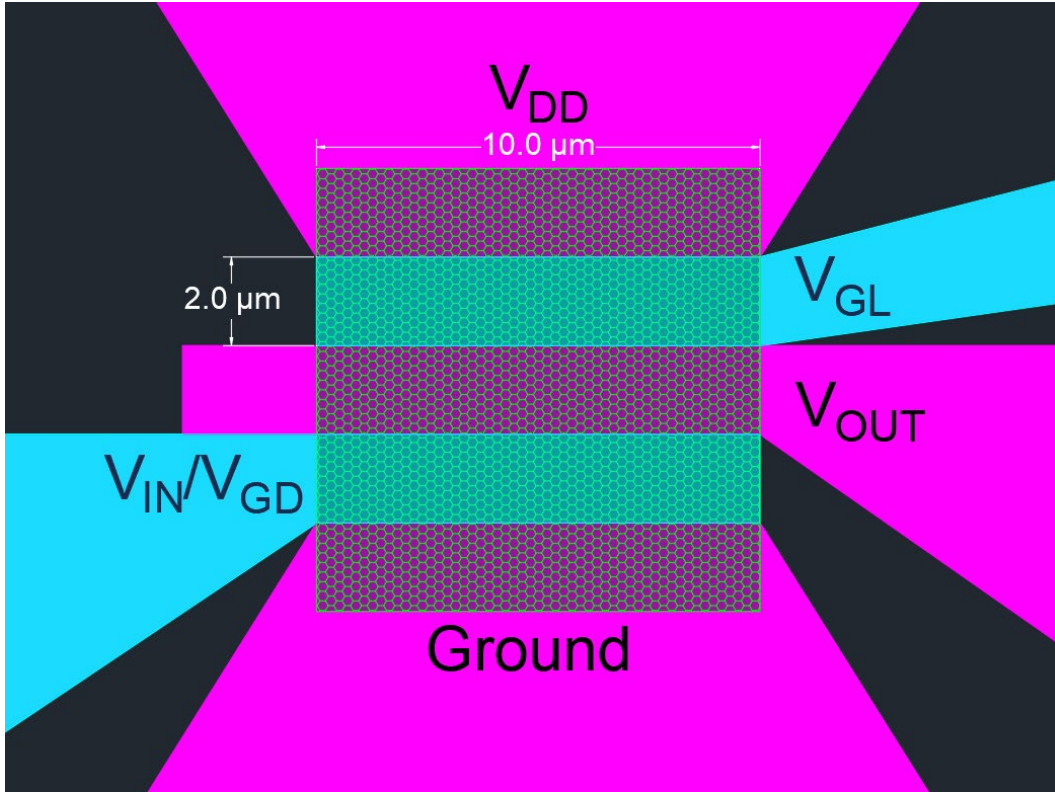
Figure 6 shows an overhead view of the CAD drawing used to fabricate the CS amplifier with the depletion-mode load transistor. The four large squares are probing pads that are 100  $\mu\text{m}$  per side. These pads are labeled corresponding to the same voltage nodes as that of Fig. 2. The colors represent different masks of the fabrication process.



**Fig. 6** CAD drawing used for the CS amplifier with depletion-mode load transistor. The colors represent different layers, with the green representing boundaries of the MoS<sub>2</sub> mesa etch, pink representing the contact metal, cyan representing the top-gate metal, and yellow showing the via to connect the contact and gate layers.

Figure 7 shows the CAD drawing zoomed into the MoS<sub>2</sub> channel region. A 10- $\mu\text{m}$   $\times$  10- $\mu\text{m}$  square of MoS<sub>2</sub> serves as the basis to form two identically sized transistors. The input signal goes into the gate of the lower transistor and the upper

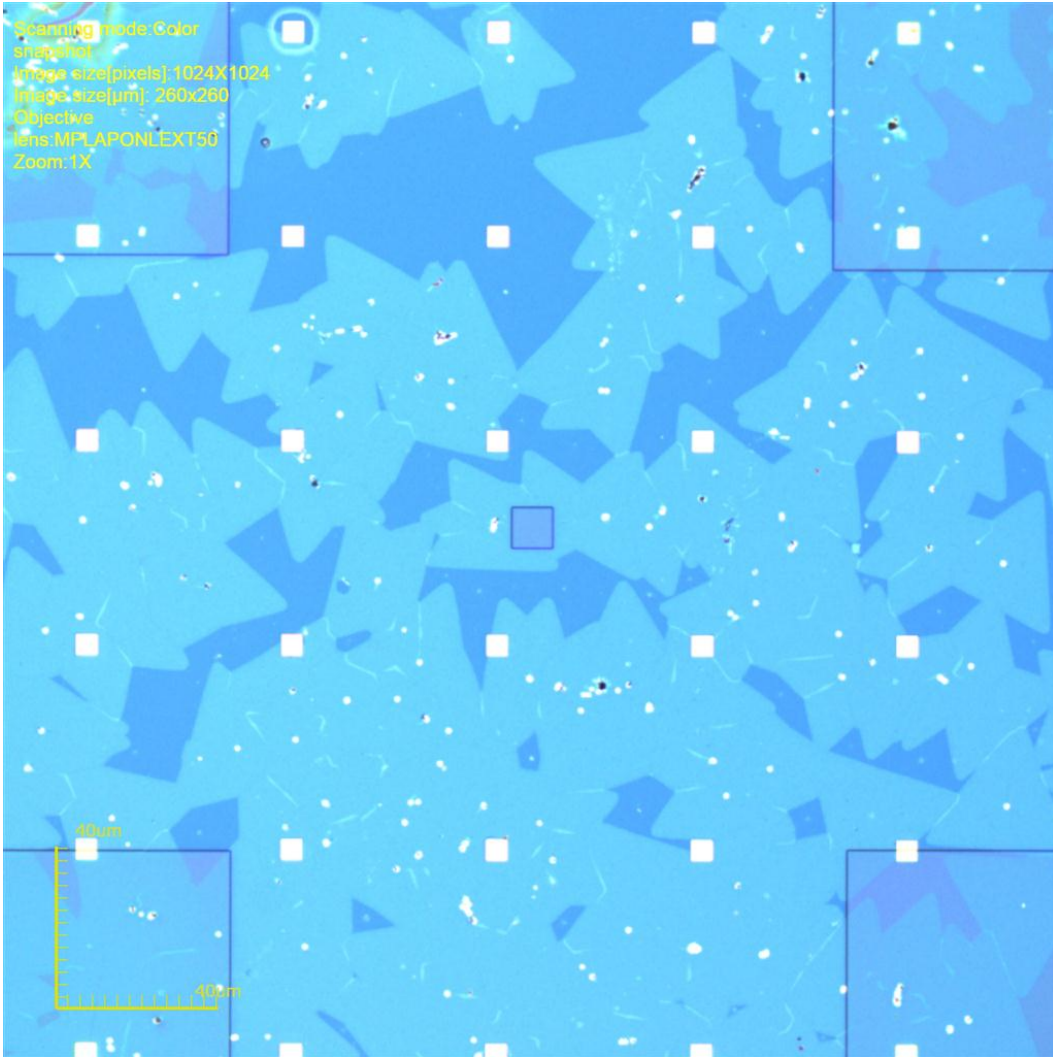
transistor becomes the load. The channel width of these transistors is  $10\ \mu\text{m}$  and the channel length is  $2\ \mu\text{m}$ . The contact width is  $10\ \mu\text{m}$  and the contact length is  $2\ \mu\text{m}$ .



**Fig. 7** Zoomed-in version of the CAD design in Fig. 6. The colors represent different layers, with the green honeycomb representing the MoS<sub>2</sub> channel, pink representing the contact metal, and cyan representing the top-gate metal.

#### 2.4.1.2 Mesa Etch (Channel Definition)

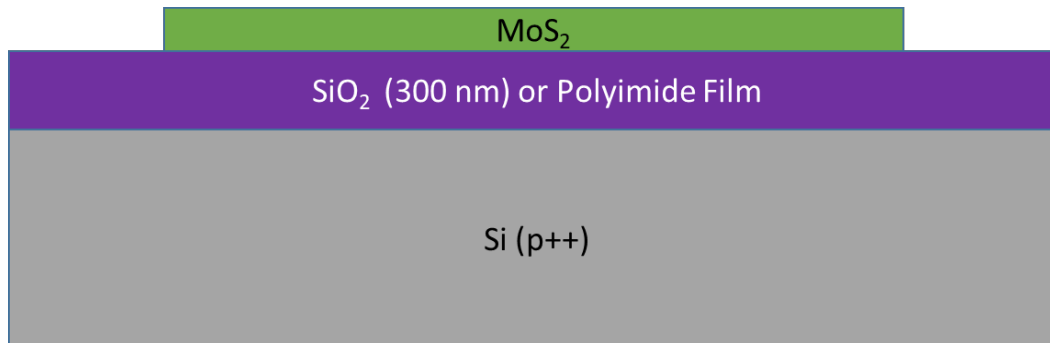
Etching of the MoS<sub>2</sub> is necessary to define the channel to known, specific dimensions and to electrically isolate devices from each other. Looking at Fig. 6, the area inside the large green cross will undergo an etch process to remove the MoS<sub>2</sub>, except for the small square in the center that forms the transistor channel material. Figure 8 shows an example device after the channel definition EBL exposure and development, but before the MoS<sub>2</sub> etch.



**Fig. 8** Example device after the MESA (channel-defining) EBL step. The light blue triangular shapes/conglomerations are areas of monolayer MoS<sub>2</sub> growth. The small dark square in the center is PMMA, which will protect that region of MoS<sub>2</sub> to serve as the channel material of the transistors, while the rest of the MoS<sub>2</sub> will be etched away.

To etch the MoS<sub>2</sub>, a two-step reactive ion etching (RIE) process involving chlorine (Cl<sub>2</sub>) and oxygen (O<sub>2</sub>) plasma was used.<sup>5</sup> The first step was 40 s long and used 15 sccm Cl<sub>2</sub> + 5 sccm O<sub>2</sub> and 250 W of RF power to etch the MoS<sub>2</sub>. A secondary, 200 W pure O<sub>2</sub> etch for 10 s was performed to remove any hardened PMMA from the previous Cl<sub>2</sub> etch step. After the RIE the PMMA was removed with acetone and the sample was rinsed with IPA.

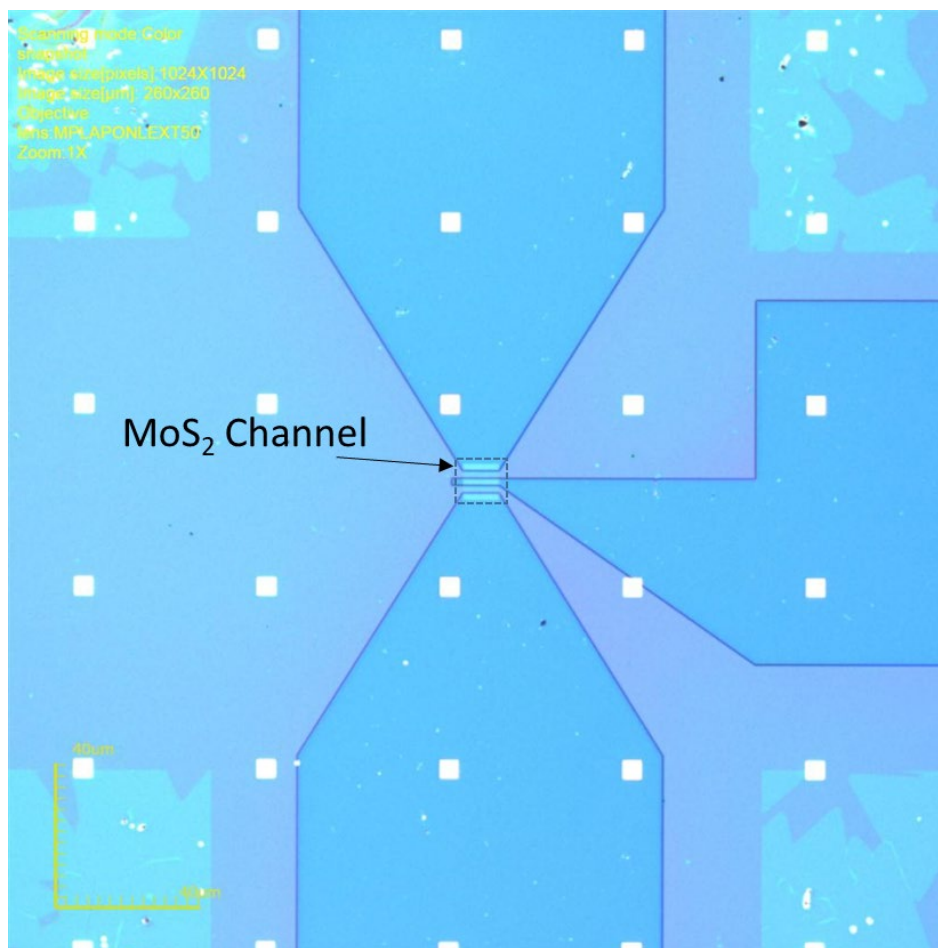
The cross section of the device at this point is shown in Fig. 9.



**Fig. 9** Cross section of device after the mesa (channel-defining) etch step

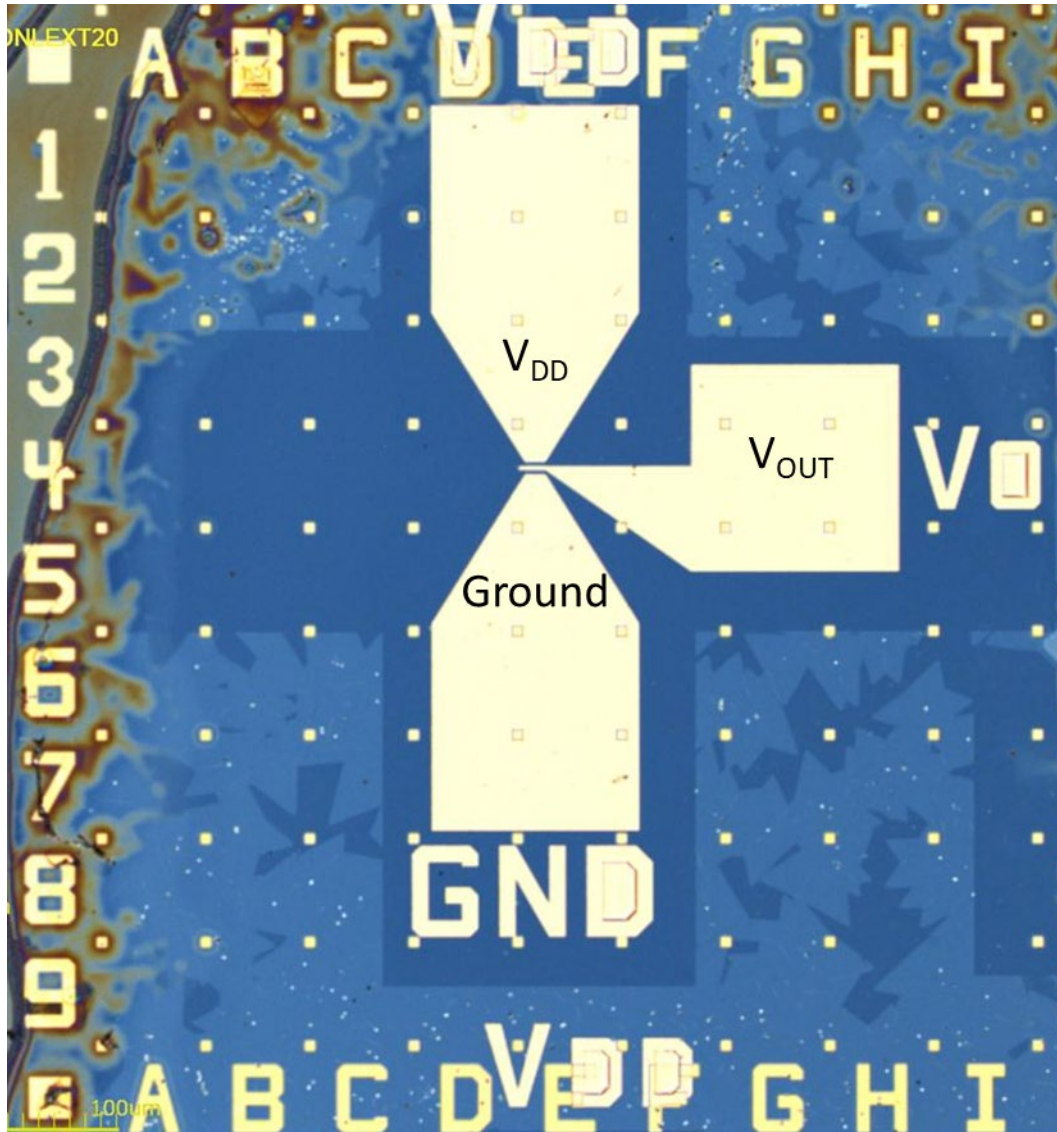
#### 2.4.1.3 Drain/Source Contacts

After the mesa etch (channel definition), the next step is to deposit drain/source contacts to the two transistors. Figure 10 shows the example device after PMMA development for the contact layer.

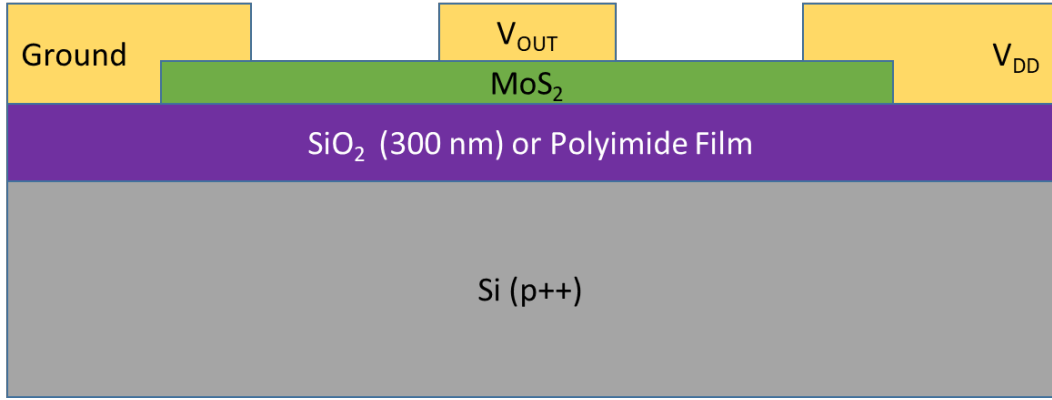


**Fig. 10** Example device after the metal contact EBL step. The light-blue square in the center is a square of MoS<sub>2</sub> that was protected during the mesa etch step and serves as the channel material.

Metal contacts of 20-nm nickel (Ni) followed by 60-nm Au were deposited via electron beam evaporation (CHA Industries) after an overnight pump down and were lifted off in acetone at room temperature. A top-down optical image (Fig. 11) and corresponding cross section (Fig. 12) of the example device after the metal contact step are shown in the following figures.



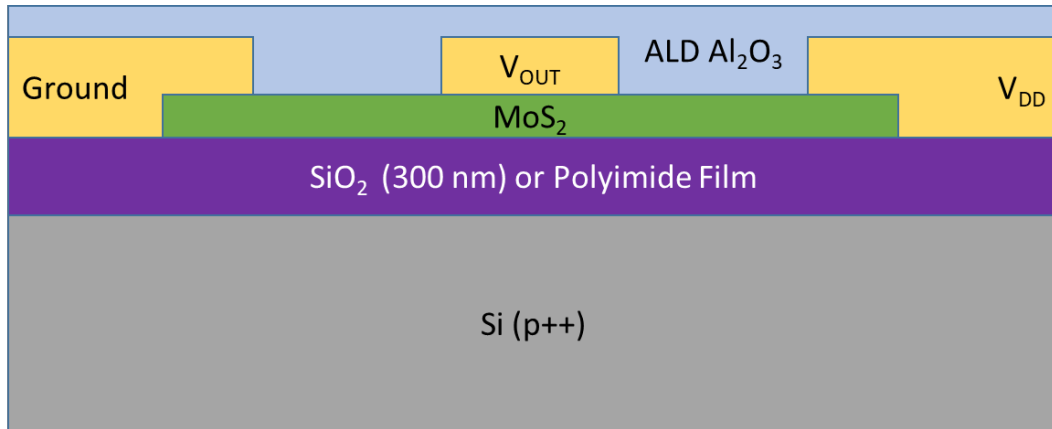
**Fig. 11** Example device after the metal contact layer evaporation and liftoff. The residue seen on the left side and top right is left over from the transfer process. Only clean areas of monolayer MoS<sub>2</sub> were targeted for device fabrication.



**Fig. 12** Cross section of device after the metal contact evaporation and liftoff

#### 2.4.1.4 Top-Gate Dielectric

Following the contact metal, the next step is the deposition of the top-gate dielectric. Seeding atomic layer deposition (ALD) films on 2-D layers is known to be difficult, so we used a metallic seed layer to remedy this.<sup>6</sup> 1 nm of Al was deposited across the whole sample and then the sample was left in ambient for a few hours to oxidize, forming an Al<sub>2</sub>O<sub>3</sub> seed layer. On this seed layer, 250 cycles (22.6 nm) of PEALD Al<sub>2</sub>O<sub>3</sub> was deposited (Kurt J. Lesker Company) at 200 °C. The cross section of the device at this point is shown in Fig. 13.

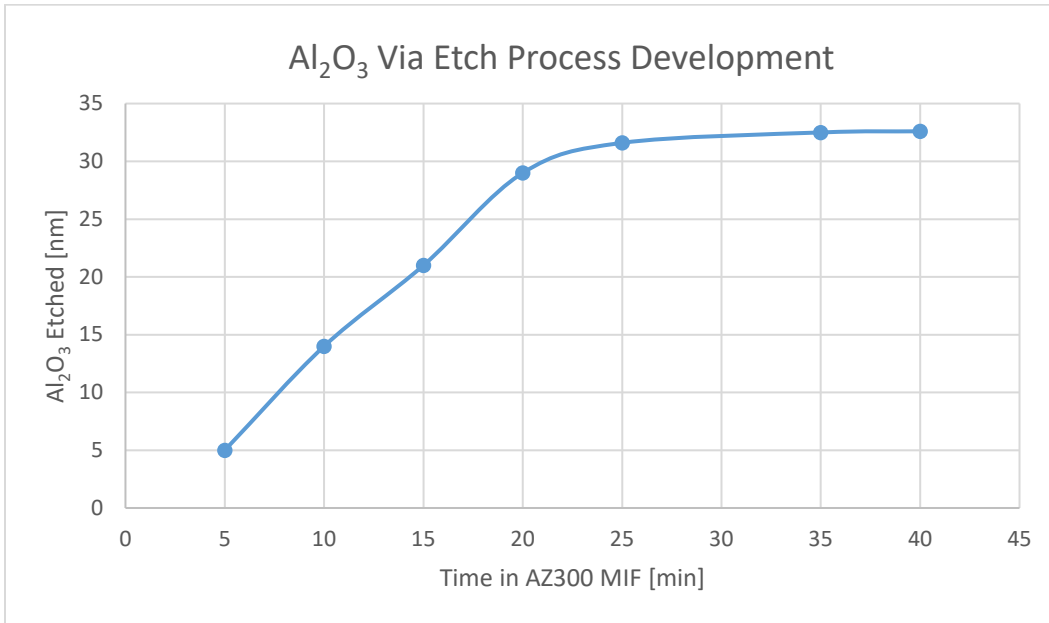


**Fig. 13** Cross section of device after the top-gate dielectric deposition

#### 2.4.1.5 Via Etch

The next step is to create a via to connect the drain/source contact layer to the gate layer. To etch the Al<sub>2</sub>O<sub>3</sub> to make the via hole, AZ300 MIF developer (2.38% tetramethylammonium hydroxide [TMAH] by weight) was used. Along with the actual samples, a dummy SiO<sub>2</sub> chip was loaded into the Al seed layer evaporation and the 250 cycle PEALD run. This chip served as a process development sample to determine etch rates of Al<sub>2</sub>O<sub>3</sub> in AZ300 MIF. Arrays of 5- $\mu$ m squares were

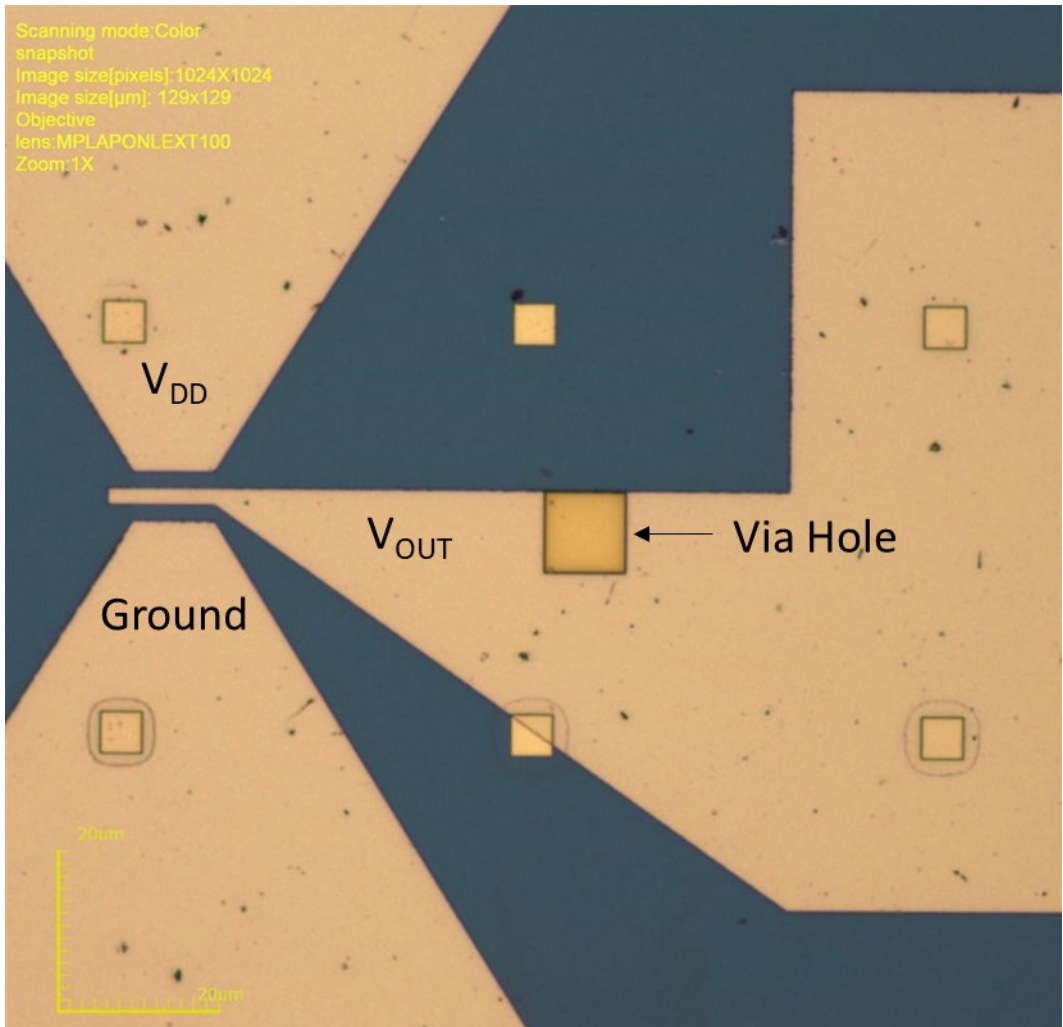
fabricated in PMMA via EBL and the chip was broken into multiple pieces. These pieces were then soaked in AZ300 MIF for varying lengths of time (5, 10, 15, 20, 25, 35, 40 min) and had their PMMA removed in acetone. Atomic force microscopy was used to determine the amount of  $\text{Al}_2\text{O}_3$  etched and the results are plotted in Fig. 14.



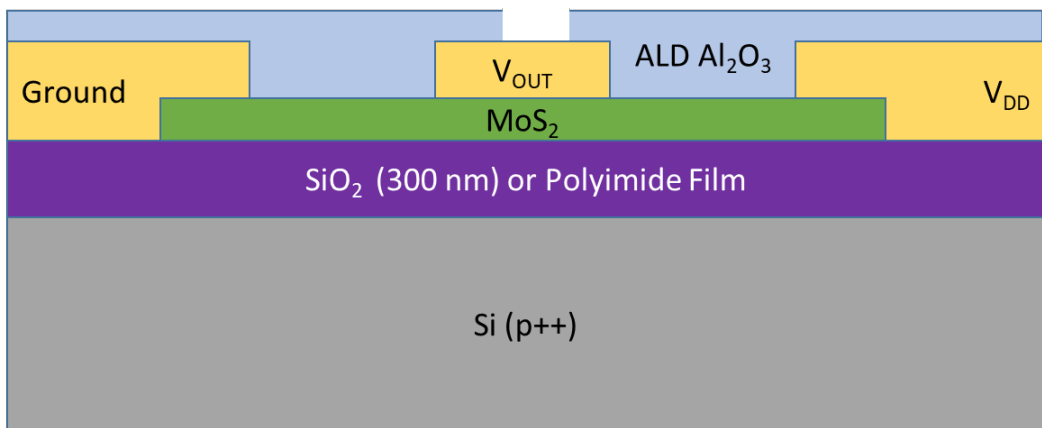
**Fig. 14** Etch rates determined prior to the via etching step

Based on the process development, we etched the samples for 35 min in AZ300 MIF to ensure all the  $\text{Al}_2\text{O}_3$  was removed.

Figure 15 shows an optical image of the example device after the via etch and the corresponding cross section is shown in Fig. 16.



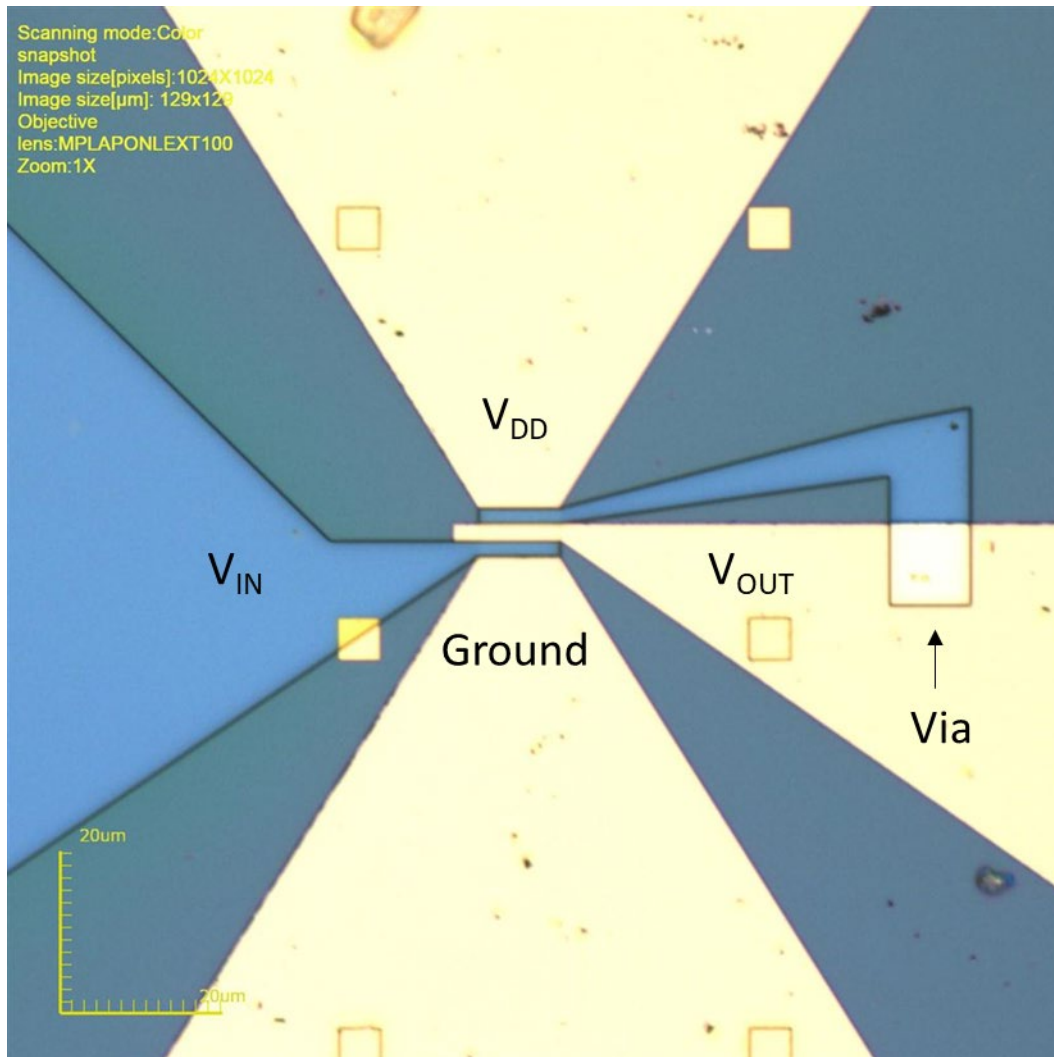
**Fig. 15** Example device after the gate via etch step. The larger square in the center is the via etch that enables the connection of the top-gate node with the output voltage node



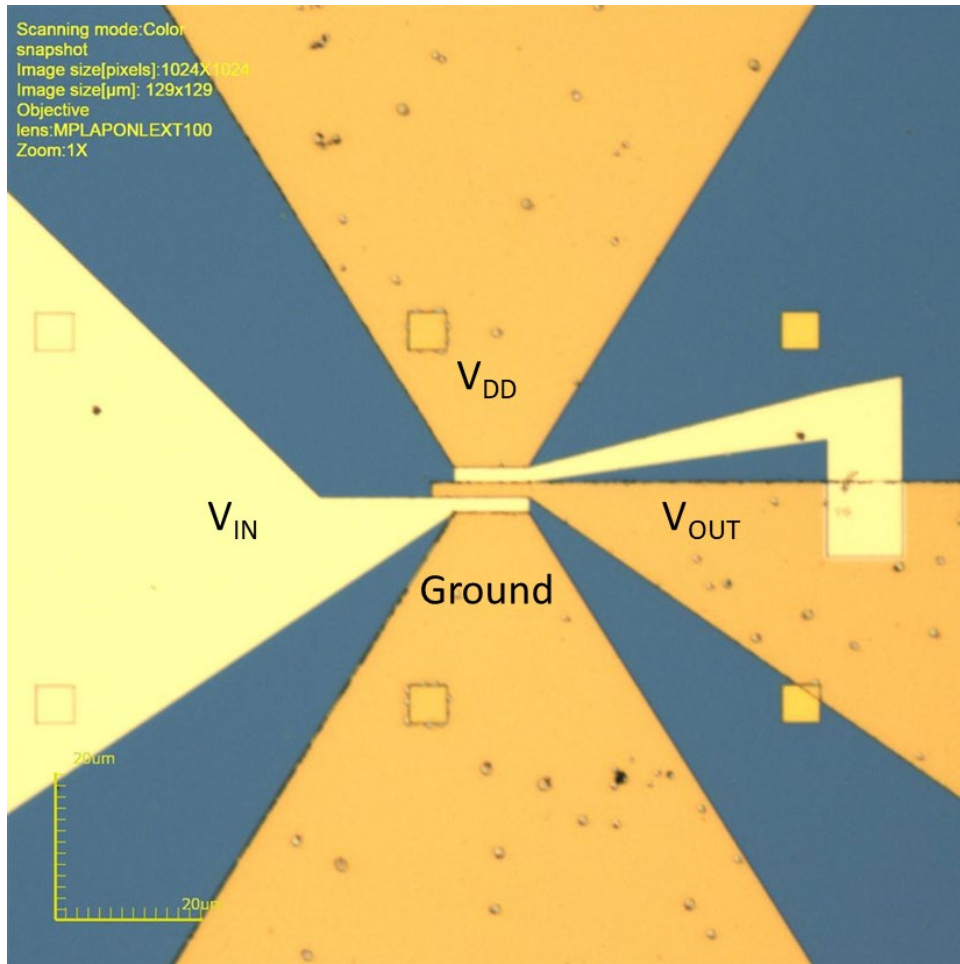
**Fig. 16** Cross section of device after the via etch step

#### 2.4.1.6 Via Fill / Top-Gate Contact

After performing the via etch, the last step in the fabrication process is the gate metal deposition/via fill. Figure 17 shows the example device after PMMA development for the gate metal layer and Fig. 18 shows the completed device after metal deposition and liftoff. Gate metal contacts received the same metal stack as the source/drain contacts (20-nm Ni, followed by 60-nm Au) and underwent the same processing conditions.

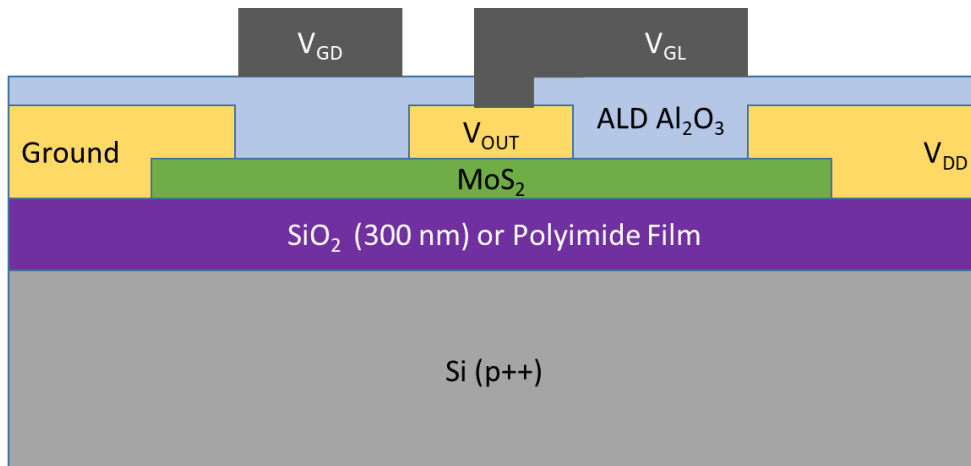


**Fig. 17** Example device after the gate metal EBL step



**Fig. 18** Example completed device after the gate metal evaporation step

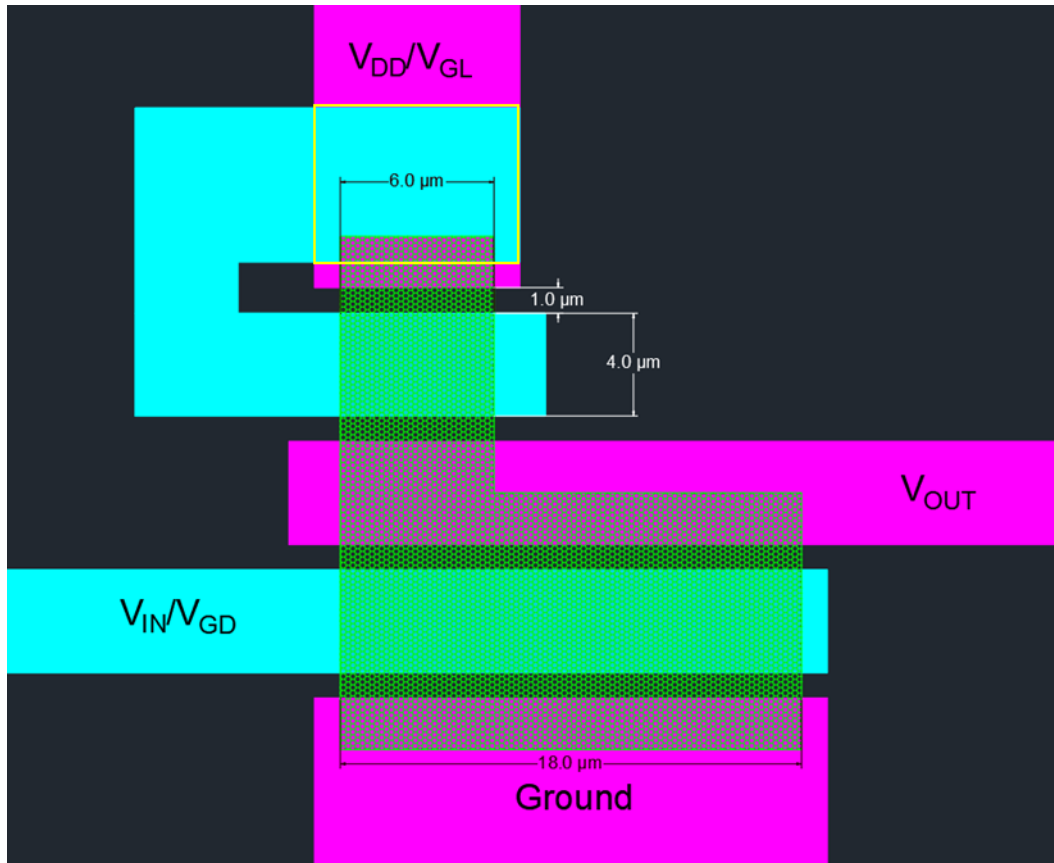
The cross section of a completed CS amplifier with a depletion-mode load transistor is shown in Fig. 19.



**Fig. 19** Cross section of CS amplifier with depletion-mode load transistor

## 2.4.2 Diode-Connected Load Transistor and Polyimide Devices

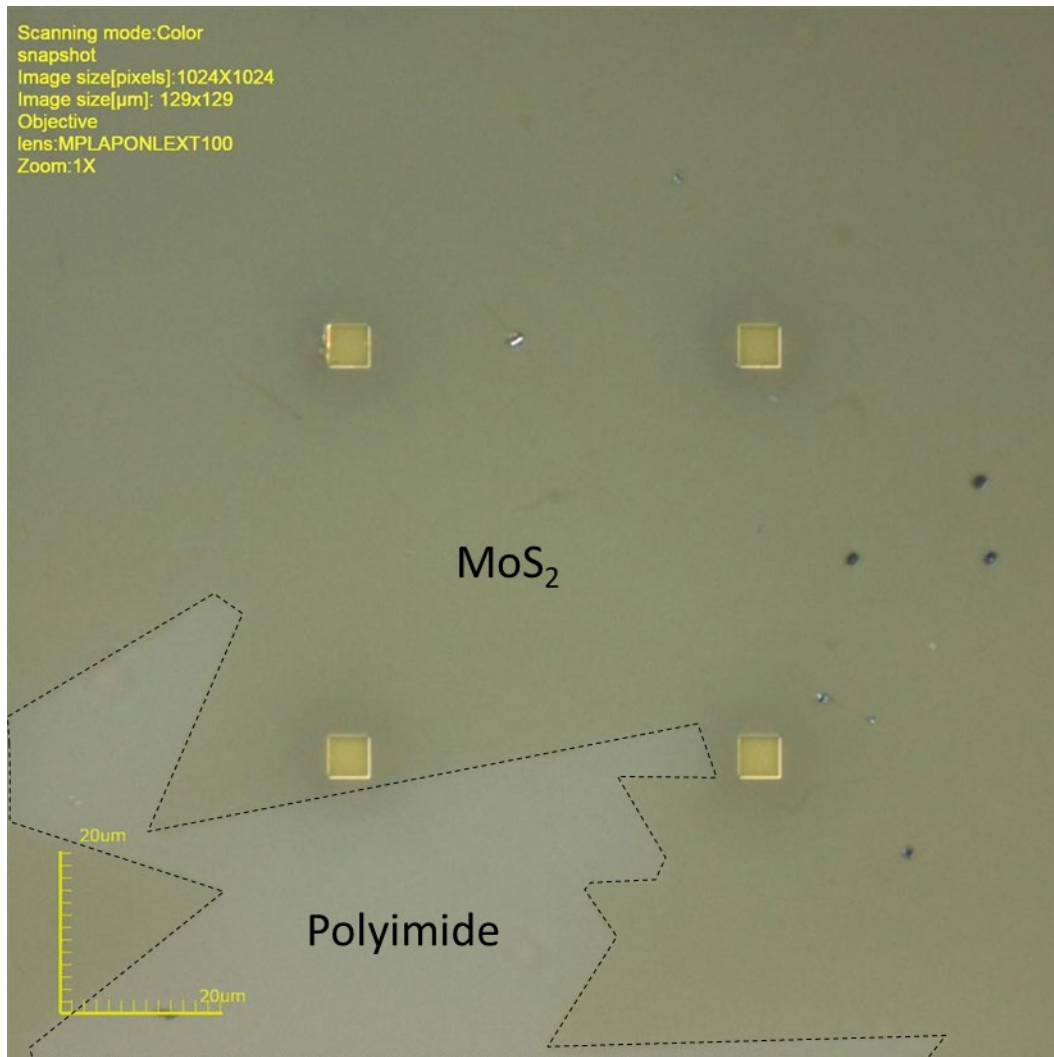
The other device fabricated had a diode-connected load transistor. This transistor has the same fabrication process, except the via connects the gate with the drain of the load transistor instead of the source. The CAD drawing for this device is shown in Fig. 20.



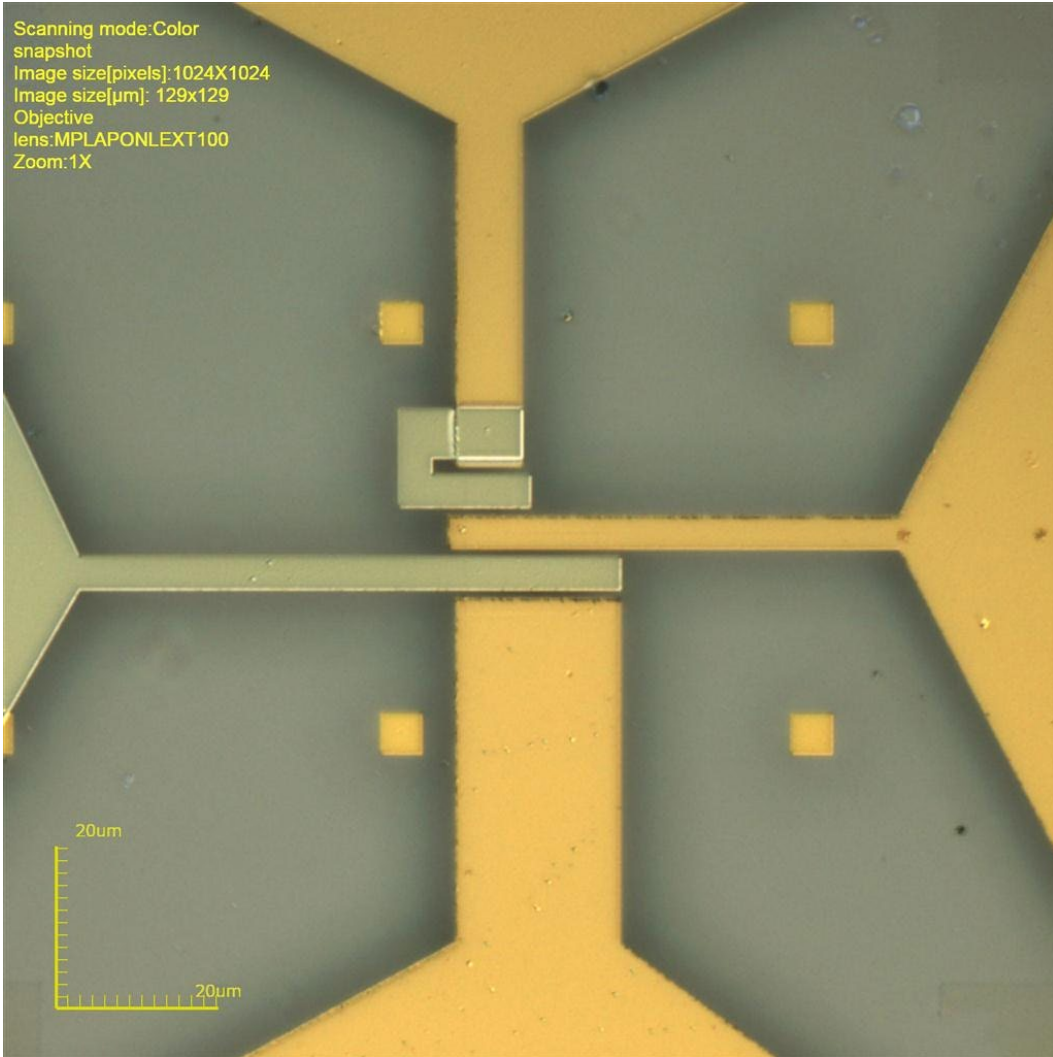
**Fig. 20** CAD drawing used for the CS amplifier with an enhancement load transistor. The lower transistor has a width of  $18\ \mu\text{m}$ , while the upper transistor's width is  $6\ \mu\text{m}$ . The location of the via etch is noted by the yellow box.

As mentioned previously, devices were also fabricated on chips that were topped with a spin-on polyimide layer. Normally for EBL on insulating substrates one must use a conductive polymer layer (or equivalent layer such as thin metal) to prevent charging artifacts from degrading the quality of the EBL write. We performed resolution experiments with and without a conductive polymer layer and determined that in our case the polyimide layer was sufficiently thin, so that charging was not an issue at the resolution we needed. Locating the  $\text{MoS}_2$  layer on the polyimide-coated substrate is substantially more difficult than on the plain thermal oxide chips. To enable easier location of areas to create devices, the differential interference contrast mode on an Olympus LEXT microscope was used.

This was done by inserting the differential interference contrast lens and the polarizer lens into the microscope, and then scrolling through the color wheel until the best optical contrast was achieved. An image of an area targeted for device fab after transfer onto polyimide is shown in Fig. 21 and a completed amplifier device with a diode-connected load on the polyimide layer is shown in Fig. 22. While devices were made and tested on the spin-on polyimide layer, the devices were not tested after delamination and bending of the flexible layer.



**Fig. 21** Area chosen for device fabrication on the substrate coated with a polyimide layer. The lighter region highlighted by the dashed line is just the polyimide substrate, whereas the darker area has monolayer MoS<sub>2</sub>.



**Fig. 22** Example of a completed amplifier with a diode-connected load on the substrates coated with a polyimide layer.

## 2.5 DC Electrical Characterization

---

All devices were tested at room temperature in a vacuum probe station at a pressure no higher than  $5 \times 10^{-5}$  Torr. Prior to testing, the devices were annealed overnight at 400 K in a vacuum to drive out water vapor and other atmospheric species. A Keithley 4200 Semiconductor Characterization System was used to perform the electrical measurements. The viewport was covered with aluminum foil to block any light from entering the probe station and ensure no impact from photosensitivity.

## 2.6 AC Electrical Characterization

---

AC electrical characterization took place in the same probe station as the DC measurements. A sinusoidal input voltage of 200 mV<sub>pp</sub> was applied via a function generator (Tektronix AFG 3252) and the output voltage was measured with a Rohde and Schwarz RTM 1054 oscilloscope in high-Z mode.

## 3. Results

---

---

This section covers the DC and AC electrical results of testing the common-source amplifiers, as well as a discussion on the impact that our testing setup has on the AC electrical measurements.

### 3.1 DC Electrical Data

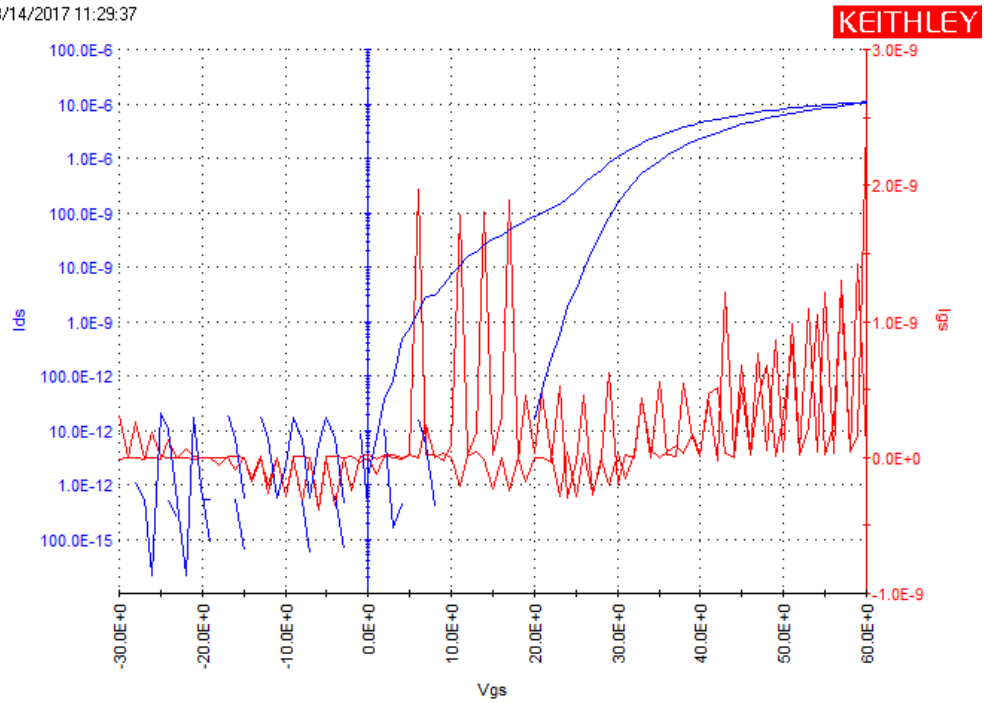
---

After completion of the metal contact layer (see Figs. 11 and 12), devices on the Si/SiO<sub>2</sub> substrate were tested in a back-gated configuration to establish a baseline of the electrical properties. Devices fabricated on the polyimide layer have a much thicker back-gate dielectric, eliminating the possibility of back-gated testing. By comparing the back-gated and top-gated characteristics of the lower transistors of the devices fabricated on the thermal oxide, we can determine how the top-gate dielectric deposition impacts the device properties.

#### 3.1.1 Back-Gated Testing

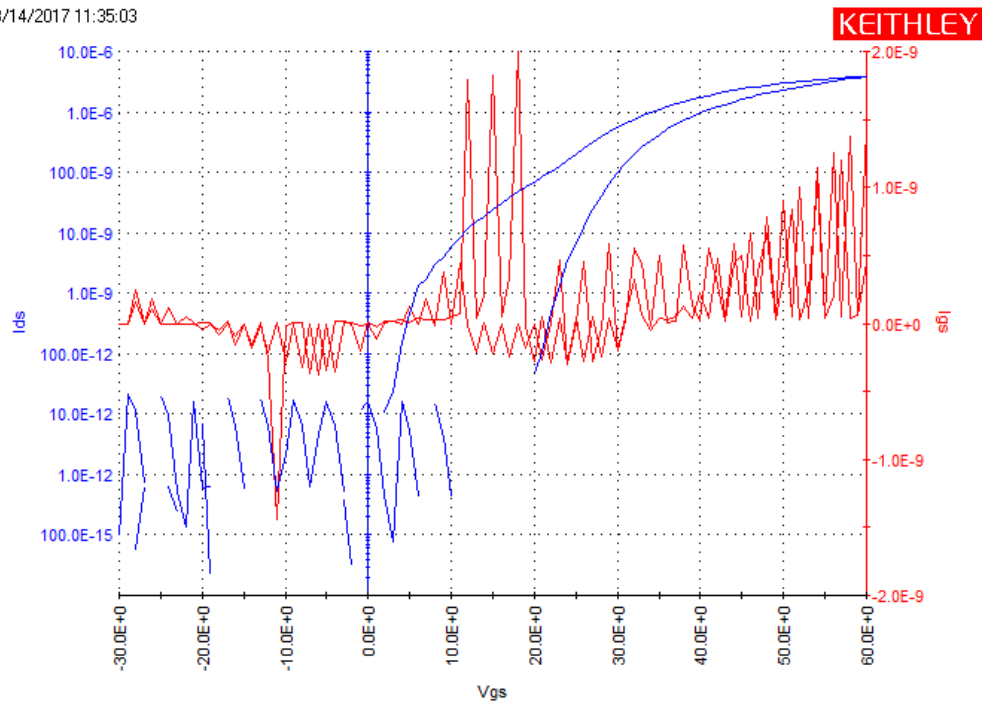
Devices were tested with a constant drain-source bias ( $V_{DS}$ ) of 100 mV, while sweeping the back-gate voltage ( $V_{GS}$ ) back and forth from -30 to +60 V. Figure 23 shows an example transfer curve ( $I_{DS}$  vs.  $V_{GS}$ ) for the bottom transistor of what will become a CS amp with a diode-connected load transistor, while Fig. 24 shows the transfer curve for the top transistor (that will become the load transistor). As one would expect, with the bottom transistor having a width of 18  $\mu\text{m}$  versus 6  $\mu\text{m}$  for the top load transistor (see Fig. 20), roughly three times the current flows through the bottom transistor.

08/14/2017 11:29:37



**Fig. 23**  $I_{DS}$ - $V_{GS}$  curve for the bottom transistor (width of  $18 \mu\text{m}$ ) of a CS amp with a diode-connected load, tested in a back-gated configuration.

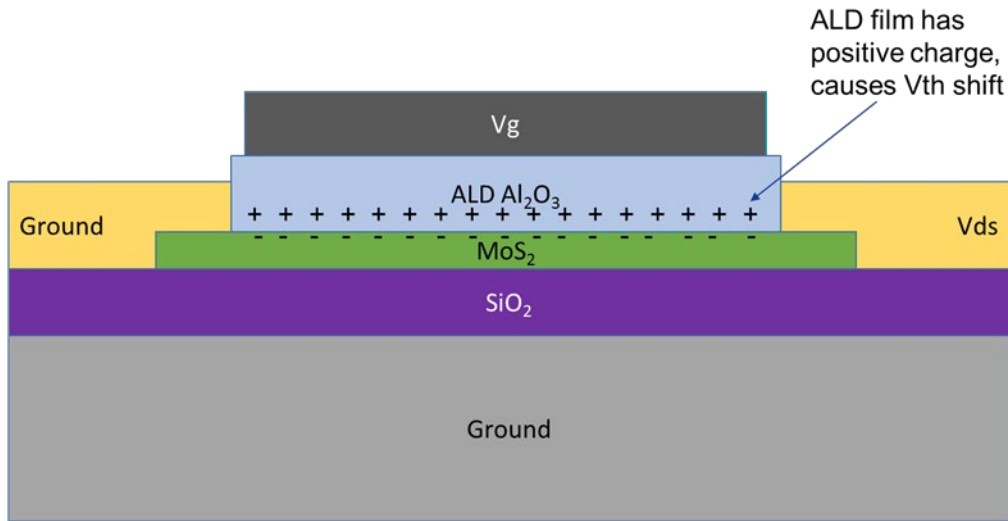
08/14/2017 11:35:03



**Fig. 24**  $I_{DS}$ - $V_{GS}$  curve for the load transistor (width of  $6 \mu\text{m}$ ) of a CS amp with a diode-connected load, tested in a back-gated configuration. Note the current is roughly 3 times lower than that of the transistor in the previous image.

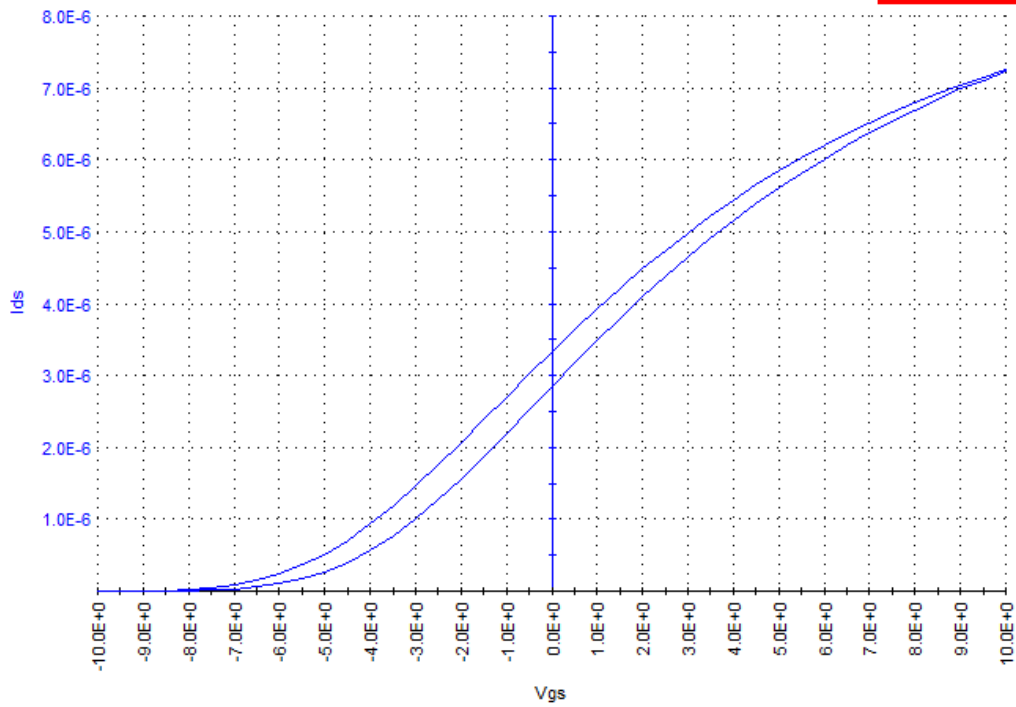
### 3.1.2 Top-Gated Testing

In the back-gated testing, devices showed a threshold voltage greater than zero. After fabrication of the top gate, it is common for the threshold voltage to substantially shift negatively. This is a result of trapped positive charge in the  $\text{Al}_2\text{O}_3$  film that attracts electrons to the  $\text{MoS}_2$  surface.<sup>7</sup> A simplified drawing of this charge doping is provided in Fig. 25.



**Fig. 25** Cross section of a top-gated  $\text{MoS}_2$  device showing the location of fixed positive charge in the gate oxide and how it changes the threshold voltage by attracting electrons to the channel.

Figure 26 shows as an example the bottom transistor  $I_{DS}-V_{GS}$  characteristics using the top gate. Clearly these devices are “on” at 0 volts  $V_{GS}$ , enabling depletion-mode electronics.



**Fig. 26** Si/SiO<sub>2</sub> substrate – device A13 CS transistor – top gated –  $I_{DS}$  vs.  $V_{GS}$ ,  $V_{DS} = 100$  [mV]

The threshold voltage of the device shown in Fig. 26 is roughly  $-5$  V. Figure 27 shows the  $I_{DS}$ - $V_{DS}$  characteristics of the same example device as Fig. 26. As one would expect, the device is entering saturation around  $V_{DS} = 5$  V when  $V_{GS} = 0$ .

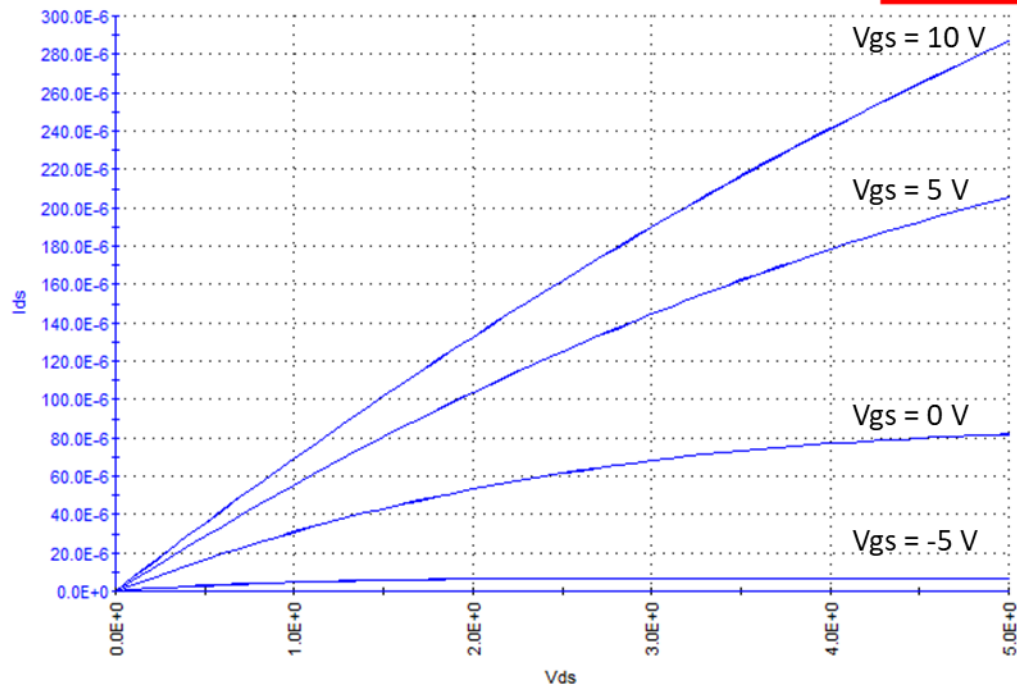
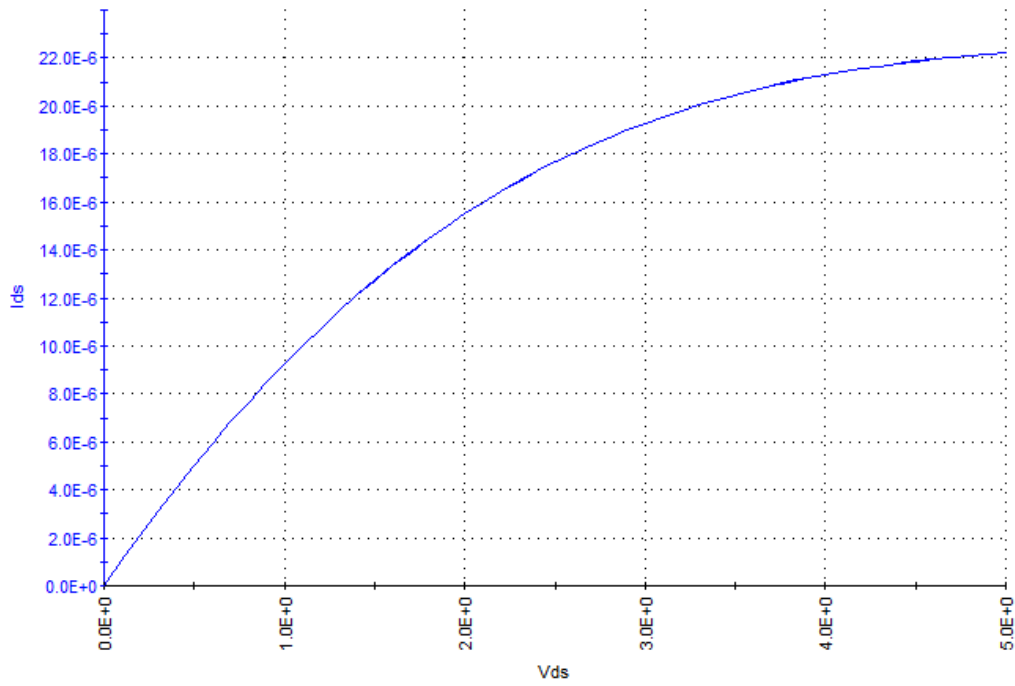


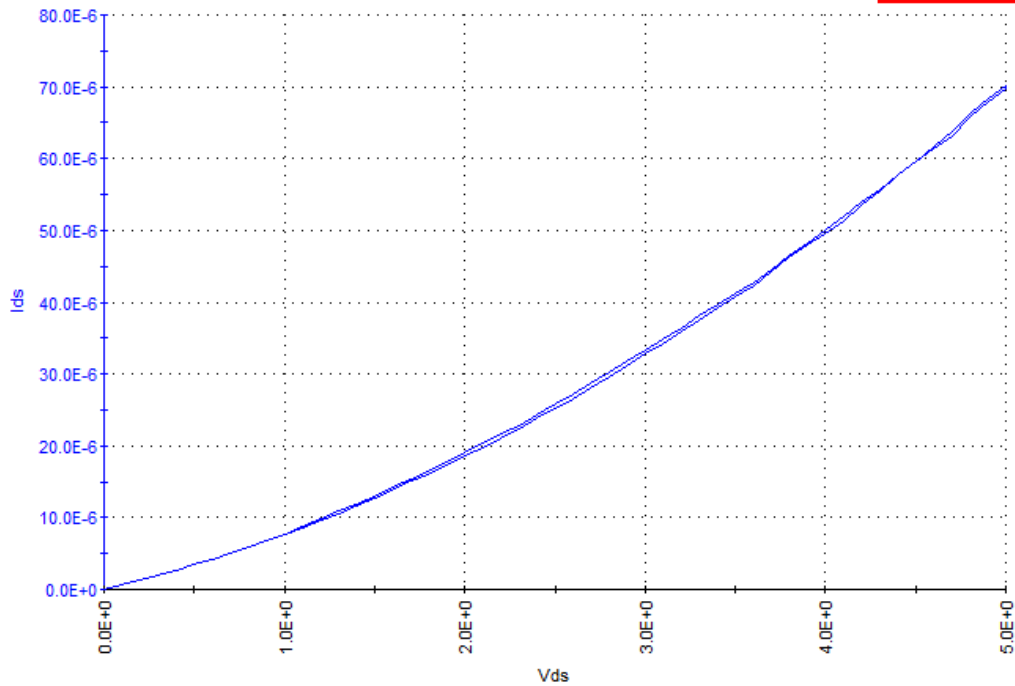
Fig. 27 Si/SiO<sub>2</sub> substrate – device A13 CS transistor – top gated –  $I_{ds}$  vs.  $V_{ds}$ ,  $V_{GS} = -10, -5, 0, 5, 10$  [V]

Figure 28 shows an example current-voltage (I-V) curve of a depletion-mode load transistor. It similarly starts to saturate at a  $V_{DS}$  of 5 V, leading to a high output resistance.



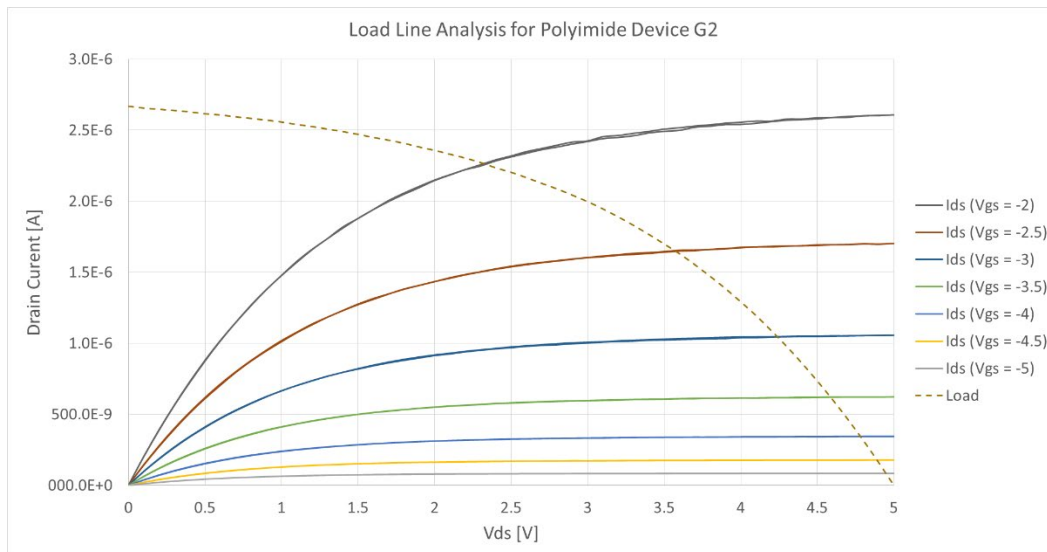
**Fig. 28** Si/SiO<sub>2</sub> substrate – device A13 load (depletion) transistor – top gated –  $I_{DS}$  vs.  $V_{DS}$ ,  $V_{GS} = 0$

Figure 29 shows an example I-V curve of a diode-connected load transistor. Compared to the depletion-mode load, the diode-connected load has a decreasing output resistance with increasing  $V_{DS}$ .



**Fig. 29** Si/polyimide substrate – device M5 load (enhancement) transistor –  $I_{ds}$  vs.  $V_{ds}$ ,  $V_{ds} = 0-5$  [V],  $V_{gs} = V_{ds}$

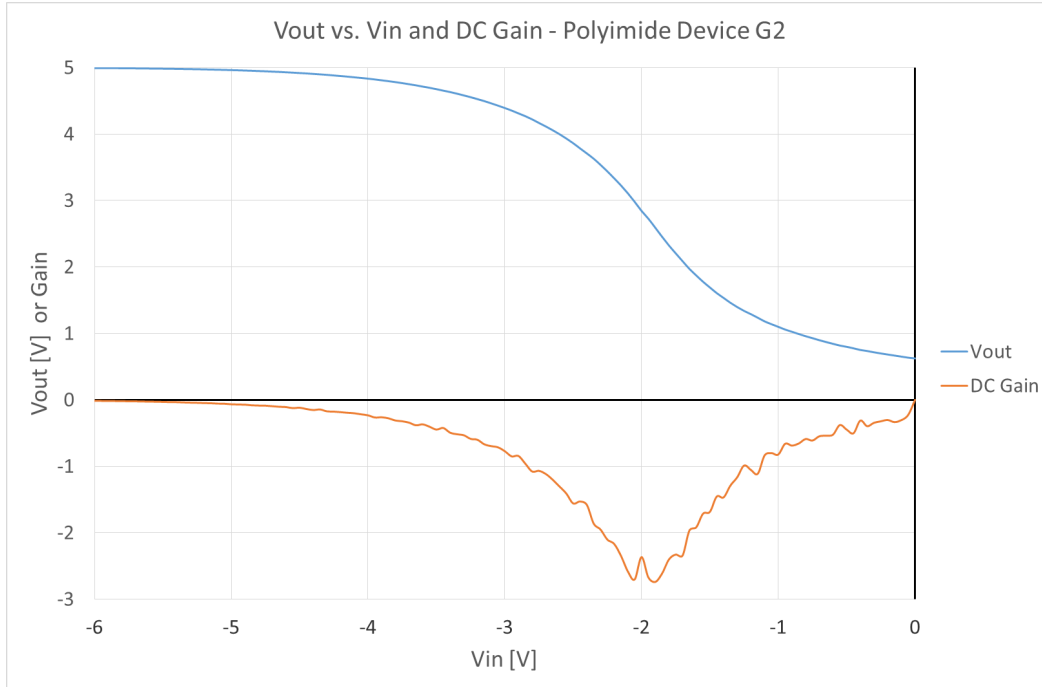
One can determine the DC operating characteristics of the amplifier circuits through load-line analysis. By plotting the reversed I-V curve of the load transistor on the same axes of the bottom transistor's  $I_{ds}$ - $V_{ds}$  curves, the areas of operation are where the curves intersect. This load-line analysis is shown in Fig. 30 for a depletion-mode load on the PI substrate.



**Fig. 30** Example load-line analysis of a CS amp with a depletion-mode load transistor

Clearly it would be beneficial to increase  $V_{DD}$  for this device as it would push both the load and lower transistor further into saturation and increase  $r_o$ .

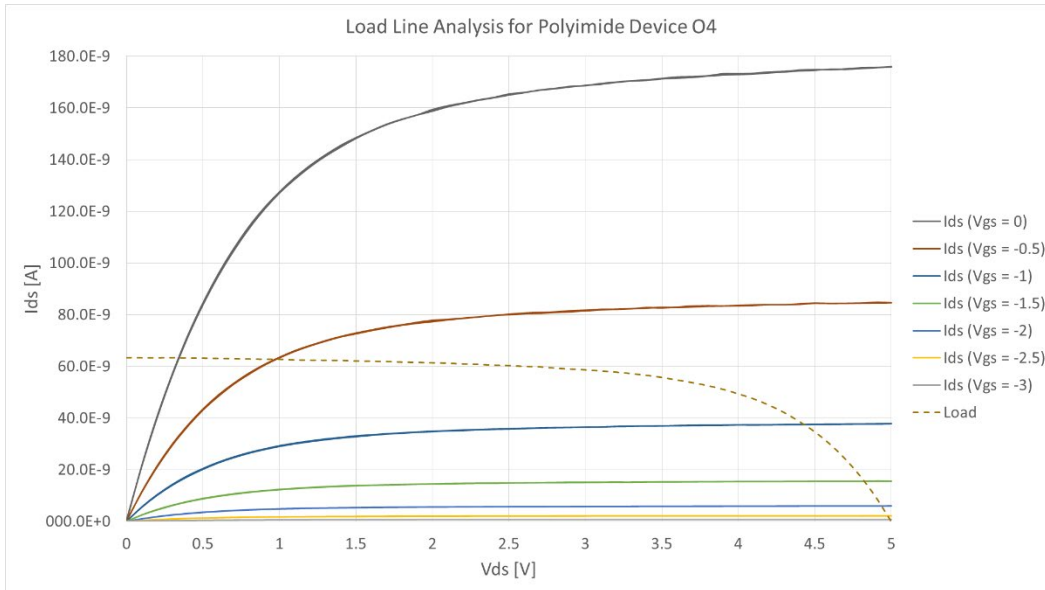
One can also perform DC sweeping of the input voltage while measuring the output voltage and get a DC gain by taking the derivative of  $V_{out}$  with respect to  $V_{in}$ . This is shown in Fig. 31, using the same device that was plotted in Fig. 30.



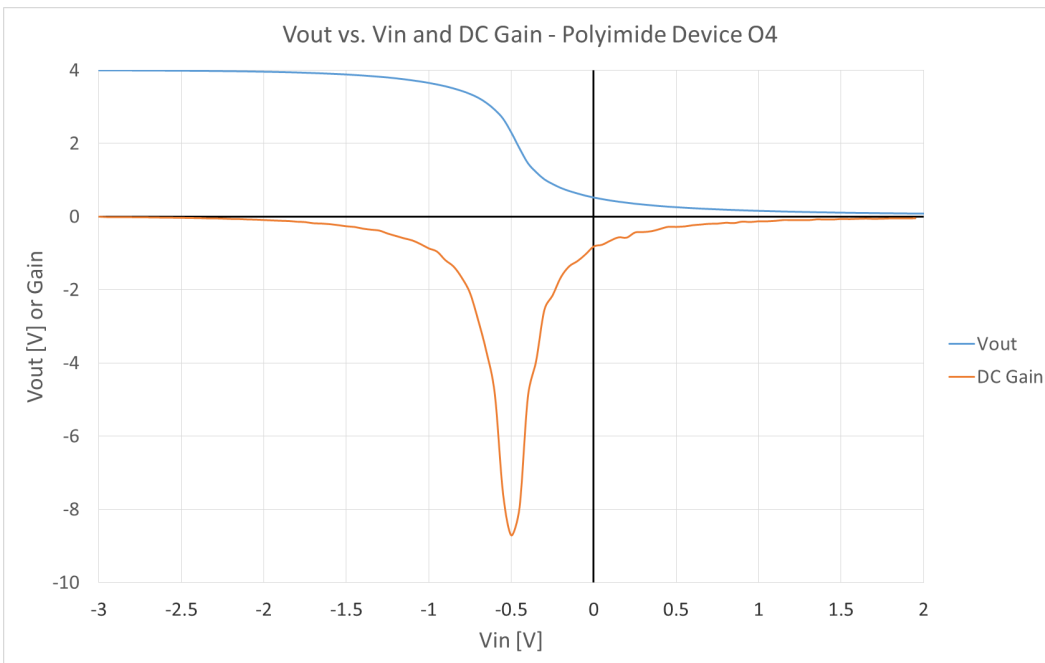
**Fig. 31** Plotted in blue is the output voltage versus the input voltage. The derivative of this blue curve gives the DC gain, plotted in orange. The maximum gain approaches  $-3$  at  $V_{in} = -2$  V with a  $V_{DD}$  of 5 V.

Other devices tested had threshold voltages closer to zero, making it possible to enter the saturation regime at lower values of  $V_{DD}$ . This device variability could be attributed to a multitude of factors such as variations in the growth properties, residue from the transfer properties, or inconsistent amounts of trapped charge at the dielectric interface.

Figure 32 shows the load line analysis of another amplifier circuit on the polyimide substrate with a threshold voltage closer to zero. The current is substantially lower, but the output resistance and DC gain is higher (Fig. 33).



**Fig. 32** Example load-line analysis of a CS amp with a depletion-mode load transistor



**Fig. 33** Plotted in blue is the output voltage versus the input voltage. The derivative of this blue curve gives the DC gain, plotted in orange. The maximum gain approaches  $-9$  at  $V_{in} = -0.5$  V with a  $V_{DD}$  of 4 V.

This DC gain analysis provides us with knowledge on how to properly bias the devices for AC measurements and gives us an upper bound of what to expect in terms of gain.

### 3.2 AC Electrical Results

A gain of around 1–2.5 was measured for most devices, while operating from a single kilohertz to 10’s of kilohertz. The gain increase expected for some devices by raising  $V_{DD}$  was not as large as expected and—as is discussed in Section 3.3—this was mainly hindered by a low-frequency pole on the output voltage node caused by our testing setup.

An example display from the oscilloscope is shown in Fig. 34. Very clear gain and inverting behavior can be seen.

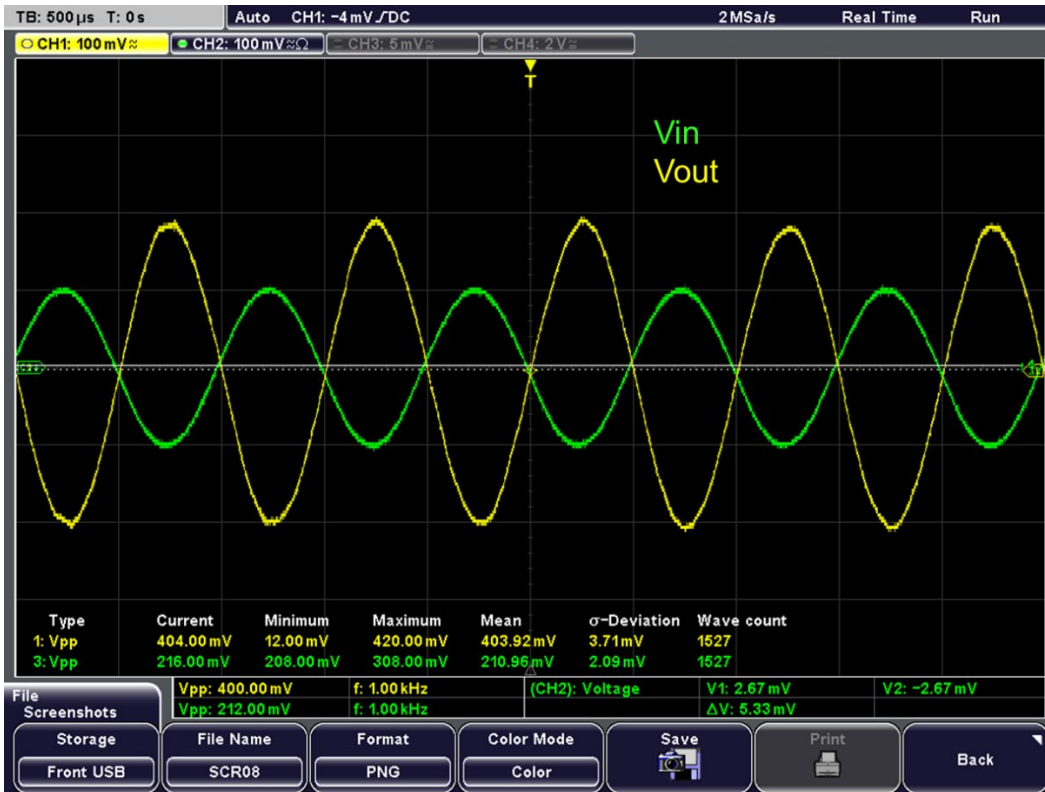


Fig. 34 Example oscilloscope waveform showing the input voltage (green) and output voltage (yellow) at a frequency of 1 KHz

Table 1 shows the maximum gain at 1 KHz and the maximum frequency of unity gain for both types of substrates and both types of transistor load.

**Table 1 Summary of the gain and frequency response measured**

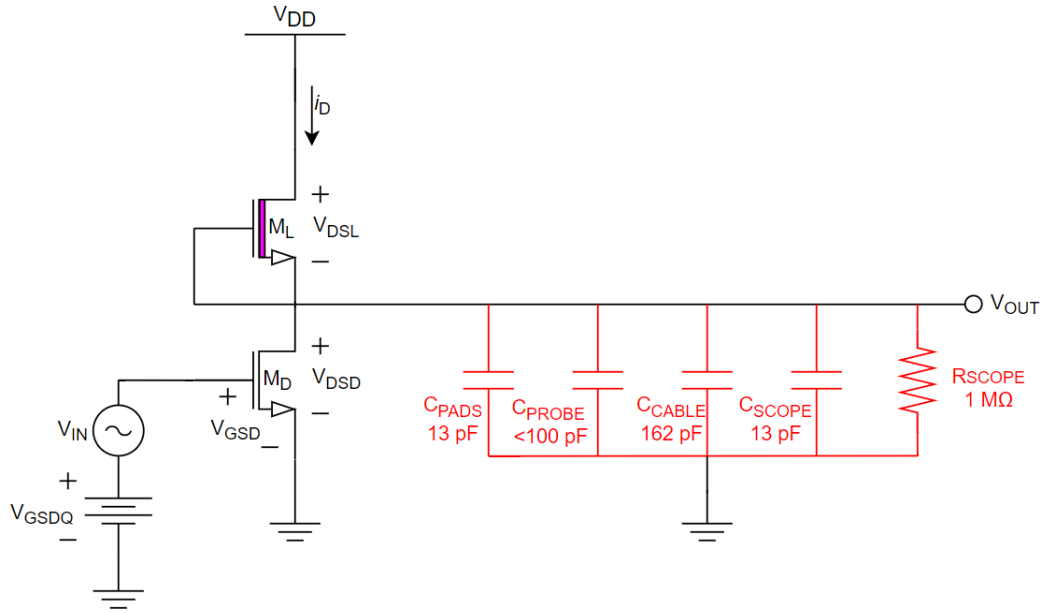
Substrate	Transistor load type	Max gain at 1 kHz	Max frequency of unity gain (kHz)
Hard (Al <sub>2</sub> O <sub>3</sub> )	Depletion	2.45 (V <sub>DD</sub> = 10 V)	19.5 (V <sub>DD</sub> = 10 V)
Soft (polyimide)	Depletion	2.26 (V <sub>DD</sub> = 10 V)	3.6 (V <sub>DD</sub> = 10 V)
Hard (Al <sub>2</sub> O <sub>3</sub> )	Enhancement	1.44 (V <sub>DD</sub> = 15 V)	16 (V <sub>DD</sub> = 20 V)
Soft (polyimide)	Enhancement	1.55 (V <sub>DD</sub> = 15 V)	15 (V <sub>DD</sub> = 20 V)

As  $V_{DD}$  was increased, the gain for the enhancement load amplifiers approached the expected value of  $\sqrt{3} \sim 1.732$ . It should be noted here that since these devices have a threshold voltage less than zero, the diode connect devices are not in the saturation regime, but rather in the linear regime. However, the expression for  $g_m$  using the linear regime current equation becomes the same as  $g_m$  for the saturation regime when  $V_{DS}$  is tied to  $V_{GS}$ .

### 3.3 Testing Setup Impact

The frequency response of common-source amplifiers is eventually limited due to the Miller effect; however, that is not the case here. The frequency response of our amplifiers was severely limited by the capacitances and resistances of the testing setup. These resistances and capacitances are in parallel on the output voltage node and create a pole around 1 kHz.

A more accurate representation of our amplifier circuit that includes the capacitances and resistances is shown in Fig. 35.



**Fig. 35** Circuit diagram of the CS amplifier including the parasitic capacitances and resistance coming from the testing setup

The relevant capacitances are as follows:

- $C_{pad} \sim 13$  pF on the  $\text{SiO}_2$  substrate, 0.07 pF on the polyimide substrate. Related to the probe pads.
- $C_{probe}$  arm is unknown, but listed as less than 100 pF for the DC LakeShore probe station arm cable.
- $C_{cable} = 162$  pF for the coaxial cable connecting the probe station arm to the oscilloscope.
- $C_{scope} = 13$  pF for the oscilloscope input (Rhode and Schwarz Scope).
- These capacitances add to a total capacitance on the output node of  $C_{output} \sim 200$  to  $288$  pF.

The relevant resistance of the testing setup is the oscilloscope's  $1\text{ M}\Omega$  input impedance. This input impedance is added in parallel with the two transistor output resistances to give  $R_{output} = 1\text{ M}\Omega \parallel r_{oD} \parallel r_{oL} \sim 10\text{ k}\Omega$  to  $1\text{ M}\Omega$ .

Including only the abovementioned resistances and capacitances, the transfer function of the gain is

$$\frac{V_{out}}{V_{in}}(s) = \frac{g_m R_{output}}{1 + s(RC)_{output}}. \quad (10)$$

The frequency of the pole that will lower the output voltage is given by the RC time constant related to the total resistance and capacitance on the output voltage node:

$$f_{output} = \frac{1}{2\pi (RC)_{output}}. \quad (11)$$

If  $R = 10 \text{ K}\Omega$  and  $C = 200 \text{ pF}$ , then the pole is located at 79.6 kHz. This represents the best-case frequency response assuming there is minimal probe arm capacitance and low output resistance ( $10 \text{ K}\Omega$ ). The output resistance would only be this low in the diode-connected loads; however, these devices are limited in gain to  $\sqrt{3}$  due to their W/L ratios. Better frequency response was noted for the diode-connected loads (that is, the pole was clearly at a higher frequency).

If  $R = 1 \text{ M}\Omega$  and  $C = 280 \text{ pF}$ , then the pole is located at 554 Hz. This represents the worst-case frequency response, assuming the probe arm capacitance is 100 pF and that the transistor's output resistance is substantially higher than the oscilloscope's input impedance, meaning the total resistance on the output node is dominated by the 1-M $\Omega$  input impedance. This scenario is more likely for the depletion-mode loads, where the gain is higher, but the lower frequency pole interferes with that gain earlier.

## 4. Conclusions/Future Work

---

Here we detail potential improvements or considerations for future devices and general observations about the fabrication, testing, or performance of these amplifiers.

### 4.1 Increasing Gain

---

Looking back at Eq. 8 for the gain of a CS amplifier, it is the product of the transconductance,  $g_m$ , and the output resistance,  $r_o$ . Looking back at Eq. 5 for the transconductance of a MOSFET, there are many options for increasing  $g_m$ :

- Better contacts
  - While contact resistance is not included in the transistor current expression (Eq. 4), contact resistance limits the amount of current that can flow through the channel and also limits the transconductance. The improvements listed below will ultimately be limited by the large contact resistance to 2-D monolayers like MoS<sub>2</sub>.

- Larger W/L ratio
  - With access to large-area MoS<sub>2</sub>, the width of the MoS<sub>2</sub> transistors can be increased to 50–100 μm. With EBL fabrication methods, the length of the transistors can also be scaled down to the 200–400 nm range (increasing the W/L ratio by 25–100 times).
- Increased cox (thinner/higher-κ gate dielectric)
  - First round devices used 250 cycles of ALD Al<sub>2</sub>O<sub>3</sub> in order to ensure no gate leakage. However, cutting this in half should still lead to a gate dielectric with high electrical integrity and would theoretically double the device transconductance. Additionally, switching to a higher-κ dielectric is another route to increase the gate capacitance.
- Higher mobility material
  - The transconductance is also directly proportional to the mobility of the MoS<sub>2</sub> material. The theoretical maximum room temperature mobility of monolayer MoS<sub>2</sub> is around 130–320 cm<sup>2</sup>/V·s, depending on the intervalley separation.<sup>8</sup> The mobility we normally measure is around 10 cm<sup>2</sup>/V·s; however, the improvement to be expected here is minimal based on the similarly reported values of mobility in the literature for MoS<sub>2</sub> grown by powder vaporization.

While the methods listed will increase  $g_m$ , that does not mean that the device gain will increase by that amount since the output resistance will decrease as well. For standard Si MOSFETs, the maximum gain is listed as follows:  $g_m r_o = \frac{1}{\lambda} \frac{2}{(V_{GS} - V_{th})}$ .  $\lambda$  is proportional to  $1/L$ , so to improve the gain the length of the channel ( $L$ ) should not be scaled aggressively to improve  $g_m$  but rather investigated for its impact on  $\lambda$  to improve  $r_o$ .<sup>4</sup> The other term in the denominator of the maximum gain expression is  $(V_{GS} - V_{th})$ . This is where we see the largest potential for improvement in semiconductor electronics made from MoS<sub>2</sub>: precise control of the doping levels. Other researchers have seen an improvement in threshold voltage uniformity by moving to a gate-first fabrication process, enabling improved circuit design and circuit complexity.<sup>9</sup> Unfortunately, while their devices are more consistent, their device threshold voltage is still positive, meaning to use a depletion-mode load (setting  $V_{GS} = 0$ ) they are limited in how much current they can push through it. Ideally there will be improvements to both the growth and doping capabilities to enable precise control over the threshold voltage in MoS<sub>2</sub>.

## 4.2 Improving Frequency Response

---

As mentioned in Section 3.3, the main reason for the limited frequency response of the devices are contributions from the parasitic resistances and capacitances of the test setup. Assuming we are constricted and only interested in the performance of these amplifiers in a similar test setup (directly probing the device with a signal generator input and measuring the output with an oscilloscope), then the output RC constant must be reduced.

Options for lowering R:

- Most of the improvements for a higher transconductance will also lower the output resistance.
- Add source follower stage (common drain).
- Off-chip voltage buffer (OP-AMP).

Options for lowering C:

- Cpad can go from 13 pF to 2–4 pF with changes in pad sizes.
- Direct probing of devices in a wire-bonded package (avoiding probe station cable capacitance).
- Probe capacitance-compensation.

Alternatively, devices could be fabricated in a manner that enables standard S-parameter measurements and de-embedding. In this case, one would wish to maximize  $g_m$  and limit the Miller capacitance. Using a cascode layout and the previously mentioned gate-first fabrication process, amplification at gigahertz frequencies has been demonstrated.<sup>10</sup>

## 4.3 Other Observations

---

Other observations from our study include the following:

- Heating the KOH will facilitate a quicker separation of the PMMA film from the growth substrate; however, this often leads to increased levels of residue on the transferred film. We found it preferable to leave the samples in room temperature KOH overnight rather than speeding up the process via heating.
- Electrical performance of devices on the Si/polyimide substrate was more inconsistent and had lower current levels compared to the devices on the Si/SiO<sub>2</sub> substrate.

- The device yield for the Si/SiO<sub>2</sub> substrate was 24/25 amplifiers and 11/13 for the Si/polyimide substrate.

In summary, common-source amplifiers were fabricated using ARL-grown monolayer MoS<sub>2</sub> as the transistor channel material. Two different load transistor configurations were investigated: a depletion-mode load transistor (gate and source tied together) and a diode-connected load transistor (drain and gate tied together). After transferring from the growth substrate via a potassium hydroxide wet etch process, devices were fabricated on a thermal oxide substrate and on a spin-on polyimide layer. The depletion-mode load transistor devices showed a DC voltage gain up to  $-10$  with a supply voltage of 4 V, with the device performance mainly determined by the variation in doping level after the top-gate dielectric deposition. AC voltage gain for both load types was typically  $-1$  to  $-2.5$  at frequencies of 1 kHz to 10's of kilohertz. The AC performance was mainly limited by parasitic resistances and capacitances of the testing setup, which created a low frequency pole at approximately 1 kHz. Ways to improve device transconductance were mentioned; however, improved control over the device threshold voltage level and variation was highlighted as a main concern for the design of future circuits.

## 5. References

---

1. Wang G, Chernikov A, Glazov MM, Heinz TF, Marie X, Armand T, Urbaszek B. Colloquium: Excitons in atomically thin transition metal dichalcogenides. *Rev Mod Phys.* 2018;90:021001.
2. Akinwande D, Petrone N, Hone J. Two-dimensional flexible nanoelectronics. *Nat Commun.* 2014;5:5678.
3. Mazzone AL, Burke RA, Chin ML, Hwee MJ. Effects of growth conditions on the measured electrical properties of monolayer molybdenum disulfide. Aberdeen Proving Ground (MD): Army Research Laboratory (US); 2017 Feb. Report No.: ARL-TR-7949.
4. Gray PR, Hurst PJ, Lewis SH, Meyer RG. Analysis and design of analog integrated circuits. Hoboken (NJ): John Wiley & Sons, Inc.; 2001.
5. Chipara AC, Mazzone AL, Burke RA, Nichols BM, Chin ML, Najmaei S, Zakar E, Dubey M. Process development for reactive-ion etching of molybdenum ( $\text{MoS}_2$ ) utilizing a poly(methyl methacrylate) (PMMA) etch mask. Aberdeen Proving Ground (MD): Army Research Laboratory (US); 2017 Oct. Report No.: ARL-TR-8192.
6. Son S, Yu S, Choi M, Kim D, Choi C. Improved high temperature integration of  $\text{Al}_2\text{O}_3$  on  $\text{MoS}_2$  by using a metal oxide buffer layer. *Appl Phys Lett.* 2015;106(2):021601.
7. Na J, et al. Low-frequency noise in multilayer  $\text{MoS}_2$  field-effect transistors: the effect of high-k passivation. *Nanoscale.* 2014;6:433–441.
8. Jin Z, Li X, Mullen JT, Kim KW. Intrinsic transport properties of electrons and holes in monolayer transition-metal dichalcogenides. *Phys Rev B.* 2014;90(4):045422.
9. Yu L. et al. Design, modeling, and fabrication of chemical vapor deposition grown  $\text{MoS}_2$  circuits with e-mode FETs for large-area electronics. *Nano Lett.* 2016;16(10):6349–6356. doi:10.1021/acs.nanolett.6b02739.
10. Sanne A, Park S, Ghosh R, Yogeesh MN, Liu C, Akinwande D, Banerjee S, Mathew L, Rao R. Record  $f_T$ ,  $f_{\text{max}}$ , and GHz amplification in 2-dimensional CVD  $\text{MoS}_2$  embedded gate FETs. In: 2017 IEEE International Symposium on Circuits and Systems (ISCAS) 1–4; 2017 May 28–31; Baltimore, MD. IEEE. doi:10.1109/ISCAS.2017.8051016.

## List of Symbols, Abbreviations, and Acronyms

---

2-D	two-dimensional
AC	alternating current
Al	aluminum
Al <sub>2</sub> O <sub>3</sub>	aluminum oxide
ALD	atomic layer deposition
Au	gold
CAD	computer-aided design
CCDC ARL	US Army Combat Capabilities Development Command Army Research Laboratory
Cl <sub>2</sub>	chlorine gas
CS	common source
DC	direct current
DI	deionized
EBL	electron beam lithography
FET	field-effect transistor
IPA	isopropyl alcohol
I-V	current-voltage
KOH	potassium hydroxide
MIBK	methyl isobutyl ketone
MoS <sub>2</sub>	molybdenum disulfide
MOSFET	metal-oxide-semiconductor field-effect transistor
NMOS	n-type metal-oxide-semiconductor
Ni	nickel
O <sub>2</sub>	oxygen gas
PEALD	plasma-enhanced atomic layer deposition
PMMA	poly(methyl methacrylate)

RIE	reactive ion etching
Si	silicon
SiO <sub>2</sub>	silicon dioxide
Ti	titanium
TMAH	tetramethylammonium hydroxide
vdW	van der Waals

1 DEFENSE TECHNICAL  
(PDF) INFORMATION CTR  
DTIC OCA

2 CCDC ARL  
(PDF) IMAL HRA  
RECORDS MGMT  
FCDD RLD CL  
TECH LIB

1 GOVT PRINTG OFC  
(PDF) A MALHOTRA

12 CCDC ARL  
(PDF) FCDD RLS  
R BURKE  
FCDD RLS RE  
T IVANOV  
P SHAH  
G BIRDWELL  
J WEIL  
FCDD RLS RL  
A MAZZONI  
M CHIN  
S NAJMAEI  
M DUBEY  
M VALENTIN  
E ZAKAR  
FCDD RLS RM  
K PRICE