DE10 PINS AND CONNECTIONS FOR BASIC MIPS

TECHNICAL REPORT

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Abstract

This report describes in detail the pins and connections for the Basic MIPS architecture on a Terrasic DE10-Standard board utilizing an Intel Cyclone V FPGA. Specifically, the detailed connections between one DE10-Standard running Basic MIPS, Temporal Software Redundancy (TSR) MIPS, Triple Modular Redundancy (TMR) MIPS, or Adaptive-Hybrid Redundancy (AHR) MIPS and a second DE10-Standard storing a program in a memory emulator are fully documented.

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DE10 PINS AND CONNECTIONS FOR BASIC MIPS

I. Connections

This report describes the DE10-Standard pins used to implement the various MIPS architectures (Basic, Triple Modular Redundancy (TMR), Temporal Software Redundancy (TSR), and Adaptive-Hybrid Redundancy (AHR)) as well as the memulators. It also describes the interconnections between them. The DE10-Standard pinouts are described in detail in the "DE10-Standard User Manual" and the "DE10-Standard Schematic" [2, 3]. Additionally, the HSTC to GPIO Daughter Board pinouts are described in the "THDB-HTG Revision B Schematic" [1]. By examining these documents together, it is possible to determine a mapping from MIPS and Memulator signals to specific pins on connectors.

The first connection between a MIPS processor DE10-Standard board and a Memulator DE10-Standard board is between the onboard 2x20 pin GPIO connectors on each board. Figure 1 shows the pinout of the GPIO connector as viewed from above. The figure shows the alignment notch as a gap in the left edge of the connector. The pin numbers are shown as well. The red "x" symbols over pins 11 and 29 indicates that those pins are intentionally not connected. Table 1 shows the connections to these pins as determined by tracing pin numbers from the schematics in the "DE10-Standard Schematic" and "DE10-Standard User Manual" [2, 3]. This table also shows the associated MIPS processor signals for the DE10-Standard running the processor. Similarly, Table 2 shows the Memulator signals for the DE10-Standard running the Memulator. In these tables, VCC5 and VCC3P3 denote 5V and 3.3V power respectively and GND denotes ground. Also note that the processor uses the signal names

i_MEM_READY, o_MEM_READ, o_MEM_WRITE, and o_MEM_IN where the Memulator uses o_READY, i_read_enable, i_write_enable, and i_data respectively. The inputs and outputs denoted by "i" and "o" are also swapped between the two tables because the MIPS processor's output is the Memulator's input and vice versa.

One other final note is that the ground pins (GPIO pins 12 and 30) are connected while the VCC pins (GPIO pins 11 and 29) are left unconnected. The ground pins are connected to ensure a common ground between the DE10-Standard boards while the VCC pins are left unconnected to ensure that neither board is pushing a current to the other one in case the VCC values are not correctly matched. A common ground between the two DE10-Standard boards is essential if either board is to correctly resolve signals from the other board.

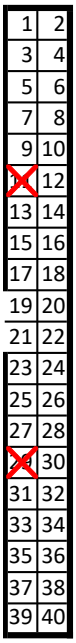

Figure 1. DE10-Standard GPIO Connector

Table 1. MIPS Processor DE10-Standard GPIO Connector Pinout

GPIO Pin Number	Cyclone V Signal Name	Cyclone V Pin	MIPS Signal
1	GPIO_D0	PIN_W15	o_MEM_IN(0)
2	GPIO_D1	PIN_AK2	o_MEM_IN(1)
3	GPIO_D2	PIN_Y16	o_MEM_IN(2)
4	GPIO_D3	PIN_AK3	o_MEM_IN(3)
5	GPIO_D4	PIN_AJ1	o_MEM_IN(4)
6	GPIO_D5	PIN_AJ2	o_MEM_IN(5)
7	GPIO_D6	PIN_AH2	o_MEM_IN(6)
8	GPIO_D7	PIN_AH3	o_MEM_IN(7)
9	GPIO_D8	PIN_AH4	o_MEM_IN(8)
10	GPIO_D9	PIN_AH5	o_MEM_IN(9)
11	VCC5		
12	GND		
13	GPIO_D10	PIN_AG1	o_MEM_IN(10)
14	GPIO_D11	PIN_AG2	o_MEM_IN(11)
15	GPIO_D12	PIN_AG3	o_MEM_IN(12)
16	GPIO_D13	PIN_AG5	o_MEM_IN(13)
17	GPIO_D14	PIN_AG6	o_MEM_IN(14)
18	GPIO_D15	PIN_AG7	o_MEM_IN(15)
19	GPIO_D16	PIN_AG8	o_MEM_IN(16)
20	GPIO_D17	PIN_AF4	o_MEM_IN(17)
21	GPIO_D18	PIN_AF5	o_MEM_IN(18)
22	GPIO_D19	PIN_AF6	o_MEM_IN(19)
23	GPIO_D20	PIN_AF8	o_MEM_IN(20)
24	GPIO_D21	PIN_AF9	o_MEM_IN(21)
25	GPIO_D22	PIN_AF10	o_MEM_IN(22)
26	GPIO_D23	PIN_AE7	o_MEM_IN(23)
27	GPIO_D24	PIN_AE9	o_MEM_IN(24)
28	GPIO_D25	PIN_AE11	o_MEM_IN(25)
29	VCC3P3		
30	GND		
31	GPIO_D26	PIN_AE12	o_MEM_IN(26)
32	GPIO_D27	PIN_AD7	o_MEM_IN(27)
33	GPIO_D28	PIN_AD9	o_MEM_IN(28)
34	GPIO_D29	PIN_AD10	o_MEM_IN(29)
35	GPIO_D30	PIN_AD11	o_MEM_IN(30)
36	GPIO_D31	PIN_AD12	o_MEM_IN(31)
37	GPIO_D32	PIN_AC9	o_MEM_READ
38	GPIO_D33	PIN_AC12	o_MEM_WRITE

Table 1 – *Continued on next page*

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GPIO Pin Number	**Cyclone V Signal Name**	**Cyclone V Pin**	**MIPS Signal**
39	GPIO_D34	PIN_AB12	i_MEM_READY
40	GPIO_D35	PIN_AA12	i_DONE

Table 2. Memulator DE10-Standard GPIO Connector Pinout

GPIO Pin Number	**Cyclone V Signal Name**	**Cyclone V Pin**	**MIPS Signal**
1	GPIO_D0	PIN_W15	i_data(1)
2	GPIO_D1	PIN_AK2	i_data(0)
3	GPIO_D2	PIN_Y16	i_data(3)
4	GPIO_D3	PIN_AK3	i_data(2)
5	GPIO_D4	PIN_AJ1	i_data(5)
6	GPIO_D5	PIN_AJ2	i_data(4)
7	GPIO_D6	PIN_AH2	i_data(7)
8	GPIO_D7	PIN_AH3	i_data(6)
9	GPIO_D8	PIN_AH4	i_data(9)
10	GPIO_D9	PIN_AH5	i_data(8)
11	VCC5		
12	GND		
13	GPIO_D10	PIN_AG1	i_data(11)
14	GPIO_D11	PIN_AG2	i_data(10)
15	GPIO_D12	PIN_AG3	i_data(13)
16	GPIO_D13	PIN_AG5	i_data(12)
17	GPIO_D14	PIN_AG6	i_data(15)
18	GPIO_D15	PIN_AG7	i_data(14)
19	GPIO_D16	PIN_AG8	i_data(17)
20	GPIO_D17	PIN_AF4	i_data(16)
21	GPIO_D18	PIN_AF5	i_data(19)
22	GPIO_D19	PIN_AF6	i_data(18)
23	GPIO_D20	PIN_AF8	i_data(21)
24	GPIO_D21	PIN_AF9	i_data(20)
25	GPIO_D22	PIN_AF10	i_data(23)
26	GPIO_D23	PIN_AE7	i_data(22)
27	GPIO_D24	PIN_AE9	i_data(25)

Table 2 – *Continued on next page*

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GPIO Pin Number	**Cyclone V Signal Name**	**Cyclone V Pin**	**MIPS Signal**
28	GPIO_D25	PIN_AE11	i_data(24)
29	VCC3P3		
30	GND		
31	GPIO_D26	PIN_AE12	i_data(27)
32	GPIO_D27	PIN_AD7	i_data(26)
33	GPIO_D28	PIN_AD9	i_data(29)
34	GPIO_D29	PIN_AD10	i_data(28)
35	GPIO_D30	PIN_AD11	i_data(31)
36	GPIO_D31	PIN_AD12	i_data(30)
37	GPIO_D32	PIN_AC9	i_write_enable
38	GPIO_D33	PIN_AC12	i_read_enable
39	GPIO_D34	PIN_AB12	o_DONE
40	GPIO_D35	PIN_AA12	o_MEM_READY

The next two connections between the processor and Memulator are made using the 2x20 pin GPIO connectors on the daughter board, however the mapping of pins across the HSTC connection between the DE10-Standard and the daughter board must be understood first. For reference, Figure 2 shows the daughterboard. Note that the alignment notch is on the left side of all three 2x20 pin GPIO connectors. Table 3 shows the pin mapping from the DE10-Standard side of the connector to the daughter board side. In the "THDB-HTG Connector" column, the "J#" indicates the name of the 2x20 connector to which a signal is connected. The pin to which the signal is connected is indicated by the associated " - #". The "+" indicates that there is a separate breakout pin connection associated with the connector, but not one of the pins in the 2x20 GPIO connector. Blanks in this column indicates that the signal is not associated with one of the connectors. In Figure 2, the "J#" connectors are labeled as J2, J3, and J4. Also shown are the breakout pins associated with each connector; these are labeled as J2+, J3+, and J4+. Also note that DE10-Standard HSTC Pins 161-172 are all ground pins used to establish a common ground across

the DE10-Standard and daughter board interface.

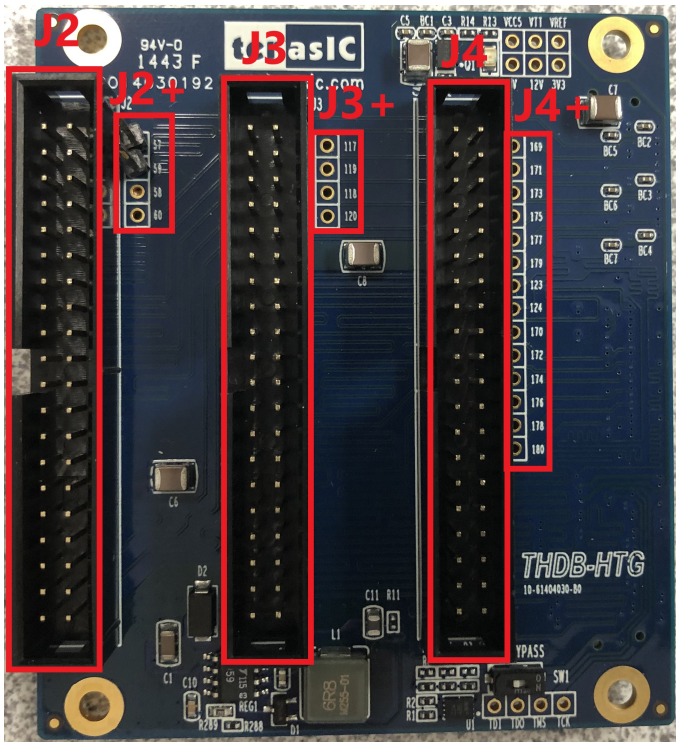

Figure 2. Daughter Board

Table 3. HSTC Connector Pin Mapping from DE10-Standard to Daughter Board

Cyclone V Pin	Cyclone V Signal Name	DE10 Pin	THDB-HTG Pin	THDB-HTG Signal Name	THDB-HTG Connector
		1	179	HSTC_TX_p29	J4+
		2	180	HSTC_RX_p29	J4+
		3	177	HSTC_TX_n29	J4+
		4	178	HSTC_RX_n29	J4+
			175	HSTC_TX_p28	J4+
			176	HSTC_RX_p28	J4+
		5	173	HSTC_TX_n28	J4+
		6	174	HSTC_RX_n28	J4+
		7	171	HSTC_TX_p27	J4+
		8	172	HSTC_RX_p27	J4+
			169	HSTC_TX_n27	J4+
			170	HSTC_RX_n27	J4+
		9	167	HSTC_TX_p26	J4 - 39
		10	168	HSTC_RX_p26	J4 - 36
		11	165	HSTC_TX_n26	J4 - 37
		12	166	HSTC_RX_n26	J4 - 34
			163	HSTC_TX_p25	J4 - 35
			164	HSTC_RX_p25	J4 - 40
		13	161	HSTC_TX_n25	J4 - 33
		14	162	HSTC_RX_n25	J4 - 38
		15	159	HSTC_TX_p24	J4 - 31
		16	160	HSTC_RX_p24	J4 - 32
			157	HSTC_TX_n24	J4 - 27
			158	HSTC_RX_n24	J4 - 28

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Cyclone V Pin	**Cyclone V Signal Name**	**DE10 Pin**	**THDB-HTG Pin**	**THDB-HTG Signal Name**	**THDB-HTG Connector**
		17	155	HSTC_TX_p23	J4 - 25
		18	156	HSTC_RX_p23	J4 - 26
		19	153	HSTC_TX_n23	J4 - 23
		20	154	HSTC_RX_n23	J4 - 24
			151	HSTC_TX_p22	J4 - 21
			152	HSTC_RX_p22	J4 - 22
		21	149	HSTC_TX_n22	J4 - 19
		22	150	HSTC_RX_n22	J4 - 20
		23	147	HSTC_TX_p21	J4 - 17
		24	148	HSTC_RX_p21	J4 - 18
			145	HSTC_TX_n21	J4 - 15
			146	HSTC_RX_n21	J4 - 16
		25	143	HSTC_TX_p20	J4 - 13
		26	144	HSTC_RX_p20	J4 - 14
		27	141	HSTC_TX_n20	J4 - 9
		28	142	HSTC_RX_n20	J4 - 10
			139	HSTC_TX_p19	J4 - 7
			140	HSTC_RX_p19	J4 - 8
		29	137	HSTC_TX_n19	J4 - 5
		30	138	HSTC_RX_n19	J4 - 6
		31	135	HSTC_TX_p18	J4 - 3
		32	136	HSTC_RX_p18	J4 - 4
			133	HSTC_TX_n18	J4 - 1
			134	HSTC_RX_n18	J4 - 2
	HSMC_SDA	33	131	HSTC_SDA	

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Cyclone V Pin	**Cyclone V Signal Name**	**DE10 Pin**	**THDB-HTG Pin**	**THDB-HTG Signal Name**	**THDB-HTG Connector**
	HSMC_SCL	34	132	HSTC_SCL	
	HSMC_TCK	35	129	HSTC_TCK	Breakout
	HSMC_TMS	36	130	HSTC_TMS	Breakout
			127	VREF	
			128	VTT	
	HSMC_TDO	37	125	HSTC_TDO	Breakout
	HSMC_TDI	38	126	HSTC_TDI	Breakout
	HSMC_CLKOUT0	39	123	HSTC_CLKOUT_2	J4+
	HSMC_CLKIN0	40	124	HSTC_CLKIN_2	J4+
			121	POWER_ON	
			122	VCC5	
PIN_C10	HSMC_D0	41	119	HSTC_TX_p17	J3+
PIN_H13	HSMC_D1	42	120	HSTC_RX_p17	J3+
PIN_C9	HSMC_D2	43	117	HSTC_TX_n17	J3+
PIN_H12	HSMC_D3	44	118	HSTC_RX_n17	J3+
	VCC3P3	45	115	3V3	
	VCC12_HSMC	46	116	12V	
PIN_A9	HSMC_TX_D_P0	47	113	HSTC_TX_p16	J3 - 40
PIN_G12	HSMC_RX_D_P0	48	114	HSTC_RX_p16	J3 - 36
PIN_A8	HSMC_TX_D_N0	49	111	HSTC_TX_n16	J3 - 38
PIN_G11	HSMC_RX_D_N0	50	112	HSTC_RX_n16	J3 - 34
	VCC3P3	51	109	3V3	
	VCC12_HSMC	52	110	12V	
PIN_E8	HSMC_TX_D_P1	53	107	HSTC_TX_p15	J3 - 39
PIN_K12	HSMC_RX_D_P1	54	108	HSTC_RX_p15	J3 - 32

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Cyclone V Pin	**Cyclone V Signal Name**	**DE10 Pin**	**THDB-HTG Pin**	**THDB-HTG Signal Name**	**THDB-HTG Connector**
PIN_D7	HSMC_TX_D_N1	55	105	HSTC_TX_n15	J3 - 37
PIN_J12	HSMC_RX_D_N1	56	106	HSTC_RX_n15	J3 - 28
	VCC3P3	57	103	3V3	
	VCC12_HSMC	58	104	12V	
PIN_G7	HSMC_TX_D_P2	59	101	HSTC_TX_p14	J3 - 35
PIN_G10	HSMC_RX_D_P2	60	102	HSTC_RX_p14	J3 - 26
PIN_F6	HSMC_TX_D_N2	61	99	HSTC_TX_n14	J3 - 33
PIN_F10	HSMC_RX_D_N2	62	100	HSTC_RX_n14	J3 - 24
	VCC3P3	63	97	3V3	
	VCC12_HSMC	64	98	12V	
PIN_D6	HSMC_TX_D_P3	65	95	HSTC_TX_p13	J3 - 31
PIN_J10	HSMC_RX_D_P3	66	96	HSTC_RX_p13	J3 - 22
PIN_C5	HSMC_TX_D_N3	67	93	HSTC_TX_n13	J3 - 27
PIN_J9	HSMC_RX_D_N3	68	94	HSTC_RX_n13	J3 - 20
	VCC3P3	69	91	3V3	
	VCC12_HSMC	70	92	12V	
PIN_D5	HSMC_TX_D_P4	71	89	HSTC_TX_p12	J3 - 25
PIN_K7	HSMC_RX_D_P4	72	90	HSTC_RX_p12	J3 - 18
PIN_C4	HSMC_TX_D_N4	73	87	HSTC_TX_n12	J3 - 23
PIN_K8	HSMC_RX_D_N4	74	88	HSTC_RX_n12	J3 - 16
	VCC3P3	75	85	3V3	
	VCC12_HSMC	76	86	12V	
PIN_E3	HSMC_TX_D_P5	77	83	HSTC_TX_p11	J3 - 17
PIN_J7	HSMC_RX_D_P5	78	84	HSTC_RX_p11	J3 - 14
PIN_E2	HSMC_TX_D_N5	79	81	HSTC_TX_n11	J3 - 15

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Cyclone V Pin	**Cyclone V Signal Name**	**DE10 Pin**	**THDB-HTG Pin**	**THDB-HTG Signal Name**	**THDB-HTG Connector**
PIN_H7	HSMC_RX_D_N5	80	82	HSTC_RX_n11	J3 - 10
	VCC3P3	81	79	3V3	
	VCC12_HSMC	82	80	12V	
PIN_E4	HSMC_TX_D_P6	83	77	HSTC_TX_p10	J3 - 13
PIN_H8	HSMC_RX_D_P6	84	78	HSTC_RX_p10	J3 - 8
PIN_D4	HSMC_TX_D_N6	85	75	HSTC_TX_n10	J3 - 9
PIN_G8	HSMC_RX_D_N6	86	76	HSTC_RX_n10	J3 - 6
	VCC3P3	87	73	3V3	
	VCC12_HSMC	88	74	12V	
PIN_C3	HSMC_TX_D_P7	89	71	HSTC_TX_p9	J3 - 7
PIN_F9	HSMC_RX_D_P7	90	72	HSTC_RX_p9	J3 - 4
PIN_B3	HSMC_TX_D_N7	91	69	HSTC_TX_n9	J3 - 5
PIN_F8	HSMC_RX_D_N7	92	70	HSTC_RX_n9	J3 - 2
	VCC3P3	93	67	3V3	
	VCC12_HSMC	94	68	12V	
PIN_E7	HSMC_CLKOUT_P1	95	65	HSTC_CLKOUT_p1	J3 -
21 PIN_AA26	HSMC_CLKIN_P1	96	66	HSTC_CLKIN_p1	J3 - 3
PIN_E6	HSMC_CLKOUT_N1	97	63	HSTC_CLKOUT_n1	J3 - 19
PIN_AB27	HSMC_CLKIN_N1	98	64	HSTC_CLKIN_n1	J3 - 1
	VCC3P3	99	61	3V3	
	VCC12_HSMC	100	62	12V	
PIN_E1	HSMC_TX_D_P8	101	59	HSTC_TX_p8	J2+
PIN_F11	HSMC_RX_D_P8	102	60	HSTC_RX_p8	J2+
PIN_D1	HSMC_TX_D_N8	103	57	HSTC_TX_n8	J2+
PIN_E11	HSMC_RX_D_N8	104	58	HSTC_RX_n8	J2+

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Cyclone V Pin	**Cyclone V Signal Name**	**DE10 Pin**	**THDB-HTG Pin**	**THDB-HTG Signal Name**	**THDB-HTG Connector**
	VCC3P3	105	55	3V3	
	VCC12_HSMC	106	56	12V	
PIN_D2	HSMC_TX_D_P9	107	53	HSTC_TX_p7	J2 - 40
PIN_B6	HSMC_RX_D_P9	108	54	HSTC_RX_p7	J2 - 36
PIN_C2	HSMC_TX_D_N9	109	51	HSTC_TX_n7	J2 - 38
PIN_B5	HSMC_RX_D_N9	110	52	HSTC_RX_n7	J2 - 34
	VCC3P3	111	49	3V3	
	VCC12_HSMC	112	50	12V	
PIN_B2	HSMC_TX_D_P10	113	47	HSTC_TX_p6	J2 - 39
PIN_E9	HSMC_RX_D_P10	114	48	HSTC_RX_p6	J2 - 32
PIN_B1	HSMC_TX_D_N10	115	45	HSTC_TX_n6	J2 - 37
PIN_D9	HSMC_RX_D_N10	116	46	HSTC_RX_n6	J2 - 28
	VCC3P3	117	43	3V3	
	VCC12_HSMC	118	44	12V	
PIN_A4	HSMC_TX_D_P11	119	41	HSTC_TX_p5	J2 - 35
PIN_E12	HSMC_RX_D_P11	120	42	HSTC_RX_p5	J2 - 26
PIN_A3	HSMC_TX_D_N11	121	39	HSTC_TX_n5	J2 - 33
PIN_D12	HSMC_RX_D_N11	122	40	HSTC_RX_n5	J2 - 24
	VCC3P3	123	37	3V3	
	VCC12_HSMC	124	38	12V	
PIN_A6	HSMC_TX_D_P12	125	35	HSTC_TX_p4	J2 - 31
PIN_D11	HSMC_RX_D_P12	126	36	HSTC_RX_p4	J2 - 22
PIN_A5	HSMC_TX_D_N12	127	33	HSTC_TX_n4	J2 - 27
PIN_D10	HSMC_RX_D_N12	128	34	HSTC_RX_n4	J2 - 20
	VCC3P3	129	31	3V3	

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Cyclone V Pin	**Cyclone V Signal Name**	**DE10 Pin**	**THDB-HTG Pin**	**THDB-HTG Signal Name**	**THDB-HTG Connector**
	VCC12_HSMC	130	32	12V	
PIN_C7	HSMC_TX_D_P13	131	29	HSTC_TX_p3	J2 - 25
PIN_C13	HSMC_RX_D_P13	132	30	HSTC_RX_p3	J2 - 18
PIN_B7	HSMC_TX_D_N13	133	27	HSTC_TX_n3	J2 - 23
PIN_B12	HSMC_RX_D_N13	134	28	HSTC_RX_n3	J2 - 16
	VCC3P3	135	25	3V3	
	VCC12_HSMC	136	26	12V	
PIN_C8	HSMC_TX_D_P14	137	23	HSTC_TX_p2	J2 - 17
PIN_F13	HSMC_RX_D_P14	138	24	HSTC_RX_p2	J2 - 14
PIN_B8	HSMC_TX_D_N14	139	21	HSTC_TX_n2	J2 - 15
PIN_E13	HSMC_RX_D_N14	140	22	HSTC_RX_n2	J2 - 10
	VCC3P3	141	19	3V3	
	VCC12_HSMC	142	20	12V	
PIN_C12	HSMC_TX_D_P15	143	17	HSTC_TX_p1	J2 - 13
PIN_H14	HSMC_RX_D_P15	144	18	HSTC_RX_p1	J2 - 8
PIN_B11	HSMC_TX_D_N15	145	15	HSTC_TX_n1	J2 - 9
PIN_G13	HSMC_RX_D_N15	146	16	HSTC_RX_n1	J2 - 6
	VCC3P3	147	13	3V3	
	VCC12_HSMC	148	14	12V	
PIN_B13	HSMC_TX_D_P16	149	11	HSTC_TX_p0	J2 - 7
PIN_F15	HSMC_RX_D_P16	150	12	HSTC_RX_p0	J2 - 4
PIN_A13	HSMC_TX_D_N16	151	9	HSTC_TX_n0	J2 - 5
PIN_F14	HSMC_RX_D_N16	152	10	HSTC_RX_n0	J2 - 2
	VCC3P3	153	7	3V3	
	VCC12_HSMC	154	8	12V	

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Cyclone V Pin	**Cyclone V Signal Name**	**DE10 Pin**	**THDB-HTG Pin**	**THDB-HTG Signal Name**	**THDB-HTG Connector**
PIN_A11	HSMC_CLKOUT_P2	155	5	HSTC_CLKOUT_p0	J2 - 21
PIN_H15	HSMC_CLKIN_P2	156	6	HSTC_CLKIN_p0	J2 - 3
PIN_A10	HSMC_CLKOUT_N2	157	3	HSTC_CLKOUT_n0	J2 - 19
PIN_G15	HSMC_CLKIN_N2	158	4	HSTC_CLKIN_n0	J2 - 1
	VCC3P3	159	1	3V3	
	HSMC_PSNT_n	160	2	GND	
	GND	161	192	GND	
	GND	162	191	GND	
	GND	163	190	GND	
	GND	164	189	GND	
	GND	165	188	GND	
	GND	166	187	GND	
	GND	167	186	GND	
	GND	168	185	GND	
	GND	169	184	GND	
	GND	170	183	GND	
	GND	171	182	GND	
	GND	172	181	GND	

Figure 3 shows the pinout of a daughter card GPIO connector as viewed from above. Table 4 shows the MIPS processor signals associated with the daughter board GPIO connectors for the DE10-Standard running the MIPS processor. Similarly, Table 5 shows the Memulator signals associated with the daughter board GPIO connectors for the DE10-Standard running the Memulator. Also note that the processor uses the signal names i_MEM_OUT and o_MEM_ADDRESS where the Memulator uses o_data and i_address respectively. The inputs and outputs denoted by "i" and "o" are also swapped between the two tables because the MIPS processor's output is the Memulator's input and vice versa. Table 5 also includes the breakout pins used to articulate the error signal which is recorded by a laptop computer and the done signal measured by an oscilloscope to record timing information. While the signal here is called o_DONE2, it is identical to the o_DONE signal transmitted on the DE10-Standard GPIO connector.

As was done for the GPIO connectors on the DE10-Standard board, the ground pins (GPIO pins 12 and 30) are connected while the VCC pins (GPIO pins 11 and 29) are left unconnected for the daughter board GPIO connectors. Additionally, the clock signals are also left unconnected as these signals are unused.

Figure 3. Daughter Board GPIO Connector

Table 4. MIPS Processor Daughter Board GPIO Connector Pinout

GPIO Pin Number	Cyclone V Signal Name	Cyclone V Pin	MIPS Signal
J2 - 1	HSMC_CLKIN_N2	PIN_G15	
J2 - 2	HSMC_RX_D_N16	PIN_F14	i_MEM_OUT(0)
J2 - 3	HSMC_CLKIN_P2	PIN_H15	
J2 - 4	HSMC_RX_D_P16	PIN_F15	i_MEM_OUT(1)
J2 - 5	HSMC_TX_D_N16	PIN_A13	o_MEM_ADDRESS(0)
J2 - 6	HSMC_RX_D_N15	PIN_G13	i_MEM_OUT(2)
J2 - 7	HSMC_TX_D_P16	PIN_B13	o_MEM_ADDRESS(1)
J2 - 8	HSMC_RX_D_P15	PIN_H14	i_MEM_OUT(3)
J2 - 9	HSMC_TX_D_N15	PIN_B11	o_MEM_ADDRESS(2)
J2 - 10	HSMC_RX_D_N14	PIN_E13	i_MEM_OUT(4)
J2 - 11	VCC5		
J2 - 12	GND		
J2 - 13	HSMC_TX_D_P15	PIN_C12	o_MEM_ADDRESS(3)
J2 - 14	HSMC_RX_D_P14	PIN_F13	i_MEM_OUT(5)

Table 4 – *Continued on next page*

Table 4 – *Continued from previous page*

GPIO Pin Number	**Cyclone V Signal Name**	**Cyclone V Pin**	**MIPS Signal**
J2 - 15	HSMC_TX_D_N14	PIN_B8	o_MEM_ADDRESS(4)
J2 - 16	HSMC_RX_D_N13	PIN_B12	i_MEM_OUT(6)
J2 - 17	HSMC_TX_D_P14	PIN_C8	o_MEM_ADDRESS(5)
J2 - 18	HSMC_RX_D_P13	PIN_C13	i_MEM_OUT(7)
J2 - 19	GPIO_CLKOUT_N2	PIN_A10	
J2 - 20	HSMC_RX_D_N12	PIN_D10	i_MEM_OUT(8)
J2 - 21	HSMC_CLKOUT_P2	PIN_A11	
J2 - 22	HSMC_RX_D_P12	PIN_D11	i_MEM_OUT(9)
J2 - 23	HSMC_TX_D_N13	PIN_B7	o_MEM_ADDRESS(6)
J2 - 24	HSMC_RX_D_N11	PIN_D12	i_MEM_OUT(10)
J2 - 25	HSMC_TX_D_P13	PIN_C7	o_MEM_ADDRESS(7)
J2 - 26	HSMC_RX_D_P11	PIN_E12	i_MEM_OUT(11)
J2 - 27	HSMC_TX_D_N12	PIN_A5	o_MEM_ADDRESS(8)
J2 - 28	HSMC_RX_D_N10	PIN_D9	i_MEM_OUT(12)
J2 - 29	VCC3P3		
J2 - 30	GND		
J2 - 31	HSMC_TX_D_P12	PIN_A6	o_MEM_ADDRESS(9)
J2 - 32	HSMC_RX_D_P10	PIN_E9	i_MEM_OUT(13)
J2 - 33	HSMC_TX_D_N11	PIN_A3	o_MEM_ADDRESS(10)
J2 - 34	HSMC_RX_D_N9	PIN_B5	i_MEM_OUT(14)
J2 - 35	HSMC_TX_D_P11	PIN_A4	o_MEM_ADDRESS(11)
J2 - 36	HSMC_RX_D_P9	PIN_B6	i_MEM_OUT(15)
J2 - 37	HSMC_TX_D_N10	PIN_B1	o_MEM_ADDRESS(12)
J2 - 38	HSMC_TX_D_N9	PIN_C2	o_MEM_ADDRESS(13)
J2 - 39	HSMC_TX_D_P10	PIN_B2	o_MEM_ADDRESS(14)
J2 - 40	HSMC_TX_D_P9	PIN_D2	o_MEM_ADDRESS(15)
J3 - 1	HSMC_CLKIN_N1	PIN_AB27	
J3 - 2	HSMC_RX_D_N7	PIN_F8	i_MEM_OUT(16)
J3 - 3	HSMC_CLKIN_P1	PIN_AA26	
J3 - 4	HSMC_RX_D_P7	PIN_F9	i_MEM_OUT(17)
J3 - 5	HSMC_TX_D_N7	PIN_B3	o_MEM_ADDRESS(16)
J3 - 6	HSMC_RX_D_N6	PIN_G8	i_MEM_OUT(18)
J3 - 7	HSMC_TX_D_P7	PIN_C3	o_MEM_ADDRESS(17)
J3 - 8	HSMC_RX_D_P6	PIN_H8	i_MEM_OUT(19)
J3 - 9	HSMC_TX_D_N6	PIN_D4	o_MEM_ADDRESS(18)
J3 - 10	HSMC_RX_D_N5	PIN_H7	i_MEM_OUT(20)
J3 - 11	VCC5		
J3 - 12	GND		

Table 4 – *Continued on next page*

Table 4 – *Continued from previous page*

GPIO Pin Number	**Cyclone V Signal Name**	**Cyclone V Pin**	**MIPS Signal**
J3 - 13	HSMC_TX_D_P6	PIN_E4	o_MEM_ADDRESS(19)
J3 - 14	HSMC_RX_D_P5	PIN_J7	i_MEM_OUT(21)
J3 - 15	HSMC_TX_D_N5	PIN_E2	o_MEM_ADDRESS(20)
J3 - 16	HSMC_RX_D_N4	PIN_K8	i_MEM_OUT(22)
J3 - 17	HSMC_TX_D_P5	PIN_E3	o_MEM_ADDRESS(21)
J3 - 18	HSMC_RX_D_P4	PIN_K7	i_MEM_OUT(23)
J3 - 19	GPIO_CLKOUT_N1	PIN_E6	
J3 - 20	HSMC_RX_D_N3	PIN_J9	i_MEM_OUT(24)
J3 - 21	HSMC_CLKOUT_P1	PIN_E7	
J3 - 22	HSMC_RX_D_P3	PIN_J10	i_MEM_OUT(25)
J3 - 23	HSMC_TX_D_N4	PIN_C4	o_MEM_ADDRESS(22)
J3 - 24	HSMC_RX_D_N2	PIN_F10	i_MEM_OUT(26)
J3 - 25	HSMC_TX_D_P4	PIN_D5	o_MEM_ADDRESS(23)
J3 - 26	HSMC_RX_D_P2	PIN_G10	i_MEM_OUT(27)
J3 - 27	HSMC_TX_D_N3	PIN_C5	o_MEM_ADDRESS(24)
J3 - 28	HSMC_RX_D_N1	PIN_J12	i_MEM_OUT(28)
J3 - 29	VCC3P3		
J3 - 30	GND		
J3 - 31	HSMC_TX_D_P3	PIN_D6	o_MEM_ADDRESS(25)
J3 - 32	HSMC_RX_D_P1	PIN_K12	i_MEM_OUT(29)
J3 - 33	HSMC_TX_D_N2	PIN_F6	o_MEM_ADDRESS(26)
J3 - 34	HSMC_RX_D_N0	PIN_G11	i_MEM_OUT(30)
J3 - 35	HSMC_TX_D_P2	PIN_G7	o_MEM_ADDRESS(27)
J3 - 36	HSMC_RX_D_P0	PIN_G12	i_MEM_OUT(31)
J3 - 37	HSMC_TX_D_N1	PIN_D7	o_MEM_ADDRESS(28)
J3 - 38	HSMC_TX_D_N0	PIN_A8	o_MEM_ADDRESS(29)
J3 - 39	HSMC_TX_D_P1	PIN_E8	o_MEM_ADDRESS(30)
J3 - 40	HSMC_TX_D_P0	PIN_A9	o_MEM_ADDRESS(31)

Table 5. Memulator Daughter Board GPIO Connector Pinout

GPIO Pin Number	Cyclone V Signal Name	Cyclone V Pin	Memulator Signal
J2 - 1	HSMC_CLKIN_N2	PIN_G15	
J2 - 2	HSMC_RX_D_N16	PIN_F14	i_address(12)
J2 - 3	HSMC_CLKIN_P2	PIN_H15	
J2 - 4	HSMC_RX_D_P16	PIN_F15	i_address(14)
J2 - 5	HSMC_TX_D_N16	PIN_A13	o_data(2)
J2 - 6	HSMC_RX_D_N15	PIN_G13	i_address(0)
J2 - 7	HSMC_TX_D_P16	PIN_B13	o_data(3)
J2 - 8	HSMC_RX_D_P15	PIN_H14	i_address(1)
J2 - 9	HSMC_TX_D_N15	PIN_B11	o_data(4)
J2 - 10	HSMC_RX_D_N14	PIN_E13	i_address(2)
J2 - 11	VCC5		
J2 - 12	GND		
J2 - 13	HSMC_TX_D_P15	PIN_C12	o_data(5)
J2 - 14	HSMC_RX_D_P14	PIN_F13	i_address(3)
J2 - 15	HSMC_TX_D_N14	PIN_B8	o_data(6)
J2 - 16	HSMC_RX_D_N13	PIN_B12	i_address(4)
J2 - 17	HSMC_TX_D_P14	PIN_C8	o_data(7)
J2 - 18	HSMC_RX_D_P13	PIN_C13	i_address(5)
J2 - 19	GPIO_CLKOUT_N2	PIN_A10	
J2 - 20	HSMC_RX_D_N12	PIN_D10	i_address(13)
J2 - 21	HSMC_CLKOUT_P2	PIN_A11	
J2 - 22	HSMC_RX_D_P12	PIN_D11	i_address(15)
J2 - 23	HSMC_TX_D_N13	PIN_B7	o_data(10)
J2 - 24	HSMC_RX_D_N11	PIN_D12	i_address(6)
J2 - 25	HSMC_TX_D_P13	PIN_C7	o_data(11)
J2 - 26	HSMC_RX_D_P11	PIN_E12	i_address(7)
J2 - 27	HSMC_TX_D_N12	PIN_A5	o_data(12)
J2 - 28	HSMC_RX_D_N10	PIN_D9	i_address(8)
J2 - 29	VCC3P3		
J2 - 30	GND		
J2 - 31	HSMC_TX_D_P12	PIN_A6	o_data(13)
J2 - 32	HSMC_RX_D_P10	PIN_E9	i_address(9)
J2 - 33	HSMC_TX_D_N11	PIN_A3	o_data(14)
J2 - 34	HSMC_RX_D_N9	PIN_B5	i_address(10)
J2 - 35	HSMC_TX_D_P11	PIN_A4	o_data(15)
J2 - 36	HSMC_RX_D_P9	PIN_B6	i_address(11)
J2 - 37	HSMC_TX_D_N10	PIN_B1	o_data(0)
J2 - 38	HSMC_TX_D_N9	PIN_C2	o_data(8)

Table 5 – *Continued on next page*

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GPIO Pin Number	**Cyclone V Signal Name**	**Cyclone V Pin**	**Memulator Signal**
J2 - 39	HSMC_TX_D_P10	PIN_B2	o_data(1)
J2 - 40	HSMC_TX_D_P9	PIN_D2	o_data(9)
J2+	HSMC_TX_D_P8	PIN_E1	o_zero
J2+	HSMC_RX_D_P8	PIN_F11	
J2+	HSMC_TX_D_N8	PIN_D1	o_UART_ERROR
J2+	HSMC_TX_D_N8	PIN_E11	
J3 - 1	HSMC_CLKIN_N1	PIN_AB27	
J3 - 2	HSMC_RX_D_N7	PIN_F8	i_address(28)
J3 - 3	HSMC_CLKIN_P1	PIN_AA26	
J3 - 4	HSMC_RX_D_P7	PIN_F9	i_address(30)
J3 - 5	HSMC_TX_D_N7	PIN_B3	o_data(18)
J3 - 6	HSMC_RX_D_N6	PIN_G8	i_address(16)
J3 - 7	HSMC_TX_D_P7	PIN_C3	o_data(19)
J3 - 8	HSMC_RX_D_P6	PIN_H8	i_address(17)
J3 - 9	HSMC_TX_D_N6	PIN_D4	o_data(20)
J3 - 10	HSMC_RX_D_N5	PIN_H7	i_address(18)
J3 - 11	VCC5		
J3 - 12	GND		
J3 - 13	HSMC_TX_D_P6	PIN_E4	o_data(21)
J3 - 14	HSMC_RX_D_P5	PIN_J7	i_address(19)
J3 - 15	HSMC_TX_D_N5	PIN_E2	o_data(22)
J3 - 16	HSMC_RX_D_N4	PIN_K8	i_address(20)
J3 - 17	HSMC_TX_D_P5	PIN_E3	o_data(23)
J3 - 18	HSMC_RX_D_P4	PIN_K7	i_address(21)
J3 - 19	GPIO_CLKOUT_N1	PIN_E6	
J3 - 20	HSMC_RX_D_N3	PIN_J9	i_address(29)
J3 - 21	HSMC_CLKOUT_P1	PIN_E7	
J3 - 22	HSMC_RX_D_P3	PIN_J10	i_address(31)
J3 - 23	HSMC_TX_D_N4	PIN_C4	o_data(26)
J3 - 24	HSMC_RX_D_N2	PIN_F10	i_address(22)
J3 - 25	HSMC_TX_D_P4	PIN_D5	o_data(27)
J3 - 26	HSMC_RX_D_P2	PIN_G10	i_address(23)
J3 - 27	HSMC_TX_D_N3	PIN_C5	o_data(28)
J3 - 28	HSMC_RX_D_N1	PIN_J12	i_address(24)
J3 - 29	VCC3P3		
J3 - 30	GND		
J3 - 31	HSMC_TX_D_P3	PIN_D6	o_data(29)
J3 - 32	HSMC_RX_D_P1	PIN_K12	i_address(25)

Table 5 – *Continued on next page*

Table 5 – *Continued from previous page*

GPIO Pin Number	**Cyclone V Signal Name**	**Cyclone V Pin**	**Memulator Signal**
J3 - 33	HSMC_TX_D_N2	PIN_F6	o_data(30)
J3 - 34	HSMC_RX_D_N0	PIN_G11	i_address(26)
J3 - 35	HSMC_TX_D_P2	PIN_G7	o_data(31)
J3 - 36	HSMC_RX_D_P0	PIN_G12	i_address(27)
J3 - 37	HSMC_TX_D_N1	PIN_D7	o_data(16)
J3 - 38	HSMC_TX_D_N0	PIN_A8	o_data(24)
J3 - 39	HSMC_TX_D_P1	PIN_E8	o_data(17)
J3 - 40	HSMC_TX_D_P0	PIN_A9	o_data(25)
J3+	HSMC_D0	PIN_C10	o_DONE2
J3+	HSMC_D1	PIN_H13	
J3+	HSMC_D2	PIN_C9	
J3+	HSMC_D3	PIN_H12	

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14. ABSTRACT

This report describes in detail the pins and connections for the Basic MIPS architecture on a Terrasic DE10-Standard board utilizing an Intel Cyclone V FPGA. The connections between one DE10-Standard running Basic MIPS, Temporal Software Redundancy (TSR) MIPS, Triple Modular Redundancy (TMR) MIPS, or Adaptive-Hybrid Redundancy (AHR) MIPS and a second DE10-Standard storing a program in a memory emulator.

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