ARL-TN-0984 ● Nov 2019

The Design of a Multichannel Time Interval Measurement Interface Box

by Michael L Don, Kenneth E Pugh, Barry J Kline, and Jonathan M Hallameyer

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REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

1. REPORT DATE *(DD-MM-YYYY)*	2. REPORT TYPE	3. DATES COVERED (From - To)
November 2019	Technical Note	December 2018–February 2019

4. TITLE AND SUBTITLE
The Design of a Multichannel Time Interval Measurement Interface Box

5a. CONTRACT NUMBER

5b. GRANT NUMBER

5c. PROGRAM ELEMENT NUMBER

6. AUTHOR(S)
Michael L Don, Kenneth E Pugh, Barry J Kline, and Jonathan M Hallameyer

5d. PROJECT NUMBER

5e. TASK NUMBER

5f. WORK UNIT NUMBER

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
CCDC Army Research Laboratory
ATTN: FCDD-RLW-LF
Aberdeen Proving Ground, MD 21005-5066

8. PERFORMING ORGANIZATION REPORT NUMBER
ARL-TN-0984

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)

10. SPONSOR/MONITOR'S ACRONYM(S)

11. SPONSOR/MONITOR'S REPORT NUMBER(S)

12. DISTRIBUTION/AVAILABILITY STATEMENT
Approved for public release; distribution is unlimited.

13. SUPPLEMENTARY NOTES
ORCID ID(s): Michael Don, 0000-0002-8021-9066

14. ABSTRACT
Precise time interval measurement is required for a number of applications including clock stability analysis, time-of-flight measurements, and particle physics. Commercial time interval measurement devices can achieve picosecond resolution but are expensive, especially for multichannel applications. In previous research, the US Army Combat Capabilities Development Command Army Research Laboratory demonstrated 10-ns resolution on 10 channels using a low-cost field-programmable gate array (FPGA) suitable for pulse-per-second monitoring. This technical note details the design of an interface box for this FPGA device, enabling practical time interval measurement with a variety of input signals. The purpose of this note is twofold: 1) to document the interface box to allow for easy use and future modifications and 2) to provide a reference to facilitate the construction of other interface units, including design advice and lessons learned.

15. SUBJECT TERMS
time interval measurement, field-programmable gate array, FPGA, pulse per second, test and measurement, electronic interface

16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT	18. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON
a. REPORT	b. ABSTRACT	c. THIS PAGE			Michael L Don
Unclassified	Unclassified	Unclassified	UU	22	19b. TELEPHONE NUMBER (Include area code) 410-306-0775

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Acknowledgments

The authors would like to thank the following people from the US Army Combat Capabilities Development Command Army Research Laboratory for their help with this project:

- Steve Buggs for his help with assembling the circuit boards
- Mark Ilg for his consultations, which simplified the system design

1. Introduction

Precise time interval measurement is required for a number of applications including clock stability analysis, time-of-flight measurements, and particle physics.[1] Commercial time interval measurement devices can achieve picosecond resolution[2] but are expensive, especially for multichannel applications. In previous research, the US Army Combat Capabilities Development Command Army Research Laboratory demonstrated 10-ns resolution on 10 channels using a low-cost field-programmable gate array (FPGA) suitable for pulse-per-second (PPS) monitoring.[3] This technical note details the design of an interface box for this FPGA device, enabling practical time interval measurement with a variety of input signals. The purpose of this note is twofold: 1) to document the interface box to allow for easy use and future modifications and 2) to provide a reference to facilitate the construction of other interface units, including design advice and lessons learned.

This note is organized as follows. First, the system requirements are reviewed. Next, the electrical and mechanical design is presented. Then the unit assembly is described along with the testing procedure. Finally, the entire design process is reviewed, noting both good decisions that should be repeated in other projects as well as mistakes to be avoided in the future.

2. System Requirements

The system is required to measure the interval between the rising edge of a reference signal to the rising edges of 10 input signals with a 10-ns accuracy. Although a variety of signals may be measured, the intended use is to compare 10 PPS signals to a reference PPS. Both the reference PPS and input PPS signals generally conform to the following characteristics:

- Load: 50 Ω or high impedance
- Pulse high width: 20 μs ± 20%
- Steady-state pulse high voltage: +3.0 to +5.5 V
- Steady-state pulse low voltage: 0.0 to +0.5 V
- Pulse rise time: 50 ns maximum, measured from 10% to 90% amplitude
- Pulse fall time: 1 μs maximum, measured from 10% to 90% amplitude

In addition, it is possible that some nonstandard input signals may have amplitudes as high as 12 V. In order to balance functionality with complexity, two threshold values are selectable for the midpoint of standard 3-V and 5-V signals. Higher

voltage nonstandard signals share the 5-V threshold. A 10-MHz atomic clock signal is used as a reference to generate the 100-MHz FPGA clock. The input clock signal is an AC-coupled sine wave with a 3-Vpp amplitude. Specifications of the computer interface and data structure have been documented in previous research.[3]

3. Design

3.1 Electrical Design

Figure 1 shows a top-level schematic of the overall design. An off-board 3.3-V AC/DC converter supplies power to the system through connector J20. The Analog Devices LTC6957 clock buffer integrated circuit converts the input sinusoidal atomic clock signal to 3.3-V complementary metal–oxide semiconductor (CMOS) logic levels. Resistors R14 and R15 divide the input voltage to ensure it is below the 2-Vpp limit while presenting a 50-Ω input impedance. The FiltA and FiltB clock buffer inputs are determined by the clock input signal's slew rate given by

$$r_{slew} = \pi f v, \tag{1}$$

where f is the frequency in megahertz, v is the Vpp in volts, and r_{slew} is the slew rate in volts per microsecond.[4] Assuming a 10-MHz, 3-Vpp input clock signal that is divided down to 1.5 Vpp, the slew rate is approximately 47 V/µs. This determines the FlitA and FiltB settings as low and high, respectively, as outlined in the clock buffer specification.[5] Connectors J1 and J2 hold the FPGA board, which processes all of the input signals and provides USB connectivity for data readout.

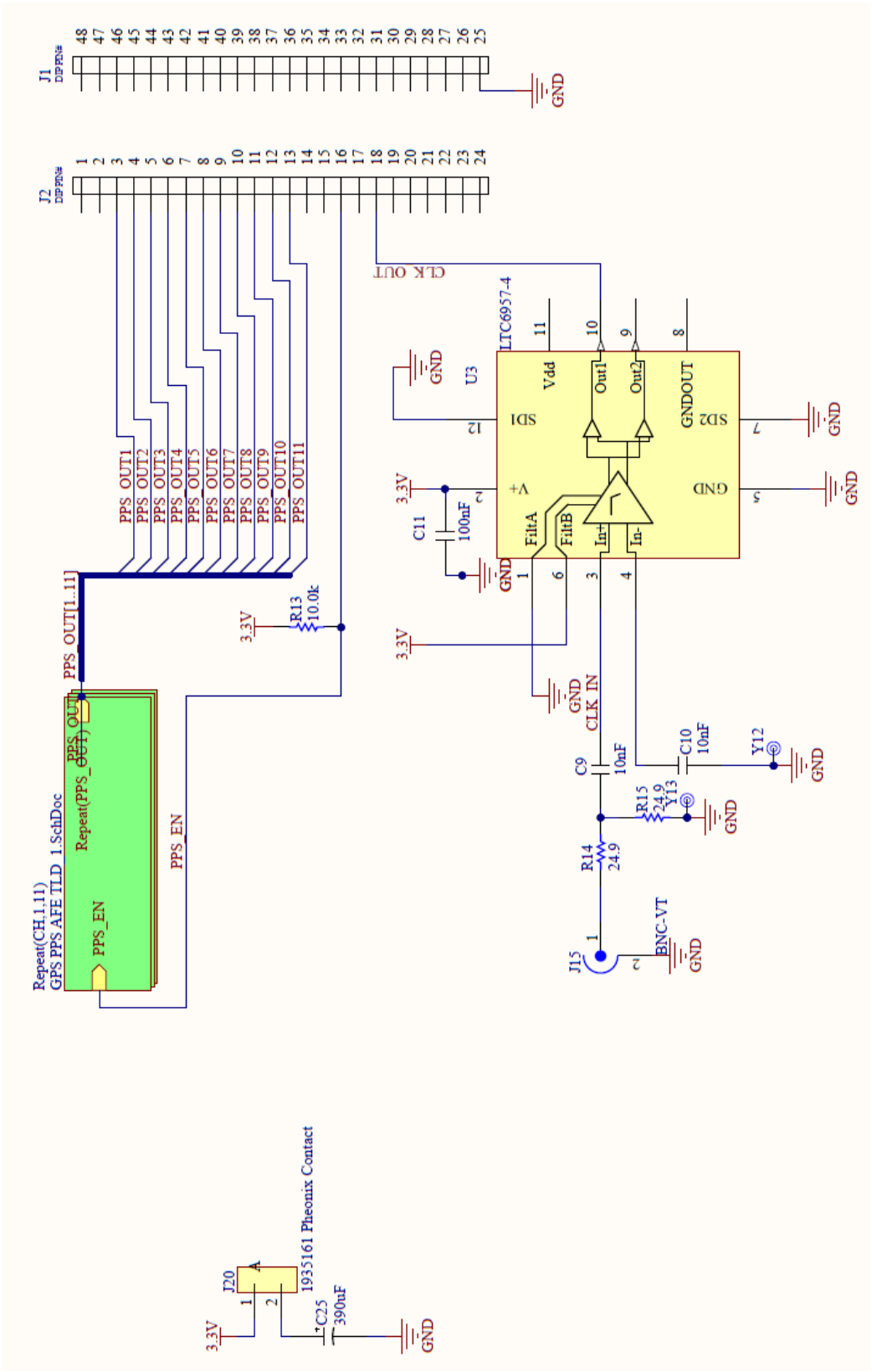

Fig. 1 Top-level schematic

Figure 2 shows a schematic of the circuit for the 11 input signals (the reference signal is treated the same as the other inputs). R4 through R7 with the associated capacitors divide the input signal voltage by 4 on wire PPS_DIV4, allowing the circuit to handle input voltages up to 13.2 V. For additional protection, the transistor Q1 and Zener diode U1 form an over-voltage protection circuit on PPS_DIV4. Switch SW1 connects or disconnects a 50-Ω load for a 50-Ω or high-impedance input, respectively. Comparator U2 uses threshold voltages selectable by switch SW2 that are suitable for either 3-V or 5-V input signals. The FPGA board controls the PPS_EN signal to ensure that the comparator is only enabled after the FPGA board is powered. The bill of materials (BOM) is displayed in Tables 1 and 2.

Altium Designer was used for the schematic and printed circuit board (PCB) layout.[6] To make the layout less tedious, a multichannel design layout was used to create an input signal circuit module, which was instantiated for the entire 11-signal input channel, automatically assigning unique designators for all repeated components. During PCB layout, the Copy Room Format function allowed this module to be automatically copied for each channel.

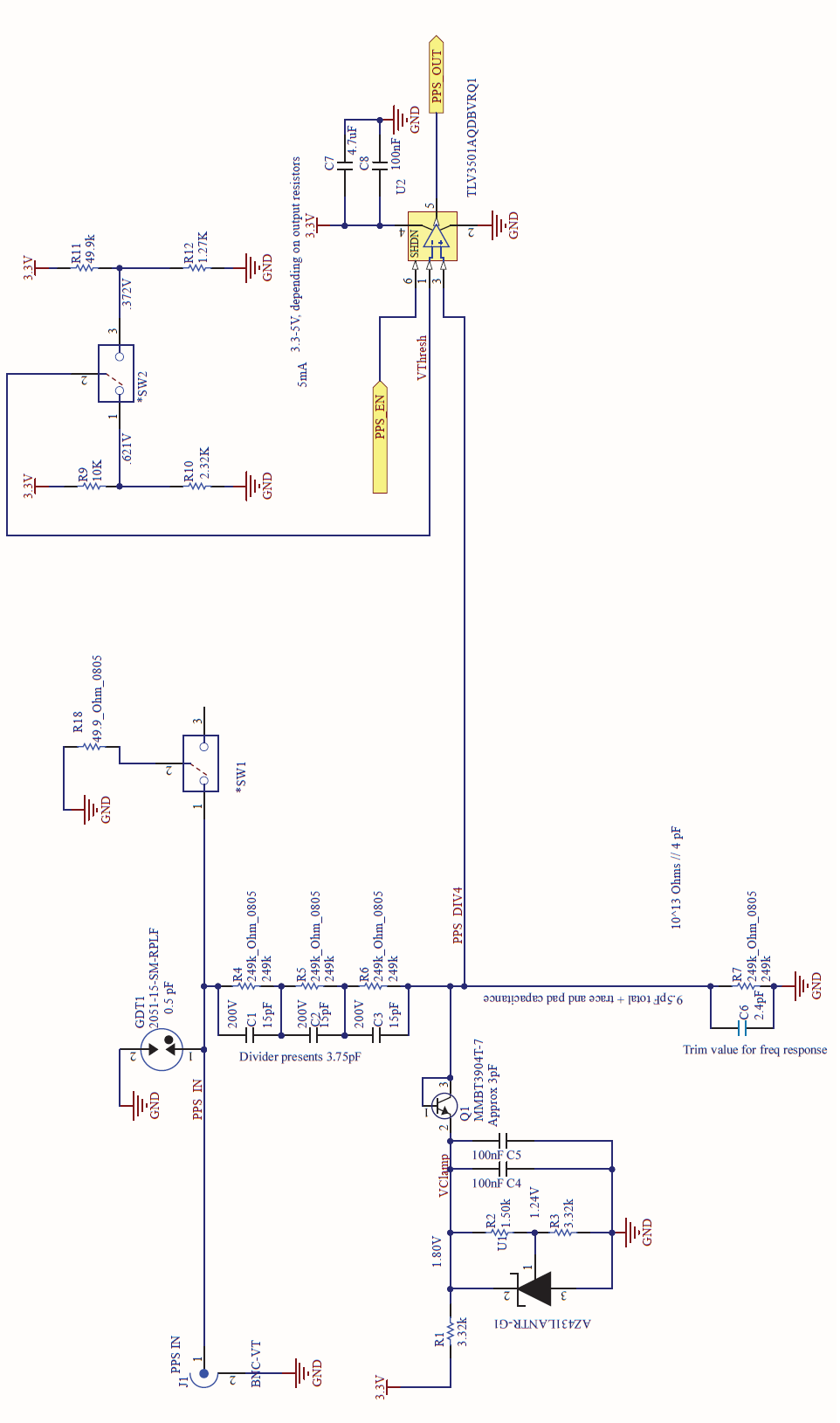

Fig. 2 Channel schematic

Table 1 PCB BOM

Name	Description	Designator [a]	Quantity
NKK_M2013SS1W03	Switch Toggle SPDT 6A 125V	SW1,SW2 (CH)	22
15pF_0603_200V_NP0	Cap 15pF 0603 200V NP0	C1-3 (CH)	33
100nF_0402_16V_X7R	Cap, 100nF 0402 16V X7R	C4,C5,C8 (CH), C11	34
2.4pF_0402_50V_NP0	Cap, 2.4pF 0402 50V NP0	C6 (CH)	11
4.7uF_0805_16V_X7R	Cap, 4.7uF 0805 16V X7R	C7 (CH)	11
10nF_0805_16V_PPS	Cap, 10nF 0805 16V PPS	C9, C10	2
390uF	Cap, AL, 35V, 390uF, 8mmDiax10H	C25	1
2051-15-SM-RPLF	GDT, 150V, 0.5pF, 2kA 1812 SMD	GDT1 (CH)	11
HDR_1*24_VRT_0.1"_Unshrd	HDR_1*24_VRT_0.1"_Unshrd	J1, J2	2
BNC-VT	Conn, BNC JACK Vert 50ohm PCB	J1 (CH), J15	12
1935161 Phoenix Contact	PCB terminal block TH 2 position	J20	1
MMBT3904T-7	Trans-BJT, 40V, 200mA, NPN	Q1 (CH)	11
3.32k_Ohm_0402	Res, 3.32k_Ohm_0402 1%	R1,R3 (CH)	22
1.50k_Ohm_0402	Res, 1.50k_Ohm_0402 1%	R2 (CH)	11
249k_Ohm_0805	Res, 249k_Ohm_0805 1%	R4-7 (CH)	55
49.9k_Ohm_0402	Res, 49.9k_Ohm_0402 1%	R9-12 (CH)	44
10.0k_Ohm_0402	Res, 10.0k_Ohm_0402 1%	R13	1
24.9_Ohm_0402	Res, 24.9_Ohm_0402 1%	R14, R15	2
49.9_Ohm_0805	Res, 49.9_Ohm_0805 1%	R18 (CH)	11
AZ431LANTR-G1	IC-VReg, Shunt, Adjustable, 0.5%	U1 (CH)	11
TLV3501AQDBVRQ1	IC-Analog, Single, 4.5ns	U2 (CH)	11
LTC6957-4	IC, Clk Converter/Buffer, CMOS	U3	1

[a] (CH) designates that the designators exist for each input channel.

Table 2 Off-board BOM

Name	Description	Quantity
P937 USB cable	Panel Mount USB Cable - B Female to Micro-B Male	1
VSK-S20-3R3U-T	AC/DC CONVERTER 3.3 V 20 W	1
Qualtek 764-00/002	AC Power Entry Module Screw	1
Cmod A7	Digilent Artix-7 FPGA Module	1

3.2 Mechanical Design

The interface box mechanical architecture was designed into a Pelican 1450 size case (Fig. 3).[7] This model was deemed sufficiently sized for the number of connections required for the PPS box. This style case can accept an interior panel as an accessory, and this panel can be used to mount electrical interface components such as switches, indicators, and connectors. Below the panel, circuit boards and other electrical components, such as regulators and transformers, are housed.

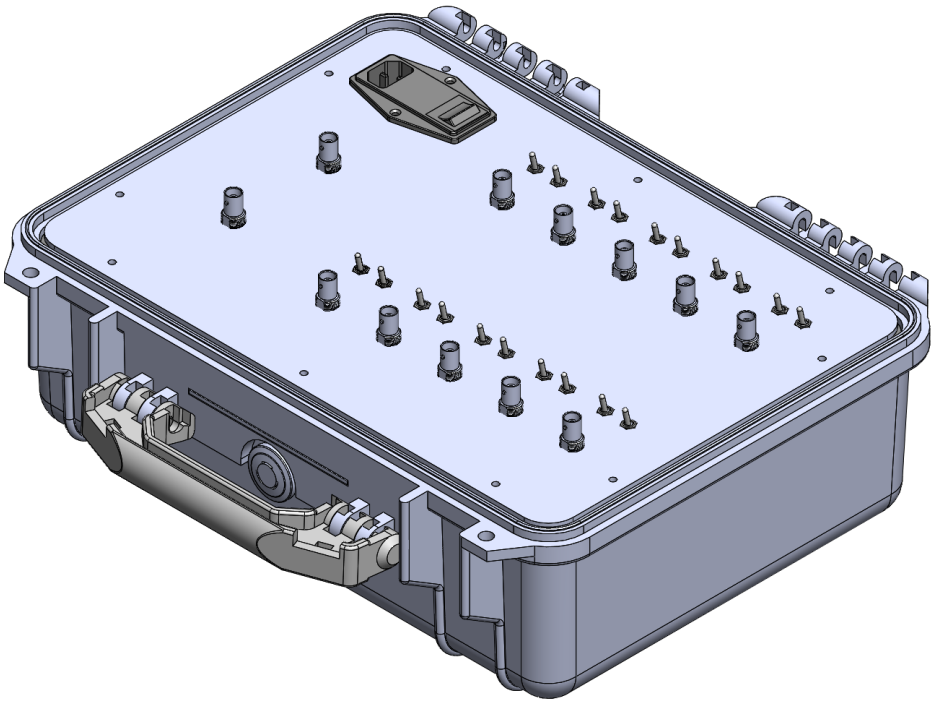

Fig. 3 SolidWorks model of PPS box showing panel and interface components

A novel approach to this mechanical design was to suspend the main circuit board below the panel using the many BNC connectors as standoffs. This approach removed the need to have wires connecting the components on the panel and the circuit card below them, greatly simplifying assembly.

A label for the box was an important part of the mechanical design as the function of all the switches would not be known without it. The label was produced by Image 360 in Aberdeen, Maryland, based on a scale PDF of the panel, a list of required labels, and the originations logos.[8] A finished interface box is shown in Fig. 4.

Fig. 4 Finished interface box

4. Assembly and Testing

4.1 Assembly

The steps for assembling the PPS box are as follows:

1. Remove lid pins and lid from Pelican 1450.
2. Install panel frame in Pelican 1450 with the included screws.
3. Populate circuit board with a pick and place machine as required by the schematic and bill of materials.
4. Attach BNCs and switches to the panel.
5. Solder those components to the circuit board using the panel as a guide.
6. Install FPGA board and USB cable.
7. Install the power transformer and connect it to the AC connector.
8. Install entire assembly into pelican case and attach it to the panel frame.

4.2 Testing

The purpose of the interface box testing was to verify the proper operation of all of the switches and USB connection. The functional verification of the design has already been performed during the FPGA development.[3] Figure 5 shows the interface box test setup. Hewlett Packard 33120A waveform generators were used to produce the input signals. The clock signal was set to a 10-MHz, 3-Vpp, 0-V offset sine wave. The PPS signals were set to 1-Hz, 8-Vpp, 4-V offset sine wave. The large input voltage setting was necessary since the waveform generators were not designed to drive a 5-Ω load. The PPS signals were configured as sine waves so that a change in signal amplitude would translate into a time delay. During testing, the switches were cycled through the five states in Table 3 to verify the operation of all of the switch settings. Table 3 also lists the expected result when transitioning from the previous state. Since the results are measured with respect to a 1-Hz signal, results near 0 or 1 are close to each other, both representing transitions close to the reference signal. Tables 4 and 5 list example interval readings for each state of the two boxes. Inspecting the recorded times and comparing them to the expected results show that all of the switch modes operate as expected. Changes from close to 0.99 in state 1 to 0.14 in state 2 also represent an interval increase, since the measured delay wraps back to 0 once it passes 1.

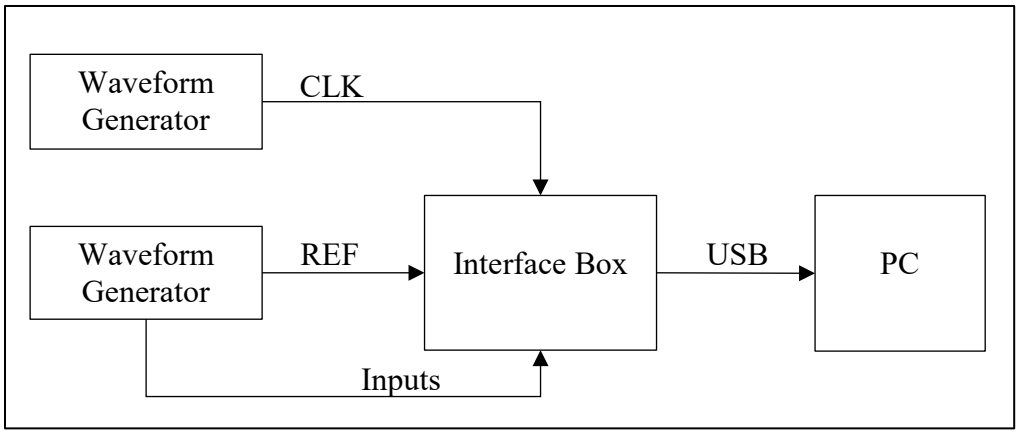

Fig. 5 Interface box test setup

Table 3 Test states

State number	Data impedance	Data voltage	Clock impedance	Clock voltage	Expected result
1	50 Ω	3	50 Ω	3	Interval near 0 or 1
2	50 Ω	5	50 Ω	3	Interval increases
3	1 MΩ	5	50 Ω	3	Interval decreases
4	1 MΩ	5	50 Ω	5	Interval decreases
5	1 MΩ	5	1 MΩ	3	Interval should be different than state 3

Table 4 Box 1 test results

Input	State 1	State 2	State 3	State 4	State 5
1	0.00236571	0.14190595	0.07878852	0.99999799	0.04565385
2	0.00052549	0.13849657	0.07748398	0.99865509	0.04498221
3	0.00116786	0.14345689	0.07937618	0.00054948	0.04594214
4	0.00302388	0.14390545	0.07962024	0.00079349	0.04608911
5	0.00123868	0.14115308	0.07858320	0.99975550	0.04560073
6	0.00126261	0.14276150	0.07907127	0.00024407	0.04575320
7	0.00179526	0.14352509	0.07947498	0.00055690	0.04598969
8	0.00056401	0.13971118	0.07788065	0.99905206	0.04516555
9	0.00239094	0.14234422	0.07907204	0.00024404	0.04584448
10	0.0010875	0.13962881	0.07788361	0.99905203	0.04516830

Table 5 Box 2 test results

Input	State 1	State 2	State 3	State 4	State 5
1	0.99906621	0.13977659	0.07751982	0.99973214	0.04674491
2	0.00000044	0.13909711	0.07735985	0.99917581	0.04611031
3	0.99915247	0.13772343	0.07681271	0.99753480	0.04721526
4	0.99884881	0.13748766	0.07680793	0.99752878	0.04726347
5	0.99912074	0.14131595	0.07824686	0.00127104	0.04672261
6	0.00000011	0.14003234	0.07769678	0.00014677	0.04675605
7	0.00008353	0.14062320	0.07791772	0.00049904	0.04724640
8	0.99929675	0.13766741	0.07705139	0.99820614	0.04657532
9	0.00030508	0.14318239	0.07879481	0.00299550	0.04713002
10	0.00039695	0.13982466	0.07769567	0.99986708	0.04654592

5. Lessons Learned

The overall system design was successful, producing a handsome, sturdy interface box that functioned properly with the very first PCB layout. A number of aspects were specifically advantageous and should be repeated in future designs:

- The system was overdesigned from the start. Original specifications limited the input voltage to 5.5 V. Months later this was revised to include inputs up to 12 V. We were able to easily accommodate this change by overdesigning the system from the start to handle inputs up to 13.2 V.
- Extra parts were ordered. Although two complete units were required, extra parts were ordered, which helped to accommodate mistakes made in the design and support an extra prototype unit for debugging.

- Using BNCs as standoffs was a very effective means of attaching the PCB to the panel and greatly simplified the design.
- Using the Pelican case as the base allowed for easy storage and transportation, and the pins could be removed to detach the lid for convenient benchtop use.
- Contracting out the label to a print shop resulted in a professional design for an affordable price.

Although the overall design was successful, there were a few mistakes and poor choices that should be corrected in the future:

- GNDOUT and Vdd pins of the clock buffer were not connected. This was corrected by adding a wire connecting Vdd to the system 3.3-V power and connecting GNDOUT to the adjacent ground on pin 7.
- The PPS_EN pin was connected to pin 16, which is reserved on the FPGA board as an analog input. This was corrected by clipping pin 16 on the FPGA board and connecting pin 16 to pin 17 on the PCB. Pin 17 on the FPGA board was then employed as the PPS_EN signal.
- The installed resistor values of R9–12 used to produce the 3-V and 5-V threshold values were incorrect. This is because changing the resistor values in the schematic text does not automatically update the part value in the BOM. The resistors were removed and replaced with the correct values.
- The assessment of the switch positions were flipped. New labels were ordered to correct this problem.
- Most of the board components were put on the top of the PCB. This made them inaccessible once the panel was attached. It would have been advantageous to put the components on the bottom of the board so that they could be easily probed and replaced.
- Two full panels were assembled before testing. This was a waste of effort considering the changes that were eventually required. It would have been better to first assemble one test PCB without a panel, and only assemble full panels after the test PCB was debugged.
- The extra internal USB cable that is inserted between the FPGA board and external USB cable degrades the USB performance. Only high-quality USB cables will properly connect the interface box to a PC. In the future, more care should be given to making the USB connection as robust as possible.

6. Conclusion

This technical note detailed the design of an interface box for time interval measurement. The overall design of the box was successful, producing a working box with the first PCB layout. The electrical and mechanical design was described, and both good and bad design decisions were reviewed. This note will serve as a valuable resource for future interface box modifications and upgrades, as well as an interface box design template for other projects.

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List of Symbols, Abbreviations, and Acronyms

AC	alternating current
ARL	US Army Research Laboratory
BOM	bill of materials
BNC	Bayonet Neill–Concelman
CMOS	complementary metal–oxide semiconductor
DC	direct current
FPGA	field-programmable gate array
IC	integrated circuit
PC	personal computer
PCB	printed circuit board
PDF	portable document format
PPS	pulse per second
USB	universal serial bus
Vpp	peak-to-peak voltage

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