
Loading Classical Data into a Quantum Computer

by

John A. Cortese and Timothy M. Braje

Lincoln Laboratory
Massachusetts Institute of Technology
Lexington, Massachusetts, USA

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1 Overview

This document describes a family quantum circuits and associated techniques and design principles which collectively serve to efficiently transfer data, specifically binary data or bits, from the classical domain (classical world) into the quantum domain (quantum world). In addition, the quantum data is formatted into quantum states for follow-on processing by efficient quantum algorithms.

1.1 Block diagram description of a quantum algorithm

The three generic stages of execution in a quantum computer are shown in Figure 1. The work in this document concerns the leftmost, green stage shown in Figure 1 labeled *Load classical data into quantum format*.

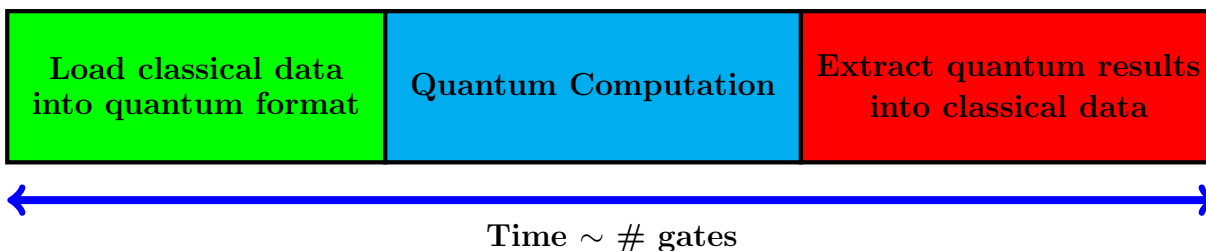


Figure 1: The three stages of execution in a quantum computer.

2 The data loading quantum circuits

Quantum circuits for loading classical data into quantum states for processing by a quantum computer are the focus of this document. As different quantum algorithms have varying constraints on how the classical input data is loaded and formatted into the corresponding quantum states, a number of data loading circuits will be presented. The utility and usage

of each data loading circuit is discussed in the context of the quantum algorithms to which the classical data is being passed.

2.1 Quantum state formats for representing classical data

Consider the problem of mapping a matrix of classical single bit values (b_{ij}) into a quantum state. As an example, take the 2 by 2 matrix $A = \begin{bmatrix} b_{00} & b_{01} \\ b_{10} & b_{11} \end{bmatrix}$. Note that for bit b_{ij} , the i subscript indicates the row, with $i = 0$ or 1 , and the j subscript indicates the column, with $j = 0$ or 1 . The corresponding quantum state which will hold the matrix A bit values is ψ_A . The quantum state ψ_A uses three (3) qubits to represent the four single bit values b_{ij} , as well as the corresponding positions of the bits in the matrix.

$$\begin{aligned} |\psi_A\rangle &= |00\rangle \otimes |b_{00}\rangle + |01\rangle \otimes |b_{01}\rangle + |10\rangle \otimes |b_{10}\rangle + |11\rangle \otimes |b_{11}\rangle \\ &\equiv |00b_{00}\rangle + |01b_{01}\rangle + |10b_{10}\rangle + |11b_{11}\rangle. \end{aligned} \quad (1)$$

The symbol \otimes is the tensor product operator and will be used to delineate groups of qubits within a quantum state. Quantum information notation often drops the tensor symbol to write the state as shown in the second line of Equation 1. The first, leftmost qubit of the state represents the row within the matrix, corresponding to the i index. Similarly the second qubit represents the column, corresponding to the index j . The third, rightmost qubit represents the single bit value of the corresponding (row,column) matrix entry. As is traditional in quantum information, the overall quantum state normalization constant is dropped for readability. The overall state normalization constant is straightforward to compute and reinsert when necessary. For the state in Equation 1, the normalization constant is $\frac{1}{2}$, regardless of the values of the b_{ij} .

This document describes several families of data loading circuits. Each family is optimal under a different set of constraints. Each circuit family is given in order of circuit complexity, with a corresponding discussion. The material in this document is concerned with the gate based model of quantum computation and the circuits are presented in a gate based framework.

2.2 Circuit Family #1

The quantum circuit shown in Figure 2 loads a single classical bit into a qubit. In Figure 2, double wires are classical wires conveying a classical bit value = $\{0,1\}$. Single wires are quantum wires along which quantum states or qubits move. The box with the **X** inside is a quantum bit flip gate. The quantum bit flip gate acts the same on quantum states as a classical inverter gate does on classical bits, reversing the value of the qubit. In both the classical and quantum scenario bit flip gate action, a "0" goes to a "1" and a "1" goes to a "0". In the circuit shown in Figure 2, the quantum bit flip gate is a controlled gate. The control is a classical wire feeding into the top of the gate. The solid dot indicates the control wire for the corresponding box/gate action. If the classical control wire is a "0", then the bit flip gate is not executed. If the classical control wire is a "1", then the bit flip gate is executed. The circuit diagram data flow is always left to right in quantum circuits.

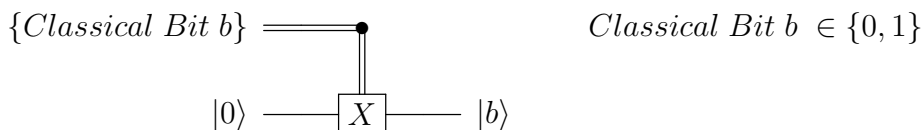


Figure 2: Loading a classical bit b into the qubit quantum state $|b\rangle$.

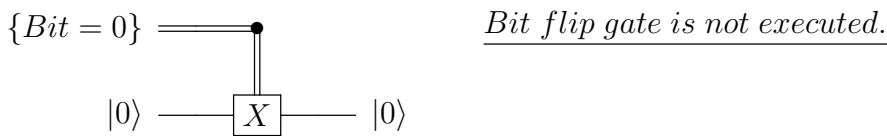


Figure 3: Loading a classical "0" bit into the $|0\rangle$ qubit quantum state.

In circuit family #1, each classical bit is stored in one qubit and requires the execution of one quantum gate to implement the classical bit loaded into a qubit storage operation. To better understand the asymptotic behavior of the size of the circuits and other aspects of the circuit families, let the total number of classical bits being loaded into the quantum computer be \mathcal{N} . If the input data consists of N words where each word is P bits long, then the total number of bits \mathcal{N} are $\{b_i\} \in \{0, 1\}$ with $i = 1, 2, \dots, \mathcal{N} = NP$. The circuit

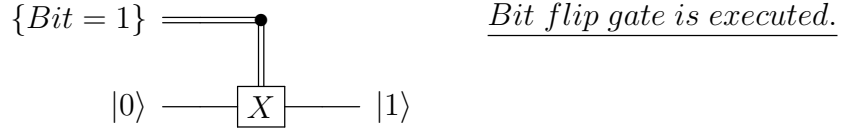


Figure 4: Loading a classical "1" bit into the $|1\rangle$ qubit quantum state.

shown in Figure 5 which is loading the $\mathcal{N} = NP$ classical bits will require a quantum state consisting of $\mathcal{N} = NP$ qubits to store these bits. Computationally, the circuit requires the execution of $\mathcal{N} = NP$ gates in parallel. The gate depth corresponds to the time the circuit will take to execute on the input data. The gate depth of the quantum circuit in Figure 5 is 1. The gate depth for all family #1 data loading quantum circuits is 1.

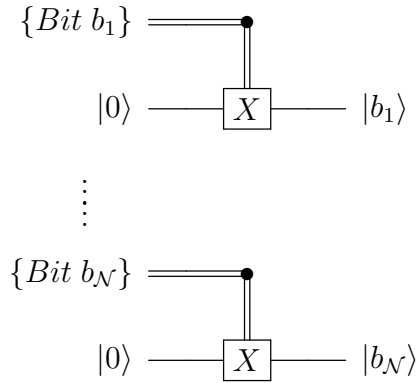


Figure 5: Loading \mathcal{N} classical bits $\{b_1, \dots, b_{\mathcal{N}}\}$ into \mathcal{N} qubits in a quantum circuit with a gate depth equal to one.

The \mathcal{N} qubit quantum state ψ produced by the circuit is

$$\psi = |b_1\rangle \otimes |b_2\rangle \otimes \dots \otimes |b_{\mathcal{N}}\rangle \equiv |b_1 b_2 \dots b_{\mathcal{N}}\rangle. \quad (2)$$

A table of the resource requirements for each data loading circuit family will gradually be compiled. For circuit family #1 described in this section, the resource requirements are given

in Table 1.

Circuit family	Number of classical bits	Number of qubits in the quantum state ψ	Number of total gates	Gate depth	Number of ancilla qubits
#1	\mathcal{N}	\mathcal{N}	\mathcal{N}	1	0

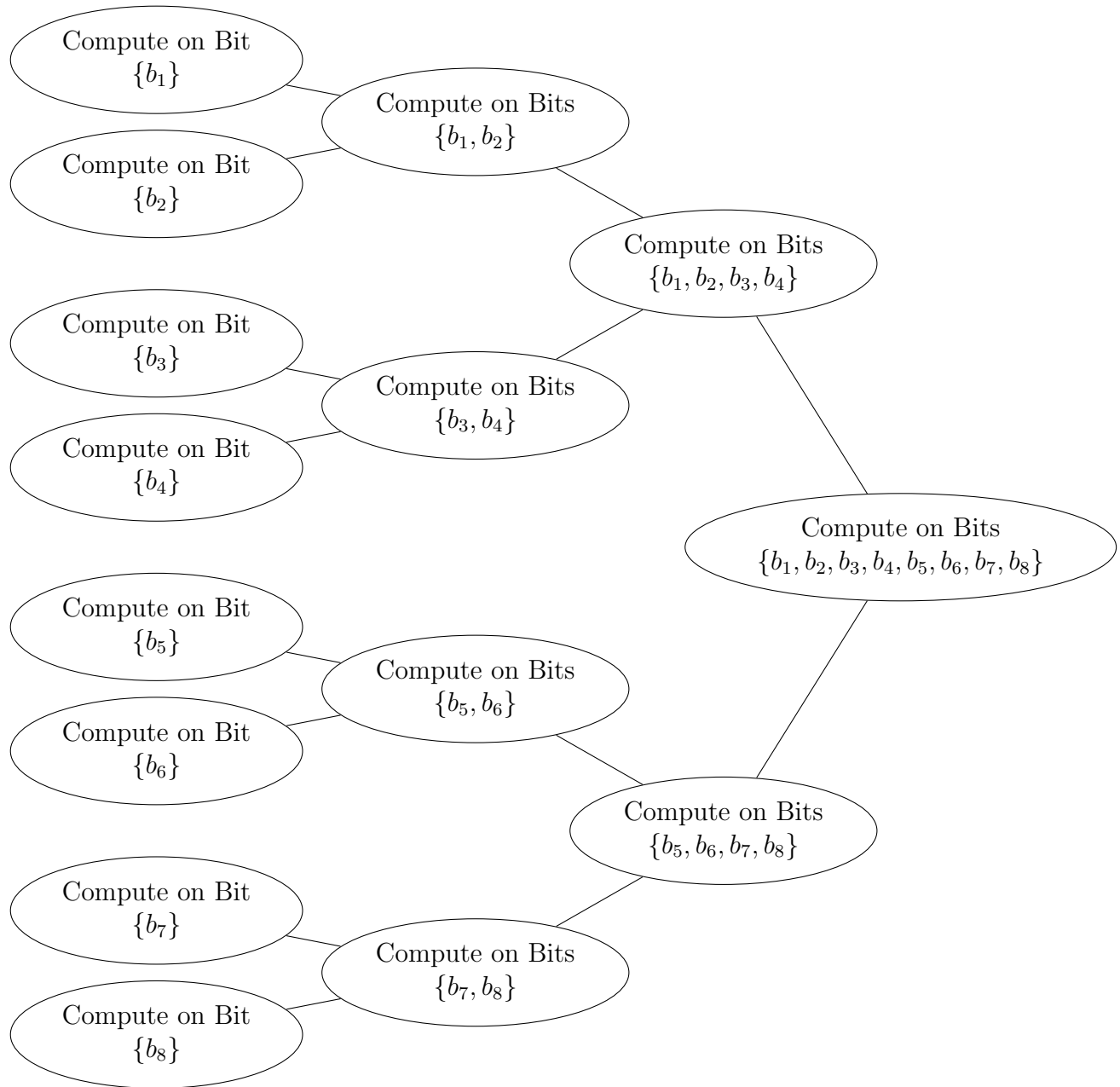
Table 1: Resource requirements for data loading circuit family #1. N is the number of vector entries or words. Let $N = 2^n$. P is the number of bits per vector entry or word. The total number of classical bits is $\mathcal{N} = NP = 2^n P$.

The quantum state shown in Equation 2 is not optimal for use as the input to a quantum algorithm exhibiting exponential speedup. Loading \mathcal{N} classical bits into a quantum state composed of $\text{Log}_2(\mathcal{N})$ or fewer qubits is needed. This fact motivated the development of circuit family #2.

2.3 Circuit Family #2

Circuit family #1 loads \mathcal{N} bits into a quantum state of size \mathcal{N} using a gate depth of 1. The benefit of quantum circuits over classical circuits is the potential for the quantum circuit to exhibit exponential speedup in execution time, which translates to a logarithmic reduction in the gate depth. In order for this speedup to be possible, the size, meaning the number of qubits of the quantum state containing the relevant classical data, should be logarithmic in the number of classical bits being manipulated. That is, if there is no pattern or symmetry indicating preference among the incoming data items, then all the data must be considered equally. A circuit implementing a generic algorithm on \mathcal{N} data items should have a gate depth which is logarithmic in \mathcal{N} . For the case of $\mathcal{N} = 8$ bits, the recursive exploration of the data is shown as a tree in Figure 6.

The size of the circuit family #1 quantum state is \mathcal{N} qubits, which is typically too large for quantum circuitry to use and still exhibit exponential speedup over classical circuitry. It is possible to pack \mathcal{N} classical bits into a quantum state of size $\text{Log}_2(\mathcal{N})$ qubits. Such a

Figure 6: Recursive Computation on $\mathcal{N} = 8$ bits.

compression of the classical bit count is a key factor enabling quantum algorithm design for exponential speedup over classical algorithms. Circuit family #2 exhibits this logarithmic compression of classical bits into qubits. As a result, circuit family #2 is an enabling technology for the implementation of quantum algorithms exhibiting exponential speedup over classical algorithms.

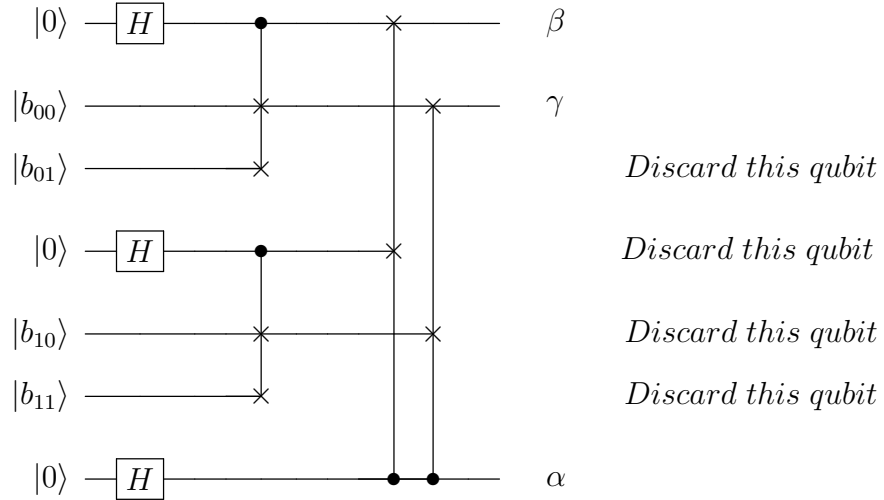


Figure 7: A circuit family #2 implementation layout loading the four classical bits, $\{b_{00}, b_{01}, b_{10}, b_{11}\}$ into the three qubits $|\alpha\beta\gamma\rangle$. Recall that a classical bit b is loaded into a single qubit denoted $|b\rangle$ using the quantum circuit/gate shown in Figure 2.

The three qubit state $|\psi_A\rangle$ on the right hand side of the circuit in Figure 7 is storing the four classical bit values of the matrix A .

$$|\psi_A\rangle = |\psi_{\alpha\beta\gamma}\rangle = |\alpha\beta\gamma\rangle = |00\rangle \otimes |b_{00}\rangle + |01\rangle \otimes |b_{01}\rangle + |10\rangle \otimes |b_{10}\rangle + |11\rangle \otimes |b_{11}\rangle. \quad (3)$$

Key aspects of circuit family #2 are shown in Figure 7 and will be described in the next several sections.

2.4 More about quantum circuits

To understand the circuit shown in Figure 7, more detail about the constituent gates must be given. Quantum circuits are composed of quantum gates. Quantum gates act linearly on their input. Therefore, knowing the action of any gate on all possible computational basis inputs suffices to completely characterize the gate. In this section, several gates will be described which are used in the circuit shown in Figure 7.

2.4.1 The quantum Swap gate

The quantum swap gate shown in Figure 8 will be used extensively in the circuits to follow.

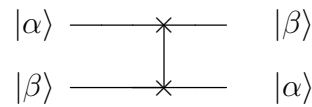


Figure 8: The quantum Swap gate interchanges the states of two qubits.

The quantum swap gate shown in Figure 8 can be implemented with three Controlled-Not (CNOT) gates as shown in Figure 9.

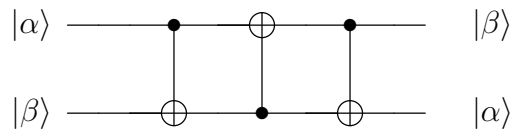


Figure 9: The Swap gate implemented with three Controlled-Not (CNOT) gates.

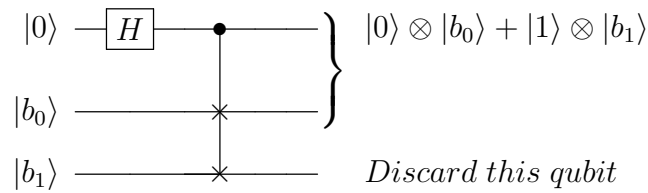


Figure 10: The Controlled Swap (CSwap) gate.

2.4.2 The Controlled Swap gate

The controlled quantum swap gate (C-Swap or CS) is shown in Figure 10. Whether two qubit states are swapped depends on the quantum state of a control line. The three qubit input state to the quantum circuit in Figure 10 is $|q_1 q_2 q_3\rangle = |0 b_0 b_1\rangle$. The three qubit output state at the right hand side of the circuit in Figure 10 is the superposition shown in Equation 4.

$$|q_1 q_2 q_3\rangle = |0 b_0 b_1\rangle + |1 b_1 b_0\rangle, \quad (4)$$

where, as discussed previously, without loss of generality, the normalization coefficient, which in this case is $\frac{1}{\sqrt{2}}$, has been dropped from Equation 4.

2.4.3 The Toffoli gate

The Toffoli gate is a Controlled-Controlled-Not gate (CCNot). It has two control lines and executes a bit flip on a third qubit if and only if the two control qubits are both in the $|1\rangle$ state. A controlled swap gate can be implemented with three Toffoli gates as shown in Figure 11.

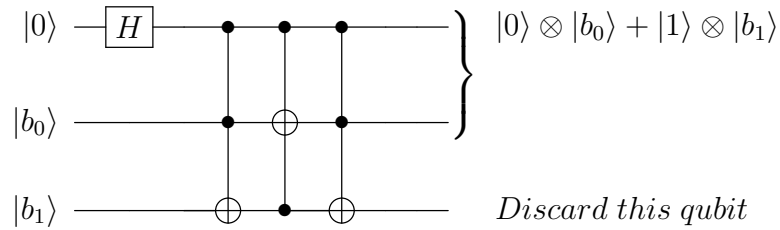


Figure 11: The controlled quantum swap gate using Controlled Controlled Nots (CCNot's), which are equivalent to Toffoli gates.

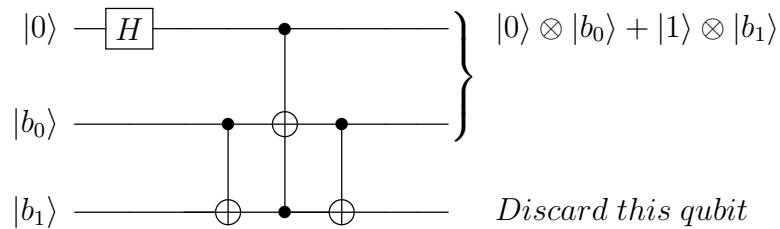


Figure 12: The controlled quantum swap gate using one CCNot (Toffoli) gate and two Controlled-Not gates.

A simplification of the circuit in Figure 11 using only one Toffoli gate and two Controlled-Not gates is shown in Figure 12. A Toffoli gate can be decomposed into a sequence of one and two qubit gates. The circuit shown in Figure 13 is one such decomposition. The single qubit gate S in Figure 13 is the Phase gate, defined as $S = \begin{bmatrix} 1 & 0 \\ 0 & i \end{bmatrix}$, where i is the square root of -1 , namely $i = \sqrt{-1}$.

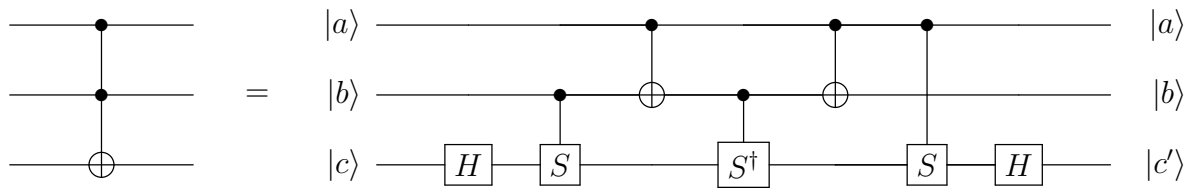


Figure 13: A two qubit gate implementation of the three qubit Toffoli (CCNot) gate.

2.4.4 Controlled Swaps of multiple qubits

Looking back at the recursive structure shown in Figure 7, one notes the need for a quantum circuit which will swap into superposition more than two bits. Building upon the one qubit circuit shown in Figure 10, a two qubit swap quantum circuit is shown in Figure 14.

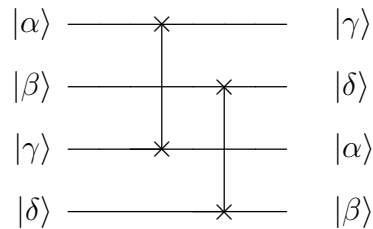


Figure 14: Using two Swap gate's to exchange two pairs of two qubits.

The controlled swap of multiple pairs of qubits is used extensively in the quantum circuits to follow. A quantum circuit implementing the controlled swap of two pairs of qubits is shown in Figure 15.

2.5 Reusing *Discarded* qubits

The quantum circuits shown in Figures 7, 10, 11, 12 and 15 all have *Discarded* qubits at the end of the computation. Ideally one would like to reuse the *Discarded* qubits later in

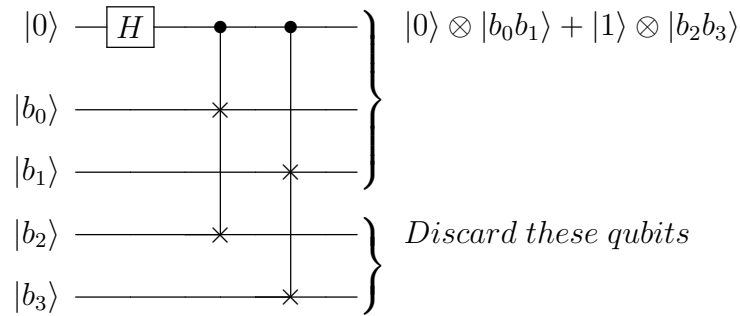


Figure 15: Using controlled quantum Swap gates to exchange two pairs of two qubits. Note the use of quantum superposition to build the quantum state.

the computation. However the *Discarded* qubits are typically entangled with other qubits in the circuit, complicating the reuse of the discarded qubits in other circuit blocks. The qubit reuse problem is shown in Figure 16, which is the same circuit as Figure 10 on page 13 but with the qubit labels $|q_1, q_2, q_3\rangle$ added for clarity.

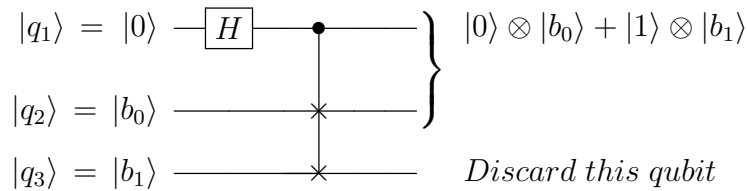


Figure 16: The Controlled Swap (CSwap) gate.

In Figure 16, the variables b_0 and b_1 are individually either 0 or 1. There are four (4) possible $\{b_0, b_1\}$ pairings. In Figure 16 the final circuit state is

$$|q_1, q_2, q_3\rangle = |0b_0b_1\rangle + |1b_1b_0\rangle. \quad (5)$$

Ideally, one would like to see the final circuit quantum state be as shown in Equation 6.

$$|q_1, q_2, q_3\rangle = \underbrace{(|0b_0\rangle + |1b_1\rangle)}_{|q_1, q_2\rangle} \otimes \underbrace{|junk\rangle}_{|q_3\rangle}. \quad (6)$$

Given the single qubit *junk* state $|junk\rangle$ in Equation 6 is in a tensor product with the remaining two qubit state $|q_1, q_2\rangle$, the *junk* state can be removed without affecting the $|q_1, q_2\rangle$ state. The *junk* state can be reused as an ancilla or in some other role later in the computation without fear of impacting earlier completed computational operations. The removal and reuse of the *junk* qubit can occur even if there are classical correlations between the *junk* state $|junk\rangle$ and the state $|q_1, q_2\rangle$. While entanglement between $|junk\rangle$ and $|q_1, q_2\rangle$ would allow a manipulation of $|junk\rangle$ to affect the state of $|q_1, q_2\rangle$, correlations do not.

Returning to the quantum state in Equation 5 which is output by the circuit in Figure 16, if $b_0 \neq b_1$, measuring the *Discarded* qubit q_3 would influence the remaining $|q_1 q_2\rangle$ possibly superposition state. For example, if $b_0 = 0$ and $b_1 = 1$, the state shown in Equation 5 becomes

$$|q_1 q_2 q_3\rangle = |001\rangle + |110\rangle. \quad (7)$$

In this situation, obtaining a q_3 measurement outcome of 0 would leave $|q_1 q_2\rangle = |11\rangle$, which is not the desired $|q_1 q_2\rangle$ state of $|q_1 q_2\rangle = |00\rangle + |11\rangle$. Similarly, obtaining a q_3 measurement outcome of 1 would leave $|q_1 q_2\rangle = |00\rangle$, which again is not the desired $|q_1 q_2\rangle$ state of $|q_1 q_2\rangle = |00\rangle + |11\rangle$.

For the choice of $b_0 = 0$ and $b_1 = 1$ as in the measurement examples above, the *desired* form of $|q_1 q_2\rangle$ after a measurement of q_3 would leave $|q_1 q_2\rangle$ in the state $|q_1 q_2\rangle = |00\rangle + |11\rangle$. The qubit reuse scenario requires post-processing of qubit q_3 so that measuring q_3 will not impact the remaining $|q_1 q_2\rangle$ superposition state, leaving $|q_1 q_2\rangle$ in the state $|q_1 q_2\rangle = |0b_0\rangle + |1b_1\rangle$ regardless of the measurement outcome of q_3 . Mathematically one would like a disentangling processing \mathcal{F} producing a three qubit state as shown in Equation 8.

$$|q_1 q_2 q_3\rangle \xrightarrow{\mathcal{F}} |q_1 q_2\rangle \otimes |\tilde{q}_3\rangle, \quad (8)$$

where \tilde{q}_3 represents the state of the third qubit after the disentangling process and $|q_1 q_2\rangle$ represents the state $|q_1 q_2 q_3\rangle$ with the state of q_3 traced out. The disentangling strategy allows *Discarded* qubits to be reused in the computation, lowering the overall number of qubits needed to implement the circuits to be discussed.

The inspiration for the disentangling approach is taken from Quantum Error Correction (QEC) techniques. In the circuit shown in Figure 17, the three gates within the dashed box implement the disentangling operation referred to above as \mathcal{F} , which is a parity checking function as implemented for a variety of quantum codes. The innovation is the implementation of error correction circuitry to enable qubit reuse in a computation. The three terminal Toffoli gate inside the dashed disentangling box \mathcal{F} of Figure 17 can be decomposed into CNOT's and single qubit unitaries. Table 2 lists the quantum states at various points in the circuit shown in Figure 17 for the four cases $b_0 = \{0,1\}$ and $b_1 = \{0,1\}$. The ancilla qubit $|a\rangle$ is always $|0\rangle$ at the input of the circuit. As in quantum error correction protocols, the ancilla qubit is measuring the parity of b_0 and b_1 , which is equivalent to the sum $a = b_0 \oplus b_1$ modulo 2.

Measuring the $|q_3\rangle$ qubit and the ancilla qubit $|a\rangle$ indicates which of the four bit pairs $\{b_0, b_1\}$ were loaded into the two qubit state $|q_1, q_2\rangle$. Unlike the situation in quantum error correction, the measurement of $|q_3\rangle$ and the ancilla qubit $|a\rangle$ will not destroy the desired superposition of the remaining qubits. One already knows what b_0 and b_1 are from the original classical bit specification, so the measurement does not gain any additional information about b_0 and b_1 from the $|q_3\rangle$ and the ancilla qubit $|a\rangle$ measurement outcomes.

The qubits $|q_3\rangle$ and $|a\rangle$ can be measured or left untouched at the end of the disentangling circuit. In either case these qubits, either singly or together, can be used in later parts of the computation. The $|q_3\rangle$ and $|a\rangle$ qubits have been stripped by the disentangling operation \mathcal{F} of their entangled connection to the $|q_1 q_2\rangle$ qubit state.

The same approach can be used iteratively to remove multiple *discarded qubits* in a circuit. Referring to Figure 7, one can apply the disentangling method to decouple all four (4)

2.5.1 Optimizing the data flow from classical bits into quantum states

Information theory provides guidance on how to think about optimally transferring bits from the classical domain to the quantum domain using the minimum number of qubits and gates in the transfer operation. A block diagram of the transfer process is given in Figure 18.

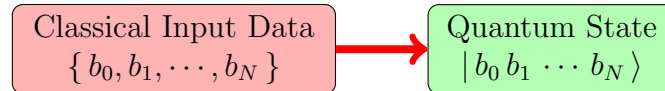


Figure 18: Classical to quantum data flow. The Red shaded boxes denote classical domain data. Green shaded boxes denote quantum data. The output quantum state is a product state: $|b_0 b_1 \dots b_N\rangle = |b_0\rangle \otimes |b_1\rangle \otimes \dots \otimes |b_N\rangle$.

The process of transferring bits from the classical domain to the quantum domain is a *channel* in information theoretic language. The picture of the data transfer dynamics is represented as shown in Figure 19.

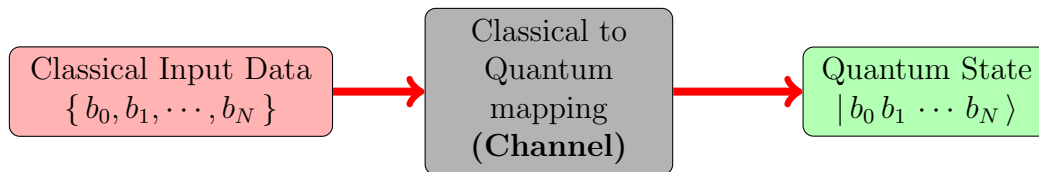


Figure 19: Classical to quantum data flow through a quantum channel. The Red shaded boxes denote classical domain data. Green shaded boxes denote quantum data. The black box will use the circuits shown in Figures 2 and 5.

Claude Shannon's channel capacity theorem, together with the source coding theorem, indicate that to optimize the classical to quantum transfer of data, one should compress the incoming bit stream to remove any redundancies among the input bits, transmit the compressed data through the channel, and decompress the data stream at the channel output to recover the original data bits. This sequence of operations is shown in Figure 20.

Any improvement in data transfer rate depends on the compressibility of the incoming data stream. For incoming bits which are statistically **I**ndependent, **I**dentically **D**istributed (**IID**) and equiprobable, there is no benefit to using a compression/decompression scheme. However, in other scenarios there will be a benefit.

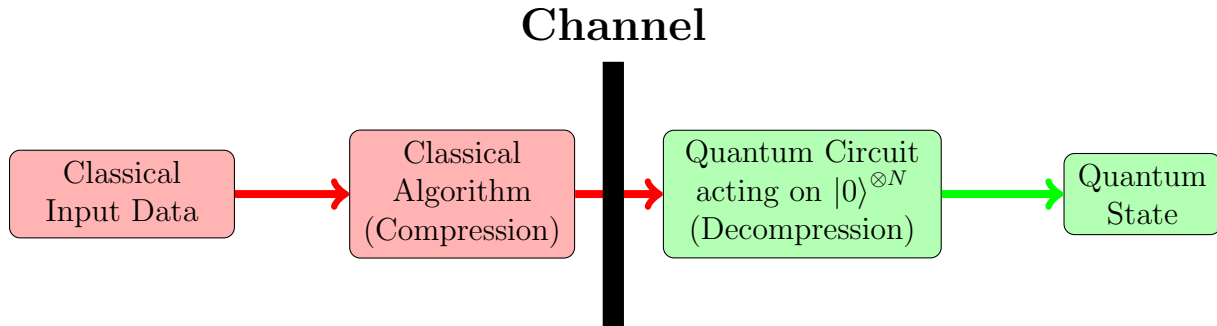


Figure 20: To optimize data flow, compress binary data in the classical domain and decompress in the quantum domain.

Figures 21 and 22 present the basic concepts of the compression/decompression approach. In Figure 21, a block of N bits is compressed by a factor of L to a block of M bits, where $M \leq N$. The factor $L = -E_S[\text{Log}(p_i)]$ is the average entropy of a bit in the incoming bit stream. For large blocks, meaning $N \gg 1$, a single bit is mapped to L bits, where $0 \leq L \leq 1$. Therefore the block of length N bits is mapped by the compression algorithm to $LN = M$ bits, where $0 \leq M \leq N$. In our scheme the compression algorithm is implemented on a classical computer.

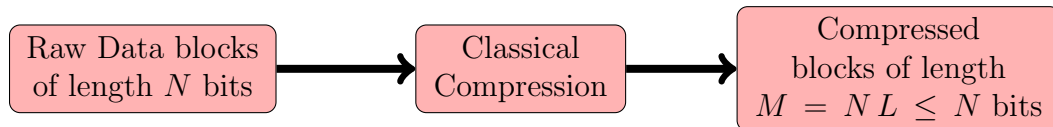


Figure 21: The compression rate is $\frac{1}{L}$, with $L > 1$. The red shading indicates all three blocks are implemented in the classical domain.

The improvement in data transfer performance can be quantified in terms of the number of bit to qubit stages such as shown in Figure 5 on page 8 needed to transfer N bits of information. For example, for IID classical bits for which binary 1's occur with probability p and 0's occur with probability $1 - p$, with $0 < p \ll 1 - p < 1$, the compression parameter L defined above behaves as shown in Figure 23. Working from the curve in Figure 23, when $p = 0.03$, then $M = 0.2N = \frac{N}{5}$. (For this operating point, please see the **red dot** on the curve in Figure 23.) When only 3% of the incoming bits are on average 1's, compression/decompression methods can reduce the number of loading circuits shown in

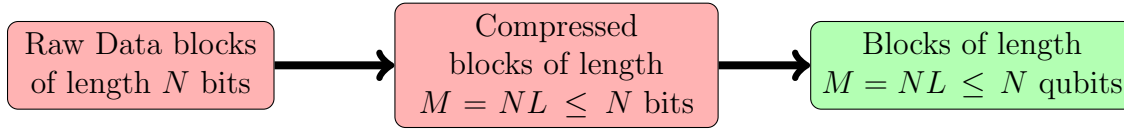


Figure 22: Quantifying circuit complexity reduction using compression techniques. The circuits shown in Figure 5 become M parallel stages instead of the N parallel stages shown. The number of qubits saved by the compression/decompression approach is $N - M$. The red shaded blocks occur in the classical domain, while the green block is in the quantum domain.

Figure 5 from N to $\frac{N}{5}$. For $N = 100$ and $p = 0.03$, the number of stages needed in the circuit shown in Figure 5 is 20, yielding a savings in the number of front end qubits and gate count through the use of compression/decompression techniques of $N - M = 80$ qubits. This should be compared to approaches which do not use compression/decompression methods, which for the circuit shown in Figure 5 would require $N = 100$ qubit stages to transfer 100 uncompressed classical bits.

2.5.2 Computational Complexity of Compression and Decompression

Referring to the leftmost (Green) block in Figure 1 on page 5, to ensure the data loading circuit implementation is a time complexity of order $\mathcal{O}[\text{Log}(N)]$, the quantum gate circuit depth of the decompression stage must be of order $\mathcal{O}[\text{Log}(N)]$.

A proof that the $\mathcal{O}[\text{Log}(N)]$ decompression bound is achievable proceeds as follows. Recall that although the data structures involved in the quantum decompression algorithm are qubits, the qubits are storing classical bit values and are in the pure state $|0\rangle$ or $|1\rangle$ at the beginning of the decompression circuit. This fact is due to the nature of the data loading circuitry shown in Figures 24 which serves to transfer the M compressed bits output from the classical compression algorithm from the classical domain into the quantum domain.

As the qubits $|b_k\rangle$, $k = 1, \dots, M$, are individually either $|0\rangle$ or $|1\rangle$, with no quantum superposition present, the orthogonality of the pure states single qubit $|0\rangle$ or $|1\rangle$ allows the quantum decompression algorithm and corresponding quantum decompression circuit to be

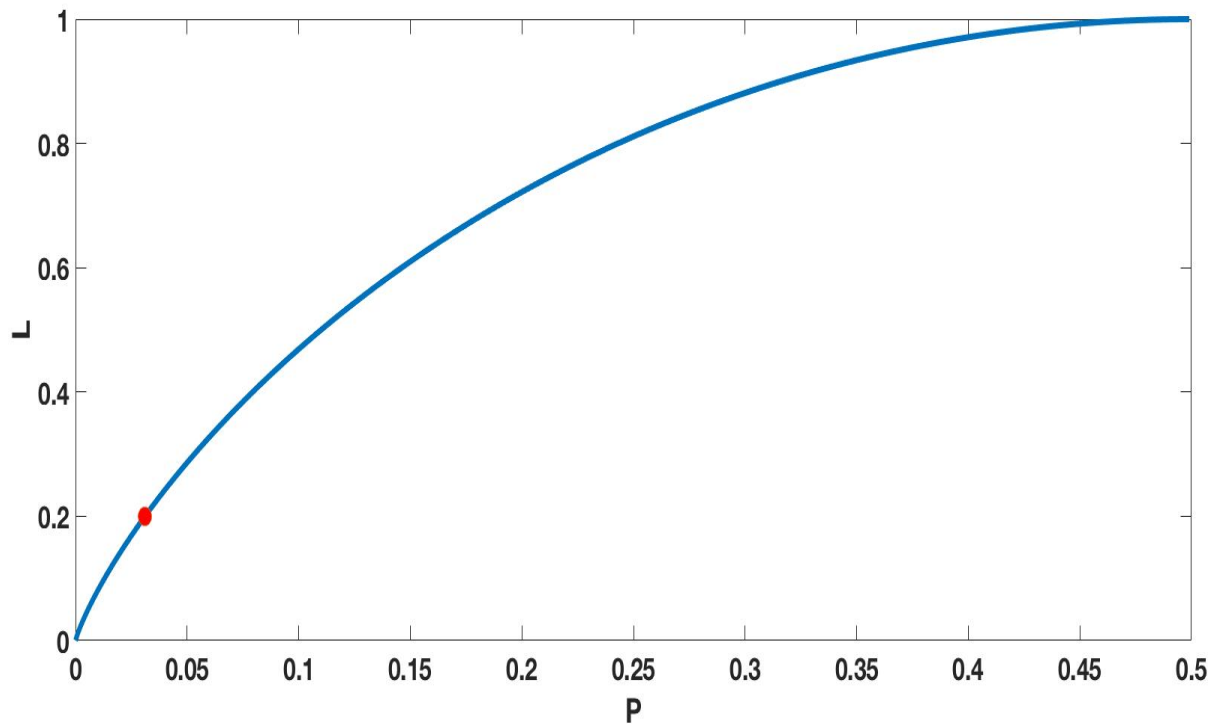


Figure 23: The circuits in Figure 5 become M parallel stages instead of the N parallel stages shown in Figure 5. The number of qubits saved by the use of the compression/decompression approach is $N - M$. The red dot indicates the $(p = 0.03, L = 0.2)$ operating point discussed in the main body.

a quantum version of the classical decompression corresponding to the classical compression algorithm which was used. The classical gates in the classical decompression circuit (e.g. NAND) are implemented using quantum gates. In this manner, the extensive literature of classical decompression algorithms and circuits can be leveraged.

Using the fact that one can represent each classical gate in the classical decompression algorithm with a quantum gate configuration consisting of, at most, a fixed, finite number of quantum gates, the proof of $\mathcal{O}[\text{Log}(N)]$ quantum gate depth for the quantum decompression circuit follows from the corresponding proof of $\mathcal{O}[\text{Log}(N)]$ gate depth of the classical decompression circuit. As there are many classical decompression algorithms with $\mathcal{O}[\text{Log}(N)]$ classical gate depth, this concludes the discussion of the application of

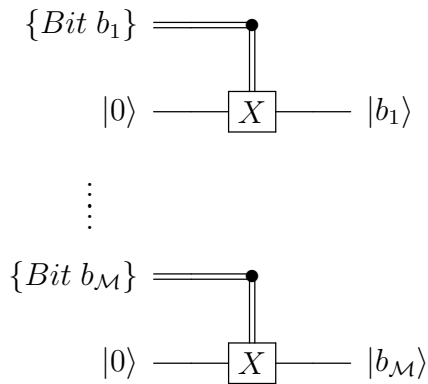


Figure 24: Loading \mathcal{M} classical bits $\{b_1, \dots, b_{\mathcal{M}}\}$ into \mathcal{M} qubits in a quantum circuit with a gate depth equal to one.

classical compression/decompression algorithms to optimize the transfer of classical bits into qubits.

3 The recursive nature of Circuit Family #2

The circuit shown in Figure 7 on page 11 has a recursive structure which enables the asymptotic behavior of circuit family #2 to be extrapolated for large \mathcal{N} . The recursive nature of the assembly of the quantum state

$$\psi_A = |00\rangle \otimes |b_{00}\rangle + |01\rangle \otimes |b_{01}\rangle + |10\rangle \otimes |b_{10}\rangle + |11\rangle \otimes |b_{11}\rangle \quad (9)$$

for the 2 by 2 matrix $A = \begin{bmatrix} b_{00} & b_{01} \\ b_{10} & b_{11} \end{bmatrix}$ is shown in Figure 25. Recall that each entry b_{ij} in the matrix A is a single classical bit.

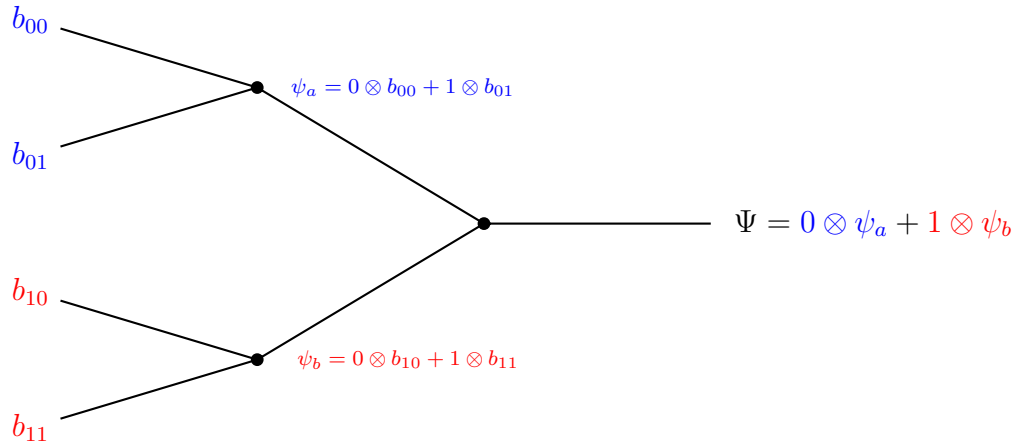


Figure 25: The recursive assembly of the quantum state $\Psi = |00b_{00}\rangle + |01b_{01}\rangle + |10b_{10}\rangle + |11b_{11}\rangle$. The depth of the recursion is $\text{Log}_2(\mathcal{N}) = \text{Log}_2(4) = 2$.

Consideration of the recursive tree construction in Figure 25 allows for the calculation of the number of qubits needed, as well as the gate depth for assembling, a quantum state containing \mathcal{N} classical bits.

3.1 Resource tabulation for Circuit Family #2

The general approach to loading \mathcal{N} classical bits into $\text{Log}_2(\mathcal{N})$ qubits is a generalization of the recursive method shown in Figure 25 for $\mathcal{N} = 2^2$. Without loss of generality for asymptotic calculations, let \mathcal{N} be a power of 2 and define n such that $\mathcal{N} = 2^n$. In this case there will be a total of n levels of recursion in the quantum circuit loading \mathcal{N} classical bits into $\text{Log}_2(\mathcal{N})$ qubits.

3.1.1 Asymptotic Quantum Gate Depth and Execution Time Resource Calculation for Circuit Family #2

The data loading circuit depth must obey bounds compatible with the quantum algorithm to be implemented. For an exponential speedup over a classical polynomial complexity algorithm, the data loading circuit depth must scale ideally as $\mathcal{O}\left[\text{Log}(\mathcal{N})\right]$ and at most polylogarithmically in $\text{Log}(\mathcal{N})$.² For circuit family #2, the gate depth can be computed with the aid of the recursive tree diagram in Figure 25, together with the controlled swap based circuits shown in Figures 7, 10 and 15. Moving from left to right in Figure 25, the first layer requires one Hadamard gate and one controlled swap gate (CSwap). The second layer requires one Hadamard and two CSwap gates. The third layer requires one Hadamard and three CSwap gates. And so on. Tabulating the number of gates in these recursion layers leads to the summations in Equations 10 and 11.

$$\# \text{ of Hadamards} = n = \text{Log}(\mathcal{N}). \quad (10)$$

$$\# \text{ of CSwap's} = \sum_{k=1}^{k=n} k = \frac{n(n+1)}{2} \equiv \mathcal{O}(n^2). \quad (11)$$

Tallying all the gates in a generic family #2 circuit from start to finish yields the total gate depth.

$$\mathcal{O}(n) + \mathcal{O}(n^2) = \mathcal{O}(n^2) \equiv \mathcal{O}\left[\left(\text{Log}_2\{\mathcal{N}\}\right)^2\right]. \quad (12)$$

The total gate depth is proportional to time. Therefore the asymptotic time scaling for circuit family #2 is $\mathcal{O}\left[\left(\text{Log}_2\{\mathcal{N}\}\right)^2\right]$, which is acceptable, but not ideal, for an exponential

²See Figure 1.

speedup quantum algorithm. Ideally one would like a gate depth which scales at most as $\mathcal{O}\left[\text{Log}(\mathcal{N})\right]$.

3.2 Asymptotic Space (Qubit) Resource Calculation for Circuit Family #2

Looking at Figure 25, note the left most tree level uses \mathcal{N} qubits and the next level to the right utilizes $\frac{\mathcal{N}}{2}$ *additional* qubits. Moving to the right, for generic \mathcal{N} , each succeeding level *additionally* needs a number of qubits equal to half of the number of qubits of the previous level. There are a total number of $n = \text{Log}_2(\mathcal{N})$ levels. Tabulating the total number of qubits used by circuit family #2 as a summation yields Equation 13.

$$\begin{aligned} \text{Total \# of qubits} &= \sum_{k=1}^{k=n} \frac{\mathcal{N}}{2^{k-1}} = \mathcal{N} \left(1 + \frac{1}{2} + \frac{1}{2^2} + \frac{1}{2^3} + \cdots + \frac{1}{2^{n-1}} \right) \\ &= \mathcal{N} \left(\frac{1 - \frac{1}{2^n}}{1 - \frac{1}{2}} \right) = 2\mathcal{N} \left(1 - \frac{1}{2^n} \right) = 2\mathcal{N} - 2 < 2\mathcal{N}. \end{aligned} \quad (13)$$

Note the use of the finite sum identity

$$\sum_{k=0}^{k=n} x^k = 1 + x + x^2 + \cdots + x^n = \frac{1 - x^{n+1}}{1 - x}, \quad (14)$$

valid for $|x| < 1$, in Equations 13, 15 and 16.

The time and space tabulation for circuit family #2 added to the numbers in Table 1 on page 9 yields Tables 3 and 4. Note that the tabulation of the total number of qubits for

Circuit family	Number of classical bits	Final number of qubits in the quantum state ψ	Final number of ancilla qubits (*)	Final total number of qubits	Gate depth
#1	\mathcal{N}	\mathcal{N}	0	\mathcal{N}	1
# 2^{ne}	\mathcal{N}	$\lceil \text{Log}_2(\mathcal{N}) \rceil = n$	$2\mathcal{N} - 2 - n$	$2\mathcal{N} - 2$	$\lceil \text{Log}_2(\mathcal{N}) \rceil$
# 2^e	\mathcal{N}	$\lceil \text{Log}_2(\mathcal{N}) \rceil = n$	0	n	$\lceil \text{Log}_2(\mathcal{N}) \rceil$

Table 3: Resource requirements for data loading circuit families #1 and #2. The total number of classical bits is $\mathcal{N} = 2^n$. Note that $\lceil - \rceil$ is the integer ceiling function. The circuit families 2^e and 2^{ne} stand for *erasure* and *no erasure*. The circuit family #2 variations differ in whether ancilla qubits are erased and available for reuse upon completion of the data loading circuitry. (*) = Note that some or all of any remaining ancilla qubits at circuit completion may be entangled with the quantum state qubits.)

circuit family # 2^{ne} does not permit ancilla qubit *reuse*. However for circuit family # 2^e , ancilla qubits are erased and these qubits are available for reuse in other portions of the circuit. In family # 2^e qubits are reused as the master state ψ is constructed, decreasing the overall spatial (qubit) resource requirements for the data loading circuit.

3.3 Computing total gate counts for Circuit Family #2

3.3.1 The number of Hadamard gates

Looking back to Figure 25 on page 25 and the quantum circuits shown in Figures 7, 10 and 15, observe the overall tally of Hadamard gates is $\frac{\mathcal{N}}{2}$ for the first time slice, $\frac{\mathcal{N}}{4}$ for the second time slice, $\frac{\mathcal{N}}{8}$ for the third time slice, and so on. This summation is shown in Equation 15.

Circuit family	Final number of ancilla qubits (*)	Final total number of qubits	Total number of gates			
			CNOT	H	CSWAP	CCNot
#1	0	\mathcal{N}	\mathcal{N}	0	0	0
# 2^{ne}	$2\mathcal{N} - 2 - n$	$2\mathcal{N} - 2$	0	$\mathcal{N} - 1$	$2\mathcal{N} - n - 2$	0
# 2^e	0	n	$2(2\mathcal{N} - 2 - n)$	$\mathcal{N} - 1$	$2\mathcal{N} - n - 2$	$2\mathcal{N} - 2 - n$

Table 4: Resource requirements for data loading circuit families #1 and #2. The total number of classical bits is $\mathcal{N} = 2^n$. Note that $\lceil _ \rceil$ is the integer ceiling function. The circuit families 2^e and 2^{ne} stand for *erasure* and *no erasure*. The erasure circuit family # 2^e has additional circuitry to decouple discarded qubits from the circuit, erasing their contents and making the discarded qubits available for reuse. The circuit family #2 variations # 2^e versus # 2^{ne} differ only in whether ancilla qubits are erased and available for reuse at circuit completion. (* = Note that some or all of any remaining ancilla qubits at circuit completion may be entangled with the quantum state qubits.)

$$\sum_{k=1}^{k=n} \frac{\mathcal{N}}{2^k} = \frac{\mathcal{N}}{2} \sum_{k=0}^{k=n-1} \frac{1}{2^k} = \frac{\mathcal{N}}{2} \frac{1 - \frac{1}{2^n}}{1 - \frac{1}{2}} = \mathcal{N} \left(1 - \frac{1}{\mathcal{N}} \right) = \mathcal{N} - 1, \quad (15)$$

which is entered under the column labelled $\boxed{\text{H}}$ in Table 4 for families # 2^e and # 2^{ne} .

3.3.2 The number of Controlled Swap gates (CSwap's)

Looking back to Figure 25 on page 25 and the quantum circuits shown in Figures 7, 10 and 15, observe the tally of Controlled Swap (CSwap) gates is $\frac{\mathcal{N}}{2}$ for the first time slice, $2\frac{\mathcal{N}}{4}$ for the second time slice, $3\frac{\mathcal{N}}{8}$ for the third time slice, and so on. This summation is shown in Equation 16. Let b be a variable which will later be set to $\frac{1}{2}$.

$$\mathcal{N} \sum_{k=1}^{k=n} \frac{k}{2^k} = \mathcal{N} \sum_{k=1}^{k=n} k b^k = \mathcal{N} b \frac{\partial}{\partial b} \sum_{k=1}^{k=n} b^k = \mathcal{N} b \frac{\partial}{\partial b} \left(\frac{1 - b^{n+1}}{1 - b} - 1 \right) \quad (16)$$

$$= \mathcal{N} b \left(\frac{-(n+1)b^n}{1-b} - \frac{(1-b^{n+1})(-1)}{(1-b)^2} \right) = \mathcal{N} \left(-(n+1)b^n + 2(1-b^{n+1}) \right). \quad (17)$$

As just mentioned, in Equation 17 set $b = \frac{1}{2}$ and note that $b^n = \frac{1}{\mathcal{N}}$, so $\mathcal{N}b^n = 1$. Also note that $2b = 1$. As a result Equation 17 becomes Equation 18.

$$\mathcal{N} \sum_{k=1}^{k=n} \frac{k}{2^k} = -(n+1) + 2\mathcal{N} - 2b\mathcal{N}b^n = -(n+1) + 2\mathcal{N} - 1 = 2\mathcal{N} - n - 2. \quad (18)$$

The summation result shown in Equation 18 is entered under the column labelled CSWAP in Table 4 for circuit families $\#2^e$ and $\#2^{ne}$. As a check, note that when $\mathcal{N} = 4$, then $n = \text{Log}_2(\mathcal{N}) = 2$ and $2\mathcal{N} - n - 2 = 8 - 2 - 2 = 4$. Referring to the $\mathcal{N} = 4$ examples shown in Figures 7 and 25, on pages 11 and 25 respectively, one may verify that the number of CSwap's is indeed 4.

3.3.3 The number of Controlled Not \equiv CNOT gate's

For circuit family $\#2^{ne}$, the number of controlled Not gates is zero. Looking back to the quantum erasure circuit in Figure 17, when the erasure circuitry of circuit family $\#2^e$ is included in the gate count, two controlled Not gates are used for every qubit discarded or erased. Since in circuit family $\#2^e$ the number of discarded and erased qubits is seen in Tables 3 and 4 to be $2\mathcal{N} - 2 - n$, twice this number or $2(2\mathcal{N} - 2 - n)$ is entered in Table 4 under the Controlled Not gate count column.

3.3.4 The number of Toffoli gates \equiv CCNot gate's

For circuit family $\#2^{ne}$, the number of Toffoli gates is zero.³ Looking back to the quantum erasure circuit in Figure 17, when the erasure circuitry of circuit family $\#2^e$ is included in the gate count, one Toffoli is used for every qubit which is discarded or erased. Since in circuit family $\#2^e$ the number of discarded and erased qubits is seen in Tables 3 and 4 to be $2\mathcal{N} - 2 - n$, this is the number of Toffoli gates entered in Table 4.

4 Circuit Family #3

Circuit family #2 presents the basic approach to data loading. In either of the two #2 circuit families, 2^e or 2^{ne} , the data loading circuit depth is the primary concern.⁴ For circuit family #2 the gate depth scaling with \mathcal{N} was computed with the aid of the recursive tree diagram in Figure 25 and determined in Equation 12 on page 26 to be $\mathcal{O}\left[\left(\text{Log}_2\{\mathcal{N}\}\right)^2\right]$. Ideally one would like a gate depth which scales at most as $\mathcal{O}\left[\text{Log}(\mathcal{N})\right]$. Looking back at the gate depth computation for circuit family #2, one finds the number and implementation of CSwap's is leading to the $\mathcal{O}\left[\left(\text{Log}_2\{\mathcal{N}\}\right)^2\right]$ gate depth scaling behavior. Further examination of circuit family #2's architecture indicates the serial nature of the use of CSwap's in each time slice ultimately generates the limiting $\mathcal{O}\left[\left(\text{Log}\{\mathcal{N}\}\right)^2\right]$ scaling behavior.

Circuit family #3 reduces the CSwap gate depth for time slice # k from k to $\text{Log}_2(k)$. This reduction is implemented by using a tree-like circuit structure which enables *parallel* execution of the k CSwap's for the k 'th time slice. The tree-like parallelization circuit takes a circuit of gate depth $\text{Log}(k)$ to construct, thereby limiting the parallelization construction to a gate depth at time slice # k of $\text{Log}_2(k)$. Figure 26 demonstrates the circuit family #3

³Do not count the Toffoli gate inside the Controlled Swap gate. That Toffoli gate is accounted for in the CSwap gate count.

⁴See Figure 1.

approach for the scenario of $\mathcal{N} = 8$ classical bits.⁵ Every gate within a time slice is executed simultaneously. Thus, in time slice #4 all four controlled swap's are executed in parallel. This is allowed as all four CSwap's act on qubits which are not involved with any other gate *in that time slice*. The tradeoff is that a circuit of gate depth $\text{Log}_2(k)$ is needed to set up the simultaneous execution of the four CSwap's in one time slice. This *Log* depth circuitry is shown in time slices # 2 and #3 in Figure 26. Focussing on qubits $|a_0, a_1, a_2, a_3\rangle$ and the first three times slices of Figure 26 leads to Figure 27, where the CSwap gates shown in time slice # 4 of Figure 26 are removed for clarity.

Location in Circuit	Quantum State $ a_0, a_1, a_2, a_3\rangle$
Before Time Slice #1	$ 0000\rangle$
After Time Slice #1	$(0\rangle + 1\rangle) \otimes 000\rangle$
After Time Slice #2	$(00\rangle + 11\rangle) \otimes 00\rangle$
After Time Slice #3	$ 0000\rangle + 1111\rangle$

Table 5: Working through the quantum state transformations among the ancilla qubits in the circuit shown in Figure 27 for parallelizing the CSwap's execution. The resulting four qubit state $|a_0, a_1, a_2, a_3\rangle$ is a Shor Cat state. Time slices #5 and #6 serve to decouple the ancilla qubits a_1, a_2 and a_3 from the remaining qubits, allowing a_1, a_2 and a_3 to be used elsewhere in the circuit. *Warning: Note that for ease of presentation the sequence of qubits in the ket shown in the rightmost column of Table 5 is different than the top \rightarrow down sequence of qubits shown in the Figure 27 circuit.*

4.1 Gate depth analysis for Circuit Family #3

As done earlier, without loss of generality, let $\mathcal{N} = 2^n$ be the total number of classical bits to be loaded into a quantum state. Circuit family #3 follows the same general recursion scheme of circuit family #2, but with additional ancilla circuitry. As in circuit family #2, the recursion is broken down into a total of n stages. From the circuits in Figures 26 and 27, as well as the state transformations shown in Table 5, the gate depth of each of the k stages can be calculated. For stage k , where $k \in \{1, 2, 3, \dots, n\}$, one time slice is dedicated to the Hadamard and one time slice is dedicated to executing *all* of the stage k CSwap's. In addition,

⁵Therefore $n = \text{Log}_2(\mathcal{N}) = \text{Log}_2(8) = 3$.

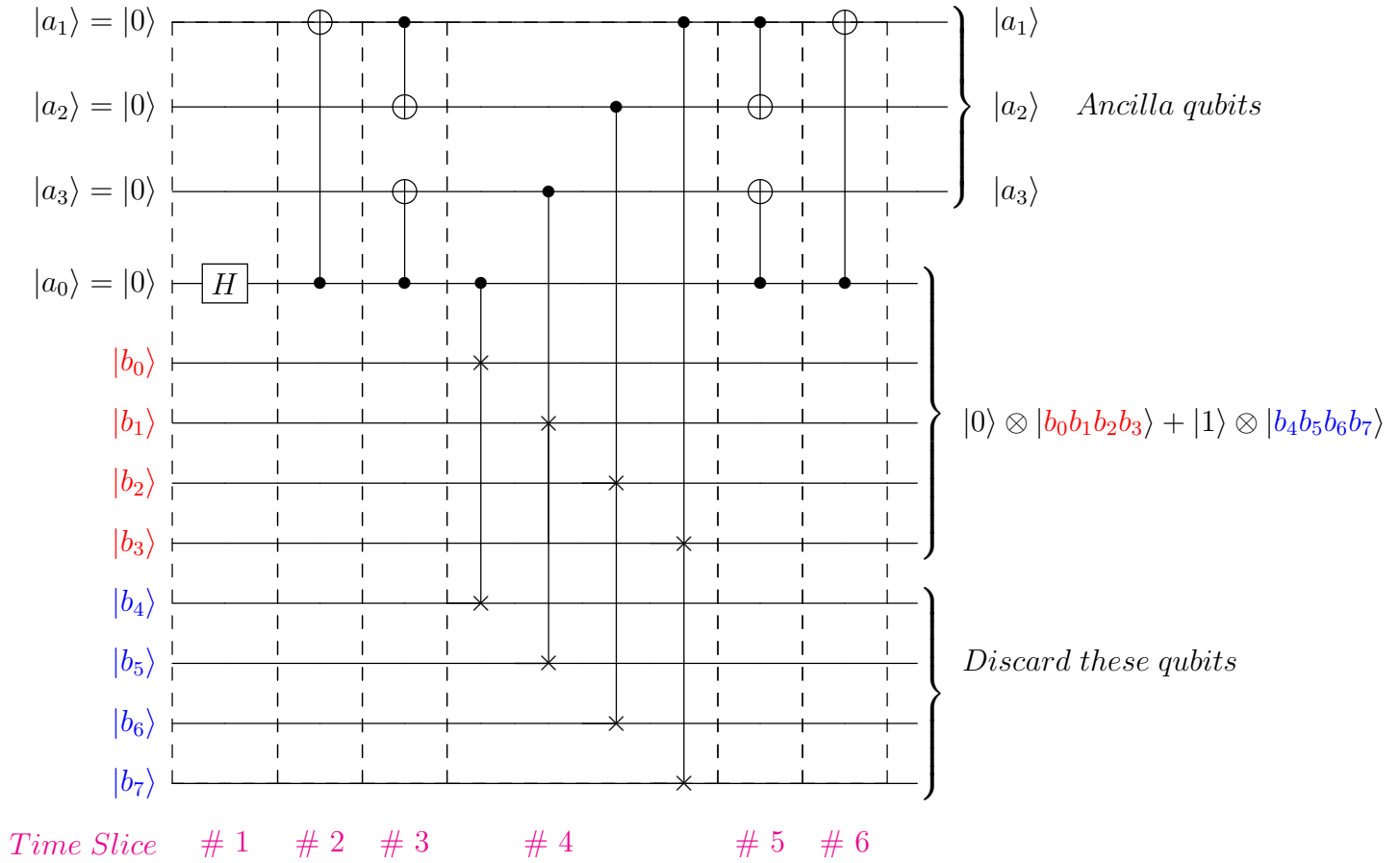


Figure 26: Circuit family #3 for $\mathcal{N} = 8$. The controlled quantum swap gate for two pairs of four qubits or eight data qubits. Note the use of superposition to build the quantum state.

each stage has one ancilla construction circuit and a corresponding ancilla deconstruction circuit. Each of these latter circuits have gate depth $\lceil \text{Log}_2(k) \rceil$. Thus the gate depth of a family # 3 circuit loading \mathcal{N} classical bits is as given in Equation 19.

$$Gate\ Depth = \sum_{k=1}^{k=n} \left(1 + 1 + \lceil \text{Log}_2(k) \rceil \right) \tag{19}$$

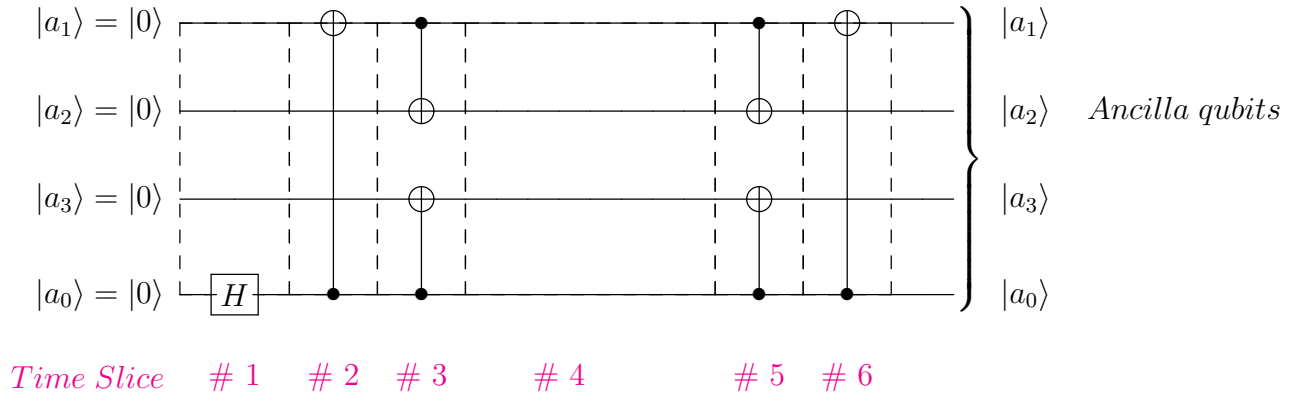


Figure 27: Gates used to minimize Circuit Family #3 gate depth. The precursor and post circuitry used in circuit family #3 for $\mathcal{N} = 8$ are for setting up the parallel CSwap execution stages in Figure 26.

$$\leq \sum_{k=1}^{k=n} \left(3 + \text{Log}_2(k) \right) = 3n + \sum_{k=1}^{k=n} \text{Log}_2(k), \tag{20}$$

where the bound $\lceil \text{Log}_2(k) \rceil \leq 1 + \text{Log}_2(k)$ is used. The key quantity in Equation 20 is the term $\sum_{k=1}^{k=n} \text{Log}_2(k)$. Rewriting the summation term in Equation 20 yields

$$\sum_{k=1}^{k=n} \text{Log}_2(k) = \text{Log}_2(e) Ln \left(\prod_{k=1}^{k=n} k \right). \tag{21}$$

Since $\prod_{k=1}^{k=n} k = n!$, applying Stirling’s approximation to first order yields Equation 22.⁶

⁶For Stirling’s approximation, see *Mathematical Methods in the Physical Sciences* by Mary Boas, Second Edition, Section 11, Page 472, Equation 11.1.

$$\sum_{k=1}^{k=n} \text{Log}_2(k) = \text{Log}_2(e) n \text{Ln}(n), \quad (22)$$

where $\text{Ln}(n)$ is the natural logarithm of n , specifically $\text{Ln}(n) \equiv \text{Log}_e(n)$. Rewrite $\text{Ln}(n) = \frac{\text{Log}_2(n)}{\text{Log}_2(e)}$ yielding

$$\sum_{k=1}^{k=n} \text{Log}_2(k) = n \text{Log}_2(n). \quad (23)$$

Recall that $n = \text{Log}_2(\mathcal{N})$ and one obtains

$$\sum_{k=1}^{k=n} \text{Log}_2(k) = \text{Log}_2(\mathcal{N}) \text{Log}_2\left(\text{Log}_2(\mathcal{N})\right) \approx \text{Log}_2(\mathcal{N}) \quad (24)$$

where the justification for the approximation in Equation 24 is given by the plot of $\text{Log}_2\left(\text{Log}_2(\mathcal{N})\right)$ shown in Figure 28. Using the result from Equation 24 in Equation 25 yields the gate depth of circuit family #3.

$$\text{Gate Depth} = 3n + \sum_{k=1}^{k=n} \text{Log}_2(k) \approx \mathcal{O}\left(\text{Log}(\mathcal{N})\right), \quad (25)$$

where the fact that $\text{Log}_2\left(\text{Log}_2(\mathcal{N})\right)$ grows very slowly with increasing \mathcal{N} , as shown in the plot of Figure 28, is used. Note that $\text{Log}_2\left(\text{Log}_2(\mathcal{N})\right)$ is essentially a constant less than 10 in value for large, but finite, \mathcal{N} in the numerical range of interest for the data loading circuitry.

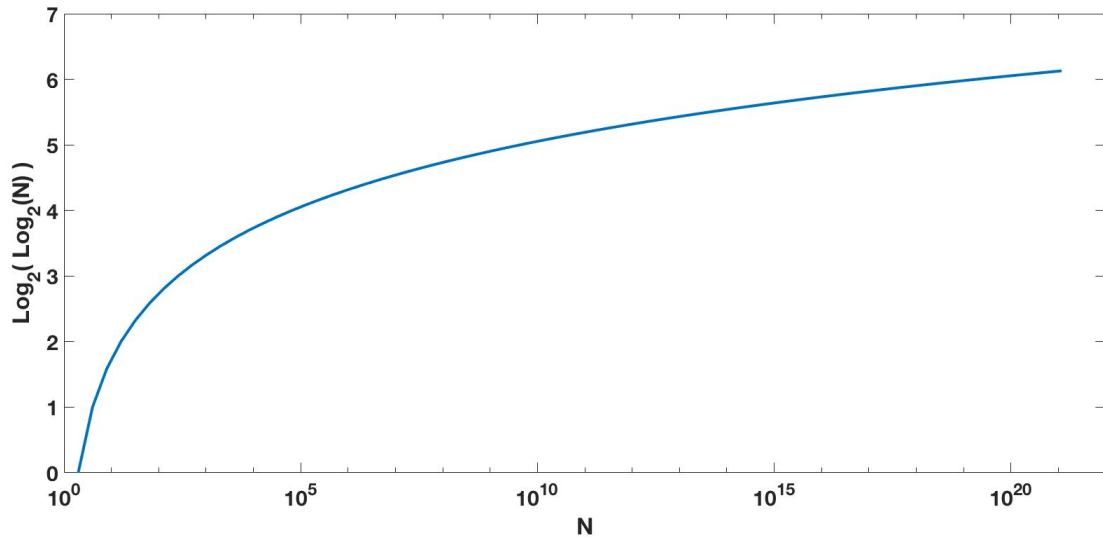


Figure 28: Plot of $\text{Log}_2(\text{Log}_2(\mathcal{N}))$ versus \mathcal{N} . See Equation 24 for application.

5 Summary

All the circuit families discussed in this document, in both the erasure and no erasure forms, have been simulated in the Quipper quantum computer simulation framework. Quipper is a well known classical computer based software tool used by the quantum computing community as a test and verification framework for proposed quantum circuits and algorithms.

To summarize, the work presented in this document describes the following.

- A practical circuit family (#3) which loads \mathcal{N} classical bits into a quantum data structure of size $\text{Log}_2(\mathcal{N})$ qubits in a quantum circuit depth of $\mathcal{O}(\text{Log}(\mathcal{N}))$. Both this data structure size and this gate depth are critical requirements for generic quantum algorithms and circuits exhibiting exponential speedup over their classical algorithm and circuit counterparts.
- Classical compression with quantum decompression can ease the complexity and gate count of the data loading circuitry, while optimizing the transfer of bits into qubits. The design methodology described shows how classical compression/quantum decompression schemes can be designed using classical compression and decompression algorithms.
- Ancilla qubits are used in circuits detailed in this document, as well as in most circuits in the literature. Ancilla qubits are typically discarded after use, which means that in practice the ancilla qubits are preserved, but ignored, until the end of the computation[1]. In practice, rather than preserve but ignore these idle qubits until the completion of the computation, one would like to reuse these ancilla qubits so as to keep the spatial overhead (the # of qubits used by the computation and/or circuit) to a minimum. Section 2.5 of this document describes a procedure and associated family of quantum circuits which decouple discarded qubits from the main body of qubits in use during the computation, thereby enabling the discarded qubits to be reused later in the circuit and as a result minimizing overall spatial qubit usage in a quantum circuit computation.

6 Acknowledgements

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7 Bibliography

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- [1] *An Introduction to quantum information and quantum circuits* by John Watrous, Published in The Association of Computing Machinery - Special Interest Group in Algorithms and Computation Theory (ACM SIGACT), June, 2011, Volume 42, Issue Number 2, Page 52-67.