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Low-Noise Amplifiers (LNAs) and Power Amplifiers (PAs) for Next-Generation S- and X-Band Radars

by John E Penn

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Low-Noise Amplifiers (LNAs) and Power Amplifiers (PAs) for Next-Generation S- and X-Band Radars

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Sensors and Electron Devices Directorate, CCDC Army Research Laboratory

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<tr><td colspan="6">14. ABSTRACT
The US Army Combat Capabilities Development Command Army Research Laboratory (CCDC ARL) has been evaluating and designing efficient broadband high-power amplifiers for future adaptive multimode radar systems in addition to other circuits for use in communications, networking, and electronic warfare (EW). ARL submitted designs of broadband amplifiers, power amplifiers, high-dynamic range low-noise amplifiers, high-power switches, frequency multipliers, and other circuits for future radar, communications, EW, and sensor systems using Qorvo’s high-performance 0.15-µm gallium nitride (GaN) fabrication process. This technical note briefly summarizes several designs using Qorvo’s 0.15-µm high-power, efficient GaN on 4-mil silicon carbide process that were submitted to an ARL prototype wafer option fabrication.</td></tr>
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1. Introduction

The US Army Combat Capabilities Development Command Army Research Laboratory (CCDC ARL) has been evaluating and designing efficient broadband high-power amplifiers and robust low-noise amplifiers (LNAs) for future multimode radar systems that could be used in other applications such as communications, networking, and electronic warfare (EW). ARL submitted designs of broadband amplifiers, power amplifiers (PAs), and high-dynamic range LNAs for future radar, communications, EW, and sensor systems using Qorvo's high-performance 0.15-µm gallium nitride (GaN) fabrication process. The circuits most applicable to radar applications are documented in this technical report. When the fabricated designs are returned and tested, future technical reports will document results of circuit characterization.

2. S- and X-Band Low-Noise Amplifier

Not all high-electron-mobility transistor (HEMT) models in the Qorvo 0.15-µm GaN process design kit (PDK) had noise figure data, which are necessary for the design of an LNA. Initially, gain, noise figure, quality factor (Q) of the optimal noise match, and stability were simulated over 2–10 GHz for the recommended HEMT sizes with noise data of 4 × 25 µm and 6 × 25 µm. Some source inductance was used to optimize the performance tradeoffs, with the 6- × 25-µm HEMT chosen for the initial design. DC biases of 5 and 10 V were recommended for low-noise applications, rather than the 25 to 28 V that would be typical for high-power applications. These designs should be able to operate over a large range of DC, though the best noise figure is typically at a moderately low-drain current.

Initial lossless matched LNA designs achieved good noise figure, very good gain, and conditional stability over an octave bandwidth, 3–6 GHz, 4–8 GHz, or 5–10 GHz, but achieving 3–10 GHz bandwidth with good stability, noise figure, gain, and return loss was difficult. Large coupled lines, such as used on a prior Raytheon GaN fabrication[1] were suitable for larger bandwidths but compact lumped element matching circuits resulted in the best compromise of layout area, noise figure, stability, and gain. Figure 1 shows a schematic of the initial design using ideal lossless matching elements, while Fig. 2 shows its corresponding linear simulation. The noise figure (green, right axis) is well below 1 dB from 3 to 12 GHz, and gain is above the 10-dB goal from 3 GHz to above 9 GHz. Note that with ideal lossless matching elements there is a stability problem near 2 GHz (black, right axis). When lossy monolithic microwave integrated circuit (MMIC) elements are substituted into the output matching network and the source feedback inductors, the gain decreases but the stability improves. Figure 3 shows better than 10 dB gain from 3 to 9 GHz, and the noise figure is still below 1 dB over the desired range. Conditional stability is achieved for nominal loads (near 50 ohms), but there is still a potential instability near 3 GHz for poor matches (Mu > 0.4). When the lossless input match is converted to MMIC elements, unconditional stability is achieved, but the gain drops about 1.5 dB, below the 10 dB goal, and the noise figure increases nearly 0.5 to a respectable 1.4 dB over a broad frequency range from 3.3 GHz up to 10 GHz. Linear simulations of the full MMIC layout are shown in Fig. 4. The layout was then electromagnetic (EM)-simulated and readjusted to achieve performance similar to the original MMIC linear simulation (Fig. 5). Final layout of the S- to X-band LNA is shown in Fig. 6.

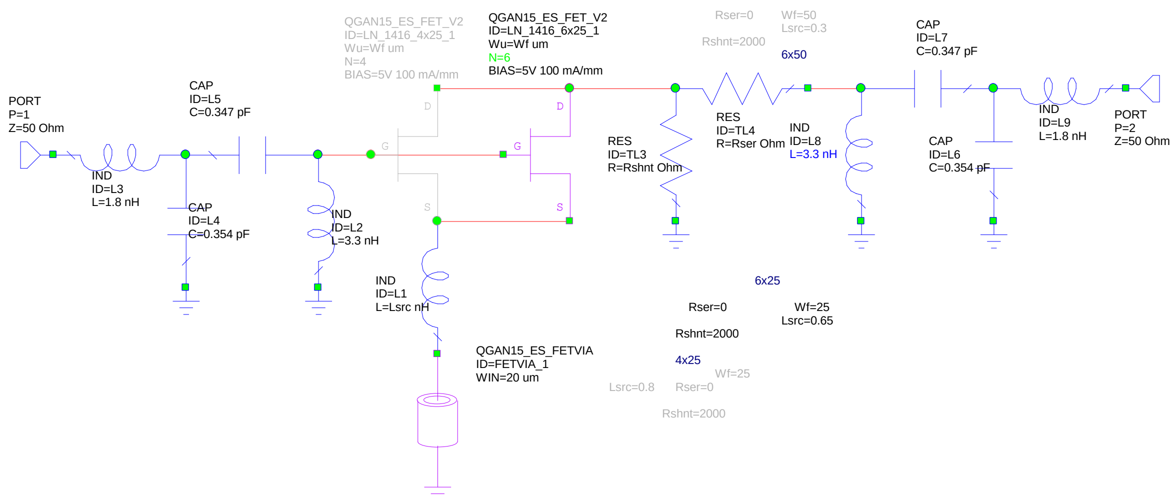


Fig. 1 S- to X-band LNA ideal schematic (6- × 25-µm HEMT)

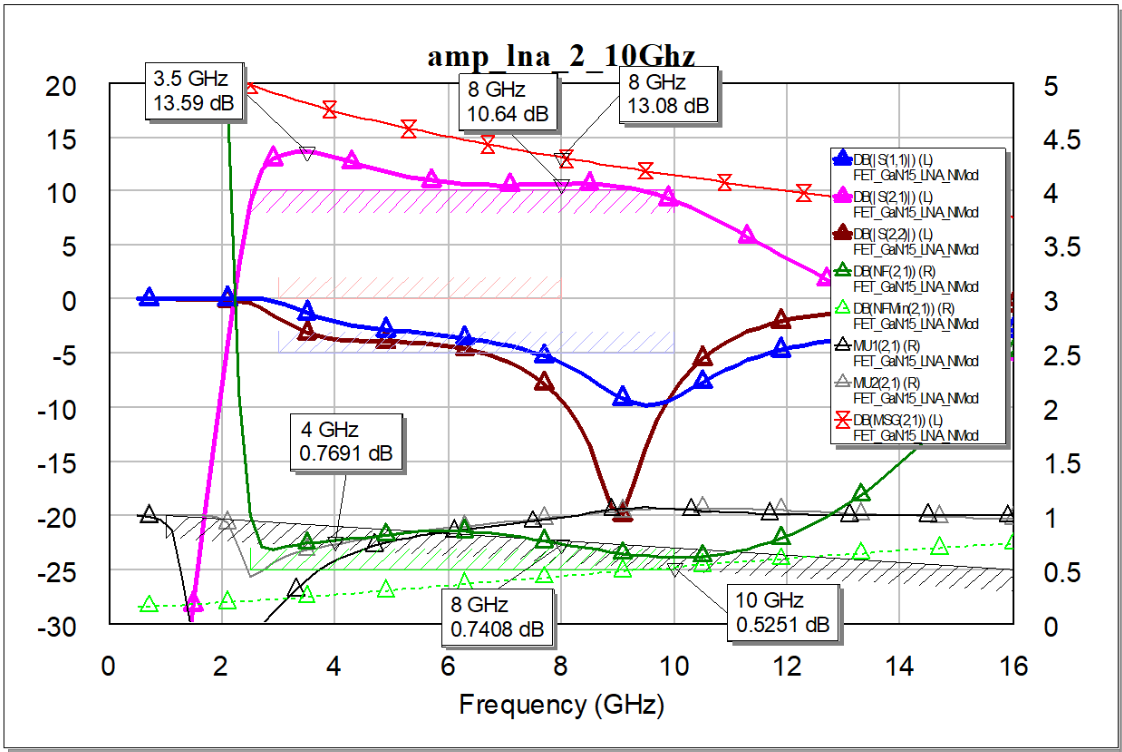


Fig. 2 S- to X-band LNA simulation (ideal lossless match)

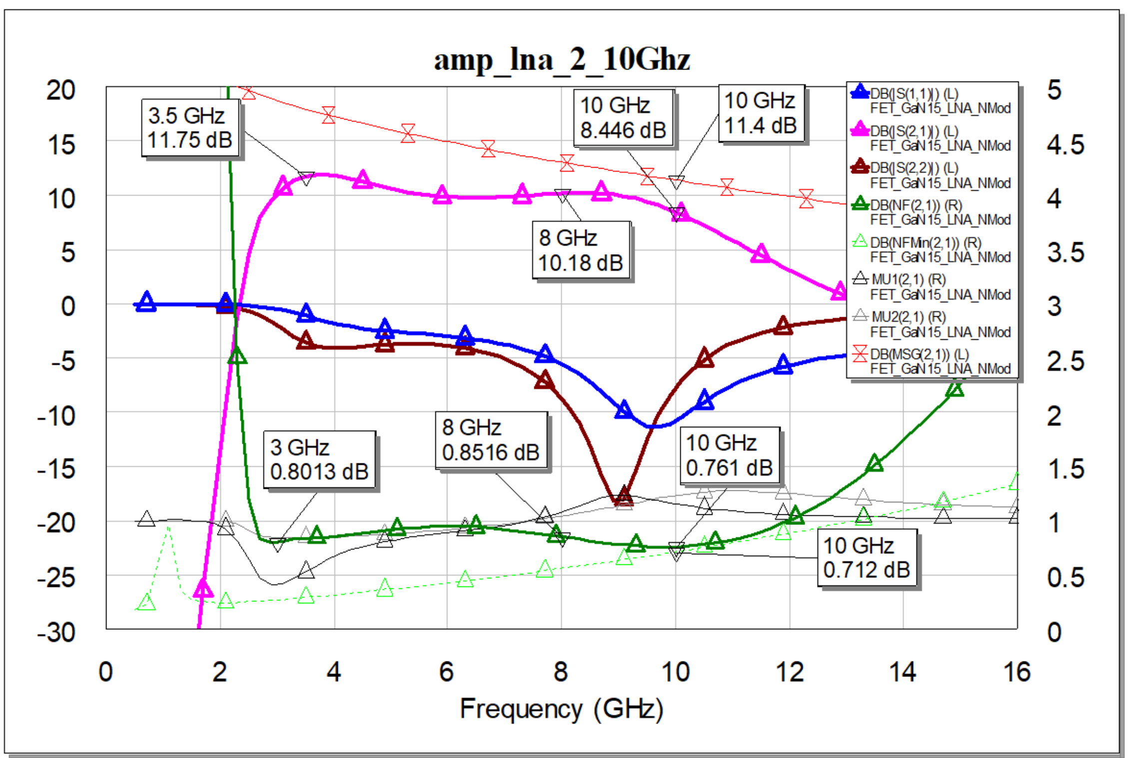


Fig. 3 S- to X-band LNA simulation (lossless input match, MMIC output match)

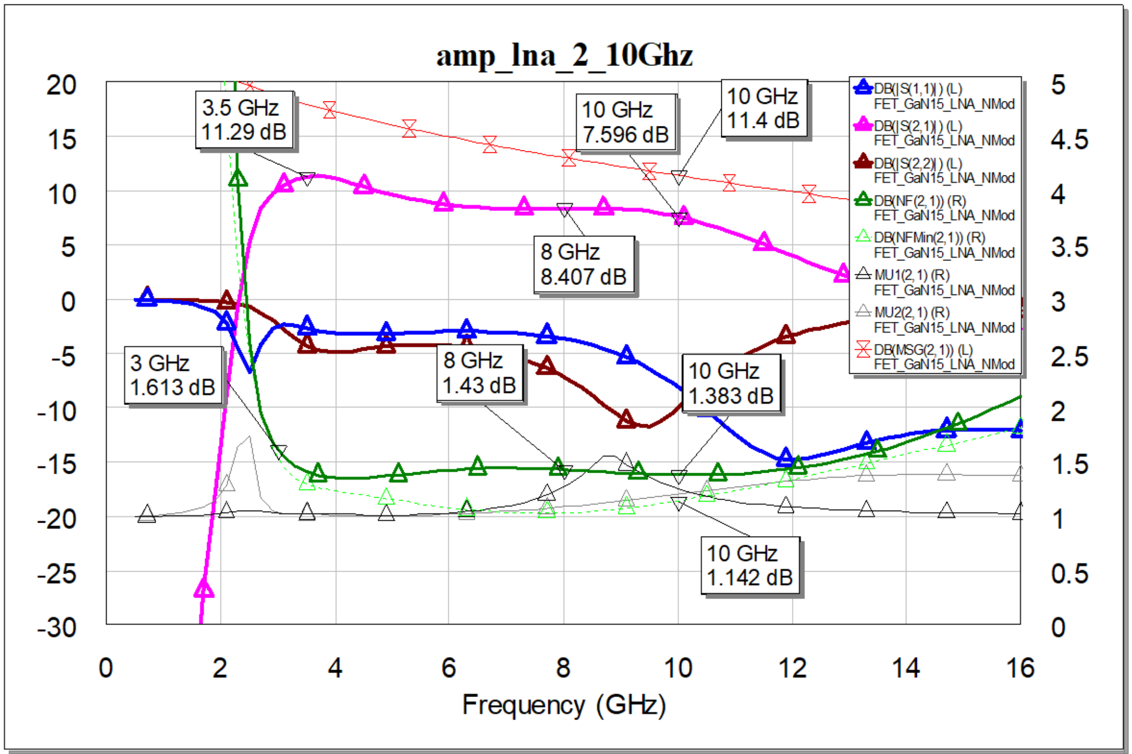
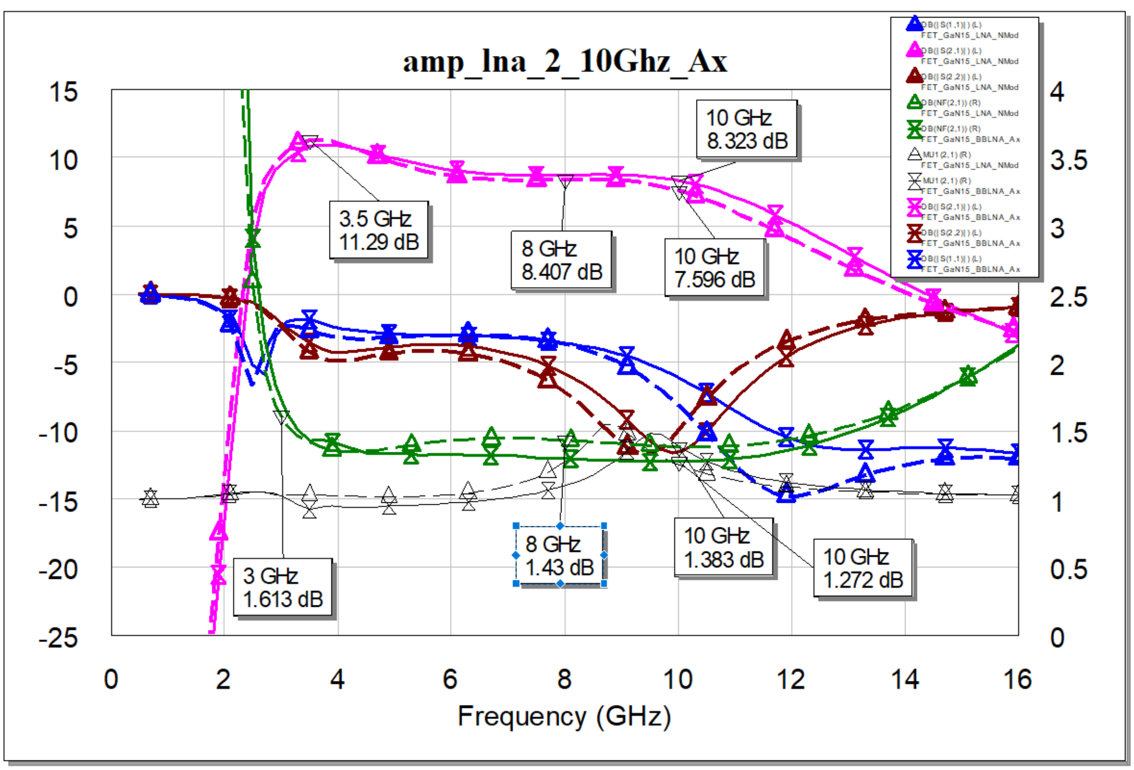


Fig. 4 S- to X-band LNA simulation (full MMIC layout)



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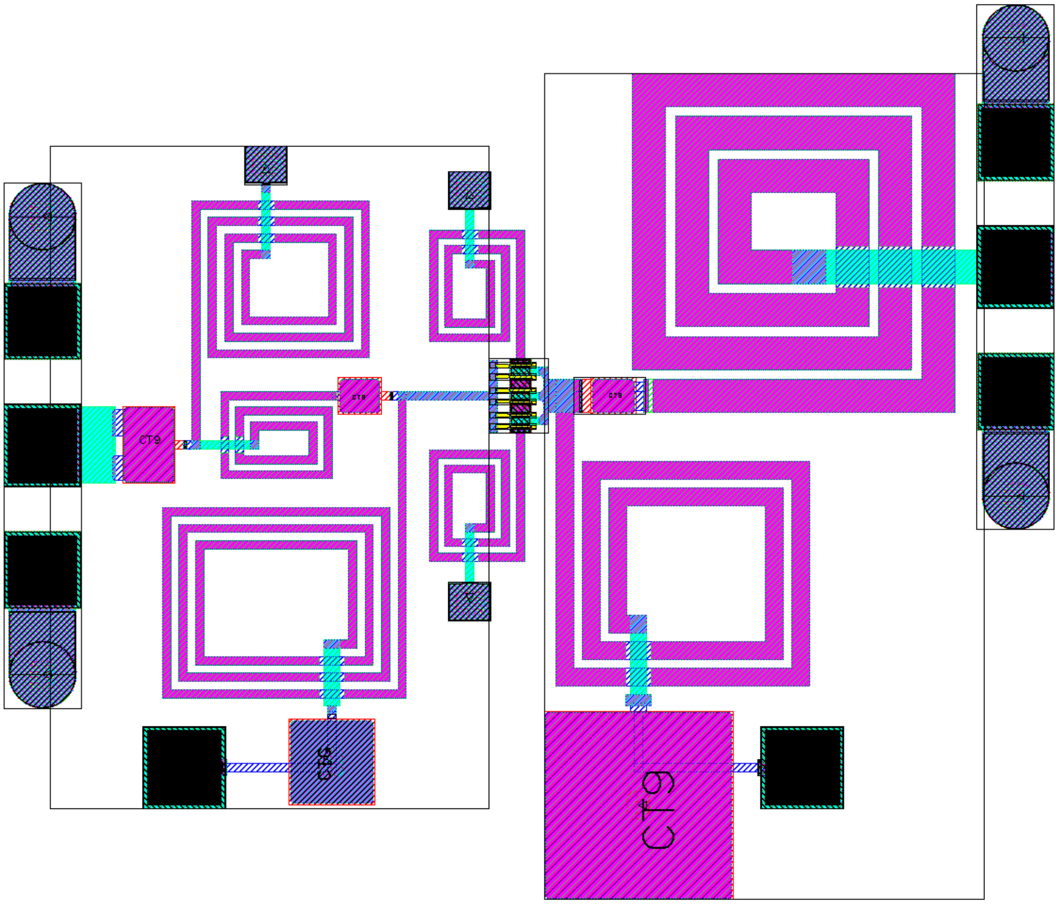

Fig. 6 S- to X-band LNA layout

3. S- and X-Band Power Amplifier

For the design of an S- to X-band PA, load pull simulations were performed on a 1-mm (8- × 125-µm) HEMT at 3, 6, and 9 GHz. The maximum allowed DC bias for the 0.15-µm GaN process is 28 V and that was assumed for this PA design to maximize power. Figure 7 shows an example of the power and power-added efficiency (PAE) contours at 6 GHz for a 1-mm HEMT, yielding a maximum 60% PAE for a load of 0.62 at 75° and a Q of 1.95. Maximum power of 37.1 dBm (5.1 W) is shown for a load of 0.43 at 98° and a Q of 1.05, and a very good compromise load of 0.47 at 94° and a Q of 1.2 yields 37 dBm (5 W) and 55% PAE. Lower Q means larger achievable bandwidth, and the compromise target impedance yields 5 W/mm with 55% PAE at 28 V. These load pull simulations were used to create a simple scalable model of the target load impedance. A slightly larger 8- × 150-µm (PDK limit) HEMT was chosen to achieve 5 W per device with 0.8-dB margin for losses. In order to achieve higher powers, multiple HEMTs would have to be parallel combined. A 10-W PA design was later achieved by paralleling two 8- × 150-µm HEMTs, starting with this initial 8- × 150-µm HEMT 5-W PA design. Another ideal lossless matched PA design based on 8- × 93-µm HEMTs achieved very good gain but the bandwidth was less than desired. Figure 8 shows linear simulations of an initial 8- × 93-µm PA (solid lines) and a two-way combined 8- × 93-µm PA at twice the output power. Very good maximum efficiency (PAE) of 52% PAE was simulated with 3.5 W for the single 8- × 93-µm PA and 7 W for the two-way combined 8- × 93-µm PA at 3-dB gain compression and peak efficiency (Fig. 9). A redesign with a larger HEMT device was needed for the 5-W and 10-W power goals, and additional compromises in performance would be needed to achieve the bandwidth goals of S- to X-band (3–10 GHz). A larger 8- × 175-µm HEMT was used in a prior successful PA design in Qorvo's 0.25-µm GaN process, but the 0.15-µm GaN PDK would not allow scaling the nominal 8- × 100-µm HEMT beyond 8- × 150-µm, so these second PA (no. 2) designs were limited to 8 × 150 µm (1.2 mm). The ideal lossless matched single-stage 8- × 150-µm PA no. 2, whose schematic is shown in Fig. 10, predicts 7 W (38.6 dBm) at less than 3-dB gain compression with an excellent 54% PAE that is still rising toward its peak (Fig. 11).

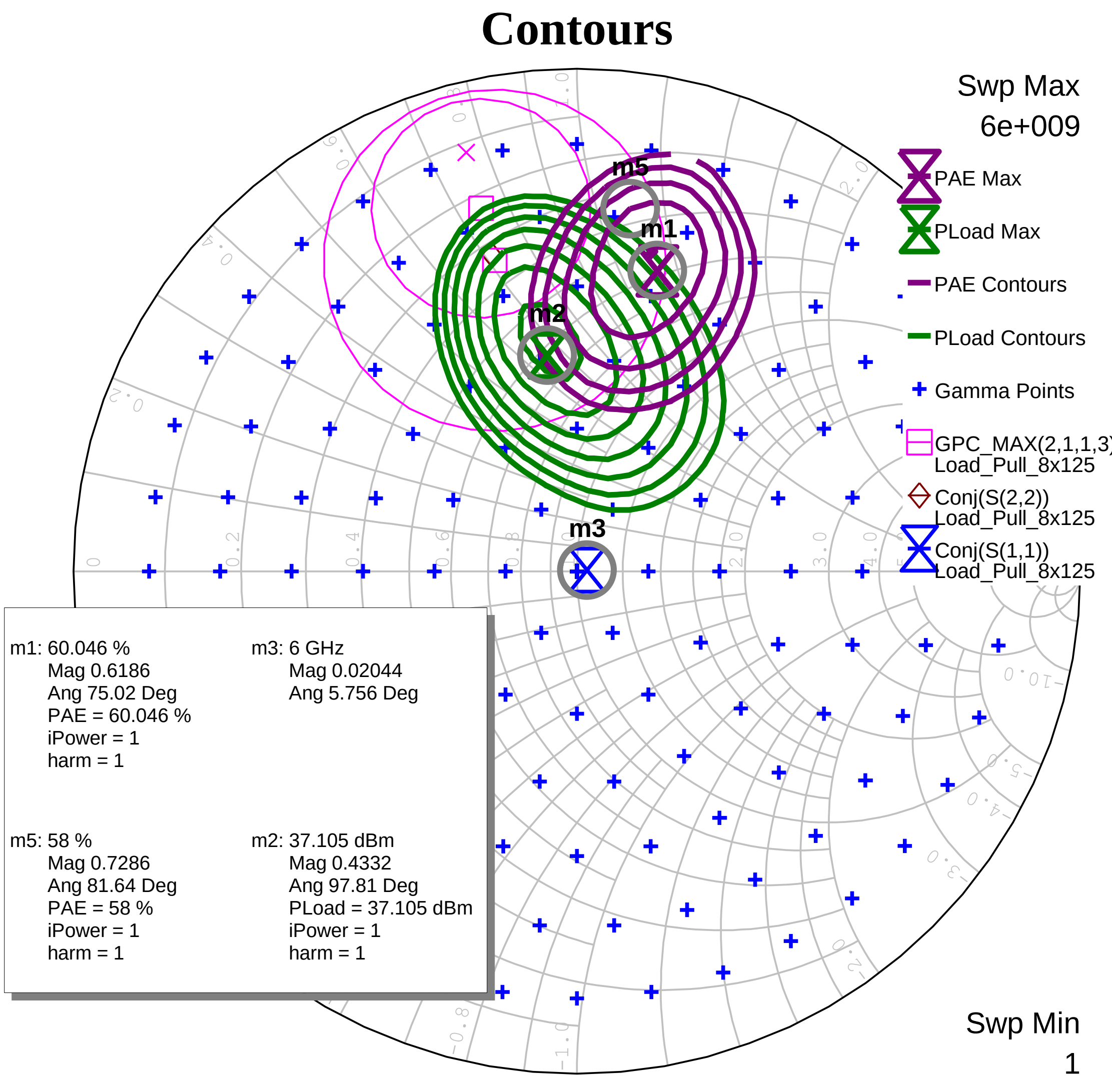

Fig. 7 Power (green) and efficiency (magenta) contours at 6 GHz (8 × 125 µm)

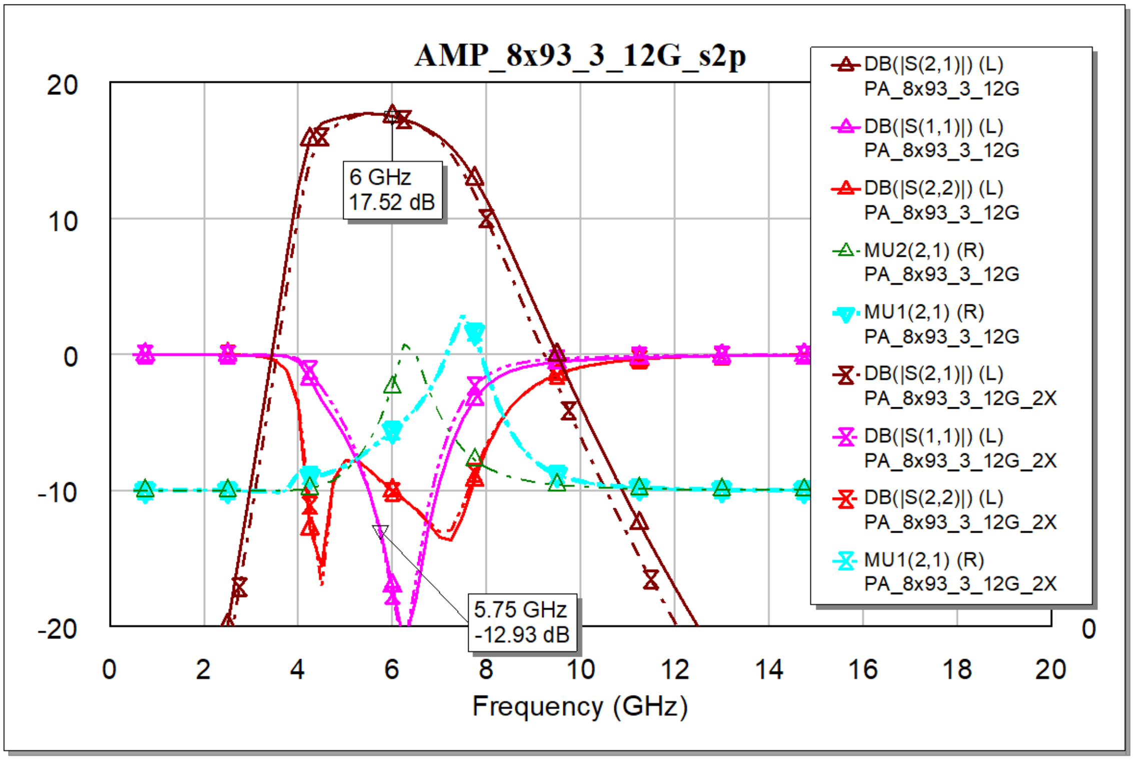

Fig. 8 Initial ideal 3.5- and 7-W PA linear simulations (8 × 93 µm vs. two 8 × 93 µm)

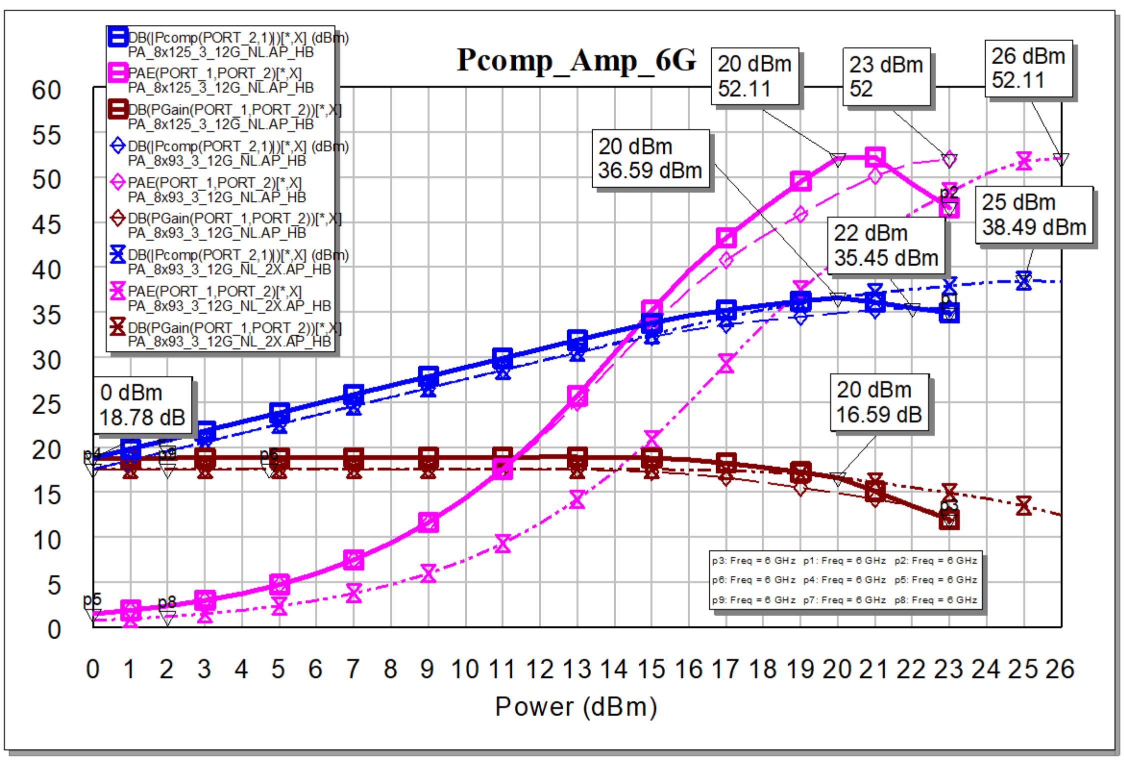

Fig. 9 Power and PAE simulations at 6 GHz of ideal 3.5-W (solid) and 7-W PA (dotted)

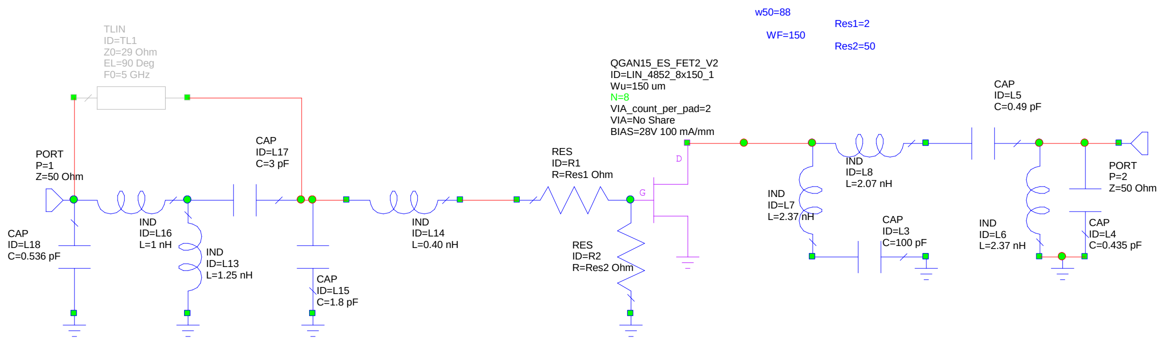

Fig. 10 **Ideal PA no. 2 schematic (8- × 150-µm HEMT)**

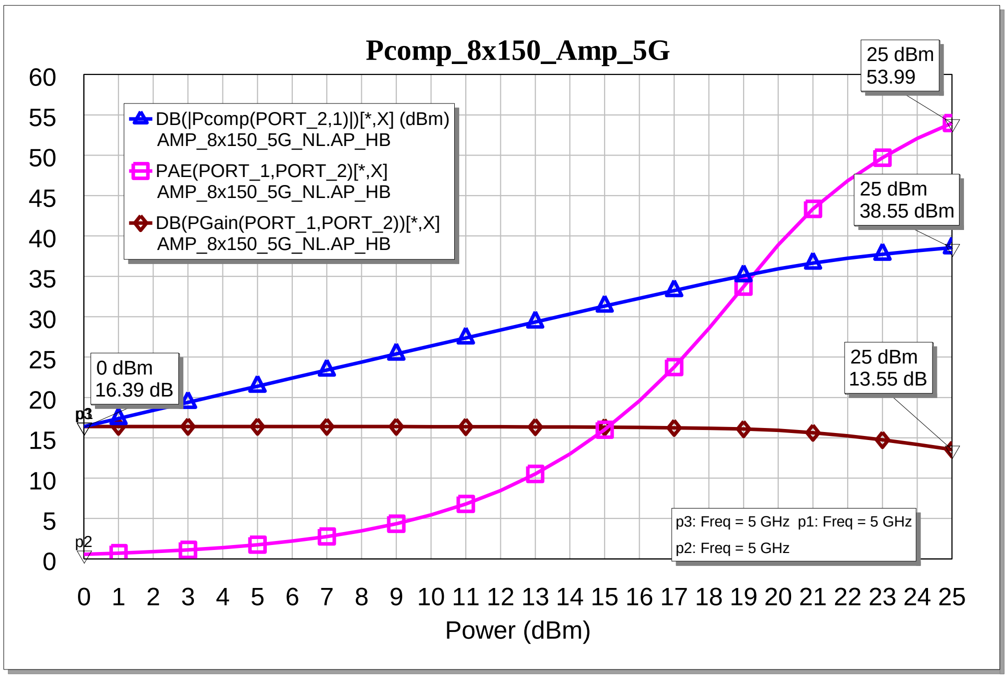

Fig. 11 **Power and PAE simulations at 6 GHz of ideal PA no. 2 (8 × 150 µm)**

In increase the gain bandwidth, the input match of the 8- × 150-µm PA was increased in complexity to achieve broadband S- to X-band gain, 3–9 GHz. Stable gain was achieved with nearly identical gain performance for the lossy MMIC PA design versus the original ideal lossless PA as shown in Fig. 12. Comparing the ideal output match design to the desired optimal parallel resistor-capacitor load model shows excellent match from about 2.6 to 9 GHz (Fig. 13, dashed lines). Converting the broadband output match to actual MMIC elements reduced the bandwidth slightly with minimal losses of 0.5–0.6 dB across most of the band, rolling off below 3 GHz and above 9 GHz (Fig. 13, solid lines). A 0.5-dB loss corresponds to about 12% power and efficiency loss in the output match compared to the ideal case. Output power and PAE performance simulations for the ideal lossless S- to X-band 8- × 150-µm PA from 3 to 9 GHz are shown in Fig. 14. Efficiency (PAE) ranges from a peak of 60% at 3 GHz to 52% at 9 GHz, while output power is approximately 6.75 W (38.3 dBm) from 3 to 7 GHz, falling off some at 8 and 9 GHz, with an input power of 0.5 W (27 dBm). Once the 0.5-dB losses of the actual MMIC matching elements are factored in, the output power drops to 6 W (37.8 dBm), falling even more at 8 and 9 GHz, with an input power of 0.5 W (27 dBm), while PAE drops to a peak of 51% at 3 GHz, dropping farther to a peak PAE of 44% at 9 GHz. Figure 15 shows the simulated output power and PAE performance for the S- to X-band 8- × 150-µm PA with lossy MMIC matching circuits from 3 to 9 GHz. When the MMIC layout is EM-simulated and the layouts readjusted to get back to the prior performance, the output power is similar, as are the peak efficiencies which range from about 44% to 50% as shown in Fig. 16. The small signal linear performance of the final layout (EM) is shown in Fig. 17 and is very similar to the original MMIC linear simulation. Final layout plot of the compact 5- to 6-W broadband 3- to 9-GHz PA is shown in Fig. 18.

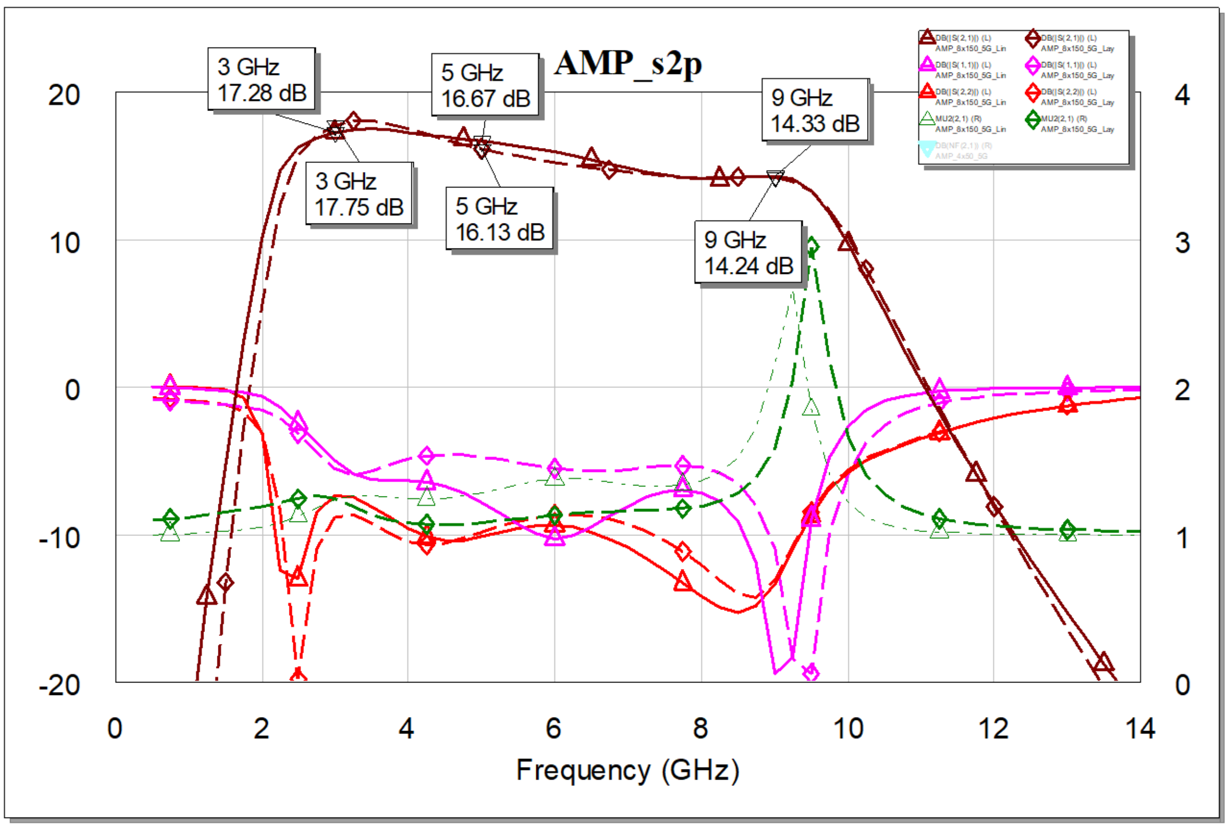

Fig. 12 Revised S- to X-band 8- × 150-µm PA simulations: ideal (dash) vs. MMIC (solid)

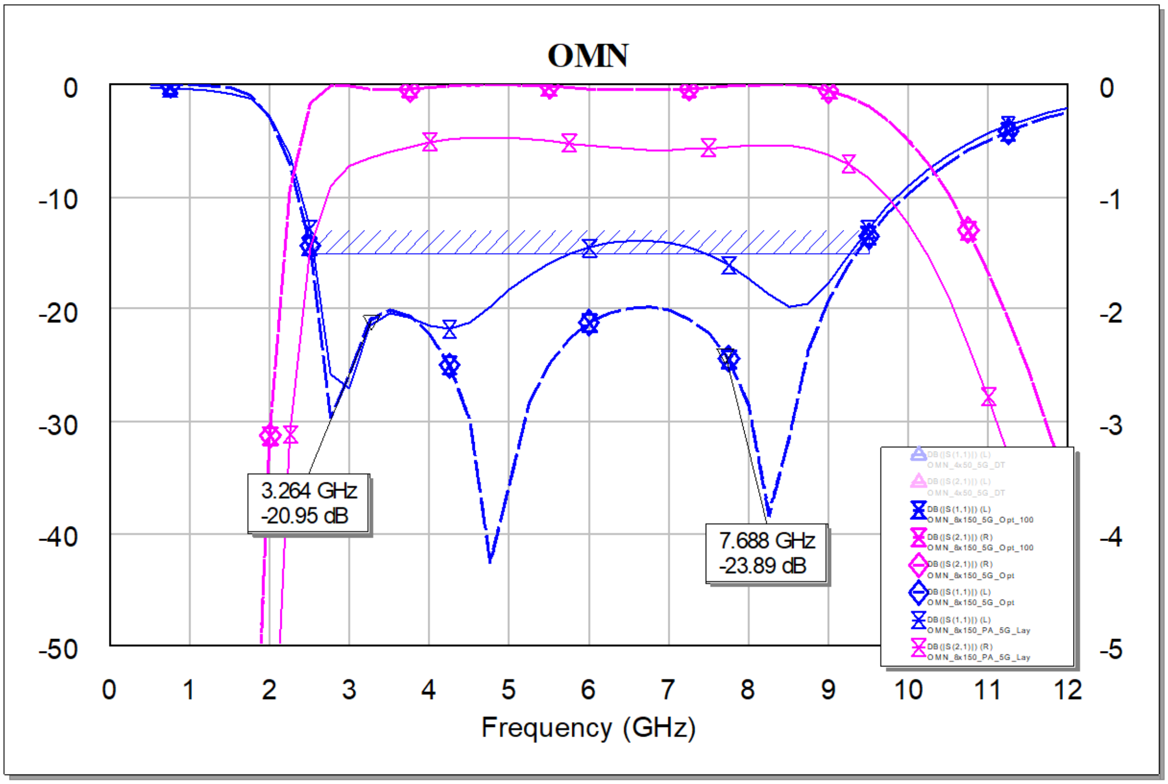

Fig. 13 Output match of S- to X-band 8- × 150-µm PA simulation: ideal (dash) vs. MMIC (solid)

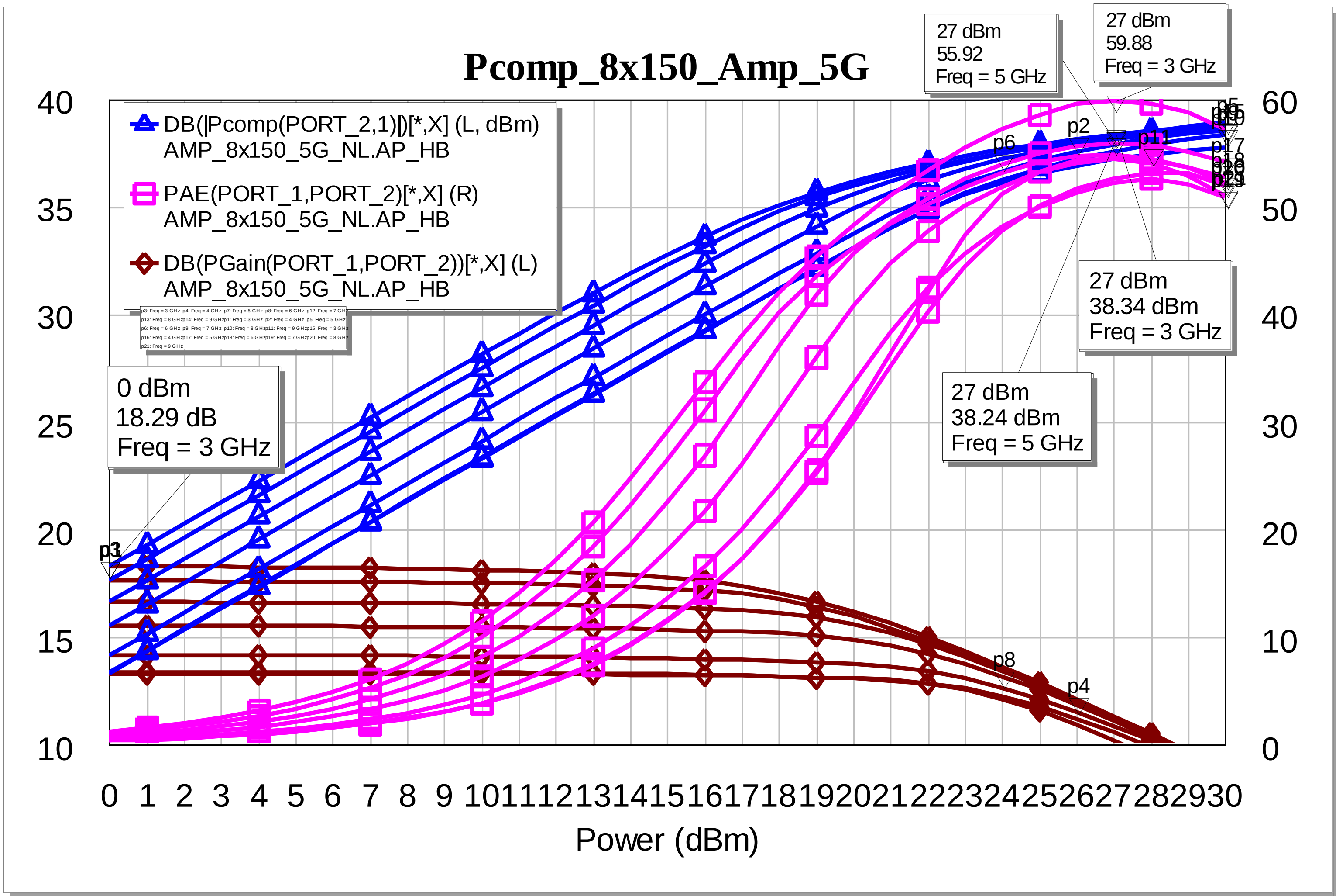

Fig. 14 **Power and PAE of 8- × 150-μm PA from 3 to 9 GHz, ideal lossless design (28 V)**

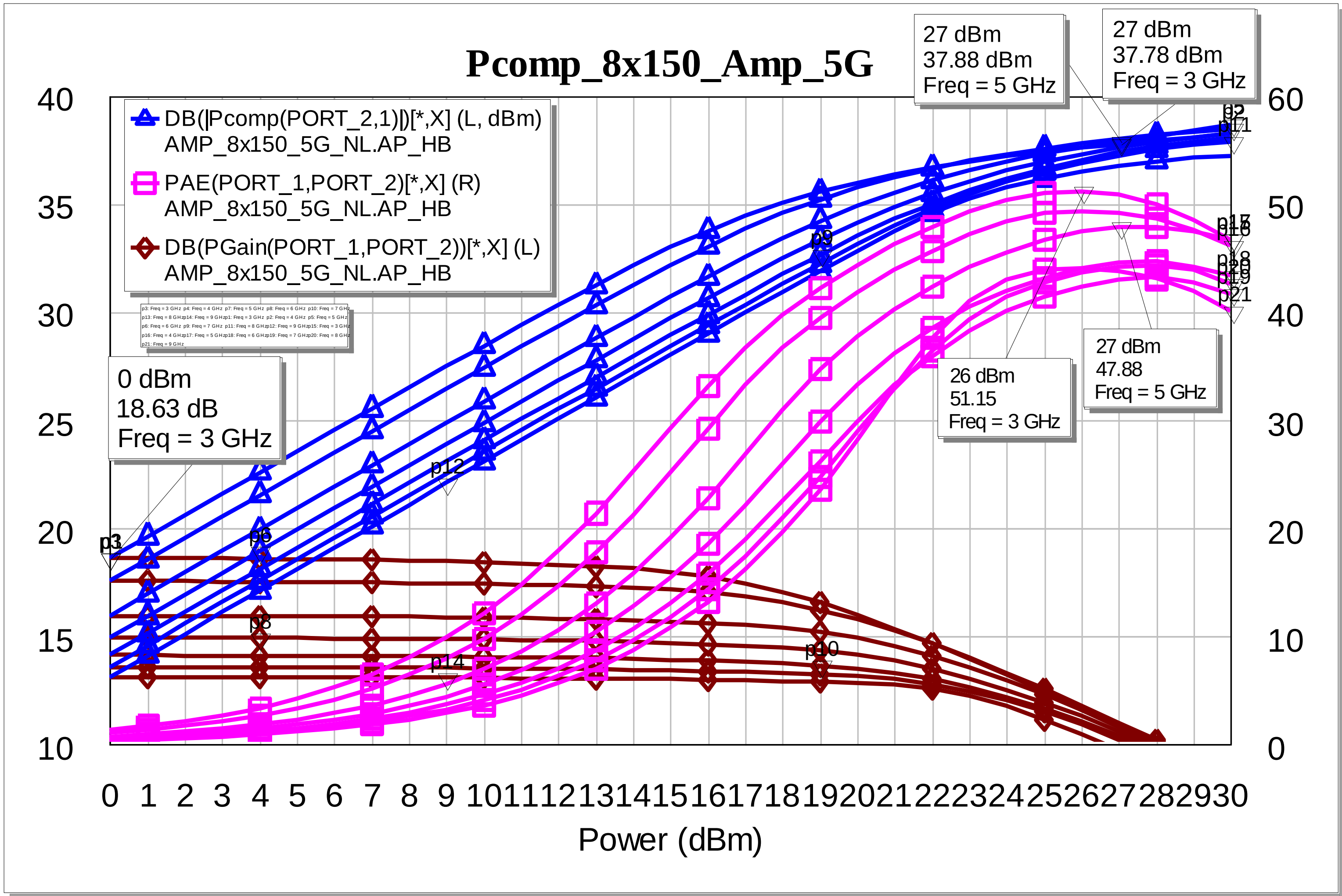

Fig. 15 **Power and PAE of 8- × 150-μm PA from 3 to 9 GHz, with lossy MMIC elements (28 V)**

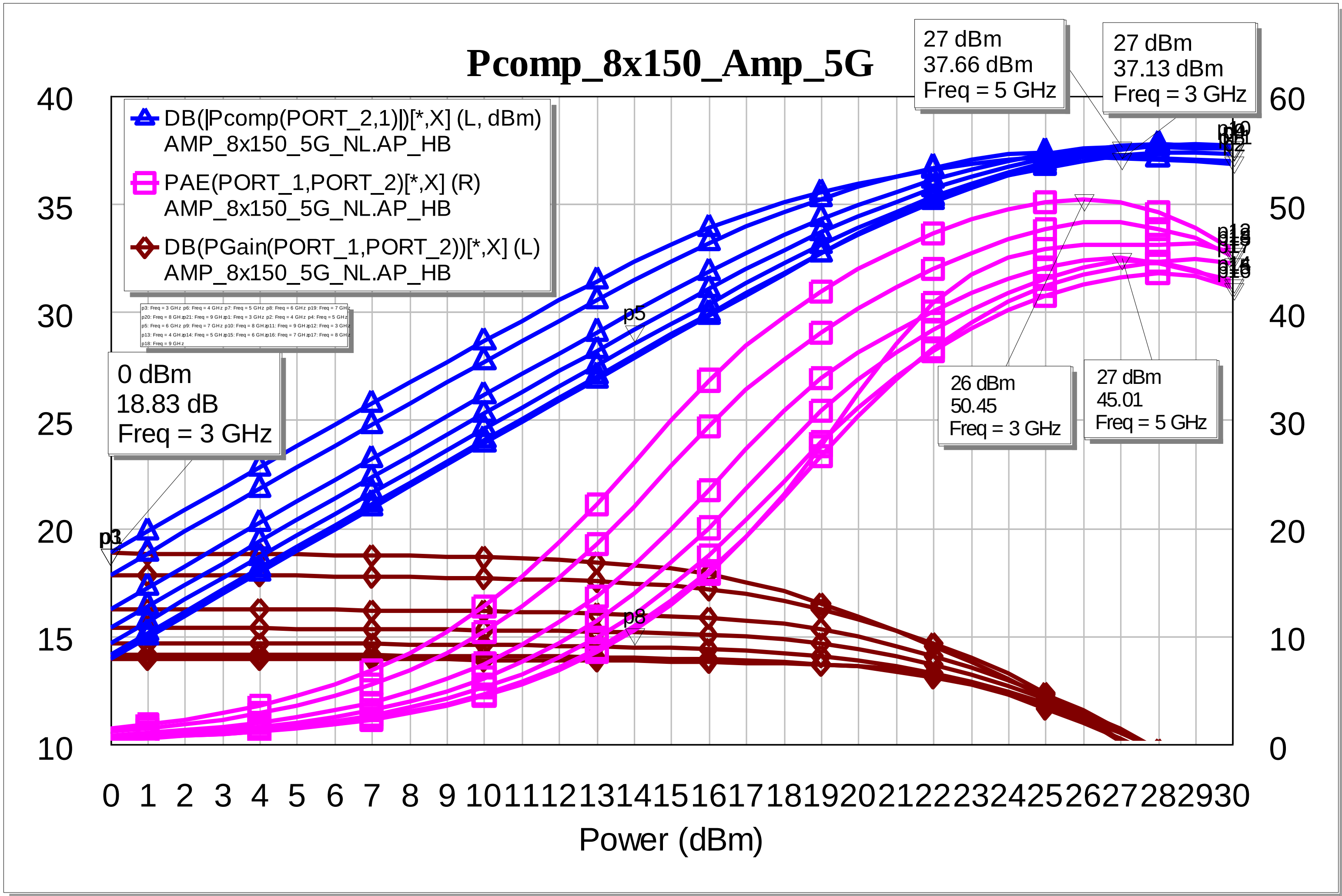

Fig. 16 **Power and PAE of 8- × 150-µm PA from 3 to 9 GHz, final layout EM (28 V)**

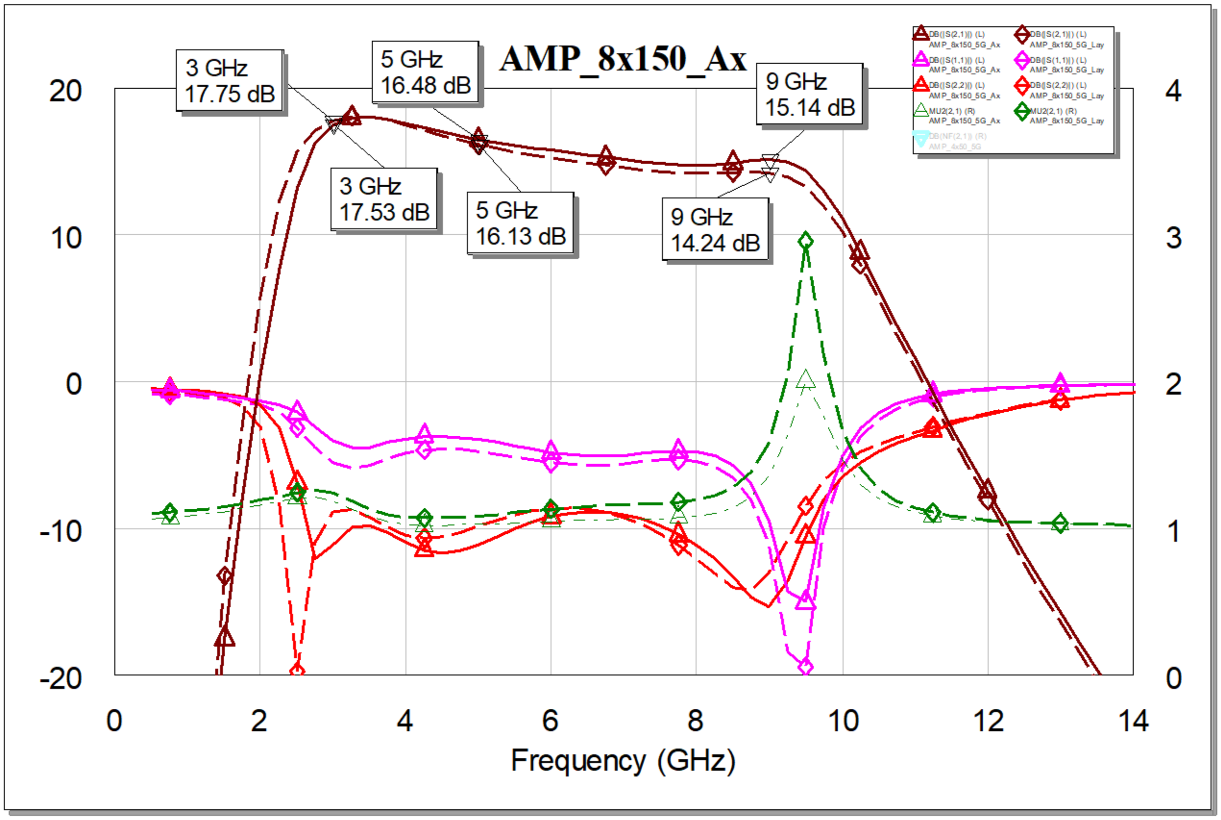

Fig. 17 S- to X-band 8- × 150-µm PA simulations: MMIC (dash) vs. EM (solid)

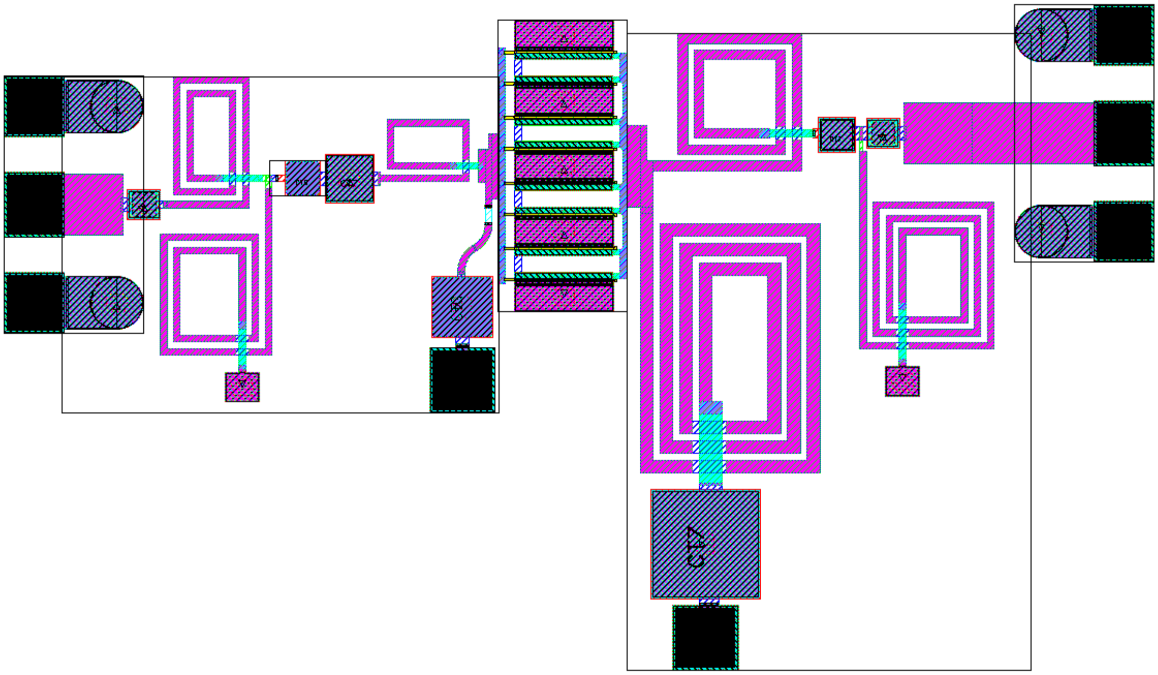

Fig. 18 Final compact layout of 8- × 150-µm S- to X-band PA

4. S- and X-Band 10-W Power Amplifier

The previous 5- to 6-W S- to X-band PA design was used as the basis for parallel combining two 8- × 150-μm HEMTs to achieve a 10-W output power goal. First, an ideal double-tuned lossless output match for an 8- × 150-μm HEMT was designed based on the prior ideal match to 50 ohms but translated to 100 ohms. Then, two of these circuits were combined in parallel to create the output match to 50 ohms. Output power and PAE performance simulations for the ideal lossless S- to X-band 2X 8- × 150-μm PA from 3 to 9 GHz are shown in Fig. 19. Efficiency (PAE) ranges from a peak of 58% at 3 GHz, to 49% at 9 GHz, while output power is up to 16 W (42 dBm) with an input power of 1 W (30 dBm). Once the 0.75-dB losses of the actual MMIC matching elements are factored in, the output power is as high as 13.2 W (41.1 dBm), falling off at 7 to 9 GHz, with an input power of 1 W (30 dBm), while PAE is a peak of 50% at 4 GHz, dropping to a peak PAE of 31% at 9 GHz. Figure 20 shows the simulated output power and PAE performance for the S- to X-band 2X 8- × 150-μm 10-W PA with lossy MMIC matching circuits from 3 to 9 GHz. When the MMIC layout is EM-simulated and the layouts readjusted to get back to the prior performance, the output power ranges from 10 to 12 W from 3 to 9 GHz, while PAE ranges from 39% to 48% with an input power of 1 W (30 dBm), as shown in Fig. 21. The small signal linear performance of the final layout of the parallel 10-W PA versus the prior single 8- × 150-μm PA is shown in Fig. 22. It is similar in shape but the gain is 2 to 3 dB lower than the prior 5- to 6-W PA. The small signal linear performance of the final layout (EM) is shown in Fig. 23 and is very similar to the original MMIC linear simulation. Final layout plot of the compact 10- to 12-W broadband 3- to 9-GHz PA is shown in Fig. 24.

Note the odd-mode stabilizing resistors between the gates and drains of the two parallel combined 8- × 150-μm HEMTs shown in the layout of Fig. 24. An analysis of the odd-mode stability showed a potential problem around 5.2–6.6 GHz that could be removed with either an odd-mode resistor on the gates of less than 150 ohms or an odd-mode resistor on the drains of less than 250 ohms. To provide margin in avoiding an odd-mode oscillation, both a 100-ohm resistor placed on the gates and a 200-ohm resistor placed on the drains were added to the two parallel 8- × 150-μm HEMTs.

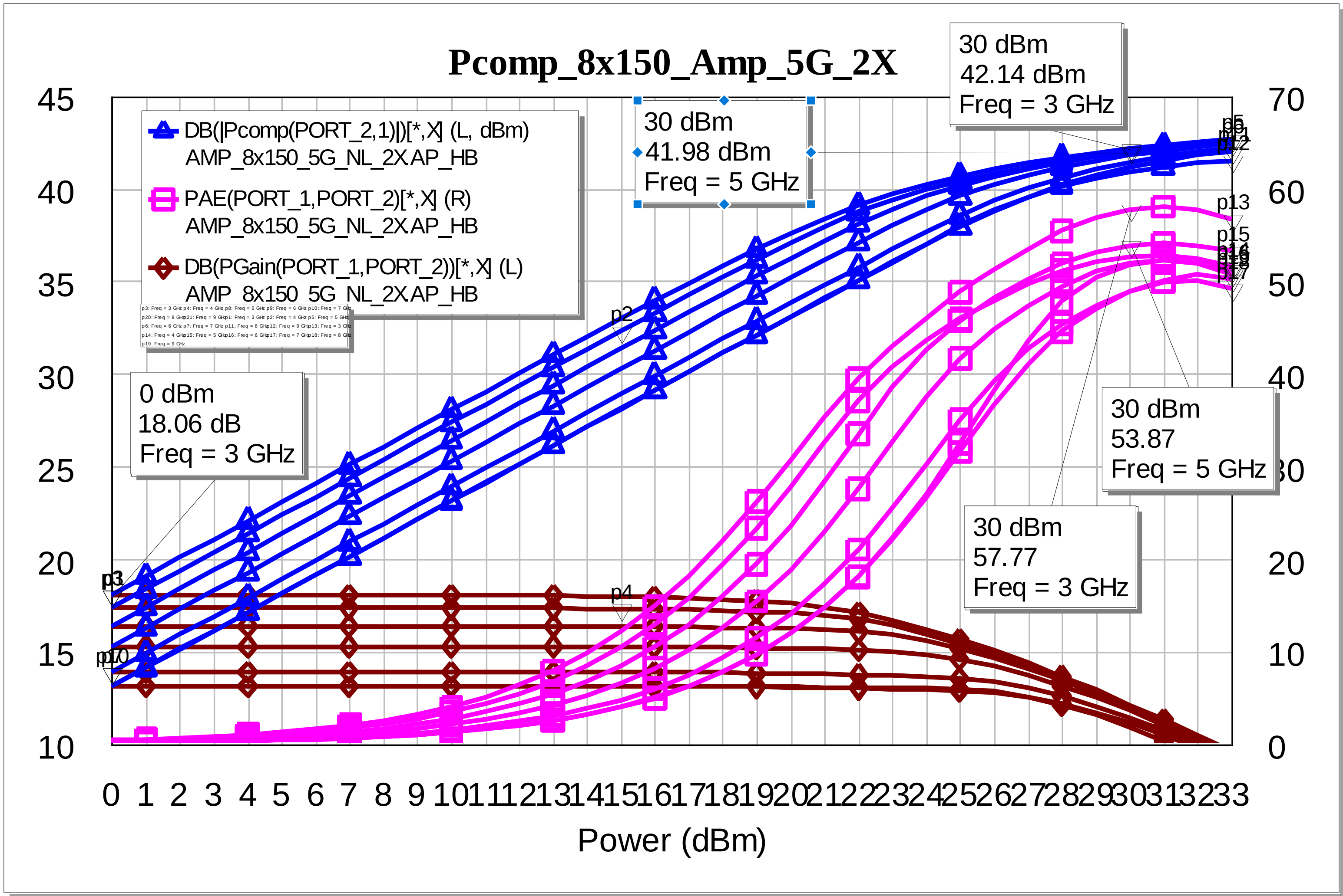

Fig. 19 Power and PAE of 2X 8- × 150-µm 10-W PA from 3 to 9 GHz, ideal lossless design

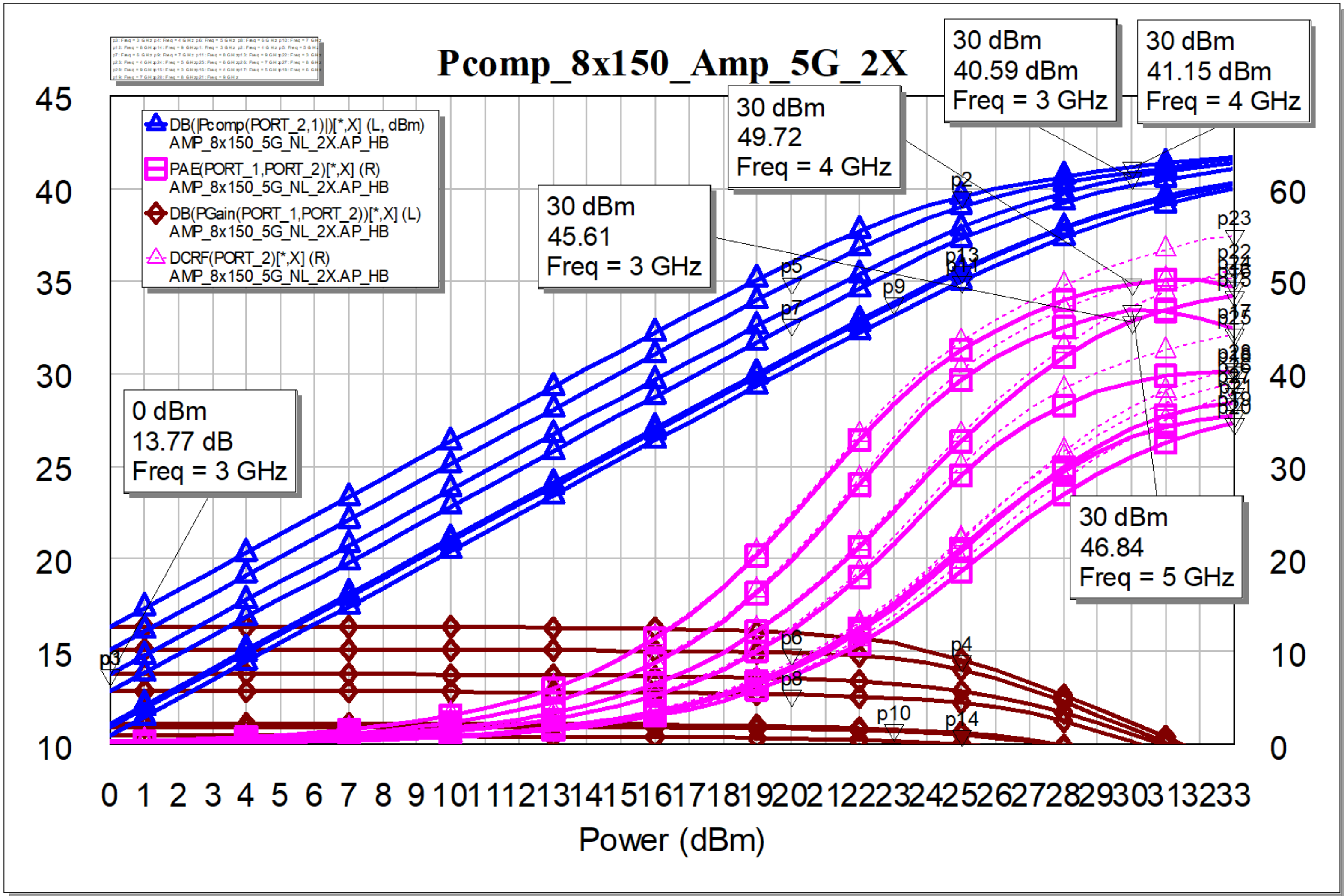

Fig. 20 Power and PAE of 2X 8- × 150-µm 10-W PA from 3 to 9 GHz, lossy MMIC PA

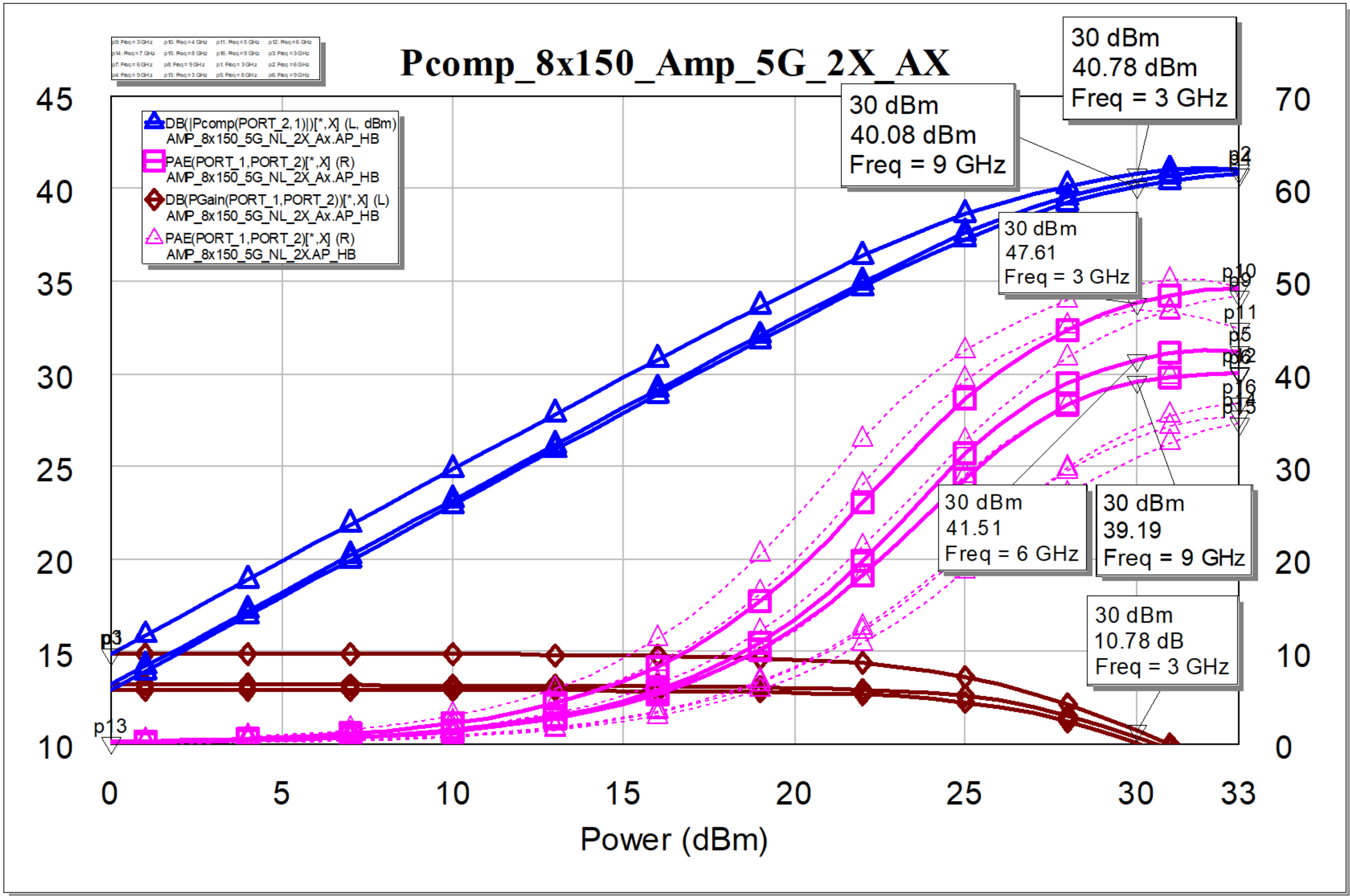

Fig. 21 **Power and PAE of 2X 8- × 150-µm 10-W PA from 3 to 9 GHz, final layout EM (28 V)**

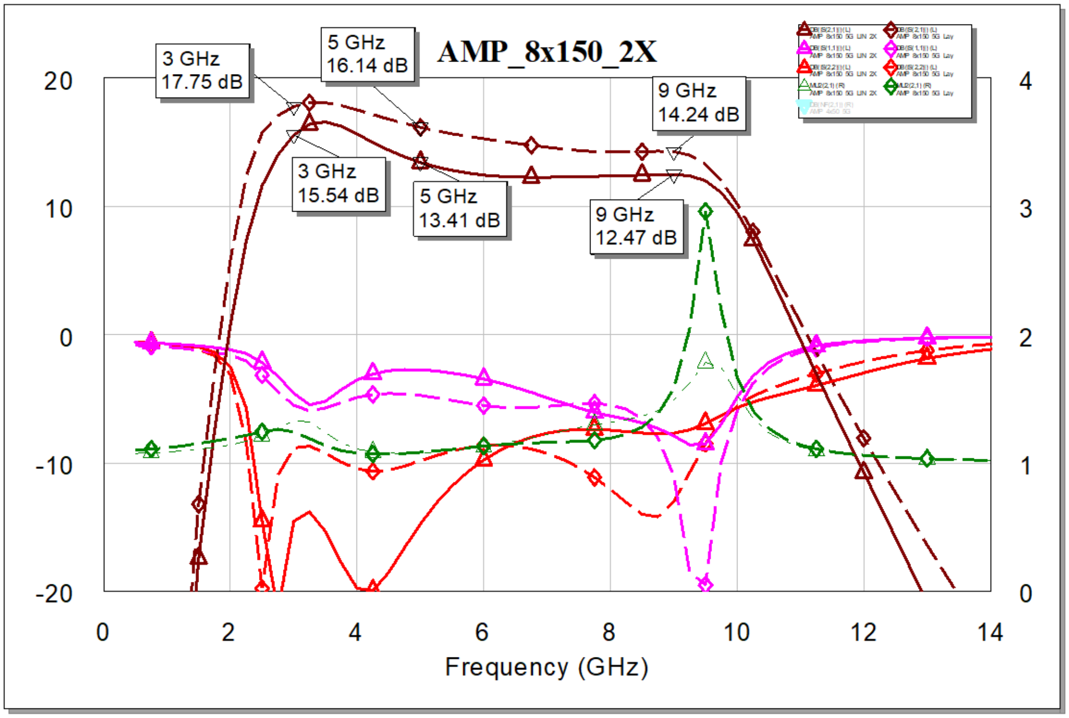

Fig. 22 S- to X-band 2X 8- × 150-µm 10-W PA linear simulations: 1X (dash) vs. 2X (solid)

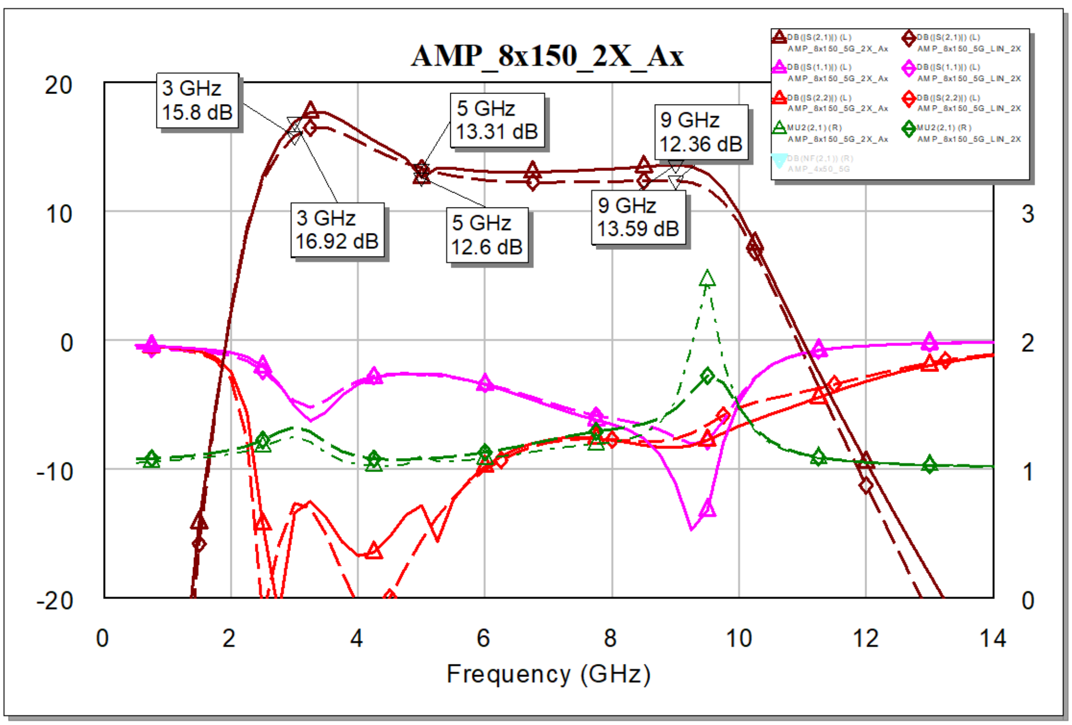

Fig. 23 S- to X-band 2X 8- × 150-µm 10-W PA simulations: MMIC (dash) vs. EM (solid)

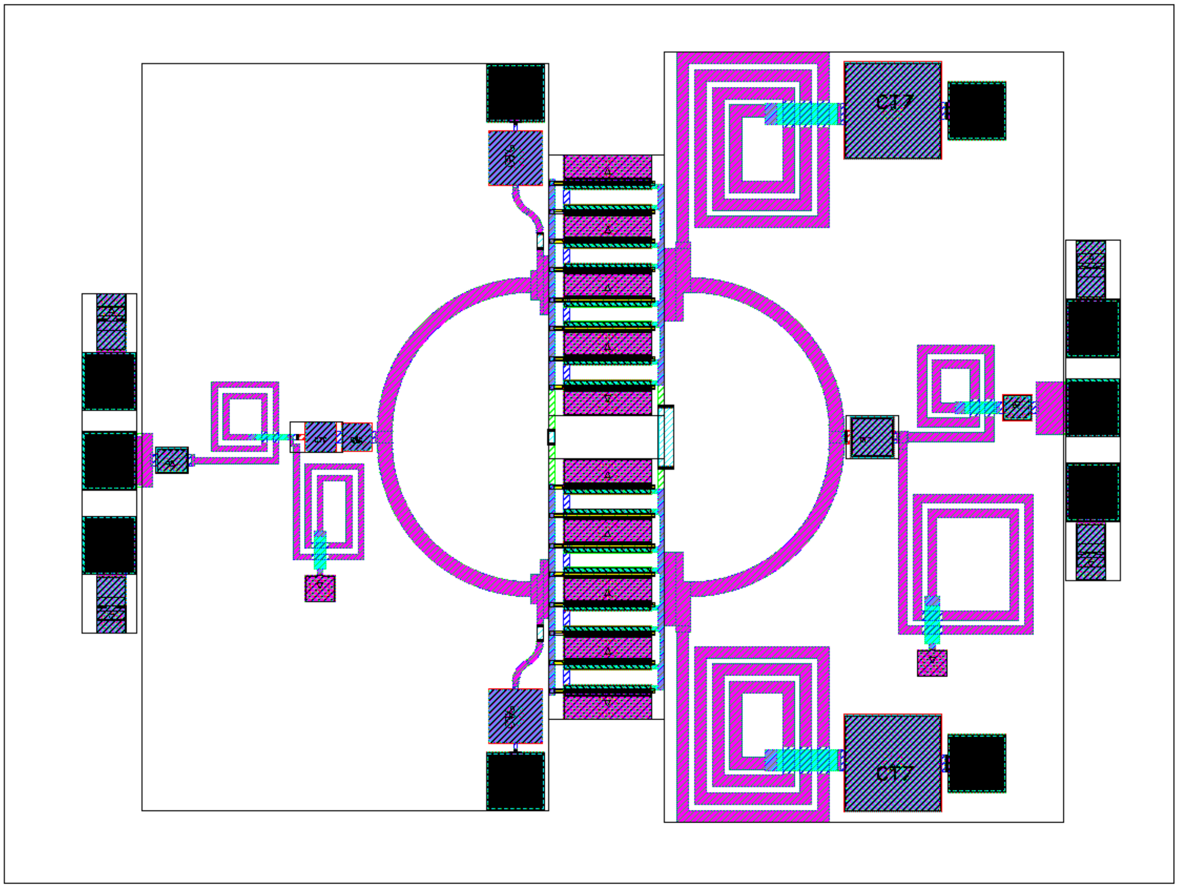

Fig. 24 Final compact layout of 2X 8- × 150-µm S- to X-band 10-W PA

5. Broadband Feedback Amplifiers

A simple approach to a broadband amplifier uses feedback, typically resistive feedback from drain to gate. Several broadband feedback amplifiers were designed in a prior Raytheon GaN process, demonstrating excellent noise figure as well as broadband gain. Using the two provided noise figure HEMT models for the Qorvo 0.15-µm GaN process, variations of a broadband feedback amplifier were designed. One amplifier uses a 6- × 50-µm HEMT with resistive feedback, and the other two designs use source inductance to create broadband LNAs. These small compact designs are intended to be biased through an external bias tee for the drain supply. Figure 25 shows the layouts of a 6- × 50-µm feedback amplifier using a series 450-ohm resistor and capacitor for the feedback path, plus a 4- × 50-µm and a 4- × 65-µm feedback amplifier that use source inductance. The 6- × 50-µm resistive feedback amplifier simulation shows 13.5-dB gain at 0.5 GHz rolling off to 10.1-dB gain at 7 GHz with a minimum noise figure of 1.5 dB increasing gradually to 2 dB at 7 GHz. Simulations of the 6- × 50-µm MMIC layout (solid) versus an ideal lossless amplifier are shown in Fig. 26. Next, the simulations of the 4- × 50-µm feedback amplifier show the MMIC element performance (solid) versus an ideal lossless design in Fig. 27. The 4- × 50-µm source feedback amplifier simulation shows 15.5-dB gain at 0.5 GHz rolling off to 10.5-dB gain at 7 GHz with a minimum noise figure of 1.1 dB increasing gradually to 1.25 dB at 7 GHz. The second source feedback amplifier using a slightly larger 4- × 65-µm HEMT provides higher low-frequency gain and slightly better noise figure. Simulations of the 4- × 65-µm feedback amplifier show the MMIC element performance (solid) versus an ideal lossless design in Fig. 28. The 4- × 65-µm source feedback amplifier simulation shows 17.3-dB gain at 0.5 GHz rolling off to 10.3-dB gain at 7 GHz with a minimum noise figure of 1.0 dB increasing gradually to 1.2 dB at 7 GHz.

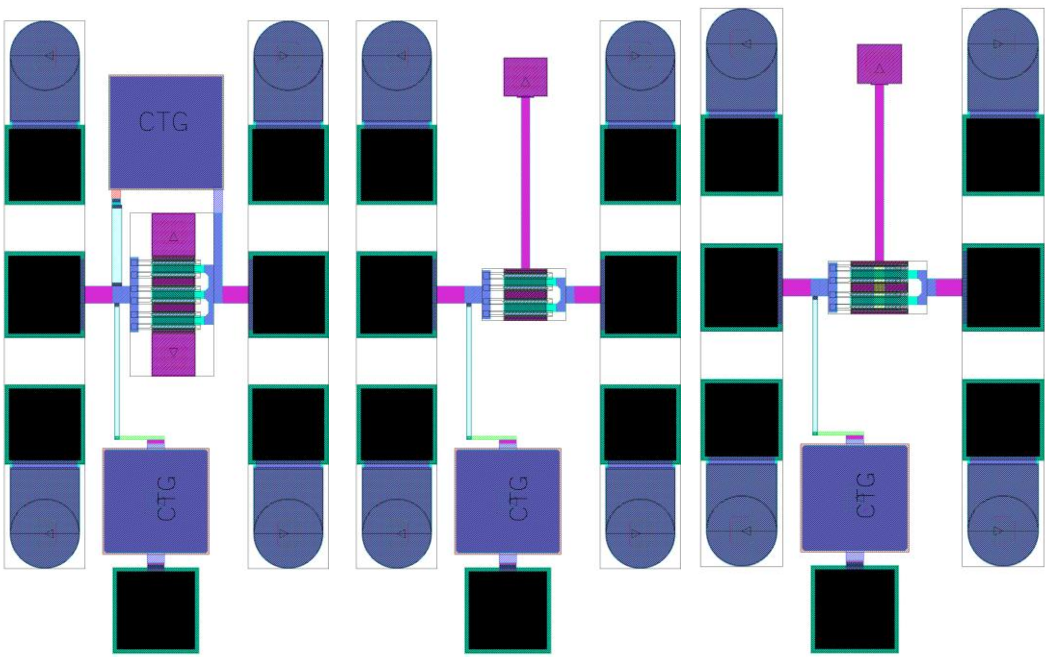

Fig. 25 Final compact layouts of broadband feedback amplifiers (6× 50 µm, 4× 50 µm, and 4× 65 µm)

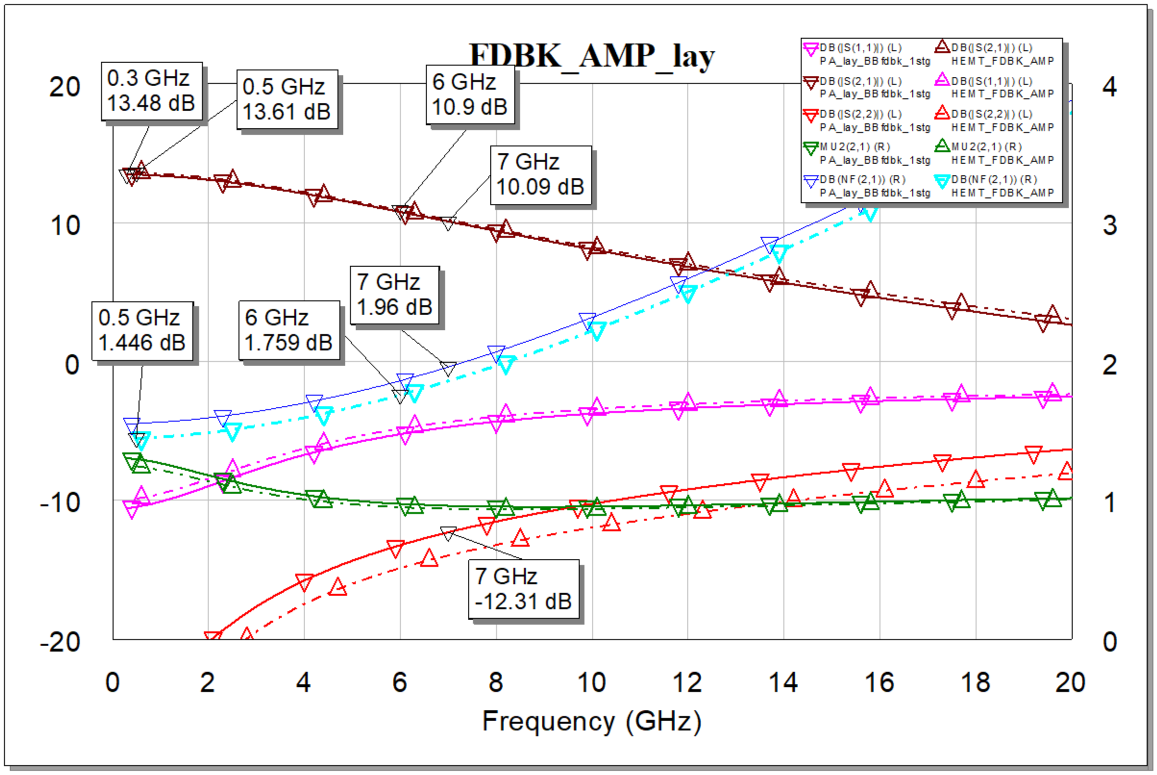

Fig. 26 **Simulation of 6- × 50-µm resistive feedback amplifier (MMIC [solid] vs. ideal [dot])**

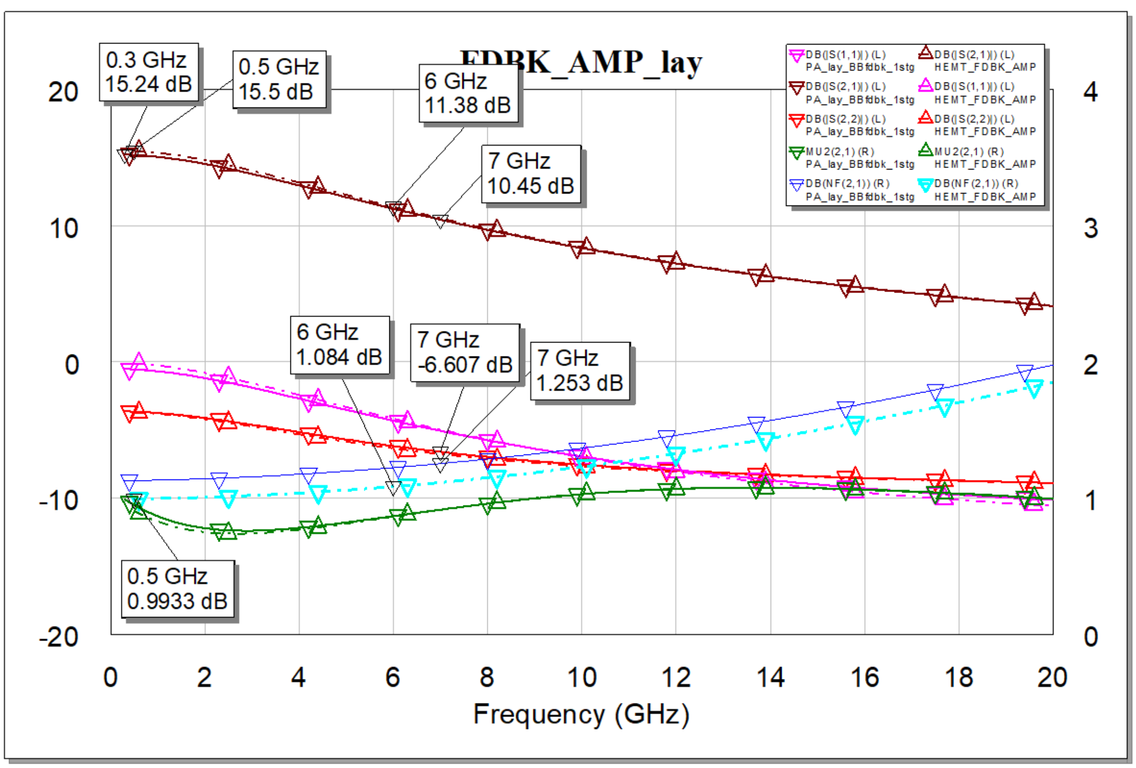

Fig. 27 **Simulation of 4- × 50-µm source feedback amplifier (MMIC [solid] vs. ideal [dot])**

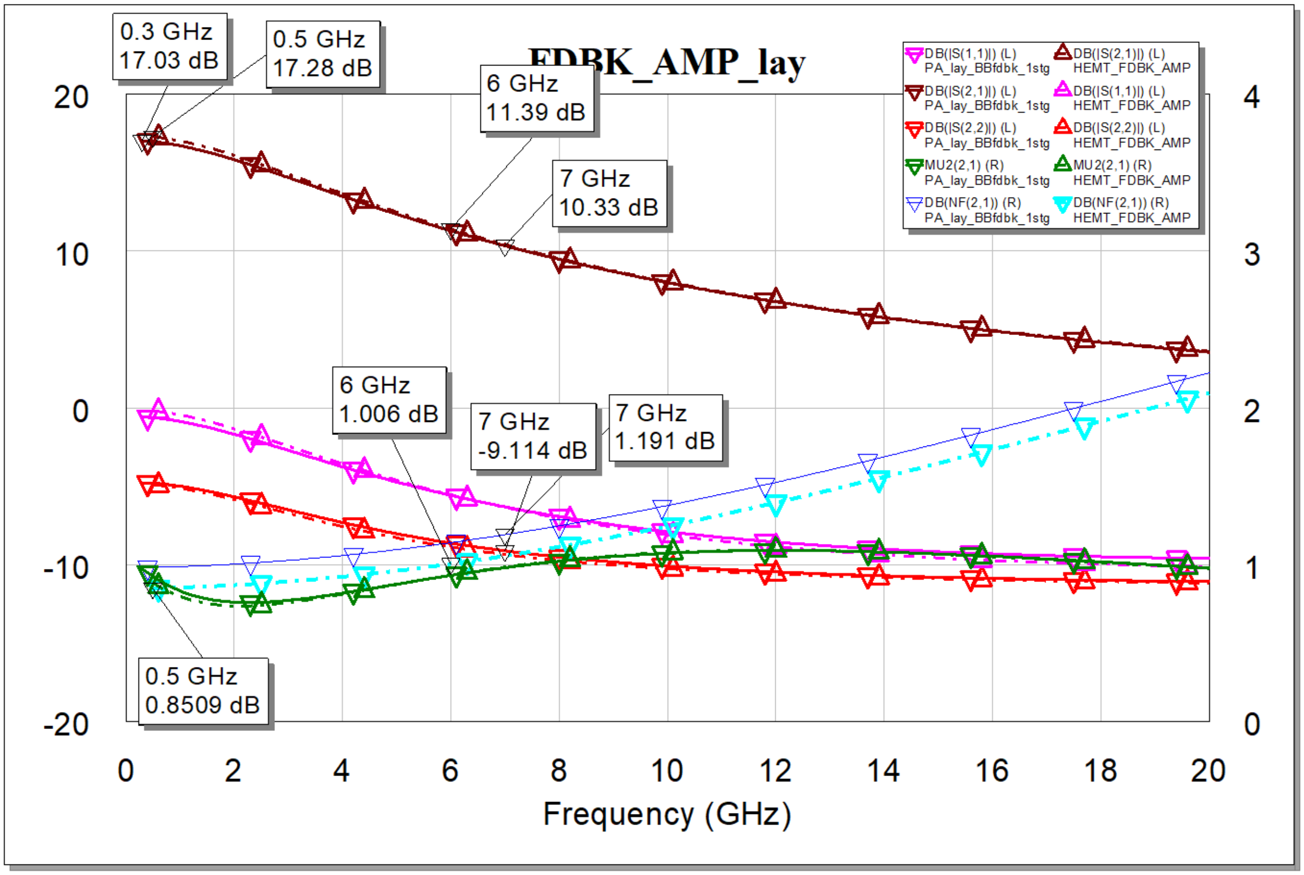

Fig. 28 Simulation of 4- × 65-µm source feedback amplifier (MMIC [solid] vs. ideal [dot])

6. Broadband Nonuniform Distributed Amplifier

Distributed amplifiers (DAs) provide very broadband gain and decades of bandwidth but are typically a compromise on performance when power efficiency or low noise figure is desired. Nonuniform DAs have been explored to achieve large bandwidth gain with better efficiencies for PAs. A nonuniform approach was explored, but with lower noise figure as the main objective. Using the 4-finger HEMT model with noise data, a simple uniform ideal DA was designed using 4- × 20-µm HEMT devices. Figure 29 shows the simple ideal schematic and Fig. 30 shows the preliminary simulation with good flat 10-dB gain to nearly 30 GHz. Note the stability problem near 40 GHz that needs to be addressed. The noise figure of the ideal DA is almost 2 dB at its minimum and is below 2.5 dB from about 8 to 26 GHz. This initial design was retuned, allowing varying HEMT sizes resulting in a better noise figure, below 2.5 dB from below 5 GHz up to 26 GHz with a minimum noise figure of 1.8 dB at 8 GHz (Fig. 31). Gain of this retuned DA is higher, and flat to 30 GHz, while stability is vastly improved. Once the ideal DA was converted to MMIC elements, EM-simulated, and re-tuned, the final EM simulations show a higher noise figure closer to 2.5-dB average over 6 to 26 GHz, with a minimum of 2.2 dB at 8 GHz. Gain is still good, close to 10 dB to 30 GHz. Figure 32 shows the EM simulation (solid) versus the original lossy MMIC element nonuniform DA simulation (dotted). The final layout is shown in Fig. 33 of the nonuniform distributed amplifier (NUDA). It should have very good gain bandwidth but the noise figure is higher than desired at lower frequencies, below 6 GHz.

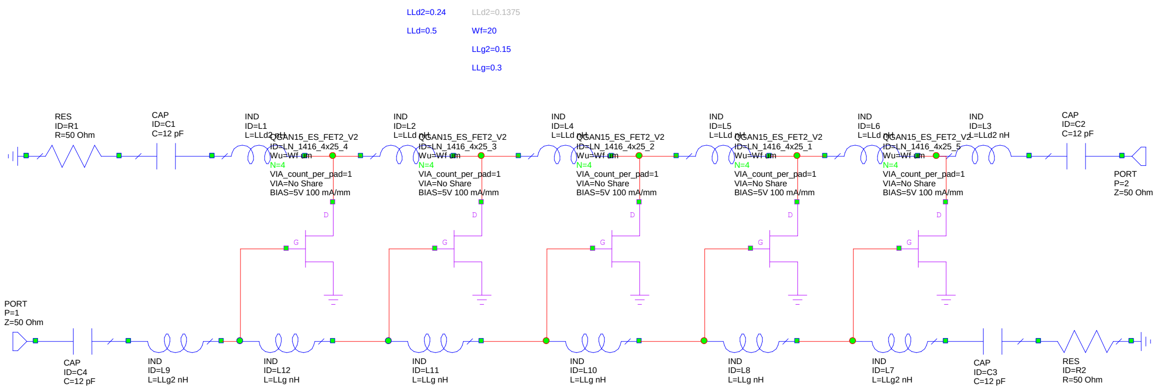

Fig. 29 Schematic of initial ideal uniform 4- × 20-µm DA

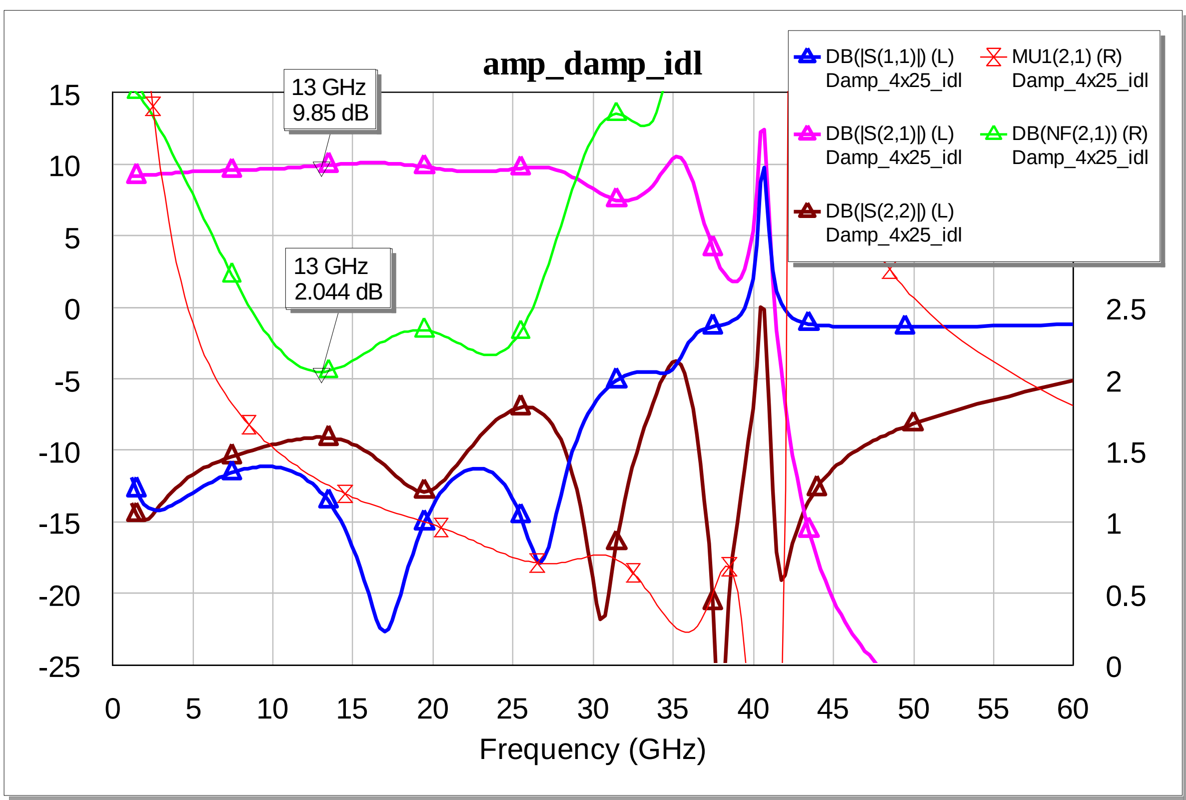

Fig. 30 Simulation of initial ideal uniform 4- × 20-µm DA

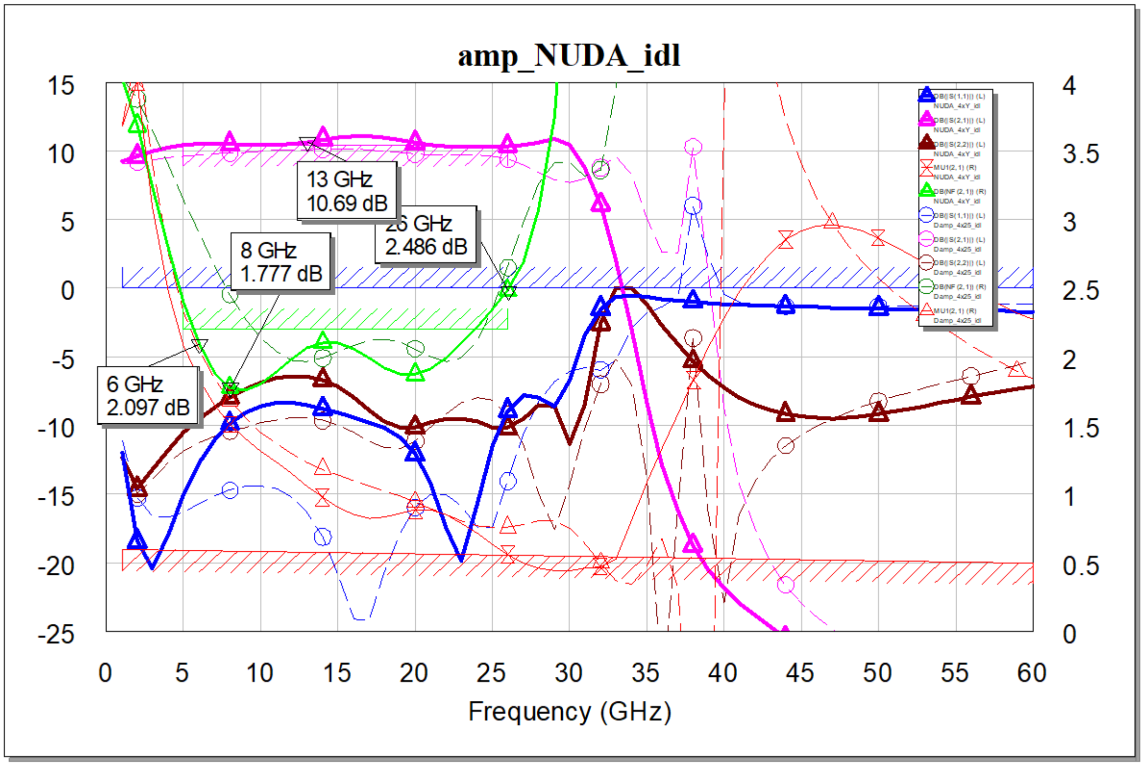

Fig. 31 Simulation of re-tuned ideal NUDA

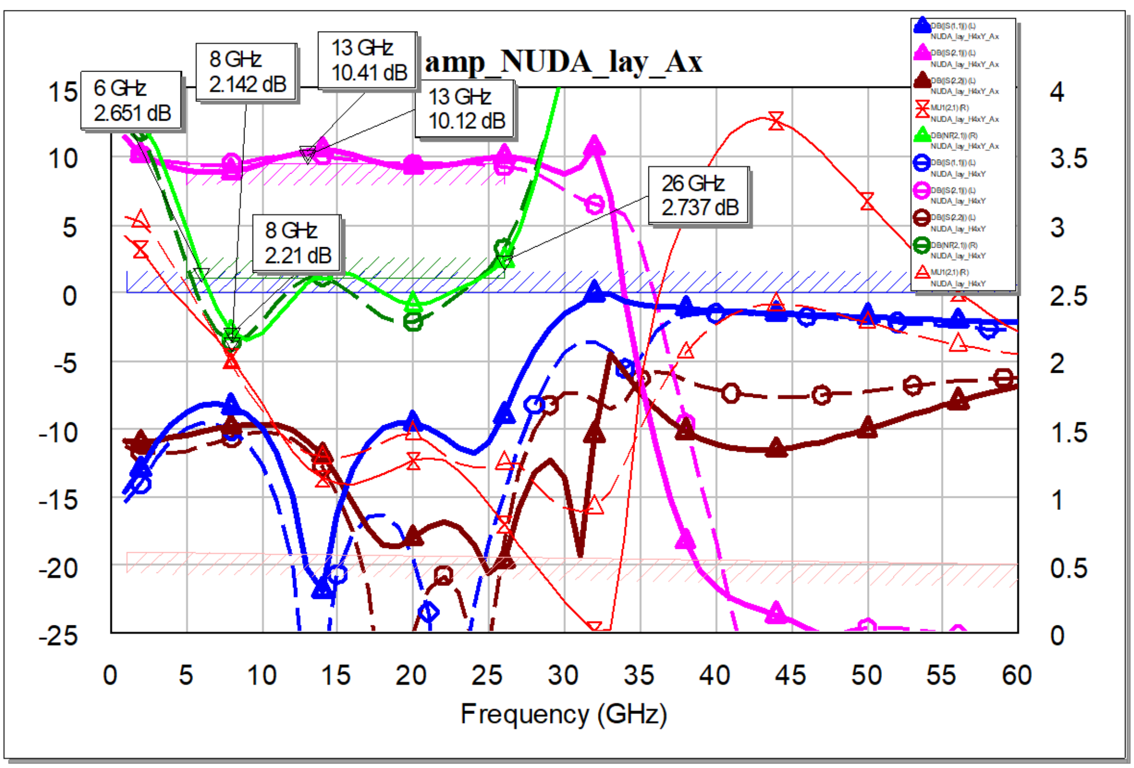

Fig. 32 EM simulation (solid) of nonuniform MMIC DA

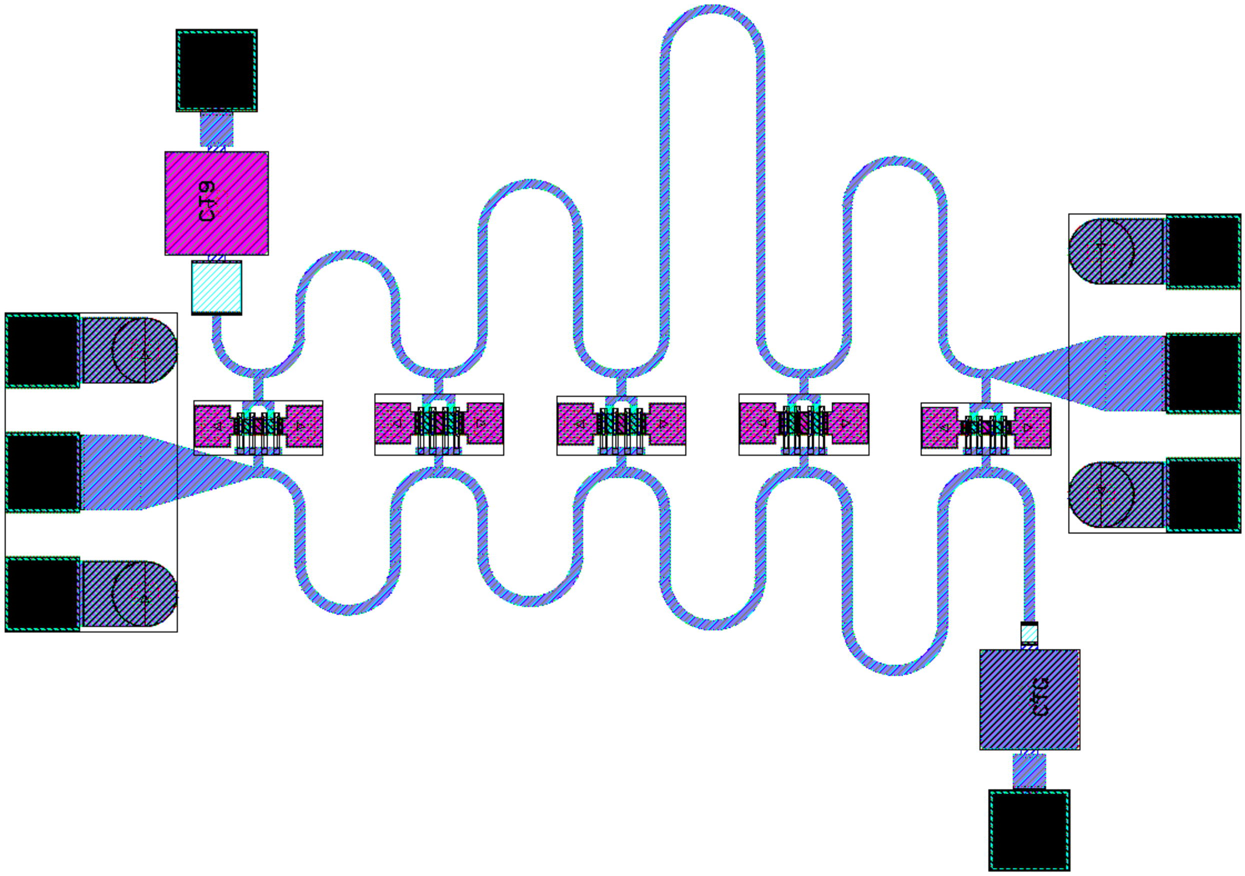

Fig. 33 Layout of NUDA

7. Conclusions

Multiple MMIC designs were submitted to an ARL Qorvo 0.15-µm GaN prototype wafer option to demonstrate the performance, bandwidth, capability, versatility, and applicability of GaN for compact, efficient microwave circuit designs—particularly for air and missile defense radars, but also applicable to EW, network communications, and efficient amplifiers for future radio and communications networks.

The designs described in this report are not the only designs in fabrication, nor the only MMIC designs targeted for radar applications. Those designers are expected to document these other designs in current and future reports. Some of the LNAs and PAs built upon prior work with Raytheon, which has a high-performance in-house GaN process. Future reports will document the testing and characterization of the designs that are expected to be fabricated and returned 3–4 months after commitment to the mask submission, which was completed in mid-September 2019.

The III/V design team has developed a full reticle of creative high-performance circuits that were submitted to fabrication in Qorvo’s 0.15-µm commercial GaN process.[2]

8. References

1. Penn JE, Darwish A. Broadband low noise gallium nitride (GaN) amplifiers for next-generation radars. Adelphi (MD): Adelphi (US); 2017 Nov. Report No.: ARL-TR-8208.

2. Penn J, Darwish A, Hawasli S, McKnight K, Hawasli S. Gallium nitride high-electron-mobility transistor (HEMT) monolithic microwave integrated circuit (MMIC) designs submitted for Qorvo prototype wafer option (PWO) fabrication. Adelphi (MD): CCDC Army Research Laboratory (US); 2019 Sep. Report No.: ARL-TR-8811.

List of Symbols, Abbreviations, and Acronyms

ARL	Army Research Laboratory
CCDC	US Army Combat Capabilities Development Command
DA	distributed amplifier
DC	direct current
EM	electromagnetic
EW	electronic warfare
GaN	gallium nitride
HEMT	high-electron mobility transistor
LNA	low-noise amplifier
MMIC	monolithic microwave integrated circuit
NUDA	nonuniform distributed amplifier
PA	power amplifier
PAE	power-added efficiency
PDK	process design kit
Q	quality factor

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