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Single Step Bonding of Thick Anodized Aluminum Oxide Templates to Silicon Wafers for Enhanced System-on-a-Chip Performance

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Abstract

Vertically-aligned nanowires are of interest for novel applications including sensing, photonics, and energy storage. Templated synthesis of such structures has been previously demonstrated via anodized aluminum oxide (AAO). However, the performance of AAO-on-Si devices has been limited by current methods of obtaining well-adhered, thick AAO templates on Si substrates. Thicker AAO templates allow for longer nanowires of active material, which is expected to increase performance of devices reliant on the surface area or volume of the active material. In this report, Al-Si eutectic bonding was used to achieve thick AAO-on-Si, with templates up to 90 μm thick bonded to the wafer. Carbon nanotubes (CNTs) were grown in the AAO templates bonded to Si to create proof-of-concept on-chip supercapacitor devices. Our devices show a promising value of 0.44 mF cm^{-2}, much higher than previous AAO-on-Si capacitors. The structure of the CNT/AAO/Si stack is examined using SEM and TEM, and the device

performance is tested through cyclic voltammetry (CV), electrochemical impedance spectroscopy (EIS), and galvanostatic charge-discharge (GCD) measurements.

Keywords

Anodized aluminum oxide; carbon nanotubes; ionic liquid; supercapacitor; system-on-a-chip

1. Introduction

Systems-on-a-chip (SOCs) are of great interest in remote sensing, with applications in structural health monitoring, gas sensing, and implantable biological sensing [1–3]. Ideal remote sensing SOC devices would be operable as-deployed over long periods of time without active maintenance such as battery replacement or manual data collection. These devices would require on-chip energy harvesting and storage in addition to their sensing and transmitting modules. Recently, a fully integrated SOC energy storing and harvesting module was demonstrated using thin-film microsupercapacitors (MSCs) integrated with on-chip transistors [4].

Anodized aluminum oxide [5] (AAO) is a hard nanotemplate that has been used to create vertically-aligned nanostructures for sensing, energy harvesting, and energy storage applications [2,6–10] making it a material of great interest for SOCs. AAO is an ordered array of cylindrical channels within an Al_xO_y matrix perpendicular to the Al substrate. The channels are open on the surface but the base of the pore has a thin oxide layer often referred to as the barrier oxide layer. Electrical contact to nanomaterials in the pores can be made by removing this barrier layer through either a modification to the anodization potential [11] or wet etching [12]. The performance of devices based on AAO is limited by the thickness of the AAO template [13]; thicker templates allow for greater volumes or surface areas of active materials per footprint area on the chip.

AAO has been integrated with Si in the past using two methods. In the first method, Al is deposited on Si through one of several vacuum deposition processes and subsequently anodized to form AAO directly on the wafer. Vacuum deposition processes are well-suited for thin-films, but deposition rates on the order of 1 nm s^{-1} greatly limit this approach for AAO applications requiring thick films such as high-performance SOCs [14–16]. Rabin et al. reported the thickest AAO from this method we are aware of, depositing 12 μm of Al to yield approximately 17 μm of AAO if the entire film were consumed [17]. However, the film thickness varied by as much as 50% across the wafer and delamination of the film after anodization was often observed. Delamination of vacuum-deposited Al films is a well-known issue in the field and has been addressed through both precise control of the anodizing process and by depositing additional adhesion layers between the Al and Si [17–19]. These methods allow for well-adhered AAO films on Si, but they do not address the issue of limited film thickness which limits overall device performance.

The second method of obtaining AAO on Si is the so-called template transfer process in which the AAO template is freed from the residual Al through chemical etching and subsequently attached to the Si [20–22]. In this method, the brittle AAO templates are prone to fracture, and the process is not favorable for large-scale production. Jang et al. [23] attempted to solve the problems associated with the brittleness of the templates by creating thicker than normal AAO, removing the underlying Al as normal, and using vacuum deposited gold as a bonding layer between the AAO and substrate. To our knowledge this is the only report of thick (>20 μm) AAO templates on Si which could be used for high performance SOCs. However, this technique relies on chemical etching steps to remove the residual Al from the AAO, vacuum

deposition of bonding materials and high pressure (5 MPa) heat treatments, and ion etching to remove the barrier layer, all of which are avoided in the present study.

In this work, eutectic bonding of Al and Si is demonstrated as a single-step method of bonding thick AAO films to Si wafers. Al-Si eutectics [24] are commonly used in contacting solar cells and older generation CMOS devices, and they have also been used as a braze material between Al surfaces [25–28]. Using these eutectics to produce thick (>20 μm) AAO templates on Si would enable a new generation of integrated SOCs due to the versatility of AAO as a nanotemplate. As proof of concept, 250 μm thick Al films were anodized to produce 55 μm thick AAO templates. The un-anodized Al films with the AAO template on top were then bonded to Si, and carbon nanotubes (CNTs) were deposited in the AAO via chemical vapor deposition (CVD). CNT filled templates were then used as electrodes in bulk scale pouch-cell type electrochemical double-layer capacitors (EDLCs) to study their applications for on-chip microsupercapacitors [29,30]. AAO-based electrochemical capacitors (EDLCs) have shown as much as 223 mF cm^{-2} under optimized conditions [31] but for on-chip applications, electrostatic metal-insulator-metal capacitors made using AAO-on-Si [32] have only reported values as high as 0.002 mF cm^{-2}. The AAO-on-Si devices in the present study show a promising capacitance of 0.44 mF cm^{-2}, much higher than previous AAO-on-Si capacitors.

2. **Methods**

2.1 Anodization

Unless otherwise stated, chemicals were obtained from Sigma-Aldrich and used as-received. Discs of Al (99.999%, Goodfellow) 2.5 cm in diameter were punched out of 250 μm thick sheeting. The pieces were degreased by sonication in soapy water, acetone, and ethanol. The Al was anodized via the two-step method [33] in 0.3 M oxalic acid at 15°C and 40 V. The first

anodization lasted for more than 16 h. The resulting disordered AAO layer was then removed through etching for 2 h in a 1.8% wt. chromic acid/6% wt. phosphoric acid solution heated to at least 60°C. The second anodization was carried out using the same conditions for 10 h to achieve a final AAO thickness of 55 μm, depicted in Fig. 1a. Longer anodization times were also used to create thicker AAO layers of 90 μm which were successfully bonded to Si. At the end of the second anodization, the voltage was dropped linearly to 0 V by 1 V s^{-1} to achieve barrier layer thinning at the AAO pore bottom. The Al discs were anodized in a custom built sample holder which kept the anodized area constant for all samples at a 1.9 cm diameter circle (2.85 cm^2).

SEM was performed on cross sections of a series of anodizations to determine the growth rate given in Eq. (1) below. Thickness in μm is given as *t* and charge passed in coulombs in the anodization is given as *Q*. Eq. (1) was used to determine the thickness of the template for pouch cell devices which were not directly imaged via SEM.

$$t = 0.134Q\,\frac{\mu m}{C} - 1.91\ \mu m \qquad (1)$$

2.2 Carbon Nanotube Deposition and AAO/Si Bonding Post-Anodization

The anodizations consume approximately 80 μm of Al in the 1st step and 40 μm in the 2nd step, leaving approximately 130 μm of Al to react in the eutectic bonding process. Si squares 2.5 cm × 2.5 cm were cleaved from 300 mm wafers. A hole was drilled through the Si using a modified drill press to allow for electrical connection to the Al current collector in capacitor devices. Before CVD, the Si was washed through sonication in acetone and ethanol. No pre-bonding etching was performed on the native oxide on the Al or Si. The anodized Al was bonded to the Si during the growth of the CNTs in the AAO pores shown in Fig. 1b. A homebuilt CVD chamber (2-inch diameter tube furnace, Lindberg Blue M from Thermo Scientific) was used to

deposit CNTs in the pores of the AAO by decomposing C_2H_2 (21 sccm) in Ar (284 sccm) and H_2 (10 sccm) at 650°C for 6 h. In order to keep the AAO/Al film from deforming and to maintain contact with the Si wafer, an Al_2O_3 washer of approximately 60 g was used to weigh down the AAO. The washer pressed only on the un-anodized rim of the AAO/Al film while leaving the AAO template open to the reaction gas during CNT growth. After CVD, the CNT/AAO/Si stacks were etched with Ar plasma using a Unaxis SLR RIE/ICP etch system. The plasma was generated at 90 W and the samples were etched for 2 min under 20 sccm Ar at 20 mTorr pressure with a power of 250 W. This etch step was important to remove the amorphous carbon film deposited on top of the AAO template during CVD and fully open the CNTs as seen in Fig. 1c.

2.3 Pouch Cell Supercapacitors

Symmetrical pouch cell devices were made using two CNT/AAO/Al/Si electrodes separated by glass fiber filter paper (0.7 μm pore size, 0.46 mm thick, MilliporeSigma) as in Fig. 1d. The electrodes were contacted from the backside and sealed along three sides in a Mylar pouch. The unsealed pouch was transferred to a vacuum oven and dried overnight at 50°C. The unsealed devices were then transferred to an Mbraun glovebox antechamber and held under pumping vacuum for more than 1 h to cool before being transferred into the Ar atmosphere. The separator was wetted with 0.5 mL of neat 1-ethyl-3-methylimidazolium tetrafluoroborate (EMIM-BF4, ≥99%) as the electrolyte. The hollow CNTs create very large and controllable surface areas that can be tuned by changing the pore size or pore length of the AAO via the anodization conditions.

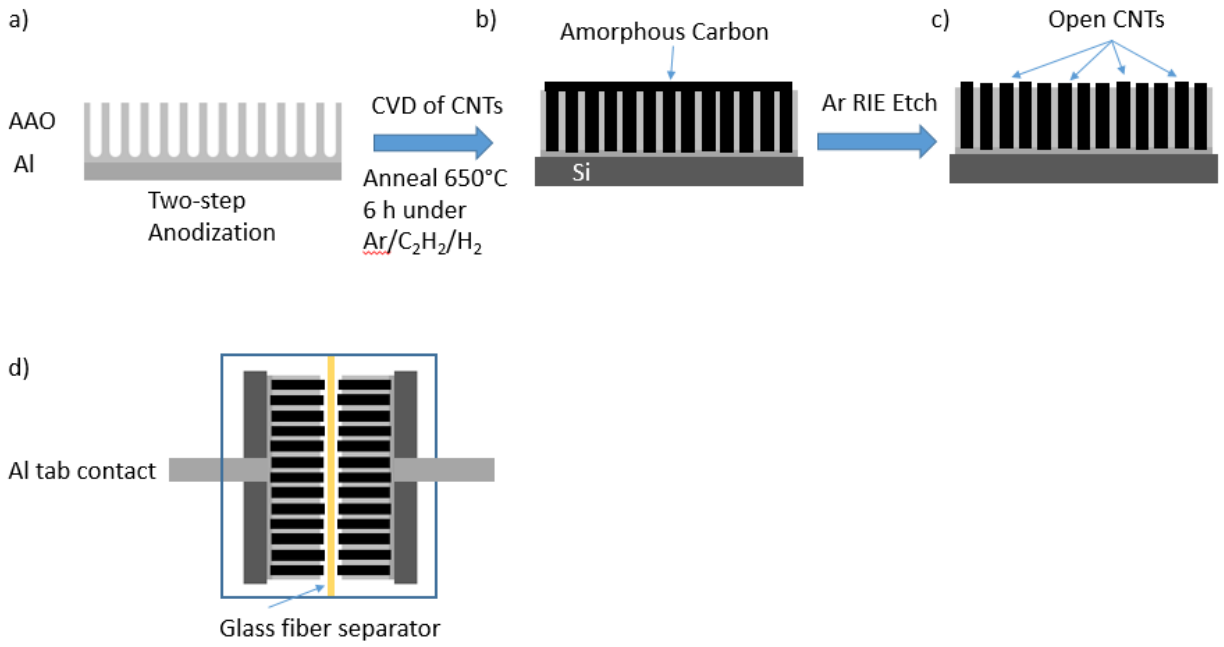

Fig. 1: Schematic showing the fabrication steps of a single CNT/AAO/Al/Si stack electrode including a) anodization, b) CVD, and c) RIE etching. d) The configuration of the pouch cell capacitor.

2.4 Electrochemical Testing

The devices were tested through cyclic voltammetry (CV), electrochemical impedance spectroscopy (EIS), and galvanostatic charge-discharge (GCD) in order to measure capacitance, internal resistance, and cycling stability. Impedance analysis and cyclic voltammetry testing was performed on a VersaSTAT 3 potentiostat (Princeton Applied Research) and cycle stability testing was performed using an Arbin BT-2000 battery cell testing station.

2.5 Structure Characterization

The microstructure of the AAO templates and structure of the CNTs were examined under SEM using a FEI Nova 430 FE-SEM. AAO/CNT composites and CNTs freed from the AAO template were examined using a FEI Tecnai F20 S/TEM. Plan-view TEM samples of the AAO/CNT composite were made from the cleaved cross-section using a FEI Helios Nanolab 600 Dualbeam FIB/SEM. SEM and TEM images were analyzed using ImageJ software.

3. Results and discussion

The effect of the 650°C bonding treatment/CVD process on the pore structure was first explored. Harsher heat treatments of 1200°C have been shown to decrease pore ordering and increase pore diameter which is unwanted for controllable device performance [34].

Fig. 2a shows the top view of a representative AAO film with no heat treatment. The average pore diameter, D_p, based on 512 pores is 51 ± 11 nm. The average interpore spacing, D_{int}, is 92 ± 19 nm giving an average wall thickness of 41 nm. The measured pore density is 9.9×10^9 cm^{-2}. These measurements are in the expected range for oxalic anodization at 40 V [35].

Fig. 2b shows the top surface of the AAO template which was bonded to the Si wafer after anodization. The bonding procedure was performed at 650°C for 6 h, the same as the CVD process used to deposit CNTs but in this case without flowing C_2H_2 or H_2. The pores are unchanged from the normally anodized sample, with an average D_p of 52 ± 8.5 nm over 2000 pores and an average D_{int} of 90 ± 14 nm, giving a resulting wall thickness of 38 nm. These measurements are well within the measurement error of the non-heat-treated AAO indicating none or minimal pore widening.

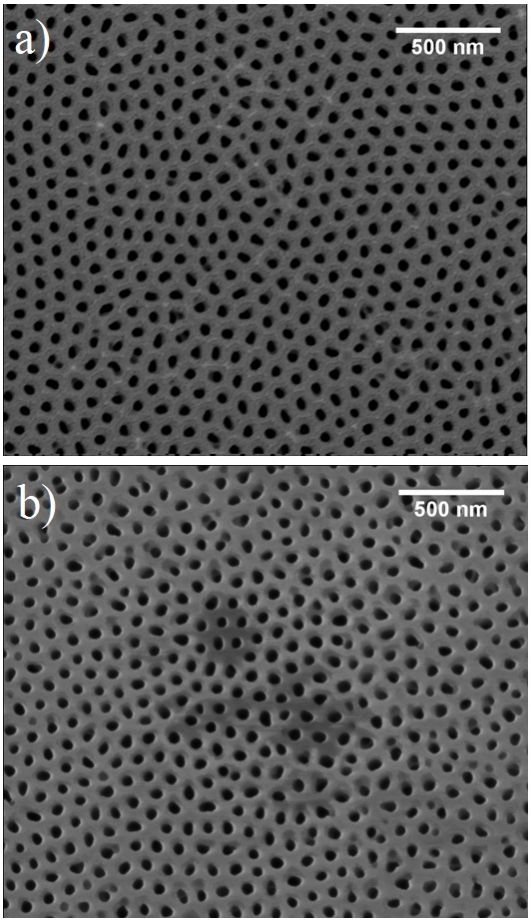

Fig. 2: Top-down view of the AAO pores a) as-prepared and b) after bonding to Si at 650°C for 6 h under flowing Ar.

The structure of the composite AAO/Al/Si stack after bonding for 6 h at 650°C under Ar is shown in Fig. 3a. This sample was anodized for 24 h and did not undergo any barrier layer thinning techniques. The result is a 90 μm thick AAO template, the thickest ever AAO reported on a Si wafer to our knowledge. The composite sample was cleaved to view the cross section, and the ductile Al is easily distinguishable between the brittle AAO and Si layers. Fig. 3b shows that the interior of the pore structure is unaffected by the heat treatment. Pores are straight with no aberrations. At the base of the pore is the barrier oxide layer, shown in Fig. 3c, which prevents electrical contact between the Al current collector and any materials deposited in the

AAO pores. The barrier oxide is unaffected by the bonding process and must be dealt with in other ways such as the anodization modification used for our pouch cell EDLCs.

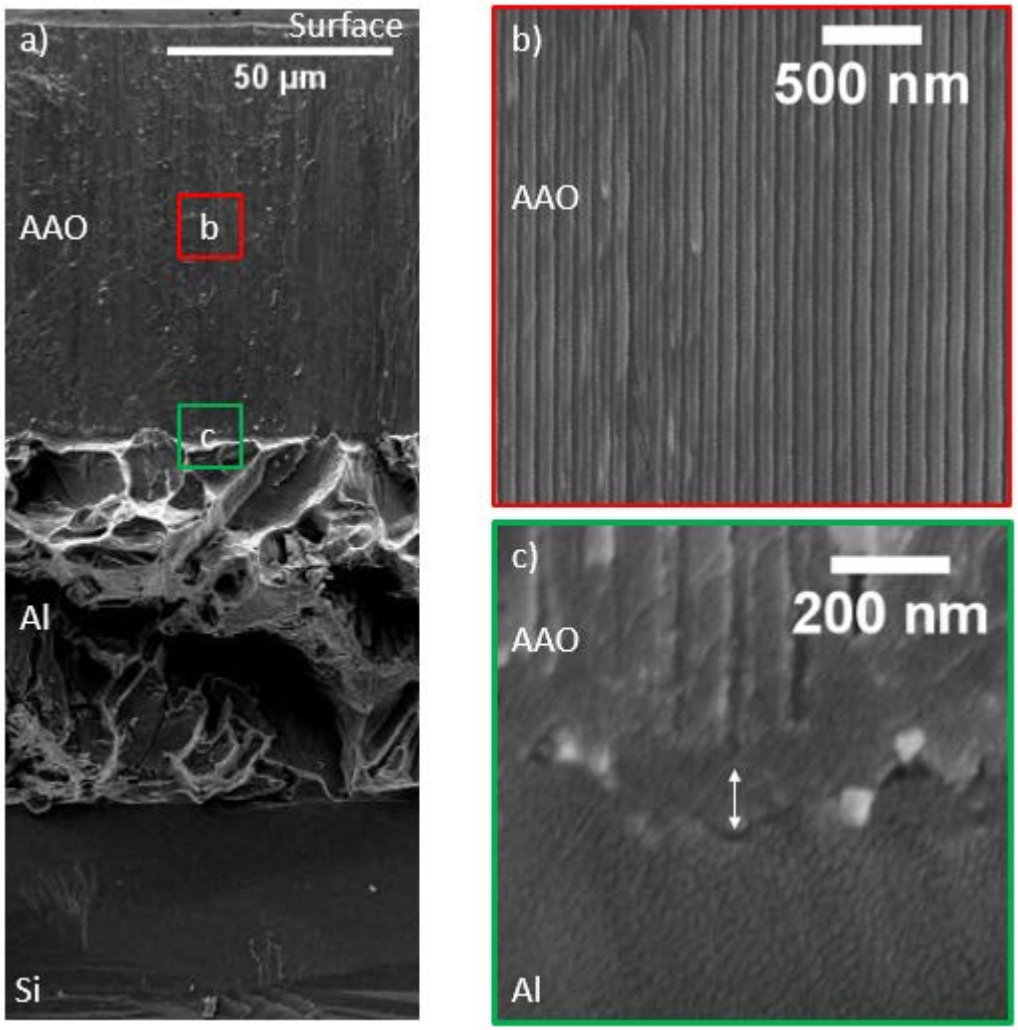

Fig. 3: a) Cross section of the bonded stack showing AAO (top), Al (middle), and Si (bottom). Areas of interest are outlined and shown in higher magnification, demonstrating b) that the pore wall structure of the AAO is maintained after bonding and c) that the barrier oxide, highlighted with white arrow, is intact.

Fig. 4 shows the interface between the Al and Si layers after annealing at 650°C for 6 h under Ar flow. There are three common microstructural features seen at the interface. In Fig. 4a, Si is shown redepositing at the interface forming Si islands similar to those seen in Al metallized contact holes in integrated circuits [36]. Due to the low solubility limit of Si in Al, slow cooling of the bonded structure can easily precipitate Si from the eutectic composition of 12.2% at. to the

solid solubility limit of <1.2% at. at room temperature. Faster cooling rates can decrease the size of precipitates and could be explored to eliminate these plateaus [37]. Fig. 4a also shows large, hemispherical pits into the Si. These pits are the result of the liquid eutectic reaction between Al and Si and are commonly seen in Al contacted solar cells annealed above the eutectic point [25,38]. Since the Al and Si used in this study was extremely pure, there are large concentration gradients for interdiffusion of Si and Al. However, the diffusion of Si is much faster into Al than vice versa, and this mismatch of diffusion coefficients (a.k.a. the Kirkendall effect) is thought to exacerbate the eutectic pitting seen in Fig. 4a. Therefore, the use of anodized AlSi alloys is being investigated to reduce the interdiffusion and eliminate such pitting. AlSi alloys have been used in the semiconductor industry at approximately 0.7% Si to combat similar pitting defects, and anodization of similar purity alloys has been shown to have minimal effect on the AAO structure [27,39].

In Fig. 4b, a different microstructure is seen (note the difference in scale bars). The bonding interface is much more planar compared to Fig. 4a and there are small voids on the Al side of the interface. Voids may have been caused by mass transport during the bonding process, and the roughness of the rolled Al used in this study could also play a role in forming this structure. Roughness values obtained from profilometry are on the order of R_a ~ 100 nm for the Al, which is similar to the height of the voids seen in Fig. 4b. Due to this roughness, the Al and Si may not have been in as intimate contact as other regions leading to void formation. Overall, the Al film showed excellent bonding characteristics using this process, with no signs of delaminated regions and high structural integrity.

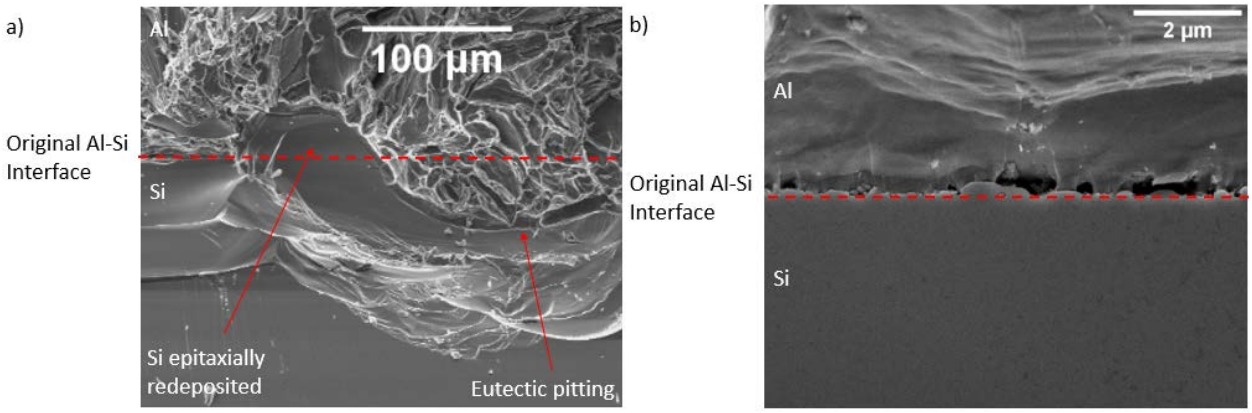

Fig. 4: Resulting Al-Si interface after annealing at 650°C for 6 h. Dashed red line indicates the proposed original position of the interface. At lower magnifications a), islands of epitaxially regrown Si and Al-Si eutectic pits are seen along the interface. Higher magnification of some regions b) show the presence of voids which are believed to be caused by surface roughness of the Al leading to non-intimate contact during bonding, but which may also be the result of mass transfer during the bonding process.

CNTs were grown inside the AAO by decomposition of C_2H_2 mixed with H_2 and Ar in a CVD tube furnace. Fig. 5 shows the resulting nanostructure from the single-step CNT CVD and Al-Si eutectic bonding. Fig. 5a shows the top view of the AAO template filled with CNTs after an ICP-RIE etching step. The nanotubes are conformally grown in the template with an average pore diameter after growth of $D_p = 33 \pm 13$ nm. With an initial D_p of 51 nm, the CNT wall thickness is determined to be 9 nm. Fig. 5b shows a cross section of the midpoint of the AAO template with CNTs inside. This is evidence that CNTs grow throughout the length of the entire template. Some tubes were pulled out of the template when it was fractured for SEM analysis, but the top view indicates that all AAO pores are lined with CNTs. Fig. 5c shows plan-view TEM of the CNTs within the AAO template. The inner wall of the AAO is clearly delineated as a sharp hexagon of relatively pure alumina [40]. Some texture can be observed within the CNTs. During the CVD growth of CNTs in AAO, both graphitic and amorphous carbon are known to be deposited [41]. The texture on the inner tube could then be some overgrown amorphous material. Fig. 5d shows TEM of CNTs freed from the AAO template. Some amorphous material is clearly clinging to the outside of the tubes. TEM images were used to corroborate the CNT

wall thickness obtained from SEM. 10 measurements each of 15 distinct CNTs gave an average wall thickness of 9.4 ± 2.8 nm, in good agreement with the SEM analysis. The agreement between SEM and TEM analysis also indicates that tubes are formed along the entire AAO pore and do not taper in either direction.

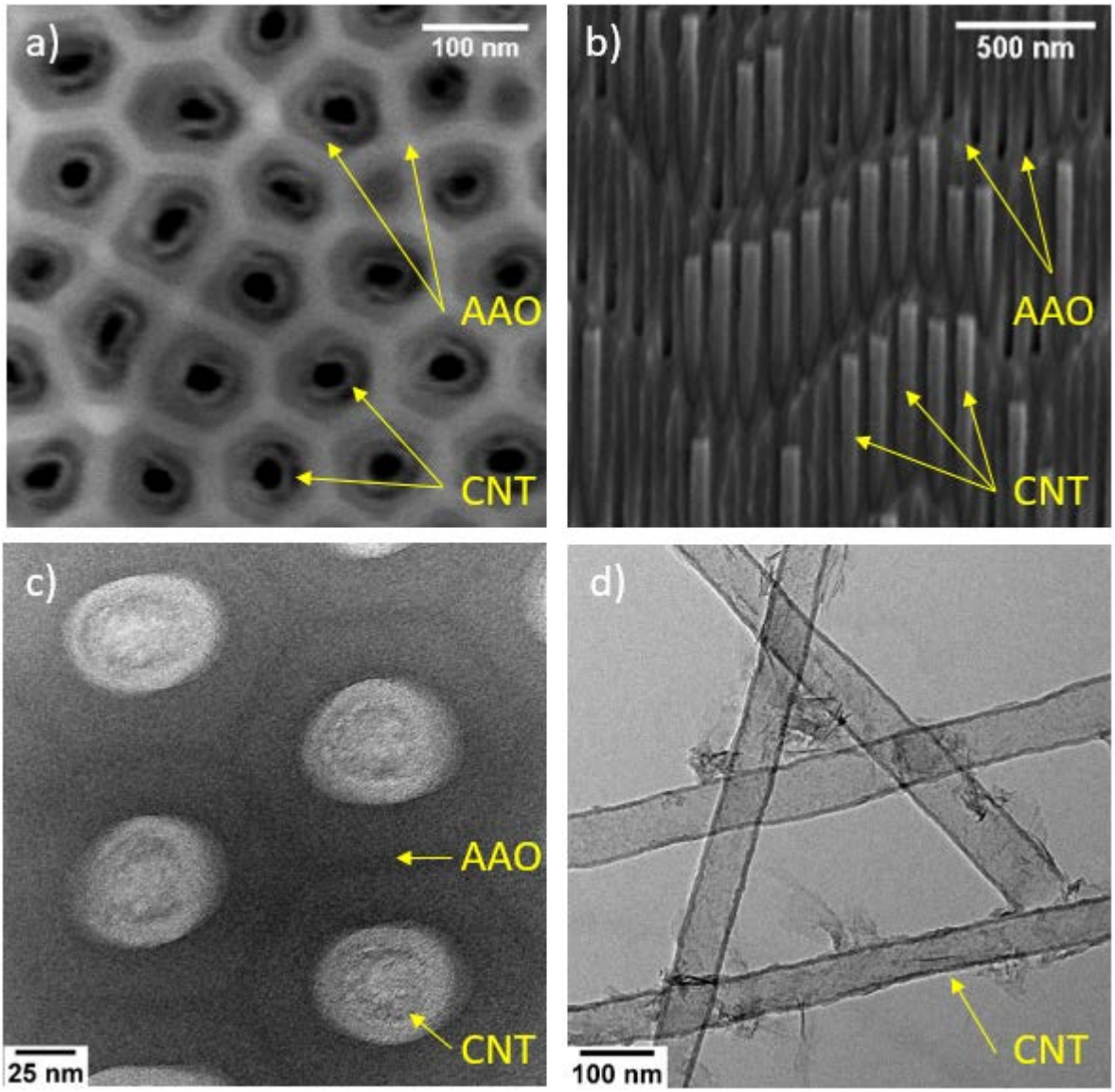

Fig. 5: SEM images of CNTs deposited in the pores of AAO in a) top down view and b) side view. TEM of CNTs c) in AAO pores and d) freed from the AAO template.

Pouch cell performance was measured through CV, GCD, and EIS. Using the anodization data and Eq. (1), the thickness of the AAO in the cells was determined to be 55 μm. Fig. 6 shows the

Nyquist plot of the EIS scans for the device. The ohmic resistance taken as the high-frequency limit of the real part of the impedance is 5.4 Ω cm^2 showing that there is good electrical connection to the CNTs and the barrier layer has been effectively dealt with. The slope of the impedance at low frequencies should be vertical (90°) for a purely capacitive response [42]. The pouch cell gives a phase of 83° over the frequency window 1 – 0.1 Hz indicating near ideal capacitive behavior. Higher frequency regions above 40 Hz show a phase angle close to 45° which is expected due to the ordered porous structure of the electrode [43].

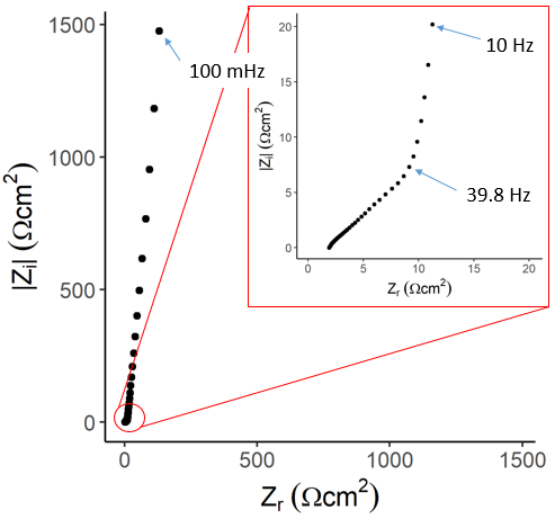

Fig. 6: Nyquist plot of the pouch cell device from 100 kHz to 100 mHz. Inset highlights the high frequency region from 100 kHz to 10 Hz with a knee frequency at 39.8 Hz.

Fig. 7 shows the CV response of the 55 µm thick AAO cell. The CV curve shows no peaks or valleys related to redox reactions [44]. The shape is nearly rectangular, ideal for such an EDLC device, and the current transient at the switching potential is sharp. Specific capacitance was calculated using Eq. (2) below.

$$C = \frac{\int_{V1}^{V2} di\, dV}{Av\Delta V} \qquad (2)$$

Where $\int di\ dV$ is the integrated current with respect to voltage, V_1 and V_2 are the switching voltages in the CV scan, A is the footprint area, v is the sweep rate, and ΔV is the voltage window. The capacitance calculated from the CV curves is shown in Fig. 7b, decreasing from 0.44 mF cm^{-2} at 10 mV s^{-1} to 0.36 mF cm^{-2} at 500 mV s^{-1}. The capacitance decreased only 18% over more than an order of magnitude change in sweep rate, indicating that similar devices are suitable for the high power, short duration pulses which may be expected for SOC charging.

Based on the density of the pores and the thickness of the CNT wall, the surface area of the CNTs per Si footprint is calculated to be 613 cm^2 cm^{-2}. Normalizing the total capacitance measured with CV (1.26 mF) to the internal area of the CNTs gives a value of 0.73 ± 0.29 μF cm^{-2}. Error bars were determined through propagation of error [45] in pore size, template length, potentiostat sensitivity, etc. Literature values of activated carbon in neat ionic liquid [46] and simulations of single walled carbon nanotubes in ionic liquid [47] report values of 1-2 μF cm^{-2}. Our value of specific capacitance is then very reasonable on the high end, but ranges fairly low. It is possible that the ionic liquid did not fully wet the interior of CNTs which would decrease the active surface area and lead to a decreased values of the calculated specific capacitance.

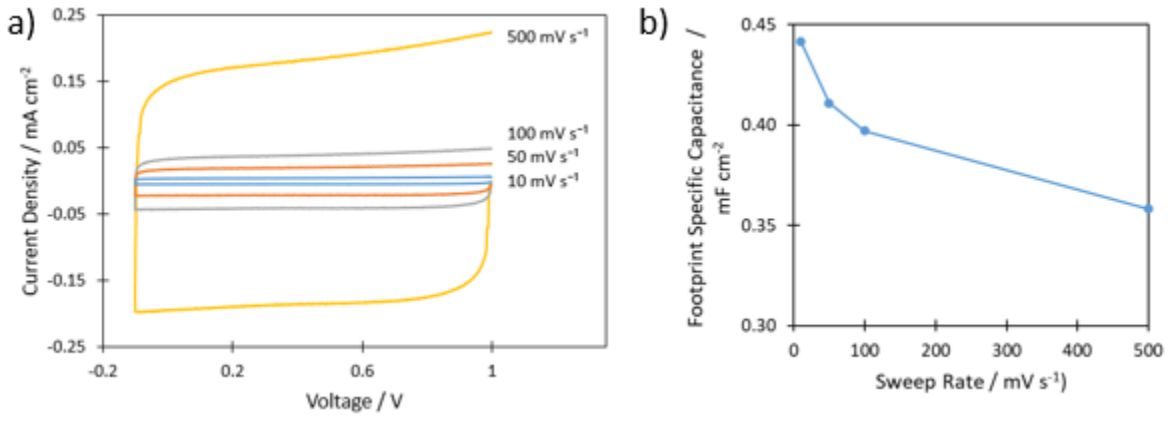

Fig. 7: a) CV response at sweep rates between 10 and 500 mV s^{-1} and b) corresponding capacitance of the pouch cell device.

Fig. 8a shows the GCD measurements for the cell cycled 1000 times at 17.5 μA cm^{-2} and another 1000 times at 1.75 μA cm^{-2} between -0.1 and 1.0 V. The 55 μm cell suffered minimal fade in discharge energy over the first 1000 cycles at 17.5 μA cm^{-2}, falling by just 1%. The fade was slightly more drastic at lower charge rates, falling by 10% of the first cycle after all 2000 cycles. The charging efficiency given in Fig. 8b was much better for the higher charge rate, with an average of 87% compared to an average of 69% efficiency for the 1.75 μA cm^{-2} rate. The decreased efficiency at lower charge rates, combined with the greater fade, may indicate that some impurities either on the electrode surface or in the electrolyte were consumed during cycling. The GCD results indicate that thick AAO films are suitable for the large current transients which might be expected from intermittent energy harvesting sources on self sustaining SOCs [4].

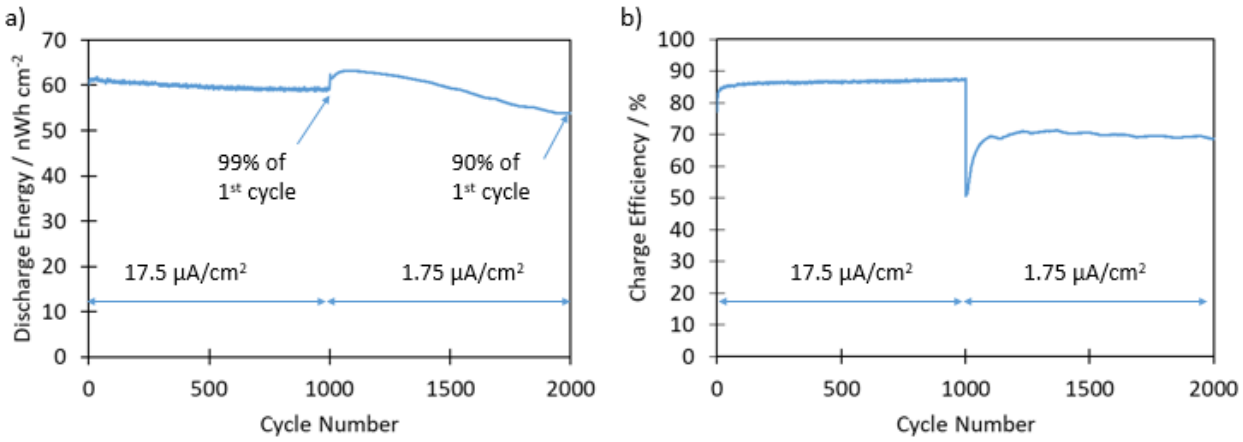

Fig. 8: GCD of the pouch cell device of 1000 cycles each at 17.5 and 1.75 μA cm^{-2}. a) Discharge energy from 1 to -0.1 V and b) charging efficiency based on charge and discharge energy.

Conclusions

Thick AAO templates were bonded to Si wafers using a simple single step eutectic bonding method which had no impact on the AAO structure. The bonding interface between the Si and Al displays some defects including Si islands, eutectic pits, and void content, but the

AAO/Al/Si stack is physically robust with the AAO firmly attached to the Si. Importantly, electrical connection can be made to materials deposited in the AAO pores via the underlying Al. CNTs deposited in bonded AAO templates were used to create pouch cell EDLCs with a capacitance as high as 0.44 mF cm^{-2}, more than two orders of magnitude higher than previously reported AAO-on-Si capacitors. This eutectic bonding approach to creating very thick AAO films on Si can drastically increase the active loading of vertically-aligned 1-D nanostructures and opens the door for enhanced performance in SOC devices.

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14. ABSTRACT

Vertically-aligned nanowires are of interest for novel applications including sensing, photonics, and energy storage. Templated synthesis of such structures has been previously demonstrated via anodized aluminum oxide (AAO). However, the performance of AAO-on-Si devices has been limited by current methods of obtaining well-adhered, thick AAO templates on Si substrates. Thicker AAO templates allow for longer nanowires of active material, which is expected to increase performance of devices reliant on the surface area or volume of the active material. In this report, Al-Si eutectic bonding was used to achieve thick AAO-on-Si, with templates up to 90 μm thick bonded to the wafer. Carbon nanotubes (CNTs) were grown in the AAO templates bonded to Si to create proof-of-concept on-chip supercapacitor devices. Our devices show a promising value of 0.44 mF cm-2, much higher than previous AAO-on-Si capacitors. The structure of the CNT/AAO/Si stack is examined using SEM and TEM, and the device performance is tested through cyclic voltammetry (CV), electrochemical impedance spectroscopy (EIS), and galvanostatic charge-discharge (GCD) measurements.

15. SUBJECT TERMS
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