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**32NM HAFNIUM (IV) DIOXIDE (HFO₂) NEGATIVE METAL OXIDE
SEMICONDUCTOR (NMOS) ELECTRICALLY ERASABLE
PROGRAMMABLE READ-ONLY MEMORIES (EEPROMS) FOR
OPEN SYSTEMS COMPUTER APPLIANCES**

OKLAHOMA STATE UNIVERSITY

FEBRUARY 2020

FINAL TECHNICAL REPORT

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14. ABSTRACT The research objectives of this work are improvements to stress arrays of low threshold HfO2/SiOx N-CMOS architectures. Many of these designs are currently employed in advanced computer architectures that have secure capabilities for the Air Force Research Laboratory (AFRL) in Rome, NY. This will be accomplished by creating a complete design flow integration with commercial and open-source Electronic Design Automation (EDA) tools. Designs will then be formalized as EEPROM bank cell intellectual property. The acceleration parameter is then combined with time dependent breakdown models resulting in device lifetime models for both write and erase as a function of applied gate voltage. This results in write and erase protocols as a function. Results demonstrate successful research that utilizes the CMOS SOI32 EEPROM test structures submitted with USAFAFMC AFRL/RITA to develop Stochastic based write-erase models and other yield-associated results.					
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1.0 SUMMARY

At the present time, all computer appliances are vulnerable to attack from both in-house and outside intruders. Of particular interest are open systems including cloud, remote, or local serve platforms, smart phone networks, and networks in general. Encryption used to protect the basic input/output system (BIOS), bootloader, operating systems, and private user keys etc. can only successfully address these concerns if they are NOT observable and encryption is secure and observed in their encrypted form. In core, on-chip electrically erasable programmable read-only memories (EEPROMs) created utilizing standard complementary metal-oxide semiconductor (CMOS) technology is an integral part of the Central Processing Unit (CPU) integrated circuit (IC). Placing EEPROM banks on chip as an integral or embedded function within the IC eliminates decoding of write-once memories by mechanical and/or chemical means, eavesdropping of off chip Read-Only Memory (ROM) and cold boot attacks of random access memory (RAM) or static random access memory (SRAM). In future secure-computer appliances, it is required that all communications including I/O, code and data access be encrypted and only observable upon core entry pre-execution as code, and during execution, and not at CPU exit. All data entering the CPU or exiting processor ICs is to be encrypted. Only when one has a "need to know" or a "key", does data become observable. This project focuses on two types of EEPROMs, 1) large storage, high density with decreased/shortened lifetime or cycles having 10 to 20-year retention times and 2) low storage, low density, many program cycles but shortened retention.

To achieve these EEPROMs we exploit the observation that modern Hafnium dioxide (HfO₂) Silicon Oxide (SiO_x) CMOS can suffer from oxide charge traps both shallow and deep within the HfO₂ in which deep trap charges are tightly held but readily erased when excess voltage in proper amplitude and duration is applied. The voltage controlling the charge trapping (write) and unstrapping (erase) do not destroy the device but reduce device lifetime. Unfortunately, limited knowledge exists regarding device lifetime/wear out and retention verses the write and erase voltage pulse amplitude and duration. During write, charges become trapped in the Silicon Dioxide (SiO₂) to HfO₂ interface and within the HfO₂ layer resulting in both a storage and aging mechanism. Deep or tightly-held trap charges require a greater voltage write/erase, further stressing the oxide potentially degrading both long-term charge retention and device endurance/lifetime. In this project we exploit long-term threshold (ΔV_{TH}) shift in 32nm SiO₂/HfO₂ negative metal oxide semiconductor (NMOS) devices as well as next generation 22nm CMOS designs. In SiO₂/HfO₂ NMOS devices ΔV_{TH} shift is a strong function of both interface oxide and high-k oxide thicknesses, applied gate voltage, frequency and duty cycle of gate stress voltage. Aggressive gate voltage leads to a greater ΔV_{TH} shift and to simpler higher density EEPROM architectures but with fewer life cycles. These poorly understood issues demand that process characterization, i.e. ramp voltage stress, be carried out to ensure reliable EEPROM designs.

The objective when applying ramped voltage stress to arrays of low threshold HfO₂/SiO_x negative CMOS (N-CMOS) is to measure resulting threshold shift verse applied voltage (write and erase), determine the field acceleration parameter using 100s of measurements over thousands of transistors. The acceleration parameter is then combined with time dependent breakdown models resulting in device lifetime models for

both write and erase as a function of applied gate voltage. This results in write and erase protocols as a function lifetime, candidate write/erase voltages, high voltage programming circuit specifications, EEPROM architectures and candidate protocols for memory retention studies. With candidate write/erase protocols, selected unpowered retention studies were carried post write at elevated temperature using an Arrhenius relationship between lifetime and bake temperature. Write, erase, and retention loss stochastics were recorded from up to 20 die to assist statistical based EEPROM architecture designs, and final programming protocol down selection. EEPROM cell current measurements are supported by full custom printed circuit board that were designed, populated and tested when evaluating both test runs.

Two candidate EEPROM architectures were selected for design, verification and fabrication. This need was based on the observation that computer appliances, in general, need, at least, two varieties of EEPROMs 1) high density, long-term retention with limited lifetimes or use cycles, and 2) low density, high write/erase cycle devices with shortened retention times. After fabrication of the integrated circuit, these two EEPROM candidates were then themselves tested for write, read, and retention (elevated temperature Arrhenius testing) failure rates using both all-digital testing and supported by bank cell current measurements.

2.0 INTRODUCTION

2.1 Research Objectives

The goal of this project was to research and develop EEPROM intellectual property (IP) based on SiO₂/HfO₂ gate 32nm CMOS. SiO₂/HfO₂ gate 32nm CMOS is known to be at risk for long-term threshold shifts due to charge trapping. To this end, 32 and 22nm CMOS SOI processes have been proposed by others as potential EEPROM memory Intellectual Property (IP). This research and development effort were to develop (1) Stochastic based write-erase threshold shift models, (2) Write and erase protocols, i.e. voltages and duration, (3) retention rates, including read-write error rates, and (4) Multiple EEPROM architecture IP available for Air Force Research Laboratory (AFRL) personnel. The outcomes of this project aid in the deployment of in-situ EEPROM IP for silicon architectures for any division that employs trusted foundry fabrication capabilities.

2.2 Scope

The scope of this project was targeted at the implementation of EEPROM intellectual property in support of truly secure processor architectures at the 32nm and 22nm feature sizes. All computer appliances require security. Those of special interest are open systems including cloud, remote, or local serve platforms, smart phone networks, and networks in general. In *core or on chip* EEPROM encryption serves to protect the BIOS, bootloader, operating systems, and private user keys etc. from observation ensuring compute security. Computer appliance security is only successful if all code is made non-observable or encryption is secured on chip. This effort was to develop two chip EEPROMs based on standard 32nm CMOS technology to be an integral part of the CPU integrated circuit (IC). Such EEPROMs and their usage will not be observable by even the sophisticated user.

2.3 Background

Design of an integrated in-situ EEPROM circuit is not only a circuit design task. Moreover, fabricating a reliable megabyte memory compared to a kilobyte demonstration is a significantly different task. Due to limited knowledge of write-erase verses wear out, retention and threshold shift stochastics as a function of voltage and process variation, it is impractical to develop in-situ CMOS EEPROM memories knowledge of storage device stochastics. To this end, thousands of devices must be written and erased at least 10s of times at voltage ranges from 1V to 3V in 10mV steps in the effort to develop this knowledge. Test die have been designed, submitted and verified as well as rough test developed to accomplish the task to determine the needed knowledge. The required test plans were finalized in detail, test hardware and software were developed, device data was collected and EEPROM storage transistors were characterized. To compound this effort, the design of memories is a 5 or 6 sigma process based on sheer bit count in modern memory designs. The characterization effort requires a statistically significant number of devices be ramp voltage stress (RVS) tested, retention tested, and data fit to time dependent device breakdown down (TDDb) models. These modeling efforts provide life-time or wear out, threshold shifts as a function of applied voltage amplitude and pulse

duration and the related device stochastics i.e. retention or knowledge needed to design application specific EEPROMs.

The resulting in-situ EEPROM designs vary in architecture, high voltage circuitry requirements, and programming protocol, and sense amplifier as the application demands. The stochastically significant models developed in this effort not only support implementation efforts of the two EEPROM in this effort but are extensible to broad range of density wear out tradeoffs in targeting EEPROMS to a specific range of needs. This work makes complex networks of secure multi-core architecture clusters realizable by researchers and designers at the AFRL.

3.0 METHODS, ASSUMPTIONS, AND PROCEDURES

3.1 Specific Tasks

The tasks involved in meeting the technical requirements require flushing out the details of testing the submitted EEPROM test cells and consolidating this data into detail knowledge. Knowledge required to support the stochastic design of multiple EEPROMs resulted in informed decisions regarding trade-offs in wear-out verse EEPROM density. The knowledge was applied to the development and deployment of two EEPROM IP blocks. The following list constitutes the specific tasks that allowed the implementations in 32nm CMOS, with a potential extension to 22nm node designs via the characterization process effort.

- A validated characterization procedure for 32nm SiO₂/HfO₂ CMOS gate technology which models applied programming voltages verses device durability or life time. This characterization combines ramp voltage stress modeling with Time-Dependent Dielectric Breakdown (TDDB) models.
- Printed Circuit Boards (PCBs) (Two) for memory testing.
- Program code to control and extract analog data from test die populating the above PCBs.
- TDDB models for both write and erase voltages.
- Lifetime or wear out, i.e. number of program cycles as a function of write-erase voltage protocols.
- Retention as a function write-erase voltage protocols.
- Two write-erase voltage protocols.
- High voltage (2V to 3.5V) programming circuits for write and ease.
- A high density reduced life time EEPROM IP bank.
- A low-density long-lived time EEPROM IP bank.
- Read failure models with recommended error correction for all EEPROM banks developed.
- EEPROM cell library is comprised of but not limited to:
 - a. Low density IP bank, storage cell, write cell circuits, erase cell circuit, and sense amplifiers.
 - b. High density IP bank, storage cell, write cell circuit, erase cell circuit, and sense amplifiers.
 - c. Cell Layout and verification for a and b above.
- Assistance in the layout, verification and extension using each EEPROM bank to develop a large memory of AFRL choosing.
- Read-write error rates and retention times based on the Arrhenius relationship between lifetime and bake temperature for EEPROM banks above.

3.2 Literature Models Review

The deployment of high k materials in the CMOS technology for continued device scaling, reliability and lifetime modeling of high k materials such as HfO₂ have been extensively studied. However, an agreed-upon model has yet to be settled on. Research

groups claim genericity in their models by showing experimental data fitting without an appreciable detailed description of the physics. The following summarizes different schools of thought that prevail in the literature. Three aspects we learned from literature and were adopted for our model development are the concept of progressive breakdown, 3D Kinetic Monte Carlo algorithm and different current transport mechanisms in the gate dielectric.

Of the three models, the progressive breakdown model [1] [2] [3] [4] shown in Figure 1 is “quasi well accepted”. This model divides breakdown into four states. The first state is stress induced leakage current (SILC) stage. In this stage defects are randomly generated in both Interfacial Layer (IL) layer and High Dielectric (HK) layer. Gate current is in a power law relation with the stress time. Current transport mechanism in this stage is possibly charge trap assisted tunneling (TAT), Poole-Frenkel (PK) emission or Fowler-Nordheim (FN) tunneling [5]. Defects generate locally along grain boundary fault lines which resulted from dislocation of lattice atoms and appear in the polycrystalline form of HfO₂ lattice [5]. According to Cartier & Kerber [6], this process is recoverable. As SILC stage continues, more and more defects accumulate in IL and HK layers. Eventually a single percolation path forms and connects the gate electrode with the substrate. At this point the transistor reaches soft breakdown (SBD) as indicated by marker (B) in Figure 1. Once the SBD is reached an observable sudden but small increase of gate leakage current appears. Although there is still controversy as to which layer fails first, [7-8] suggest HK to be the first to fail while [9-12] suggest IL to be the first one, our application considers IL failure first and SBD marks the end of device lifetime. Continuing stress the device beyond SBD, the oxide layer enters post SBD stage or wear out stage indicated by marker (C) in Figure 1. During this stage, random jumps in the current levels corresponding to random telegraph noise are being observed [5]. This is due to the stochastic capture and emission of electrons into and out of the vacancy defect sites and constitutes the percolation path [5]. The final stage of this model is thermal runaway or hard breakdown (HBD). During this stage multiple percolation paths may form and current increases significantly. The HBD stage also involves migration of the metal atoms/ions from the gate into the dielectric and protruding all the way to the substrate [5]. The device completely fails once HBD occurs. Model development here uses this progressive breakdown model as a guideline for the TDDDB simulation. An accurate material model for IL and HK is critical.

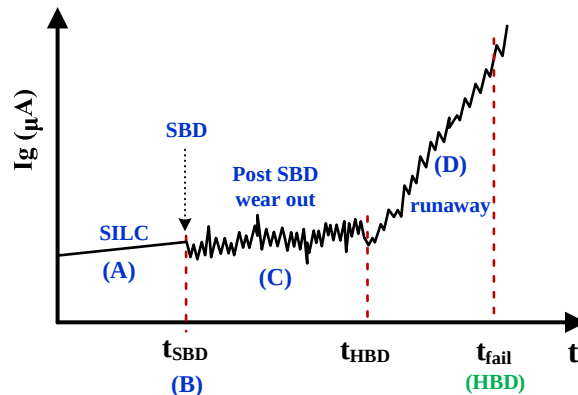


Figure 1. Progressive breakdown model current evolution with respect to time

Progressive breakdown regimes

N. Raghavan et al. [4] from Singapore University of Technology and Design have used COMSOL Multiphysics software package with Kinetic Monte Carlo (KMC) simulation to simulate the breakdown process in the HfO_2 gate stack. The simulation results, Figure 2, show the support of progressive breakdown process. The first row shows the cross section of the gate stack and second row shows the top view of the stack. Figure 2 (a) and (b) are for fresh device. Figure 2 (a) shows the existence of grain boundary (GB) fault lines. During SILC phase enhanced E field are mainly located along the GB fault lines as shown by (b) and (c). Soft Breakdown (SBD) occurs when IL layer breaks down shown by (e) and (f) and finally both HK and IL break down, (g) and (h).

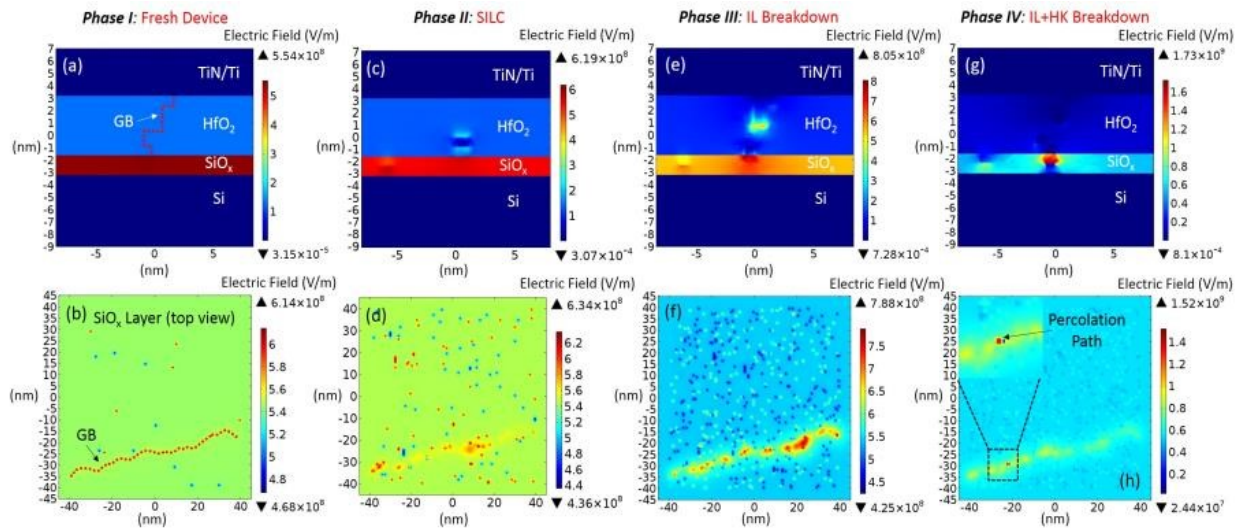


Figure 2 Simulated electric field distributions of different breakdown phases. Top row is cross-section view. Bottom row is the top view [4].

The Japanese research group, K. Okada et al., published a generated subordinate carrier injection (GSCI) model to explain the dielectric breakdown mechanism [8] [13]. The GSCI model considers that injected subordinate carriers rather than the electric field degrade the dielectric and breakdown occurs when their number reaches a threshold value. The subordinate carrier current can be decomposed into two components that one, I_{DC} , contributing to the breakdown and dominates at high voltage and the other, I_{TA} , does not contribute and dominates at lower voltages. The I_{TA} component results from trap assisted conduction such as PK tunneling. Okada et al consider I_{TA} currents not to contribute to defect generation and breakdown. As shown in [8] [13], the subordinate carrier current is constant with respect to different gate voltages. This means the carrier type with smaller current dominates the breakdown and the current is referred to as *dominating carrier for breakdown*, I_{DC} .

Within Advanced Micro Devices' (AMD) research group, A. Kerber et al. [14], made observations that HK dielectric gate stacks are characterized by short breakdown times and shallow Weibull slopes. The observations are explained by a percolation model

with different defect generation rates in the HK and IL layers. The difference of defect generation rates results in bimodal distributions with a transition from a shallow to steep Weibull slope. Test device area range is from $0.006 \mu\text{m}^2$ to $1000 \mu\text{m}^2$ and stressed at 125°C . Two different IL thickness were investigated (paper doesn't specify numbers) with 2nm HK layer.

A Failure criterion is defined as $1\mu\text{A}$ gate current density. Results show that for both nMOS and positive metal oxide semiconductor (pMOS), larger area devices have larger Weibull slopes. NMOS devices show significant current increase prior to breakdown which is suggested to be due to either a progressive component or stress-induced leakage current (SILC). Using AC stress where devices are allowed to discharge at a fixed negative voltage, no significant increase in gate current is seen. Therefore, the authors conclude the absence of progressive component. And the increase of gate current is attributed to SILC is due to defects generated in the HK layer. Similar results apply to pMOS as well. The progressive component may be used for explaining the transition of Weibull slope. Since this work shows no progressive component, different defect generation rates in the IL and HK layers are used to explain the transition. 3D KMC simulation is performed. Observations made from simulation results are (1) increasing defect generation rate in HK decreases time to breakdown, (2) TDDB distributions are bimodal for non-uniform defect generation in HK and IL layers. Transition occurs at lower Weibits since defect generation rate of the HK layer is higher than the IL layer. Area effect on TDDB can be summarized as 1) for small areas, defect density in the HK layer is high and t_{BD} and Weibull slope is limited by IL layer, 2) for large areas, Weibull slope is determined by the complete stack thickness.

Studies from Belgium T. Kauerauf, R. Degraeve et al. [15] [16] [17] have presented an all-in-one TDDB reliability predicting model. The authors believe that the constant voltage stress (CVS) extrapolation of SBD is challenged because (1) due to low breakdown voltages and low Weibull slope, the extrapolated SBD maximum applicable voltage for 10 years is significantly below the operating voltage, (2) high intrinsic gate leakage current comparing to the percolation current makes the SBD and its trigger moment hard to observe. In order to overcome the limitations, a combined TDDB extrapolation including both SBD and HBD is presented. Lifetime is no longer plotted as a function of the applied gate voltage but as a dielectric area vs. gate voltage plot including three regions: SBD free region, region of multiple SBD (wearout) and an HBD region, see Figure 3. It predicts no SBD on 0.1cm^2 after 10 years if $V_G < 0.52\text{V}$. If $V_G = 0.9\text{V}$ more than 1000 SBDs will be created after 10 years and for $V_G = 1\text{V}$, 0.01% of the chips will fail due to HBD. To generate the all-in-one TDDB reliability prediction in Figure 3, reliability parameters from the SBD and wearout distributions are needed: the Weibull slopes β_{SBD} and β_{WO} , the 63% values η_{SBD} and η_{WO} and voltage acceleration power-law exponents n_{SBD} and n_{WO} . Their relation to the HBD is given in equation 1, [15] [16].

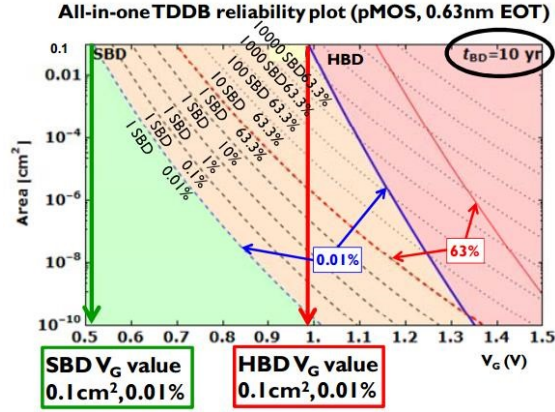


Figure 3. All-in-one TDDDB reliability for a 0.63nm EOT pMOS [15].

$$F_{HBD}[t] = 1 - \exp \left[- \left(\frac{\eta_{WO}}{\eta_{SBD}} \right)^{\beta_{SBD}} \cdot \int_0^{\left(\frac{t}{\eta_{WO}} \right)^{\beta_{WO}}} \left(\frac{t}{\eta_{WO}} - u^{\beta_{SBD}} \right)^{\beta_{SBD}} \cdot e^{-u} du \right] \quad (1)$$

3.3 Current Transport Mechanisms [18] [19] [20]

This section summarizes the current transport mechanisms in the HK gate stacks. These are also the mechanisms to be considered during model development. Current transport mechanisms can be classified into two categories, the intrinsic transport and extrinsic transport. The intrinsic transport is always present even if a defect free dielectric film is assumed. The extrinsic transport mechanism is related to the existence of defect states. The intrinsic transport mechanism includes direct tunneling which is merged with Fowler-Nordheim (FN) tunneling at high stress voltages and Schottky emission (SK). The extrinsic transport mechanism includes carrier elastic/inelastic tunneling into and out of defects known as trap-assisted tunneling (TAT), carrier tunneling between defects is known as trap-to-trap tunneling (TT), and Poole-Frenkel (PK) tunneling which is field enhanced thermal emission of electron from defects. Figure 4 shows the HK gate stack energy band diagram under positive gate voltage with all the current transport mechanisms.

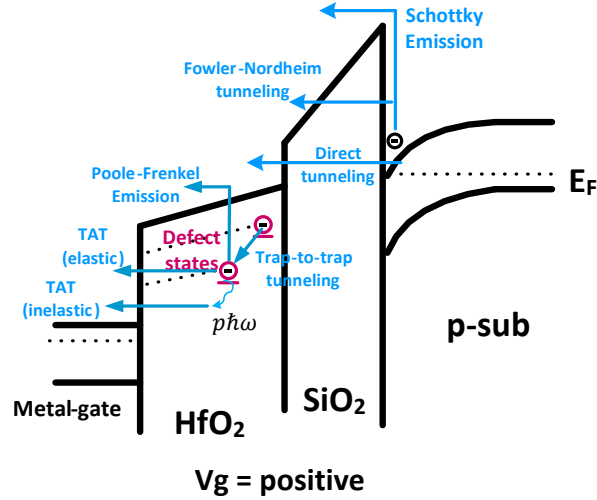


Figure 4. Summary of current transport mechanism in HK gate stacks.

Direct tunneling refers to carrier tunneling through the full barrier height of the SiO₂ layer determined by the conduction band offset of the material. Tunneling current density is given by

$$J_{dir} = A \cdot E_{ox}^2 \cdot \left(\frac{\Phi_B}{V_{ox}}\right) \cdot \left(\frac{2\Phi_B}{V_{ox}} - 1\right) \cdot e^{-\frac{B \left(1 - \left(1 - \frac{V_{ox}}{\Phi_B}\right)^{\frac{3}{2}}\right)}{E_{ox}}} \quad (2)$$

where A and B are constant, E_{ox} is the electric field across the dielectric, V_{ox} is the voltage applied to the oxide, Φ_B is barrier potential. Higher applied voltages result in a steeper band bending. Carriers tunnel through the triangular energy band and result in Fowler-Nordheim tunneling,

$$J_{FN} = A_{FN} E_{ox}^2 e^{-\frac{B_{FN}}{E_{ox}}} \quad (3)$$

where A_{FN} and B_{FN} are constants.

As the conduction band offset of SiO₂ layer is low, emission of carriers over the SiO₂ barrier into the conduction band of the HK film is called thermionic emission. For high temperatures and low electric fields emission of electrons over the SiO₂ barrier dominates current contribution, while for low temperatures and high electric fields tunneling of electrons dominates. The former case is called Schottky emission and is given by

$$J_{SK} = AT^2 e^{-\frac{1}{k_B} \left(\Phi_B - \sqrt{\frac{q^3 E_{ox}}{4\pi\epsilon_{ox}}} \right)} \quad (4)$$

where A is a constant, T is temperature, k_B is Boltzmann constant, Φ_B is barrier potential of SiO_2 , ϵ_{ox} is oxide permittivity. The latter case is also known as FN tunneling.

Besides direct or FN tunneling, which are one-step tunneling processes, defects in the dielectric layers give rise to tunneling processes based on two or more steps. For our study, this tunneling component is observed after write-erase cycles due to the generation of more defects in the dielectric. The increased tunneling current at low gate stress is called SILC and is mainly responsible for the degradation of the retention time of nonvolatile memory devices [19]. It is accepted that it is caused by inelastic TAT [19]. Reference [20] has summarized the current density for trap-to-trap conduction, equation (5) and PK emission, equation (6),

$$J_{TT} = C_1 E_{ox} e^{-\frac{E_a}{k_B T}} \quad (5)$$

where C_1 is a constant, E_a is activation energy,

$$J_{pf} = E_{ox} \cdot e^{-\frac{q \left(\Phi_B - \sqrt{\frac{q \cdot E_{ox}}{\pi \epsilon_i}} \right)}{kT}} \quad (6)$$

This concludes all the current transport mechanisms in the HK gate stacks.

4.0 RESULTS AND DISCUSSION

4.1 EEPROM Wrapper Interface Specification

4.1.1. Wrapper Introduction

Figure 5 represents a block diagram of the EEPROM that was proposed including EEPROM core and the wrapper. The wrapper consists of three input registers, finite-state machine (FSM) controller, counters, clock divider, necessary combinational logic, and CPU/EEPROM interface logic. CPU/EEPROM interface needs final decision from AFRL, indicated in TBD region of Fig. 5. The designed version assumes a four-signal set interface consisting of data bus, R/W indicating CPU read or CPU write, address that specifies the register to be accessed, and a clock signal. The wrapper has reserved error-correcting code (ECC) functional block and on-chip programming voltage supplies for future versions.

4.1.2 Wrapper Block Specification

Wrapper consists of three input registers, CUI (command user interface), controller (FSM), counters, clock divider, and other combinational logic. The wrapper serves the purpose of interfacing CPU and EEPROM core with control signals and appropriate transferring of input/output (I/O) data.

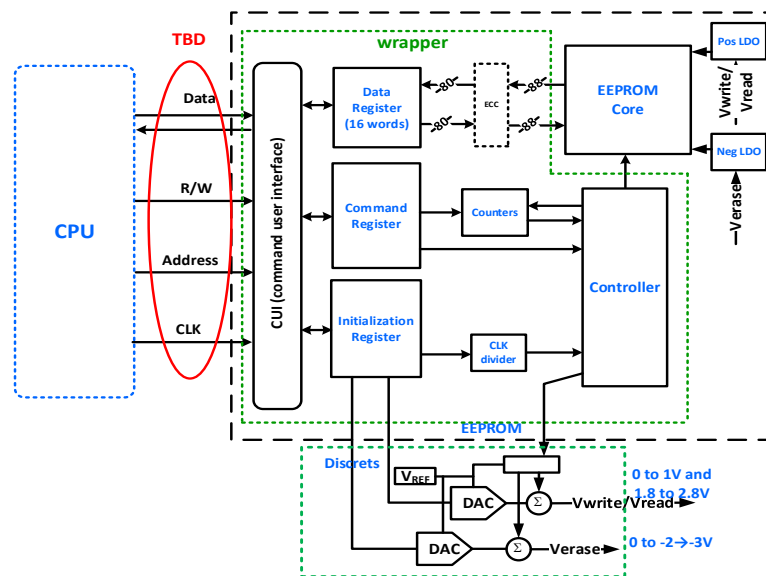


Figure 5. Top level block diagram of the final EEPROM and its interface with the CPU and the low drop-out regulator (LDO) controlled Digital to Analog Converters (DACs).

Input Register Definition -- There are three input registers, *initialization register*, *command register* and a *16 words data register*.

The initialization register is 80 bits wide containing the CPU clock divide value and programming voltage values, digital to analog converter (DAC) set points. See Figure 6 for the bit allocation of the initialization register. Reserved voltage programming bits are

for future on-chip or off-chip DAC controlled supply voltages. Programming voltages are integral to the test PCB in the present version.

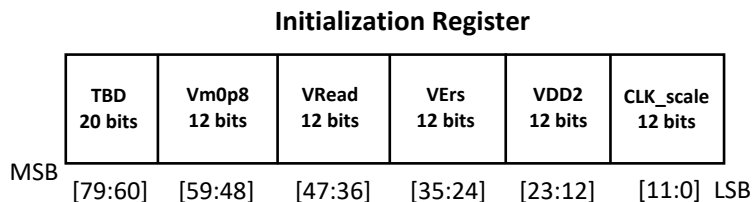


Figure 6. Initialization register bit allocation.

The command register is 80 bits wide containing the EEPROM address, counter/timer values for voltage stabilization time and voltage application time for write, read, and erase operations respectively, a time out value, a **BUSY** bit and command bits. Figure 7 shows the bit allocation of command register.

The **BUSY** bit is an access control bit in the CUI shared between CPU and EEPROM. The **BUSY** bit prohibits the CPU from writing the data register until a command execution has completed by the EEPROM. The address bits **CMD[0:9]** include word and bank address pointer to the EEPROM location to be written/read/erased. Bits **CMD[10:11]** are reserved for future use. Voltage stabilization time bits, **CMD[12:19]**, **[28:35]**, and **[44:51]**, are the time delays ensuring programming voltages become stable at the supply pins before applying to the EEPROM cell by control signals. Voltage application time bits, **CMD[20:27]**, **[36:43]**, and **[52:59]**, set the time period that the programming (W/R/E) voltage is to be applied. The timeout bits, **CMD[60:67]**, are provided for high voltage supply quenching to avoid excess voltage as the state transitions back to the idle mode. Bits **[68:70]** are reserved for future use. **CMD[72:79]** 8 bits, specify the memory operation to be carried out. **CMD[76:79]** 4 bits, specifies a block (16 words) when equal to x"f" and a single word operation when equal to x"0". The type of operation is specified by **CMD[72:75]**. Write (**WR**) operation is "1"x, Erase (**ER**) operation is "2"x and Read (**RD**) operation is "3"x, respectively. All other combinations of **CMD[72:79]** are invalid for this design and reserved for future use.

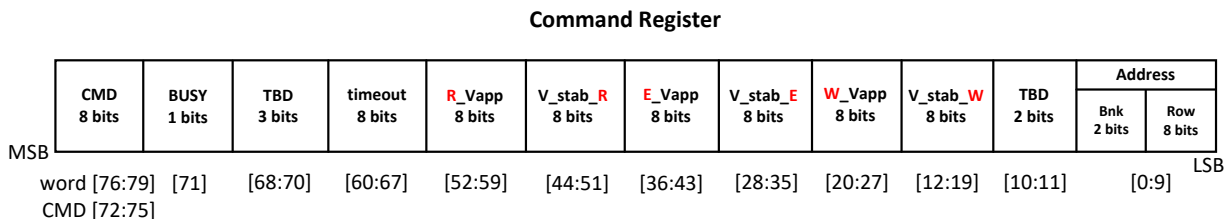


Figure 7. Command register bit allocation.

CUI Definition -- CUI, the command user interface, is a logic block that schedules data traffic among CPU, input registers and EEPROM core. Figure 8 represents the CUI circuit diagram. This unit consists of an initialization register, command register, sixteen (a block of 16 words) 80-bit data registers, a 4-bit word counter, and other control logic. Registers can be accessed by applying the correct CPU address which uses the two least

significant bits (LSB) of the CPU address, **CPU_addr[0:1]**. The **CPURW** bit indicates that CPU writes to the registers when it is logic 1 and reads from registers when it is logic 0. Both CPU and EEPROM core access the 16-word data register in a mutually exclusive manner depending on the status of **BUSY** bit. A clear **BUSY** bit, logic 0, allows CPU to have access to the data register. CPU write or read depends on the **CPURW** bit status. When the **BUSY** is true, logic 1, the EEPROM has access to the data register. In this manner, CPU and EEPROM can never access data registers simultaneously since the CPU sets the **BUSY** bit for passing control to EEPROM while the wrapper clears the **BUSY** bit for passing control back to CPU. *The CPU may read initialization and command registers independent of the status of the **BUSY** bit.* The data register serves as an intermediate buffer or storage between CPU and EEPROM to minimize the overhead time since EEPROM operates at lower clock rate than CPU.

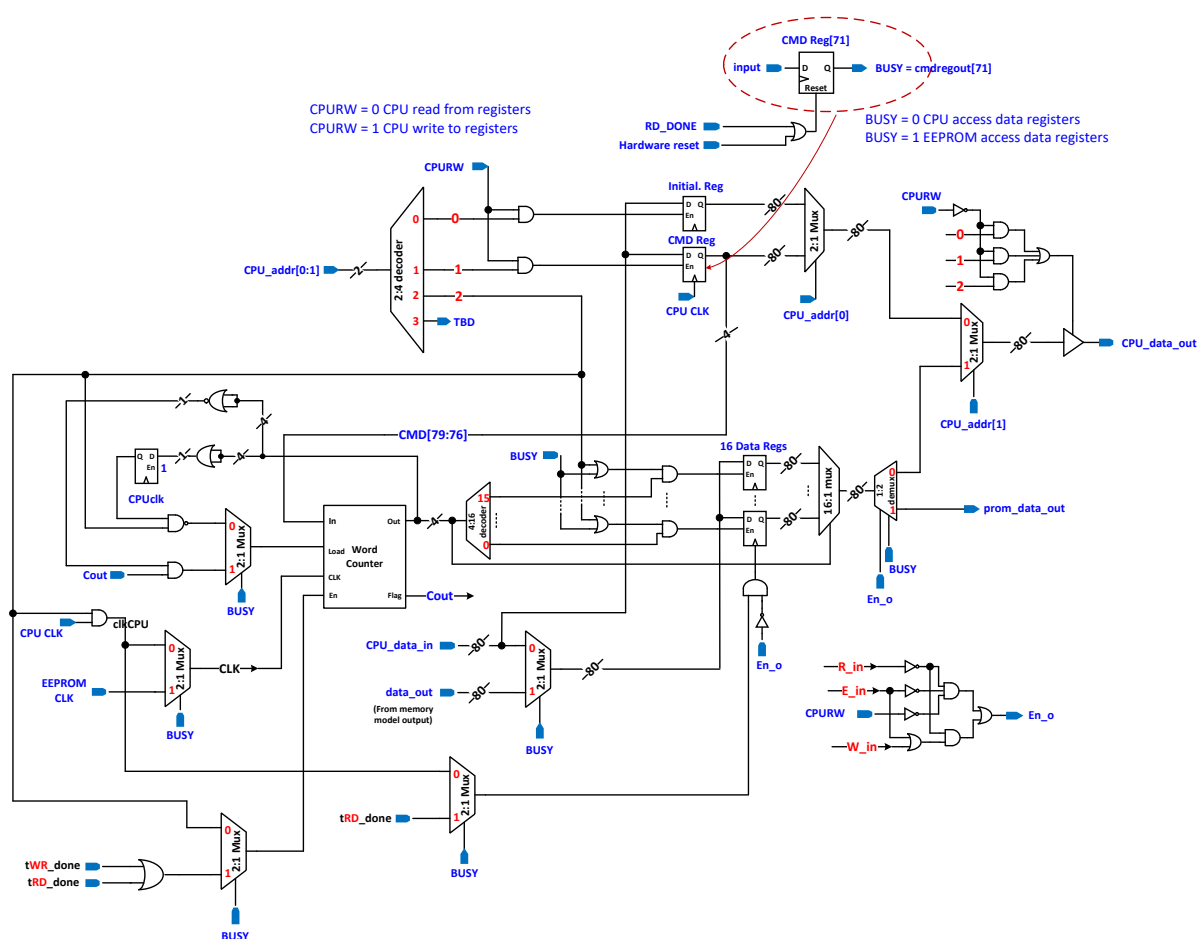


Figure 8. CUI (command user interface) schematic.

The 4-bit word counter tracks operation progress through the 16-word data register. For a block (16 words) of data, the word counter is loaded with value x'f' via the command register bits **CMD[76:79]**. For single word data, the word counter is loaded with value x'0'. Granting CPU access to the data register enables the word counter. The word counter is decremented via the CPU clock as execution progresses through the data

register count. The word count is decremented during EEPROM register access, for each data register read by the EEPROM during Write. The word counter is decremented only when one Write or Read operation is completed and indicated by signal **tWR_done** or **tRD_done** by being true, logic 1. The data register latches data when **tRD_done** is true indicating the content read from EEPROM memory was written back into the data register. For both CPU and EEPROM access, when either a block (16 words) or a word access is finished, the overflow bit, **Cout**, of the word counter goes high indicating the completion of operation. Relevant state(s) within the wrapper state machine are relative to the **Cout** signal.

Controller (FSM) -- Figure 9 summarizes EEPROM wrapper operation using the state diagram. This design uses separate counters/timers for each state of operation. Write voltage stabilization timer is loaded in "Write Starts" state. This timer starts in "VDD2 V_Stab" state. The write voltage application timer is loaded during the "Write starts" state or "Read Starts" state or reloaded for next word in "W_done" state. The voltage application timer starts in "W_Vapp time" state. In "W_done" state, check for **Cout='1'** and **t_out='0'** which depicts the completion of an operation. **t_out** signal is the timeout indicator. It is high when timeout counter is finished counting. With **Cout='0'** and **t_out='0'**, control returns to "W_Vapp time" state that means there are still words to write. Timeout timer starts only when **Cout** equals 1 irrespective of being in the "W_done" state indicating there are no more words in data register to be written. After Write operation is complete, control enters the memory Read operation automatically to read out the words as written or as erased and stores them back to the data register for CPU to retrieve and confirm data validity.

Erase voltage stabilization timer is loaded in the "Erase Starts" state and enabled in "VErs V_Stab" state. Erase voltage application timer is loaded in "Erase Starts" state or "Read Starts" state and enabled in "E_Vapp time" state. Since only a block (16 words) is erased, timeout counter starts on the first "E_done" state occurrence, the word counter is loaded with value "1" and sufficient voltage application time is applied so as to erase all 16 words at once. After erase time out, i.e. **t_out** is true, the read operation starts automatically to confirm erasure. This design only does a block erase. *The block access is restricted to addresses that have a 16-bit boundary available within the same bank. In other words, this design does not support block operations that overlap between two banks i.e., all the 16 addresses of the block must be in the same bank.*

The Read voltage stabilization timer is loaded in the "Read Starts" state and enabled in "Vread V_Stab" state. Read voltage application timer is loaded in "Read Starts" state or reloaded for next word in "R_done" state and enabled in "R_Vapp time" state. After the completion of Read operation, the control returns to "idle" state and waits there until it receives a new operation command from the CPU.

The Write operation and Erase operation share the Time out counter and the time out timer is loaded in "Write starts" state or "Erase starts" state. It starts only if the control is in "E_done" state or "W_done" state and **Cout** is true.

This controller also generates control signals **W_in**, **E_in**, **R_in**, **WR**, **ER**, **RD** and **RD_DONE** that are required for processing few other signals in the Very-High Speed Integrated Circuit (VHSIC) Hardware Descriptive Language (VHDL) code. Signal **W_in**, **E_in**, and **R_in** stays high from the time the control enters "W/E/R_Vapp" state till "W/E/R_done" state is active of the corresponding operation. Signal **WR**, **ER**, and **RD** is

true only during the “W/E/R_Vapp” state of the corresponding operation. **RD_DONE** is generated when Read operation is completed and the control is returned to “idle” state and used to set **BUSY** bit to 0 so that CUI access is returned to CPU.

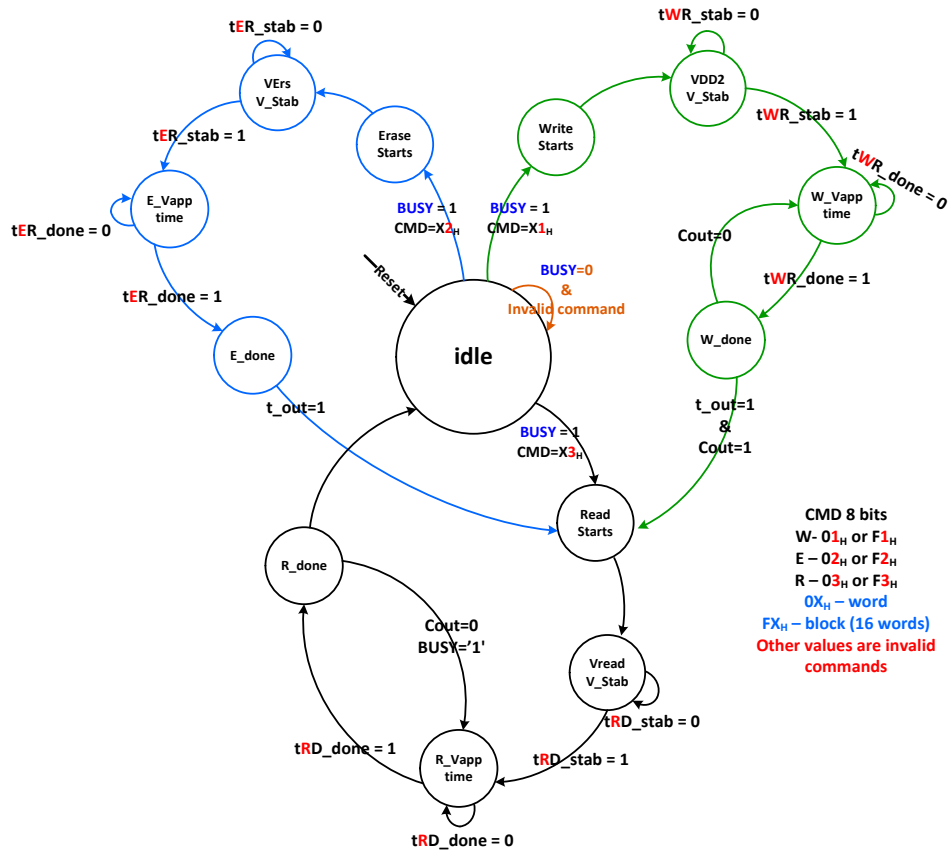


Figure 9. State diagram of the controller.

4.1.3 Wrapper Operation

Write -- Write operation begins by the CPU observing the **BUSY** bit false, loading the initialization, command, and data registers and setting the **CPURW** bit true. **CPU_addr** '00' refers to the initialization register, '01' refers to the command register and '10' refers to the data register. **CPU_addr** '11' is reserved for future use. When loading the command register for the first time, the **BUSY** bit (**CMD[71]**) should be loaded with 0 allowing the CPU to access the input registers. After the data register is loaded, the command register is reloaded to setting the **BUSY** bit passing control to the EEPROM wrapper state machine, Fig. 9. This will start the designated EEPROM operation set by the command bits **CMD[72:79]**.

Example CPU commands for write are the following:

```
CPURW <= '1';
CPU_addr <= "00"; -- initialization register
CPU_data_in <= x"123456789abcdef12340";
```

wait for 10 ns;

CPU_addr <= "01"; -- command register

CPU_data_in <= x"010020502020202000"; -- write one word, BUSY bit is 0, CPU access data register.

wait for 10 ns;

CPU_addr <= "10"; -- data register

CPU_data_in <= x"a0000000000000000000";

wait for 10 ns;

CPU_addr <= "01"; --reload command register

CPU_data_in <= x"018020502020202000"; --BUSY bit is set to 1, EEPROM operation starts.

Command register bits **CMD[72:79]** should be x"01" or x"f1" indicating write one word or a block (i.e.16) of words respectively. *The EEPROM wrapper returns to the idle state and access to data register is given to the CPU. Command is given to the CPU in the event of an invalid command or state in the CUI.* Command register address bit **CMD[0:9]** is decoded to allow access to the target address and bank. When writing a block of words, the initial address is decoded. The word counter in CUI is loaded with x"f". The address counter increments to the next addresses sequentially after each word write. The word counter is decremented and points to the next word moved to memory from the data register. This process repeats until all 16 words (one block) is transferred to memory. *This design does not support block operations that overlap between two banks. This means block access is consecutive from the address of the first memory word only on 16 bit boundaries. The starting block address must be an integer multiple of 16 on a 16-word boundary.* After the write operation is complete, read operation automatically starts to confirm the write. The stored words are written back to the data register for CPU to retrieve and confirm. After EEPROM read operation is completed, data register (or CUI) access is returned to CPU by FSM which clears the **BUSY** bit. The EEPROM then enters idle state. The CPU may then retrieve the data from the data register or disregard it by over writing the data register with new values.

The EEPROM control signals to one bank for write operation are **W1_Bk0[0:87]**, **W0_Bk0[0:87]**, **BS_Bk0[0:87]**, **TL_Bk0[0:87]**. These signals are generated for four or more banks based to the decoded bank address from command register bits **CMD[8:9]**. This design has preserved 8 bits for ECC. Therefore, the 80-bit data has 8 bits appended to the MSB side after leaving the CUI to make an 88-bit data word in the memory core. All the EEPROM control signals are 88 bits. The control signals **BS_Bk0[0:87]**, and **TL_Bk0[0:87]** are generated using the signals **Bnk**, **WR**, **RD**, **ER**, **Data_ECC** which are generated from the controller. Control signal generation is discussed in a later section.

Erase -- Erase simultaneously clears a block of words. Erase operation begins when the CPU loads the command register **CMD[72:79]** bits with x"f2", **BUSY** bit 0, correct timer values and address. Even though a block of words is erased at the same time, the bits **CMD[76:79]** need to be loaded with x"f" for the word counter to enable 16 words read after erase operation. The **BUSY** bit is set via command register starting a

new block erase operation. Other **CMD** bits remain the same from previous load. It is necessary for the two separate load operations to the command register for setting up the word counter and **BUSY** bit. The block to be erased is determined by decoding the address bits **CMD[4:7]**. After an erase operation is completed, read operation starts automatically to confirm the erase result. The erased words are read and written back to the data register for CPU confirmation. With the read operation complete, the **BUSY** bit is cleared and EEPROM enters idle state. To erase an additional block, CPU must initiate via the command register with block starting address and erase command.

Example CPU commands for an erase operation are the following:

```
CPURW <= '1';
CPU_addr <= "00"; --No need to reload initialization register if its value is unchanged.
CPU_data_in <= x"123456789abcdef12340";
wait for 10 ns;

CPU_addr <= "01"; -- command register
CPU_data_in <= x"f2002050202020202000"; -- erase command, BUSY bit is 0,
CMD[76:79] loaded with f.
wait for 10 ns;

CPU_addr <= "01"; -- reload command register
CPU_data_in <= x"f2802050202020202000"; --BUSY bit is set to 1, EEPROM operation
starts.
```

Read -- Read operation begins by the CPU loading the command register **CMD[72:79]** bits with x"f3" or x"03" indicating a block read or a single word read respectively, while the **BUSY** bit is clear. In addition, the correct timer values and EEPROM address must be loaded. Again, the BUSY is set while other bit values are maintained identical to the first load. The command bits **CMD[0:9]** are decoded to allow access to targeted EEPROM address and bank. The read data from each memory address is transferred to the data register for CPU retrieval. When reading a block of words, the initial memory address is decoded, placed in the address counter, which is incremented after each word read. After read operation is completed, the **BUSY** bit is cleared returning data register access back to CPU and the EEPROM wrapper enters the idle state.

Example CPU commands for a read operation are the following:

```
CPURW <= '1';
CPU_addr <= "00"; --No need to reload initialization register if its value is unchanged.
CPU_data_in <= x"123456789abcdef12340";
wait for 10 ns;

CPU_addr <= "01"; -- command register
```

```
CPU_data_in <= x"002050202020202000"; -- read one block, BUSY bit is 0, CPU
access data register.
wait for 10 ns;
```

```
CPU_addr <= "01"; -- reload command register
CPU_data_in <= x"f3802050202020202000"; -- BUSY bit is set to 1, EEPROM operation
starts.
```

EEPROM Core Control Signals -- The control signals of EEPROM core are classified into two groups for further discussion. One group of signals control the transistors of each column to assist cell operation. This group of signals include **W1_Bk0[0:87]**, **W0_Bk0[0:87]**, **BS[0:87]**, **WR_b +ER_b**, and **RD** for a bank. It is important to note that there are two inversions for generating TL signal. Fig. 13 shows both version circuits. The basic difference of the two versions is that one uses one signal TL to control the tail inverter while the other uses two separated signals. The advantage of the second version is both pmos and nmos are off resulting in lower leakage current. The simulation in this report uses the version of a single TL signal. The **Bkn** where n in the signal name indicates the bank number. For four banks, the names are **Bk0**, **Bk1**, **Bk2**, **Bk3**. The generation of these signals depends on decoded bank select signal **Bnk**, **WR**, **RD**, **ER**, and **W1/W0**. Fig. 10 shows the signal location in the circuit. Table 1 shows signal status for different memory operations. The transistor on the side where W1 or W0 is logic 1 will have charge traps in the dielectric resulting in increase of threshold. When reading, this side will have smaller current than the non-programed side of the storage pair.

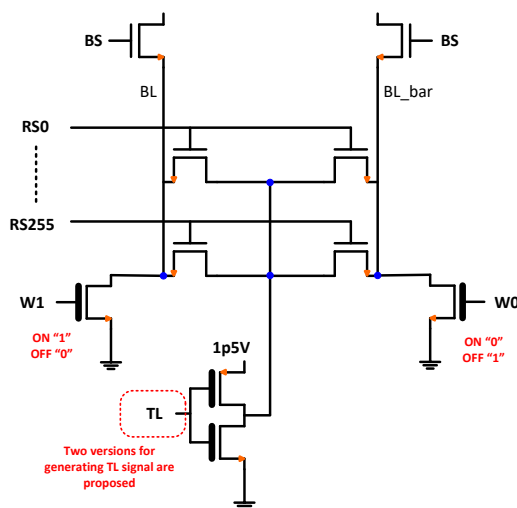


Figure 10. EEPROM cell control signals.

The second group of signals includes 256 **pside** and **nside** signals that are connected to the level shifter to generate the row select signal, **RS** and sense enable signal **SE** to enable the sense amplifier. The signal status of **pside** and **nside** are derived from level shifter logic. The row select, **RS** level requirement for each memory operation is presented in Table 2. Figure 11 shows the level shifter logic. Signals **pside** and **nside** are generated based on signals **WR**, **ER**, **RD**, decoded address **addr_decode**, and block

select signal **Blk**, which is decoded from address bits **CMD[4:7]**. The red line of synthesis in Figure 11 shows the boundary of circuit synthesized.

This design has preserved 8 bits for ECC. Therefore, the 80-bit data from data register will be appended 8 bits to the MSB side after coming out from CUI to make 88-bit data (**Data_ECC**) in the memory core. All the EEPROM control signals are 88 bits.

Table 1. Signal status of each memory operation

	Signals	Write WR =1, ER = RD =0	Erase ER =1, RD = WR =0	Read RD =1, WR = ER =0,
Selected bank Bnk(#) = 1	W1_Bk#	Data_ECC	0	0
	W0_Bk#	Data_ECC_bar	0	0
	BS_Bk#	1	1	1
	(W+Ers)_b	0	0	1
	R	0	0	1
Non-selected bank Bnk(#) = 0	W1_Bk#	0	1	0
	W0_Bk#	0	1	0
	BS_Bk#	1	1	0
	W_b +Ers_b	1	0	0
	R	1	0	0

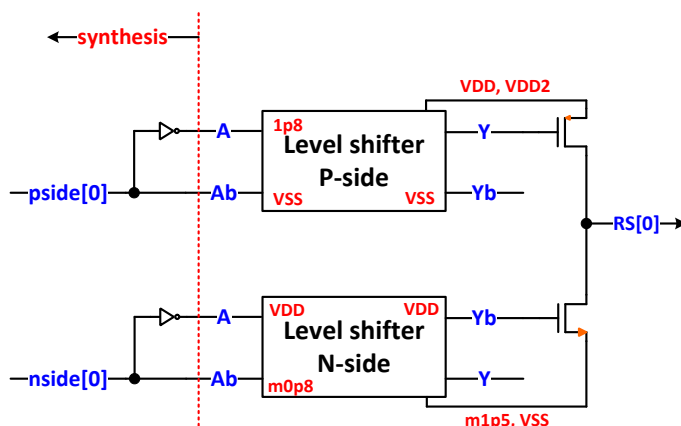


Figure 11. Control signal for generating **RS** signal.

Table 2. Row select (RS) logic

	pside, Yb	nside, Yb	RS
Write (WR =1, ER =0, RD =0, addr_decode =1, Blk =0)	1	0	VDD2
Non write (WR =1, ER =0, RD =0, addr_decode =0, Blk =0)	0	1	VSS
Erase (WR =0, ER =1, RD =0, addr_decode =x, Blk =1)	0	1	m1p5
Non erase (WR =0, ER =1, RD =0, addr_decode =x, Blk =0)	1	0	VDD
Read (WR =0, ER =0, RD =1, addr_decode =1, Blk =0)	1	0	VDDR
Non read (WR =0, ER =0, RD =1, addr_decode =0, Blk =0)	0	1	VSS
Idle (WR =0, ER =0, RD =0, addr_decode =0, Blk =0)	0	1	VSS

4.1.4 Wrapper Block Signals and Overall Schematic

Fig. 12 shows the signals between CPU wrapper interface and wrapper EEPROM interface. The circuit in the dotted box of Fig. 12 is replicated 256 times for all words. Fig. 13 shows the full wrapper schematic. The circuit (i.e., within the blue box in Fig. 13) is implemented through synthesis.

4.1.5 Wrapper Synthesis Report

Reports are generated through the synth.out code file synthesized via the DC compiler. The code incorporates our VHDL files into the server and analyzes all the aspects and constraints and delivers reports on power requirements, timing enclosure, total area and number of gates and components. It also generates a netlist (.vh file) which we use for importing the design into encounter tool to perform place and route of design.

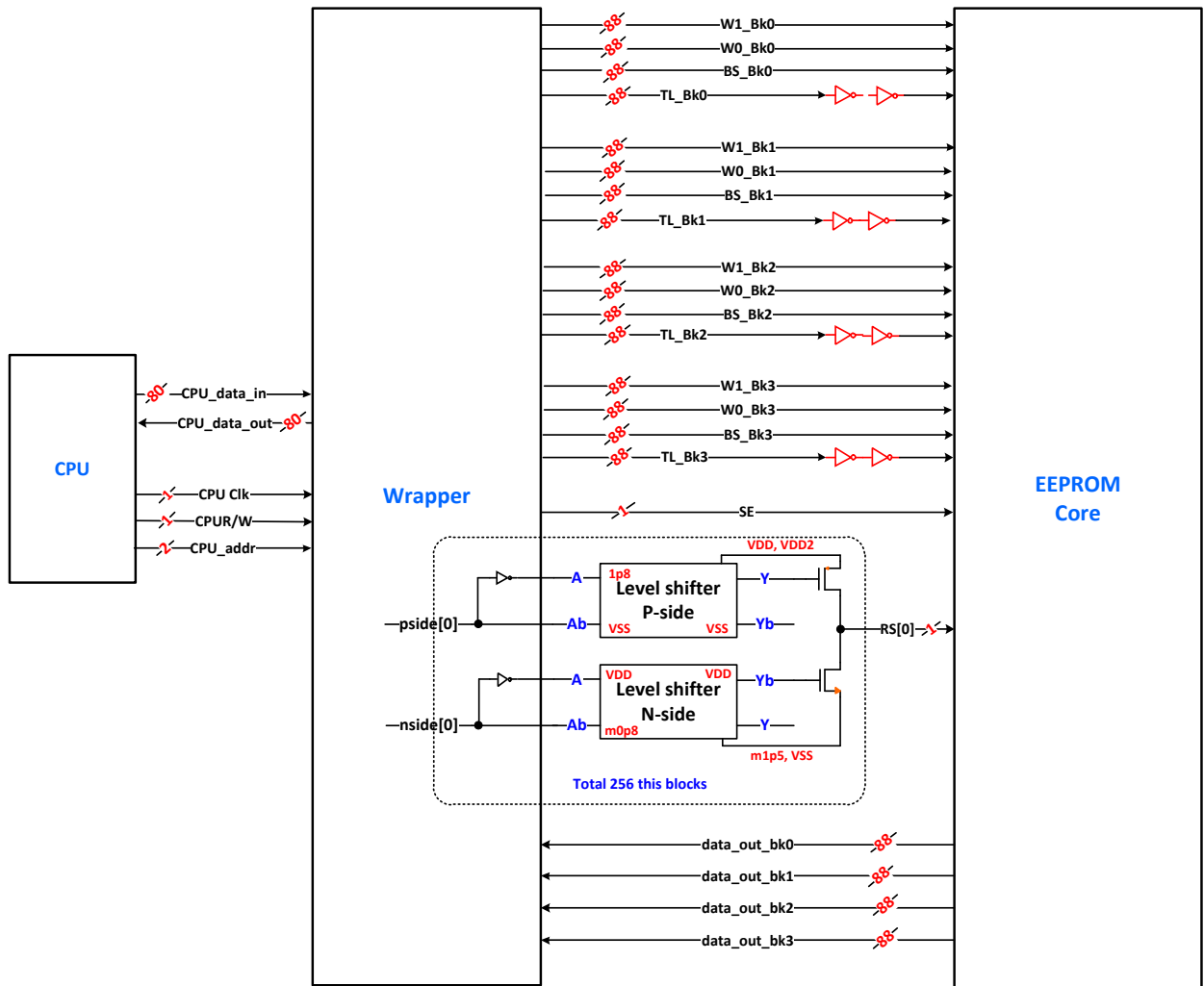


Figure 12. CPU, wrapper and EEPROM interconnect signals.

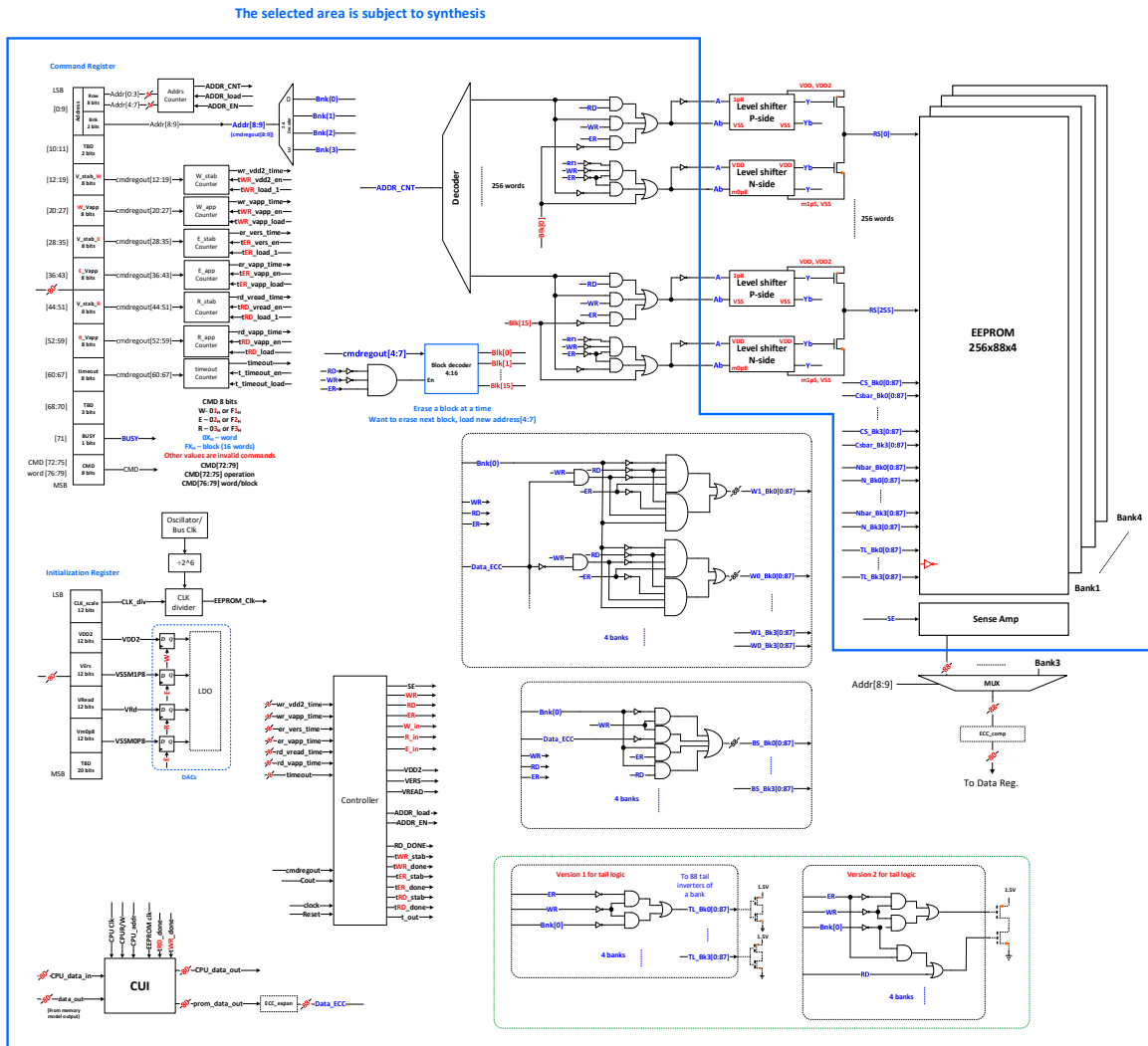


Figure 13. Wrapper schematic.

4.1.6 JTAG Project Setup (IEEE Std. 1149)

This project utilizes the preferred method of setting up JTAG on the project to provide for accurate testing. Figure 14 is a simplified diagram that displays a top view of the entire JTAG system:

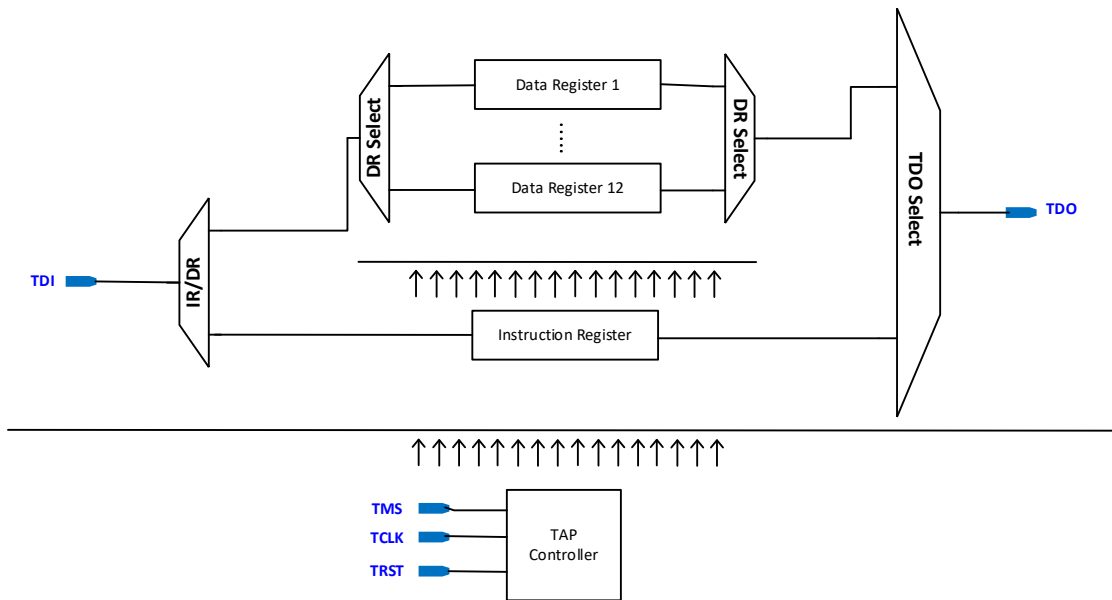


Figure 14. JTAG registers.

In Figure 14, TDI (Test Data Input) is input information used for scanning in data to a circuit and for inserting commands in the instruction register. The TDO (Test Data Out) pin scans out data from either one of the data registers or the instruction register. The registers in the system are shift-registers, meaning that input shifted into a register via TDI causes data to shift out of the TDO pin. TCLK and TRST are the JTAG clock and reset pins respectively. TMS (Test Mode Select) is a pin used for a finite state machine in the controller. This finite state machine controls the IR/DR Multiplexer determining if data from the TDI pin are being scanned into the data registers or control registers and when to save the information.

Note: Control of all aspects of the JTAG configuration are by SVF files.

The bottom data register in Figure 14, “Data Registers 12”, is to convey that there are 12 data registers in the preferred setup. The list of the registers is on the next page.

Note: All registers must be able to both read and scan-in information.

Figure 15 shows the full schematic of the test bed with certain lines highlighted in blue and encircled in dotted boxes to indicate areas where data registers placement. Next to the lines are blue outlined boxes that indicate which registers the lines exist.

Note: Some lines will not have all their bits used. Some Registers will have their specific signals displayed under the list.

JTAG Data Registers:

1. Bypass Register
2. ID Code Register
3. In-Command Register (80bit)
4. Out-Command Register (80bit)
5. In-Initialization Register (80bit)
6. Out-Initialization Register (80bit)
7. In-Data Register (80bit)
8. Out-Data Register (80bit)
9. Out-EEPROM Register (80bit)
10. In-EEPROM (1) Register (80bit)
11. In-EEPROM (2) Register (80bit)
12. FSM/Misc. Register (80bit)

In-EEPROM (1), In-EEPROM (2), FSM/Misc. Registers Detailed:

In-EEPROM (1) Register:

- RS (8bits)
 - o [Bit Values]: [0], [36], [73], [110], [146], [182], [219], [256]
- W1_Bnk0 (9bits); W1_Bnk1 (9bits); W1_Bnk2 (9bits); W1_Bnk3 (9bits)
 - o [Bit Values]: [0], [15], [20], [29], [44], [50], [59], [73], [88]
- Csbar_Bnk0 (9bits); Csbar_Bnk1 (9bits); Csbar_Bnk2 (9bits); Csbar_Bnk3 (9bits)
 - o [Bit Values]: [0], [15], [20], [29], [44], [50], [59], [73], [88]

In-EEPROM (2) Register:

- BS-Bnk0 (7bits); BS-Bnk1 (7bits); BS-Bnk2 (7bits); BS-Bnk3 (7bits)
 - o [Bit Values]: [0], [15], [29], [44], [59], [73], [88]
- BS_Bnk0 (7bits); BS_Bnk1 (7bits); BS_Bnk2 (7bits); BS_Bnk3 (7bits)
 - o [Bit Values]: [0], [15], [29], [44], [59], [73], [88]
- TL_Bnk0 (6bits); TL_Bnk1 (6bits); TL_Bnk2 (6bits); TL_Bnk3 (6bits)
 - o [Bit Values]: [0], [15], [29], [59], [73], [88]

FSM/Misc. Register: TBD/Empty (8bits)

FSM (63bits) -

- | | | |
|---------------|-----------------------|------------------------|
| • WR (1bit) | • E_in (1bit) | • rd_vread_time (8bit) |
| • RD (1bit) | • wr_vdd2_time (8bit) | • rd_vapp_time (8bit) |
| • ER (1bit) | • wr_vapp_time (8bit) | • timeout (8bit) |
| • W_in (1bit) | • er_vers_time (8bit) | • SE (1bit) |
| • R_in (1bit) | • er_vapp_time (8bit) | |

Misc. (9bits)

ADDR_EN (1bit)

Addr[0:7] (8bit)

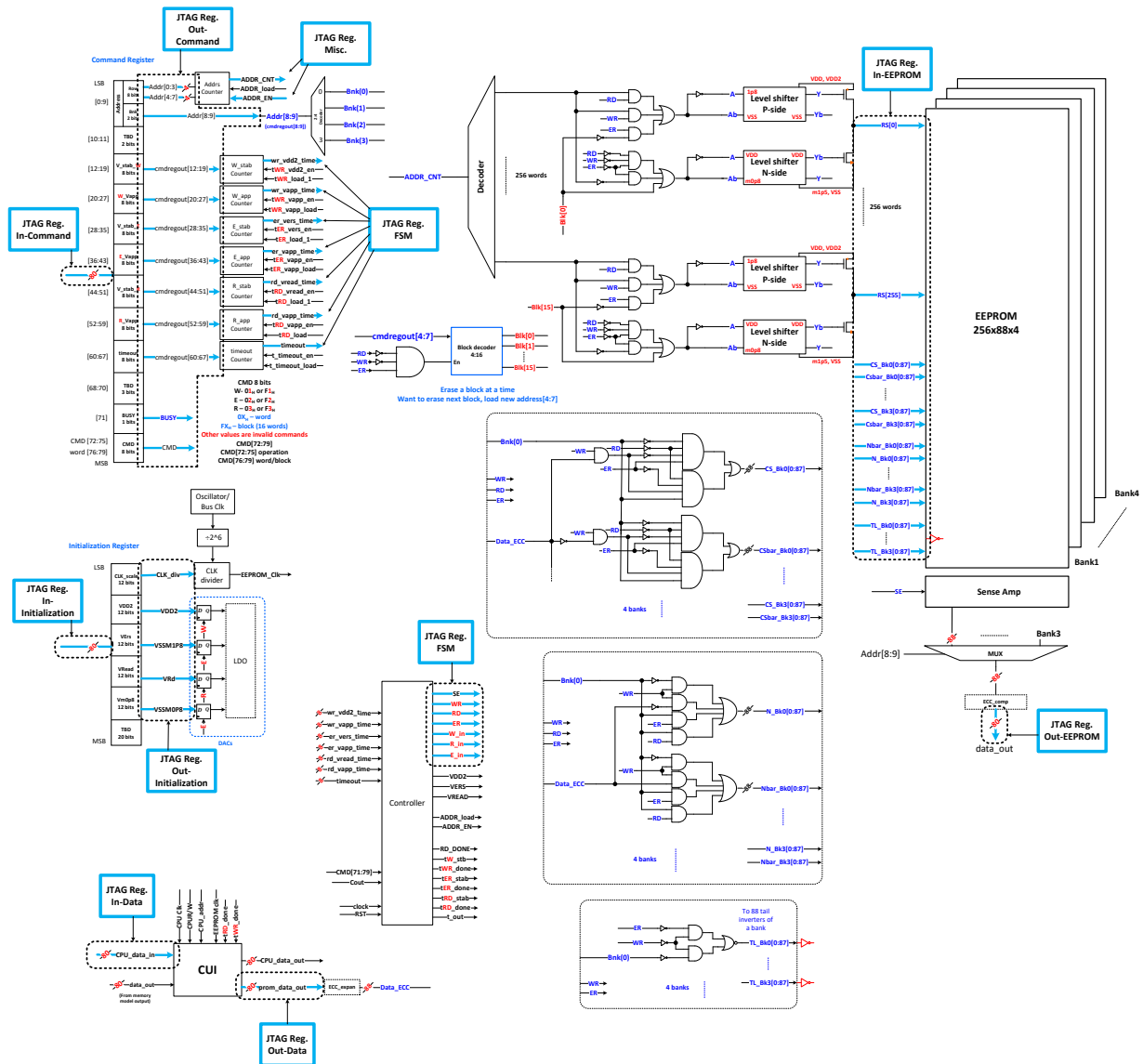


Figure 15. JTAG registers in the wrapper.

4.1.7 Programming Voltage Generation

The programming voltages, VDD2, m1p5, 1p5V, are generated using two on-chip LDOs (low dropout voltage regulator) and two off-chip DACs (digital to analog converter) for programming and read. Figure 16(a) shows the schematic of LDO for positive voltage and (b) for negative voltage. The DAC has full scale range 0 to 3V and 12-bit resolution allowing an LSB of 0.73mV. The DAC is the “reference” voltage controlling the LDO, whereas LSB is the incremental programming voltage or resolution. The literature reports 200mV and 300mV threshold shifts, for a 2.5V write pulse voltage of 10ms and 100ms in duration. The write voltage (VDD2) has a programmable range of 1.5V to 2.7V as well as the read voltage from 0 to 700mV. On the other hand, the erase voltage (m1p5) has a range from 0V to -1.5V. The LDOs settle within 0.1% of shortest programming pulse width.

As shown by Table 2, for each memory operation, either PMOS or NMOS is ON meaning VDD2 and m1p5 must be exclusive. Therefore, only two LDOs are required for these voltage supplies. Table 3 shows the LDO design specifications according to the programming requirements.

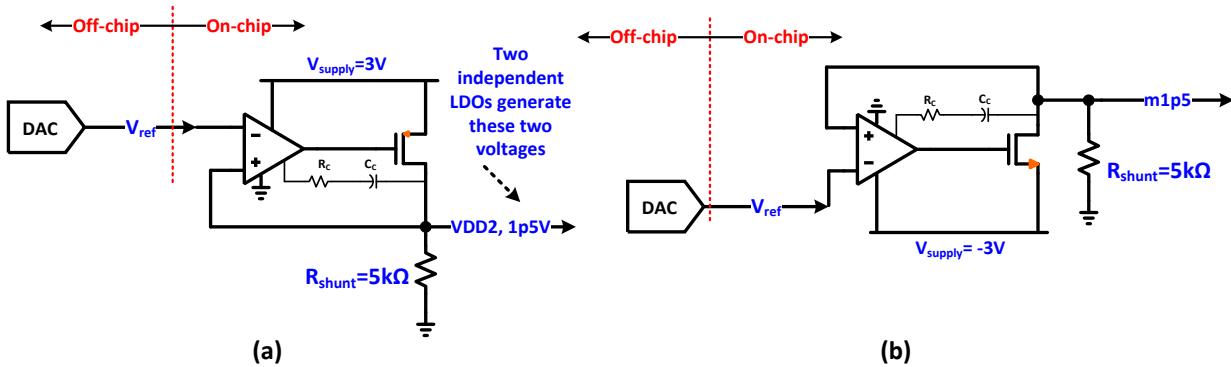


Figure 16. (a) LDO schematic for generating positive programming voltage, VDD2 and 1p5V. (b) LDO schematic for generating negative erase voltage, m1p5.

Table 3. LDO design specification

Gain Bandwidth Product	~ 20MHz
Settling time	< 10 μ s
Loop Gain	~ 80dB
GND Current	< 50 μ A
Dropout Voltage	200mV
Output Current	0.5mA (no load) ~ 2mA (full load)
Line Regulation	0.01%
Load Regulation	0.01%
Output Noise	<50 μ V
PSRR	40dB

4.1.8 EEPROM Macro Model

A 256x88 array models the EEPROM core. Each bank is controlled by signals **BS_Bk#[0:87]** and **TL_Bk#[0:87]**. Table 1 summarizes signal conditions generated and coded as following:

```

state_bk0 <=
w_bk0 when
(
    (W1_bk0 /= W0_bk0) and
    (TL_bk0 = x"000000000000000000000000")
) else

```

```

e_bk0 when
(
    (W1_bk0 = x"00000000000000000000") and
    (W0_bk0 = x"00000000000000000000") and
    (BS_bk0 = x"ffffffffffffffff") and
    (TL_bk0 = x"00000000000000000000")
) else
r_bk0 when
(
    (W1_bk0 = x"00000000000000000000") and
    (W0_bk0 = x"00000000000000000000") and
    (BS_bk0 = x"ffffffffffffffff") and
    (TL_bk0 = x"ffffffffffffffff")
);

```

The above code is repeated for each bank. When write operation signal condition is met, **w_bk#** is high. When erase operation signal condition is met, **e_bk#** is high. When read operation signal condition is met, **r_bk#** is high. The modeled EEPROM array is written, read, and erased based on **w_bk#**, **r_bk#**, and **e_bk#** status respectively. The following code shows memory operations based on control signals.

```

prom_bk_one: process(data_ecc, ADDR_CNT, n_encode, clock)
begin
    if(clock'event and clock='1') then
        if(state_bk0 = w_bk0) then
            prom_bk0(to_integer(unsigned(ADDR_CNT))) <= data_ecc;
        elsif(state_bk0 = r_bk0) then
            data_out_ecc_bk0 <=
prom_bk0(to_integer(unsigned(ADDR_CNT)));
            databar_out_ecc_bk0 <= not
prom_bk0(to_integer(unsigned(ADDR_CNT)));
        elsif(state_bk0 = e_bk0) then
            for i in 0 to 15 loop
                prom_bk0((to_integer(unsigned(n_encode)))+i) <=
(others=>'0');
            end loop;
        end if;
    end if;
end process;

```

4.2 Operational Summary and Corners Validation for 256x88bits EEPROM Bank

4.2.1 EEPROM Control Signal Definition and Overview of Operation

Figure 17 represents the functional control of read, write, and erase. The following section presents a summary of the four states of EEPROM operation. Applying 1.5 to 2.5 V to the gate while applying 1.5V across VDS via high voltage switches creates the device

environment to support hot carriers, which then tunnel, trapping in the HfO₂ oxide of the storage pair to achieve write. A bold gate notes thick-oxide switches. Erase is achieved by applying 1.5 at the drain and storage tail while minus 1 to -1.5V is applied to the NMOS storage gates resulting a 3V drop from V_{GD} - V_{GS} to remove trapped charges from the HfO₂ gate oxide. Observe that the storage pair are in accumulation where V_S≈V_D. Read is accomplished by biasing the storage pair gates at 500 to 600mV with the differential storage pair sources pulled to V_{SS} by the thick-oxide NMOS creating a grounded or tailless differential pair. Due to trapping on one of the devices, storage pairs or the other ("1" or "0") resulting pair currents will mismatch by design supporting the retrieval of the stored "1" or "0". Reliability depends on a first order residual trapped charge being greater than storage pair mismatch. This is due to the greater device areas used in the sense structure. Observe that the left and right thick-oxide pairs control the present state of hot carriers storing a "1" on the right and "0" on the left by definition. The left high voltage level shifters buffer and the two thick-oxide NMOS and PMOS devices form a three-state steering circuit. The three-state operation applies the voltages for read (500 to 600mV), write (1.5→2.7V), and erase (0 to -1.5V). The EEPROM I/O and control signals are defined below:

Power Supplies

- **VDD/VSS** – core power 0.8 to 0.9 Volts
- **VDD1V5** – High voltage logic and level shifter power. VDD1V5 is intended to be DAC programmable from 1.5 to 1.8V in 2 mV steps and aids in supporting both Write and Erase. Beyond the research effort, the VDD1V5 is to be set at 1.5V. This supply is an integral part of erase and write.
- **VDD2** – Programing (Write) voltage and Read voltages – programmable in 1mV steps from 0 to 1V for Read and 1.5 to 2.5V (1.7 to 2.7V for testing) in 1mV steps for the write. In the write operation, VDD2 is expected to accommodate process variation across a 2 to 2.5V.
- **m1p5V** – Supports or completes the Erase operation and is programmable in 1.5mV steps and nominally V_{SS} to -1.5V nominal (to -1.8V for testing). The sum or VDD1V5 minus m1p5V develops an erase voltage less than minus 3.3 while projected usage is expected to be in the range of minus 2.5 to 3 volts.

Signals –

Where the schematic and layout utilized a different naming convention the difference is noted by (XX).

- **BS** – provides an EEPROM Bank Select function used in the read operation ONLY.
- **SE** – latches Sense Amplifier data into a D-flip flop register contained within the EEPROM wrapper on its rising edge. The time of this pulse is controlled by the EEPROM wrapper.
- **Data<0:87>** and **Data_bar<0:87>** are EEPROM bank word data output bits.
- **WorErsE/(WorErsE_bar)** (Synthesized as TK see Figure 10)– indirectly apply 1.5V to the storage pair tail (full word or all bits) during both W and Erase operating modes while serving as a bank select in these modes.

- **R/(R_bar)** (Synthesized as TK see Figure 10)– Grounds the storage pair tail (full word all bits) for the data read operation.
- **A<0:255>/A_bar<0:255>** selects one of 256 words to be Read or written from the 256 words x 88-bit bank.
- **Ers<0:255> (Ers_bar<0:255>)** (ER<0:255> (ER_bar<0:255>)) – selects one of 256 or a 16 words block (consecutive words) of 256 words to be Erased.
- **A<0:255>/A_bar<0:255>** and **Ers<0:255> (Ers_bar<0:255>)** are applied mutually exclusively, Figure 16, to avoid storage device destruction.
- **W1<0:87>** and **W0<0:87>** control the bit storage within each bit of the 88-bit word when writing. **W1** and **W0** must be mutually exclusive to avoid writing both sides of the storage pair. **W1<n>** being a logic “1” defined the storing of “1” at word location, n, while **W0<n>** defined the storing of “0” at word location, n, Figure 17.

4.2.2. EEPROM Control

The EEPROM has four functional states; Idle, Read, Write, and Erase. Core VDD and high voltage logic VDD1V5 are always ON and nominally 800mV and 1.5V. The design avoided setting VDD1V5 to 1.8 V to minimize stressing the high voltage read and write transistors. VDD1V5 is used in the control of all read/write/erase operations. To save or minimize power, pull down all HV voltage EEPROM supplies (non-Core) down in the “idle” mode. Figure 17 schematically presents memory cell write, read, and erase operation in detail.

Simply stated **Ers<0,255>/Ers_bar<0,255>** applies m1p5V (-0.5 to -1.5V for erase) to the storage gates while **A<0,255>/A_bar<0,255>** apply **VDD2** (The VDD2 ranges are 500mV to 2.7V for read and write.) to the gates of the selected word. **A<n>** and **Ers<n>** must never be true at the same time to avoid shorting **VDD2** to **m1pV**. Both may be OFF while only one may be ON creating a 3 state supply mux at each row select point. By example, row select supports 1) 2.5V or VSS on the word **RS** gates for writing or not writing in the write mode respectively and 2) 0.6V or VSS on the word **RS** gates for reading or not reading a word and 3) m1p5V (-1.5V) and VDD on the word RS gates for erasing or not erasing. When writing or reading **m1p5V** is at VSS and when erasing **VDD2** may take on values of VSS to VDD, in Figure 17. The HV power application circuit is at the left in Figure 17 while the four storage cells at the right present the storage cell setup in the idle, write, read, and erase moving counter clockwise around the figure. The bold gate identifies thick-oxide transistors. The two outside NMOS devices control writing (1 or 0) while the P and N pair (left side) control the application of Read, Write and Erase voltages to the storage device gate. The four thick-oxide devices setup precursor conditions for write/read/erase while the 3 state structure applies the primary condition to complete read, write, or erase on the selected word(s). ONLY these 4 are needed for any column or restated to implement a 1Kx88 word bank only requires 892 (4x88+ 2x256) thick-oxide transistors plus 512 minimum geometry level shifters. In summary, when writing or reading the VDD2 voltage is applied to RS of the selected word and m1p5 equal VSS is applied to RS of the unselected words by **Ers<0,255>/Ers_bar<0,255>**. When erasing, the m1p5 voltage is applied to RS of the selected word and VDD2 equal 600mV is applied to **RS** of the unselected words by **A<0,255>/A_bar<0,255>**.

keep all high voltage supplies at VSS when not in use. VDD2 takes on two roles, supplying the write, 1.5 to 2.5V and read 600 to 700mV voltages. VDD2 will take on a range of voltages from 0 and 2.5V and for research purposes up to 2.7V. When writing or erasing, 1.5V is applied to the memory sense node (**MemS**) *common to all storage tails* for a bank. **WorErsE/WoErs_bar**, controls the application of 1.5V to the tail, see Figure 18. See Figure 10 as well. In the read R/R_bar ground the storage pair tail, in Figure 19. Notice the "HV_W_R_Ers_logic_Array_Col" cell at the left controls word selection for the Write/Read and Erase operations. The right block includes the storage array (center), sense amps (top) and HV circuits to setup the write, reading and erase of each word (bottom). The bank is approximately 65um x 250um and a one to one relationship exists between the layout and schematic blocks. Care in switching **VDD2** and **m1p5V** is necessary to avoid destroying the thick-oxide devices or thin-oxide memory devices, stressing damages, or limits lifetime. The intention in operating or testing is to switch only a single supply voltage at any time. *This avoids the overlapping of power control and shunt currents.* In addition, an active state of read, write, or erase are entered from idle mode ensuring safer starting point in operation with less likelihood of an overlap error. Active state exit is handled in a similar manner, one supply change per wrapper clock with delays to account for supply quenching.

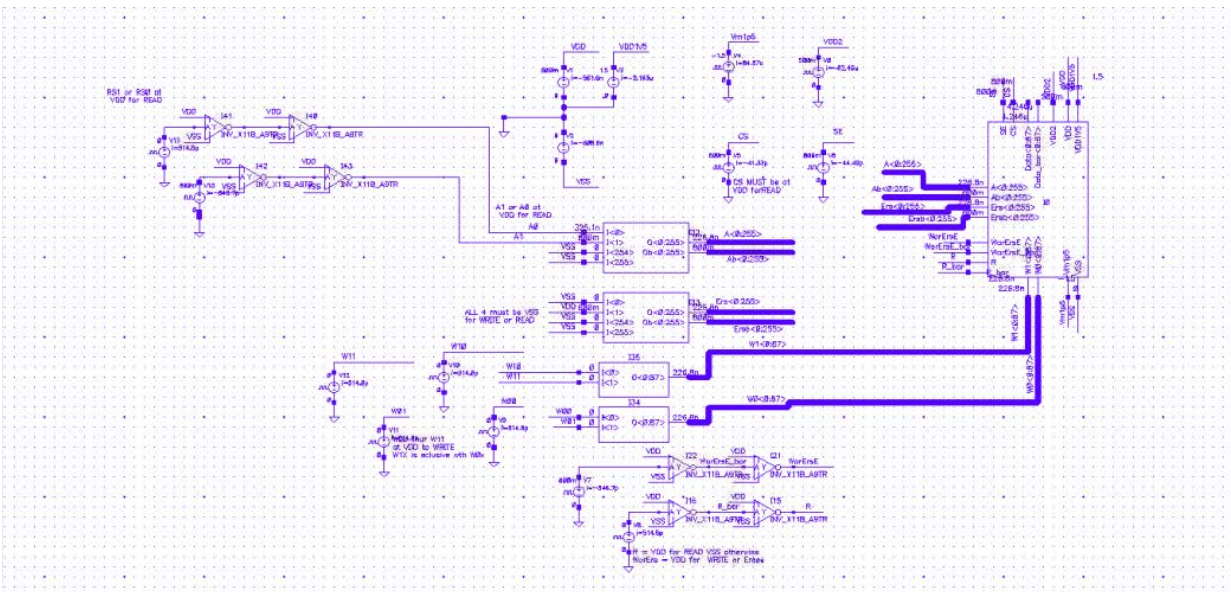


Figure 18. EEPROM bank test bench with EEPROM bank on the right.

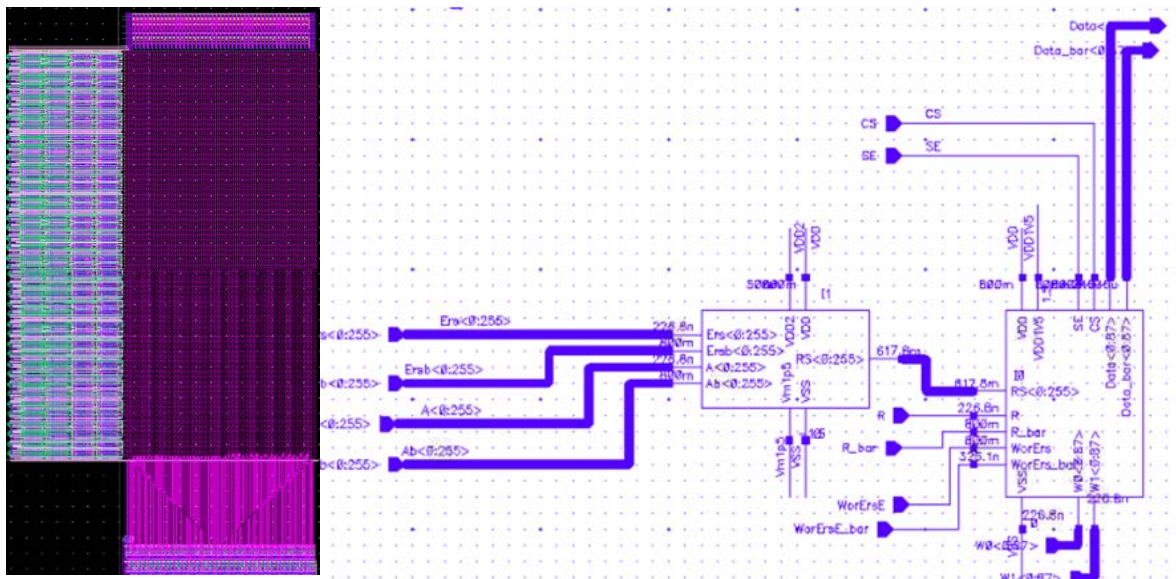


Figure 19. EEPROM Bank Level one.

Idle - As long as both VDD2 and m1p5V equal 0V the application order of the remaining control signal is not critical. Timeliness to enter the idle state saves power.

1. **Voltages VDD2 is set to VREAD = VSS, m1p5V = VSS**
2. **WorErsE (WorErsE_bar) → VSS/VDD (0/1)**
3. **W1<0:87> and W0<0:87> all held at VSS, always at VSS unless write is taking place.**
4. **R /(R_bar) → VSS/VDD (0/1)**
5. **A<0:255>/ (A_bar<0:255>)- selects one of 256 words to be Read → VSS/VDD (0/1)**
6. **Ers<0:255>/ (Ers_bar<0:255>) – selects one of 256 or a 16 words block or 256 words to be Erased. → held at VDD/VSS or FF/00.**
7. **BS → VSS**
8. **SE ↓↑ pulse held at VDD**
9. **Data<0:87> and Data_bar<0:87> are Bank word data latched in rising edge of SE. Output held at VDD internally by BS signal.**

4.2.4 Read Validation

The currents and voltages for a simulated storage cell (programmed) read are shown in Figure 20 where the residual programmed voltage is modeled by using SVT transistor to represent a programmed HVT with an approximately *100mV differential voltage resulting in 30uA/44uA of differential (Vg =500mV/600mV) cell current*. Time, temperature dependent loss and storage cell mismatch degrade the initial stored threshold shift value, 150 to 250mV. Total nominal I_{off} for the storage cell is 1uA at 50C and 3uA at 90C (PDK 63uA at 85°C) per bit line. A first order read will be unaffected by bit line leakage but does set the maximum words per column. When reading one of 256 data storage pairs, the storage pair to be read is controlled RS and it is applied

(application of 600mV to **RS<n>**) and functionally ANDed with **BS**. **BS** is enabled in the cross coupled sensing load, Fig 21 forming a regenerative sense amp. Data pair selection is achieved by the application of **A<0:255>/ (A<0:255>)** where A<0:n> selects the word storage pair, **RS<n>** currents to be applied to the column sense amps. Active control signal sequence are summarized in order from the idle thru read below in detail. Extracted loading is tabulated below along with blue highlights indicating the active signal pin functions.

1. Voltages VDD2 is set **VREAD = 0.6→0.7V, m1p5V = VSS**
2. WorErsE (WorErsE_bar) → VSS/VDD
3. W1<0:87> and W0<0:87> all held at VSS
4. R /(R_bar) → **VDD/VSS**
(The Proceeding signals and VDD2 must be stable before applying A/A_bar!)
5. A<0:255>/ (A<0:255>)- selects one of 256 words to be **Read → VDD/VSS**
Active Read signal is applied by A<n>/A_bar<n> pulling up RS<n> via the PMOS while the Ers<n>/Ersbar<n> turns off the NMOS pull down device. n takes on the value of the word being written.
6. Ers<0:255>/ (Ers_bar<0:255>) – selects one of 256 or a 16-word block or 256 words to be Erased. → VSS/VDD or 0/F. Ers<0:255>/ (Ers_bar<0:255>) of the words that is not erasing hold the NMOS pull down device OFF. Corresponding row selects are pulled to VDD by PMOS pull-up device. The words being erased **Ers<n>/Ersbar<n> turns on the NMOS device** pulling RS<n> to erase voltage, -1.5V.
7. **BS – VDD** (may be applied prior to or with or after A<0:255>/ (A<0:255>)
8. SE **↓↑ pulse** post sense amplifier settling delay. A 2us delay of the pulse or a 2us ensures valid data across all corners.
9. Data<0:87> and Data_bar<0:87> are **Bank word data is latched on the rising edge of SE.**

Table 4. Read setup

Supply Voltages			Comment
VDD2	600mV+/-100mV	Nominal	Programmable 000→1.50V
m1p5V	0V	Must be at 0V for Read & Write	Programmable 000→ -1.50V
Control Signals			
BS (57fF)	1	Bank Select	Core logic controlled
SE (125fF)	↓Pulse	Data latched on ↓	Core logic controlled
WorErsE/WorErsE_bar (0.8fF)	0/1	Deselected	Core logic controlled
R/R_bar (0.98fF)	1/0	Selected	Core logic controlled
A<0:255>/Ab<0:255> (7.2fF)	Active	Word Select	Core logic Read or Write Word select controlled
Ers<0:255>/Ersb<0:255> (7.0fF)	0/1	Deselected	Core logic Erase Word controlled
W1<0:352>/W0<0:352> (0.95fF)	0/0	Deselected	Core logic controlled
Output			
Data <0:352>/Data_b <0:352> (1.35fF)	Active		Active Latched (buffered Latch) Data lost on rising edge

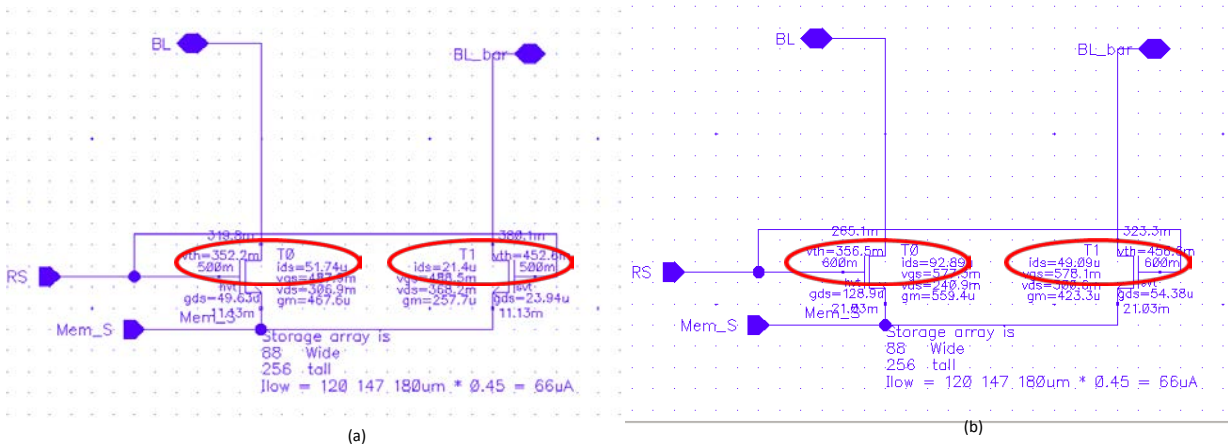


Figure 20. Programmed Storage Cell a) VDD equal 500mV and b) 600mV with modeled "Written" Voltage and Currents modeled by use of an SVT transistor $\Delta V = \approx 100\text{mV}$

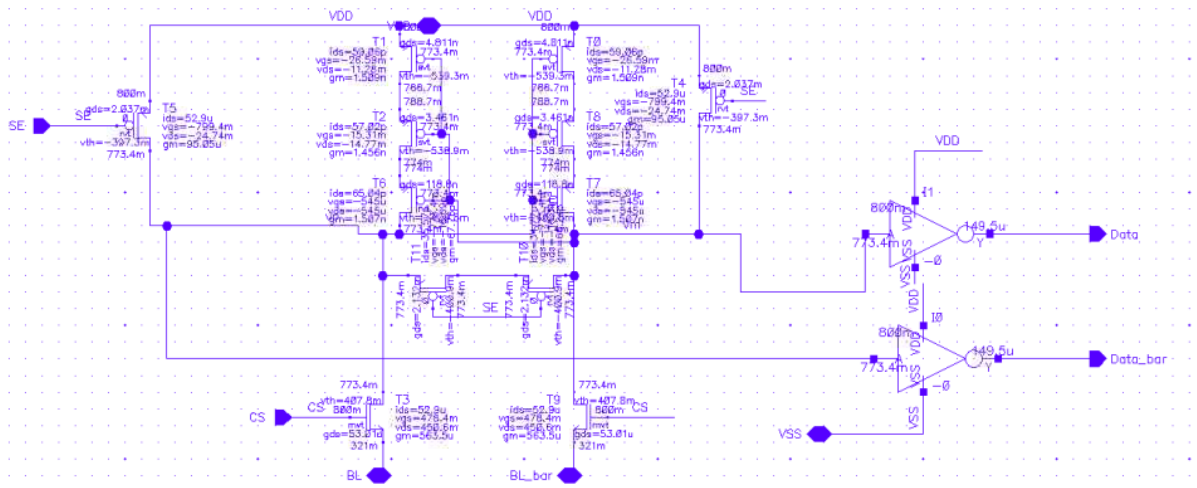


Figure 21. Storage Cell sense amplifier where the differential pair of the sense amp is the storage cell.

4.2.5. Write

Figure 22 shows the write conditions on the storage cell while in Figure 23 demonstrates validated transient circuit behavior, RS and MemS equal 2.5V and 1.44V_S respectively. The 1.5V applied to the storage tail with VDD2 applied at the gates (RS) results in an active hot carrier current path way provided by write activation signals W1/W0 resulting in trapped charge on the selected gate. The 150mV drop is across the thick-oxide tail switch that is a result of “hot” write currents. The application of A<0:255>/ (A_bar<0:255>) selects the word to be written (application of VDD2 to the gates of the selected word). While W1<0:87> and W0<0:87> set the conditions to program the selected storage transistor and in turn the data pattern to be written in the selected word. Setting W1 to VDD raises the left storage transistor threshold, typically by 200mV while setting W0 to VDD will raise the right transistor threshold equivalently. The reader is referred back to circuit of Figure 17 to observe the high voltage three state structure used to apply the desired programming conditions. Observe in Figures 11 and 12, VDD2 (2.5V) is applied to gates of the storage cells while the application of W1/W0 (VDD/VSS) results in a 250uA shift of device drain current providing the source hot carriers (electrons) desired to positively shift the threshold. Hot carrier and damage occurs on the storage pair tail. The write protocol sequence is tabulated below;

1. Voltages VDD2 is set to a Voltage write value equal 1.5 to 2.5V, and m1p5V equal VSS
2. BS – VDD (applied with WorErsE / WorErsE_bar)
3. SE – VDD (applied with WorErsE / WorErsE_bar)
4. WorErsE (WorErsE_bar) → VDD/VSS Applies 1.5 volts to all bank tails and serves as the bank select during bank erase/write. *Duration TBD.*
5. W1<0:87> and W0<0:87> All 88 set to VDD/VSS (VSS/VDD) as word storage dictates.

6. $R/(R_bar) \rightarrow VSS/VDD$
(Proceeding signals and VDD2 must be stable before applying A/A_bar!)
7. $A<0:255>/ (A_bar<0:255>)$ - selects one of 256 words to be Written $\rightarrow VSS/VDD$.
Followed by a programming delay. **All nonelected word storage gates are pulled VSS by $Ers<0:255>/(Ers_bar<0:255>)$.**
8. $Ers<0:255>/(Ers_bar<0:255>)$ – selects one of 256 or a 16 words block or 256 words to be Erased. $\rightarrow VSS/VDD$ or 0/F.

Table 5. Write setup

Supply Voltages			Comment
VDD2	1.5→2.5	Nominal	Programmable 000→2.70V
m1p5V	0V	Must be at 0V for Read & Write	Programmable 000→ -1.50V
Control Signals			
BS (57fF)	1	Bank Select Active↑	Core logic controlled by EEPROM wrapper
SE (125fF)	1	Inactive Held at VDD	Core logic controlled by EEPROM wrapper
WorErsE/WorErsE_bar (0.8fF)	1/0	Selected	Enable write of desired bank. Supplies 1.5 to cell tail.
R/R_bar (0.98fF)	0/1	Deselected	Core logic EEPROM wrapper controlled
$A<0:255>/Ab<0:255> (7.2fF)$	Active	Selected	Core logic EEPROM wrapper select of word to be written
$Ers<0:255>/Ersb<0:255> (7.0fF)$	0/1	Deselected	Core logic controlled
$W1<0:352>/W0<0:352> (0.95fF)$	0/1	Deselected	Core logic controlled
Output			
Data <0:352>/Data_b <0:352>	In Active	Held at VDD	

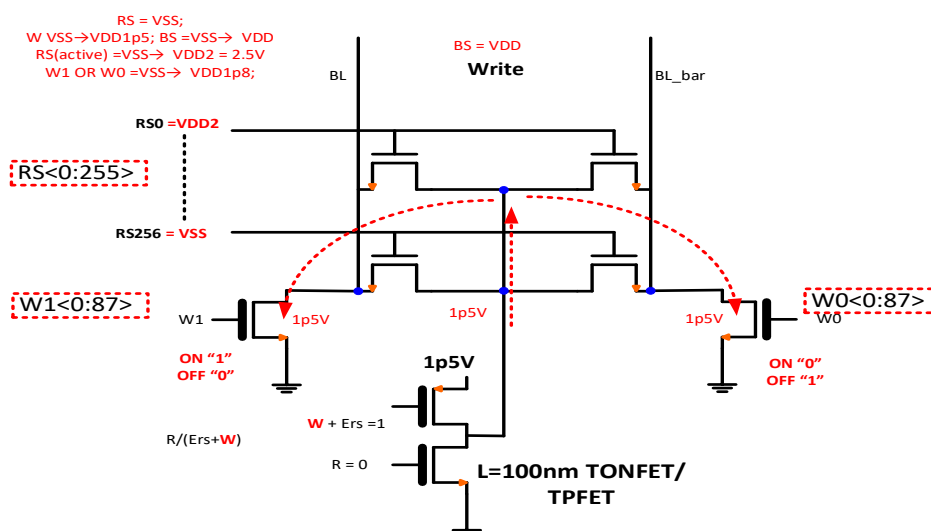


Figure 22. Storage Cell "Write" Voltages applied to gate and resulting currents flow paths.

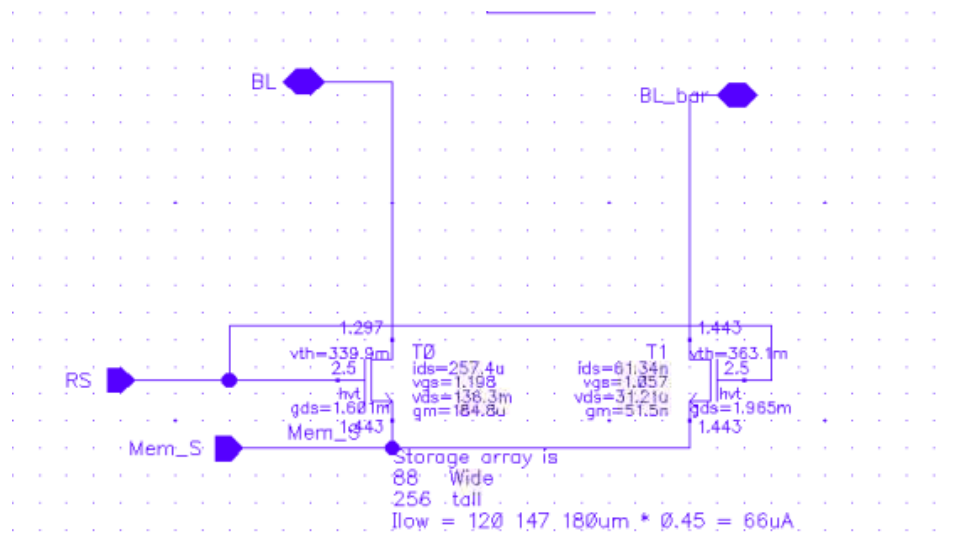


Figure 23. Storage Cell “Write” Voltage and Currents. Note gate and storage pair tail voltages and 257uA drain current in the transistor to be programmed.

4.2.6 Erase

Figure 24 annotates the erase conditions on the storage cell while valid circuit behavior demonstrated in Figure 25. Again, the reader is referred back to circuit of Figure 17 to observe the high voltage three state structure used to apply the desired programming conditions. The application of **WorErsE/(WorErsE_bar)** applies 1.5V to all storage cell tails, Figs. 12 and 13 while serving as the bank select function when writing and erasing. The application of **Ers<0:255>/(Ers_bar<0:255>)** causes -1.0 to -1.5V to the gates of the selected word(s). This results in up to -3V being applied across the gate to source to remove trapped charge from the gate oxide of the storage cell transistor pair. Erase protocol is outlined below, summarized, and tabulated as follows.

1. Voltages **VDD2** is set **VREAD = 0→0.6V OR VDD** and **m1p5V** i.e -1 to -1.5V
2. **BS** and **SE** are set to **VDD**
3. **WorErsE/(WorErsE_bar)** set to **→ VDD/VSS**: This applies 1.5V to ALL storage cell tails.
4. **W1<0:87>** and **W0<0:87>** all remain at **VSS** and are inactive
5. **R /(R_bar)** **→ VSS/VDD** in active
6. **A<0:255>/ (A<0:255>)**- proper selection sets ALL word(s) NOT to be Erased **→ (VSS/VDD) to VDD2** to all storage gates to be erased **applying VDD2 (equal 0.6V) to all gates not to be erased**. **VDD2** held off from being applied to any of the 256 **RS** pins to be erased and **m1p5V** held off from all 255 **RS** pins. All proceeding signals and voltages and in particular **m1p5V** must be stable before applying **Ers / Ers_bar**.
7. **Ers<0:255>/(Ers_bar<0:255>)** – selects one of 256 or a consecutive block of 16 words of 256 words to be erased. **→ VDD/VSS** or **F/0** controlling the application of -3V across the storage word pairs to be erased. The table below further

tabulates EEPROM signal control and loading along with signal function.
Duration TBD.

Table 6. Erase setup

Supply Voltages			Comment
VDD2	0→0.8V	Nominally 600mV	Programmable 000→2.70V
m1p5V	VSS, -1.2 → -1.5V	Nominal 1.5 -(-1.2→-1.4V)	DAC Programmable 000→ -1.50V
Control Signals			
BS (57fF)	1	Switched to VDD	Core logic controlled
SE (125fF)	1	Held at VDD	Core logic controlled
WorErsE/WorErsE_bar (0.8fF)	1/0	Selected	Core logic controlled Enables erase of desired bank serves as bank select
R/R_bar (0.98fF)	1/0	Deselected	Core logic controlled
A<0:255>/Ab<0:255> (7.2fF)	Inactive	Deselected	Core logic controlled Removes VDD2
Ers<0:255>/Ersb<0:255> (7.0fF)	1/0	Word or 16 Words Selected	Core logic controlled Selects word(s) to be erased by applying m1p5V
W1<0:352>/W0<0:352> (0.95fF)	0/0	Deselected	Core logic controlled
Output			
Data <0:352> / Data_b <0:352>	In Active		Active Latched (buffered Latch)

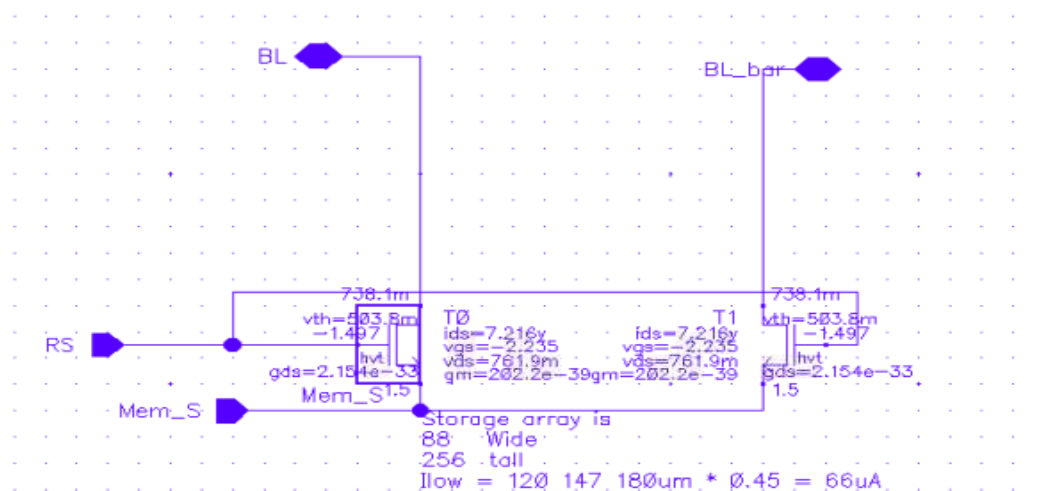


Figure 24. Storage Cell “Erase” Voltage (e.g. -3V = VGS) and Currents. Note gate and storage pair tail voltages.

- In Active signals
 - o W1<0:87>/W0<0:87>, VDD to program the desired word bits. See W10, W00, W11, and W01 of the purple block
 - o Erase generator blue block

PER sets the write cycle of frequency and the fraction of PER (i.e. $0.5 \cdot \text{PER} = \text{PW}$ is the active cycle fraction), in an alternate example PER is $10 \cdot \text{Per}$ and $\text{PW} = 5 \cdot \text{PER}$. By changing PER, all signals remain relative to each other. Doubling PER halves the read rate and vice-versa. Typical-typical (TT) read transient at 50 C and VDD equal 800mV can be observed in Fig. 26, from which one can observe 1) read is initiated by the present state of BS, the read condition and A<0>, *an initial condition of 56 to 99mV (senses structure input) is settled in less than 30-60nS. The logic value is valid less than 30nS following the rising edge of SE to be latched on the falling edge of SE. Total read time BS to the rising edge of SE is less than a 100nS exclusive of the HV level shifter delay. See Figs. 15 - 18 and Tables 1 - 3 for greater detail. The 3 sigma (2 sigma) mismatch of the combined storage cell and sense structure is less than 54mV(36mV) leaving 45mV(20mV) initial condition to set the settling time and resolve the stored value. Approximately 1/3rd of the initial threshold shift, 150mV is lost to thermal charge loss over the oxide barrier, sensing offset (cell offset, and sense amp offset), leaving an effective read voltage approaching 50mV. While 50 mV of the initial storage cell write is lost to shallow trapping in the SiO₂ interface layer. A loss of 50% of the effective read voltage increases read time by 44%. In this application, this is a minor consequence.*

The SS corner is of concern at sigma -3 (while -2 to +2 sigma will be more than sufficient for concept validation.), temp 0, and VDD: 720mV. The TT or nominal read response from the test bench is presented below in Figure 26 where the signal of interest (See Table 1) are as follows;

1. Bank Select in red is valid the full read test cycle, approximately 3uS across 720 to 900mV.
2. A<0,1> in orange and yellow the active signal selecting word 1 and 2 in the design respectively. Valid for the period required to retrieve the storage word being read, typically less than 1uS per read.
3. RS lines in blue and red (net<60<1> and net60<0>) apply the storage cell currents the regenerative sense structure making up the sense amp.
4. The BL difference net35<1> minus net 35<0> and net36<1> minus net 36<0> is the voltage value applied to the regenerative sense circuits. *The approximately 50 to 90mV initial condition results in a 20-40nS settling at the -3 sigma, 800mV, 50C corner.* This affirms that read times delays are in effect set by the HV level shifters not by sense amplifier settling or D-flip flop setup and hold times.
5. Data and data_bar (purple and yellow) (net35<0> & net34<0>) and white and brown (net35<1> & net34<1>) bit 0 of word 0 and bit 1 of word 0.

Read time is limited by the rise and fall times, Figure 29, of the HV level shifters used to apply gate voltages to the storage cell which are VDD to 2.5 V and VDD to -1.5V, Figure 17. At the worst case functioning corner; VDD =720mV, -3 sigma, and 50C corner

the HV or thick-oxide level shifter contributes 1.2 μ S to read delay versus a 30nS setup and convergence delay for the sense amp. Resizing the level shifter by an additional 3X will reduce read delay of this SS corner while increasing the HV row select logic area by 2X. It is not clear at this time that the overall benefit (reduced to 400nS) is worthwhile given core logic delays and sense amp delays are in 10s of nS. RS to valid Sense Amp delays (initial condition and settling Figure 28) are less than 20 to 40nS. *Read times are bound by the HV thick oxide level shifters but most importantly fast infrequent read have little impact on processor performance.* Finally, it should be noted that the lever shifter passes worst case corner as a standalone logic driven when logically loaded cell but not when tested as a part of the full EEPROM block. Thin-oxide level shifter circuits topologies exist, while being faster and more compact they are significantly more complex. This is recommended as the final solution due to its greater compactness and read performances in the 50 to 70nS range. Given the desired read times, the value of such a modification would be in reduced area and power. See Figure 17 to identify the locations of the problematic level shifters.

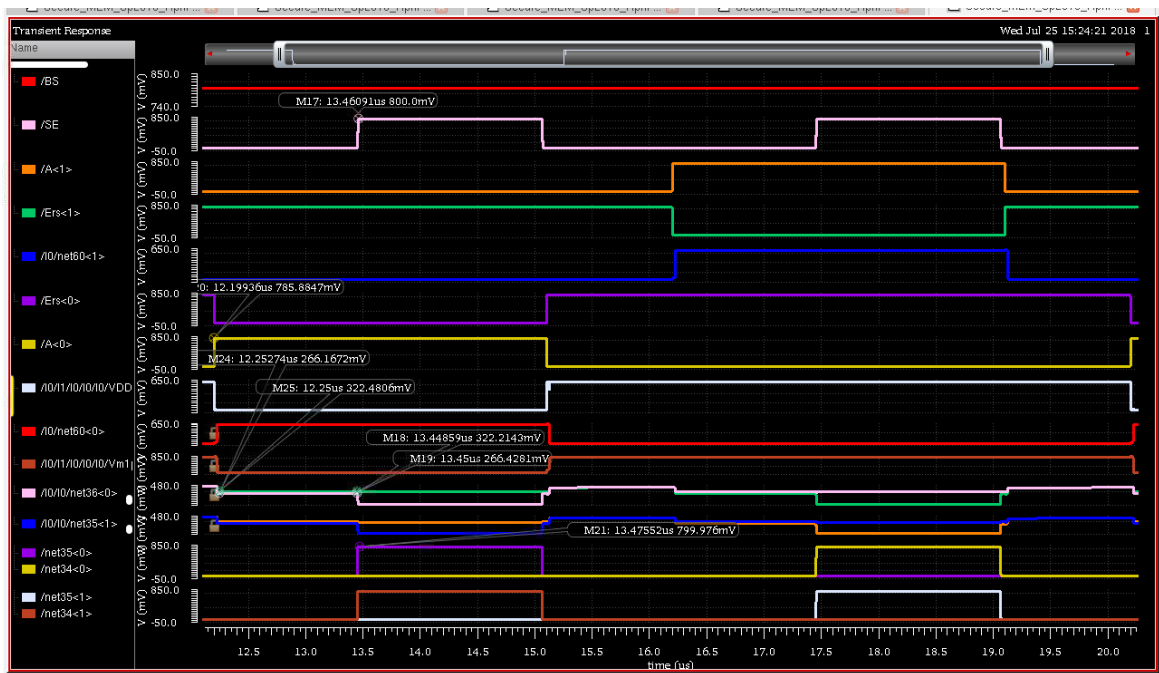


Figure 27. Typical Read test bench transient.

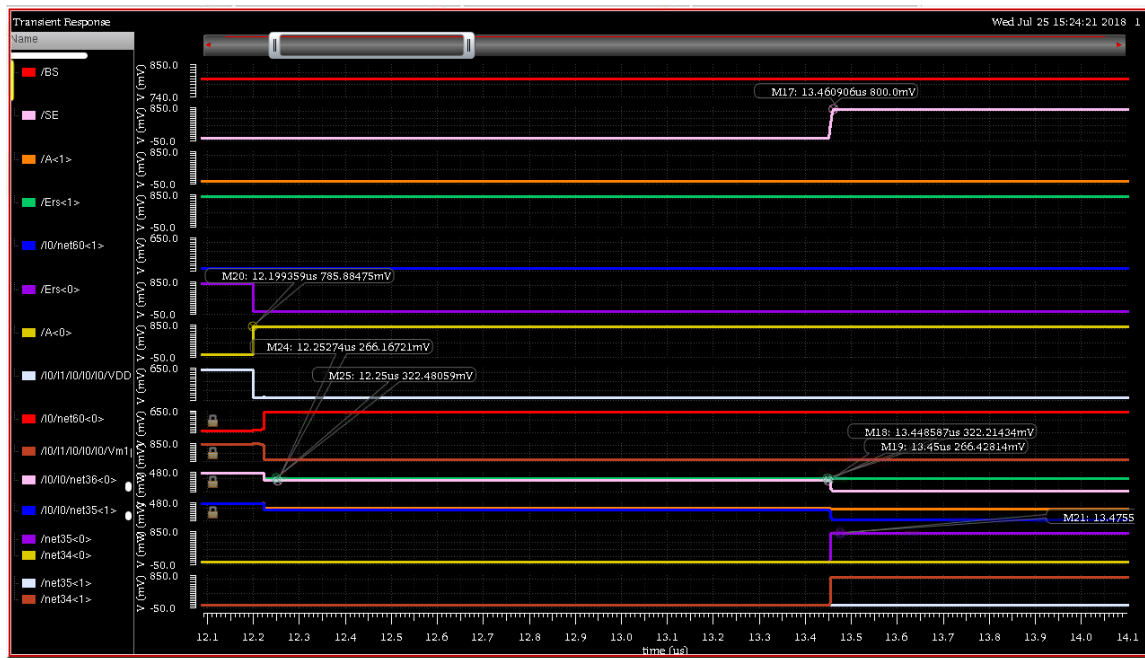


Figure 28. Expanded view of Figure 27.

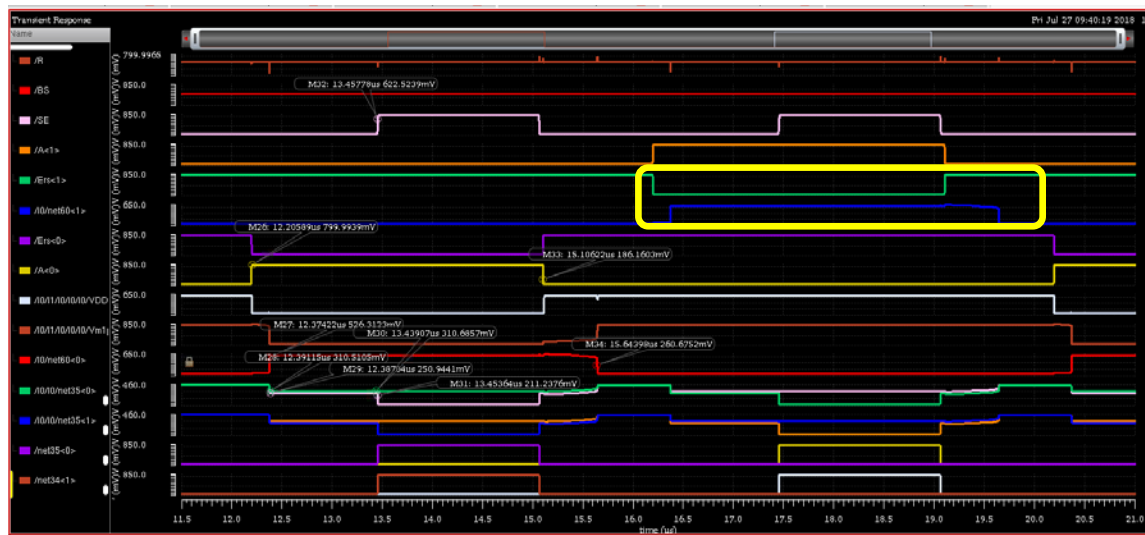


Figure 29. Read test bench transient temp = 50C, sigma = -3, and VDD = 800mV illustrating the delay associated with level shifter delay.

4.2.9 Write and Erase Corners

The write and erase corners are VDD: 720, 800, and 900mV, Temp: 0, 50, 90C; Sigma: 3→0→3 are for the write tests 1) VDD2 takes on 1.5V and 2.5V and 2) erase m1p5 equals minus 1.5V for a erase voltage of 3V.

Setup is as follows:

- Control Signals - Write W equal VDD, Erase equal VSS, **W1<0:87>** and **W0<0:87>** are set to VDD as word storage dictates. Observe that in the test

bench $W1<0> = W10$, $W0<0> = W00$, $W1<1> = W11$, $W0<1> = W01$ are controlled by parameters $W10$, $W00$, $W11$, $W01$ and $Wxx_DC = VDD$, and $WorErs = VDD$. $VDD2$ maybe set between 1.5 and 2.5 as a practical matter for observing an interleave write of any two bits of any word.

- For the purpose of the test bench, the remainder of $W1<2:87>$ and $W0<2:87>$ are hard coded in the test bench to alternating 1's and 0's.
- Bank Select $BS = VDD$, Sense Enable $SE = VDD$. *BS and SE only function in the read mode.*
- Each bank has a $WorErsE/WorErsE_bar$ that takes on the role of bank select for each bank when in the **Write** or **Erase** mode.
- Read (R_bar) and $WorErsE$ functions are controlled by R_W and Erase generators (outlined in blue).
 - o **For the Write** corner $VDD2$ is set at 1.5 and 2.5V while the application of $A<0:255>/A_bar<0:255>$ selects one of 256 words to be Written → VDD/VSS . For the future, it is deemed as unnecessary.
 - o **In Erase**, $m1pV$ is set between 0 and -1.5V while the application of $Ers<0:255>/Ers_bar<0:255>$ – selects one of 256 or a 16 words block or 256 words to be Erased. → For write mode set to VSS/VDD or 000/FFF.
 - o $A<0:255>/A_bar<0:255>$ or $Ers<0:255>/Ers_bar<0:255>$ are the last signals applied and are always mutually exclusive. When writing, the words not being written (RS not at $VDD2$) are held at VSS . Likewise, when erasing the word(s) not being written (-1.5 at RS) at held at 600 to VDD . When writing, all RS pins are held at VSS then word being written $RS<n>$ is placed in the high impedance state and then pulled to $VDD2$, 1.5 or 2.5 in this corners testing. The idea is to avoid the moment that both the PMOS and NMOS devices are ON and creating short path between $VDD2$ and $m1p5$ supplies, reference Figure 17. While erasing, all RS are initially at $VDD2$ i.e. 600mV and the word(s) to be erased are placed in the high impedance state then pulled to $m1pV$ i.e. -1.5V. When writing, $Ers<0:255>/Ers_bar<0:255>$ is applied first followed by $A<0:255>/A_bar<0:255>$, while erasing the opposite order must be followed.

Test Bench Voltages parameters

- $VDD = 800mV$, $VSS = 0$, $VDD1V5 = 1.5V$, $VDD1p8 = 1.5V$
- **Write** --- $VDD2$, $VDD2_r$, $VDD2_w$, $VDD2_DC$, 1.5 to 2.5V continuous. CORNER Write Test are for 1.5 and 2.5V and $m1p5V = VSS$
- **Erase** – $m1p5V = -1.5v$ → $m1p5V_DC = VSS$ and $VDD2$, $VDD2_r$, $VDD2_w$, $VDD2_DC$, 1.5 to 2.5V = VSS
- **PER** - Sets the write cycle of frequency and the fraction of PER (i.e. $0.5 * PER = PW$ is the active cycle fraction), in an alternate example PER is $10 * Per$ and $PW = 5 * PER$. By changing PER, all signals remain relative to each other. Doubling PER halves the read rate. While halving, doubles the read rate and read time. For Write and Erase Per is in 10 to 100s of mS.

4.2.10 Write Corners at VDD = 800mV

The write corners test: temp = 0, 50, 90C; sigma= -3, -2, -1, 0, 1, 2, 3; VDD2 equals 1.5 and 2.5V; and m1p5V equals 0V. The typical write corner; temp 50, sigma 0, and VDD2 equals 2.5V is reviewed below. By way of an example discussion, the TT write corner is reviewed below, Figure 30.

Signals of interest for the “write” corner transient simulations, Figure 30 are as follows:

BS, SE (brown and red, not shown) are at VDD to avoid overvoltage on the core logic devices. **Ers<n>/Ers_bar<n>** are at VSS/VDD and **A<n>/A_bar<n>** VDD/VSS are applied selecting the word to be written. In Ers<0,255>/Ers_bar<0,255> apply the m1p5V at VSS for write (-0.5 to -1.5V for erase) to the gates while A<0,255>/A_bar<0,255> applies VDD2 equal 2.5V or write to the gates (0.6V for read) of the selected word to be written. A<n> and Ers<n> MUST never be true at the same time. The reader is encouraged to reference Figure 16. The 88-bit word applied to A<n>/A_bar<n> is complement of Ers<n>/Ers_bar<n>, e.g. 80/7F.

The application of A<1> in pink applies Row Select (net60<1>) in green or 2.5V to all gates of the selected word storage cells to be written. It can be observed that application of A<0> in purple applies Row Select (net60<0>) in brown or 2.5V to all gates of the selected word storage cells to be written. ErsE/ErsE_bar applies 1.5V to the tail of all storage cells (In read storage cells sources while in write this becomes the drains of the two storage devices.) When writing W1<1>/W0<1> (red/brown) and W1<0>/W0<0> (pink/orange) are applied to BL<0> and BLbar<0> (net35<0>/net34<0>) and BL<1> and BLbar<1> (net35<1>/net34<1>). Note that when writing (2.5V applied) net35 and net34 have an approximate 200mV difference.

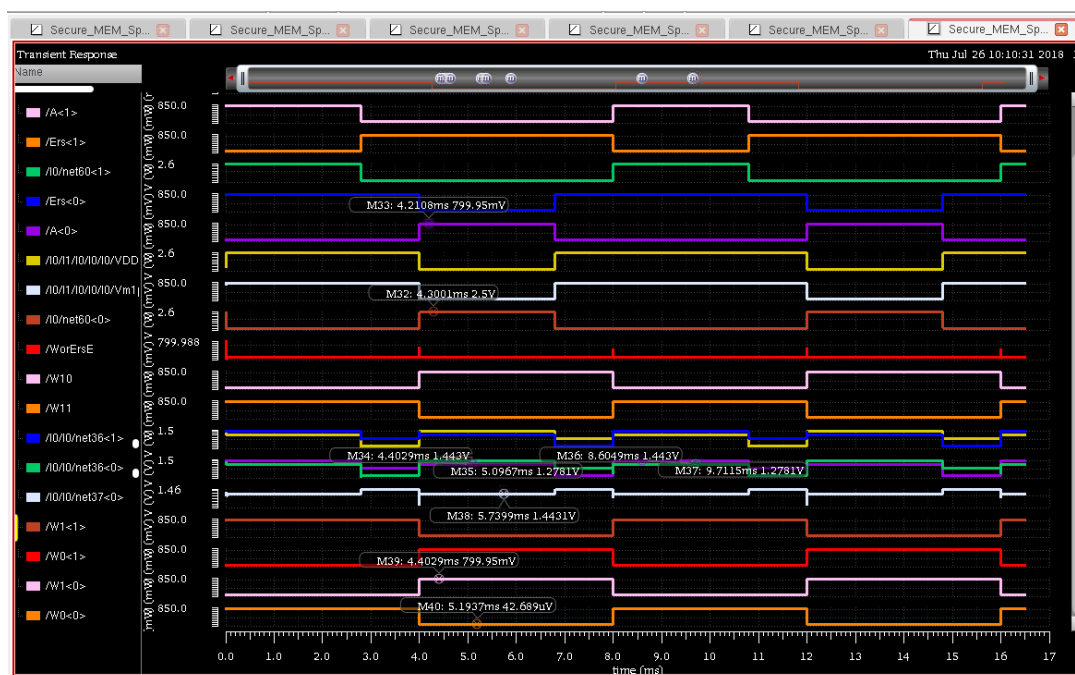


Figure 30. Write Corners TRAN VDD = 0.800V, 3sigma, 0C VW 1p5V.

4.2.11 Erase Corners at VDD = 800mV

The erase corners are summarized as follows: temp = 0, 50, 90C; sigma=-3→, 0, →3; VDD2 equals 720mV, 800mV, 900mV and m1p5V equals -1.5V. The TT corner is temperature 50, sigma 0, VDD = 800mV, m1p5V equals -1.5 and VDD2 equals 0.6V is presented.

Signals of interest for the “erase” corner transient are as follows:

BS (brown), SE (Red) are at VDD to avoid over voltage on the core logic devices (exclusive of the gate to source storage pair).

A<n>/A_bar<n> are at VSS/VDD for the word(s) NOT being erased when Ers<n>/Ers_bar<n> VDD/VSS are applied selecting the word(s) to be erased. For the words being erased and A<n>/A_bar<n> at VDD/VSS. A<n>/A_bar<n> and VSS/VDD must be the compliment of each other. When actively applying a voltage the other must be off. Ensuring that the application of A<n>/A_bar<n> and Ers<n>/Ers_bar<n> are mutually exclusive avoids shunt currents between the VDD2 and m1p5V in addition to avoiding unsafe over voltages on the storage cells.

The application of Ers<0> in purple applies Row Select (net60<0>) in brown or -1.5V to all gates of the selected word(s) storage cells to be erased. It can be observed that application of A<0> in purple applies Row Select (net60<0>) or -1.5V to all gates of the selected word(s) storage cells to be erased. ErsE/ErsE_bar applies 1.5V to the tail net37(n=0,1 in white & yellow) of all storage cells. When erasing W1<0,87>/W0<0,87> (red/brown) and W1<0>/W0<0> (not shown) are held at zero to isolate the bit lines being written, BL<0,87> and BLbar<0,87> (net35<0,87>/net34<,87>). The storage cell drain and source held at 1.5V and VDS of the storage cells approximately 0V. The gates of the all erased storage cells (the full word) are at -1.5V for erase. During erase, a voltage as large as 3.0V is proposed and while during developmental testing, this can be as great as 3.3V. The 1.5V at the tail net37(n) in white and yellow and -1.5V at net60(n), row select to the gate develop 3 V. M1p5V takes on a range from 0 to -1.5V in 0.75mV steps while having no real effect at VDD1p5 and is expected to be used in the range -1 to -1.5V resulting in an erasure range of -2.5 to -3V. Bit lines i.e. net35 and net34 are at 1.5V since the storage device is effected due to higher channel leakage with their drains open due to W1<0,87>/W0<0,87> being at VSS. The reader should refer back to Fig. 17.

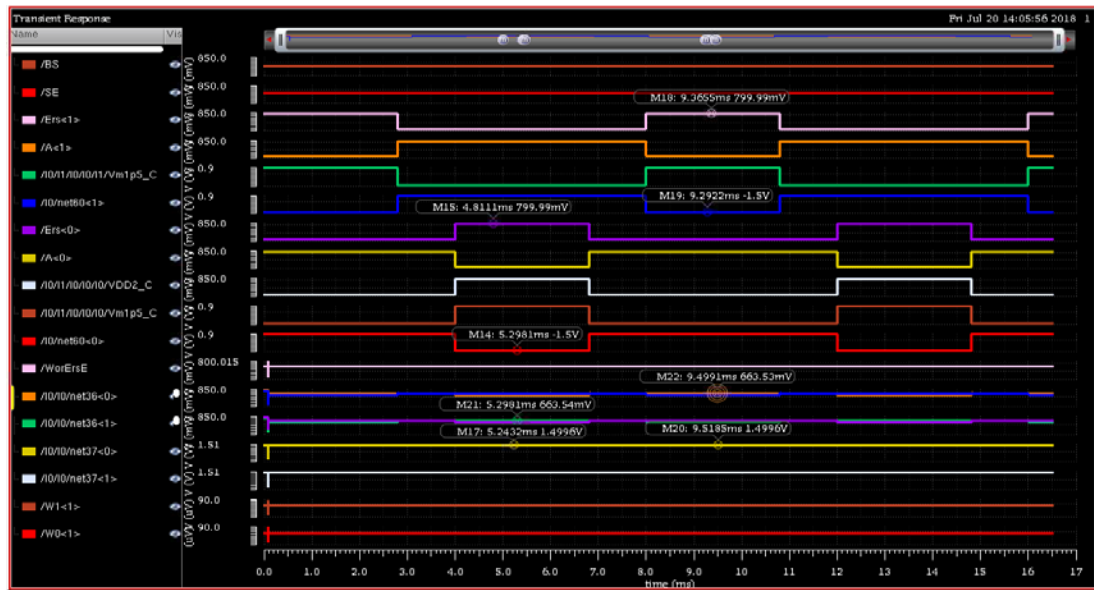


Figure 31. Erase Corners TRAN VDD = 0.800V, 3sigma, 0C m1p5V.

4.2.12 Observations

Storage cell write and erase times from the literature range from 10mS to 100ms while being exponentially sensitive to the gate channel voltage difference. The tradeoff is between write/erase times and durability or wear out and storage time. Generally, the slower one writes or erases, the longer EEPROM lifetimes or the number write/erases cycles. Initially, with harder writes, higher voltages result in longer storage times. Faster wear out is observed with higher write/erase voltages. Restated longer write /erases occurring at lower voltages require longer erase/write times that provide a greater number of write/erase cycles and greater memory life time. As a result, the HV long channel gate delays have no impact on write or erase times. However, the long channel devices do have a modest effect on EEPROM read times performance. Thin-oxide level shifters mitigate concerns for fast read times. At the slow-slow corner (VDD= 720mV, sigma =-3, and temp 50C) read times are pushed out from a typical 1uS to 10uS. This observation can be improved by scaling up the VDD2 level shifter by 3X to achieve a 2 to 3uS read times or using a thin-oxide level shifter pushing read times below a 100nS. Figure 32 is a snapshot of a four-bank implementation of a 1Kx 88-bit word EEPROM.

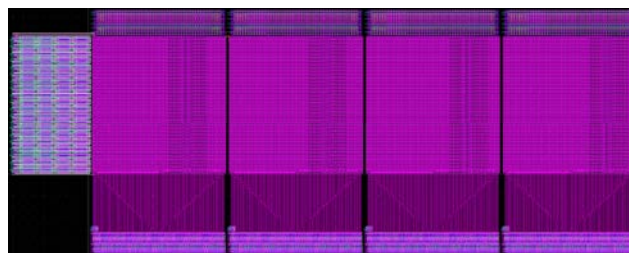


Figure 32. 1Kx88-bit EEPROM composed of four banks.

4.3 Overview of MTBF Model

This model is expected to project long-term EEPROM lifetime and data retention time tradeoff with respect to different programming voltages in order to establish optimal programming protocols. The final model integrates two independent building blocks, a time dependent dielectric breakdown (TDDB) model and a charge trap retention model, with modification that is applicable to HfO₂ gate dielectric CMOS. Figure 33 shows the high-level block diagram of the model. Long-term charge retention loss, required read voltage and input offset voltages of storage cells and sense amplifier define the programming threshold shift requirement for successful read operations.

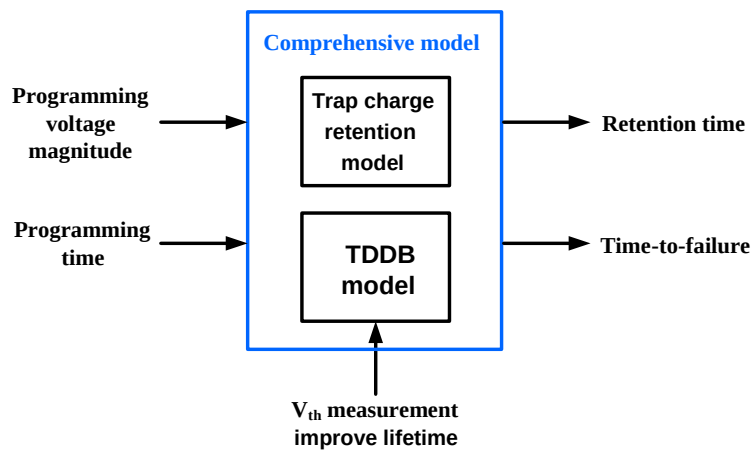


Figure 33. Block diagram of the final EEPROM programming model.

Knowing the amount of trapped charge for a desired threshold shift, desired trap energy [21] and gate stack thickness and applying Fowler-Nordheim (FN) tunneling mechanism [22-25], programming voltages can be established. In this way, data (or stored charge) retention loss and required programming voltage are linked through the programming threshold shift. EEPROM lifetime under various programming voltages is predicted by TDDB models. The Literature has shown TDDB models for SiO₂ gate dielectric [26-37] and Hf alloys such as HfAlO_x and HfSiON but few papers on HfO₂ based transistor TDDB model [38-40]. Therefore, our work incorporates existing models with weighting factors to best fit the results to HfO₂ based transistors. Validation of the final TDDB model relies on data comparison with published data that relates to HfO₂ gate dielectric devices which are also quite few.

In addition to the model, we designed a threshold measurement method for an EEPROM bank that allows us to *estimate the average threshold for each die* so that the process variation across wafer and the lot can be taken into account when developing selecting programming voltages. This knowledge of average threshold voltage allows adjustment of programming voltage unique to each die that prolongs the lifetime of the EEPROM, and as a result increases yields.

Model development starts with long-term read success where the programming threshold shift has to tolerate or absorb the presence of storage cell mean threshold variation, sense amplifier input offsets, storage charge retention losses and write/erase effect residual shift. The required total programming threshold shift for long-term read success is given by

$$V_{th,shift} \geq V_{read} + \sqrt{V_{os,cell}^2 + V_{os,SA}^2 + \sigma_{W/E,residual}^2} + \Delta V_{th,loss} \quad (7)$$

where $V_{th,shift}$ is the programmed threshold shift, $V_{os,cell}$ and $V_{os,SA}$ are the offset voltages of the storage cell and sense amplifier respectively, $V_{W/E,residual}$ is write/erase residual variation and $\Delta V_{th,loss}$ is undesired threshold shift due to trapped charge loss over time. V_{read} is the minimum voltage of the memory pair ensuring 4 sigma read recovery. The write/erase residual variation refers to the fact that after erase operation the threshold voltage will not return to its native value exactly. According to [41] and [42], the residual value is small compared to the programming threshold shift and has negligible effect on memory operation. With required threshold shift known from equation (7), the total trapped charge can be calculated using relation $Q_{trap} = V_{th,shift} \cdot C_{ox}$. With knowledge of amount of trapped charge along with desired trap energy, carrier tunneling (FN) mechanisms and gate stack thickness, the required programming voltage can be calculated. This links the desired programming threshold shift and storage pair mean threshold to the programming voltages.

The next step is to define the desired trap energy levels. Defect levels in the HfO_2 high-k dielectric layer are classified into three groups according to their locations within the bandgap relative to the Si substrate conduction band and valence band [43]. Figure 34 shows a simplified pictorial representation of the energy band diagram for a HfO_2 high-k NMOS transistor gate stack and group allocation. Trap levels in group 1 are considered as shallow high-k NMOS transistor gate stack and group allocation. Trap levels in group 1 are considered as shallow levels where trapped carriers can easily de-trap after programming voltage is removed. This group of traps does not provide long-term memory functionality. Group 2 levels whose energy span maps to the Si substrate bandgap are the desired trap energy. Under nonprogramming condition, carriers trapped in group 2 energy levels detrapp slowly to the Si substrate according to their physical distance from the substrate, the activation energy [43] and the quality of the dielectric material. Threshold shifts due to carriers trapped in these levels are suitable for memory application. Group 3 levels shown in Figure 34 are levels map below the valance band of Si substrate. Carriers trapped in these levels give rise to the fixed oxide charges [43] and are difficult to remove under normal erase voltages. Group are to be avoided as result in sever oxide damage. *The desired trap energy is about 1.2eV to 2.3eV below the conduction band edge of the HfO_2 dielectric as shown in Figure 34.*

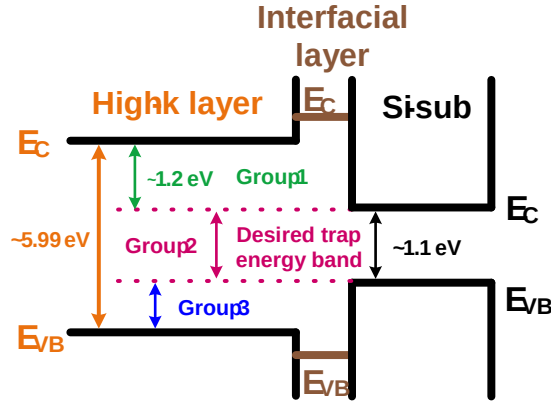


Figure 34. Different groups of defect levels within the bandgap of high-k dielectric layer.

The connection between programming threshold voltage shift and programming voltages has been demonstrated. The final step of the model development is invoking the TDDB model and extracting lifetime of the cell transistor with various programming voltages. McPherson [44] and Padovani [45] summarized frequently used TDDB models; the thermochemical E model [26, 27], 1/E model [28-31], power-law voltage V^N -model [32-34] and exponential $E^{1/2}$ model [35-37]. All models predicted the same TDDB results for electric field strength above 8MV/cm while disparities show up at lower field strength [44]. Among all models, the thermochemical E model gives the most conservative time-to-failure results whereas the 1/E model gives the most optimistic results [44]. The above-mentioned models are derived for SiO₂ gate dielectric. Our final model incorporates the existing model as a basis and adds weighting factors to fit for HfO₂ gate dielectric CMOS transistors.

As mentioned above, the knowledge of average threshold voltage of a die can improve EEPROM lifetime and yield when different dies from a same wafer or from different wafers are considered. The balance of this section is dedicated to discussing the need for accurate threshold measurement. To illustrate the idea, we use the 1/E model. The time-to-failure predicted by 1/E model is given by

$$T_{BD} \cong \tau_0 e^{\frac{K t_{ox}}{V_g - V_{th}}} \quad (8)$$

where K is associated with the carrier tunneling and τ_0 is a temperature dependent pre-factor [44]. This equation reveals an exponential relationship between the transistor lifetime and gate overdrive voltage, $-V_{th}$. Therefore, accurately controlling the gate voltage is critical. It is worth noting that the threshold process variation is also critical in lifetime improvement. Threshold variation due to fabrication process gradient dominates when considering silicon areas larger than about 200 μ m in diameter. The four EEPROM banks of this design are laid out in an area about 260 μ m x 268 μ m. Threshold mismatch for one EEPROM die (four banks) is considered the dominate factor across the EEPROM area and is controlled by transistor pair area. The average or mean threshold across the four banks is the *process threshold* for the EEPROM memory and is approximately constant across this area. We produced a simple method that enables the average threshold measurement across the four banks in Figure 35 showing a conceptual

diagram. Four sets of test transistors are placed at the four corners of the full EEPROM bank. These test transistors have a sufficient number of fingers such that the threshold mismatch between them is negligible. The threshold mismatch by measurement is given by

$$V_{os,vth} = \frac{A_{VT}}{\sqrt{WL}} \quad (9)$$

where A_{VT} is Pelgrom coefficient. The four test transistors are connected in parallel and their average threshold is measured using circuit shown in Figure 35(b). The reference current in Figure 35(b) is the current at which the threshold is measured. The top current mirror output is scaled down four times to average the current sum of the four test transistors. As the DAC sweeps the gate voltage of the test transistors, their average current is compared with the reference current. The result is feed to a Sense amplifier inverter. The trip point of the inverter is the estimated mean threshold across the EEPROM bank. Knowing the mean threshold for each die, the programming voltage can be adjusted so that the low threshold dies will not be over stressed and high threshold dies under programmed enhancing EEPROM yield and lifetimes.

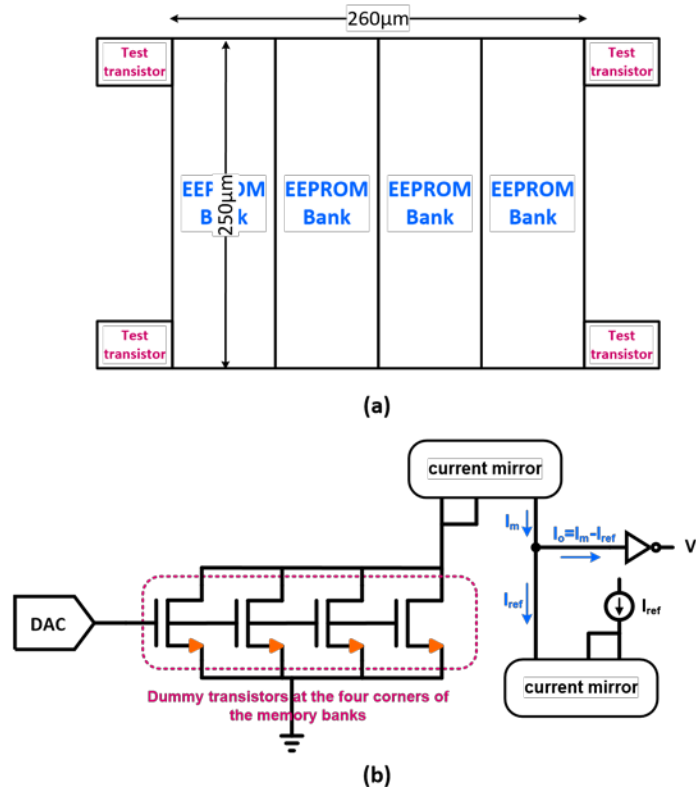


Figure 35(a) Four test transistors are placed at four corners of the full EEPROM bank for V_{th} measurements. (b) Threshold voltage measurement circuits.

4.4 LDO Implementation

This section discusses LDO implementation for generating the programming voltages. In order to have highly accurate control over the programming voltages, on-chip LDO and off-chip DAC are employed. The LDO and DAC provide fine tuning to the programming voltages so that the trapping characteristics can be studied while avoiding catastrophic damage to the device due to sudden high voltages. Parameters that matter in this application related to LDO and DAC are minimum programming voltage step, LDO output current and voltage capability, LDO and DAC accuracy and LDO stability. The LDO settling time is not a burden in this application since we have allocated voltage stabilization time in the wrapper that provides enough time for the programming voltage to stabilize. With the given process, the 10 μ s designed settling time should easily be met. Khan et al. [46, 47] have used 10ms programming pulse with 10mV and 50mV increments. We decided to use 5mV programming step to achieve fine tune on the programming voltages. Two 16 bits discrete DACs are selected (DAC7631 and LTC1650). The LDO output swing is from 0.6V to 2.5V which covers read and write operations. The erase voltage is generated by a similar LDO which has negative output. The erase LDO output is -1.5V that results a -3V across the storage cell.

The main current load to the LDO is the storage cell gate leakage of one word. The programming current of a word is much less compared to the leakage. Fowler-Nordheim tunneling is used to estimate the programming current. With 2V write voltage, 1nm thick IL layer and 400mV threshold voltage, the programming current of one word (88 bits) is about 704nA. Using the PDK typical I_{off} of HVTNFIET which is 94nA/ μ m. Leakage current of one word is about 10uA. The LDO is designed to support 100uA load current.

Accuracy of LDO is given by

$$Accuracy\% \approx \frac{\Delta V_{IR} + \Delta V_{LR} + \sqrt{\Delta V_{o,REF}^2 + \Delta V_{o,amp}^2 + \Delta V_{o,R}^2 + \Delta V_{TC}^2}}{V_o} \times 100\% \quad (10a)$$

where ΔV_{IR} is line regulation, ΔV_{LR} is load regulation, $\Delta V_{o,REF}$ is voltage reference drift, $\Delta V_{o,amp}$ is error amplifier drift, $\Delta V_{o,R}$ feedback resistor network tolerance and ΔV_{TC} is temperature coefficient

$\Delta V_{TC} = TC \cdot (T_{max} - T_{min})V_o$. Expanding quantities ΔV_{IR} and ΔV_{LR} , equation (10b) is obtained.

$$Accuracy\% \approx \frac{\frac{1}{A\beta} + \frac{R_1 + R_2}{g_{m,pass} \cdot A \cdot R_1} + \sqrt{\Delta V_{o,REF}^2 + \Delta V_{o,amp}^2 + \Delta V_{o,R}^2 + \Delta V_{TC}^2}}{V_o} \times 100\% \quad (10b)$$

where A is error amplifier open loop gain, feedback factor β equals $R_I/(R_I + R_F)$ shown in Figure 36(a). To simplify the calculation, we assume the square root term in equation (10b) is less than the sum of other terms. Since the DAC (DAC7631) has full scale error of ± 1 mV, we set 0.33% accuracy of the LDO to preserve the DAC accuracy when LDO output is 0.6V. The open loop gain of the error amplifier is obtained using equation (10b) and is about 133dB. To achieve high open loop gain, a boosted single ended telescopic

OTA is used as the error amplifier. Figure 36(b) shows the circuit topology. The error amplifier is biased using a bandgap voltage reference shown in Figure 37.

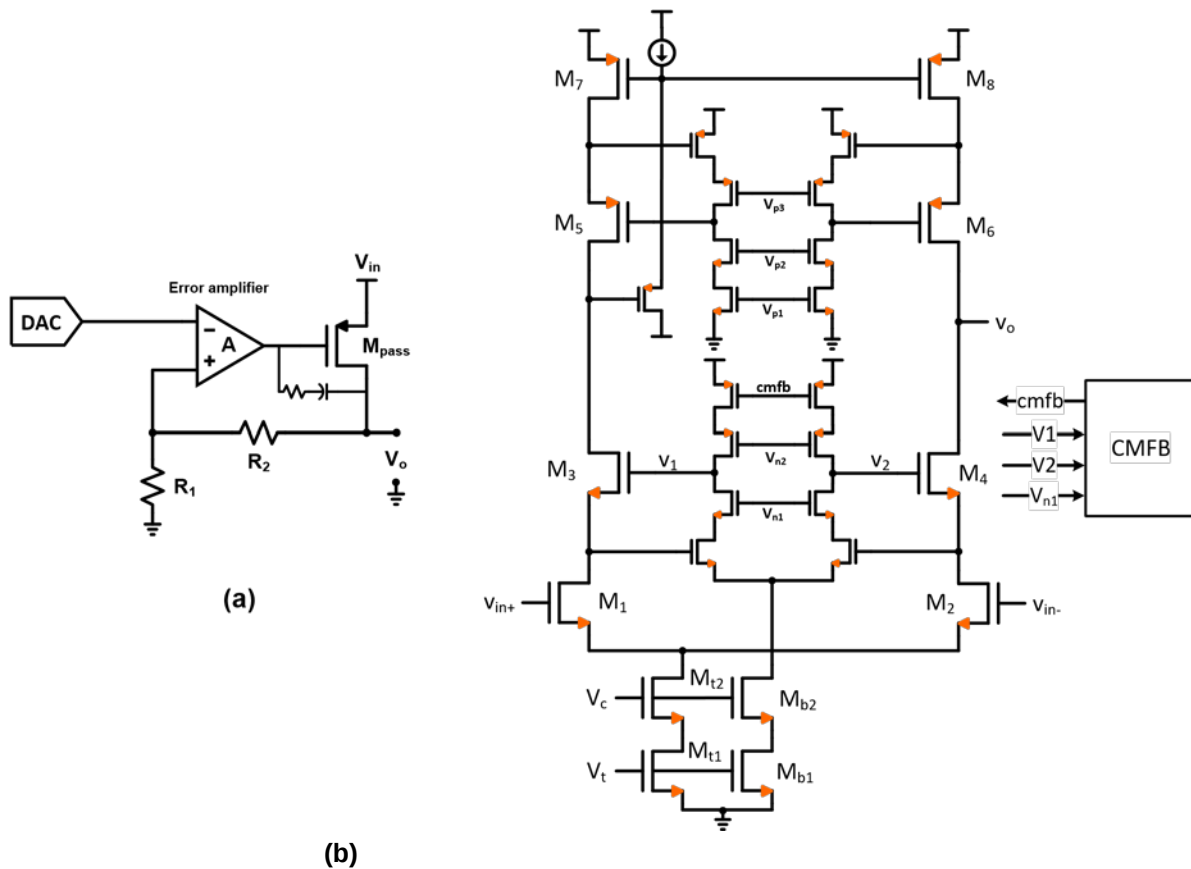


Figure 36. (a) LDO schematic. (b) Error amplifier schematic.

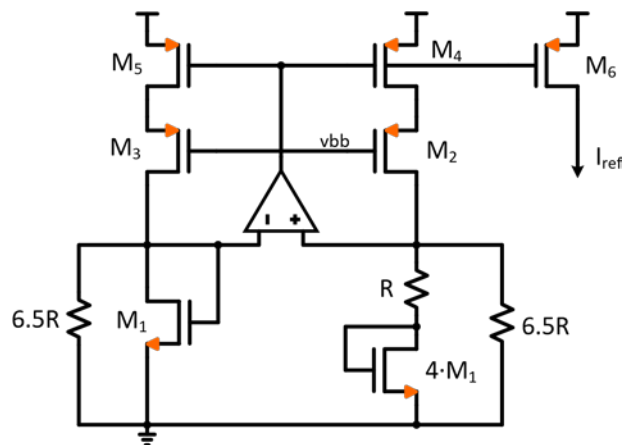


Figure 37 Bandgap reference for basing the error amplifier.

4.5 MTF and Data Retention Trade-off Model

This model is expected to allow users project long term EEPROM lifetime and data retention time tradeoff with respect to different programming voltages in order to establish optimal programming protocols for both short and retention. A comprehensive model block diagram is shown in Figure 38. The key parameters that connect the EEPROM retention time and lifetime are programming threshold shift,

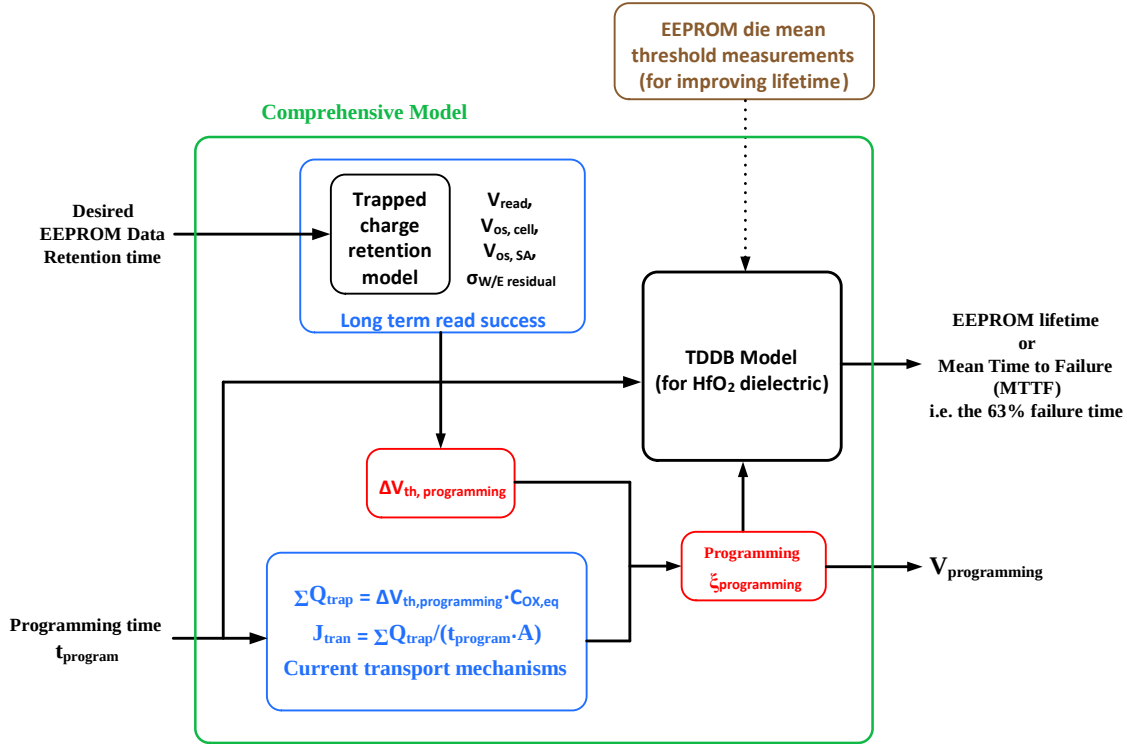


Figure 38. Block diagram of the final comprehensive model.

$\Delta V_{th, programming}$, and programming electric field (applied programming voltages), $\xi_{programming}$, across the gate oxide. The amount of or desired programming threshold shift is determining by projected long term charge retention loss, required read voltage and input offset voltage of the storage cells and sense amplifier as shown by equation 11.

$$\Delta V_{th, programming} \geq V_{read} + \sqrt{V_{os, cell}^2 + V_{os, SA}^2 + \sigma_{W/E, residual}^2} + \Delta V_{th, loss} \quad (11)$$

where $V_{th, programming}$ is the programmed threshold shift, $V_{os, cell}$ and $V_{os, SA}$ are the offset voltage of the storage cell and sense amplifier respectively, $V_{W/E, residual}$ is write/erase residual variation and $\Delta V_{th, loss}$ is undesired threshold shift due to trapped charge loss over time.

With programming threshold voltage known, the total amount of trapped charge required to is determined by

$$\sum Q_{tapping} = \Delta V_{th,ing} \cdot C_{ox,eq} \quad (12)$$

where $C_{ox,eq}$ is the equivalent gate stack capacitance which includes SiO₂ interfacial layer (IL) and HfO₂ high dielectric (HK) layer. The tunneling current density resulted from transport of trapped charge is determined by

$$J_{tran} = \frac{\sum Q_{tapping}}{t_{program} \cdot A} \quad (13)$$

where $t_{program}$ is the duration of programming time, A is gate dielectric area and J_{tran} is tunneling current density. As shown by Figure 38, the programming electric field $\xi_{programming}$ can be determined by equation (11) through (13) together with current transport mechanisms.

Once the programming electric field is determined, the time dependent dielectric breakdown (TDDB) model is invoked. There are many proposed TDDB models in the literatures. Every proposed model has its own pros and cons. In this effort, we desire a model that is more universal which means the model is not bounded by any application constraints yet still provides accurate lifetime estimates. It should be noted that in addition to various TDDB models, current transport mechanisms that result in breakdown of the gate stack dielectric are also multiple. How to incorporate each mechanism for the best fitting to the experimental data is still under study by multiple researchers. In order to preserve the universal feature of our model we use the concept of progressive breakdown and percolation mechanism with the 3D Kinetic Monte Carlo algorithm to predict the mean time to failure (i.e. defined as the 63% failure time, t_{63}). The challenge is how to incorporate each current transport mechanism with different weighting into the 3D KMC algorithm and determining the defect generation rate and the probability of next defect location in the lattice. Simplifications such as considering certain transport mechanisms while eliminating others are anticipated. The model simulation is going to be carried out using a MATLAB® implementation.

As shown by Figure 38, we have defined the comprehensive EEPROM lifetime averages data retention time trade-off model. The critical intermediate parameter that connects data retention time to the lifetime is the programming electric field, $\xi_{programming}$. In order to determine $\xi_{programming}$, different current transport mechanisms are considered. Determining how to incorporate these transport mechanism for determining $\xi_{programming}$ is the remaining work.

The TDDB modeling simulation is performed using 3D Kinetic Monte Carlo (KMC) simulation algorithm and is implemented using MATLAB®. The 2D KMC simulation can be visualized as the formation of cubic cell connection in the IL and HK layer lattices shown in Figure 39. Each cube represents a defect in the dielectric lattice. Defect generation rate and probability of next defect location are the two critical parameters that govern the appearance of defect in the grid. These two parameters are determined by local electric field strength, local dielectric permittivity, activation energy associated with the specific defect location and temperature, which are related back to the current transport mechanisms.

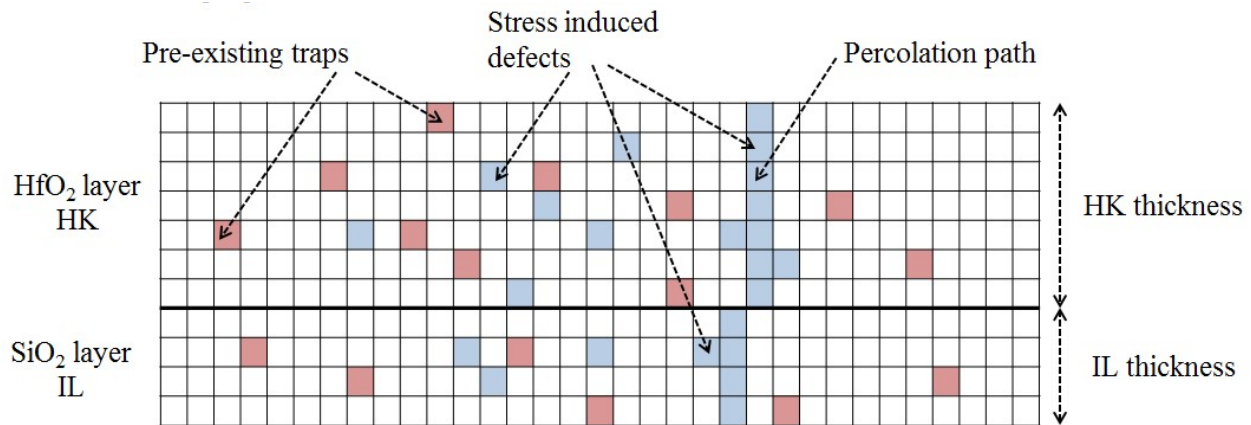


Figure 39. 2D Kinetic Monte Carlo simulation diagram.

Our KMC simulation extends 2D to 3D for better presentation of the 3D dielectric bulk, shown in Figure 40. The KMC algorithm flow chart is shown in Figure 41.

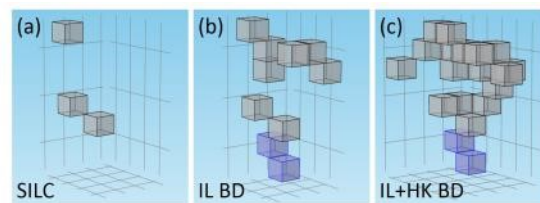


Figure 40. Percolation path formations by 3D Kinetic Monte Carlo simulation. Each cube represents a defect. (a) SILC stage, (b) IL layer breakdown, (c) IL+HK layers breakdown. Purple cubes represent defects in the IL layer and grey cubes represent HK layer defects [4].

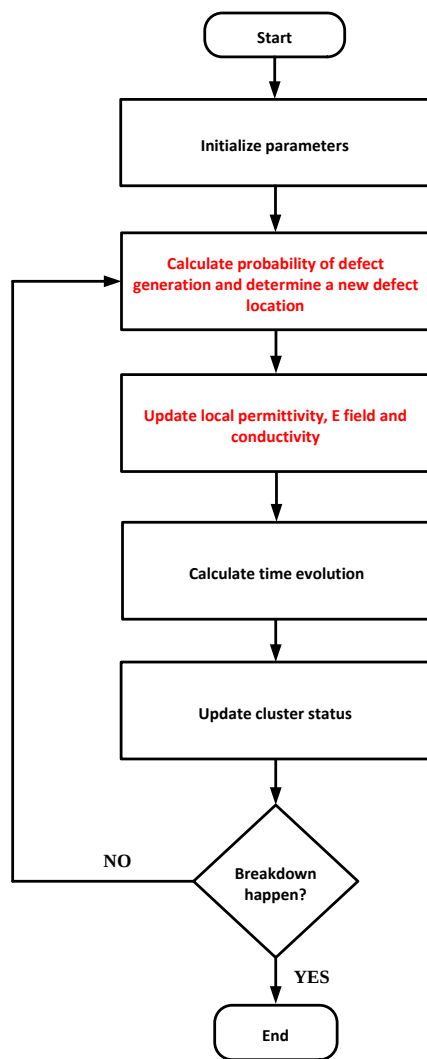


Figure 41. 3D Kinetic Monte Carlo simulation algorithm flow chart

5.0 CONCLUSIONS

This report specifies the implementation of and guidelines for the interfacing control logic, the wrapper, for the 256x88x4 bytes EEPROM. This wrapper provides a functional interface between the CPU bus and the 256x88x4 bytes EEPROM. Test points for JTAG testing are outlined in this document as well. A VHDL EEPROM model based on the operation of the EEPROM storage core was developed. The wrapper VHDL logic was validated using the Top-level simulation waveforms along with blocks of the EEPROM storage core, the controller (FSM), CUI (command user interface or CPU/EEPROM interface). Secondly, the EEPROM corner verification documents the VLSI block functions, their location and EEPROM top cells with respect to a single bank and a four bank EEPROM, operational documentation, 3 sigma corners test benches, and 3 sigma corners operational validation. Corner testing is presented along with results for ± 3 sigma, 0 to 90°C, and VDD 720mV to 900mV, for read, write and erase respectively. Erase operation is completed at m1p5 equals -1.5V. Valid write operation is for VDD2 equals 1.5 to 2.7V. Read validation is carried out at VDD equals both 500 and 600mV. Beyond the typical supply voltages, the EEPROM utilizes a dedicated write, read, and erase LDO supplies programmable to 100 ppm from 1.5 to 2.7, 0 to -1.5, and 0 to 1V respectively.

This report documents as well as verifies the EEPROM wrapper specification, controller program model, synthesis code, and code verification. In addition, the VLSI layout is documented for a single bank and four banks EEPROM along with a description of operation, location of top cells, corners test benches and test bench operation.

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7.0 LIST OF SYMBOLS, ABBREVIATIONS AND ACRONYMS

3D	Three Dimensional
AFRL	Air Force Research Laboratory
BIOS	Basic Input/Output System
CMOS	Complementary Metal-Oxide Semiconductor
CPU	Central Processing Unit
CVS	Constant-Voltage Stress
DAC	Digital-to-Analog Converter
Δ	Delta
ECC	Error-Correcting Code
EEPROM	Electrically Erasable Programmable Read-Only Memory
FN	Fowler-Nordeim Tunneling
FSM	Finite-State Machine
HBD	Hard Breakdown
HfO ₂	Hafnium Oxide
HK	High Dielectric
I/O	Input/Output
IC	Integrated Circuit
IL	Interfacial level
IP	Intellectual Property
KMC	Kinetic Monte-Carlo
LDO	Low Dropout
LSB	Least-Significant Bit
MTBF	Mean-Time Between Failure
NMOS	Negative Metal-Oxide Semiconductor
PCB	Printed-Circuit Board
PK	Poole-Frenkel tunneling
PMOS	Positive Metal-Oxide Semiconductor
ppm	parts-per million
RAM	Random Access Memory
ROM	Read-Only Memory
RVS	Ramp Voltage Stress
SBD	Soft Breakdown
SiO ₂	Silicon Dioxide
SiO _x	Silicon-Dioxide
SILC	Stress-Induced Leakage Current
SK	Schottky emission
SRAM	Static Random-Access Memory
TAT	Trap-Assisted Tunneling
TDDDB	Time-Dependent Dielectric Breakdown
TDI	Test Data Input
TDO	Test Data Out

TT
VHDL
VTH

Trap-to-Trap Tunneling
VHSIC Hardware Descriptive Language
Threshold Voltage