
AFRL-RY-WP-TR-2020-0008

# MILLIMETER-WAVE WAFER-SCALE PHASED ARRAYS

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**MARCH 2020**
**Final Report**



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# REPORT DOCUMENTATION PAGE

*Form Approved*
*OMB No. 0704-0188*



| 1. REPORT DATE *(DD-MM-YY)* | 2. REPORT TYPE | 3. DATES COVERED *(From - To)* |
|---|---|---|
| March 2020 | Final | 14 December 2012 – 30 June 2019 |

**4. TITLE AND SUBTITLE**
MILLIMETER-WAVE WAFER-SCALE PHASED ARRAYS

**5a. CONTRACT NUMBER**
FA8650-13-1-7316/
ECCS-1542148

**5b. GRANT NUMBER**

**5c. PROGRAM ELEMENT NUMBER**
6110E/62716E

**6. AUTHOR(S)**
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**5d. PROJECT NUMBER**
1000

**5e. TASK NUMBER**
N/A

**5f. WORK UNIT NUMBER**
Y0WF

**7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)**
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**8. PERFORMING ORGANIZATION REPORT NUMBER**

**9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)**
Air Force Research Laboratory
Sensors Directorate
Wright-Patterson Air Force Base, OH 45433-7320
Air Force Materiel Command
United States Air Force

National Science Foundation (NSF)
2415 Eisenhower Avenue
Alexandria, VA 22314

**10. SPONSORING/MONITORING AGENCY ACRONYM(S)**
AFRL/RYDI

**11. SPONSORING/MONITORING AGENCY REPORT NUMBER(S)**
AFRL-RY-WP-TR-2020-0008

**12. DISTRIBUTION/AVAILABILITY STATEMENT**
Approved for public release; distribution is unlimited.

**13. SUPPLEMENTARY NOTES**
This report is the result of contracted fundamental research deemed exempt from public affairs security and policy review in accordance with The Under Secretary of Defense memorandum dated 24 May 2010 and AFRL/DSO policy clarification email dated 13 January 2020. This material is based on research sponsored by Air Force Research Lab (AFRL) and the Defense Advanced Research Projects Agency (DARPA) under agreement number FA8650-13-1-7316. The U.S. Government is authorized to reproduce and distribute reprints for Governmental purposes notwithstanding any copyright notation thereon. The views and conclusions contained herein are those of the authors and should not be interpreted as necessarily representing the official policies or endorsements, either expressed or implied, of AFRL and DARPA or the U.S. Government. Report contains color.

**14. ABSTRACT**
Developed 60 GHz 2x64- and 2x256-element dual-polarized dual-beam wafer-scale phased-array transceivers with integrated up/down converters. The 2x64-element phased-array is built as a single reticle and occupies 21x21 $mm^2$. To our knowledge, this work presents the first fully polarimetric scalable wafer-scale phased-array transceivers using simple reticle-to-reticle stitching, resulting in state-of-the-art functionality and complexity on a single chip.

**15. SUBJECT TERMS**
phased-array transceivers, reticle stitching, polarimetric

| 16. SECURITY CLASSIFICATION OF: | | | 17. LIMITATION OF ABSTRACT: | 18. NUMBER OF PAGES | 19a. NAME OF RESPONSIBLE PERSON (Monitor) |
|---|---|---|---|---|---|
| a. REPORT | b. ABSTRACT | c. THIS PAGE | | | Paul Watson |
| Unclassified | Unclassified | Unclassified | SAR | 59 | 19b. TELEPHONE NUMBER *(Include Area Code)* N/A |

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# 1. Project Summary

We have developed 60 GHz 2x64- and 2x256-element dual-polarized dual-beam wafer-scale phased-array transceivers with integrated up/down converters. The 2x64-element phased-array is built as a single reticle and occupies 21x21 $mm^2$. It is based on radio frequency (RF) beam-forming transmit/receive (TRX) channels with 5-bit phase and 9-bit gain control, dual nested 1:64 distribution networks with Wilkinson divider/combiners, line amplifiers (LA), and dual up/down converters with a shared local-oscillator (LO) multiplier chain. The differential on-chip antenna feeds are electromagnetically (EM)-coupled to a high-efficiency quartz superstrate dipole antenna array placed $\lambda/2$ apart in the horizontal and vertical directions. Four 2x64-element phased-array reticles are then bondwired and stitched in the intermediate-frequency (IF)/LO domain to form a 2x256-element phased-array super-reticle which occupies 42x42 $mm^2$. The 2x64- and 2x256-element phased-arrays scan to 50deg in the elevation (Eplane) and azimuth (H-plane) planes. The equivalent isotropically radiated power (EIRP) of the 2x64-element array is 37-38 dBm with a 3-dB bandwidth of 60-64 GHz, while that of the 2x256 element array is 42-44 dBm with a 3-dB bandwidth of 61-63 GHz per polarization. A communication link using the 2x64-element array is demonstrated with quadrature phase-shift keying (QPSK), 16-quadrature amplitude modulation (QAM) and 64-QAM waveforms, reaching 12-16 Gb/s data rates per polarization at 1.3 m.

To our knowledge, this work presents the first fully polarimetric scalable wafer-scale phased-array transceivers using simple reticle-to-reticle stitching, resulting in state-of-the-art functionality and complexity on a single chip.

Detailed papers and reports have been shared with the Defense Advanced Research Projects Agency (DARPA) and with several Department of Defense (DoD) companies.

## 1.1 Detailed Description of the Work

Since the work is unrestricted, the entire project is detailed in a seminal paper in the Institute of Electrical and Electronics Engineers (IEEE) Microwave Theory and Techniques (MTT), one of the longest papers ever accepted in IEEE. This paper is included in this report.

## 1.2 Publications during the Program

1. Umut Kodak, Bhaskara Rupakula, Samet Zihir and Gabriel M. Rebeiz, "*A Scalable 60 GHz Tx/Rx 2x64-Element Dual-Polarized Dual-Beam Wafer-Scale Phased-Array with Integrated Dual-Transceivers,*" *IEEE Int. Microwave Symposium*, 2019, Boston, MA.
2. Umut Kodak, Bhaskara Rupakula, Samet Zihir and Gabriel M. Rebeiz, "*A 62 GHz Tx/Rx 2x128-Element Dual-Polarized Dual-Beam Wafer-Scale Phased-Array Transceiver with Minimal Reticle-to-Reticle Stitching*," *IEEE RF Integrated Circuits Conference*, 2019, Boston, MA.
3. Umut Kodak, Bhaskara Rupakula, Samet Zihir, and Gabriel M. Rebeiz, "60 GHz 64- and 256-Element Dual-Polarized Dual-Beam Wafer-Scale Phased-Array Transceivers with Reticle-to-Reticle Stitching," *IEEE Microwave Theory and Techniques*, Accepted. To appear in 2020.

## 1.3 Patents in this Program (Submitted or Granted)

None

## 1.4 Technology Transfer

Professor Rebeiz gave talks at several defense companies and National Laboratories explaining his work in wafer-scale phased-arrays. The list is shown below.

- Lockheed Martin
- Northrop Grumman
- Lincoln Laboratories
- DARPA/ONR
- Raytheon
- L3Harris
- Collins Aerospace

# 2. IEEE MTT Seminal Paper

## 2.1 Introduction

The continuous advances in silicon-based technologies have led to the development of large-scale, highly-complex and highly-integrated phased-arrays over the past decade. All-RF beamforming [1]-[10], intermediate-frequency (IF) beamforming [11] and local-oscillator (LO) beamforming architectures [12]-[14] have been proposed, and the all-RF beamforming architecture has been widely adopted due to its enhanced performance in the presence of in-band and out- of-band blockers [1], [2], [15], [16]. It also offers reduced power consumption and complexity due to the elimination of LO distribution network to each channel in which a mixer is employed.

Large-size all-RF beamforming phased-arrays can be implemented in two ways: 1) using 2x2 quad (4-element) beam- forming core-chips and their assembly (multitude of them) on a printed circuit board (PCB) with PCB-based antennas [6], [10] and 2) using silicon chips which contain 16 or more transmit-receive (TRX) channels, on-chip RF distribution network and integrated up/down converters, phase-locked loop (PLL) circuitry, analog-to-digital (ADC) and digital-to-analog (DAC) converters. Although, the former offers smaller interconnect lengths from the TRX channel to the antenna when the integrated circuit (IC) area is smaller than the total antenna array area, the latter results in lower-complexity PCBs, centralized digital control and less chips to assemble [4], [5]. The wafer-scale phased-array approach demonstrated in [3], [4], is another technique for building mm-wave phased-arrays and eliminates the transition loss from the chip to the antenna by using high-efficiency on-chip quartz superstrate antennas ([3], [17], [18]), and allows for high-complexity design on a single chip.

The 60-140 GHz band is ideal for wafer-scale phased-arrays since the TRX channels are spaced $\lambda/2$ apart (2.5-1 mm) which allows for integrating dual-polarized dual-beam phased-arrays in a single chip, leading to highly-efficient use of the silicon area. Additionally, the full-reticle size allowed by standard SiGe BiCMOS technology is 22x22 $mm^2$, and therefore the maximum on-grid number of elements can be 64 at 60 GHz and 196 at 100 GHz in a single reticle. The construction of larger-arrays beyond the reticle size requires a wafer-to- wafer stitching technique as shown in [4]. The full-reticle and sub-reticle stitching techniques are possible with high yield, however, they greatly increase the fabrication cost and design effort. In this work, a novel reticle-to-reticle stitching technique is proposed, and is based on forming scalable and large “super-reticles” by wire-bonding the standard-reticles (64-element) in the IF and LO domains. Also, the full-reticle and sub-reticle stitching techniques rely on separate fabrication cycles to implement different phased-array sizes (either 128-, 256- or even 1024-elements), however with this new method, only one fabrication cycle is required to build any phased- array size (64-, 128-, 256- and even 1024-elements from the same wafer).

This paper expands on [19], [20], and presents 60 GHz 2x64-element and 2x256-element dual-polarized dual-beam wafer-scale phased-array transceiver which is based on a single reticle design. Section 2.2 presents the wafer-scale phased-array transceiver architecture and Section 2.3 presents the dual-polarized differential dipole antenna. Sections 2.4-2.8 elaborate on the circuit designs and breakout measurements, and Section 2.9 the system analysis for the 64-element phased-array. The 64-element phased-array system measurements are provided in Section 2.10.

The reticle-to-reticle stitching method is detailed in Section 2.11, and is implemented in a dual-polarized dual-beam 256-element phased-array with system measurements presented in Section 2.13. Section 2.12 concludes the paper.

## 2.2 Wafer-Scale Phased-Array Transceiver Architecture

A scalable 60 GHz dual-polarized dual-beam transmit/receive wafer-scale phased-array architecture is shown in Figure 1. A single reticle based on all-RF beamforming architecture is designed consisting 2x64-element TRX channels with 5-bit phase and 9-bit gain control, nested 1:64 Wilkinson combiner/divider networks, bidirectional line amplifiers (LA) for each 2x2 and 4x4 sub-arrays to compensate for the routing loss, dual up/down converters with a quadrupler (x4) in the LO path to allow for an LO frequency of 12-14 GHz. In addition, the scalability to larger arrays is achieved using separate LO and IF signal paths which consist of line amplifiers and splitter networks integrated on the same reticle.

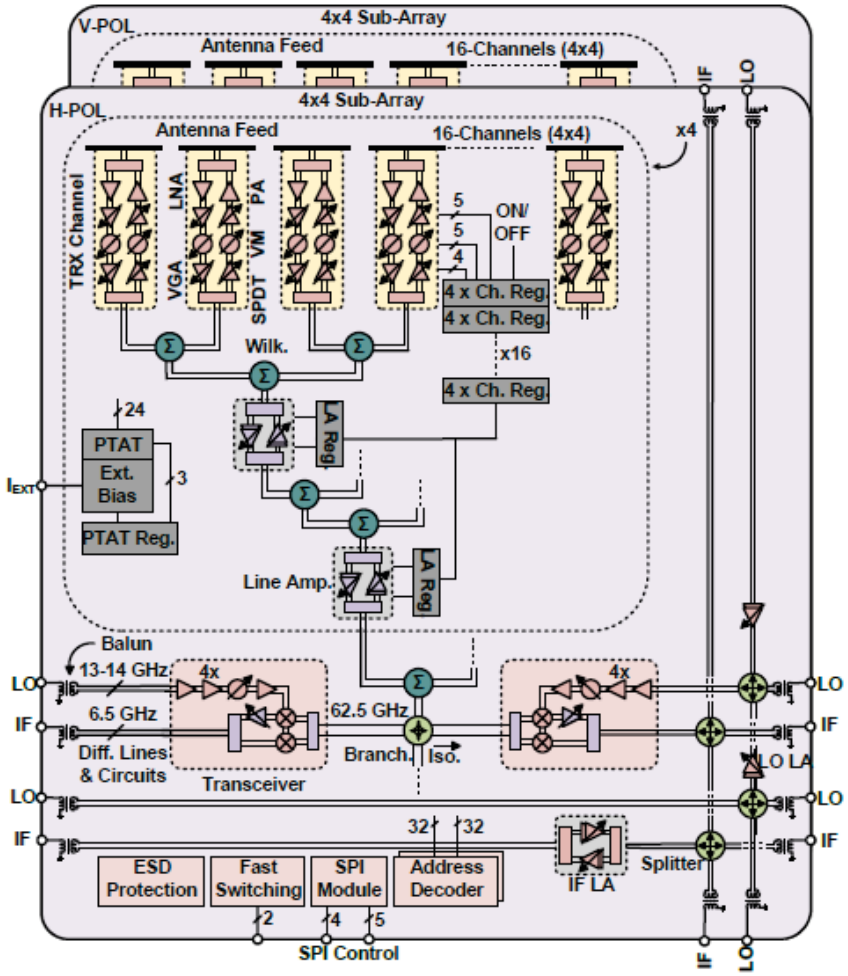



**Figure 1: Block Diagram of the 64-element Transmit/Receive, Dual-Polarized, Dual-Beam Phased-Array with integrated Dual-Transceivers**

The TowerJazz SBC18S3 SiGe BiCMOS technology offers a maximum 22x22 $mm^2$ full reticle size [21]. The on-chip electromagnetically-coupled (EM) antenna feeds are placed $\lambda/2$ apart in the x- and y-directions and occupy 20x20 $mm^2$ for an 8x8 antenna array. Note that in order for the quartz superstrate antenna not to cover the bonding-pads, the chip size is extended to 21x21 $mm^2$. The RF, IF, and LO circuit blocks are designed using the 0.13-µm SiGe bipolar transistors with an $f_t$ and $f_{max}$ of 220-230 GHz, and the digital control circuitry is designed using the 0.18-µm CMOS transistors in the BiCMOS technology.

The proposed wafer-scale phased-array architecture has several advantages: First, using a single reticle as a unit cell paves the way for a complete system on a single wafer and allows one to build phased-arrays with thousands of elements to meet the effective isotropic radiated power (EIRP) specifications for extended coverage. Additionally, down-converting the 60 GHz RF signal to an 8 GHz IF signal using a 13-14 GHz (x4) LO reduces the complexity in the assembly and PCB design, and leads to low-cost large-scale phased-arrays. Second, a dual-polarized dual-beam architecture can be implemented within the permissible area, allowing the phased-array to be used in polarization-based multiple-input multiple output (MIMO) systems which can double the communication data rate. Third, the transmission-line loss between the TRX channel port and the radiating antenna is reduced using high-efficiency quartz superstrate antennas. The routing loss from the beamformer port to the PCB antenna is reported as 1-1.5 dB in [22] and 1.8 dB in [23]. Since this loss is present both in the Tx and Rx modes, the system signal-to-noise-ratio (SNR) is improved by 2-3 dB. The quartz superstrate antennas does not increase the assembly cost since quartz-to-silicon attachment is routinely done for gyros and accelerometers in MEMS foundries. Finally, the power consumption per $mm^2$ per polarization is 15-20 $mW/mm^2$ which is less than a typical SiGe low-noise amplifier (LNA) with a power density of 30-40 $mW/mm^2$ ([24], [25], [26]). This results in a uniform heat distribution across the chip which can be dissipated from the back of the silicon wafer due to its high thermal conductivity (60-70 W/mK).

The wafer-scale phased-array adopts a reticle-to-reticle bondwire stitching method for scalability. Since each 64-element phased-array employs IF and LO signals at 8 GHz and 13 GHz, respectively, multiple reticles can be combined in an H-tree fashion. However, since each reticle is an exact copy of each other, different IF and LO paths must be activated if the reticles are stitched together. As shown in Figure 1, there are 6 sets of IF and LO feeds per reticle which ensure that any phased-array size in the vertical and horizontal direction can be implemented (the shaded circuitry represents the IF and LO networks required for stitching). The stitching details are presented in Section 2.11.

### 2.3 Dual-Polarized Differential Dipole Antennas

The dual-polarized antennas are based on differential dipoles similar to the designs shown in [3], [4], [17], and are defined on a 100-µm thick quartz superstrate ($\epsilon_r$ 3.8), which is then attached to the wafer (Figure 2(a)). The ground plane is located on M4 and the differential microstrip feeds are on the M7 layer, at a height of 10.4-µm. The antenna is not directly connected to the feeds but is excited in a microstrip mode using proximity EM-coupling to the feeds. Because of the small height of the feeds above the ground plane, the antenna naturally presents a low impedance of ~5 Ω at 60 GHz, which needs to be matched to a differential 100 Ω impedance using wide transmission lines with ~11 Ω and ~16 Ω impedance (Figure 2(b) and (c)). Note that there is no single position underneath the antennas where a radiation resistance can be defined, since the

feeds are differential and proximity-coupled. The estimated radiation resistance of 2.5 Ω at the end of each feed-arm is based on distributed coupling and is dependent on the transmission line widths and lengths $Z_0$ = 11 Ω, $l = \lambda_d/7$). The overall antenna height is 113-µm, or $\lambda_d/23$, where $\lambda_d$ is the wavelength in the quartz superstrate.

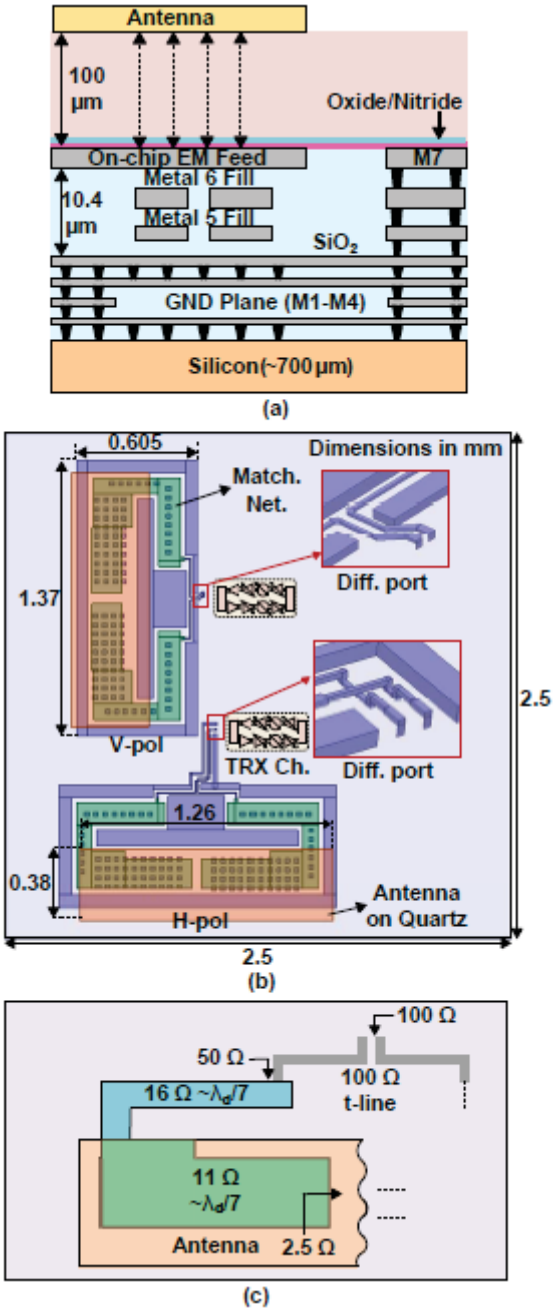



**Figure 2: High-efficiency differential Dipole Antenna (a) Cross-section, (b) Unit-cell, and (c) Single-ended Representation of the Impedance Transformation**

*Dummy metal fills are present underneath the antennas and the matching networks (small squares). Dimensions in mm.*

The antenna is linearly polarized with the E-field along its length. For dual polarization, one antenna is placed vertically and the other horizontally, and the feeds are connected to the differential V- and H-channels. In addition, design rules require a dummy metal fill below the antenna feeds, which has to be taken into account. The dual-polarized antennas were simulated in a single 0.5λ x 0.5λ cell containing one H-and one V-antenna. Periodic boundary conditions were used to simulate the antenna performance in an infinite array. The simulated $S_{11}$ of the V- and H-antennas is < -7 dB from 58.8-61.3 GHz up to 50° scan in the elevation and azimuth planes (Figure 3(a) and (b)). The simulated coupling between V- and H-antennas is below -30 dB over all scan angles in the main planes (Figure 3(c) and (d)). The simulated coupling between neighboring antenna elements with the same polarization is < -23 dB at 55-65 GHz, Figure 3(e), and results in minor $S_{11}$ variation over all scan angles as well as similar performance for the edge and interior elements. The antenna bandwidth is limited by the height of the quartz layer and the feeds.

Due to routing constraints, the feed line from the H-polarized antenna to the TRX channel is longer and has more bends than the feedline for the V-polarized antenna. As a result, the H-polarized antenna efficiency is 50%, and is lower than the V-polarized antenna efficiency of 60% (Figure 3(f)). The efficiency does not degrade with elevation scan for V-polarization and azimuth scan for H-polarization, but drops by 2 dB at 50° azimuth scan for V-polarization and at 50° elevation scan for H-polarization (Figure 3(g)). Still, an on-chip antenna on M7 without the quartz layer would have a ~15% efficiency. It has been previously reported that the air gap between the silicon chip and the quartz layer can shift the center frequency and degrade the efficiency significantly [4]. A 40-µm air gap shifts the center frequency to 69-70 GHz, and degrades the efficiency by 20 dB at 60 GHz (Figure 3(h)).

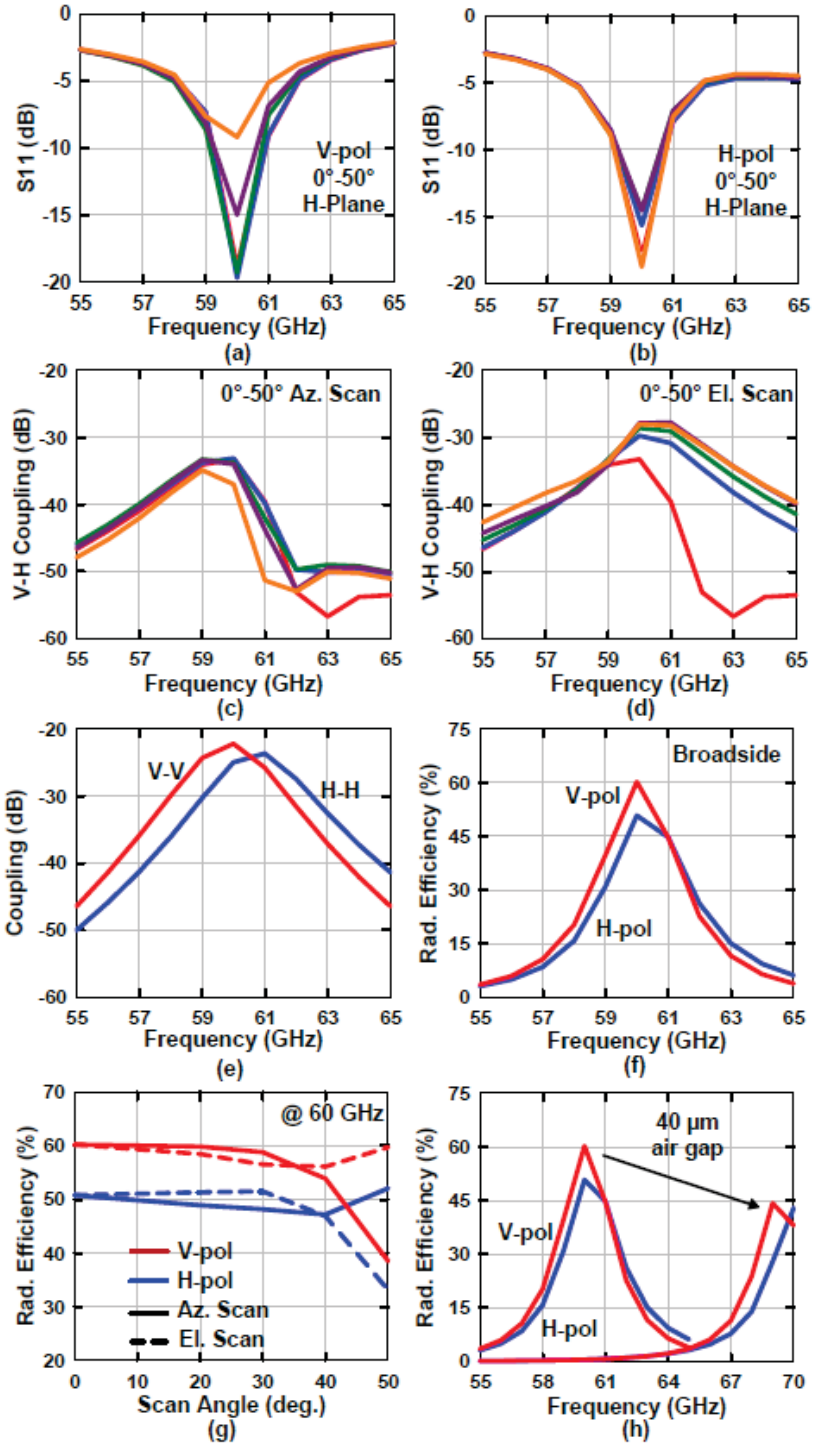



**Figure 3: Simulated Impedance Matching**

*(a) V-polarization, (b) H-polarization quartz superstrate antennas versus scan angle. Simulated V-H coupling over all scan angles in the (c) H-plane, (d) E-plane. Simulated antenna to antenna coupling for the same polarization (e) and antenna radiation efficiency at broadside (f), and versus scan angle (g). The effect of a 40-µm air gap is shown in (h).*

Single-stack quartz antennas suffer from narrower bandwidth and lower efficiency as compared to stacked patch antennas on low $\in_r$ material. A stacked patch antenna with -1.1 dB efficiency and 59-64 GHz bandwidth is presented in [27], whereas [23] demonstrates an aperture-coupled antenna with -1 dB efficiency and A10 GHz bandwidth at 60 GHz on an organic substrate. Also, a planar aperture antenna on a low temperature co-fired ceramic (LTCC) substrate is shown in [28] with -0.5 dB efficiency and A10 GHz bandwidth. However, the quartz antenna bandwidth and efficiency can be improved by using two quartz layers to 70% at 60 GHz with dual-stacked microstrip antennas, but the assembly of these quartz layers onto the chip becomes more challenging (Figure 4(a)). The bandwidth and efficiency can also be improved in the H-polarized antenna by using a shorter feed-line with fewer transitions between layers. Another technique is using probe-fed microstrip antennas, as shown in Figure 4(b). Unlike the proximity-based feeding method, via-feeding creates direct coupling and improves antenna performance. This, however, requires laser-drilled vias in the quartz superstrates, and a solder-bump attach between the quartz superstrate and the silicon chip.

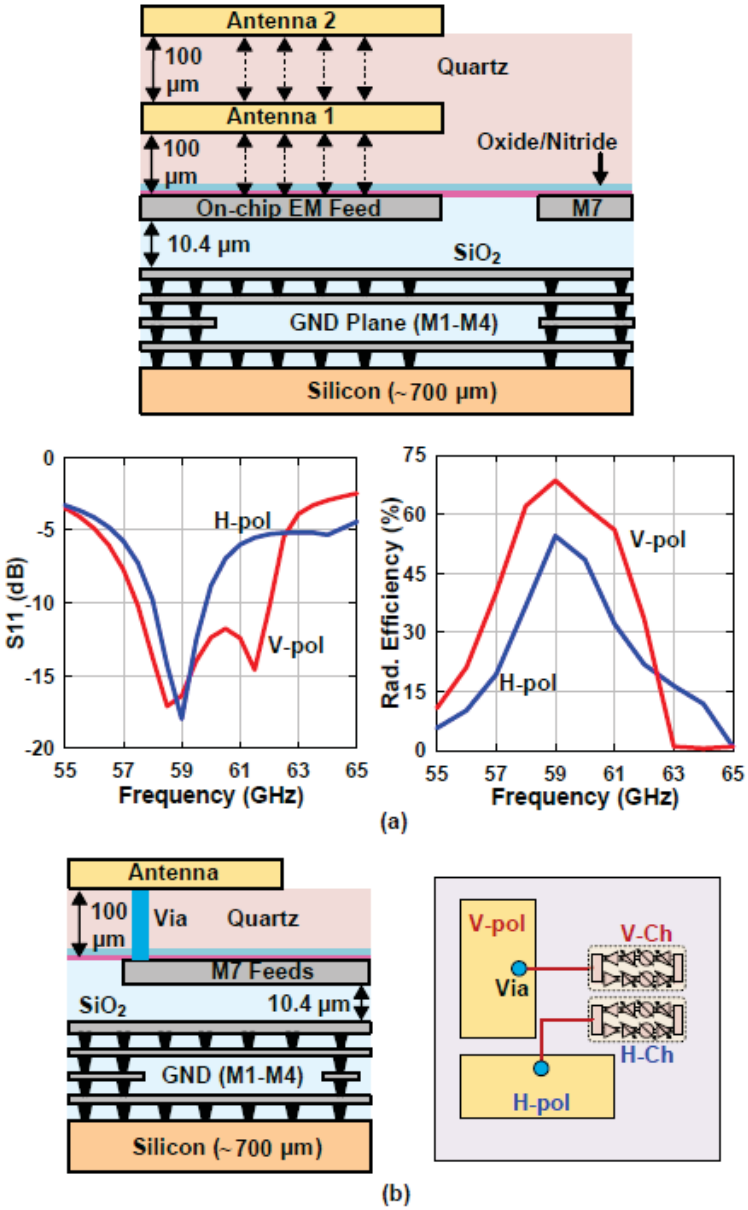



**Figure 4: Bandwidth Improvement Techniques**

*(a) dual-stack antenna cross-section, and simulated dual-stack V- and H-antenna impedance and radiation efficiency, and (b) probe-fed antenna cross-section and top-view.*

## 2.4 Phased-Array TRX Channel Design

The phased-array TRX channel consists of an LNA, two variable gain amplifiers (VGA) (4-bit and 5-bit control), and a vector modulator (VM) in the Rx path. The Tx path is similar except for a power amplifier (PA) instead of an LNA. A transmit/receive (T/R) switch is also used with a high common-mode rejection ratio (CMRR) (Figure 5(a)). Every active sub-block is based on pseudo-differential circuits, and therefore, does not provide any common-mode rejection. Due to layout conditions, some channel transmission lines are routed close to the antenna EM feeds which can create a common-mode signal in the channel due to coupling. Therefore, it is essential

to use a T/R switch with high common-mode rejection ratio. The single-pole double-throw (SPDT) switch is based on reverse-saturated shunt bipolar junction transistors (BJTs) with two 1-to-1 transformers at the antenna TRX port (Figure 5(c)). The transformer-based matching network leads to a true-differential design and achieves 40-45 dB CMRR at a penalty of 0.5 dB additional insertion loss (sim. 2.7 dB instead of 2.3 dB for single-ended SPDT switch at 60 GHz) (Figure 5(b)).

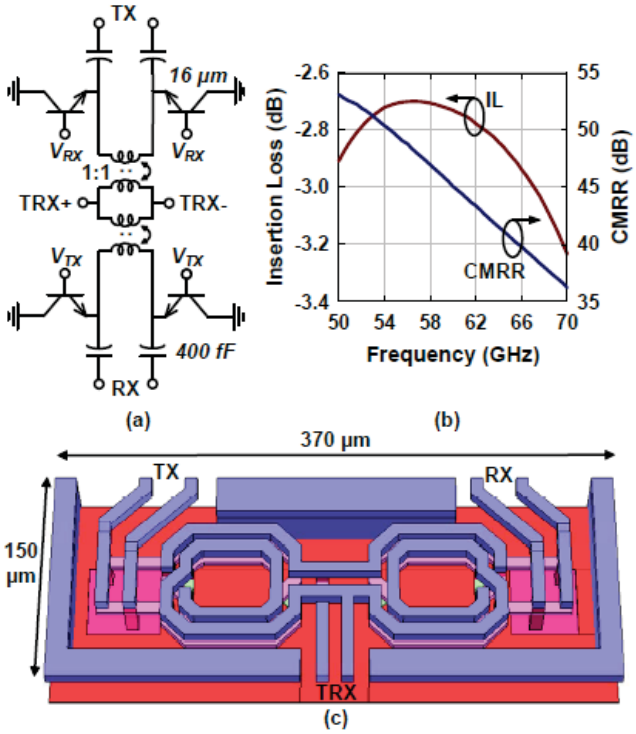



**Figure 5: (a) Schematic of the SPDT Switch, (b) Simulated Insertion Loss and CMRR, and (c) Layout of the high Common-mode Rejection SPDT Switch Transformer**

The LNA is based on a single-stage cascode design with gain peaking inductors (80 pH) and achieves 7.5 dB gain and 4.2 dB NF (Figure 6(a)). The LNA input matching is embedded into the transformer-based SPDT which favors the output $P_{1dB}$ of the TRX channel. This degrades the LNA NF by 1-1.5 dB as compared to a lumped-element SPDT switch with λ/4 networks. The vector modulators consist of a λ/4-coupled transmission lines to generate I and Q vectors and two variable gain stages ([4], [29], [30]) (Figure 6(b)). The I and Q vectors are scaled using 5-bit current DACs and summed at the outputs. The VGA and PA are co-designed for the best performance as shown in Figure 6(c). The 5-bit VGA is based on a cascode design and uses a current-steering method to achieve gain control. A Class-A cascode design is chosen for the PA with 20 pH degeneration inductors for improved linearity and interstage matching with the VGA. The simulated output $P_{1dB}$ and $P_{sat}$ are 3 dBm and 5 dBm, with a power-added efficiency (PAE) of 7% and 10%, respectively.

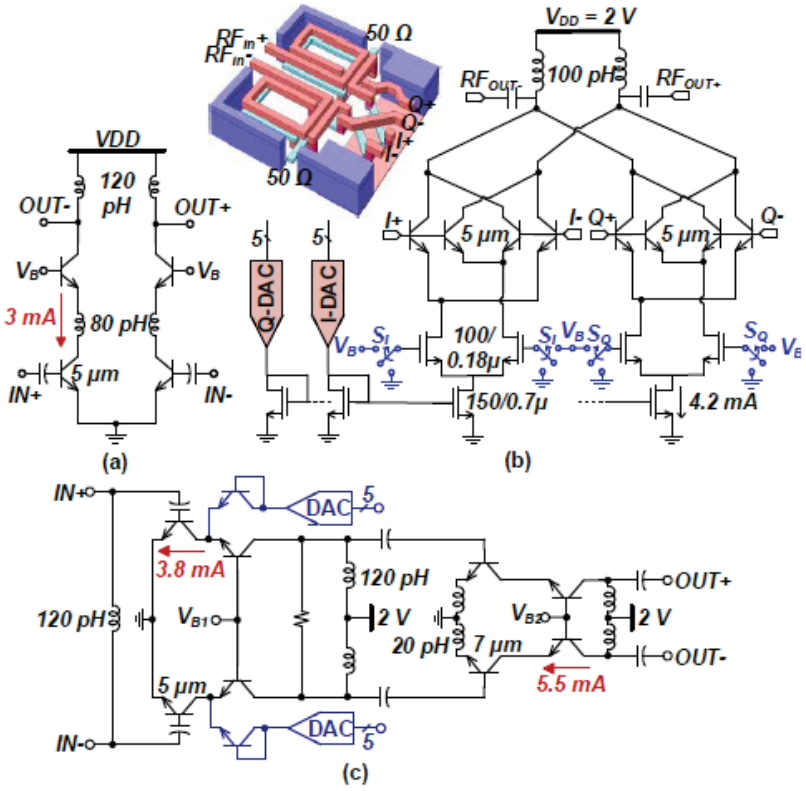



**Figure 6: Schematics of the (a) LNA, (b) Vector Modulator, and (c) VGA with 5-bit Gain Control and the PA**

Figure 7(a) presents the TRX phased-array channel breakout. Two baluns are used to allow for single-ended measurements, and their loss is deembedded so that the reference planes are at the common port of the SPDT T/R switches. The measured S-parameters show a peak gain of 24 dB with a 3 dB bandwidth of 56-66 GHz and < 1.1 dB rms gain error at 54-66 GHz for the Tx and Rx modes (Figure 7(b) and (c)). The Rx phase states show no cross-over and the rms phase error is < 8° at 54-66 GHz (Tx phase states are nearly identical and not shown for brevity) (Figure 7(d)). The measured input $P_{1dB}$ and third-order intercept point (IP3) are -27 dBm and -19 dBm in the Rx mode, and output $P_{1dB}$ and IP3 are 0 dBm and 10 dBm in the Tx mode at 60 GHz (Fig. 7(e)). The TRX phased-array channel achieves 4+5-bit, 20 dB gain control with 23° relative phase change between the highest and lowest gain states in the Rx mode (Figure 7(f) and (g)). However, the first 8 dB of gain control results in < 6° of phase change, and thus allows for compensating the gain variation across multiple channels without any additional phase calibration. Note that the VM can achieve <4° root mean square (rms) phase error, however its power consumption was reduced by 20-30% along with the other blocks in the TRX channel so as to mitigate the temperature effects in the 64- and 256-element arrays. Reported breakout measurements reflect the low-power operation. The VGA, PA, and VM in the TRX channel employs similar circuitry as [4], and are modified for compactness.

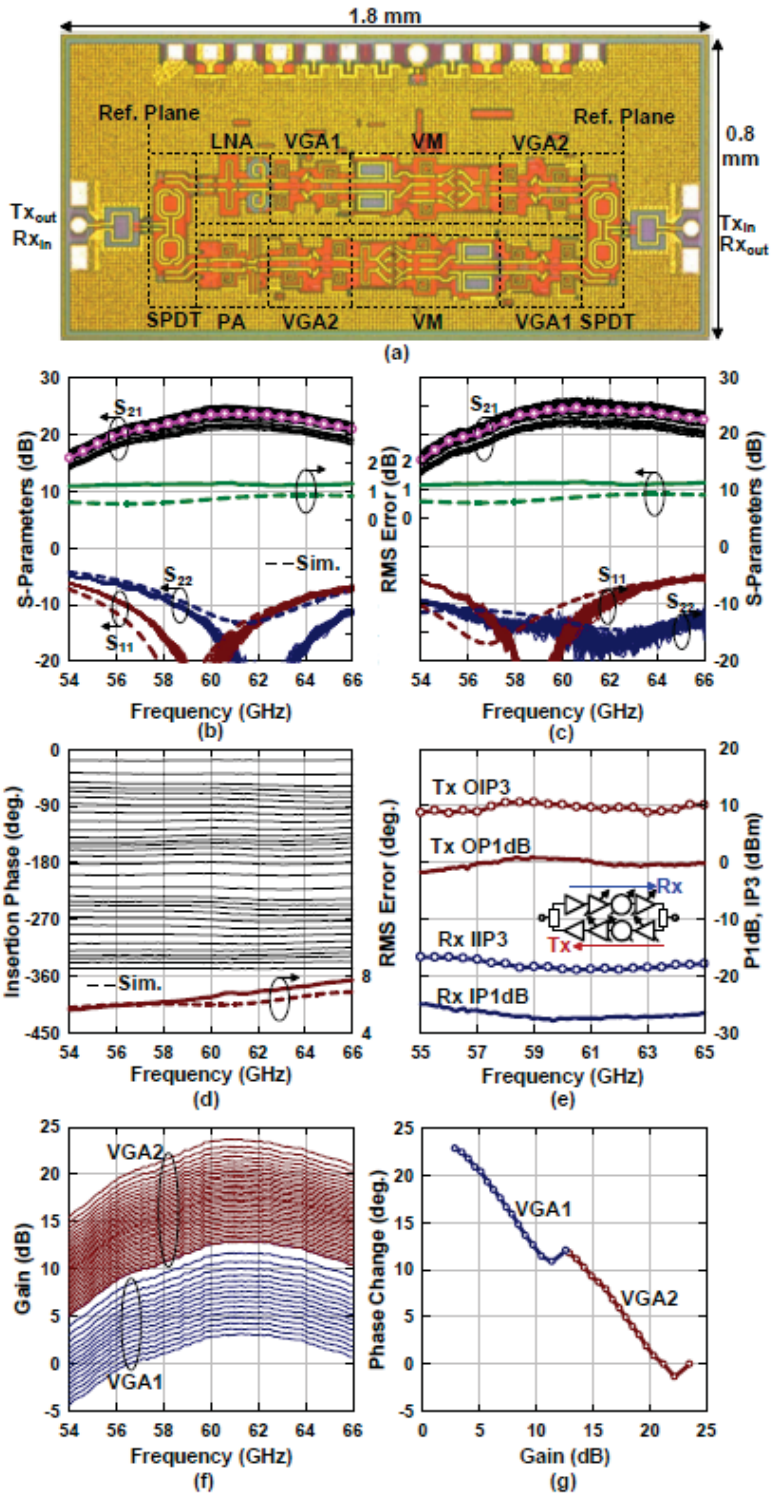



**Figure 7: Microphotograph of the TRX Channel Breakout**

*Measured S-parameters of the TRX channel in the (b) Rx mode and (c) Tx mode. Measured (d) Rx phase states and rms error, (e) Tx OP1dB and OIP3, and Rx IP1dB and IIP3, (f) Rx gain states and (g) relative phase change over gain states at 60 GHz.*

## 2.5 Nested Wilkinson Combiner and Branchline Coupler

The nested Wilkinson combiners are based on differential GSSG λ/4 transmission lines (Figure 8(a)). For a compact design, the V- and H-polarized Wilkinson combiners are intertwined with a total area of 0.22 x 0.7 $mm^2$ and result in 0.8 dB ohmic loss and 28 dB isolation for the V- and H-polarized paths. The coupling between V- and H-ports is < -47 dB at 40-80 GHz.

The branchline coupler (BC) is used only at the sum point of each 4x8 sub-array and allows to feed the array from two different ports (P1 or P4) which is essential for scalability (see Figure 1). For example, if the signal is present at P1, then P4 becomes an isolation port, and vice versa. Therefore, P1 and P4 can be connected to two independent transceivers with only one being active at a time. In this case, the H-tree distribution can be maintained as the array size increases. The simulated ohmic loss is 1 dB at 60 GHz with < -20 dB return loss at each port, and > 20 dB isolation at 56-64 GHz. The amplitude and phase mismatch between P2 and P3 is < ± 0.25 dB and < ±1.5° at 56-70 GHz, respectively (Figure 8(b)).

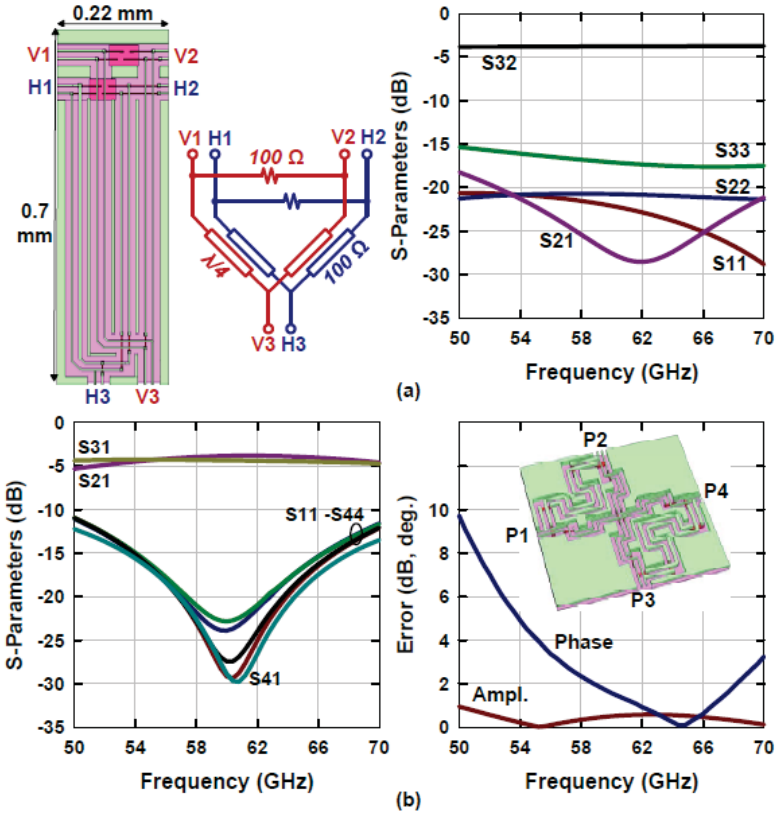



**Figure 8: (a) Nested Differential Wilkinson Divider and (b) Branchline Coupler: Layout and Simulations**

The nested distribution network is shown in Figure 9(a) for a 2x2 sub-array. A dual-polarized architecture with separate antennas does not allow for a symmetrical distribution network due to cross-overs and unequal transmission line lengths. Yet, it is possible to design the distribution

network to have equal phase from the line amplifier (LA) port to the TRX channel input port by adjusting the transmission line lengths. The equi-phase approach greatly simplifies the array calibration as seen in Section 2.10. Each cross-over employs two orthogonal differential transmission lines with a simulated coupling of < -80 dB. The 8x8 array RF-distribution network has a simulated amplitude error of ±0.5 dB and a phase error of ±7.5º across the 54-66 GHz band (Figure 9(a) and (b)).

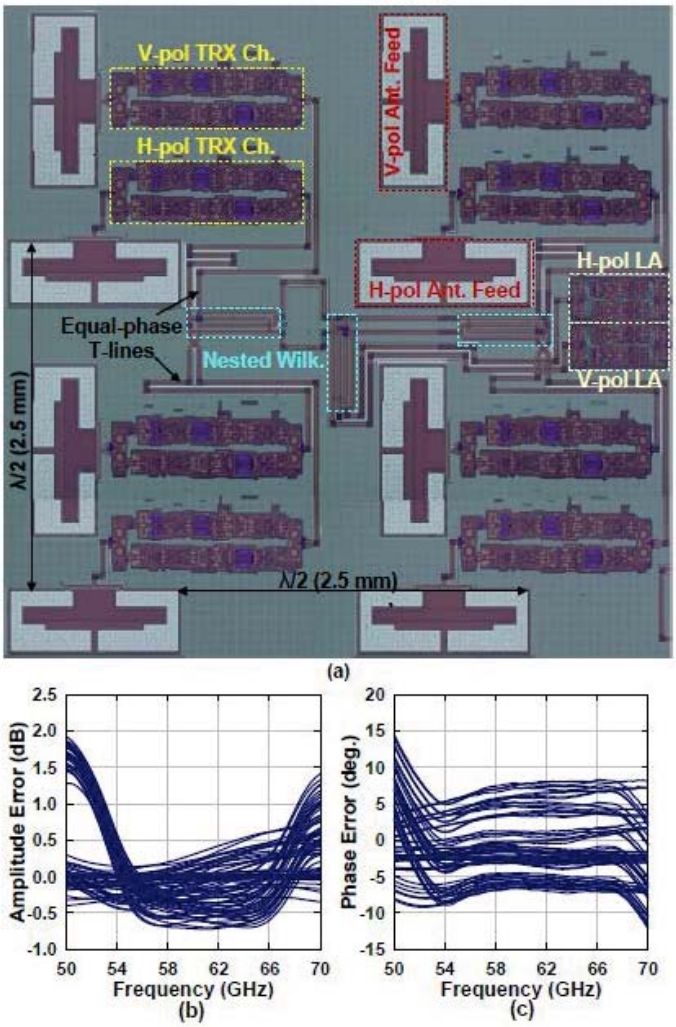



**Figure 9: (a) Microphotograph of the 2x2 Sub-array with Dual-polarized Antennas, V and H TRX Channels and Nested Distribution Network; Simulated Residual (b) Amplitude; and (c) Phase Error of the 8x8 Array Distribution Network**
*(90º phase difference from the branchline coupler is compensated)*

**Bidirectional Line Amplifier**

The bidirectional LA is based on two-stage differential cascode amplifiers and two SPDTs (Figure 10(a)). A Class AB design is adopted for the second stage to compensate the unforeseen loss in the distribution network which may cause early compression and reduced radiated power in the Tx mode. In the small-signal region, the second stage consumes 20 mW (10 mA from

2 V). If needed, the LA can deliver up to 6 dBm with a power consumption of 90 mW; however, the system measurements show that the all the LAs stay in the small-signal region. The LA achieves 4-bit gain control using the current DACs in the first stage. The diode connected BJTs steer the current from the main branch at the common-source (CS)/common-gate (CG) node and reduces the gain. The differential SPDT employs reverse-saturated BJTs and lumped-component λ/4 impedance transformation network to switch between Tx and Rx modes with high isolation. The simulated insertion loss, isolation and input $P_{1dB}$ are 2.2 dB, 22 dB and 20 dBm at 60 GHz, respectively.

The measured results of the LA breakout are presented in Figure 10(b) and Figure 10(c). The LA has 15.5 dB gain (sim. 18 dB) at 60 GHz with 54-65 GHz 3-dB bandwidth (Figure 10(b)). The measured output $P_{1dB}$ is 6 dBm and agrees well with the simulations (Figure 10(c)). However, the input $P_{1dB}$ is increased by 3 dB due to the reduced gain and is -8 dBm at 60 GHz. The bidirectional LA has 4-bit gain states with 10 dB control range. The relative phase change versus gain states is < 5° for the first 5 dB of gain control, simplifying array calibration.

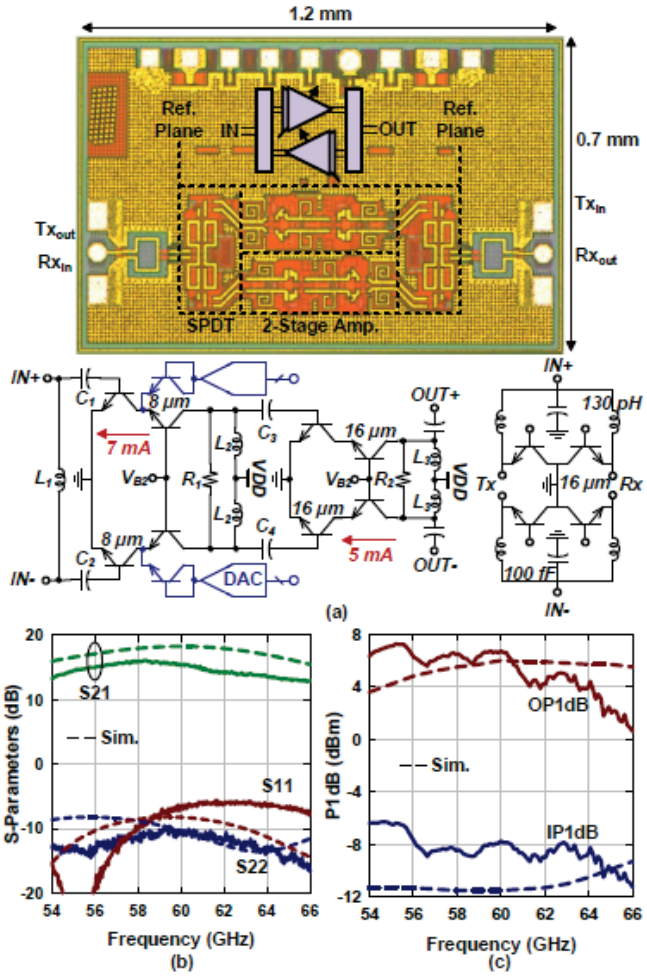



**Figure 10: (a) Microphotograph and Schematic of the Bidirectional Line-Amplifier Breakout. Measured (b) S-parameters and (c) IP1dB and OP1dB.**

## 2.6 LO Multiplier Chain and Up/Down Converter

The scalability of the 60 GHz wafer-scale phased-array is not feasible if implemented solely in the RF domain due to the high ohmic loss and bondwire effects at 60 GHz. Therefore, an up/down converter is needed at the 64-element common port for scalability at the IF and LO levels. An IF of 8 GHz and an LO of 52 GHz is obtained by using a quadrupler with an input frequency of 13 GHz.

### LO Multiplier Chain

Figure 11 presents the LO multiplier chain. The LO pre-driver is a single-stage common-emitter design with a simulated gain and output $P_{1dB}$ of 10 dB and 3 dBm at 13 GHz, respectively and ensures that the Blass-B quadrupler is driven with sufficient power. The two doublers that constitute the quadrupler are show in Figure 11 (b), (c) and are biased for Class-B operation. Both doublers employ a transistor pair and cascode stage to amplify the $2f_0$ signal, and their passive componenets are scalled with frequency. The 13-26 GHz and 26-52 GHz doublers consume 7.5 mA and 13 mA, respectively, at saturation and deliver 2.5 dBm to the 52 GHz LO driver. The simulated harmonic rejection ratio (HRR) is > 25 dBc and is limited by the $8^{th}$ harmonic (104 GHz) [31]. The 52 GHz LO driver is placed after the quadrupler and VM. It is driven to saturation by the previous stages and delivers 6 dBm at 52 GHz to the double-balanced mixers (Figure 11(d)). The entire LO multiplier chain has > 37 dBc HRR at 52-60 GHz (Figure 11(e)) with the additional harmonic rejection provided by the LO driver tuned at 52 GHz. The HRR simulations assume that the transistors are matched, and include the sub-harmonics and fundamental frequency components.

The required LO input power to drive the LO chain is -10 dBm, and one LO path is used to feed both V- and H-transceivers. Therefore, a resistive LO divider is used with 6 dB insertion loss. Considering the transmission line (-2.5 dB), input balun (-1.5 dB) and resistive divider loss, the required LO input power at 13 GHz at the 64-element phased-array chip input is 0 dBm.

Note that the TRX channel vector modulator is reused between the quadrupler and the LO driver to adjust the LO phase between multiple 64-element arrays [32]. This allows for a single-point phase adjustment between different 8x8 sub-arrays, and is much better than using the TRX channel settings and a 64-point phase adjustment scheme.

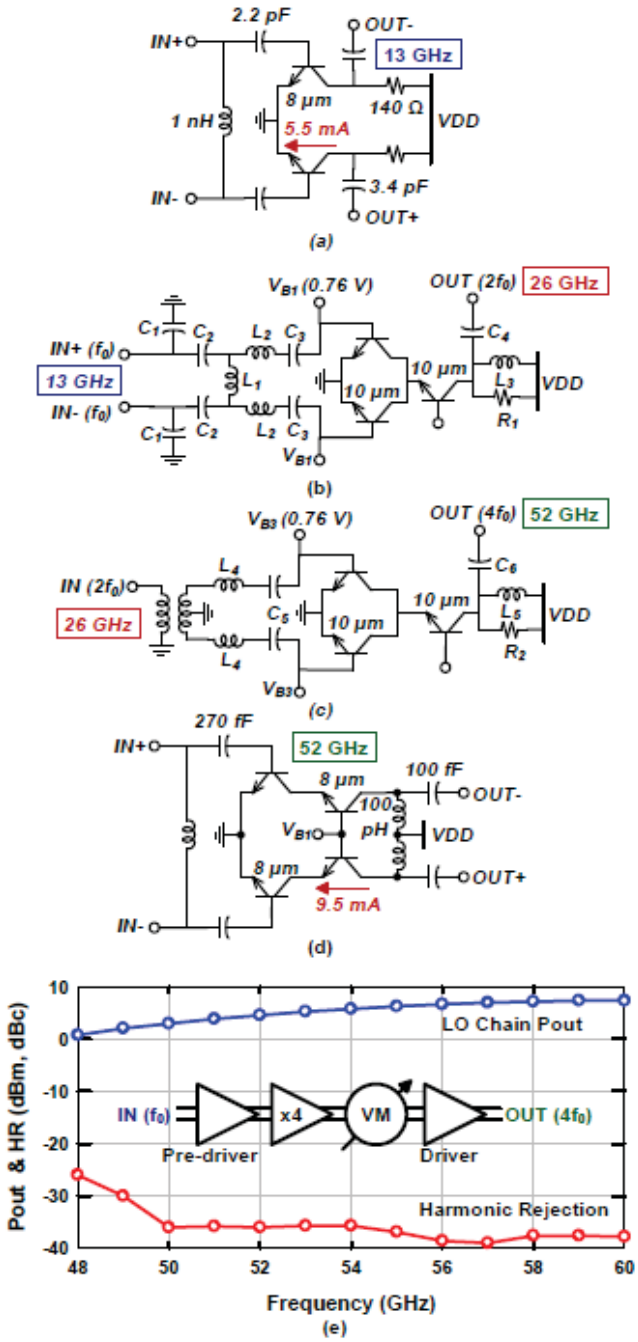



**Figure 11: Schematics of the (a) LO Pre-driver at 13 GHz, (b) Doubler at 13-26 GHz, (c) Doubler at 26-52 GHz, (d) LO Driver at 52 GHz, and (e) Simulated Output Power and HRR at 52 GHz**

### Up/Down Converter

The up/down converter consists of two double-balanced active mixers, SPDT switches at IF and RF for bidirectionality, and an IF amplifier in the Rx path (Figure 12). Since the signals from the 64-TRX channel are combined coherently, the down-converter must be highly linear, and therefore no amplifier is used before the mixer. A 60 pH emitter degeneration inductor is also

employed to further increase the input linearity (Figure 13(a)). The simulated Rx mixer conversion gain, input $P_{1dB}$ and NF are 1 dB, -2.4 dBm and 10.6 dB, respectively, at 60 GHz.

Unlike the down-conversion mixer, the up-conversion mixer creates two problems: LO leakage and image which can saturate the TRX channels and mitigate the radiated output power. The LO leakage is created by mismatch between transistors during fabrication. The solution is to place two current DACs and generate a dc offset between two branches to reject the LO (Figure 13(b)). The current DACs have 5-bit control with 1 mA range which is enough to compensate ±10% mismatch between branches [33]. The image problem is less significant than the LO leakage since it occurs at 47 GHz when LO is at 54 GHz and IF is at 7 GHz. The stages after the up-conversion mixer are tuned structures and suppress the image by A 60 dB. The simulated conversion gain and output $P_{1dB}$ are 11.9 dB and -4.6 dBm, respectively, at 60 GHz.

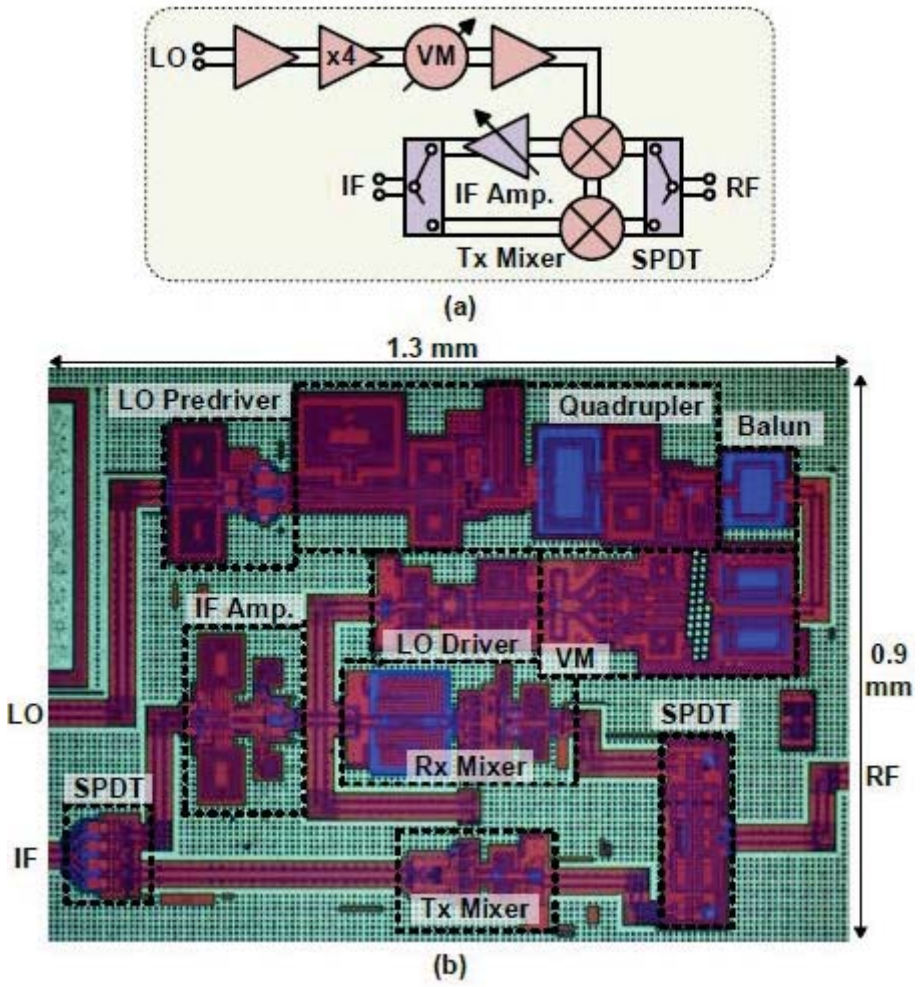



**Figure 12: (a) Block Diagram and (b) Microphotograph of the Up/Down Converter**

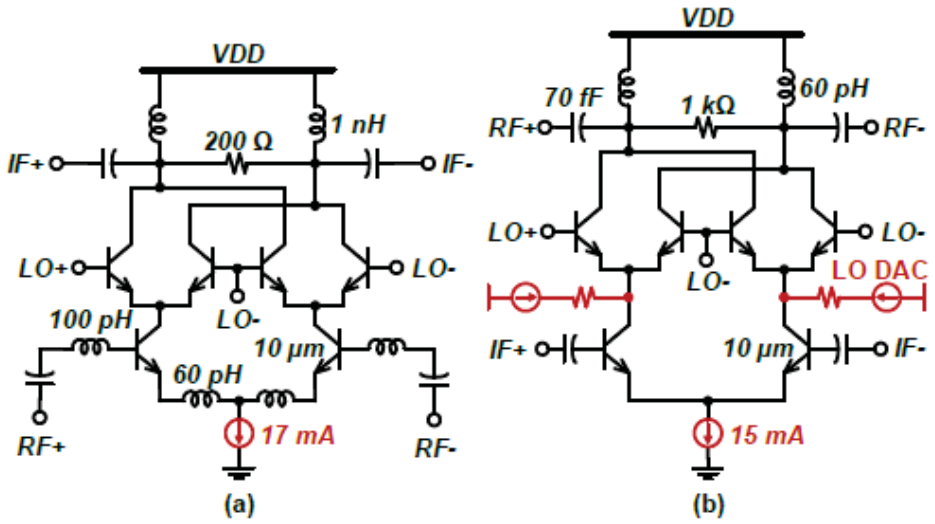



**Figure 13: Schematics of the (a) Down-conversion (Rx) Mixer and (b) Up-conversion (Tx) Mixer with 5-bit LO Leakage Tuning DACs**

A single-stage common-emitter IF amplifier is used in the Rx path after the down-conversion mixer (Figure 14(a)), with input matching achieved using shunt 80 Ω resistors. The simulated gain, input and output $P_{1dB}$ are 11 dB, -3 dBm and 7 dBm at 8 GHz, respectively. The IF SPDT employs series and reverse-saturated shunt BJTs (Figure 14(b)) with 1.5 dB insertion loss at 8 GHz. On the RF side, an SPDT switch similar to the bidirectional line amplifier is employed.

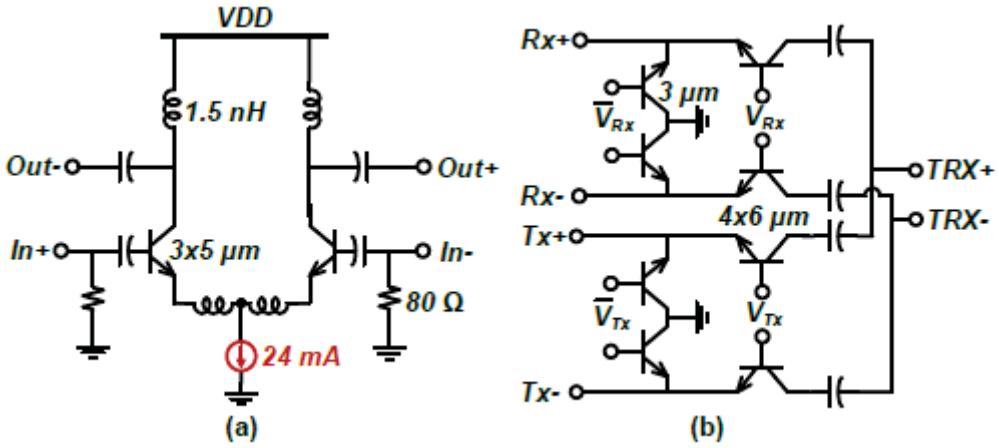



**Figure 14: Schematics of the (a) IF Amplifier in the Down-conversion Path and (b) IF SPDT Switch**

The simulated gain, input and output $P_{1dB}$ of the up/down converter in the Rx mode are 10 dB (56.4-62.7 GHz 3-dB bandwidth), -6 dBm and 3 dBm, respectively, at 60 GHz. The simulated NF is 12 dB, but this has no effect on the system NF due to the high-gain TRX channel (24 dB) and RF LAs (15 dB) (Figure 15(a)). In the Tx mode, the up-converter achieves 6.6 dB gain (54-66 GHz 3 dB bandwidth), -14 dBm input $P_{1dB}$ and -6.7 dBm output $P_{1dB}$ at 60 GHz which is sufficient to drive each LA and TRX channel in the array (Figure 15(b)). The up/down converter

with the LO multiplier chain consumes 110 mW and 160 mW in the Tx and Rx modes, respectively, using a VDD of 2 V.

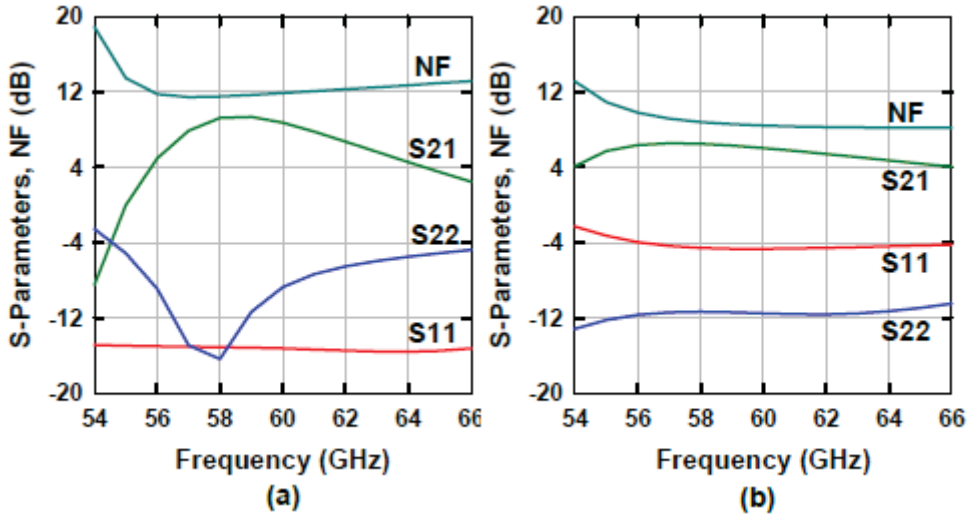



**Figure 15: Simulated S-parameters of the Up/Down Converter in the (a) Rx Mode and (b) Tx Mode**

## 2.7 Control and Feed Network Design

### SPI and PTAT Current Generation

The 64-element phased-array transceiver is controlled by a single serial-peripheral interface (SPI). The SPI module operates with a clock speed up to 100 MHz and features a global enable pin, which allows the user to preload all the phase and gain states without disturbing the current beam. The SPI module also features a fast-switching mechanism that can set the Tx/Rx mode in the entire array without reloading the registers.

The scalability requirement creates a need for a special access for digital pads. If the digital pads are located only at the South edge of the reticle, then only the South two reticles of the 256-element array would have digital access to the PCB. Therefore, at least two sets of digital pads are required per reticle. For this work, the digital pads are located at the North and South edges of each reticle with two additional pads that can activate/deactivate these two sets of digital pads at the North/South edges. Also, only one micro-controller (master) is needed to control 16 SPI slaves due to four hardwired address pins featured in the SPI module, and this facilitates the digital communication for larger arrays.

The bias currents are generated using a proportional-to-absolute-temperature (PTAT) current source with external bias option. The PTAT current reference can be controlled by ±30%. All the digital and bias pads have electro-static discharge (ESD) protection and power clamp circuitry.

## 2.8 Circuits for Scalability: IF Splitter, IF Line Amplifier, and LO Line Amplifier

Referring to Figure 16, several IF and LO amplifiers are used to allow the 64-element array to scale to 256- and 1024-element arrays. Differential IF and LO splitters are used to direct the signal to the required path, and six of them are employed in the reticle to ensure scalability and different IF feeds on four corners of the reticles (see Figure 16 bottom right). The switch is based on wideband series and reverse- saturated BJT switches on four branches and can be used in two modes: pass and division. In the pass mode, the signal can be directed between any two ports with an insertion loss, while in the division mode, the signal can be directed to any two ports with an insertion loss and 3 dB division loss. Since, the division mode is widely used due to the H-tree distribution scheme, the matching network is designed for the division mode. For example, if the signal is directed from West to North and South ports, the impedance seen from West port is 25 Ω. In order to match 25 Ω to 50 Ω, one can employ a lumped-element matching network which would lead to a non-compact design at 8 GHz. However, since the IF splitters are required to be routed along the 21 mm edges of the silicon chip, then instead of using 50 Ω transmission lines, a 4.5 mm quarter-wave impedance transformer with 35 Ω characteristic impedance is used for matching at 8 GHz on all four branches. Simulations on the IF splitter show a return loss < -10 dB, insertion loss of 7.4 dB and 10-13 dB in the pass and division modes, respectively, with input $P_{1dB}$ of 15 dBm at 8 GHz.

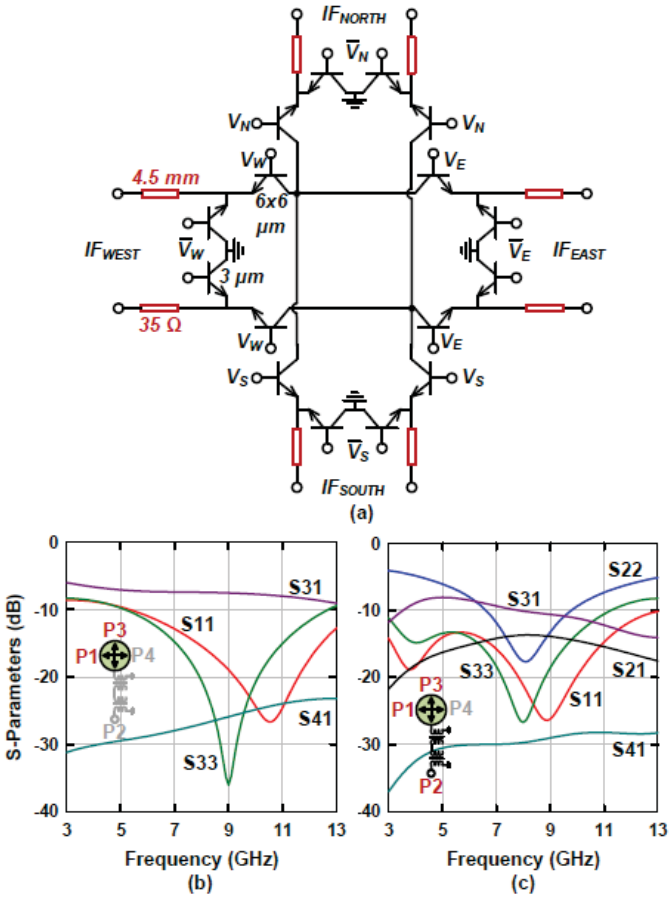



**Figure 16: (a) Schematic of the IF Splitter, Simulated S-parameters of the IF Splitter in the (b) Pass Mode, and (c) Division Mode**

The bidirectional IF LA is presented in Figure 17. It is a true-differential design based on a common-emitter topology in the first stage and a cascode topology in the second stage, and two SPDT switches for bidirectionality. The gain control is achieved by adjusting the tail current of the first stage with 4-bit current DACs and 15 dB gain control range. The simulated peak gain is 24 dB with 2.7-9 GHz 3-dB bandwidth. The IF LA delivers > 3 dBm output power with an input $P_{1dB}$ > -20 dBm at 5-10 GHz.

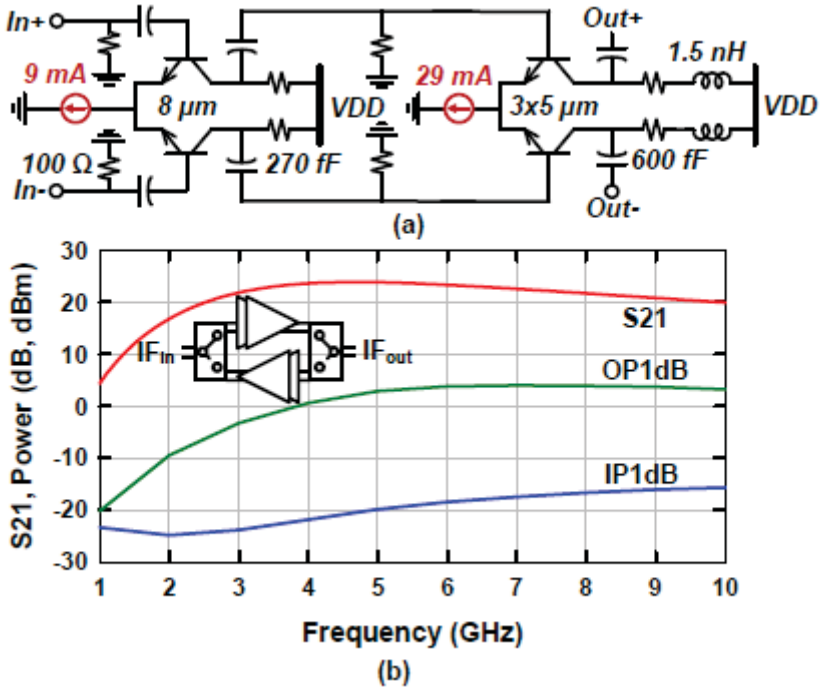



**Figure 17: (a) Schematic of the IF LA and (b) Simulated Gain, IP1dB, and OP1dB of the IF LA**

A unidirectional differential Class A LO line amplifier is shown in Figure 18(a). Similar to the IF LA, it employs a common-emitter and cascode topologies in the first and second stages, respectively. The LO LA is designed to ensure enough LO power is delivered to drive the transceiver, therefore, it has 11 dBm output power at 10-16 GHz. The simulated gain is 24.5 dB and this reduces the required input power to -12 dBm at the LO line amplifier input port (Figure 18(b)). For a 256-element array, the simulated loss prior to the LO line amplifier is 21 dB (LO splitter loss + t-line loss), and therefore, an LO power of 9 dBm would be required at the 256-element array input to saturate the LO LA. A 4-bit gain control is employed in the second stage so as to reduce the output power if desired.

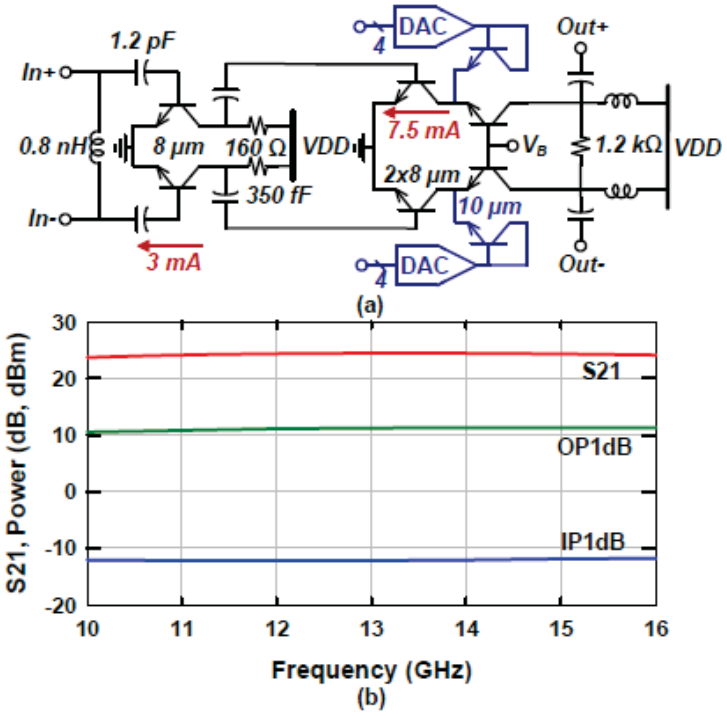



**Figure 18: (a) Schematic of the LO LA and (b) Simulated Gain, IP1dB, and OP1dB of the LO LA**

## 2.9 64-Element Phased-Array System Level Calculations

The directivity and EIRP of a phased-array is calculated using:

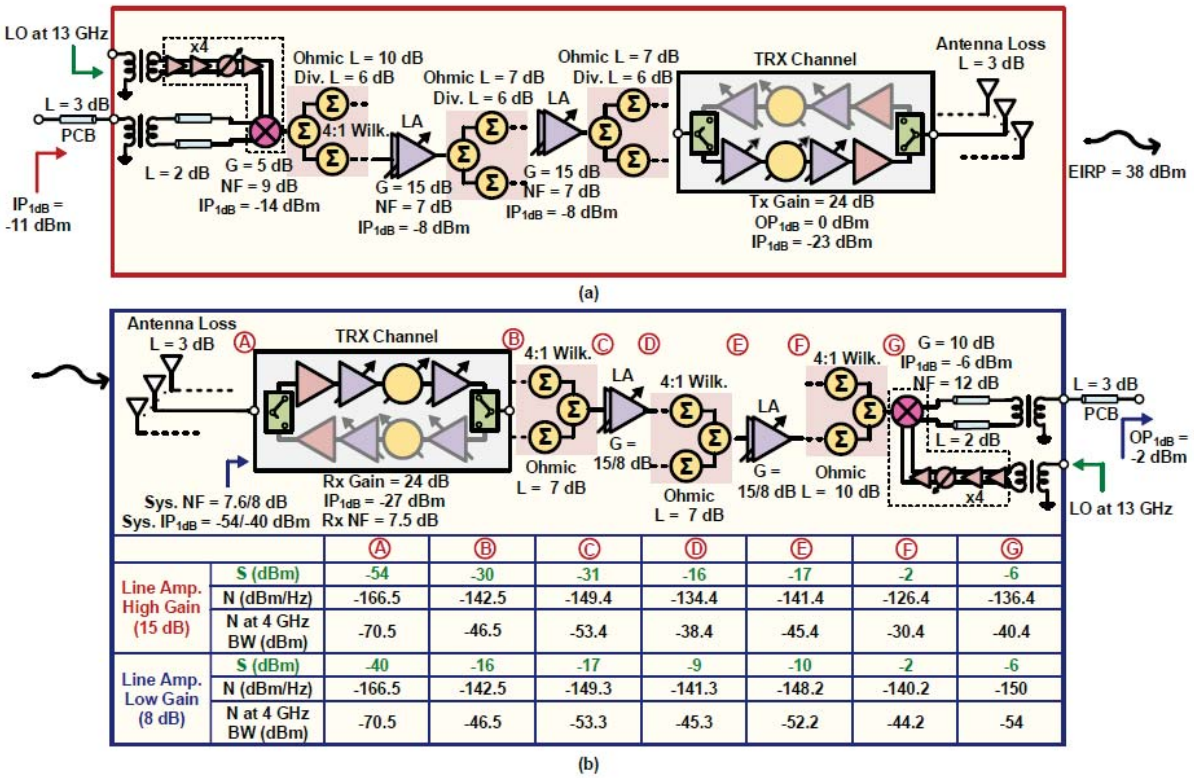
$$D = \frac{4\pi}{\lambda^2}\,(N_x d_x)(N_y d_y) \qquad (1)$$

$$EIRP = P_{\text{out}} + 10log(N_x N_y) + 10log(D) - L_{\text{ant}} \qquad (2)$$

where λ is free-space wavelength, $N_x$ and $N_y$ are the number of elements in the x- and y-directions, $d_x$ and $d_y$ are the spacings between each antenna in the x- and y-directions, $P_{out}$ is the power delivered by each TRX channel and $L_{ant}$ is the total loss due to antenna efficiency and transmission lines from the TRX channel to the on-chip EM feeds. A directivity of 23 dB is obtained for a 64-element array with λ/2 spacing. Assuming 50% worst-case on-chip antenna efficiency, an output power per element at $P_{1dB}$ of 0 dBm, the calculated EIRP for a 64-element array is 38 dBm.

Figure 19 presents the system-level calculations for the 64-element phased-array. The Tx channel gain is 24 dB with an output $P_{1dB}$ of 0 dBm (input $P_{1dB}$ = -23 dBm). The 1:64 nested Wilkinson combiner/divider network has an ohmic and division loss of 40 dB in the Tx mode. In order to compensate this loss, two line amplifiers with 15 dB gain are placed at the common

nodes of every 2x2 and 4x4 sub-arrays so as to distribute the gain and loss uniformly throughout the array. Therefore, in order to drive the entire array, the required power at the up-converter output is -11 dBm, but the up-converter is designed to have an output $P_{1dB}$ of -7 dBm so as to have enough margin if the distribution network loss increases after fabrication. The LO is suppressed in the double side-band up-converter mixer using the DAC currents and the total radiated LO power is < 30 dB than the RF signal.




| | | Ⓐ | Ⓑ | Ⓒ | Ⓓ | Ⓔ | Ⓕ | Ⓖ |
|---|---|---|---|---|---|---|---|---|
| Line Amp. High Gain (15 dB) | S (dBm) | -54 | -30 | -31 | -16 | -17 | -2 | -6 |
| | N (dBm/Hz) | -166.5 | -142.5 | -149.4 | -134.4 | -141.4 | -126.4 | -136.4 |
| | N at 4 GHz BW (dBm) | -70.5 | -46.5 | -53.4 | -38.4 | -45.4 | -30.4 | -40.4 |
| Line Amp. Low Gain (8 dB) | S (dBm) | -40 | -16 | -17 | -9 | -10 | -2 | -6 |
| | N (dBm/Hz) | -166.5 | -142.5 | -149.3 | -141.3 | -148.2 | -140.2 | -150 |
| | N at 4 GHz BW (dBm) | -70.5 | -46.5 | -53.3 | -45.3 | -52.2 | -44.2 | -54 |

**Figure 19: System-level Calculations for the 64-element Phased-array in the (a) Tx and (b) Rx Modes**

The Rx mode electronic gain in the array, referenced to the TRX channel input port, is given by:

$$G_{Rx} = \frac{P_{IF}}{S * A_{phys} * \varepsilon_{ant}} \qquad (3)$$

where $P_{out}$ is the output IF power, S is the incident plane wave intensity, $A_{phys}$ is the antenna aperture, $\varepsilon_{ant}$ is the antenna efficiency. The Rx channel gain is 24 dB, followed by a total Wilkinson combiner loss of 24 dB and line amplifier gain of 30 dB. This, together with a down-converter gain of 10 dB, IF balun/t-line loss of 2 dB, PCB t-line loss of 3 dB, results in a system electronic Rx gain $G_{Rx}$ = 35 dB. If the power is referenced to the antenna aperture with $\varepsilon_{ant}$ = 3 dB, then the array electronic Rx gain becomes $G_{arrayRx} = P_{IF}/P_{on\text{-}aperture}$ = 32 dB. The simulated system NF, referenced to the channel input is 7.6 dB, and is nearly equal to the TRX

channel NF due to the TRX gain of 24 dB. The NF is 10.6 dB when referenced to the antenna aperture.

The system input $P_{1dB}$ is limited by the down-converter, and is -54 dBm and -51 dBm per channel referenced to the TRX channel port and antenna aperture, respectively. The linearity can be increased to -40 dBm/channel if the LA gain is set to 8 dB each (instead of 15 dB). The system NF increases to 8 dB (minimal change) since the TRX channel gain is still at maximum setting. This results in 13.6 dB increase in the system dynamic range while still delivering a system electronic gain of 21 dB. The system input P1dB can be further increased to -30 dBm/channel if the TRX channel gain is reduced from 4 dB to 14 dB. However, now the system NF becomes 10.5 dB with LA gain setting of 8 dB each. This setting still results in a high dynamic range, but with 2.5 dB less sensitivity than the case above, and should not be used unless large interferers are present.

## 2.10 System Measurements

The 64-element dual-polarized dual-beam wafers-scale phased-array is shown in Figure 20. System measurements are conducted in two stages: 1) on-wafer yield tests, 2) over-the-air (OTA) performance measurements.

An 8-inch SiGe BiCMOS wafer results in 52 full-reticles (21x21 $mm^2$). In order to determine the functional reticle locations prior to dicing, a yield test (direct current (DC), digital control and RF verification) is conducted on two un-diced wafers for both polarizations in the Tx and Rx modes (104 full-reticles). The average yield was > 90%.

After the yield tests, a functional 64-element array is diced and placed on a 370HR substrate 6-layer PCB with copper-plated thru-hole vias using thermally conductive epoxy. An 8x8 dual-polarized dipole antenna array is printed on a 100-µm thick quartz superstrate, attached on the wafer-scale phased-array and aligned with the on-chip EM feeds under a microscope. The size of the quartz superstrate antenna array is 20x20 $mm^2$ and ensures that the bondpads are available for bonding. Care is taken to minimize the air gap between on-chip EM feeds and the dipole antennas. Simulations show a 40-µm air gap causes a center-frequency shift from 60 GHz to 69 GHz and results in 20 dB drop in antenna efficiency at 60 GHz. A heat sink and a small fan are placed at the back of the PCB to dissipate the heat. Finally, vdd, digital control and IF/LO pins are bonded to the PCB (Figure 20(c) and (d)). The 64-element phased-array consumes 9.4 W and 7.9 W in the Tx and Rx modes, respectively, per polarization. A power breakdown is presented in Table 1.

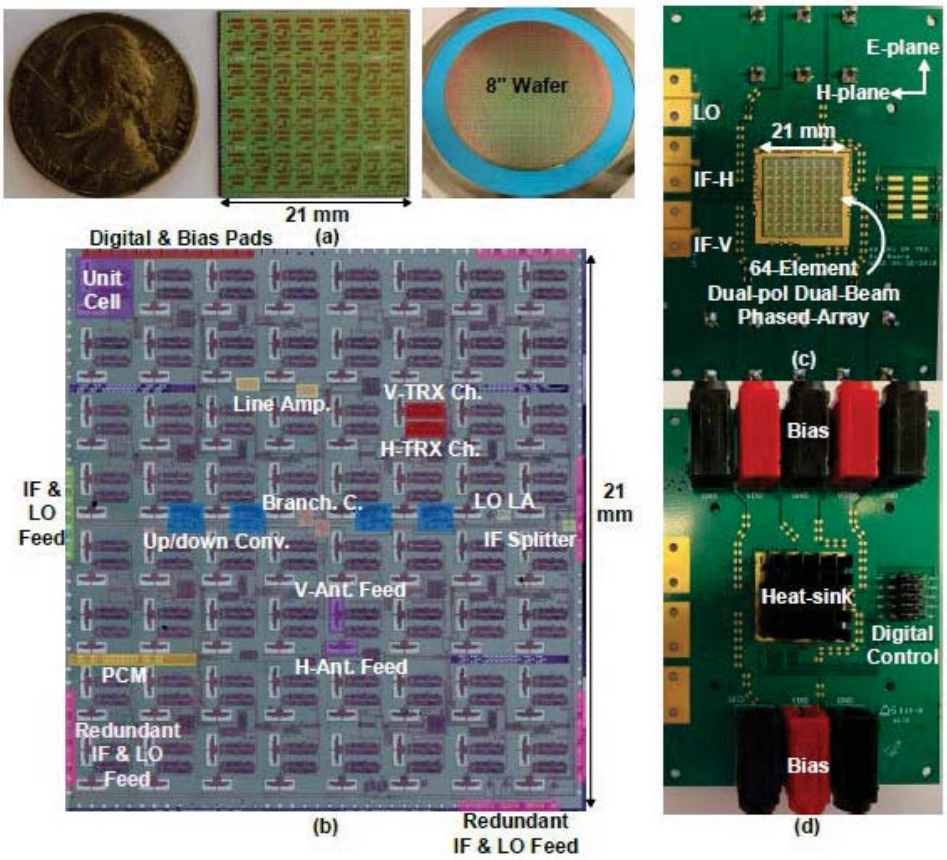



**Figure 20: (a) Picture of the 64-element Phased-array Chip with a Quartz Superstrate Antenna and as delivered on an 8-inch Wafer; (b) Expanded View of the 64-element Wafer-scale Phased-array; (c) Front; and (d) Back Views of the Assembled 64-element Phased-array Board**

**Table 1. 64-Element Phased-Array Power Breakdown**

| | Rx | Tx |
|---|---|---|
| 64 x TRX Channels | 5.1 W | 6.4 W |
| 20 x Line Amp. | 1.5 W | 1.5 W |
| 1 x Up/Down Conv. | 0.2 W | 0.15 W |
| Bias | 1.06 W | 1.36 W |
| Total | 7.86 W | 9.4 W |

Note: VDD of 2.4 – 2.5 V instead of 2 V is used due to IR drop

**Pattern, EIRP, and Miscellaneous Measurements**

The pattern measurements are done in an anechoic chamber with a standard gain WR-15 horn antenna placed 32 cm away from the 64-element array (the far-field range is $2D2/\lambda = 16$ cm at 60 GHz). The array is fully turned on with no dysfunctional channels or amplifiers, and the phase states are loaded to the TRX channels to compensate for the 90° phase shift caused by the branchline coupler as well as the ±30X phase error between channels (no amplitude calibration was done for ±3 dB gain variation across the array). The phase and gain variations are caused partly by the residual errors in the distribution network (see Figure 9(b) and (c)), small misalignment of the quartz antenna array and process variations (bias current mirrors, transistor sizing, etc.), and partly by the infrared (IR) drop inside the chip. The cross-polarization performance is measured by rotating the horn antenna 90° when the other polarization is turned off. The coupling measurements are done in a similar fashion with the cross-polarization measurements; however, this time both V- and H-polarized arrays are turned on.

Figure 21 presents the measured co-polarization, cross-polarization and coupling with cross-polarization patterns at three different scan angles for V- and H-polarized arrays in the H-plane (azimuth scan). The co-polarization measurements agree well with the ideal patterns and results in 12.6° 3-dB beamwidth and -13 dB sidelobe levels at 62 GHz (LO = 13.5x4 GHz, IF = 8 GHz). The cross-polarization levels are <-25 dB, and the cross-polarization plus coupling levels remain <-20 dB over all scan angles for both polarizations. The E-plane patterns and Tx mode patterns are similar, and not shown for brevity.

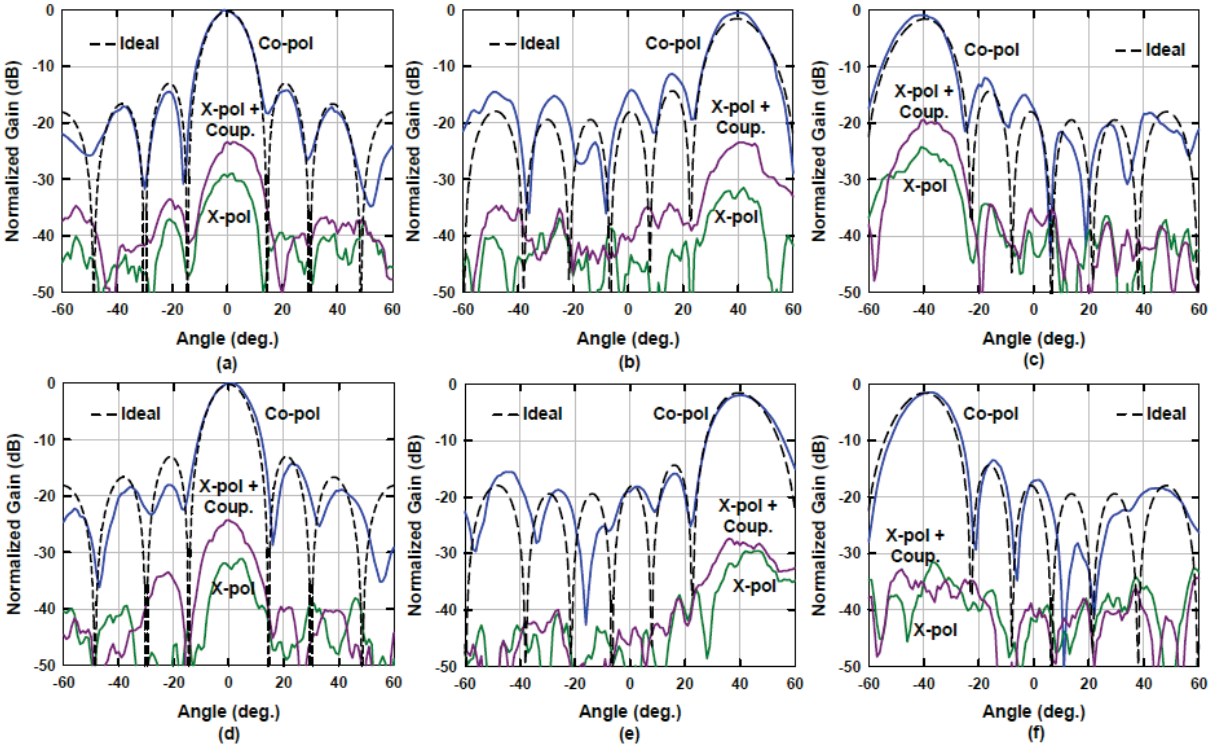



**Figure 21: Measured Patterns for H-polarized Array at (a) 0°, (b) 40°, (c) -40°, and for V-polarized Array at (d) 0°, (e) 40°, (f) -40° in the H-plane and Rx Mode at 62 GHz**
*All patterns are normalized to 62 GHz pattern at boresight.*

The 64-element phased-array is electronically scanned in the E- and H-planes for V- and H-polarized arrays in the Tx and Rx modes (Figure 22). The array scans to ±50° with no grating lobes and sidelobe levels <-13 dB in the H-plane and <-11 dB in the E-plane. The patterns for the H-polarized array in the Tx mode are nearly identical to the patterns for the H-polarized array in the Rx mode and not shown.

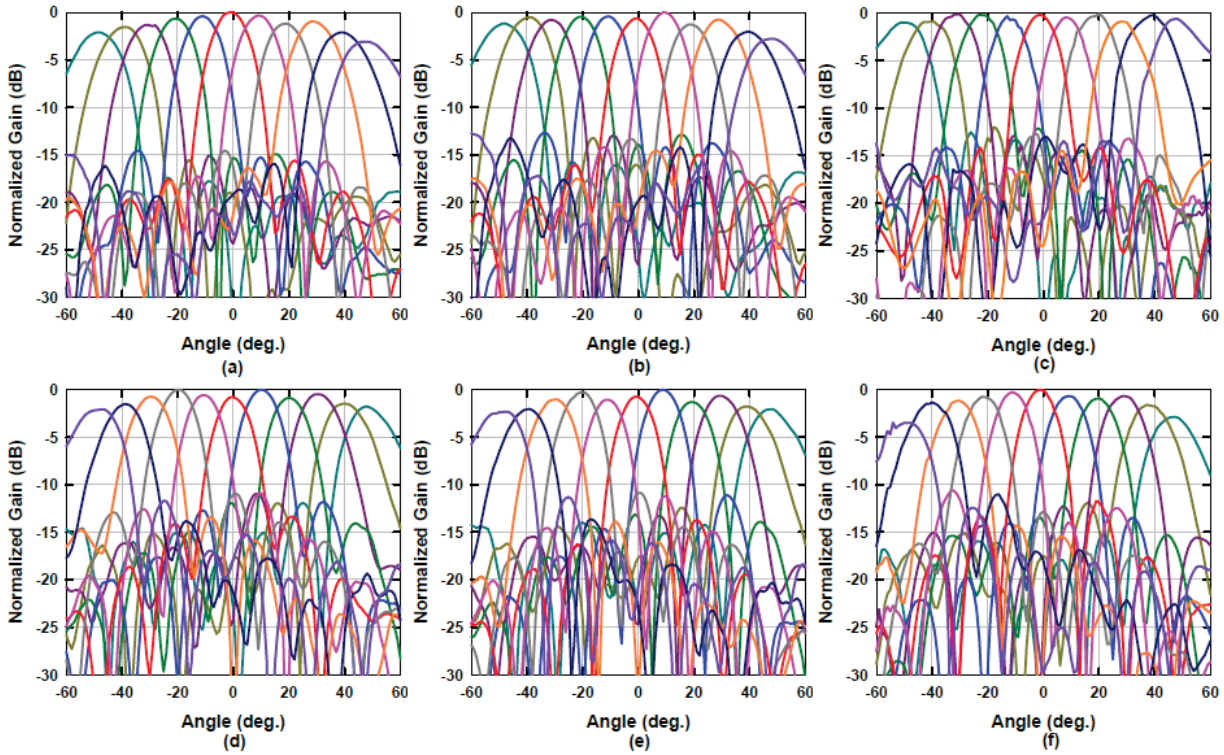



**Figure 22: Measured H-plane Patterns at 62 GHz for (a) V-polarization in the Rx Mode, (b) V-polarization in the Tx Mode, (c) H-polarization in the Rx Mode, and E-plane Patterns at 62 GHz for (d) V-polarization in the Rx Mode, (e) V-polarization in the Tx Mode, and (f) H-polarization in the Rx Mode**

The measured EIRP at $P_{1dB}$ and $P_{sat}$ versus frequency is shown in Figure 23(a) and Figure 23(b) for V- and H-polarized arrays, respectively, when only one beam is activated at a time. The peak EIRP of 36.6 dBm and 38.5 dBm is achieved at $P_{1dB}$ and $P_{sat}$, respectively for the V-polarized array with a 3-dB bandwidth of 60.7-64.2 GHz. The H-polarized array shows 35.2 dBm and 37 dBm peak EIRP at $P_{1dB}$ and $P_{sat}$, respectively with slightly larger 3-dB bandwidth (59.5-64.3 GHz). This agrees well with the simulations, and the 2 GHz frequency shift and 1-2 dB difference between calculations and measurements are due to the residual air gap (5-10-µm) between the silicon chip and the quartz superstrate antenna array. The 64-element array requires an input power of -11 dBm at the South-West IF connector port to compress by 1-dB for V- and H- polarizations (Figure 23(c) and Figure 23(d)).

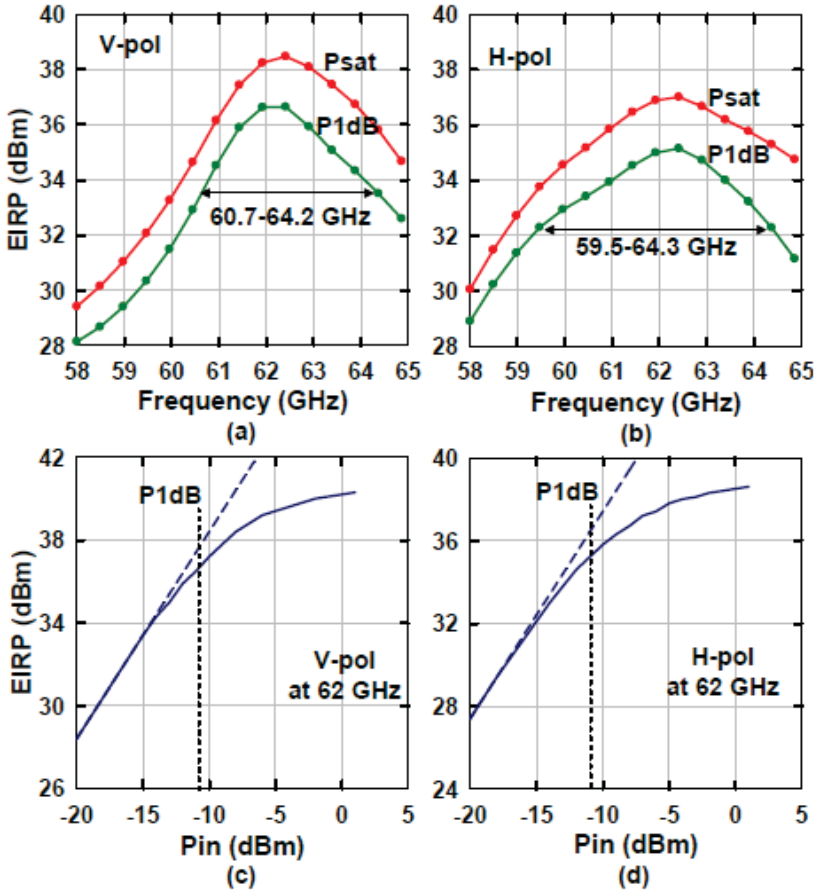



**Figure 23: Measured EIRP vs Frequency of the (a) V-polarized and (b) H-polarized, and Measured EIRP vs Phased-array Input Power of (c) V-polarized and (d) H-polarized 64-element Phased-array**

The LO leakage and image rejection are measured when the 64-element array is in the Tx mode. Figure 24(a) presents the LO leakage versus different LO DAC settings which is incorporated in the up-conversion mixer. The LO leakage is defined as the difference between the RF and LO signals at a single tuning state. Similarly, image rejection is defined as the difference between signals at RF and image frequency. At different LO frequencies, the 5-bit current DAC is swept, and a minimum LO leakage of -30 dBc is achieved at 54 GHz LO.

As the LO frequency decreases, the LO leakage also decreases due to the additional rejection from the tuned LAs and TRX channels. At 54 GHz LO and 7-8 GHz IF, the image appears at 47-46 GHz and is rejected by 60-70 dBc without any image rejection filter (Figure 24(b)). The IF is chosen high enough to place the image frequency out of band so that the following stages can substantially reject the image (17 dB, 22 dB and 15-16 dB rejection from 2xLAs, TRX channel and antenna at 47 GHz, respectively).

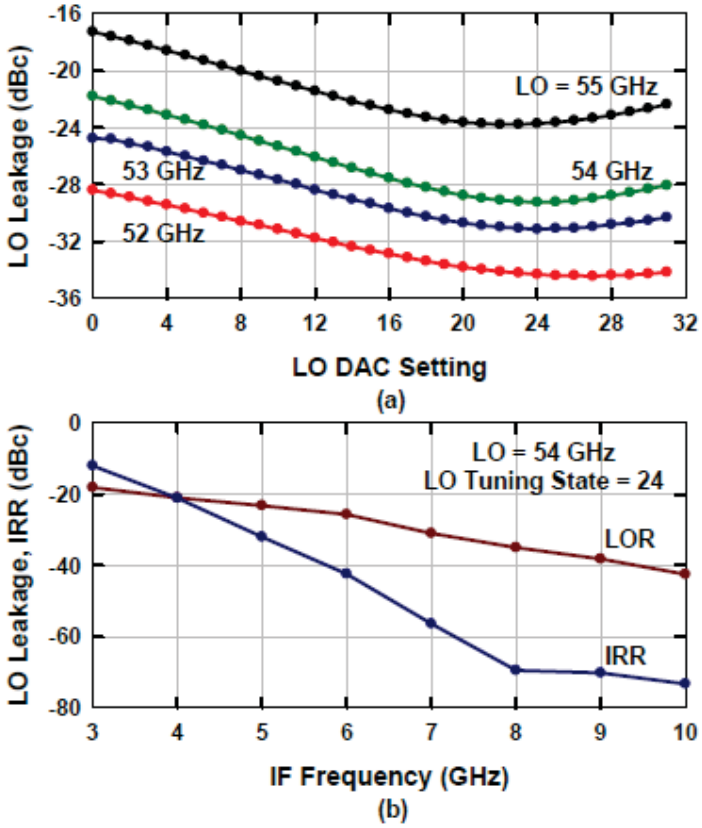



**Figure 24: (a) Measured LO Leakage at different LO Tuning Settings of the 64-element Phased-array and (b) Measured LO Leakage and Image Rejection at LO = 54 GHz**

The measured electronic gain of the array in the Rx mode is shown in Figure 25 and is referenced to the PCB South-West connector. The V-polarized array achieves 33.8 dB gain at IF = 7 GHz (RF = 62 GHz) with a 3-dB bandwidth of 5-8 GHz, and it agrees well with simulations presented in Section 2.9. The H-polarized array has a peak gain of 31.6 dB at IF = 7 GHz (RF = 62 GHz) with a 3-dB bandwidth of 5.6-8.4 GHz. The 1.4 dB difference between V-polarized and H-polarized array is due to the longer transmission line from the TRX channel to the antenna feed (Figure 25(b)).

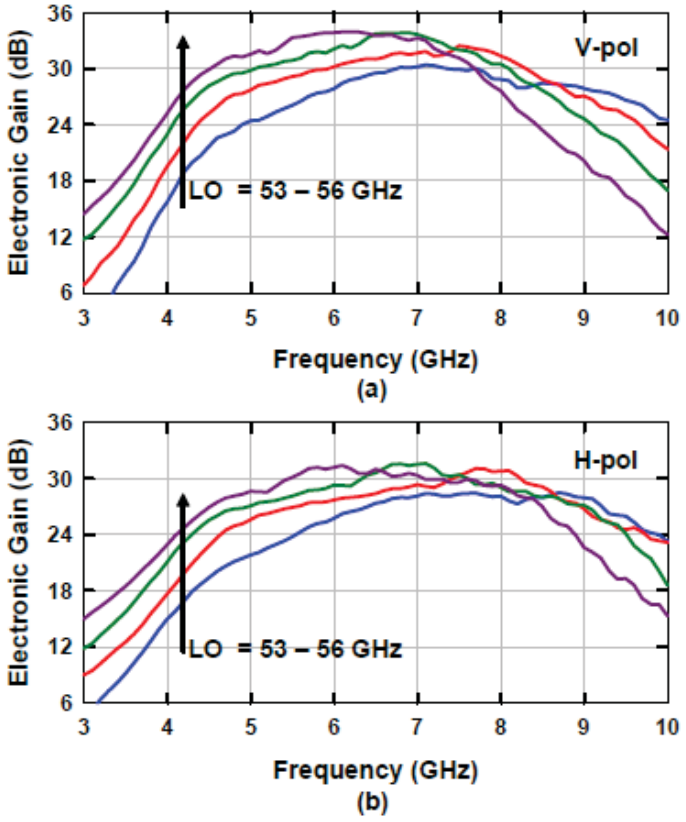



**Figure 25: Measured Electronic Gain vs IF at different LO Frequencies for (a) V-polarization and (b) H-polarization**

Figure 26 presents the measured input $P_{1dB}$ of the 64-element array in the Rx mode and is referenced to the antenna aperture. As expected, the input $P_{1dB}$ increases from -56 dBm to -44 dBm if both of the LAs are backed-off.

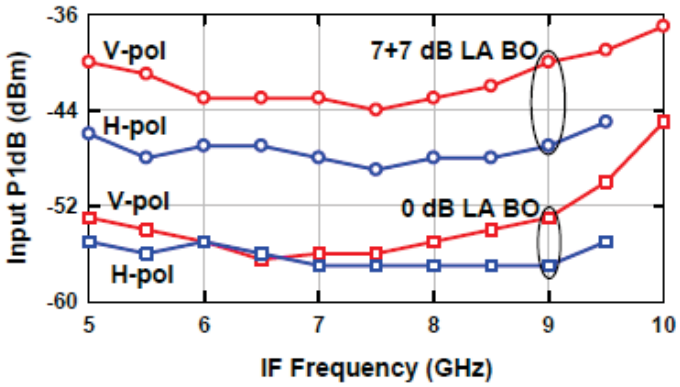



**Figure 26: Measured Input P1dB of the 64-element Array at LO = 55 GHz**

**Communication Link Measurements**

The 64-element wafer-scale phased-array is demonstrated in a 60 GHz communication link (Figure 27). A Keysight M8195A arbitrary waveform generator (AWG) is used at 7 GHz and is operated at 3-dB backoff from its peak output power for the best SNR (61 dB for 64-quadrature amplitude modulation (QAM) 100 MBaud/s). A variable attenuator is placed after the AWG to adjust the power delivered to the array. On the Rx side, a WR15 20 dB gain horn antenna with an E-band commercial amplifier is placed 1.25 m from the phased-array. Finally, the Keysight DSO-Z632A 63 GHz real-time scope running the VSA 89600 software is employed to demodulate the received signal. The E-band amplifier and variable attenuator are swapped when the array radiates an EIRP > 30 dBm so as not to saturate the amplifier. The error-vector magnitude (EVM) is measured using the equalizer function embedded in the VSA software so as to minimize the amplitude and phase variations caused by the measurement setup. EVM values reported in this paper are the rms values of the error vectors normalized to the constellation peak magnitude [34], [35].

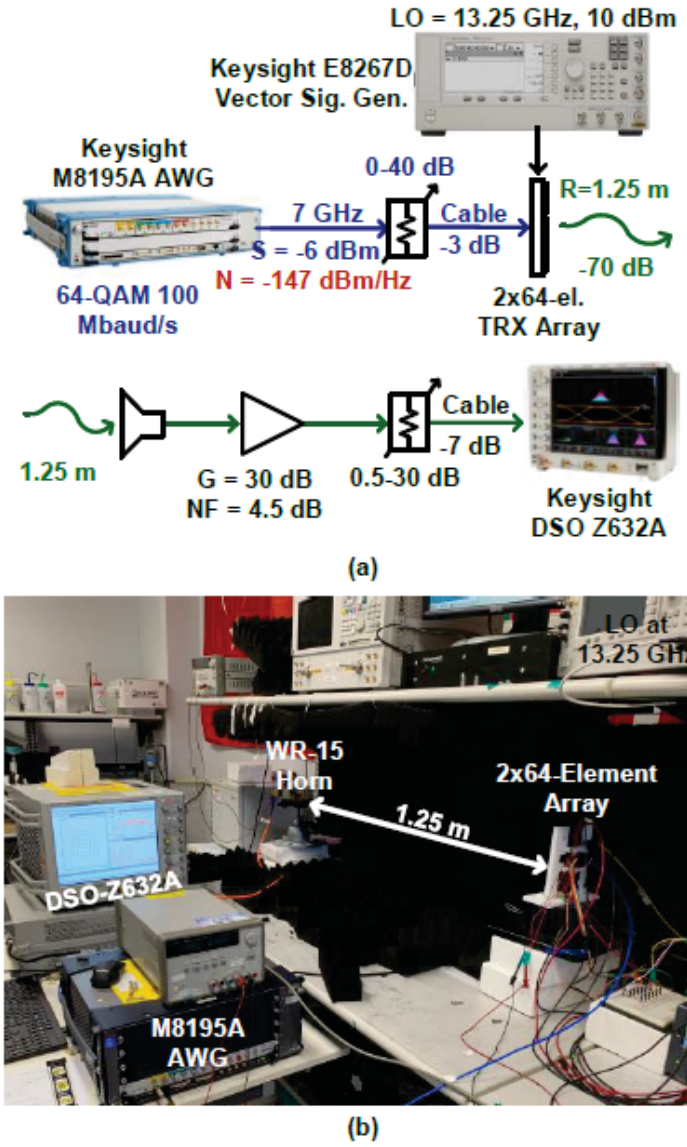



**Figure 27: (a) Measurement Setup for the 60 GHz Communication Link and (b) Photograph of the Measurement Setup**

Figure 28(a) presents the measured EVM values at different EIRP levels using a 64-QAM 100 MBaud/s waveform at 62 GHz. Since the peak-to-average power ratio (PAPR) is 7.7 dB after the root-raised-cosine filter with a roll-off factor of $\alpha = 0.35$ for a 64-QAM waveform, the EVM increases after 31 dBm EIRP which corresponds to 7-8 dB backoff from $P_{sat}$. The EVM remains <2% at 10-30 dBm EIRP. The dynamic range of the H-polarized array is lower by 3-4 dB in the SNR-limited region (A) due to its 203 dB lower electronic gain, and hence slightly elevated Tx noise. Also, it is degraded by 1-2 dB in the linearity-limited region (C) due to its slightly lower EIRP.

Selected constellations at different EIRP levels are shown for V-polarized array in Figure 28(b). In region A, the EVM is limited by the Tx noise that degrades the system SNR at low input power levels. In region B, the LO phase noise and digital storage oscilloscope (DSO) scope

clock jitter limit the EVM. In region C, the EVM is limited by the linearity of the Tx array, and the AM-AM distortion dominates the non-linearity.

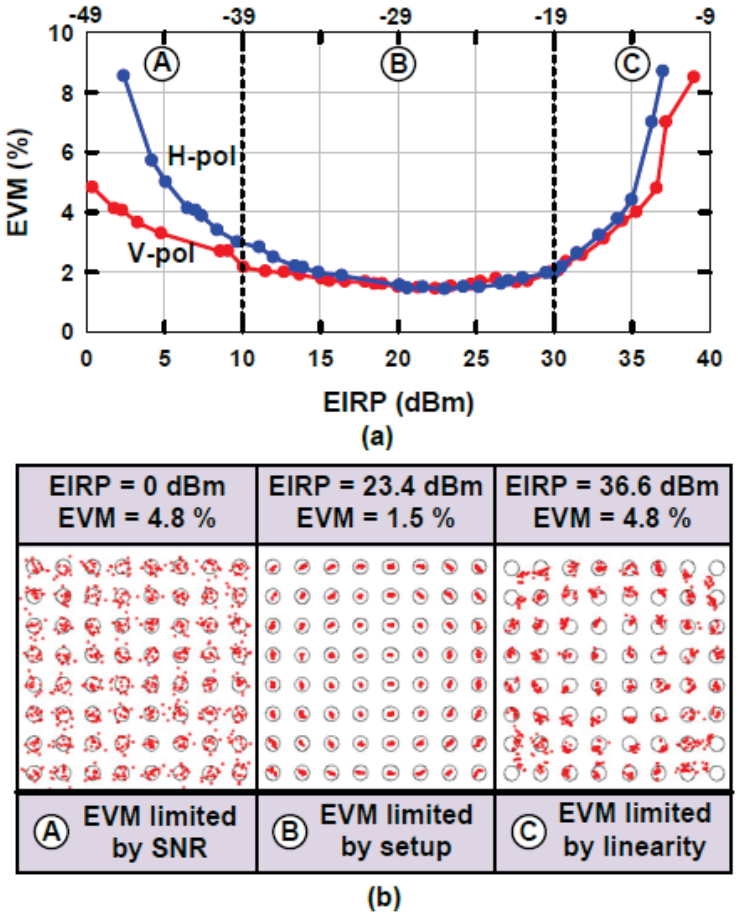



**Figure 28: (a) Measured EVM using 64-QAM 100 MBaud/s at 1.25 M vs different EIRP Levels at 62 GHz and (b) Selected Constellations for the V-polarized array at different EIRP Levels**

The measured QPSK, 16-QAM and 64-QAM constellations are shown in Figure 29 at different data-rates and scan-angles (H-plane) for V- and H-polarized arrays. For QPSK modulation, a data-rate of 7 Gbps is achieved with 12-15% EVM and no backoff from $EIRP_{sat}$ for both polarizations. A 16-QAM modulated waveform with $\alpha = 0.35$ and a PAPR of 6.6 dB shows an EVM of 6.5-9.5% with 16 Gbps and 12 Gbps data-rates for V- And H-polarized arrays, respectively, with 6.5 dB backoff from EIRP. The 64-QAM modulation with $\alpha = 0.35$ and a PAPR = 7.7 dB achieves 4.2 % EVM with 12 Gbps and 7.8 Gbps data-rates for V- and H-polarized arrays with 7-8 dB backoff from $EIRP_{sat}$. Finally, the 64-QAM 1 GBaud/s modulated signal is fed to the V-polarized array which is then electronically scanned to $\pm 50^{o}$ in the H-plane. The results also show that the EVM remains nearly constant over all scan angles.

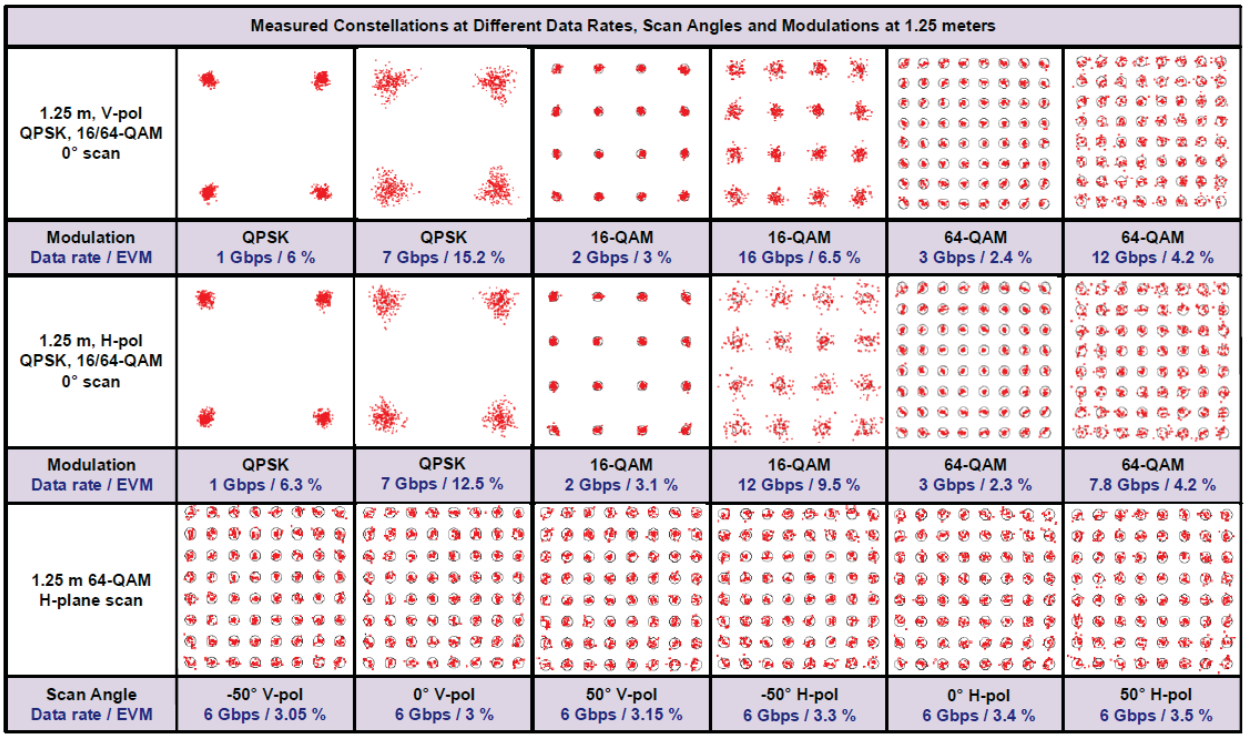



**Figure 29: Measured Constellations of V- and H-polarized 64-element Phased-array at different Data Rates, Modulations, and Scan Angles for a 1.25-m Data Link**

Figure 30 presents the measured EVM at different data rates and modulation schemes. Peak data-rates of 12-16 Gbps are achieved for both polarizations, and it is possible to build a communication link with 24-32 Gbps data-rate using the dual-polarized dual-beam wafer-scale phased-array. The measured EVM is also shown for both polarizations at all scan angles using a 64-QAM waveform at different symbol-rates (Figure 31). The EVM remains mostly constant for all scan angles.

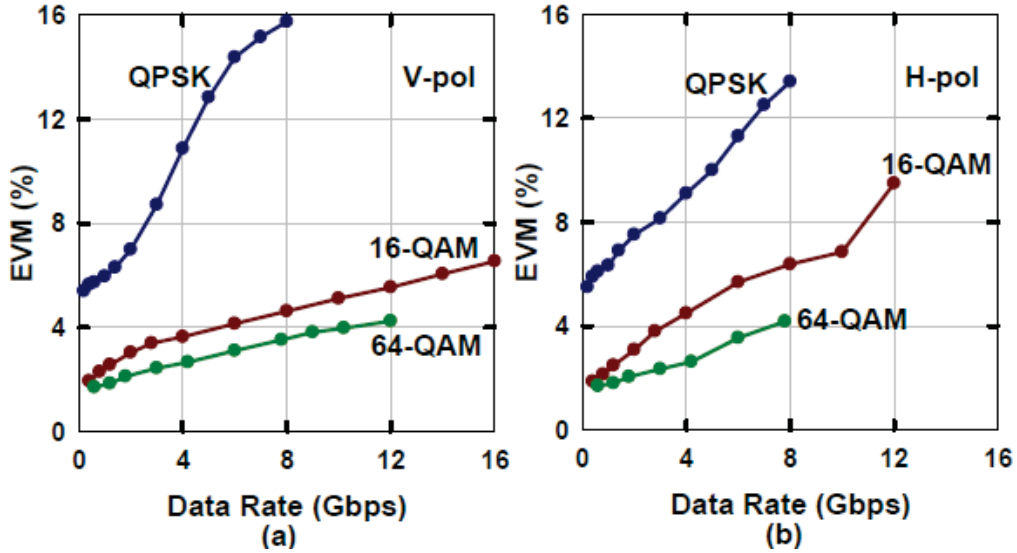



**Figure 30: Measured EVM of (a) V-polarized and (b) H-polarized 64-element Array at different Data Rates and Constellations**

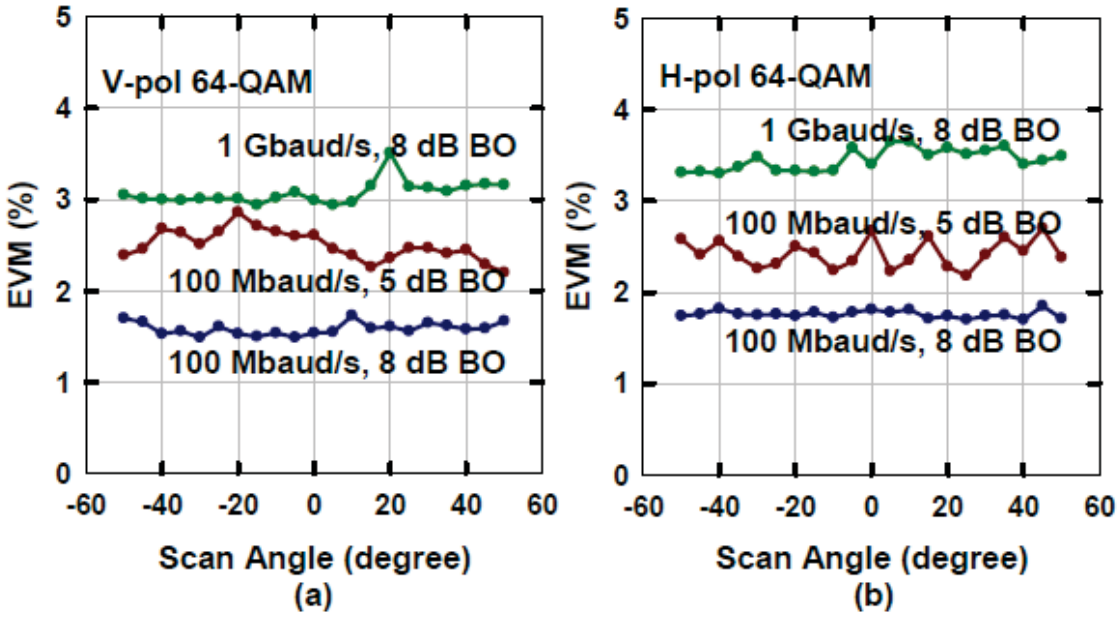



**Figure 31: Measured EVM of (a) V-polarized and (b) H-polarized 64-element Array at different Scan Angles using 64-QAM 0.1-1 GBaud/s 64-QAM at 5-8 dB Backoff**

**Noise, SNR, and EVM Analysis**

The EVM calculation consists of three components: 1) EVM due to SNR, 2) EVM due to real-time scope clock jitter and 3) EVM due to LO phase noise. In this section, each component is analyzed for the case of EIRP = 30 dBm and a 64-QAM 100 MBaud/s waveform with $\alpha = 0.35$ and PAPR = 7.7 dB at 62 GHz.

The Tx noise analysis for the 64-element phased-array is presented in Figure 32. The AWG has a wideband noise of -147 dBm/Hz at 7 GHz and is operated at $P_{out}$ = -6 dBm which results in an SNR of 61 dB at its output for a 100 MHz waveform. This waveform is then attenuated by 18 dB and includes the variable attenuator (10 dB), and losses due to the IF cable (-3 dB), PCB (-3 dB) and on-chip transmission lines and balun (-2 dB), and the SNR of 61 dB is maintained at the up-converter IF input (S = -24 dBm and N = -165 dBm/Hz). However, the up-converter has 9 dB NF (Figure 15(b)) and 5 dB gain. Considering the noise contribution from the blocks after the up-converter, the Tx system NF at the up-converter IF input is 17 dB and results in -157 dBm/Hz noise floor. The analysis, therefore, shows that the Tx noise of the 64-element phased-array limits the SNR at the array input and leads to an equivalent coherent noise floor of -156 dBm/Hz.

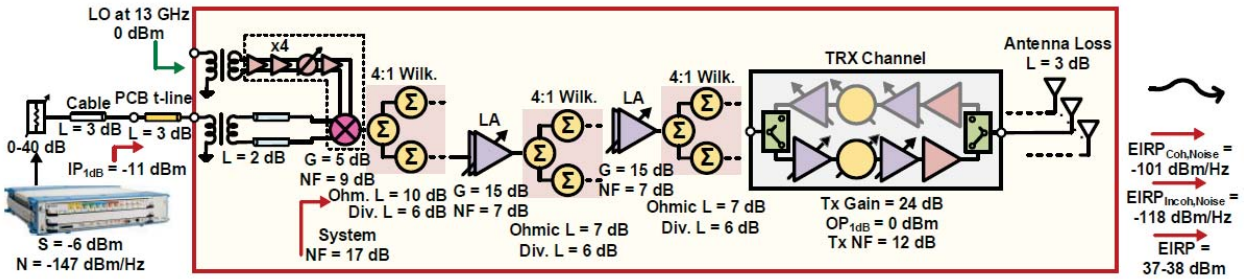



**Figure 32: Tx Noise Calculations for the 64-element Phased-array**

The up-converter noise passes through six Wilkinson di-viders and two LAs and appears at the Tx channel input as -163 dBm/Hz. Considering the Tx phased-array channel gain (24 dB), coherent addition from 64-elements (18 dB), directivity (23 dB), antenna efficiency (-3 dB) and on-chip feed line loss (-1 dB), the total coherent-noise EIRP can be calculated as:

$$EIRP_{cn} = -163 + 24 + 10log(64) + 23 - 3 = -101 \text{ dBm/Hz} \quad (4)$$

and $EIRP_{cn}$ = -21 dBm for a 100 MHz bandwidth. At EIRP-PAPR = 30 dBm, the radiated coherent SNR is therefore 51 dB. Note that, since this noise adds coherently, it is phase-shifted in each phased-array channel and has a pattern similar to the array pattern.

Additionally, the NF of each phased-array Tx channel is 12 dB and results in a noise of -162 dBm/Hz at the channel input. This noise is incoherent as it is generated by 64 independent TRX channels and therefore, it creates a noise pattern as a single radiating element with an EIRP calculated using:

$$EIRP_{icn} = -162 + G_{TRX} + 10log(64) + D_{ant} - 3 = -118 \text{ dBm/Hz} \quad (5)$$

where $G_{TRX}$ = 24 dB and $D_{ant}$ is the antenna directivity and is 5 dB. The incoherent-noise EIRP is 17 dB lower than the coherent-noise EIRP and can be neglected.

On the receive side, for EIRP = 30 dBm, a path loss of 70 dB and a horn gain of 20 dB, the average signal received at the horn is -20 dBm. After the E-band amplifier (30 dB gain) and the 17 dB loss due to the variable attenuator and RF cable (7 dB), an average signal of -14 dBm is available at the DSO scope input. The Tx noise radiated from the 64-element phased-array appears at the horn antenna as -151 dBm/Hz and is much larger than the E-band amplifier noise (NF of 4.5 dB). The received noise becomes -145 dBm/Hz at the DSO scope input. However, the DSO input equivalent noise is estimated to be -143 dBm/Hz referenced to its input (at this DSO gain setting), and therefore, the total equivalent noise is -141 dBm/Hz at the DSO scope input and resulting in 47 dB SNR for a 100 MBaud/s waveform. Therefore, for an EIRP = 30 dBm, the EVM contribution from the SNR is:

$$EVM_{\text{SNR}} = 100 * 10^{(-(SNR+PAPR)/20)} = 0.3\% \qquad (6)$$

where the PAPR is 3.7 dB without any filtering applied.

The EVM contribution due to the real-time scope clock jitter is calculated using $EVM_{jitter} = 2\pi f0*\tau*100*10^{-(PAPR)/20)}$ and is 1.9% where $f_0$ = 62 GHz, $\tau$ = 75 fs and PAPR = 3.7 dB [36]. Also, the integrated LO phase noise at 54 GHz from the transmitter contributes 0.72% to the EVM at 54 GHz. The total EVM is:

$$EVM_{\text{total}} = \sqrt{EVM_{SNR}^2 + EVM_{jitter}^2 + EVM_{LO}^2} = 2.05\% \quad (7)$$

and agrees well with the measured 2.04% EVM. The noise calculations for the Tx and Rx system as well as the SNR and EVM analysis are summarized in Table 2.

**Table 2. System Analysis for 2x64-Element Phased-Array**

| **Tx System Analysis** | |
|---|---|
| AWG average power (dBm) | -6 |
| Variable attenuator setting (dB) | -10 |
| Power at transceiver input (dBm) | -54 to -16 |
| Tx array NF at transceiver input (dB) | 17 |
| Tx channel NF (dB) | 12 |
| AWG noise floor (dBm/Hz) | -147 |
| Tx electronic gain (dB) | 12 |
| Total noise floor at transceiver input (dBm/Hz) | -156 |
| Noise floor at each antenna (dBm/Hz) | -139 |
| Coherent noise EIRP (dBm/Hz) | -101 |
| Incoherent noise EIRP (dBm/Hz) | -118 |
| Tx peak EIRP (dBm) | 37 |
| **Rx System Analysis** | |
| Path Loss (dB) | 70 |
| Horn Gain (dB) | 20 |
| Average signal power at horn (dBm) | -20 |
| Tx noise power at horn (dBm/Hz) | -151 |
| Rx amplifier gain (dB) | 30 |
| Rx amplifier noise figure (dB) | 4.5 |
| Waveguide Variable Attenuator Setting (dB) | -17 |
| DSO noise figure (dB) | 31 |
| Modulation | 64-QAM<br>100 Mbaud/s |
| Av. Signal power at DSO | -14 |
| Rx noise floor at DSO (dBm/Hz) | -143 |
| Tx noise floor at DSO (dBm/Hz) | -145 |
| Total noise at DSO integ. over 100 MHz | -61 |
| **SNR and EVM** | |
| SNR/EVM at DSO (dB)/(%) | 47/0.3 |
| EVM due to LO Phase Noise (%) | 0.72 |
| EVM due to DSO scope clock jitter (%) | 1.9 |
| Total EVM for 64-QAM 100 Mbaud/s (%) | 2.05 |
| Meas. EVM for 64-QAM 100 Mbaud/s (%) | 2.04 |

## 2.11 256-Element Phased-Array Design: Reticle-to-Reticle Stitching

The new reticle stitching method aims to achieve an easier design flow compared to previous work, reduced cost per element, higher yield without additional precautions and redundancies and true wafer-scale design where an entire 8-inch wafer can be assembled as one large phased-array.

Previously, two stitching methods have been proposed: sub-reticle stitching and full-reticle stitching [4]. The first method relies on discrete building blocks (sub-fields) which are smaller than a full-reticle size. Only one subfield is exposed at a time where the other parts of the reticle are darkened, and this is repeated as many times that this subfield is used. This method suffers from a large number of additional fabrication steps and can lower the wafer yield. Also, the shape and size of the phased-array are predetermined in which it is only possible to extract a single design (64-, 256- or 1024-element) per fabrication. The second method is based on fabricating the full reticle up to M1, and then M1-M7 are stitched together using special masks so as to connect digital, bias and RF pads between different reticles. Although, this method requires less fabrication steps than the sub-reticle stitching method, it still requires stitching masks and can result in lower yields.

The proposed reticle-to-reticle bondwire stitching method is presented in Figure 33 using a 256-element phased-array as an example with no additional fabrication steps required. Strategically placed bonding-pads allow stitching between reticles using only bondwires for IF and LO signals. In order to distribute the IF and LO signals equally to each reticle, an H-tree distribution network is adopted, and therefore, a new signal path is defined for the 256-element array. The IF and LO are fed using the pads at the South-West corner of the first reticle, divided/combined using the IF and LO splitter distribution network whose loss is compensated using line amplifiers. The distributed signals are then fed to the up/down converters located at Mid-East of the first and third reticles and Mid-West of the second and fourth reticles. Note that, the 256-element phased-array has 7 redundant IF and LO input/output pads, and if one of the blocks in the stitching path fails, it can be bypassed using the redundant bond-pads. In this work, only the IF and LO pads between reticles are stitched, but it is also possible to stitch vdd and ground pads as well as the digital control pads to build a true wafer-scale phased-array.

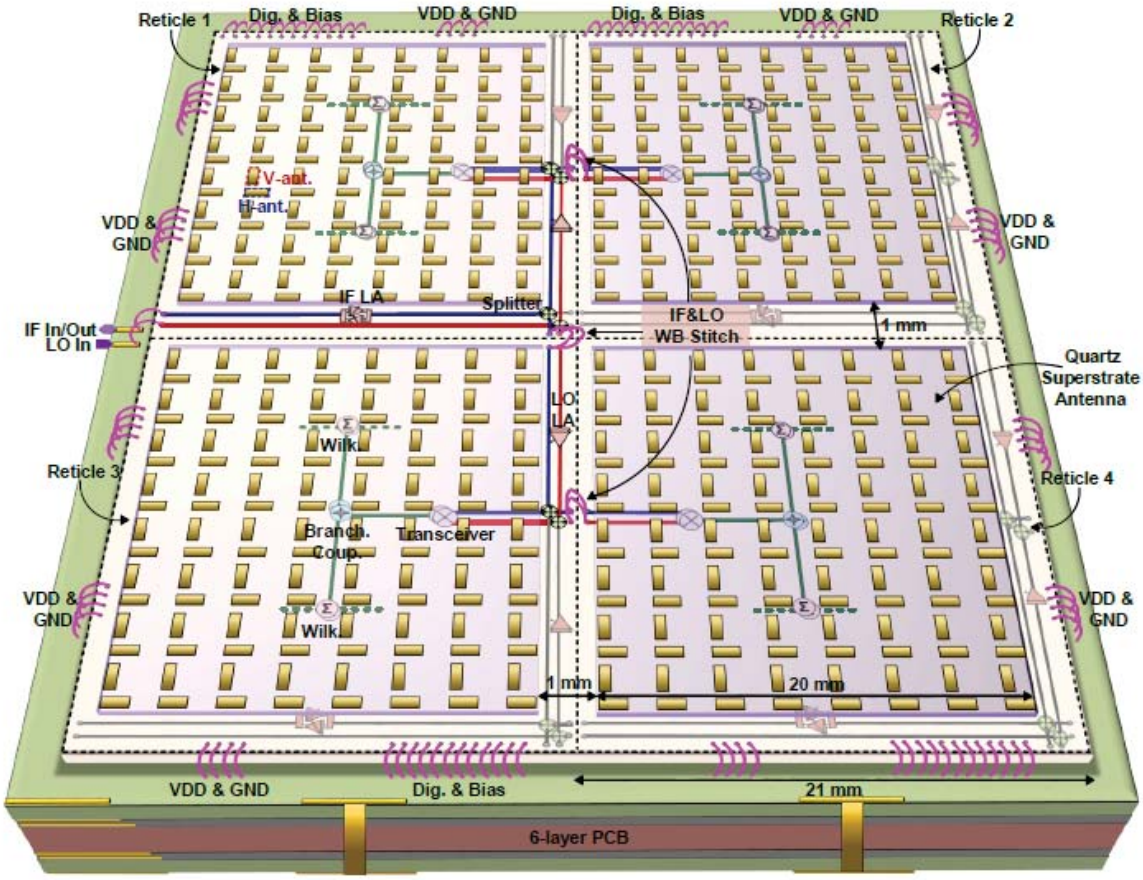



**Figure 33: Block Diagram of the Bondwire-stitched 256-element Transmit/receive, Dual-polarized, Dual-beam Phased-array with Integrated Dual-transceivers and Quartz Superstrate Antennas**

*Shaded (gray) circuitry is not used.*

The stitching path distribution loss consists of 35 mm transmission line (loss = 0.09 dB/mm at 8 GHz), two IF splitters (21 dB loss) and an IF LA (20 dB gain at 8 GHz). The total gain in the IF stitching path becomes -4 dB from the array input port to the up/down converter inputs including the division loss. Similarly, the LO signal passes through 35 mm transmission line (loss = 0.14 dB/mm at 13 GHz), a resistive polarization divider (-6 dB), two LO splitters (-22 dB) and an LO LA (24 dB gain and 11 dBm output $P_{1dB}$ at 13 GHz). The required LO power for the up/down converter is -10 dBm, and hence, the required output power from the LO line amplifier is 7.5 dBm (7.5 dBm - 11 dB - 6 dB = -10 dBm). Following the H-tree, one can find that the required LO input power for the 256-element phased-array at the South-West port is 0 dBm.

Note that in Figure 33, each reticle accesses the IF and LO signals after different number of stitching zones which contain two baluns and two GSG pads. For example, while the first reticle has IF and LO access with no stitching zones, the fourth reticle experiences 10 dB less distribution gain due to two stitching zones. It is possible to actually feed the IF and LO to each reticle independently using an external PCB distribution network, but this can only be done for a

2xN phased-array (N = 64-element reticle) where access to the pads is available from the top and bottom sides of the reticle. If an NxN array is required, then stitching between the elements is mandatory for the inner reticles.

## 2.11 256-Element Phased-Array System Measurements

An 8-inch SiGe BiCMOS results in twelve 256-element super-reticles assuming 100% yield. However, the yield tests presented in Section 2.9 provided the locations of the functional reticles, and consequently, the sample wafer is diced to obtain nine functional super-reticles (256-element) and ten functional regular reticles (64-elements), reaching A88% yield. The 256-element phased-array super-reticle is shown in Figure 34(a) and occupies 42x42 $mm^2$. The expanded view of the super-reticle is presented in Figure 34(b) and shows the IF and LO bondwire stitching zones along with the stitching path sub-blocks.

The 256-element phased-array is placed on a 6-layer 370HR PCB, and is bonded for vdd, ground, digital control, IF and LO on the edges. In addition, the IF and LO pads are bonded reticle-to-reticle to form a super-reticle. Four separate 100-µm thick quartz superstrate antennas (20x20 $mm^2$) are attached on each reticle, leaving 1 mm space between reticles for bonding. The assembled 256-element super-reticle chip and PCB are shown in Figure 34(c) and (d). Four separate heat-sinks are glued on the back side of the PCB using thermally conductive epoxy, and a small fan is placed on the heat sinks for better heat removal (not shown). The chip temperature stabilizes at 50°C, and it is possible to further reduce the temperature if copper-filled vias are used under the chip instead of copper-plated vias.

The 256-element phased-array is biased at 2.6 V and consumes 18.4 A and 15.6 A in the Tx and Rx modes per polarization. In this case, the IR drop creates a small problem since only two edges of each reticle have access to the PCB, and therefore, only half the number of vdd and ground pads could be bonded per reticle. This can be solved by either bonding vdd and ground pads reticle-to-reticle or a flip-chip design that has additional vdd and ground bumps which are distributed uniformly inside a reticle.

The measurement setup is similar to 64-element phased-array except the distance between the 256-element array and the horn antenna is increased to 1.1 m. The far-field range is calculated as $2D2/\lambda = 0.7$ m. Since each reticle experiences different IF loss in the stitching path, the reticle gains are adjusted to be within ±3 dB from each other. Also, the phases of the four reticles are aligned using the phase shifters in the LO multiplier chain. The phase-aligned reticles do not drift due to temperature. The 256-element array stabilizes at the same temperature as the 64-element array (50°C) since the power density remains constant as the reticles are powered on.

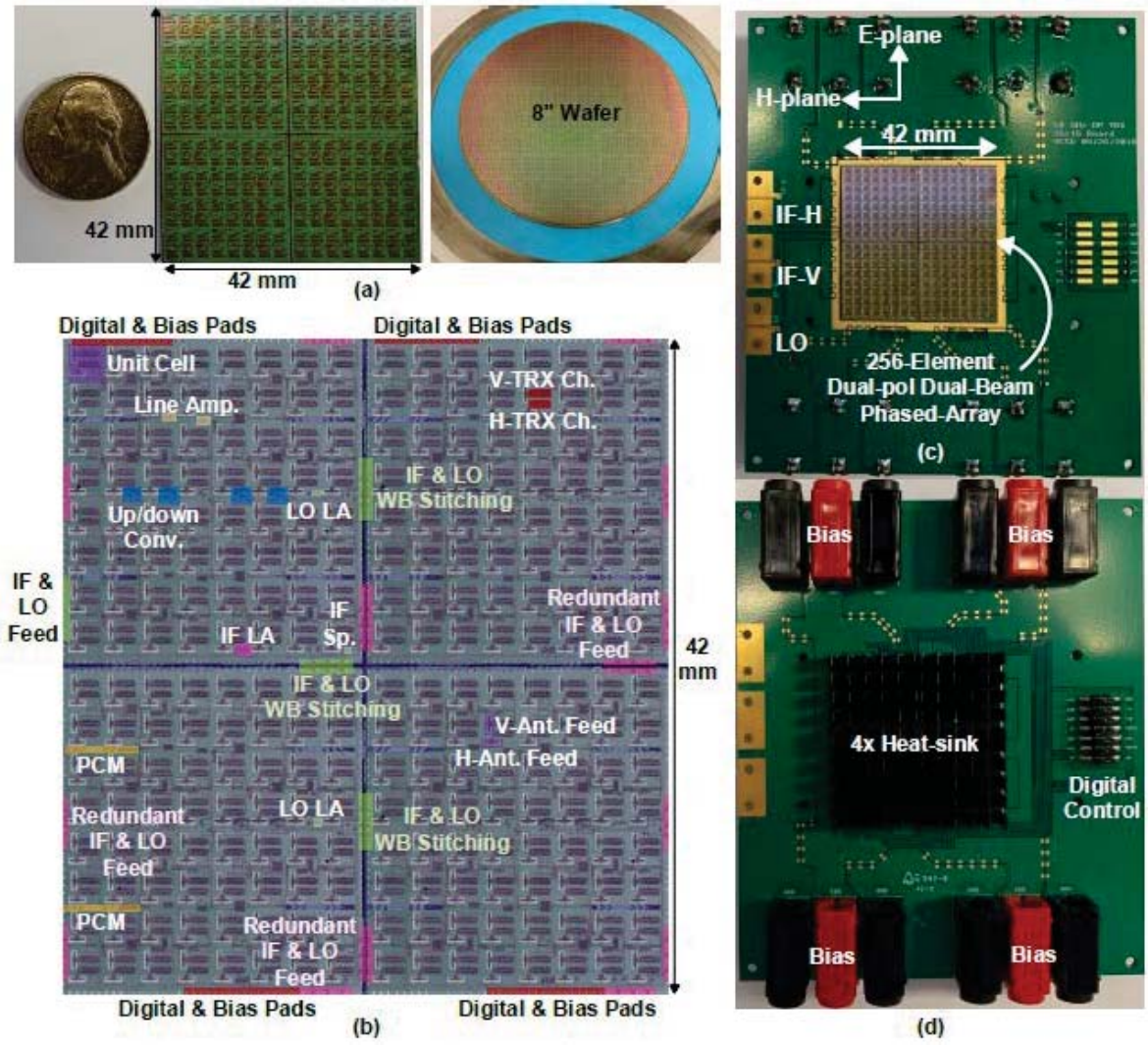



**Figure 34: (a) Picture of the 256-element Phased-array Chip with a Quartz Superstrate Antenna and as delivered on an 8-inch Wafer; (b) Expanded View of the 256-element Wafer-scale Phased-array with Bondwire Stitching-zones labeled; (c) Front and; (d) Back Views of the assembled 256-element Phased-array Board**

The measured broadside and scanned patterns in the H-plane at 62 GHz are shown in Figure 35. The broadside patterns agree well with the ideal pattern and show sidelobe levels <-12 dB and a 3-dB beamwidth of 6º. The array scans to ±50º with no grating lobes and the sidelobe levels remain <-10 dB over all scan angles. The elevated sidelobes are partly due to the 1-mm gap between the quartz superstrate antenna arrays, and partly due to the IR drop across four reticles. The center elements of the phased-array is fed with 0.2 V less voltage due to the IR drop, and therefore the edge elements have higher gain than the center elements (by 4-5 dB). This can easily be corrected by gain control (not done). The patterns of the H-polarized array in the Tx mode are similar to the patterns in the Rx mode and not shown.

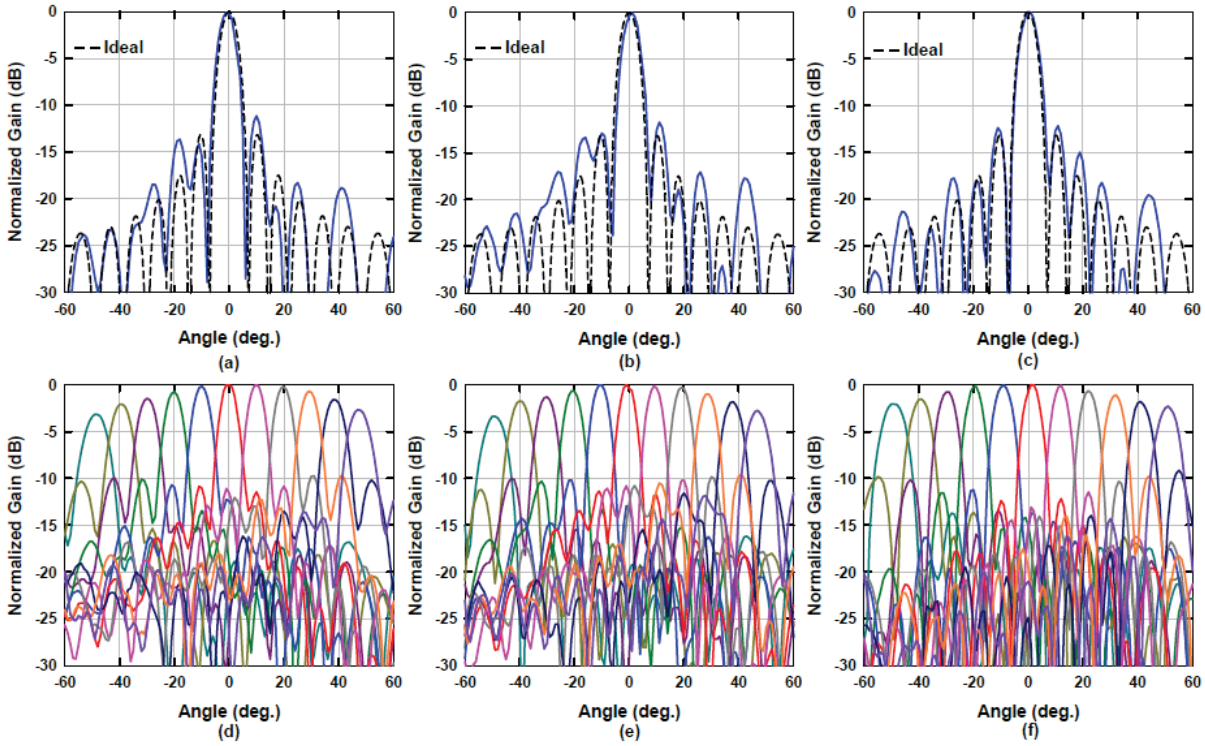



**Figure 35: Measured Broadside Patterns in the H-plane at 62 GHz**
*(a) V-polarization in the Rx Mode, (b) V-polarization in the Tx Mode, (c) H-polarization in the Rx Mode, and Measured Patterns vs Scan Angle for (d) V-polarization in the Rx Mode, (e) V-polarization in the Tx Mode, (f) H-polarization in the Rx Mode*

The measured E-plane broadside and scanned patterns at 62 GHz are presented in Figure 36. The sidelobe levels remain <-10 dB at broadside and over all scan angles. The 3-dB beamwidth is 6º at broadside. Similarly, the phased-array scans to ±50º with no grating lobes. The patterns of the H-polarized array in the Rx mode are similar to the patterns in the Tx mode, and not shown. The peak of both E- and H-plane patterns follow the simulated element factor (cos($\theta$)). The measurements at 61-63 GHz resulted in similar patterns and are not shown due to brevity.

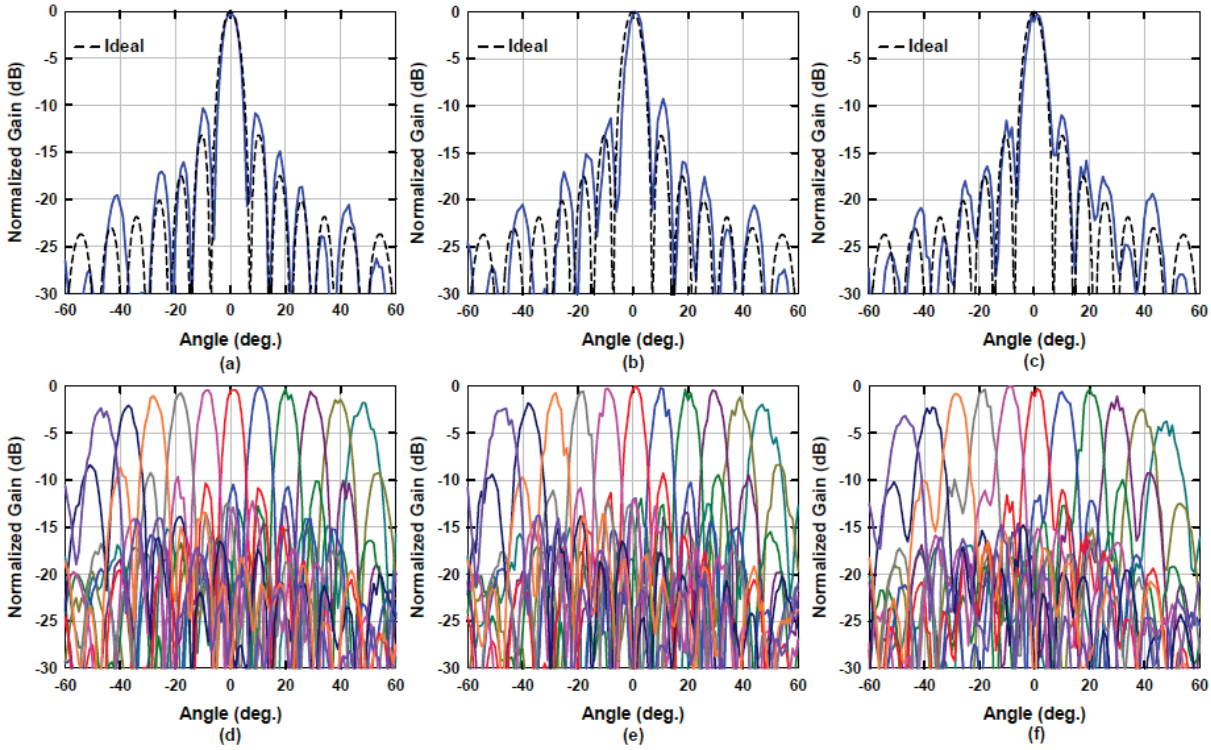



**Figure 36: Measured Broadside Patterns in the E-plane at 62 GHz**

*(a) V-polarization in the Rx Mode, (b) V-polarization in the Tx Mode, (c) H-polarization in the Tx Mode, and Measured Patterns vs Scan Angle for (d) V-polarization in the Rx Mode, (e) V-polarization in the Tx Mode, (f) H-polarization in the Tx Mode*

The measured saturated EIRP is 44 dBm and 42 dBm for V- and H-polarized arrays, respectively (Figure 37) while the simulated peak EIRP is 50 dBm for V- and 49 dBm for H-polarized arrays. The difference between simulations and measurements stems from the insufficient output power of the IF LA located in South-Center in reticle 1 (Figure 33). The IF LA has an output P1dB of 4 dBm at 8 GHz and is followed by 24 dB routing loss in the Tx mode, resulting in -20 dBm at the up-converter input. However, the IF input power required to drive the up-converters is -13 dBm (for $P_{sat}$) which explains the 6-dB decrease in the EIRP. This can be corrected by using one of the seven redundant IF and LO pins which bypasses the IF LA at a cost of abandoning the H-tree distribution network and using an external IF and LO feed network on the PCB (not done in this work).

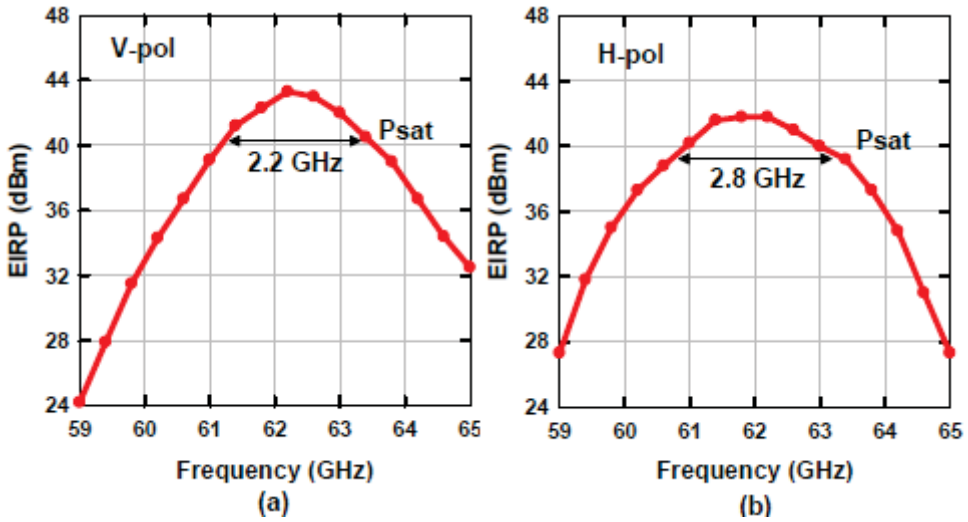



**Figure 37: Measured Saturated EIRP vs Frequency of the (a) V-polarized and (b) H-polarized 256-element Phased-array**

Table 3 summarizes the 64- and 256-element wafer-scale phased-array performance and provides a comparison with prior art.

**Table 3. Performance Comparison of the Phased-Array Transceivers**

| | This work | | Zihir '16 [4] | | Broadcom '14 [2] | Intel '13 [35] | IBM '10 [23] | Bell Labs '18 [1] | Broadcom '18 [38][2] |
|---|---|---|---|---|---|---|---|---|---|
| Process | 0.18 µm SiGe BiCMOS | | 0.18 µm SiGe BiCMOS | | 40 nm CMOS | 90 nm CMOS | 0.12 µm SiGe BiCMOS | 0.18 µm SiGe BiCMOS | 28 nm CMOS |
| Frequency (GHz) | 60-64 | | 60.5-62.5 | | 57-66 | 57-62 | 58-65 | 70-100 | 57-66 |
| IC integration level | RF front-end + RF/IF conversion | | RF front-end | | MAC/PHY/TRX w/PCIe interface | RF front-end + RF/IF conversion | RF front-end + Superhet. Conv. | RF front-end + PLL +RF/IF conversion | MAC/PHY/TRX w/PCIe interface |
| Number of elements | 2x64 TRX | 2x256 TRX | 64 TX | 256 TX | 16 TRX | 32 TRX | 16 TX | 16 TRX | 144 TRX |
| Polarization | Dual | Dual | Single | Single | Single | Single | Single | Dual | Single |
| Total Si area ($mm^2$) | 441 | 1764 | 471 | 1738 | 32.5 | 29 | 43.9 | 24.5 | 292 |
| Tx $OP_{1dB}$ / el. (dBm) | 0 | 0 | 0 | 0 | 0 | -3.5 | 9-13.5 | 8 ($P_{sat}$) | 0.8 |
| Rx NF (dB) | 8-10[1] | 8-10[1] | – | – | <10 | <9 | - | 6.5-10 | 6.5 |
| Rx & Tx gain control (dB) | 50 / 40 | 60 / 50 | - / 9 | - / 9 | 10 / - | - | - / 40 | 15 / - | - |
| EIRP at $P_{sat}$ (dBm) | 38 | 44 | 38 | 45 | 27 | 32 | 42 | 34 | 51 |
| E- / H-plane scan (°) | ±50 / ± 50 | ±50 / ± 50 | ±50 / ± 50 | ±50 / ± 50 | ±50 / ± 50 | ±30 / ± 30 | ±45 | ±30 / ± 30 | ±10 / ± 60 |
| E- / H-plane 3-dB beamwidth (°) | 12° / 12° | 6° / 6° | 12° / 12° | 6° / 6° | Not specified | Not specified | Not specified | 30° / 30° | - |
| Side-lobe level (dB) | < -12 | < -10 | < -12 | < -10 | < -10 | <-10 | < -10 | < -10 | < -10 |
| Rx / Tx Power Cons. (W) | 7.9 / 9.4 | 40.5 / 48 | - / 8 | - / 32 | 0.96 / 1.2 | 0.85 / 1.2 | - / 4 | 0.625 / el. | 6.6/8.4 (@ P1dB) |
| Antenna Substrate | Quartz | | Quartz | | Organic | LTCC | Organic | Organic | LTCC |
| Over-the-air data rate | 12-16 Gbps / pol. 16-QAM @ 1.3 m<br>8-12 Gbps / pol. 64-QAM @ 1.3 m | | 4 Gbps 16-QAM @ 4 m<br>2 Gbps QPSK @ 30 m | | 4.6 Gbps 16-QAM @ 10 m<br>3 Gbps 16-QAM @ 20 m | 16-QAM | 16-QAM Single Car. and OFDM 5.3 Gbps | 30 Gbps / pol. 64-QAM @ 1 m<br>20 Gbps / pol. 32-QAM @ 5 m | 4.6 Gbps 16-QAM |

[1]Simulated

[2]The paper has the following deficiencies: No bandwidth measurements in Tx and Rx modes to claim 57-66 GHz bandwidth. Neither the measured patterns for 144-elemen array nor the measured EIRP versus frequency are reported. The calculated $EIRP_{sat} = 20\log(N) + G_{ant} + P_{el,sat} = 49.6$ dBm, where N = 144, $G_{ant} = 1.5$ dB and $P_{el,sat} = 5$ dBm does not agree with the reported $EIRP_{sat}$ of 51 dBm. Also, the power consumption is reported at $P_{1dB}$ while the EIRP is reported at $P_{sat}$. The paper claims PA, LNA and Tx IF VGA have gain control, but no measurements are shown and no values are reported. Therefore, it is not clear if the 144-element array works well; however, the paper is cited for completeness.

## 2.12 Conclusion

This paper presented 60 GHz 2x64- and 2x256-element dual-polarized dual-beam wafer-scale phased-array transceivers. A single reticle is built to host the 2x64-element phased-array with dual up/down converters. Four identical reticles are then stitched together in the IF and LO domains to form a super-reticle that hosts a 2x256-element phased-array. The 64- and 256-element phased-arrays scan to ±50° with sidelobe levels <-12 dB and <-10 dB, respectively. The 64-element phased-array achieves 37-38 dBm saturated EIRP while the 256-element phased-array achieves 44 dBm due to limited power at the IF LA output. Future work includes bypassing the IF LA to be able to saturate the array to its $EIRP_{sat}$, using a flip-chip design to achieve better heat management and to minimize the IR drop, and building a 1024-element dual-polarized dual-beam array for long-range MIMO applications. To our knowledge, this work has demonstrated the most complex phased-array to-date at 62 GHz with dual-beam and dual-polarization capabilities.

## 2.13 Acknowledgment

The authors would like to thank Dr. Qian Ma at the University of California, San Diego for technical discussions, Arjun Karroy, Ed Preisler, Michael Scott, and Dave Howard at TowerJazz Semiconductor for their support and feedback. The antennas were printed on a quartz superstrate at the San Diego Nanotechnology Infrastructure (SDNI) of UCSD, a member of the National Nanotechnology Coordinated Infrastructure (NNCI), which is supported by the National Science Foundation (Grant ECCS-1542148).

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# List of Symbols, Abbreviations, and Acronyms

| ACRONYM | DESCRIPTION |
|---|---|
| ADC | analog-to-digital |
| AWG | arbitrary waveform generator |
| BC | branchline coupler |
| BJT | bipolar junction transistor |
| CG | common-gate |
| CMRR | common-mode rejection ratio |
| CS | common-source |
| DAC | digital-to-analog |
| DARPA | Defense Advanced Research Projects Agency |
| DC | direct current |
| DoD | Department of Defense |
| DSO | digital storage oscilloscope |
| EIRP | equivalent isotropically radiated power |
| EM | electromagnetically |
| ESD | electro-static discharge |
| EVM | error-vector magnitude |
| HRR | harmonic rejection ratio |
| IC | integrated circuit |
| IEEE MTT | Institute of Electrical and Electronics Engineers Microwave Theory and Techniques |
| IF | intermediate-frequency |
| IP3 | third-order intercept point |
| IR | infrared |
| LA | line amplifier |
| LNA | low-noise amplifier |
| LO | local-oscillator |
| LTCC | low temperature co-fired ceramic |
| MIMO | multiple-input multiple output |
| NNCI | National Nanotechnology Coordinated Infrastructure |
| OTA | over-the-air |
| PA | power amplifier |
| PAE | power-added efficiency |
| PCB | printed circuit board |
| PLL | phase-locked loop |
| PTAT | proportional-to-absolute-temperature |
| QAM | quadrature amplitude modulation |
| QPSK | quadrature phase-shift keying |
| RF | radio frequency |
| rms | root mean square |
| Rx | receive |
| SDNI | San Diego Nanotechnology Infrastructure |
| SNR | signal-to-noise-ratio |
| SPDT | single-pole double-throw |

| ACRONYM | DESCRIPTION |
|---|---|
| SPI | serial-peripheral interface |
| TRX | transmit/receive |
| Tx | transmit |
| VGA | variable gain amplifier |
| VM | vector modulator |